

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., AND
SAMSUNG AUSTIN SEMICONDUCTOR, LLC
Petitioner

v.

HOME SEMICONDUCTOR CORPORATION
Patent Owner

IPR2015-00460
Patent 6,146,997

**PETITIONER'S REPLY TO
PATENT OWNER'S RESPONSE**

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TABLE OF AUTHORITIES

Case Law

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EXHIBIT LIST

SAM-1001	U.S. Patent Number 6,146,997 to Liu et al. (“the ’997 Patent”)
SAM-1002	Excerpts from the Prosecution History of the ’997 Patent (“the Prosecution History”)
SAM-1003	Declaration of Dr. Gary W. Rubloff
SAM-1004	Curriculum Vitae of Dr. Gary W. Rubloff
SAM-1005	U.S. Patent Number 6,277,720 to Doshi et al. (“Doshi”)
SAM-1006	U.S. Patent Number 5,770,498 to Becker et al. (“Becker”)
SAM-1007	Excerpts from Webster’s Third New International Dictionary (1986)
SAM-1008	U.S. Provisional Application No. 60/051,287 filed by Doshi et al. (“the ’287 Provisional”)
SAM-1009	“Process Induced Degradation of Thin Oxides” by Wong et al., Proc. 1st Int. Symp. Ultra Large Scale Integration Sci. Technol. (1987) (“Wong”)
SAM-1010	U.S. District Court District of Delaware (Wilmington) CIVIL DOCKET FOR CASE #: 1:13-cv-02033-RGA
SAM-1011	Second Declaration of Dr. Gary W. Rubloff
SAM-1012	Deposition Transcript of Mr. Ron Maltiel Vol. 1, November 9, 2015
SAM-1013	Deposition Transcript of Mr. Ron Maltiel Vol. 2, November 10, 2015

SAM-1014 Excerpts from “VLSI Handbook” by Einspruch (“Einspruch”)

I. INTRODUCTION

The Board should find claims 1–14 of the '997 patent as unpatentable in a Final Written Decision. HSC's arguments should be rejected because, contrary to the very definition of an anisotropic etch, HSC argues that a *highly anisotropic etch* in Doshi would somehow clear all of the silicon nitride layer deposited on the sidewall of the gate electrode, thereby preventing a spacer from being formed by the etch. Paper 18, pp. 16-24. Interpreting Doshi as disclosing a complete removal of the silicon nitride layer using a highly anisotropic etch is inconsistent with Doshi's teachings because a POSITA would have known that applying an etch in this proposed manner introduces the risk of damage to the very portions of the circuitry that Doshi explicitly seeks to protect. Moreover, HSC's reliance on Fig. 3k in support of this assertion should also be rejected, as Fig. 3k fails to show a self-aligned contact hole, making Fig. 3k either irrelevant or erroneous. HSC also argues that a spacer cannot be formed if it pre-exists the anisotropic etch. Paper 18, pp. 22-24. HSC's argument should be rejected because the inquiry is not whether a spacer already exists prior to the application of an anisotropic etch, but the inquiry is instead simply whether the anisotropic etch forms a spacer.

HSC further argues that Doshi does not disclose "forming an oxide layer over the diffusion region." HSC's proposed construction for the term "over"

should be rejected as it is too narrow. Moreover, even if HSC's construction were adopted, Doshi still discloses forming an oxide layer over the diffusion region, as an oxide layer covering the diffusion region is exposed to further oxide formation.

II. CLAIM CONSTRUCTION

A. "spacer"

Petitioner has proposed construction for the term "spacer" as broad enough to encompass "a structure that spaces between two conductive structures." Paper 1, pp. 9-10. In the Institution Decision, the Board determined that this term does not require express construction. Paper 11, p.8. HSC proposes that this term should be construed as "a structure *designed* to create physical separation between conducting structures". Paper 18, p.7 (emphasis added). According to HSC, "a spacer is a structure that is *purposefully designed* into the fabrication process to achieve specific functions", and HSC also advances that Petitioner's proposed construction is unreasonably broad because it would include "any material that spaces, even if *unintentionally* formed and without a defined function". *Id.*, p. 8 (emphasis added). Below, each of HSC's arguments is debunked.

HSC's construction should be rejected because it makes the touchstone of whether a structure is a spacer turn on a state of mind, i.e., intent, of a process designer, which is improper. *See Rowpar Pharm. Inc. v. Lornamead Inc.*, 2014 WL 1259777, at 9 (D. Ariz. Mar. 25, 2014) (Court rejected the words "desired effect"

in a proposed construction as being “ambiguous” and as appearing “to focus on the **intent** of the manufacturer or users of the accused product” (emphasis added).); *see also Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1353 (Fed.Cir.2001) (“We are not prepared to assign a meaning to a patent claim that depends on the **state of mind** of the accused infringer.”) (Emphasis added). That is, HSC contends that, if the process designer intended a structure to achieve the function of creating physical separation between conducting structures, then the structure is designed for the purpose of creating space and, therefore, is a spacer. Perhaps more problematic, in stark and yet indefensible contrast, if the process designer did not intend a structure to achieve the function of creating physical separation between conducting structures then the structure is not designed for the purpose of creating space and, therefore, is not a spacer **even if** the structure actually creates physical separation between conducting structures and otherwise is not physically different from the structure intended by the designer to create space.

Such a proposal introduces various problems. First and foremost, how is a third party to discover infringement? Unreliable and subjective examination of a state of mind cannot delineate an infringer from a non-infringer, just as it cannot serve as the sole basis for discerning whether a claim distinguishes the prior art, as HSC advances. Indeed, this problem is exacerbated by comparison against prior

art, as the intent of a prior art author is too often altogether unknown/undiscernible.

Similarly, what happens if a process designer designed the structure to serve a purpose other than creating space but only later realizes or acknowledges that the structure also has the advantage of creating space between one conducting structure and another? According to HSC's definition, such a structure would not be "purposefully designed" to create space and, therefore, would not be a spacer. Conversely, what happens if a process designer purposefully designed a structure to be a spacer but it is later found that the structure does not, in fact, create physical separation between conducting structures? According to HSC's proposal, this structure would still be a "spacer." This is akin to asserting that a machine is, in fact, a perpetual motion machine simply because it was purposefully designed to achieve perpetual motion by a designer who was blissfully unaware that no machine is capable of achieving perpetual motion because such motion violates the laws of physics.

Thus, by introducing the notion of whether something is or is not "designed", HSC's definition does not clarify, but rather obfuscates the meaning of "spacer." In contrast, Petitioner's construction provides clarity by offering an objectively verifiable definition of "spacer" that turns on whether a structure

achieves a separation between conductive structures, without being subject to the unreliable and often undiscernible intent of a designer.

Moreover, Petitioner's construction is otherwise reasonable under BRI. That is, the '997 patent supports a reading that a spacer is a structure that introduces space between conductors but provides no express limiting language imposing the additional or alternative requirement that the structure be "designed to" achieve this function. Moreover, as pointed out in the Petition, Merriam Webster's Dictionary defines the word "spacer" simply as "one that spaces." Paper 1, p. 9; Ex. 1007, p. 6. Accordingly, HSC's proposed construction should be rejected.

B. "forming an oxide layer over the diffusion region"

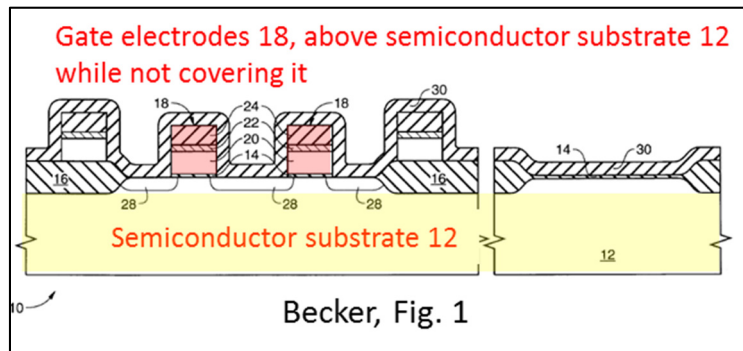
Petitioner has proposed a construction for this term as being broad enough to encompass "forming an oxide layer above the diffusion region." Paper 1, pp. 7-9. In the Institution Decision, the Board determined that this term does not require express construction. Paper 11, p.8. Thereafter, HSC proposes construing the term "forming an oxide layer over the diffusion region" to be "forming an oxide layer covering the diffusion region," while footnoting that "[c]overing, in this context, does not mean that there cannot be structures in between." Paper 18, pp. 8-10. HSC criticizes Petitioner's proposed construction as too broad, contending that Petitioner's use of "above" would be broad enough to include cases where an oxide

layer does not cover the diffusion region, and complaining that such breadth is unsupported by the '997 patent. *Id.*, p. 11.

At the outset, HSC's construction is too narrow and should be rejected. Under BRI, "limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993); Paper 11, p. 7. If HSC had intended for its claim to be limited to "covering" the diffusion region, HSC could have chosen to recite "covering"; it did not. HSC instead chose greater breadth through its recitation of "over." And, in this proceeding, HSC chose to maintain that breadth, as it forewent amending. Thus, HSC should not now be afforded amendment by fiat. *See In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989) ("during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.")

Moreover, within the specification of the '997 patent, the term "over" is applied consistent with the Merriam Webster's Dictionary definition to reference items that are above each other, even when separated by an intermediary item. Paper 1, p. 8; Ex. 1007, p. 4. Petitioner's proposed construction is also consistent with other literatures in this technology field, as cited in the Petition and not refuted by HSC. For example, U.S. Patent No. 5,770,498 ("Becker") discloses "forming a gate electrode **over** a semiconductor substrate." Ex. 1006, Abstract

(emphasis added). It is unambiguously clear that Fig. 1 of Becker, reproduced below, shows that gate electrodes 18 do not cover the semiconductor substrate 12. Rather, the gate electrodes 18 are above the semiconductor substrate 12.



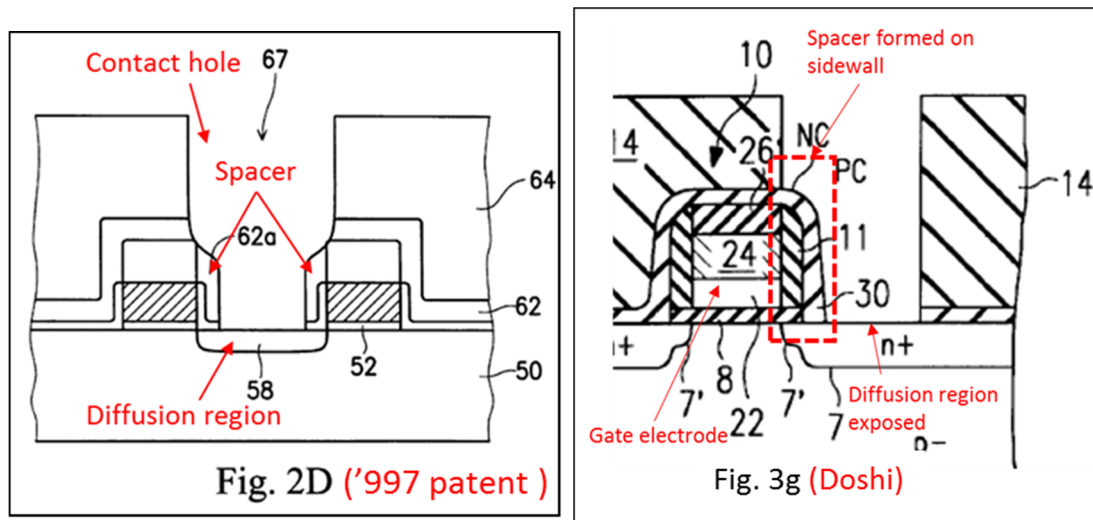
Lastly, there is no disclosure in the '997 patent that would cause a POSITA to depart from interpreting the term “over” as different from how it is commonly used in the art – i.e., as simply meaning “above.” Accordingly, Samsung's proposed construction is both reasonable and broader than HSC's proposed construction, and HSC's proposed construction should be rejected.

III. DOSHI ANTICIPATES CLAIMS 1-14

A. '997 Patent and Doshi

The '997 patent is directed to a method of forming a self-aligned contact hole. Ex. 1001, Abstract. According to the '997 patent, after gate electrodes 54, diffusion regions 58, a thermal oxide layer 60, and gate oxides 52 have been formed on a substrate 50, a conformal layer of silicon nitride 62 is deposited over the substrate surface. *Id.*, Fig. 2B, col. 2:48-67; Paper 1, p. 13. The silicon nitride 62 can have a thickness of about 100 to 500 Å. Ex. 1001, col. 2:65-67.

As shown in annotated Fig. 2D of the '997 patent (below), a planarized ILD insulating layer 64 is then formed over the conformal layer of silicon nitride 62, and a photoresist layer 66 is formed and patterned to expose a contact hole. Ex. 1001, col. 3:1-24; Paper 1, pp. 13-14. In this process, a highly selective first etch is performed to etch away the insulating layer 64. *Id.* The nitride layer 62 is then ***anisotropically*** etched to expose a portion of the diffusion region 58. Ex. 1001, col. 3:1-24; Paper 1, pp. 14-15. Due to the directionality of anisotropic etching, a portion of nitride layer 62 remains on the sidewall of the electrode 54 upon completion of the etch, thus forming spacer 62a. *Id.*



Doshi, in a same manner, discloses a method of fabricating self-aligned contacts. Ex. 1005, Abstract; Ex. 1003, ¶ A-1. In Doshi, after gate electrodes 10, diffusion regions 7/7', gate oxides 8, and sidewall filaments 11 have been formed on a substrate 2, a conformal layer of nitride layer 30 is deposited, followed by a

formation of a BPSG layer 14. Ex. 1005, Figs. 3a-3d, col. 7:29- col. 9:24; Paper 1, pp. 17-18. Notably, like the nitride 62 thickness of 100 Å to 500 Å used to form the spacer in the '997 patent, Doshi discloses that *the nitride layer 30 can have a thickness of 65 Å to 250 Å*. Ex. 1005, col. 8:19-20; Ex. 1001, col. 2:65-67; Ex. 1003, ¶ A-5.

Doshi then describes etching contact openings through the BPSG insulating layer 14 and the nitride layer 30 using a two-step etch process. Ex. 1005, Abstract and col. 9:25 – 10:16. The first step involves selectively etching BPSG insulating layer 14 relative to the nitride layer 30. *Id.* The second step follows the first, and it involves a highly anisotropic etch that exposes the diffusion region 7. This second step, due to the anisotropic nature of the etch, removes the thin surface of layer 30 more quickly than the thick vertical wall of layer 30, leaving a spacer of nitride 30 on the sidewall of the gate electrode structure 10, as shown in the annotated Fig. 3g above, consistent with the '997 patent. Ex. 1005, col. 10:11-16; Paper 1, pp. 18-19 and 25-27; Ex. 1003, ¶¶ A-12 to A-14.

B. Doshi's Anisotropic Etch Exposes The Diffusion Region While Leaving A Spacer Formed On The Gate Electrode Sidewall

Claim 1 recites “anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.” As

established in the Petition and described above, Doshi discloses etching the silicon nitride layer 30 using a brief and highly anisotropic etch, which exposes the diffusion region while leaving a spacer of the silicon nitride layer 30 formed on the sidewall of the gate electrode. Paper 1, pp. 25-27; Ex. 1003, ¶¶ A-12 to A-14. HSC alleges several substantive shortcomings of Doshi, which are noted and addressed below.

1) Doshi's nitride layer remains on the sidewall after application of a highly anisotropic etch

HSC argues that “[t]his limitation requires the formation of spacers on the sidewalls of the gate electrode at the same time as the anisotropic etch step,” and HSC contends that this distinguishes Doshi because “Doshi’s specification teaches that nitride layer 30 is removed from the contact hole locations during the nitride etch step.” Paper 18, pp. 16-17. HSC’s argument is without merit.

A POSITA reviewing Doshi would have readily recognized that Doshi retains a portion of its silicon nitride layer 30 on its sidewalls after the “highly anisotropic” etch. This would have been evident in view of both the anisotropy of the etch and the expressly stated goal of Doshi to minimize damage to gate structures 10 and sidewall filaments 11. Ex. 1005, col. 10:4-17; Ex. 1011, ¶ 2A. This conclusion would have been further reinforced by Doshi’s suggestion that

damage to Doshi's diffusion region 7, which would result from the aggressive over-etch necessary to completely remove the layer 30, also would be undesirable.

HSC's argument to the contrary relies on Fig. 3k of Doshi that omits nitride 30 along its sidewalls when otherwise illustrating structures involved in bit line contact (BLC) formation. Petitioner never relied on Fig. 3k to satisfy the claims of the '997 patent, instead only relying on Fig. 3g, which clearly shows forming a spacer of nitride 30 along sidewalls as part of plug contact (PC) formation. The PC holes shown in Fig. 3g are not etched in the Fig. 3k rendering. HSC refers to Fig. 3k, therefore, as merely a mechanism to undermine the explicit disclosure of Fig. 3g, asserting that Fig. 3k's depiction of no nitride 30 along sidewalls would have led a POSITA to conclude that Fig. 3g's depiction of nitride 30 along sidewalls was an error. But a POSITA would not have arrived at this conclusion. While Fig. 3g's depiction of the PC holes is largely consistent with the rest of Doshi's disclosure, adopting HSC's interpretation of Fig. 3k's depiction of the BLC hole, in contrast, directly undermines Doshi's express goal of minimizing damage to structures 10 and filaments 11. That is, given the anisotropy of the two-step etch process used for both the PC and BLC formation and Doshi's goal of minimizing damage, a POSITA would have concluded that nitride 30 would

remain on sidewalls of both Figs. 3g and 3k, with Fig. 3k being erroneous for failing to depict this nitride. Ex. 1011, ¶ 3A.

(i) Complete removal of the nitride exposed on the sidewall is inconsistent with Doshi's expressly stated goal of minimizing damage to gate structures 10 and sidewall filaments 11

HSC argues that “[t]he nitride etch process designed to clear the nitride layer 30 would etch *every part of layer 30 exposed under the contact opening*.” Paper 18, p. 19 (emphasis added). HSC cites to Doshi's disclosure that the brief and anisotropic nitride etch “clear[s] nitride layer 30 from within plug contact locations PC” and “remove[s] nitride layer 30 from bit line contact location BLC” as support that no portion of nitride layer 30 remains following the etch process. *Id.*, p. 17. This argument is flawed in several respects. Yet, in referring to the recited etching step that forms the spacer, the Petition cited to the Abstract and col. 10:11-13 of Doshi, and ¶¶ 12-14 of Dr. Rubloff's declaration. Paper 1, pp. 25-27. Importantly, the cited portions of Dr. Rubloff's declaration further cite to at least col. 10:11-16 of Doshi for support, which state:

the brief nitride etch used to clear nitride layer 30 from within plug contact locations PC has been observed to be *highly anisotropic*, and *because of this anisotropy in combination with its brevity, minimizes damage at the sidewall comer locations NC of gate structures 10* in integrated circuit 20. (Emphasis added).

Indeed, Doshi explains that its reference to “highly” anisotropic etching was technologically purposeful, as it notes that this etch process “is particularly

beneficial, as *damage to the corners of gate structures 10 and sidewall filaments 11 is substantially minimized*" (emphasis added), as distinguished from "conventional nitride etches" which may damage "sidewall corner locations NC illustrated in FIG. 3g." Ex. 1005, col. 10:4-11.

HSC's argument should be rejected because a complete removal of the silicon nitride layer 30 from the sidewalls of Doshi's contact holes using a highly anisotropic etch is inconsistent with Doshi's disclosure. Specifically, such a complete removal would damage the sidewall filaments 11 and expose gate structures 10 to potential damage, in direct contravention to Doshi's explicitly stated goal of minimizing damage to these structures. Ex. 1011, ¶ 2A. A POSITA would have understood that a highly anisotropic etch generally indicates that the etch rate in a perpendicular/vertical direction (i.e., etching from top to bottom) is much greater than the etch rate in a lateral/horizontal direction (i.e., etching from the side). Ex. 1014, p. 3; Ex. 1011, ¶¶ 2B-2C. Indeed, Mr. Maltiel stated that the taller the structure on the sidewall, the harder it would be to remove the structure:

Petitioner: "Do you believe there are some anisotropic etch processes that would -- that would completely remove the sidewall spacers?"

Mr. Maltiel: "That would completely remove? It's -- I mean, it would -- *it depend on the -- the height of the structure* that you're trying to -- that you make the space -- because the taller the structure is the -- I mean, *the more have -- the spacer would be. So it would be harder to fully remove it.*

Ex. 1012 at 159:7-15 (emphasis added).

Therefore, a POSITA would have understood that an aggressive over-etch would be required to completely remove the nitride layer 30 from the sidewalls when using a highly anisotropic etch. Ex. 1011, ¶ 2D. Such an aggressive over-etch, however, would damage sidewall filaments 11 and also would likely damage the gate structures 10. *Id.*

In particular, referring to FIG. 3g of Doshi, once the nitride film 30 covering the NC of filaments 11 and gate structures 10 is etched through via the faster vertical etching of the highly anisotropic nitride etch, the subsequent additional etching time used to remove the remaining sidewall portions of film 30 would result in etch of the NC portion of the filaments 11 and the gate structures 10. Ex. 1011, ¶ 2E. During this additional time, given that filaments 11 are partially formed of silicon nitride, the highly anisotropic silicon nitride etch would readily etch into the portions of the filaments 11 formed of nitride. Ex. 1005, col. 7:52-65; Ex. 1011, ¶ 2E. Moreover, the silicon nitride layer 26 of the gate structures 10 also may be etched as the NC portion of gate structures 10 progressively become exposed during the over-etching needed to completely remove the film 30. The damage caused by this over-etch is, simply put, inconsistent with Doshi's disclosure that its etch "substantially minimize[s]" damage "to the corners of gate structures 10 and sidewall filaments 11." Ex. 1005, col. 10:4-16; Ex. 1011, ¶ 2E.

Indeed, a POSITA would readily have understood that such damage to the structures 10 and sidewall filaments 11 undesirably increases the likelihood of shorts occurring between a contact plug and the gate electrode. Ex. 1011, ¶ 2E.

Therefore, contrary to HSC's assertions, a POSITA would not have been led by Fig. 3k or otherwise to believe that Doshi's highly anisotropic nitride etch completely removes the film 30 from Doshi's contact holes. *Id.* A POSITA would have understood Doshi's description of brief nitride etching to clear nitride layer 30 from within PC or BLC region to mean that the brief and highly anisotropic nitride etch is used to clear the nitride layer 30 that is conformal to the diffusion region 7, without suggesting that such a brief and anisotropic etch would clear the nitride layer 30 that is conformal to the sidewall of the gate electrode 10. *Id.* As confirmed by Dr. Rubloff, a POSITA would have understood that a nitride sidewall spacer would be formed, not completely removed, after the nitride etch:

HSC: "Where does it say you will have remaining a nitride sidewall spacer?"

Dr. Rubloff: "It doesn't say it that way. It says it's a highly anisotropic etch, and it doesn't damage or remove much at the top at that corner above the sidewall filament. Therefore, one of ordinary skill would certainly conclude that that sidewall nitride structure remains [. . .] as a spacer."

Ex. 2004 at 181:6-15; *see also* Ex. 1011, ¶¶ 2F and 5A-5D.

(ii) Complete removal of the nitride layer would likely damage the diffusion region of Doshi's device

In Doshi, there is no gate oxide 8 between the silicon diffusion layer and the silicon nitride layer 30. Ex. 1005, Fig. 3b, col. 8:3-22. After the diffusion region 7 is exposed by the silicon nitride etch, therefore, a POSITA would have understood that the diffusion regions 7, like the filaments 11 and gate electrode structures 10, are also vulnerable to etch damage from the over-etch required to completely remove the layer 30. Ex. 1011, ¶¶ 2G-2H; Ex. 1012 at 156:2-14. Doshi, however, teaches the importance of tightly controlling the dimensions of the diffusion region 7, including the junction depth, due to the heightened sensitivity of these dimensions to process variations. Ex. 1011, ¶ 2H. According to Doshi:

“[t]hese extremely small critical dimensions not only result in high density and high performance integrated circuit operation, but also involve significant sensitivity to process variations and parameters.” Ex. 1005, col. 6:57-64.

A POSITA would have readily recognized that exposing the diffusion region 7 to an aggressive over-etch would compromise the tight control of the dimensions of the diffusion region 7 by introducing variable damage and, in doing so, would cause undesirable process variation that can compromise the high density and high performance of Doshi's integrated circuits. Ex. 1011, ¶ 2I.

In particular, Doshi discloses that the junction depth of the diffusion region 7 is on the order of 0.3 μm (300 nm). Ex. 1005, col. 6:57-64. Doshi also discloses that the height of the nitride sidewall 30 on the gate electrode 10 would also be on

the order of several hundred nm. Ex. 1011, ¶ 2J. Thus, consistent with the common understanding of a POSITA, an aggressive over-etch to remove the silicon nitride layer 30 on the sidewall would likely damage the diffusion region 7, in contrast to Doshi's goal of achieving tight dimensional control to achieve desirable device performance and density. *Id.*

Mr. Maltiel acknowledged the vulnerability of a diffusion region to etch damage caused by a long over-etch when discussing the '997 patent:

Petitioner: "Without the oxide layer 60, the anisotropic etch of the conformal nitride layer 62 would etch the diffusion region 58, correct?"

Mr. Maltiel: "Well, unless you -- it's -- again, you have selectively with the nitride and the silicon. So when you etch the layer 60, you -- you still -- what I'm saying, *if you don't have the layer 60*, so when you etch the nitride layer 62, you still would be able to stop on the silicon. *You likely can damage it if you go for too long.* But if you have one controlled process, you would be able to manage it. But this is part of the reason why you have layer 60 there."

Ex. 1012 at 156:2-14 (emphasis added).

Contrary to HSC's assertions, therefore, a POSITA would not have been led to conclude that Doshi's etch process completely removes the nitride layer 30 from the contact holes because the over-etch contemplated by such an interpretation would likely damage the diffusion region 7 of Doshi's device. Complete removal of the layer 30, therefore, would be inconsistent with Doshi's teachings indicating the desirability to tightly control the small, critical dimensions of the diffusion region 7. Ex. 1011, ¶ 2K.

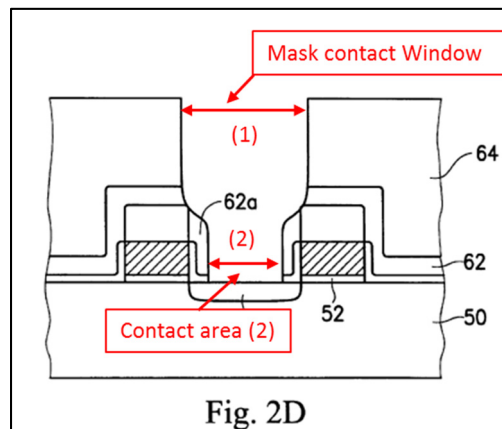
Accordingly, Doshi's disclosure is unambiguous that a brief and highly anisotropic etch would form a sidewall spacer.

(iii) Fig. 3k fails to show a self-aligned contact hole and, therefore, is inconsistent with Doshi's express goal of not damaging the sidewall filaments 11

HSC argues that "unlike Doshi Fig. 3g's depiction of the etch process of PC locations, there is no indication that Fig. 3k's depiction of the etch process in the BLC location is erroneous or unreliable." Paper 18, p. 21. A closer look at Doshi's disclosure, however, reveals that it is Fig. 3k, rather than Fig. 3g, that is incorrectly depicting the etch process used to form the illustrated contact hole. In particular, Fig. 3k fails to show a self-aligned contact hole formed by Doshi's two-step etch process. Ex. 1011, ¶ 3A. That is, because Fig. 3k fails to show a self-aligned contact hole, gate structures 10 and sidewall filaments 11 are exposed to damage from etching as a result of even a minor mask misalignment. *Id.* A POSITA, therefore, would have recognized that the depiction of the BLC hole in Fig. 3k is erroneous, and, as a consequence, fails to properly depict the BLC hole as a self-aligned contact hole consistent with Doshi's express goal of protecting structures 10 and filaments 11 from damage. *Id.*

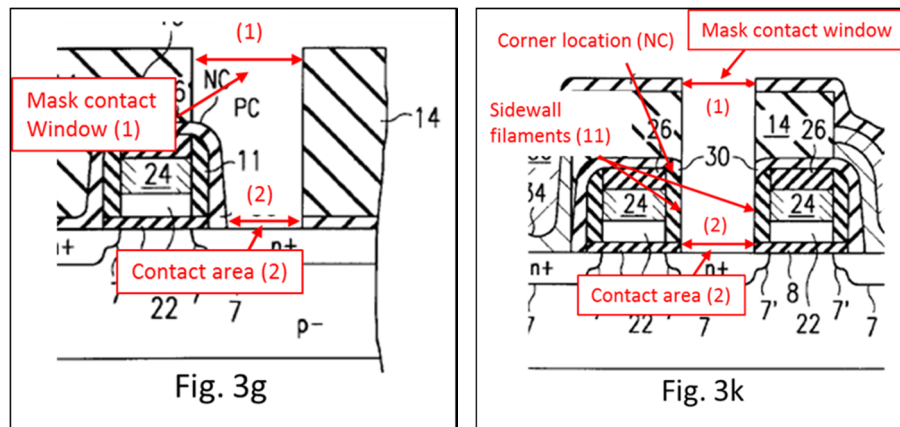
In greater detail, there is no dispute on record that Doshi discloses a method for forming a self-aligned contact hole. Paper 1, pp. 19-20; Ex. 1003, ¶ A-1.

Referring to the annotated Fig. 2D of the '997 patent below, a self-aligned contact hole is a single-mask process where the dimension of the mask contact window is oversized relative to the desired dimension of the contact area underneath in order to eliminate the alignment tolerance required by additional masks. Ex. 1001, col. 1:10-23; Ex. 1003, ¶ 15; Ex. 2002, ¶ 22. Self-alignment therefore involves a two-step etch described in Section(III)(A), where the first etch uses the silicon nitride layer 62 as a etch stop, and the second anisotropic etch ensures that the portion of the diffusion region 58 exposed by the second silicon nitride etch is determined by the lateral dimensions of the spacer 62a, and not by the dimension of the lithography mask. Ex. 1001, col. 3:10-24; Ex. 1003, ¶ 21; Ex. 1011, ¶ 3B.



In much the same way as described in Section(III)(A), the process used by Doshi to form its self-aligned contact hole involves a first selective etch and a second highly anisotropic etch. Paper 1, pp. 19-20; Ex. 1003, ¶¶ A-1 and A-12; Ex. 1005, Fig. 3f, Abstract and col. 9:25 – 10:16; Ex. 1011, ¶ 3C. Comparing the

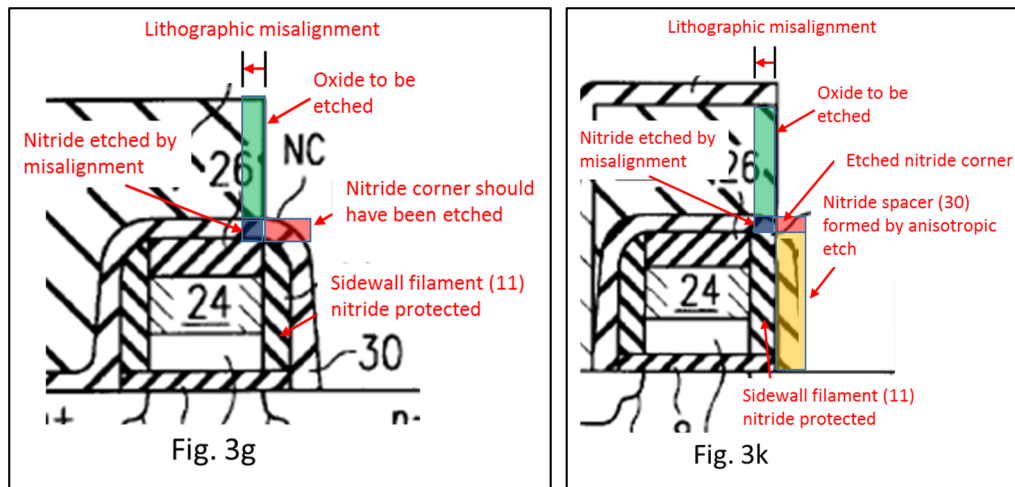
annotated Fig. 3g with the annotated Fig. 3k below, Fig. 3g shows that the dimension of the mask contact window is indeed oversized relative to the dimension of the contact area, which is consistent with a POSITA's understanding of a self-aligned contact hole. Ex. 1011, ¶ 3D. On the other hand, Fig. 3k shows that the dimension of the mask contact window *matches* the dimension of the contact area, suggesting to a POSITA that Fig. 3k may be erroneous. *Id.*



Indeed, the depiction of a contact hole in Fig. 3k would not be consistent with a POSITA's understanding of a *self-aligned* contact hole, as there is no room for any lithographic misalignment. *Id.* In other words, according to Fig. 3k as revealed by the annotations shown below, any misalignment would result in Doshi's highly anisotropic silicon nitride etch damaging the sidewall filaments 11 in a manner akin to that noted in Section(III)(B)(1)(i) above. Ex. 1005, col. 7:57-62; Ex. 1011, ¶ 3E. This result directly contradicts Doshi's disclosure, and therefore HSC's interpretation of Fig. 3k would be rejected by a disinterested

A cross-sectional diagram of a semiconductor device. The diagram shows a substrate with a patterned layer labeled '14'. Above this is a layer labeled '26'. A vertical green bar is labeled 'Oxide to be etched'. A vertical red bar is labeled 'Sidewall filament (11) nitride exposed to etch'. A horizontal line labeled '30' is shown. A vertical line labeled '24' is shown. A vertical line labeled 'Lithographic misalignment' is shown. The diagram is labeled 'Doshi, Fig. 3k'.

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2) Doshi's anisotropic etch forms a spacer that complements the spacer already existing prior to the anisotropic etch

HSC further argues that the nitride layer 30 already functions as a spacer before the anisotropic etch, and therefore cannot be “simultaneously” formed during the nitride etch process. Paper 18, pp. 22-23. HSC attempts to support its argument through citation to acknowledgement by Dr. Rubloff, in deposition, that the pre-etched nitride layer 30 creates space between two conductive structures and therefore would fit within the definition of a spacer. *Id.* HSC argues that a spacer cannot be formed if it already exists before the etch. *Id.* HSC's argument fails however, because it does not account for the fact that Doshi's anisotropic etch forms a new structure that is also a spacer.

The proper inquiry is not whether Doshi discloses a structure that may function as a spacer before the nitride etch process, but whether Doshi otherwise forms a spacer, as claimed, i.e., whether it discloses “anisotropically etching the

barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.” By comparing Fig. 3f and Fig. 3g of Doshi, it is clear that Doshi’s anisotropic nitride etch process etches the nitride barrier layer 30 underneath the PC opening, and simultaneously forms a spacer that is physically different from the unetched pre-existing spacer. It is this second etch-formed spacer that satisfies the claim. Moreover, HSC’s reliance on Dr. Rubloff’s testimony is misleading, as HSC has omitted statements made by Dr. Rubloff after the statements quoted by HSC, where he acknowledged that whether Doshi discloses a structure that may function as a spacer before the nitride etch process is not the right inquiry:

HSC: “So it is not a spacer?”

Dr. Rubloff: “Well, a diffusion barrier is a kind of spacer.”

HSC: “Okay. So it is a spacer?”

Dr. Rubloff: “Yes.”

HSC: “Okay.”

Dr. Rubloff: “***But that's not the spacer that's at issue here.*** I realize that.”

HSC: “I don't follow you.”

Dr. Rubloff: “No. ***I think your question was, at this stage after both etches of BPSG and nitride is done, how do we know there's still a nitride sidewall spacer?*** And that's a different -- that's a different question.”

Ex. 2004 at 196:10 – 197:1 (emphasis added); Ex. 1011, ¶ 4A.

C. Doshi Discloses Forming An Oxide Layer Over The Diffusion Region

As an initial matter, as established by Petitioner and undisputed by HSC, under Petitioner’s proposed construction of the term “forming an oxide layer over the diffusion region,” Doshi anticipates claims 2 and 9. Paper 1, pp. 27-29.

Although the Board has determined that this term does not require express construction, the Board has also reached the conclusion that Doshi anticipates claims 2 and 9. Paper 11, pp. 8 and 15-16. HSC's proposed construction should be rejected for the reasons set forth above in Section(II)(B). Thus, Doshi anticipates claims 2 and 9 under either Petitioner or the Board's claim construction.

Moreover, even under HSC's proposed construction, there is no dispute that Doshi discloses forming an oxide layer on the sidewalls of the gate electrode by thermal oxidation. Paper 18, p. 24. HSC only argues that, under its proposed construction, Doshi does not disclose forming an oxide layer on the diffusion region. *Id.*, pp. 24-28. Notably, however, Petitioner has established that, during the thermal oxidation of the sides of polysilicon layer 22, thermal oxide is grown over the source/drain regions because the source/drain regions are uncovered doped silicon, which is susceptible to thermal oxidation.¹ Paper 1, pp. 28-29. HSC disagrees, as it believes that the diffusion regions are covered by the gate oxide layer during the oxidation of the polysilicon gate sidewalls, and that the diffusion regions are therefore not uncovered doped silicon. Paper 18, p. 28. Whether the

¹ In the Institution Decision, the Board did not rely on this portion of the argument to reach the conclusion that Doshi anticipates claims 2 and 9. Paper 11, pp. 15-16.

diffusion region is covered by the gate oxide layer is not relevant, however, since thermal oxide is formed over the diffusion region during the oxidation of the polysilicon gate sidewalls regardless. Ex. 1011, ¶ 6A. During his deposition, Dr. Rubloff eliminated any question about this issue:

HSC: "And you said that during the oxidation process, an oxide layer would also be formed over the diffusion regions; is that correct?"

Dr. Rubloff: "Yes."

HSC: "And this is true if the diffusion region is uncovered silicon; correct?"

Dr. Rubloff: "Well, if it's -- ***it's true if it's uncovered silicon, or if it's covered by thin oxide***. Because thermal oxide has linear growth rate in the thin regime. So if you already have a thin layer of oxide and you go to oxidizing conditions, you make it thicker."

Ex. 2004 at 171:19 – 172:13 (emphasis added).

Thus, even if the diffusion regions are covered by a gate oxide layer during the oxidation of the polysilicon gate sidewalls, a thicker oxide layer would still be formed during oxidation, and the resulting thickened oxide layer covers the diffusion region. Paper 18, p. 10; Ex. 1011, ¶¶ 6A-6B. Accordingly, Doshi discloses "forming an oxide layer over the diffusion region," as recited in claims 2 and 9 even under HSC's proposed construction of the term "over."

IV. CONCLUSION

Petitioner respectfully requests that the Board find claims 1–14 of the '997 patent as unpatentable in a Final Written Decision.

Respectfully submitted,

Date: 11/30/2015

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(1) and 42.6(e)(4)(iii), the undersigned certifies that on November 30, 2015, a complete and entire copy of this Petitioner's Reply to Patent Owner's Response was provided via email to the Patent Owner by serving the email correspondence addresses of record as follows:

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