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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioner,[1]

v.

HOME SEMICONDUCTOR CORPORATION,
Patent Owner.

Case IPR2015-00460
Patent 6,146,997

Before JONI Y. CHANG, JON B. TORNQUIST, and BETH Z. SHAW, *Administrative Patent Judges.*

SHAW, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

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[1] Samsung Telecommunications America LLC, originally a real party-in-interest at the time of filing the Petition, no longer exists as a separate corporate entity, because it has merged with and into Samsung Electronics America, Inc. Paper 9.

I. INTRODUCTION

Petitioners, Samsung Electronics Co. Ltd., Samsung Electronics America Inc., Samsung Semiconductor Inc., and Samsung Austin Semiconductor LLC (collectively "Samsung"), filed a Petition requesting an *inter partes* review of claims 1–14 of U.S. Patent No. 6,146,997 (Ex. 1001, "the '997 patent"). Paper 1 ("Pet."). Patent Owner, Home Semiconductor Corporation ("HSC"), did not file a Preliminary Response. We determined that the information presented in the Petition demonstrated a reasonable likelihood that Petitioner would prevail with respect to claims 1–14 of the '997 patent. Pursuant to 35 U.S.C. § 314, we instituted trial as to those claims. Paper 11 ("Dec. Inst.").

After institution of trial, Patent Owner filed a Patent Owner Response to the Petition (Paper 18, "PO Resp."). Petitioner filed a Reply to Patent Owner's Response (Paper 21, "Reply"). An oral hearing was held on February 25, 2016.[2]

We have jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Samsung has shown by a preponderance of the evidence that claims 1–14 of the '997 patent are unpatentable.

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[2] The oral hearings for this trial and the following cases were consolidated: Cases IPR2015-00459, IPR2015-00466, and IPR2015-00467. Paper 30. A transcript of the hearing has been entered into the record as Paper 31 ("Tr.").

A. Related Matter

Samsung indicates that the ’997 patent is asserted in *Home Semiconductor Corporation v. Samsung Electronics Co. Ltd.*, No. 1:13-cv-02033 (D. Del.), filed December 16, 2013. Pet. 1.

B. The ’997 Patent

The ’997 patent relates to semiconductor device fabrication. Ex. 1001, 1:6–7. In particular, the ’997 patent discloses a method for forming a self-aligned contact hole. *Id*. at 1:5–10. The ’997 patent combines a spacer formation step and a contact hole exposure step into a single processing step to reduce the number of process steps. *Id.* at 1:65–67, 2:5–14, 3:40–47. The reduction of processing steps may reduce manufacturing costs and increase throughput. *Id.*

Figure 2B of the ’997 patent is reproduced below (red annotations added by Samsung):

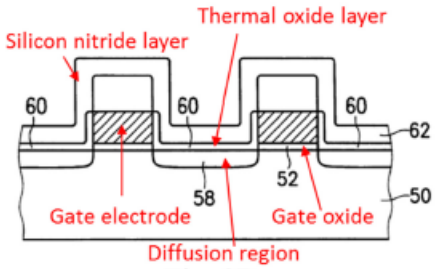

Fig. 2B

Figure 2B of the ’997 patent, reproduced above, illustrates that after gate electrodes 54 (not numbered here), diffusion regions 58, thermal oxide layer 60, and gate oxides 52 have been formed on substrate 50, conformal

layer of silicon nitride 62 is deposited over the substrate surface. *Id.* at 2:48–67.

Figure 2C of the ’997 patent is reproduced below (red annotations added by Samsung):

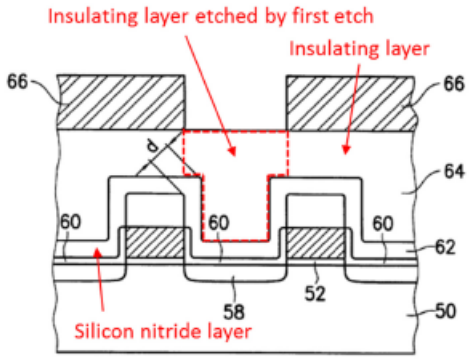

Fig. 2C

Figure 2C of the ’997 patent, reproduced above, illustrates planarized inter-layer dielectric insulating layer 64 formed over conformal silicon nitride layer 62, and photoresist layer 66 formed and patterned to expose contact hole 67 (shown in Figure 2D below). *Id.* at 3:1–24. An etch that is highly selective to silicon nitride layer 62 is performed to etch away insulating layer 64. *Id.*

Figure 2D of the ’997 patent is reproduced below (red annotations added by Samsung):

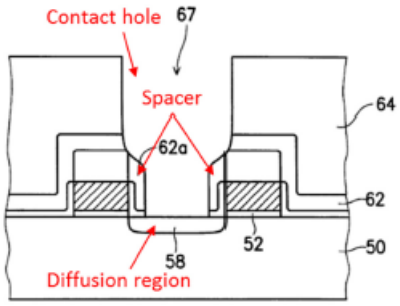

Fig. 2D

Figure 2D of the ’997 patent, reproduced above, illustrates that following the first selective etch of insulating layer 64, silicon nitride layer 62 is etched anisotropically to expose diffusion region 58. *Id.* at 3:1–24. Due to the directionality of the anisotropic etch, spacer 62a is formed on the sidewall of the electrode 54 during the same silicon nitride etch that exposes diffusion region 58 to complete contact hole 67. *Id.* After the contact hole 67 is filled with conductive material to form a conductive plug, spacer 62a can be used to prevent shorting between the gate electrode and the conductive plug. *Id.* at 3:33–39.

C. Illustrative Claim

Of the challenged claims, claims 1 and 9 are the only independent claims. Claims 2–8 depend, directly or indirectly, from claim 1; claims 10–14 depend from claim 9. Claim 1 reads as follows:

> 1. A method for forming a self-aligned contact hole, comprising the steps of:
>
> (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;

> (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;
>
> (c) forming an insulating layer overlying the barrier layer;
>
> (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and
>
> (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

Ex. 1001, 3:54–4:4.

D. Ground of Unpatentability Instituted for Trial

We instituted a trial of claims 1–14 under 35 U.S.C. § 102(e) as anticipated by Doshi et al., U.S. Patent Number 6,277,720 B1, issued on August 21, 2001 (Ex. 1005, "Doshi").

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278, 1279 (Fed. Cir. 2015) ("Congress implicitly approved the broadest reasonable interpretation standard in enacting the AIA," and "the standard was properly adopted by PTO regulation."), *cert. granted sub nom. Cuozzo Speed Techs., LLC v. Lee*, 136

S. Ct. 890 (2016). We are mindful that "limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Nevertheless, claims are not interpreted in a vacuum but are part of and read in light of the specification. *U.S. v. Adams*, 383 U.S. 39, 49 (1966) ("[I]t is fundamental that claims are to be construed in the light of the specifications and both are to be read with a view to ascertaining the invention"). In that regard, the terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the specification. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). The construction that stays true to the claim language and most naturally aligns with the inventor's description is likely the correct interpretation. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998).

Samsung proposes constructions for the following claim terms: "forming a conformal layer of [etch barrier material/silicon nitride] overlying the substrate," "spacer," and "etching an opening through the insulating layer self-aligned and borderless to the diffusion region," which are recited in at least independent claims 1 and 9, and "forming an oxide layer over the diffusion region," recited in claims 2 and 9. Pet. 5–10.

Subsequent to institution, HSC proposes constructions for the following claim terms: "spacer" and "over." PO Resp. 7–11.

We determine that only the claim terms discussed below require express construction.

"spacer"

Claim 1 recites "forming a spacer of the etch barrier material on the sidewall of the gate electrode." Ex. 1001, 4:3–4. Claim 9 recites "forming a spacer of silicon nitride on the sidewall of the gate electrode." *Id.* at 4:47–48.

In the Decision on Institution, we construed "forming a spacer of the etch barrier [material] on the sidewall of the gate electrode," as recited in claim 1, as not requiring the spacer to be in direct contact with the gate electrode. Dec. Inst. 8. We found this construction consistent with the Specification of the '997 patent, which does not require the spacers to touch the gate electrode directly. *Id.* (citing Ex. 1001, Fig. 2D, 3:20–21). Upon review of the present record, we discern no reason to change our claim construction for purposes of this Final Written Decision.

Subsequent to institution, both Samsung and HSC propose a construction for "spacer." The Specification does not expressly define the term "spacer." Samsung proposes the same construction for "spacer" as proposed in the Petition. Pet. 9–10. Samsung interprets spacer as "a structure that spaces between two conductive structures." *Id.*; Reply 2.

HSC disagrees and contends that one of ordinary skill in the art would understand that the term "spacer" means "a structure *designed* to create[] physical separation between conducting structures." PO Resp. 7 (citing Ex. 2002 ¶ 40) (emphasis added). As support, HSC cites to expert testimony and to the following portion of the Specification: "Further, the same nitride

layer is anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug." Ex. 1001, 3:35–38.

This portion of the Specification, however, does not persuade us that HSC's proposed construction is the broadest reasonable construction. Rather, this sentence merely states that a nitride layer is anisotropically etched to form sidewall spacers *that* prevent shorting, not that the sidewall spacers are *designed to* prevent shorting.

We are not persuaded by HSC's argument and expert testimony that a spacer as recited in claims 1 and 9 must be a structure that is "purposefully designed into the fabrication process [in order] to achieve specific functions." *Id.* at 8. Rather, in light of the Specification, we agree with Samsung that HSC's proposed construction, which would require a structure "designed to" create physical separation, would render this claim limitation ambiguous and would focus on the *intent* of the manufacturer or state of mind of the accused infringer. *See* Reply 2–5 (citing *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1353 (Fed. Cir. 2001) ("We are not prepared to assign a meaning to a patent claim that depends on the state of mind of the accused infringer."). As Samsung notes, the plain meaning of the term "spacer" is "one that spaces." Pet. 9; Reply 5; Ex. 1007. This is consistent with the Specification of the '997 patent. *See* Ex. 1001, Fig. 2D, 3:20–21, 36–39. In view of the foregoing, we decline to adopt HSC's proposed claim construction.

Accordingly, we construe "spacer," as recited in claim 1, as a structure that spaces between two conductive structures. Pet. 9.

"forming an oxide layer over the diffusion region"

Dependent claim 2 and independent claim 9 recite "forming an oxide layer over the diffusion region." Ex. 1001, 4:6–8, 32–34. Samsung interprets this limitation to mean forming an oxide layer above the diffusion region. Pet. 7–9. HSC disagrees and proposes that "forming an oxide layer over the diffusion region" should be construed to mean "forming an oxide layer *covering* the diffusion region." PO Resp. 8–11 (emphasis added). HSC essentially proposes to construe "over the diffusion region" as *completely* covering the diffusion region because HSC states that the oxide layer cannot be merely higher in position with structures in between. PO Resp. 10–11. HSC argues, however, that covering "does not mean that there cannot be structures in between." *Id.* at 10 n.1.

We are not persuaded that the Specification of the '997 patent supports HSC's contention that "over" must be construed so narrowly as to mean completely "covering" or completely covering with potential structures in between the diffusion region and the oxide layer.[3] PO Resp. 7–11. As a preliminary matter, we find the word "covering" does *not* appear in the claims or in the Specification. HSC argues that certain figures of the '997 patent depict an oxide layer covering the diffusion region. PO Resp. 9.

[3] Moreover, even if we adopted HSC's construction of "over" as "covering," we remain unpersuaded that such a construction would alter the outcome of this Decision at least because a construction of "covering" does not mean that the oxide layer *entirely* or *completely* covers the diffusion region.

HSC's proposed construction, however, would import improperly a limitation that is arguably disclosed in the Specification into claims 2 and 9. *See Superguide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim."); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (expressly rejecting "the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment"). We decline to insert this argued limitation, which does not appear in the claims or in the Specification, into claims 2 and 9.

A construction of "forming an oxide layer over the diffusion region" to mean forming an oxide layer above the diffusion region is consistent with the plain meaning of the claim. This is also consistent with the Specification of the '997 patent, which illustrates forming an oxide layer above the diffusion region. Figure 1B of the '997 patent is reproduced below.

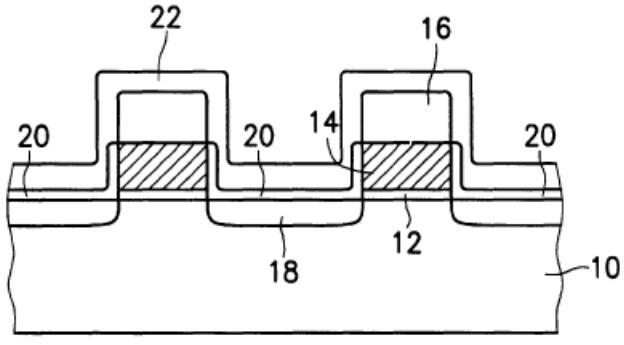

Fig. 1B (Prior Art)

Figure 1B of the ’997 patent, reproduced above, which is marked as “prior art” in the ’997 patent, illustrates a conformal layer of silicon nitride deposited over the substrate surface. Ex. 1001, 1:33–35, Fig. 1B. Prior to the deposition of the silicon nitride layer 22, at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14 have been formed on the substrate 10. *Id*. at 1:24–31. The silicon nitride layer 22 is above the substrate 10, where at least the oxide layer 20, the gate oxide layer 12, and the gate electrodes 14, are between the silicon nitride layer 22 and the surface of the substrate 10. *See id.* at Fig. 1B.

In view of the foregoing, we decline to adopt HSC’s proposed claim construction because it is not consistent with the broadest reasonable construction. The claims simply do not recite forming an oxide layer “covering” the diffusion region, and the Specification does not inform such an interpretation of “over” to mean “covering.” As Samsung argues, HSC could have chosen to recite covering, but chose greater breadth through its recitation of over. Reply 6.

In light of both the plain language of the claims and the Specification, we agree with Samsung that the aforementioned “forming an oxide layer over the diffusion region” means forming an oxide layer above the diffusion region. Pet. 7–9; Reply 5–7.

B. Principles of Law

For a prior art reference to serve as an anticipatory reference, it must disclose every limitation of the claimed invention, either explicitly or

inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). We must analyze prior art references as an ordinary artisan would. *See Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991) (stating that to anticipate, "[t]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention"), *overruled on other grounds by Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009).

C. Anticipation of Claims 1–14 by Doshi

In the Petition, Samsung asserts that claims 1–14 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Doshi. Pet. 19–36. We have reviewed Samsung's explanation identifying where each limitation allegedly appears in Doshi, along with the testimony of Petitioner's Declarant, Dr. Gary W. Rubloff. *Id.*; Ex. 1003. We have also reviewed HSC's assertions and evidence as to why Samsung's explanations and evidence are deficient, including the testimony of HSC's Declarant, Mr. Ron Maltiel. PO Resp. 2–29; Ex. 2002.

We begin our discussion with a brief summary of Doshi, and then we address Samsung's contentions, HSC's assertions, and the evidence of record.

1. Summary

Doshi discloses a method of fabricating an integrated circuit, including a method of fabricating contact openings. *See* Ex. 1005, Abstract. According to Doshi, gate electrode structures 10 and doped source/drain

diffusion regions 7 and 7' are fabricated on a semiconductor substrate 2. Ex. 1005, 7:29–8:7. Figure 3d of Doshi is reproduced below (red annotations added by Samsung):

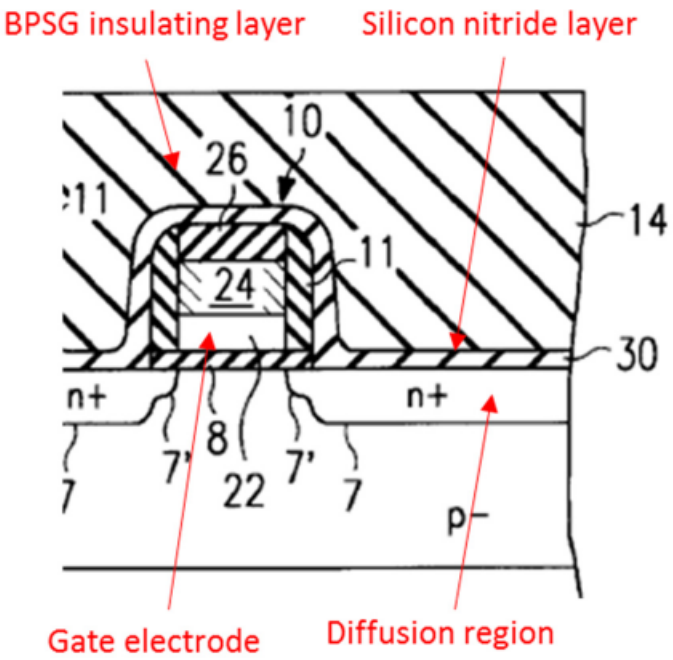

Fig. 3d, Doshi

As shown in Figure 3d of Doshi, reproduced above, conformal silicon nitride layer 30 is deposited over gate electrode structure 10 and the source/drain diffusion regions 7 and 7', followed by formation of BPSG insulating layer 14. *Id.* at 8:8–36.

2. Etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop

Doshi describes etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop, as recited in independent claims 1 and 9. Figure 3f of Doshi is

reproduced below (red annotations added by Samsung):

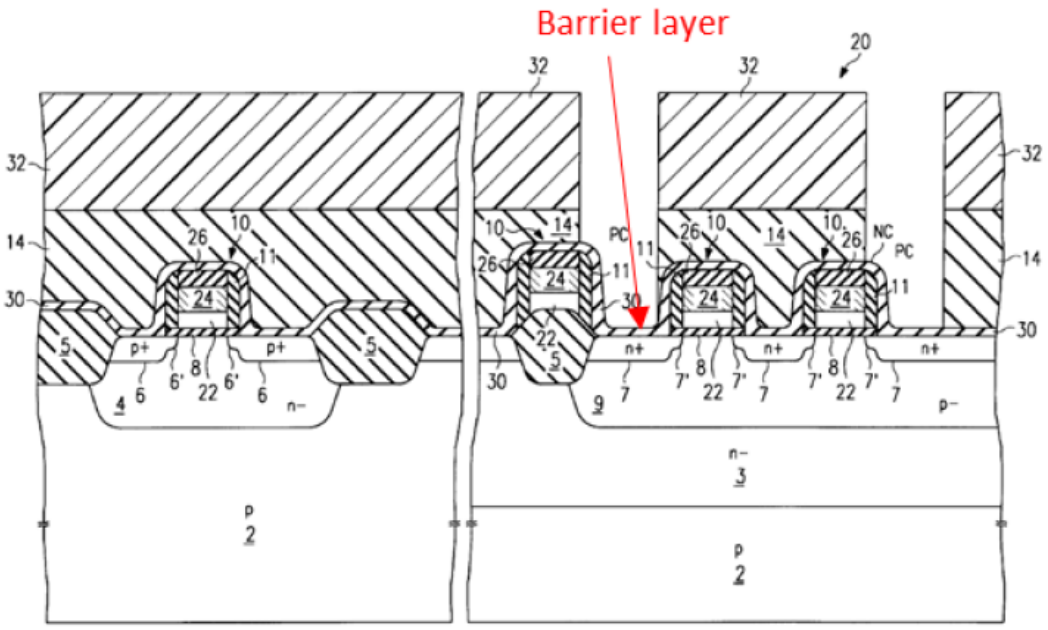

FIG. 3f

Samsung argues Figure 3f, reproduced above, shows etching an opening through BPSG layer 14 to diffusion region 7 by using silicon nitride layer 30 as an etch stop. As support, Samsung cites to the following disclosure in Doshi:

> According to this preferred embodiment of the present invention, etching of contact openings through BPSG layer 14 and nitride layer 30 is performed by way of a two-step etch. *The first step is a "dry" etch of BPSG layer 14*, carried out in a plasma etch reactor as known in the art, a preferred example of which is the TEL DRM reactor. [. . .] Under these conditions, etching of BPSG layer 14 is relatively highly selective relative to etching of nitride layer 30, and as *such the etch will tend to stop on nitride layer 30*.

Pet. 24 (citing Ex. 1005, 9:34–50). We determine that Doshi describes the etch through BPSG layer 14 will stop at nitride layer 30, which discloses etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop, as recited in independent claims 1 and 9.

3. Simultaneously forms a spacer of silicon nitride on the sidewall of the gate electrode structure

HSC argues that "[t]his limitation requires the formation of spacers on the sidewalls of the gate electrode at the same time as the anisotropic etch step," and HSC contends that this distinguishes Doshi because "Doshi's specification teaches that nitride layer 30 is removed from the contact hole locations during the nitride etch step." PO Resp. 16–17.

HSC argues that "[t]he nitride etch process designed to clear the nitride layer 30 would etch every part of layer 30 exposed under the contact opening." PO Resp. 18–19. HSC cites to Doshi's disclosure that the brief and anisotropic nitride etch "clear[s] nitride layer 30 from within plug contact locations PC" and "remove[s] nitride layer 30 from bit line contact location BLC" as support that no portion of nitride layer 30 remains following the etch process. *Id.* at 17.

Samsung contends that a person of ordinary skill in the art reviewing Doshi would have readily recognized that Doshi retains a portion of its silicon nitride layer 30 on its sidewalls after the "highly anisotropic" etch. Reply 10. Samsung argues that this would have been evident in view of both the anisotropy of the etch and the expressly stated goal of Doshi to

minimize damage to gate structures 10 and sidewall filaments 11. *Id.* (citing Ex. 1005, 10:4–17; Ex. 1011 ¶ 2A). We agree with Samsung. Doshi explains that damage to Doshi's diffusion region 7, which would result from the aggressive over-etch necessary to completely remove the layer 30, would be undesirable. Ex. 1005, 10:4–17 ("because of this anisotropy in combination with its brevity, *minimizes damage* at the sidewall corner locations") (emphasis added). This highly anisotropic etch is distinguished from "conventional nitride etches," which may damage "sidewall corner locations NC illustrated in [Figure] 3g." *Id*.

Doshi describes a second etch of silicon nitride that exposes the diffusion region and simultaneously forms a spacer of silicon nitride on the sidewall of the gate electrode structure, as required by independent claims 1 and 9. Samsung directs our attention to Figure 3g of Doshi, reproduced below (red annotations added by Samsung).

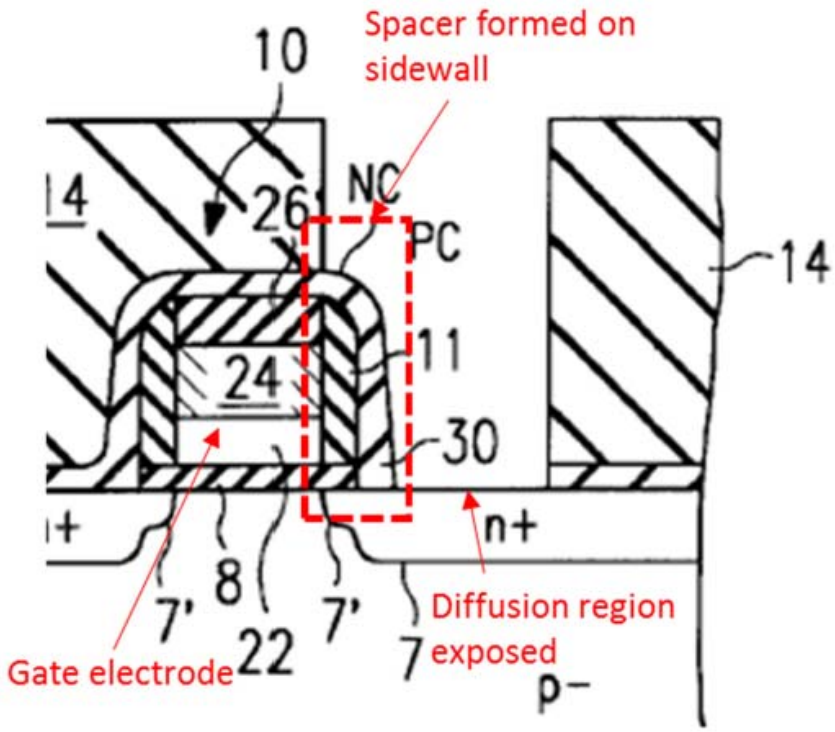

Fig. 3g, Doshi

Indeed, annotated Figure 3g of Doshi, reproduced above, "illustrates the construction of integrated circuit 20 after the completion of both etch steps, and the stripping of photoresist layer 32." Ex. 1005, 9:65–67. After the second etch, the silicon nitride layer 30 remaining on the sidewall of gate electrode 10 acts as a spacer, which provides a space as well as electrical insulation between gate electrode 10 and the contact plug to be filled in the contact hole.

HSC does not dispute that Figure 3g depicts a portion of nitride layer 30 remaining after the nitride etch. *See* PO Resp. 18. Instead, HSC essentially asks us to *ignore* Figure 3g—to give "little or no weight" to

Figure 3g of Doshi. Paper 31, 71:24. We cannot disregard Figure 3g, because patents are prior art for all they contain. "'The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain.'" *In re Heck*, 699 F.2d 1331, 1332–33 (Fed. Cir. 1983) (quoting *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)); *see also Upsher-Smith Labs. v. Pamlab, LLC*, 412 F.3d 1319, 1323 (Fed. Cir. 2005) (reference disclosing optional inclusion of a particular component teaches compositions that both do and do not contain that component); *Celeritas Techs. Ltd. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998) (The court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed."); *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962) ("[A] reference can anticipate a claim even if it 'd[oes] not expressly spell out' all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would 'at once envisage' the claimed arrangement or combination.").

We are not persuaded by HSC's Declarant Mr. Maltiel's testimony that the nitride etch process designed to clear the nitride layer 30 would etch away all of layer 30 exposed under the contact opening (*see* Ex. 2002 ¶ 67)—in direct contrast to what Figure 3g of Doshi depicts. Instead, we

find Figure 3g of Doshi depicts that nitride layer 30 remains after the second etch. *See* Ex. 1005, Fig. 3g. This is also consistent with Doshi's written description. Doshi describes an etch that "substantially minimize[s]" damage "to the corners of gate structures 10 and sidewall filaments 11." *Id*. at 10:4–16; Ex. 1011 ¶ 2E. In particular, once the nitride film 30 covering the NC of filaments 11 and gate structures 10 is etched through via the faster vertical etching of the highly anisotropic nitride etch, the subsequent additional etching time used to remove the remaining sidewall portions of film 30 would result in an etch of the NC portion of the filaments 11 and the gate structures 10. Ex. 1011 ¶ 2E. We agree with Samsung that during this additional time, given that filaments 11 are partially formed of silicon nitride, the highly anisotropic silicon nitride etch would etch into the portions of the filaments 11 formed of nitride. Reply 14 (citing Ex. 1005, 7:52–65; Ex. 1011 ¶ 2E). That scenario, proposed by HSC, would be contrary to Doshi's Figure 3g and to Doshi's "highly anisotropic" etch, which "minimizes damage" at the sidewall corner locations. Ex. 1005, 10:4–16. As Samsung argues, and we agree, if the goal is to minimize short circuits, then layer 30 would remain. *See* Reply at 15; Ex. 1011 ¶ 2E ("A POSITA would have understood that such damage to the structures 10 and sidewall filaments 11 undesirably increases the likelihood of shorts occurring between a contact plug and the gate electrode.").

HSC also asks us to disregard the entire portion of layer 30 depicted in Figure 3g because Dr. Rubloff stated that the corner of the silicon nitride layer 30 should have been depicted as being etched. PO Resp. 19 (citing

Ex. 1004, 203:11–204:15). Dr. Rubloff's testimony merely discusses removing the etch at a small portion of the corner of the sidewall, and not removing the *entire* layer of silicon nitride 30. *Id.*; *see also* Ex. 1011 ¶ 2E. Dr. Rubloff confirms that "one of ordinary skill would certainly conclude that the sidewall nitride structure remains [] as a spacer." Ex. 2004 at 181:6–15; Ex. 1011 ¶¶ 2F, 5A–5D.

HSC's also points to Figure 3k of Doshi to support its argument that the *entire* exposed portion of nitride layer 30 is removed from the bit line contact (BLC) formation location. PO Resp. 20–22. Figure 3k of Doshi omits nitride 30 along its sidewalls when otherwise illustrating structures involved in BLC formation. *See* Ex. 1005, Fig. 3k. Samsung did not rely on Figure 3k to satisfy the claims of the '997 patent, however, but relied on Figure 3g, which, as discussed above, shows forming a spacer of nitride 30 along sidewalls as part of plug contact (PC) formation. Samsung points out that the PC holes shown in Figure 3g are not even etched in the Figure 3k rendering. Reply 11. Samsung argues that Figure 3k fails to show a self-aligned contact hole formed by Doshi's two-step etching process. Reply 18; Ex. 1011, 3A. We agree with Samsung that the depiction of a contact hole in Figure 3k would not be consistent with a "self-aligned" contact hole as understood by a person of ordinary skill in the art, because there is no room for any lithographic misalignment. *Id.* at 20. Thus, we are not persuaded by HSC's arguments that Figure 3k would inform one skilled in the art to disregard the sidewalls 30 depicted in Figure 3g.

Moreover, as discussed above with respect to Figure 3g, we agree with Samsung that a *complete* removal of the silicon nitride layer 30 from the sidewalls of Doshi's contact holes using a highly anisotropic etch is inconsistent with Doshi's disclosure. A complete removal would damage the sidewall filaments 11 and expose gate structures 10 to potential damage, in direct contravention to Doshi's explicitly stated goal of minimizing damage to these structures. Ex. 1011 ¶ 2A. We agree that a person of ordinary skill in the art would have understood that a "highly anisotropic" etch generally indicates that the etch rate in a perpendicular/vertical direction (i.e., etching from top to bottom) is much greater than the etch rate in a lateral/horizontal direction (i.e., etching from the side). Ex. 1014, 3; Ex. 1011 ¶¶ 2B–2C. This is also consistent with Dr. Rubloff's testimony that a person of ordinary skill in the art would have understood that a nitride sidewall spacer would be formed, not completely removed, after the nitride etch. Ex. 1003 ¶¶ A13–A14; Ex. 2004, 181:6–15; *see also* Ex. 1011 ¶¶ 2F, 5A–5D. As confirmed by Mr. Maltiel's testimony during his cross-examination, the taller the structure on the sidewall, the harder it would be to remove the structure. Ex. 1012, 159:7–15. Mr. Maltiel also acknowledged during his cross-examination that the vulnerability of a diffusion region to etch damage caused by a long over-etch when discussing the '997 patent by acknowledging that, when etching, one "can likely damage it if you go for too long." Ex. 1012, 156:2–14.

Based on Doshi's disclosure and the evidence before us, we agree with Dr. Rubloff's testimony that Doshi's anisotropic etch of the etch-barrier

nitride layer exposes the diffusion region and simultaneously forms a spacer on the sidewall of the gate electrode, as Dr. Rubloff's testimony is consistent with the Doshi's disclosure. Ex. 1003 ¶¶ A13–A14; Ex. 2004, 181:6–15; Ex. 1011 ¶¶ 2F, 5A–5D; *see also* Ex. 2005, 10:4–16, Figs. 3g–3k. In light of the foregoing, we credit the testimony of Dr. Rubloff over Mr. Maltiel's testimony (Ex. 2002 ¶¶ 47–52) filed in support of HSC's argument. *See* 37 C.F.R. § 42.65(a); *see also Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding that the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so").

HSC also argues that nitride layer 30 already functions as a spacer before the anisotropic etch, and therefore cannot be "simultaneously" formed during the nitride etch process. PO Resp. 22–23. HSC argues that a spacer cannot be "formed" if it already exists before the etch. *Id.* at 24. We are not persuaded by this argument because the '997 patent describes the *same way* of forming a spacer. Figure 2D of the '997 patent and Figure 3g of Doshi are reproduced side by side below, with annotations by Samsung.

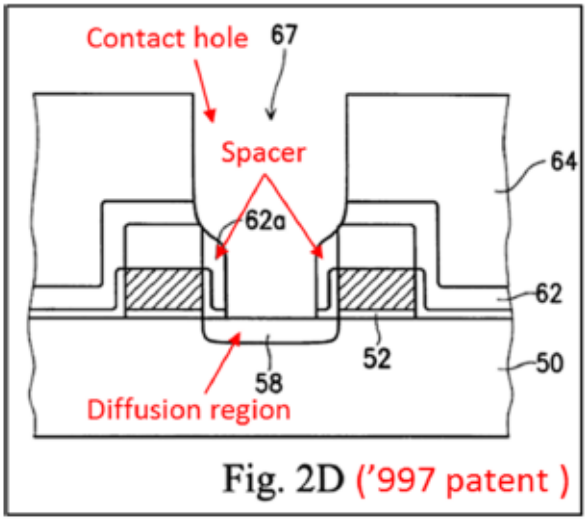

Fig. 2D ('997 patent)

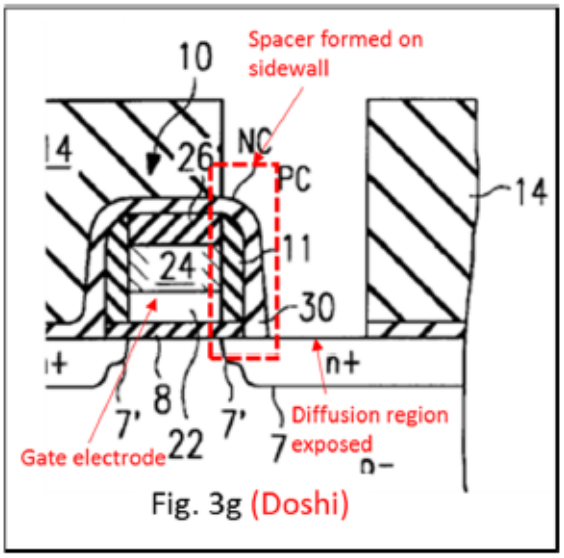

Fig. 3g (Doshi)

As shown in annotated Fig. 2D of the '997 patent, reproduced above, a planarized inter-layer dielectric (ILD) insulating layer 64 is formed over the conformal layer of silicon nitride 62, and a photoresist layer 66 is formed and patterned to expose a contact hole (shown in Fig. 2C reproduced above). Ex. 1001, 3:1–24. In this process, a highly selective first etch is performed to etch away the insulating layer 64. *Id*. The nitride layer 62 is then anisotropically etched to expose a portion of the diffusion region 58. *Id.* at 3:1–24. Due to the directionality of anisotropic etching, a portion of nitride layer 62 remains on the sidewall of the electrode 54 upon completion of the etch, thus forming spacers 62a. *Id.;* Reply at 8. Doshi discloses a method of fabricating self-aligned contacts in the same way. Ex. 1005, Abstract; Ex. 1003, ¶ A-1. In Doshi, after gate electrodes 10, diffusion regions 7/7', gate oxides 8, and sidewall filaments 11 have been formed on a substrate 2, a conformal layer of nitride layer 30 is deposited, followed by a formation of a

BPSG layer 14. Ex. 1005, Figs. 3a–3d, 7:29–9:24. Doshi then describes etching contact openings through the BPSG insulating layer 14 and the nitride layer 30 using a two-step etch process. *Id.* at Abstract, 9:25–10:16. The first step involves selectively etching BPSG insulating layer 14 relative to the nitride layer 30. *Id.* The second step involves a highly anisotropic etch that exposes the diffusion region 7. This second step, due to the anisotropic nature of the etch, removes the thin surface of layer 30 more quickly than the thick vertical wall of layer 30, leaving a spacer of nitride 30 on the sidewall of the gate electrode structure 10, as shown in the annotated Fig. 3g above. *Id.* at 10:11-16; Ex. 1003, ¶¶ A-12 to A-14. As shown by annotated Figure 2D of the '997 patent and Figure 3g of Doshi, these processes are consistent.

Samsung also points out that HSC does not account for the fact that Doshi's anisotropic etch forms a new structure that is also a spacer. Reply 22. We agree that Doshi's anisotropic nitride etch process etches nitride barrier layer 30 underneath the PC opening, and simultaneously forms a spacer that is physically different from the unetched pre-existing spacer. *Id.* at 23 (citing Ex. 1005, Fig. 3g). As Samsung points out, Dr. Rubloff's testimony does not contradict this argument. *Id.* Rather, HSC has omitted statements made by Dr. Rubloff after the statements quoted by HSC. PO Resp. 23–24. HSC argues that Dr. Rubloff has confirmed that the *claimed* "spacer" already exists *before* the contact etch process. *Id.* at 24. However, as Samsung points out, the portion of testimony that HSC quotes is

incomplete at best. Dr. Rubloff actually points out "that's not the spacer that's at issue here. I realize that." Ex. 2004, 196:10–197:1.

Accordingly, we are unpersuaded by HSC's argument that nitride layer 30 already functions as a spacer before the anisotropic etch, and therefore the spacer cannot be "simultaneously" formed during the nitride etch process. Instead, we find the silicon nitride layer 30 remaining on the sidewall of gate electrode 10 acts as a spacer, which provides a space as well as electrical insulation between gate electrode 10 and the contact plug to be filled in the contact hole. Ex. 1005, 9:65–67, Fig. 3g.

For the foregoing reasons, we determine that Doshi describes anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode, as recited in the claims at issue.

4. Forming an oxide layer over the diffusion region

As discussed, we have construed "forming an oxide layer over the diffusion region" as recited in dependent claim 2 and independent claim 9 to mean forming an oxide layer above the diffusion region.

As an initial matter, HSC presents arguments and expert testimony that Doshi does not teach "forming an oxide layer over the diffusion region" because during the oxidation of the polysilicon gate sidewalls, the diffusion regions are covered by the gate oxide layer, which HSC states is not removed until after the oxidation process. PO Resp. 27–28; Ex. 2002 ¶¶ 81–82. Those arguments and testimony, however, are predicated on HSC's

construction of "over" the diffusion region to require completely covering the diffusion region. *See* PO Resp. 27–28; Ex. 2002 ¶¶ 81–82. We have already determined not to adopt that proposed claim construction for the reasons discussed above in our claim construction analysis in regard to the claim term "forming an oxide layer over the diffusion region."

Samsung contends that Doshi describes forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode, as required by claims 2 and 9, and forming the oxide layer by thermal oxidation prior to forming the barrier layer, as required by claim 2. Pet. 27–29, 34. We agree with Samsung. Doshi describes that sidewall filaments 11 are formed by first oxidizing the sides of polysilicon layer 22. Ex. 1005, 7:52–59. Figure 3b of Doshi is reproduced below (annotations by Samsung):

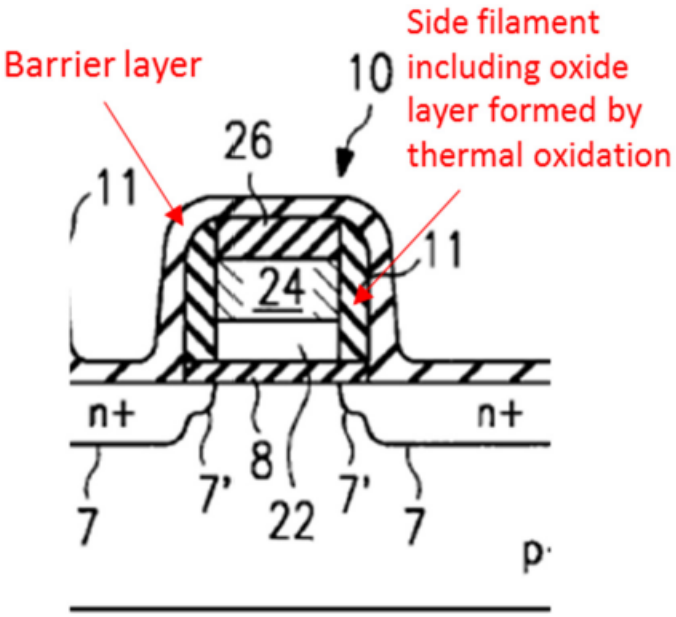

Fig. 3b, Doshi

Figure 3b, reproduced above with annotations by Samsung, illustrates that the barrier layer (i.e., the silicon nitride layer 30) is formed *after* the formation of the filaments 11, and therefore, we agree that Doshi discloses forming an oxide layer on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. We also agree with Samsung that Doshi discloses the oxidization of the sidewall filaments 11 is above the diffusion region, which includes source/drain extensions 7'. Pet. 28; Ex. 1005, Fig. 3b, 7:52–59; Ex. 1003 ¶ A-7.

HSC argues that Doshi only states that the sides of the polysilicon layer are oxidized, does not disclose forming an oxide over diffusion regions, and never depicts such an oxide layer. PO Resp. 24–25. We are not persuaded by HSC's arguments and expert testimony that the oxide on the sidewalls of the gate electrode are not "over" the diffusion region. PO Resp. 25–26; Ex. 2002 ¶¶ 78–79. Those arguments and testimony are predicated on HSC's construction of "over" to require covering or rather, *entirely* covering. *See, e.g.*, PO Resp. 26 ("The word 'over' as it is used in the claim limitation and in the specification should be understood to mean covering. Thus, any oxide layer that satisfies the claim limitation must be formed such that it covers the diffusion region."); Ex. 2002 ¶ 79. We have already determined not to adopt that proposed claim construction for the reasons discussed above in our claim construction analysis in regard to the claim term "forming an oxide layer over the diffusion region."

We are also not persuaded by HSC's argument that Figure 3b of Doshi merely depicts an oxide layer "higher but off to the side." PO Resp.

26–27. HSC reproduces and annotates Figure 3b of Doshi, as reproduced below.

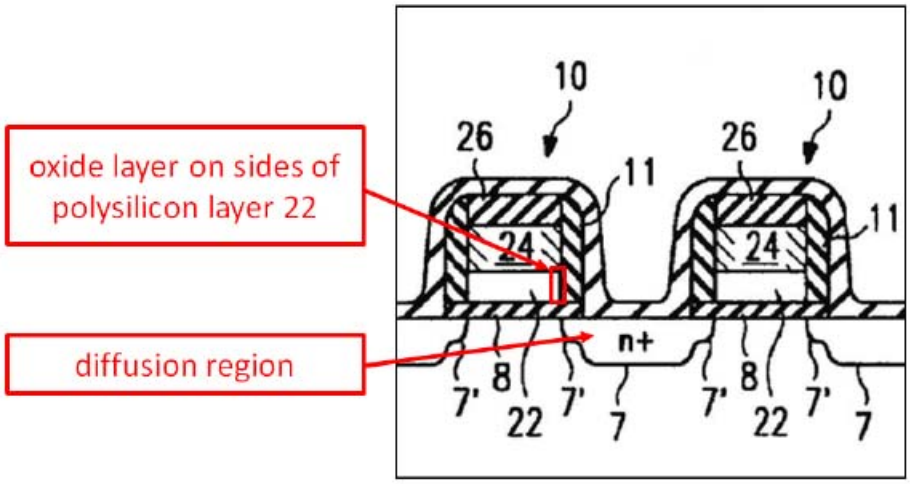

Figure 3b, as reproduced above, illustrates a cross-sectional diagram of an integrated circuit, with annotations by HSC. *See* Ex. 1005, 4:60–63. We interpret HSC's argument and annotations as an argument that we should interpret this *two-dimensional representation* ("a cross-sectional" diagram) of a *three-dimensional* integrated circuit in a way that would presumably mean the oxide layer on the sides of polysilicon layer 22 is not over, or even above, any part of the diffusion region. We are not persuaded by this argument. Instead, Doshi depicts the oxide layer, in a cross-section, as being above the diffusion region, which includes source/drain extension 7'. Additionally, when Figure 3b is considered as a cross-section of a three-dimensional integrated circuit, it is even more clear that the oxide layer (filaments 11) is above the diffusion region, for example as shown by Samsung's annotated version of Figure 3b, which was reproduced above.

Samsung's annotated version of Figure 3b makes clear that the oxide layer is above the diffusion region. As discussed above, therefore, we agree with Samsung that Doshi discloses the oxide layer (sidewall filaments 11) is above the diffusion region, and not merely "off to the side" as argued by HSC. PO Resp. 27; *see also* Pet. 28; Ex. 1005, Fig. 3b, 7:52–59; Ex. 1003 ¶ A-7.

For the foregoing reasons, we determine that Doshi discloses forming an oxide layer on the sidewalls of the gate electrode, as recited in claims 2 and 9, and forming the oxide layer by thermal oxidation prior to forming the barrier layer, as required by claim 2.

5. Dependent Claims 3–8 and 10–14

Samsung contends that claims 3–8 and 10–14 are anticipated by Doshi. Pet. 29–33, 35–36. As support, Samsung provides detailed explanations as to how the combination of prior art meets each claim limitation. *Id.* Samsung also relies upon the Declaration of Dr. Rubloff (Ex. 1003). HSC does not specifically challenge any aspect of each of the dependent claims in its Response. *See* PO Resp. 2–29.

Upon consideration of Samsung's explanations and supporting evidence, we are persuaded by Samsung's contentions. We analyze each of the dependent claims 3–8 and 10–14 in more detail below.

i. Dependent Claims 3 and 10

Dependent claim 3 requires that "said gate electrode comprises a capping layer of silicon nitride." Ex. 1001, 4:9–10. Dependent claim 10

requires that "said capping layer is a silicon nitride layer." *Id.* at 4:48–49. Samsung directs our attention to Doshi, which discloses "gate structures 10 are formed as layered structures, including polysilicon layer 22 in contact with gate oxide 8, tungsten silicide layer 24 overlying polysilicon layer 22, and silicon nitride layer 26 overlying tungsten silicide layer 24." Pet. 20, 29 (citing Ex. 1005, 7:40–43)). We agree that this description in Doshi discloses "said gate electrode comprises a capping layer of silicon nitride," as recited in claim 3 and "said capping layer is a silicon nitride layer," as recited in claim 10.

ii. Dependent Claim 4

With respect to claim 4, which requires the barrier layer is a silicon nitride layer, Samsung directs our attention to Doshi's disclosure that "[a]ccording to the preferred embodiment of the invention, *silicon nitride layer 30* is now formed overall, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in [Figure] 3b." Pet. 30 (citing Ex. 1005, 8:8–11). We agree that this description in Doshi discloses the "barrier layer is a silicon nitride layer," as recited in dependent claim 4.

iii. Dependent Claims 5 and 11

Dependent claim 5 requires that "said barrier layer has a thickness between about 100 to 500Å" and dependent claim 11 requires that "said conformal layer of silicon nitride has a thickness between about 100 to 500Å." Ex. 1001, 4:13–14, 51–53. Samsung directs our attention to

Doshi's disclosure that "the thickness of nitride layer 30 may range from *65Å to 250Å*." Pet. 30 (citing Ex. 1005, 8:19–20). Samsung argues the '997 patent fails to demonstrate any criticality of the recited thickness of between about 100 to 500 Å, and therefore, the claim is anticipated by Doshi's disclosure of a thickness from 65 to 250 Å. Pet. 30.

"[W]hen, as by a recitation of ranges or otherwise, a claim covers several compositions, the claim is 'anticipated' if *one* of them is in the prior art." *Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 782 (Fed. Cir. 1985) (internal citation omitted). If there is no allegation of criticality of the claimed range, or any demonstration that the prior art reference fails to teach one of ordinary skill in the art how to use the claimed invention, then the claim may be anticipated even if the exact range is not disclosed. *See ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012).

We are persuaded by Samsung's argument that Doshi anticipates the claimed range. Moreover, we find that the '997 patent describes, in its "Description of the Related Arts," with respect to Figure 1D which is labeled "Prior Art," that a "barrier layer is typically a silicon nitride layer having a thickness of about 100 to 500 Å." Ex. 1001, 1:44–46, Fig. 1D. Accordingly, we find that Doshi anticipates claims 5 and 11.

iv. Dependent Claims 6 and 12

Dependent claims 6 and 12 require "said insulating layer comprises a layer of borophosphosilicate." Ex. 1001, 4:15–17, 54–56. We are persuaded by Samsung's argument that Doshi discloses this limitation. In particular,

Doshi discloses that "[r]eferring now to [Figure] 3c, integrated circuit 20 is[] illustrated after the deposition of doped BPSG silicon dioxide layer 14. BPSG layer 14 is preferably deposited in the conventional manner, for example by way of LPCVD, doped with both boron and phosphorous." Ex. 1005, 8:23–27. Doshi discloses that the insulating layer 14 is formed using "BPSG," which is an acronym for borophosphosilicate glass. Ex. 1003 ¶ A-8. Accordingly, we find that Doshi discloses that "said insulating layer comprises a layer of borophosphosilicate glass," as recited in claims 6 and 12.

v. Dependent Claim 7

Dependent claim 7 requires "depositing an insulating layer overlying the barrier layer" and "planarizing the insulating layer." Ex. 1001, 4:18–22. We are persuaded by Samsung's argument that Doshi discloses these limitations. In particular, Doshi discloses depositing a BPSG layer 14 above the silicon nitride layer 30. "A silicon nitride layer (30) is in place below the BPSG layer (14), and serves as a barrier to the diffusion of boron and phosphorous from the BPSG layer (14) during high temperature processes such as reflow and densification of the BPSG layer (14) itself." Ex. 1005, Abstract.

Doshi discloses "planarizing the insulating layer" because

> [f]ollowing deposition and anneal [of the BPSG layer 14], a *planarization etchback of BPSG layer* 14 is performed according to this preferred embodiment of the invention. This etchback is performed without patterning, and is preferably a

> timed etch selected so that BPSG layer 14 remains over the top of all underlying structures.

Ex. 1005, 8:66–9:4 (emphasis added).

Accordingly, we find that Doshi discloses "depositing an insulating layer overlying the barrier layer" and "planarizing the insulating layer," as recited in claim 7.

vi. Dependent Claims 8 and 14

Dependent claims 8 and 14 both require "forming a conductive plug in said opening to electrically connect to the diffusion region." Ex. 1001, 4:23–26, 62–64. Doshi discloses that "[f]ollowing definition of plug contact openings PC, *polysilicon plugs are formed* therewithin, *in contact with source/drain regions 7*." Ex. 1005, 10:17–19 (emphases added). Accordingly, we find that Doshi discloses "forming a conductive plug in said opening to electrically connect to the diffusion region," as recited in claims 8 and 14.

Therefore, we determine that Samsung has shown by a preponderance of the evidence that claims 3–8 and 10–14 are anticipated by Doshi.

CONCLUSION

We conclude that Samsung has shown by a preponderance of the evidence that claims 1–14 of the '997 patent are anticipated by Doshi.

III. ORDER

For the foregoing reasons, it is

ORDERED that claims 1–14 of the ’997 patent are held unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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