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PATENT APPLICATION



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Claim	Date
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United States Patent [19]  
Banks

[11] Patent Number: 5,764,571  
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[54] ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL

WO90/01984 3/1990 WIPO.

OTHER PUBLICATIONS

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[73] Assignee: BTG USA Inc., Gulph Mills, Pa.  
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[22] Filed: Feb. 27, 1995

M. Bauer et al., *A Multilevel-Cell 32Mb Flash Memory*, 1995 IEEE International Solid-State Circuits Conference, Session 7, Paper TA7.7.  
John A. Bayliss et al., *The Interface Processor for the 32b Computer*, 1981 IEEE International Solid-State Circuits Conference, Feb. 1981, at 116-117.  
Christoph Bleiker & Hans Melchior, *A Four-State EEPROM Using Floating-Gate Memory Cells*, IEEE Journal of Solid-State Circuits, vol. SC-22, No. 3, Jun. 1987, at 260-263.  
Raymond A. Heald & David A. Hodges, *Multilevel Random-Access Memory Using One Transistor Per Cell*, IEEE Journal of Solid-State Circuits, vol. SC-11, No. 4, Aug. 1976, at 519-528.  
David A. Rich, *A Survey of Multivalued Memories*, IEEE Transactions on Computers, vol. C-35, No. 2, Feb. 1986, at 99-106.  
R.S. Withers et al., *Nonvolatile Analog Memory in MNOS Capacitors*, IEEE Electron Device Letters, vol. EDL-1, No. 3, Mar. 1980, at 42-45.

Related U.S. Application Data

[62] Division of Ser. No. 71,816, Jun. 4, 1993, Pat. No. 5,394,362, which is a continuation of Ser. No. 652,876, Feb. 8, 1991, Pat. No. 5,218,569.  
[51] Int. Cl.<sup>6</sup> G11C 13/00  
[52] U.S. Cl. 365/189.01; 365/189.07; 365/168; 365/201  
[58] Field of Search 365/189.01, 189.07, 365/168, 201

[56] References Cited

U.S. PATENT DOCUMENTS

3,660,819 5/1972 Frohman-Bentchkowsky ... 317/235 R  
3,801,965 4/1974 Keller et al. ... 340/173 R  
4,004,159 1/1977 Rai et al. ... 307/238  
4,054,864 10/1977 Andaine et al. ... 340/173 R  
4,090,258 5/1978 Cicchi ... 365/184

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

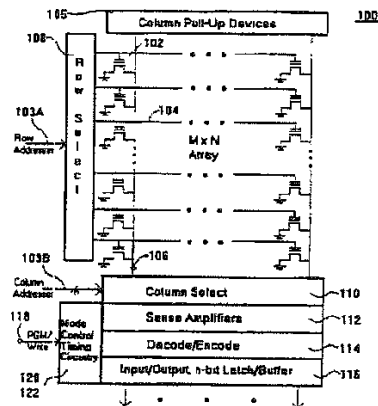
0 390 404 10/1990 European Pat. Off.  
2 630 574 10/1989 France  
WO8202276 7/1982 WIPO  
WO8202976 9/1982 WIPO

Primary Examiner—Terrell W. Fears  
Attorney, Agent, or Firm—Shapiro and Shapiro

[57] ABSTRACT

An electrically alterable, non-volatile multi-bit memory cell has  $K^n$  predetermined memory states ( $K^n > 2$ ), where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per cell. Programming of the cell is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal.

47 Claims, 14 Drawing Sheets



5,764,571

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U.S. PATENT DOCUMENTS

4,122,541	10/1978	Uchida	365/154	5,043,940	8/1991	Harari	365/168
4,139,910	2/1979	Anantha et al.	365/183	5,095,344	3/1992	Harari	357/23.5
4,149,270	4/1979	Cicchi et al.	365/222	5,163,021	11/1992	Mehrotra et al.	365/185
4,181,980	1/1980	McCoy	365/45	5,172,338	12/1992	Mehrotra et al.	365/185
4,192,014	3/1980	Craycraft	365/104	5,218,569	6/1993	Banks	365/189.01
4,272,830	6/1981	Moenach	365/45	5,258,958	11/1993	Iwahashi et al.	365/210
4,287,570	9/1981	Stark	365/104	5,262,984	11/1993	Noguchi et al.	365/185
4,300,210	11/1981	Chakravarti et al.	365/45	5,268,870	12/1993	Harari	365/218
4,306,300	12/1981	Terman et al.	365/45	5,293,560	3/1994	Harari	365/185
4,327,424	4/1982	Wu	365/104	5,295,255	3/1994	Malcock et al.	395/425
4,357,685	11/1982	Danielle et al.	365/189	5,321,655	6/1994	Iwahashi et al.	365/200
4,388,702	6/1983	Sheppard	365/104	5,351,210	9/1994	Saito	365/189.01
4,413,992	11/1983	Adiboch	365/94	5,422,845	6/1995	Ong	365/185
4,449,203	5/1984	Adiboch	365/104	5,432,735	7/1995	Parks et al.	365/168
4,462,088	7/1984	Giuliani et al.	365/105	5,434,825	7/1995	Harari	365/185
4,495,602	1/1985	Sheppard	365/104	5,440,505	8/1995	Fazio et al.	365/45
4,503,518	3/1985	Iwahashi	365/104	5,444,656	8/1995	Bauer et al.	365/189.01
4,558,241	12/1985	Suzuki et al.	307/530	5,450,363	9/1995	Christopherson et al.	365/205
4,578,777	3/1986	Fang et al.	365/184	5,457,650	10/1995	Sugiura et al.	365/184
4,586,163	4/1986	Koike	365/104	5,469,384	11/1995	Lacey	365/185.13
4,627,027	12/1986	Rai et al.	365/45	5,475,693	12/1995	Christopherson et al.	371/10.2
4,633,023	3/1987	Suzuki et al.	365/104	5,485,422	1/1996	Bauer et al.	365/168
4,661,929	4/1987	Aoki et al.	365/189	5,497,119	3/1996	Todrow et al.	327/540
4,709,350	11/1987	Nakagome et al.	365/45	5,506,813	4/1996	Mochizuki et al.	365/230.03
4,733,394	3/1988	Giebel	371/21	5,508,958	4/1996	Fazio et al.	365/185.19
4,771,404	9/1988	Mano et al.	365/189	5,515,317	5/1996	Wells et al.	395/427
4,799,195	1/1989	Iwahashi	365/185	5,523,972	6/1996	Rashid et al.	365/185.22
4,809,224	2/1989	Suzuki et al.	365/168	5,539,690	7/1996	Talreja et al.	365/185.22
4,847,808	7/1989	Kobatake	364/104	5,541,886	7/1996	Harbun	365/230.01
4,853,892	8/1989	Hori	365/49	5,544,118	8/1996	Harari	365/218
4,890,259	12/1989	Simko	365/45	5,550,772	8/1996	Gill	365/185.03
4,914,631	4/1990	Johnson et al.	365/189.11	5,568,439	10/1996	Harari	365/218
4,964,079	10/1990	Devlin	365/168	5,583,812	12/1996	Harari	365/185.33
4,989,179	1/1991	Simko	365/45	5,594,691	1/1997	Bashir	365/189.09
5,021,999	6/1991	Kobda et al.	365/168	5,596,527	1/1997	Tomioaka et al.	365/185.2

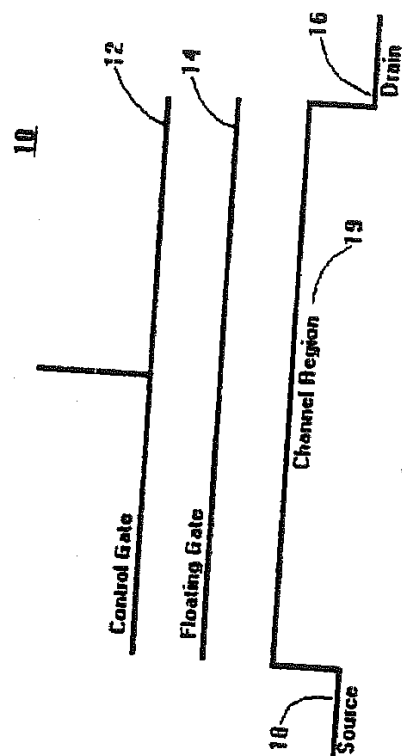
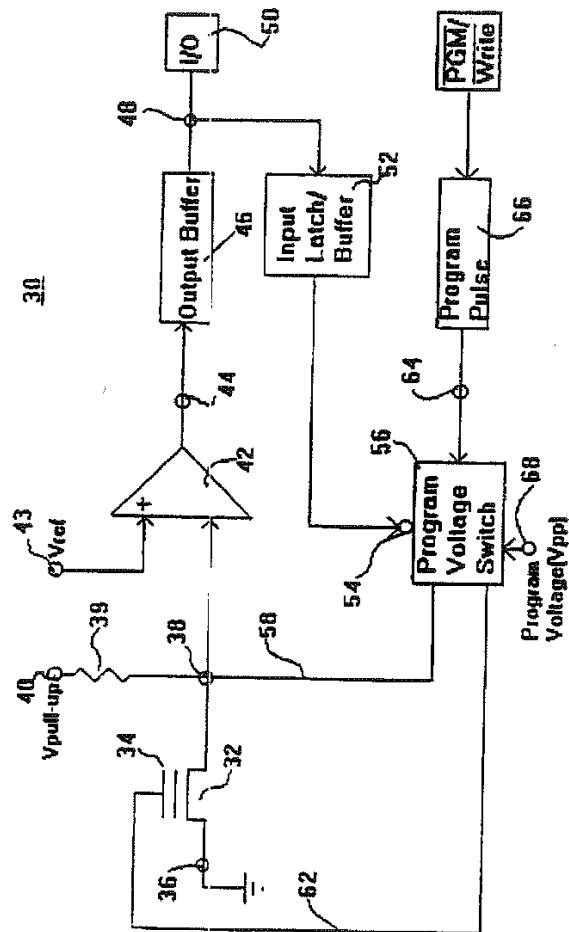


Figure 1



Prior Art  
Figure 2

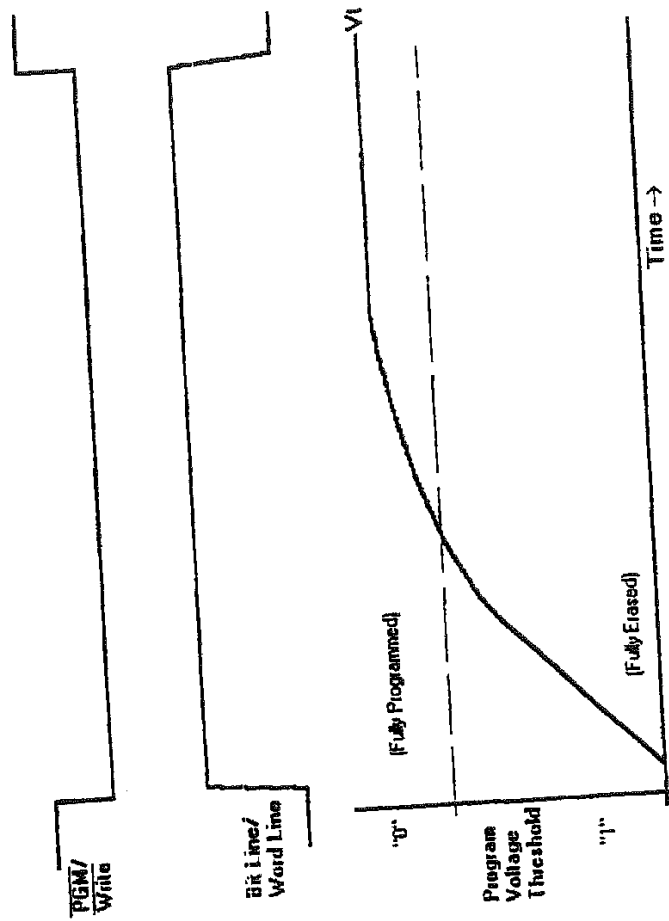
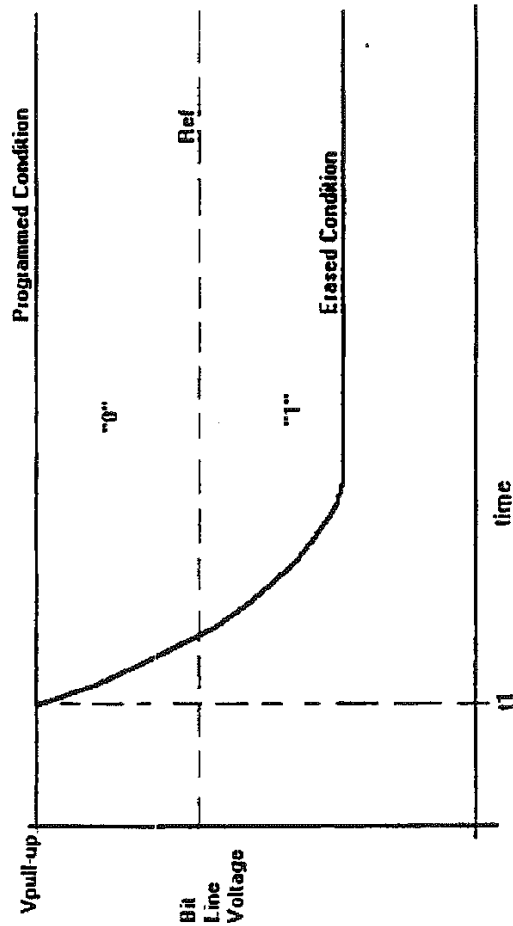


Figure 3



Prior Art Read  
Figure 4



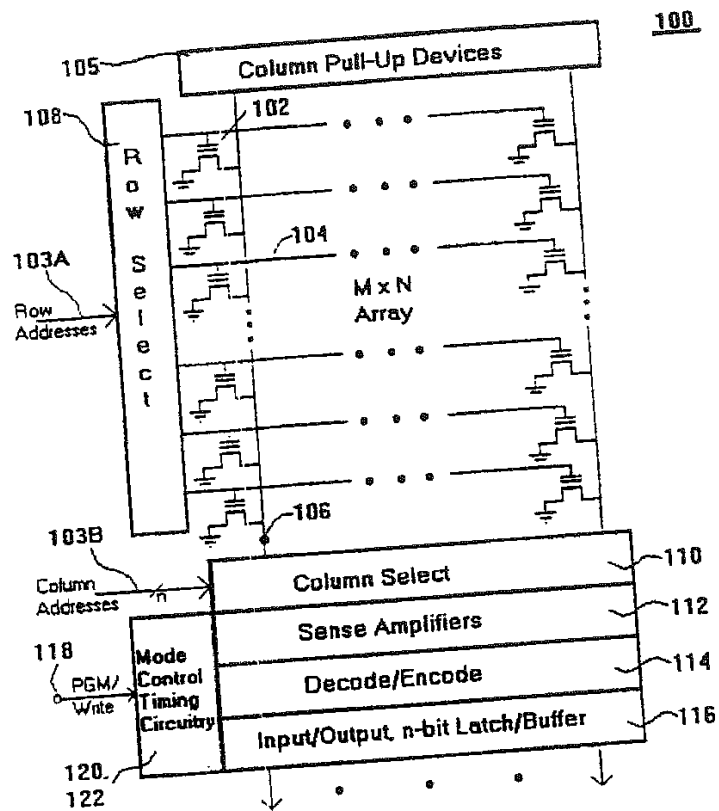


Figure 5

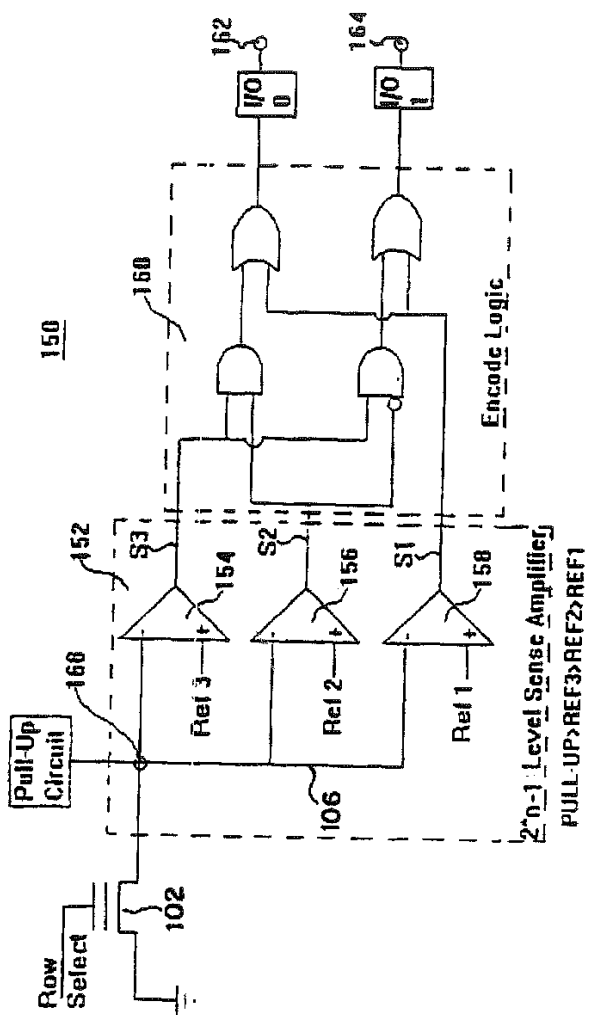


Figure 6

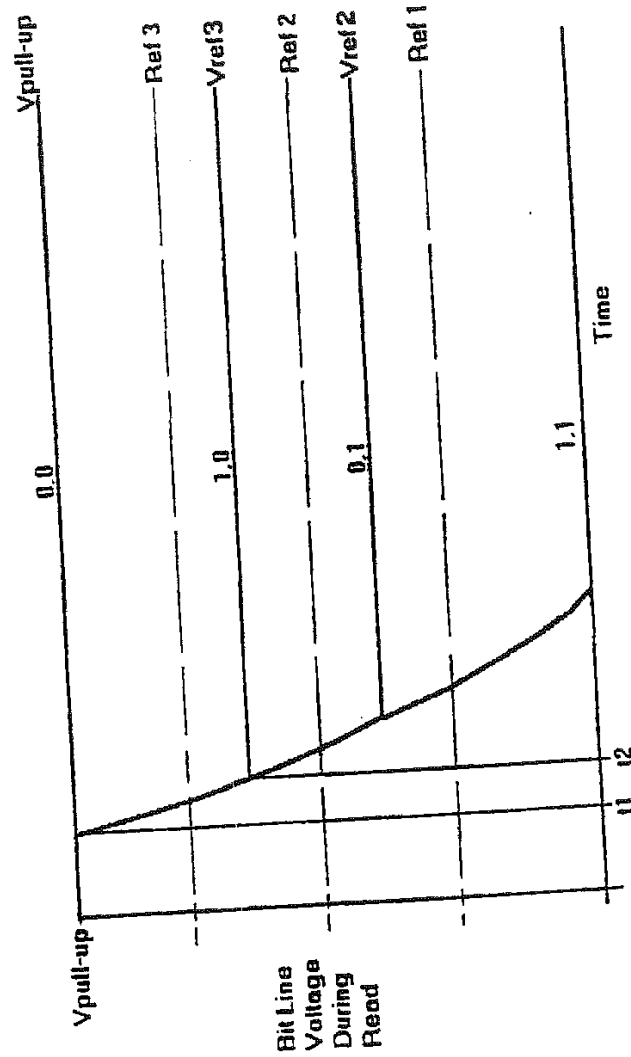


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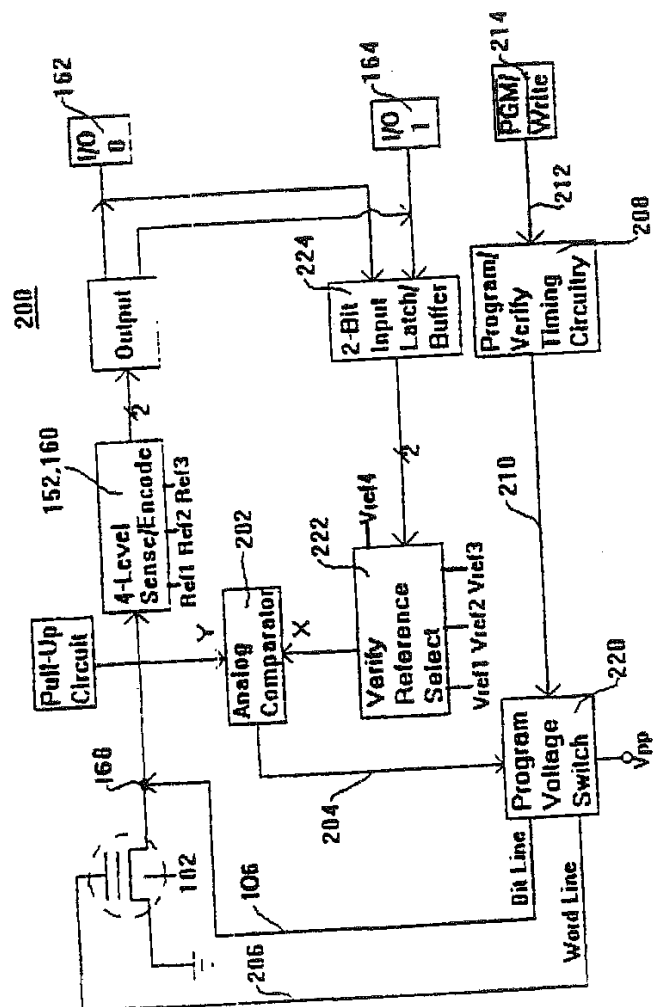


Figure 8

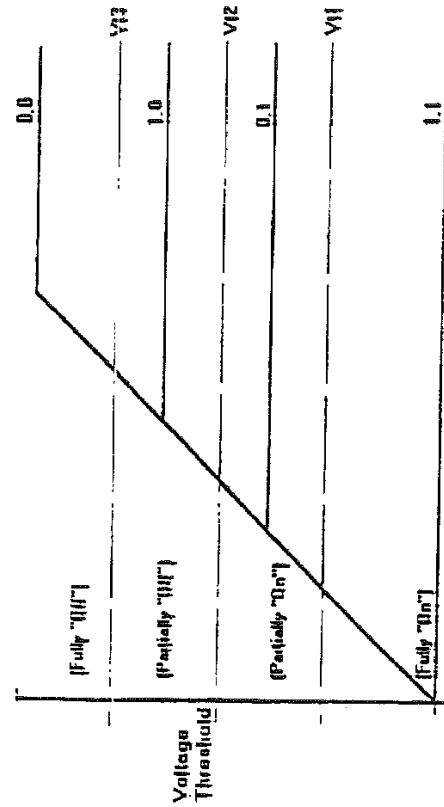


Figure 9

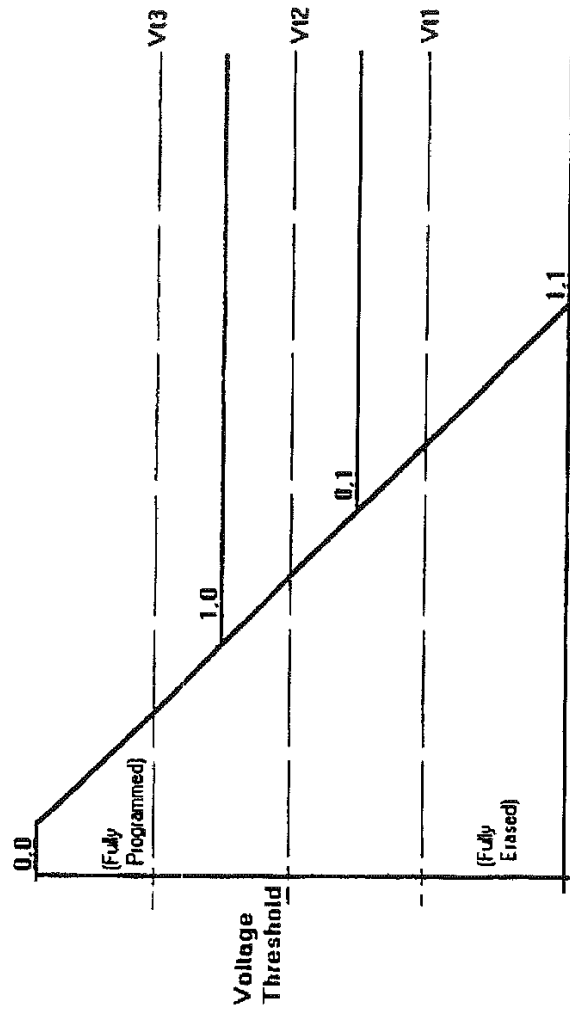


Figure 10

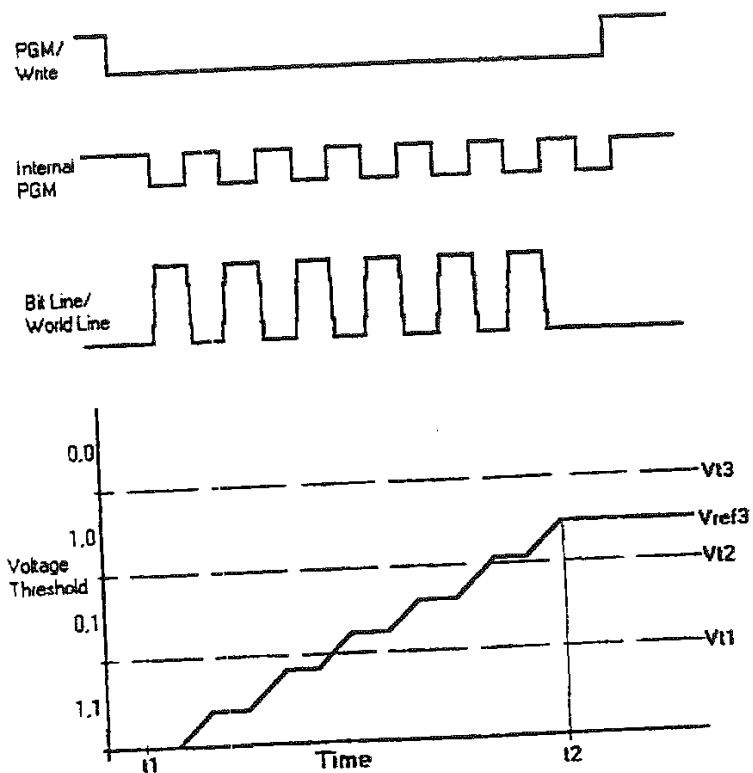


Figure 11

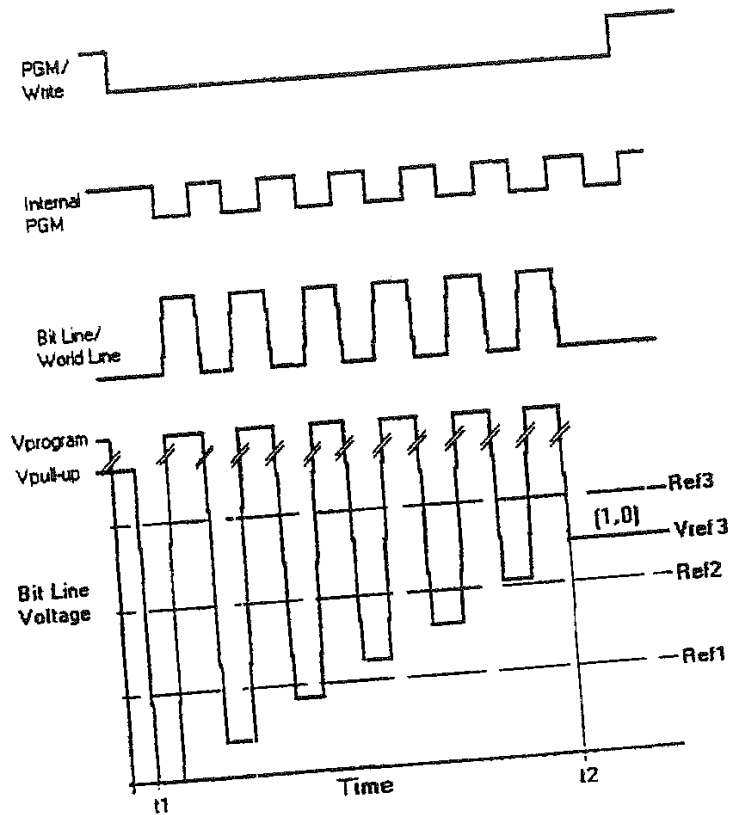


Figure 12



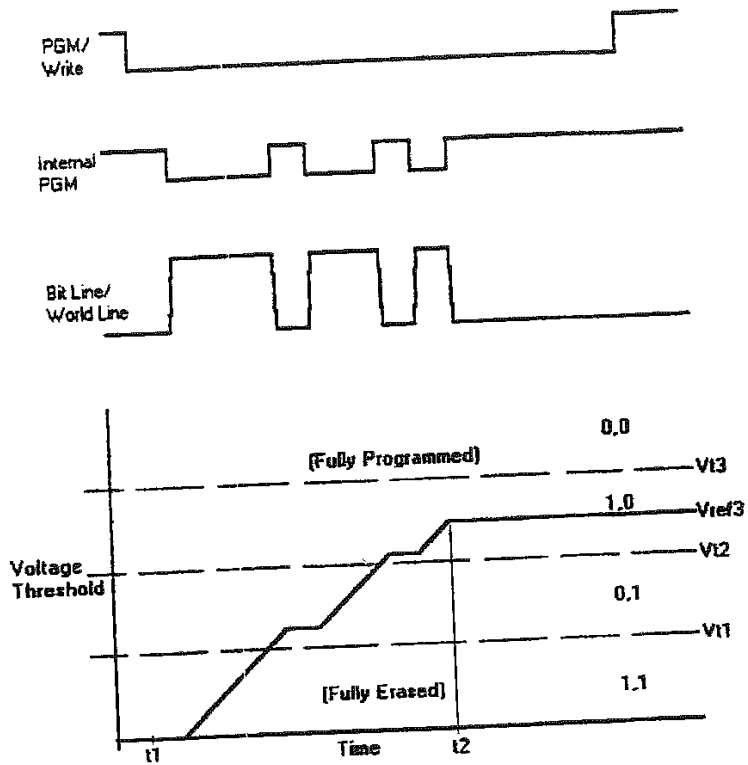


Figure 13

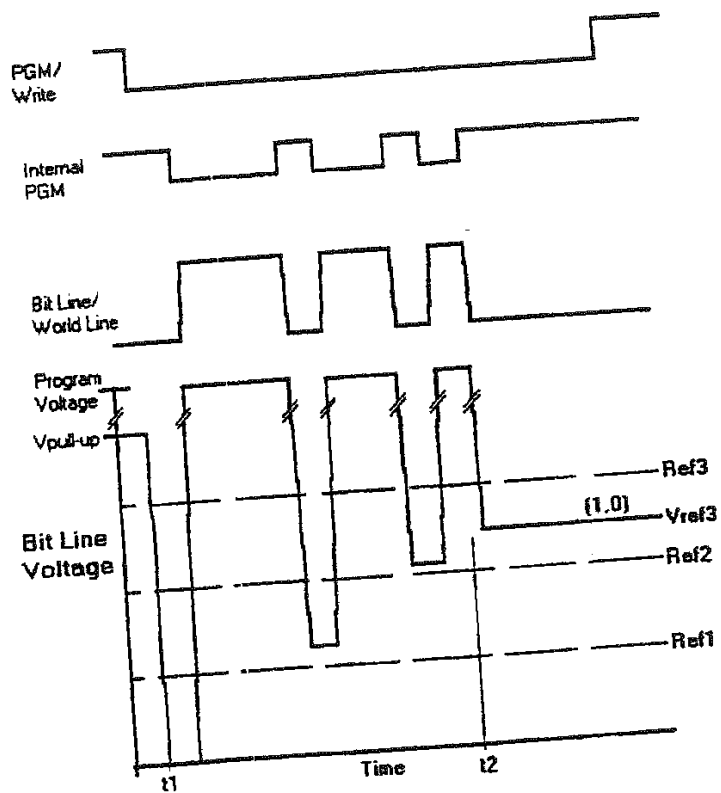


Figure 14

# 1 ELECTRICALLY ALTERABLE NON- VOLATILE MEMORY WITH N-BITS PER CELL

## Cross Reference to Related Applications

This application is a continuation-in-part of U.S. patent application Ser. No. 08/071,816, filed Jan. 4, 1993 entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Memory Cell," now U.S. Pat. No. 5,394,362, which is a continuation of U.S. patent application Ser. No. 07/652,878, filed Feb. 8, 1991 (now U.S. Pat. No. 5,218,569) entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Cell."

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to non-volatile memory (NVM) devices; and, more particularly, is concerned with an apparatus and method for programming and/or verifying programming of a multi-level NVM device with stable reference voltages.

### 2. Description of the Background Art

In conventional single-bit per cell memory devices, the memory cell assumes one of two information storage states, either an "on" state or an "off" state. This combination of either "on" or "off" defines one bit of information. As a result, a memory device which can store n-bits of data requires n separate memory cells.

Increasing the number of bits which can be stored in a single-bit per cell memory device relies upon increasing the number of memory cells on a one-for-one basis with the number of bits of data to be stored. Methods for increasing the number of memory bits in a single memory device have relied upon the following advanced manufacturing techniques: manufacture larger die which contain more memory cells; or use improved lithography techniques to build smaller memory cells and allow more memory cells to be placed in a given area on a single chip.

An alternative approach to the single-bit per cell approach involves storing multiple-bits of data in a single memory cell. Previous approaches to implementing multiple-bit per cell non-volatile memory devices have only involved mask programmable read only memories (ROMs). In one of these approaches, the channel width and/or length of the memory cell is varied such that  $2^n$  different conductivity values are obtained which correspond to  $2^n$  different states corresponding to n-bits of data which can be stored on a single memory cell. In another approach, the ion implant for the threshold voltage is varied such that the memory cell will have  $2^n$  different voltage thresholds ( $V_t$ ) corresponding to  $2^n$  different conductance levels corresponding to  $2^n$  different states corresponding to n-bits of data which can be stored on a single memory cell. Examples of memory devices of these types are described in U.S. Pat. No. 4,192,014 by Craycraft, U.S. Pat. No. 4,586,163 by Kolke, U.S. Pat. No. 4,287,570 by Stark, U.S. Pat. No. 4,327,424 by Wu, and U.S. Pat. No. 4,847,808 by Kobatake.

Single-bit per cell read-only-memory devices are only required to sense, or read, two different levels or states per cell, consequently they have need for only one voltage reference. Sensing schemes for multi-level memory devices are more complex and require  $2^n - 1$  voltage references. Examples of such multiple state sensing schemes for ROMs are described in U.S. Pat. No. 4,449,203 by Adlhoch, U.S. Pat. No. 4,493,602 by Shepard, U.S. Pat. No. 4,503,578 by Iwahashi, and U.S. Pat. No. 4,653,023 by Suzuki.

2

These approaches to a multi-bit ROM commonly have one of  $2^n$  different conductivity levels of each memory cell being determined during the manufacturing process by means of a customized mask that is valid for only one data pattern. Thus, for storing n different data information patterns, a minimum of n different masks need to be produced and incorporated into a manufacturing process. Each time a data information pattern needs to be changed a new mask must be created and a new batch of semiconductor wafers processed. This dramatically increases the time between a data pattern change and the availability of a memory product programmed with that new data pattern.

Prior art electrically alterable multiple-bit per cell memory approaches store multiple levels of charge on a capacitive storage element, such as is found in a conventional dynamic random access memory (DRAM) or a charge coupled device (CCD). Such approaches are described in U.S. Pat. No. 4,139,910 by Anantha, U.S. Pat. No. 4,306,300 by Terman, U.S. Pat. No. 4,661,929 by Aoki, U.S. Pat. No. 4,709,350 by Nakagome, and U.S. Pat. No. 4,771,404 by Mano. All of these approaches use volatile storage, that is, the charge levels are not permanently stored. They provide  $2^n$  different volatile charge levels on a capacitor to define  $2^n$  different states corresponding to n-bits of data per memory cell. All of these approaches have the common characteristic that whatever information is stored on such a memory cell is volatile because such a cell loses its data whenever power is removed. Furthermore, these types of memory cells must be periodically refreshed as they have a tendency to lose charge over time even when power is maintained.

It would be advantageous to develop a multi-bit semiconductor memory cell that has the non-volatile characteristic of a mask programmable read-only-memory (ROM) and the electrically alterable characteristic of a multi-bit per cell DRAM. These characteristics combined in a single cell would provide a multi-bit per cell electrically alterable non-volatile memory (EANVM) capable of storing  $K^n$  bits of data, where "K" is the base of the numbering system being used and "n" is the number of bits to be stored in each memory cell. Additionally, it would be advantageous if the EANVM described above was fully compatible with conventional industry standard device programmers/erasers and programming/erasing algorithms such that a user can program/erase the multi-bit per cell memory in a manner identical to that used for current single-bit per cell memory devices.

## SUMMARY OF THE INVENTION

The present invention provides a multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two distinct states.

In a specific embodiment, the present invention provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in  $K^n$  memory states, where K is a base of a predetermined number system, n is a number of bits stored per cell, and  $K^n > 2$ . The present multi-level memory device also includes a memory cell programming means for programming the multi-level cell means to a state corresponding to the input information. A comparator means for comparing the memory state of the multi-level cell means with the input information is also included. The input information corresponds to one of a plurality of reference

voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information.

An alternative specific embodiment also provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system,  $n$  is a number of bits stored per cell, and  $K^n > 2$ . A memory cell programming means for programming the multi-level cell means to a state corresponding to the input information is also included. The present multi-level memory device further includes a comparator means for comparing the memory state of the multi-level cell means with the input information. The input information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information. A reference voltage means for defining the plurality of reference voltages is also included. The present reference voltage means is operably coupled to the comparator means.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIG. 1 is a generic schematic representation of a non-volatile floating gate memory cell.

FIG. 2 is a block diagram of a prior art single-bit memory system.

FIG. 3 is a timing diagram of the voltage threshold of a prior art single-bit per cell EANVM system being programmed from an erased "1" state to a programmed "0".

FIG. 4 is a timing diagram of the bit line voltage of a prior single-bit per cell EANVM during a read operation. It illustrates waveform levels for both the programmed and erased conditions.

FIG. 5 is a block diagram of an  $M \times N$  memory array implementing a multi-bit per cell EANVM system.

FIG. 6 is a block diagram for reading a multi-bit per cell EANVM system.

FIG. 7 shows the bit line voltage during a read cycle as a function of time for a 2-bit per cell EANVM which has been programmed to one of four possible states, (0, 0), (1, 0), (0, 1) and the fully erased condition (1, 1). Four separate voltage levels are represented on this figure, each representing one of the four possible states. Only one of these would be present for any given read operation.

FIG. 8 is a block diagram of a multi-bit per cell system combining program/verify and read circuitry.

FIG. 9 is a timing diagram for the voltage threshold for a 2-bit per cell EANVM being programmed from a fully erased (1, 1) state to one of the other three possible states.

FIG. 10 is a timing diagram which illustrates the voltage threshold of a 2-bit per cell EANVM being erased from a fully programmed (0, 0) state to one of the other three possible states.

FIG. 11 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using fixed width program pulses.

FIG. 12 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses fixed width program pulses.

FIG. 13 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using variable width program pulses.

FIG. 14 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses variable width program pulses.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the specific embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the specific embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover various alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

In general, the invention described here allows  $n$ -bits of information to be stored on and read from an Electrically Alterable Non-Volatile Memory (EANVM). This is accomplished by electrically varying the conductivity of the channel of a floating gate FET to be within any one of  $K^n$  conductivity ranges where " $K$ " represents the base of the numbering system being employed (in a binary system, " $K$ " equals 2). The conductivity range is then sensed and encoded. This forms the basis of an  $n$ -bit EANVM memory cell. The floating gate FET conductivity is electrically modified by using external programming hardware and algorithms which supply signals and voltages to the EANVM memory device.

These external signals and voltages are then modified internal to the device to provide an internally controlled program/verify cycle which incrementally stores electrons on the floating gate until the desired conductivity range is achieved. For the purpose of illustration, the  $n$ -bit per cell descriptions will assume a binary system which stores 2-bits per memory cell.

#### I. PRIOR ART SINGLE-BIT EANVM DEVICES

FIG. 1 is a generic schematic representation of a non-volatile floating gate memory cell 10. It is not intended that this schematic drawing is in any way indicative of the device structure. It is used to illustrate the fact that this invention refers to an FET memory cell which uses an electrically isolated, or floating, gate 14 to store charged particles for the purpose of altering the voltage threshold and hence channel conductivity of the FET memory cell 10.

The FET memory cell 10 includes a control gate 12 which is used either to select the memory cell for reading or is used to cause electrons to be injected onto the floating gate 14 during the programming process. Floating gate 14 is an electrically isolated structure which can indefinitely store electrons. The presence or absence of electrons on floating gate 14 alters the voltage threshold of the memory cell 10 and as a result alters the conductivity of its channel region. A drain region 16 of the FET is coupled to a source region 18 by a channel region 19. When the floating gate 14 is fully erased and the control gate 12 has been selected, the channel region 19 is in the fully "on", or high conductivity, state. When the floating gate 14 is fully programmed the channel region 19 is in the fully "off", or low conductivity state.

FIG. 2 is a block diagram of a prior art conventional single-bit EANVM memory system 30. The memory system

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30 stores a single bit of information in an EANVM cell 32. The cell 32, as described in FIG. 1, is selected for reading or writing when a row, or word, select signal is applied to a control gate terminal 34. A source terminal 36 for the FET of the cell 32 is connected to a reference ground potential. A drain terminal 38 is connected through a pull-up device 39 to a voltage  $V_{pull-up}$  at a terminal 40. Terminal 38 serves as the output terminal of the cell 32. When the cell 32 stores a "1" bit, the channel of the FET is in a low conductivity, or high impedance, state so that the voltage at terminal 38 is pulled-up to the voltage level  $V_{pull-up}$  on terminal 40. When the cell 32 stores a "0" bit, the channel of the FET is in a high conductivity, or low impedance, state so that the voltage at terminal 38 is pulled-down by the ground potential at terminal 36.

For reading the value of the single-bit stored in the cell 32, a sense amplifier 42 compares the voltage at terminal 38 with a reference voltage  $V_{ref}$  at terminal 43. If a "0" is stored on the EANVM cell 32, the cell will be in a low conductivity state and as a result the voltage at terminal 38 is above the reference voltage at terminal 43. For a "0" stored in the cell 32, the output terminal 44 of the sense amplifier 42 will be a low voltage which will be transmitted through an output buffer 46 to a terminal 48 and then coupled to the I/O terminal 50 as a logical "0". If a "1" is stored on the EANVM cell 32, the cell is in a high conductivity state and as a result the voltage at terminal 38 is below the reference voltage at terminal 43. The output of the sense amplifier 42 will be a high voltage which will be transmitted to the I/O terminal 50 as a logical "1".

For writing the value of an information bit stored in the cell 32, it is assumed that the cell 32 is in the erased, or fully "on", state which corresponds to a logical "1". The I/O terminal 50 is connected to the input terminal of an input latch/buffer 52. The output of the input latch/buffer 52 is connected to an enable/disable terminal 54 of a program voltage switch 56. The program voltage switch 56 provides a bit-line program voltage on a signal line 58 connected to terminal 38. Another output from the program voltage switch 56 is the word line program voltage on a signal line 62, which is connected to the control gate 34 of the EANVM cell 32. When a logical "0" is present at terminal 54 of the program voltage switch 56 from the output of Input Latch/Buffer 52 and when the program voltage switch 56 is activated by a program pulse on a signal line 66 from a program pulse 66, activated by a PGM/Write signal, the program voltage switch 56 provides the Program Voltage  $V_{pp}$  from a terminal 68 to the control gate 34 of the EANVM cell 32. The program voltage switch 56 also biases the drain of the EANVM cell 32 to a voltage, typically between 8 to 9 volts, and the gate of the EANVM cell 32 to the program voltage  $V_{pp}$ , typically 12 volts. Under these conditions, electrons are injected onto the floating gate by a phenomenon known as hot electron injection. This programming procedure raises the voltage threshold of the EANVM cell which increases its source-drain impedance. This continues until the FET memory cell 32 is effectively turned off, which corresponds to a "0" state. When a "1" is present on terminal 54 from the output of the Input Latch/Buffer 52 and when the PGM/Write is enabled, the signal line 58 is driven low and programming is inhibited and the "1", or erased, state is maintained.

FIG. 3 is a timing diagram of a prior-art single-bit EANVM cell 32, as described in connection with FIG. 2. The timing diagram shows the change in voltage threshold of the EANVM cell 32, as controlled by the word line and bit line programming voltages, which are illustratively

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shown as a single signal and which are both controlled by the PGM/Write signal. The memory cell is being programmed from the fully erased "1" state to the fully programmed "0" state. For the duration of the PGM/Write pulse, the bit and word line program voltages, which need not be the same, are respectively applied to the source connected to the bit line 38 and to the control gate 34 of the memory cell 32. As electrons are injected onto the floating gate, the voltage threshold of the memory cell begins to increase. Once the voltage threshold has been increased beyond a specific threshold value as indicated by the dashed horizontal line, the memory cell 32 is programmed to a "0" state.

Note that Fowler-Nordheim tunnelling can also be used instead of hot electron injection to place electrons on the floating gate. The multi-bit EANVM device described here functions with either memory cell programming technique. The prior art programming algorithms and circuits for either type of programming are designed to program a single-bit cell with as much margin as possible in as short a time as possible. For a single-bit memory cell, margin is defined as the additional voltage threshold needed to insure that the programmed cell will retain its stored value over time.

FIG. 4 is a timing diagram showing the bit line voltage at terminal 38 as a function of time during a memory read operation. In this example, prior to time  $t_1$  the bit line is charged to the  $V_{pull-up}$  condition. Note that it is also possible that the bit line may start at any other voltage level prior to time  $t_1$ . At time  $t_1$ , the EANVM cell 32 is selected and, if the cell 32 is in the erased or tilt state, the cell 32 provides a low impedance path to ground. As a result, the bit line is pulled down to near the ground potential provided at terminal 36 in FIG. 2. If the EANVM cell 32 were in the "0" or fully programmed state, the bit line voltage would remain at the  $V_{pull-up}$  voltage after time  $t_1$ . The voltage on the bit-line terminal 38 and the reference voltage  $V_{ref}$  at terminal 43 are compared by the comparator 42, whose buffered output drives I/O terminal 50. When  $V_{ref}$  is greater than the bit line voltage, the output on I/O terminal 50 is a logical "1". When  $V_{ref}$  is lower than the bit line voltage, the output on I/O terminal 50 is a logical "0".

## II. MEMORY ARRAY FOR A MULTI-BIT EANVM SYSTEM

FIG. 5 is a block diagram of a multi-bit per cell EANVM system 100 which includes an  $M \times N$  array of memory cells. The cells are typically shown as a floating gate FET, or EANVM, 102, as described in connection with FIG. 1. The array uses similar addressing techniques, external control signals, and I/O circuits as are used with currently available single bit per cell EANVM devices such as EPROM, EEPROM, FLASH, etc. devices. Row Address signals are provided at input terminals 103A and Column Address signals are provided at input terminals 103B.

Each of the EANVM cells in a row of cells has its source connected to a ground reference potential and its drain connected to a column bit line, typically shown as 106. Each of the columns is connected to a pull-up device, as indicated by the block 105. All of the control gates of a row are connected to a row select, or word, line, typically shown as 104. Rows are selected with a row select circuit 108 and columns are selected with a column select circuit 110. Sense amplifiers 112 are provided for each of the selected columns. Decode/encode circuits 114 and n-bit input/output latches/buffers 116 are also provided. A PGM/Write signal is provided at an input terminal 118 for activating a mode control circuit 120 and a timing circuit 122.

A significant feature of this n-bit per cell system 100 as compared to a single-bit per cell implementation is that the memory density is increased by a factor of n, where n is the number of bits which can be stored on an individual multi-bit memory cell.

### III. BASIC READ MODE OF AN N-BIT MEMORY CELL

FIG. 6 shows a binary system 150 for reading the state of an n-bit floating gate memory cell 102, as described in connection with FIG. 1, according to the invention, where n is the number of bits stored in the memory cell. For this example, n is set to 2 and one of four states of the memory cell must be detected. The four possible states being, (0,0), (0,1), (1,0), or (1,1). Detecting which state is programmed requires a 3-level sense amplifier 152. This amplifier includes three sense amplifiers 154, 154', 158 each of which have their negative input terminals connected to the output terminal 168 of the memory cell 102. Sense amplifier 154 has a reference voltage Ref 3 connected to its positive input terminal. Sense amplifier 156 has a reference voltage Ref 2 connected to its positive input terminal. Sense amplifier 158 has a reference voltage Ref 1 connected to its positive input terminal. The voltage references are set such as follows:  $V_{pull-up} > \text{Ref 3} > \text{Ref 2} > \text{Ref 1}$ . The respective output signals S3, S2, S1 of the three sense amplifiers drive an encode logic circuit 160, which encodes the sensed signals S3, S2, S1 into an appropriate 2-bit data format. Bit 0 is provided at an I/O terminal 162 and Bit 1 is provided at an I/O terminal 164. A truth table for the encode logic circuit 160 is as follows:

S3	S2	S1	I/O 1	I/O 0	State
L	L	L	0	0	(0,0)
H	L	L	1	0	(1,0)
H	H	L	0	1	(0,1)
H	H	H	1	1	(1,1)

During a read operation of an n-bit memory cell, the levels of the respective output signals S3, S2, S1 of the sense amplifiers 154, 156, 158 are determined by the conductivity value to which the memory cell had been set during a programming operation. A fully erased EANVM cell 102 will be in its lowest threshold voltage state, or the highest conductivity state. Consequently, all of the reference voltages will be higher than the bit line voltage at terminal 168, resulting in a (1,1) state. A fully programmed EANVM cell 102 will be in its highest threshold voltage state, or its lowest conductivity state. Consequently, all reference voltages will be lower than the bit line voltage at terminal 168, resulting in a (0,0) state. The intermediate threshold states are encoded as is illustrated in the truth table for the logic circuit 160. FIG. 7 shows the bit line voltage as a function of time at terminal 168, during a read cycle, for a binary 2-bit per memory cell. For purposes of illustration, each of the four possible waveforms corresponding to the four possible programmed states of the memory cell are shown. During a read cycle only the waveform corresponding to the programmed state of the EANVM cell would occur. For example, assume the EANVM memory cell 102 has been programmed to a (1,0) state. Prior to time t1, because the EANVM cell 102 has not yet been selected or activated, the bit line 106 is pulled-up to  $V_{pull-up}$ . At time t1, the EANVM cell is selected using conventional memory address decoding techniques. Because the EANVM cell has been programmed to a specific conductivity level by the charge on the floating gate, the bit line is pulled down to a specific voltage level

corresponding to the amount of current that the cell can sink at this specific conductivity level. When this point is reached at time t2 the bit line voltage stabilizes at a voltage level  $V_{ref3}$  between reference voltages Ref 3 and Ref 2 which correspond to a (1,0) state. When the EANVM cell 102 is de-selected, the bit line voltage will return to its pulled-up condition. Similarly, the bit-line voltage stabilizes at  $V_{ref2}$  for the 0,1 state for, or at zero volts for the 1,1 state. FIG. 8 is a block diagram of an n-bit memory cell system 200. For purposes of illustration a binary 2-bit per cell system is shown. However, the concepts of the invention extend to systems where n is greater than 2. It is also intended that the invention include any system where the EANVM memory cell has more than two states. For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system. Some of the components of this system 200 are shown and described with the same reference numerals for the components of FIG. 6 for the read mode of operation. It is intended that these same reference numerals identify the same components. The system 200 includes a memory cell 102, as described in FIG. 1, with a bit line output terminal 168. For the read mode of operation, a 3-level sense amplifier 152 with read reference voltages Ref 1, Ref 2, and Ref 3 and an encoder 160 is provided. Read data is provided at a Bit I/O terminal 162 and at a Bit 1 I/O terminal 164. For the write mode of operation, a verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202. The verify reference voltages are chosen so that as soon as the bit line voltage on bit line 106 is greater than the verify reference voltage the threshold of the EANVM cell 102 is set to the proper threshold corresponding to the memory state to which it is to be programmed. To this end the verify reference voltages  $V_{ref1}$ ,  $V_{ref2}$ ,  $V_{ref3}$ , and  $V_{ref4}$  are set such that  $V_{ref4}$  is above Ref 3,  $V_{ref3}$  is between Ref 3 and Ref 2,  $V_{ref2}$  is between Ref 1 and Ref 2, and  $V_{ref1}$  is below Ref 1. During a normal read operation, the bit line voltage will settle midway between the read reference voltages to insure that the memory contents will be read accurately. The verify reference voltage select circuit 222 is controlled by the 2-output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O terminals 162 and 164. The Y signal input terminal of the analog comparator 202 is connected to the bit line output terminal 168 of the multi-level memory cell 102. The output signal from the analog comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal line 206 from the program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 106 constitutes the bit line and provides the bit-line programming voltage to the bit-line terminal 168 of EANVM cell 102. After a program/verify timing circuit 208 is enabled by a PGM/Write signal provided on signal line 212 from a PGM/Write terminal 214, the timing circuit 208 provides a series of program/verify timing pulses to the program voltage switch 220 on a signal line 210. The pulse widths are set to control the programming process so that the voltage threshold of the EANVM cell 102 is incrementally altered by controlling the injection of charge onto the floating gate of the EANVM cell. Each programming cycle increases the voltage threshold and, as a result, decreases the conductance of the memory cell 102. After each internal program cycle is complete, as indicated by signal line 210 going "high", the program voltages are removed via the Program Voltage Switch 220 and a verify cycle begins. The voltage threshold of memory cell 102 is then determined by

9 using the comparator 202 to compare the bit line voltage at terminal 168 with the selected verify reference voltage from the verify reference voltage select circuit 222. When the bit line voltage exceeds that supplied by the verify reference voltage select circuit 222, the output signal 204 from the comparator 202 will then disable the program voltage switch 220 ending the programming cycle. For this embodiment of the invention, during a write operation, comparison of the current memory cell analog contents with the analog information to be programmed on the memory cell 102 is performed by the analog comparator 202. The verify reference voltage select circuit 222 analog output voltage X is determined by decoding the output of the n-bit input latch/buffer 224 (n=2 in the illustrative form). The Y input signal to the analog comparator 202 is taken directly from the bit line terminal 168. Note that the 3-level sense/encode circuits 152, 160, and reference voltage select circuit 222 may be completely independent, as indicated in the drawing. Alternatively, they may be coupled together to alternately time share common circuit components. This is possible because the 3-level sense/encode circuits 152 and 160 are used in the read mode of operation while the verify reference voltage select circuit 222 is used only in the write/verify mode of operation.

#### IV. BASIC WRITE MODE FOR A MULTI-BIT PER CELL EANVM SYSTEM

In the write mode, a binary n-bit per cell EANVM system must be capable of electrically programming a memory cell to 2<sup>n</sup> uniquely different threshold levels. In the two-bit per cell implementation, because it is assumed that the cell starts from the erased (1,1) state, it is only necessary to program three different thresholds (Vt1, Vt2, and Vt3) which define the (0,1), (1,0), and (0,0) states. Vt1 is the threshold required such that in the read mode, the bit line voltage will fall such that in the read mode, the bit line voltage will fall between Ref 1 and Ref 2. Vt2 is the threshold required such that in the read mode, the bit line voltage will fall between Ref 2 and Ref 3. Vt3 is the threshold required such that in the read mode, the bit line voltage will be greater than Ref 3.

FIG. 9 illustrates the change in voltage threshold for a 4-level, or 2-bit EANVM cell as the floating gate is being charged from an erased (1,1) threshold state to any one of the three other possible states. In prior art single-bit memory cells where there are only two states, the design objective is to provide enough charge to the floating gate to insure that the cell's voltage threshold is programmed as high as possible, as shown in FIG. 3. Because there is no upper threshold limit in a single-bit per cell system, overprogramming the cell will not cause incorrect data to be stored on the memory cell.

As will be appreciated from FIG. 9, in an n-bit per cell system the memory cell must be charged to a point so that the voltage threshold is within a specific voltage threshold range. In this example, where the cell is being programmed to a (1,0) state, the proper threshold range is defined as being above a threshold level Vt2 and as being below a threshold level Vt3.

To accomplish this n-level programming it is necessary to add to or modify the prior art EANVM circuitry. FIG. 8 shows the additional or modified circuitry, including a reference voltage select, an n-bit latch/buffer, a program/verify timing circuit, and a comparator. The comparator can be either digital or analog.

FIG. 10 illustrates the voltage threshold of an EANVM cell as the floating gate is being erased from a (0,0) state.

Standard EANVM programming operating procedure calls for a memory cell to be erased prior to being programmed. This erasure can be performed at the byte, block, or chip level and can be performed by electrical, UV, or other means. In this type of system the cell would be completely erased to a (1,1) state prior to initiating a programming cycle. If a system has the capability to erase an individual memory cell, then it is not necessary to erase all of the cells of a group prior to initiating a programming operation. It is then possible to incrementally erase an individual memory cell, as necessary, to program the cell to the appropriate voltage threshold as is indicated by the waveforms labelled (1,0) and (0,1).

FIG. 11 is a timing diagram which illustrates how a 2-bit EANVM cell of FIG. 8 is programmed from an erased (1,1) state to a (1,0) state using the timing circuitry 208 to generate fixed length timing pulses. A low logic level state of the PGM/Write signal on signal line 212 enables the timing circuit 208. When enabled at time t1, the timing circuit 208 provides an internal fixed-width low level internal PGM timing pulse on signal line 210 to the program voltage switch 220. For the duration of the low state of the internal PGM timing pulse, the bit line and word line program voltage outputs on lines 106 and 206 will be raised to their respective programming voltage levels as shown in FIG. 11. During this programming process, charge is added to the floating gate of the memory cell 102. When the internal PGM timing pulse from timing circuitry 208 switches to a high level, the programming voltages are removed and a verify cycle begins. For this example, verify reference voltage Vref3 is compared with the bit line voltage. This internally controlled program/verify cycle repeats itself until the bit line voltage on terminal 168 exceeds Vref3. At this time, t2, the EANVM cell 102 is verified to have been programmed to a (1,0) state and programming is halted by the comparator 202 providing a disable signal on signal line 204 to the program voltage switch 220.

FIG. 12 illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1,1) to a partially "off" state (1,0) using fixed length program pulses. When the externally applied PGM/Write pulse is applied at time t1, the program/verify timing circuit 208 first initiates a verify cycle to determine the current status of the memory cell 102. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, Vpull-up. More generally, prior to time t1, the bit line voltage could be pre-set to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage, Vref3 in this example, corresponding to the data to be programmed, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first fixed length programming pulse ends, a verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between ground potential and Ref1. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues until the bit-line voltage exceeds the selected verify reference voltage, in this case Vref3, which indicates a memory state of (1,0), at time t2.

FIG. 13 illustrates how a 2-bit EANVM cell is programmed from an erased (1,1) state to a (1,0) state using variable length programming pulses. The internal PGM pulses for this implementation start with a low state longer than for fixed-width implementation of FIGS. 11 and 12. The low-state pulse widths grow progressively shorter as the memory cell approaches the appropriate voltage threshold.

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This approach requires more precise control than the fixed length approach. However, programming times can be greatly reduced on average.

FIG. 14 illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1.1) to a partially "off" state (1.0) using variable length program pulses. When the externally applied PGM/Write pulse goes to an active low level at time t1, the program/verify timing circuit 208 first initiates a verify cycle to determine the current status of the memory cell 102. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, Vpull-up. Although, prior to time t1, the bit line voltage could be preset to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage corresponding to the data to be programmed, Vref3 in this example, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first variable length programming pulse is over, another verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between Ref1 and Ref2. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues until the bit-line voltage surpasses the selected verify reference voltage, in this case Vref3 which indicates a memory state of (1.0), at time t2.

Accordingly, the programming process for an n-bit per cell EANVM uses program/verify cycles, to incrementally program a cell. The durations of these cycles are determined by the timing circuit 208. A key element of the system is to provide a programming scheme which provides for accurate programming of the memory cell 102. This is accomplished by matching the pulse widths of the timing pulses of the timing circuitry 208 to the program time of the EANVM cell being used. As indicated in FIGS. 11 and 13, a desired voltage threshold actually falls within a range of threshold voltages. If the program pulses are too long, then too much charge may be added to the floating gate of the memory cell 102. This may result in an overshoot of the target voltage threshold, resulting in incorrect data being stored in the memory cell.

The programming pulse width is set such that if the voltage threshold of the cell 102 after the (n-1) programming pulse is at a point just below the target voltage threshold, then the (n)th, or final, program pulse will not cause an overshoot resulting in an overprogrammed condition for a memory cell.

FIG. 8 may also use a digital comparator rather than the analog comparator 202 shown in FIG. 8. The digital comparator would use the encoded data from the encode circuitry 160 which represents the current contents of the EANVM cell 102, as the input to the comparator representing the. The verify reference voltage select 222 would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer 124, representing the data to be programmed. Otherwise, the function of the comparator within the system remains the same.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the

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invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A multi-level memory device comprising:
  - a) an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of  $K^n$  predetermined memory states of said multi-level memory cell, where  $K$  is a base of a predetermined number system,  $n$  is a number of bits stored per cell, and  $K^n > 2$ ;
  - b) memory cell programming means for programming said multi-level memory cell in accordance with said input information;
  - c) reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and
  - d) comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.
2. A device according to claim 1, wherein each memory state is bounded by one or more voltage values, and each reference voltage differs from the voltage value or values bounding the corresponding memory state.
3. Multi-level memory apparatus, comprising:
  - a) an electrically alterable non-volatile memory cell having more than two predetermined memory states;
  - b) a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; and
  - c) a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.
4. Apparatus according to claim 3, wherein said comparator compares a bit line signal of said memory cell with the selected reference signal.
5. Apparatus according to claim 3, wherein said comparator compares a bit line voltage of said memory cell with a voltage of the selected reference signal.
6. Multi-level memory apparatus, comprising:
  - a) an electrically alterable non-volatile memory cell having more than two predetermined memory states;
  - b) a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; and
  - c) a verifying device which detects a parameter indicating the state of said memory cell and verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.
7. Apparatus according to claim 6, wherein said verifying device detects said parameter at a bit line terminal of said memory cell.
8. Apparatus according to claim 6, wherein said parameter is a bit line voltage of said memory cell.



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9. Multi-level memory apparatus, comprising:  
an electrically alterable non-volatile memory cell having more than two predetermined memory states;
- a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
  - a programming signal source which applies a programming signal to said memory cell; and
  - a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.
10. Apparatus according to claim 9, wherein said comparator compares a bit line signal of said memory cell with the selected reference signal.
11. Apparatus according to claim 9, wherein said comparator compares a bit line voltage of said memory cell with a voltage of the selected reference signal.
12. Multi-level memory apparatus, comprising:  
an electrically alterable non-volatile memory cell having more than two predetermined memory states;
- a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
  - a programming signal source which applies a programming signal to said memory cell; and
  - a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.
13. Apparatus according to claim 12, wherein said verifying device detects said parameter at a bit line terminal of said memory cell.
14. Apparatus according to claim 12, wherein said parameter is a bit line voltage of said memory cell.
15. Multi-level memory apparatus, comprising:  
an electrically alterable non-volatile memory cell having more than two predetermined memory states;
- a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
  - a programming signal source which applies a programming signal to said memory cell; and
  - a control device which controls the application of said programming signal to said memory cell based on the selected reference signal.
16. Apparatus according to claim 15, wherein said control device detects a parameter indicating the state of said memory cell, verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal, and controls the application of said programming signal to said memory cell based on a result of the verification.
17. Apparatus according to claim 15, wherein said control device compares a signal corresponding to the state of said memory cell with the selected reference signal and controls the application of said programming signal to said memory cell based on a result of the comparison.

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18. Apparatus for verifying programming of an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:
- a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; and
  - a comparator to compare a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.
19. Apparatus according to claim 18, wherein the signal corresponding to the state of said memory cell is a bit line signal of said memory cell.
20. Apparatus according to claim 18, wherein the signal corresponding to the state of said memory cell is a bit line voltage of said memory cell.
21. Apparatus for verifying programming of an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:
- a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; and
  - a verifying device to detect a parameter indicating the state of said memory cell and to verify whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.
22. Apparatus according to claim 21, wherein said parameter is a bit line signal parameter of said memory cell.
23. Apparatus according to claim 21, wherein said parameter is a bit line voltage of said memory cell.
24. Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:
- a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
  - a programming signal source to apply a programming signal to said memory cell; and
  - a comparator to compare a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.
25. Apparatus according to claim 24, wherein the signal corresponding to the state of said memory cell is a bit line signal of said memory cell.
26. Apparatus according to claim 24, wherein the signal corresponding to the state of said memory cell is a bit line voltage of said memory cell.
27. Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:
- a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
  - a programming signal source to apply a programming signal to said memory cell; and

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a verifying device to detect a parameter indicating the state of said memory cell and to verify whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.

28. Apparatus according to claim 27, wherein said parameter is a bit line signal parameter of said memory cell.

29. Apparatus according to claim 27, wherein said parameter is a bit line voltage of said memory cell.

30. Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising:

a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;

a programming signal source to apply a programming signal to said memory cell; and

a control device to control the application of said programming signal to said memory cell based on the selected reference signal.

31. Apparatus according to claim 30, wherein said control device is constructed to detect a parameter indicating the state of said memory cell, to verify whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal, and to control the application of said programming signal to said memory cell based on a result of the verification.

32. Apparatus according to claim 30, wherein said control device is constructed to compare a signal corresponding to the state of said memory cell with the selected reference signal, and to control the application of said programming signal to said memory cell based on a result of the comparison.

33. A method of verifying programming of an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; and

comparing a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.

34. A method according to claim 33, wherein said comparing includes comparing a bit line signal of said memory cell with the selected reference signal.

35. A method according to claim 33, wherein said comparing includes comparing a bit line voltage of said memory cell with a voltage of the selected reference signal.

36. A method of verifying programming of an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;

detecting a parameter indicating the state of said memory cell; and

verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.

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37. A method according to claim 36, wherein said parameter is detected at a bit line terminal of said memory cell.

38. A method according to claim 36, wherein said parameter is a bit line voltage of said memory cell.

39. A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

selecting one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;

applying a programming signal to said memory cell; and comparing a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.

40. A method according to claim 39, wherein said comparing includes comparing a bit line signal of said memory cell with the selected reference signal.

41. A method according to claim 39, wherein said comparing includes comparing a bit line voltage of said memory cell with a voltage of the selected reference signal.

42. A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;

applying a programming signal to said memory cell;

detecting a parameter indicating the state of said memory cell; and

verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal.

43. A method according to claim 42, wherein said parameter is detected at a bit line terminal of said memory cell.

44. A method according to claim 42, wherein said parameter is a bit line voltage of said memory cell.

45. A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;


applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.

46. A method according to claim 45, including detecting a parameter indicating the state of said memory cell, verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal, and wherein the application of said programming signal is controlled based on a result of said verifying.

47. A method according to claim 45, including comparing a signal corresponding to the state of said memory cell with the selected reference signal, and wherein the application of said programming signal is controlled based on a result of said comparing.

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PATENT APPLICATION

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY  
WITH N-BITS PER CELL

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ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY  
WITH N-BITS PER CELL

410200

## ABSTRACT OF THE DISCLOSURE

5 A multi-bit memory device with a memory cell means  
for storing input information for an indefinite period of  
time. The multi-bit memory means stores information in up to  
 $K^n$  memory states ( $K^n > 1$ ). A memory cell programming means  
and comparator means is also included. The present multi-bit  
memory device also includes a voltage divider arrangement with  
10 pull-up devices in a memory array to provide stable and  
accurate reference voltages over process, temperature, and  
voltage variations.

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Attorney Docket No. 016176-000110US

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY  
WITH N-BITS PER CELL

BACKGROUND OF THE INVENTION

Cross Reference to Related Applications

A. 5 This application is a ~~continuation-in-part~~ <sup>division</sup> of U.S. Patent Application Serial No. 08/071,816, filed June 4, 1993 entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Memory Cell," <sup>now U.S. Pat. No. 5,399,262</sup> which is a continuation of U.S. Patent Application Serial No. 07/652,878, filed February 8, 1991 (now 10 U.S. Patent No. 5,218,569) entitled "Electrically Alterable Non-Volatile Memory with N-Bits Per Cell."

1. Field of the Invention

P.O. 15 This invention relates to non-volatile memory (NVM) devices; and, more particularly, is concerned with an apparatus and method for <sup>device</sup> ~~providing~~ <sup>AI</sup> a multi-level NVM device with stable reference voltages.

2. Description of the Background Art

20 In conventional single-bit per cell memory devices, the memory cell assumes one of two information storage states, either an "on" state or an "off" state. This combination of either "on" or "off" defines one bit of information. As a result, a memory device which can store n-bits of data requires n separate memory cells.

25 Increasing the number of bits which can be stored in a single-bit per cell memory device relies upon increasing the number of memory cells on a one-for-one basis with the number of bits of data to be stored. Methods for increasing the number of memory bits in a single memory device have relied upon the following advanced manufacturing techniques:  
30 manufacture larger die which contain more memory cells; or use improved lithography techniques to build smaller memory cells and allow more memory cells to be placed in a given area on a single chip.

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An alternative approach to the single-bit per cell approach involves storing multiple-bits of data in a single memory cell. Previous approaches to implementing multiple-bit per cell non-volatile memory devices have only involved mask programmable read only memories (ROMs). In one of these approaches, the channel width and/or length of the memory cell is varied such that  $2^n$  different conductivity values are obtained which correspond to  $2^n$  different states corresponding to n-bits of data which can be stored on a single memory cell. In another approach, the ion implant for the threshold voltage is varied such that the memory cell will have  $2^n$  different voltage thresholds ( $V_t$ ) corresponding to  $2^n$  different conductance levels corresponding to  $2^n$  different states corresponding to n-bits of data which can be stored on a single memory cell. Examples of memory devices of these types are described in US Patent No. 4,192,014 by Craycraft, US Patent No. 4,586,163 by Koike, US Patent No. 4,287,570 by Stark, US Patent No. 4,327,424 by Wu, and US Patent No. 4,847,808 by Kobatake.

Single-bit per cell read-only-memory devices are only required to sense, or read, two different levels or states per cell, consequently they have need for only one voltage reference. Sensing schemes for multi-level memory devices are more complex and require  $2^n - 1$  voltage references. Examples of such multiple state sensing schemes for ROMs are described in US Patent No. 4,449,203 by Adlhoch, US Patent No. 4,495,602 by Shepard, US Patent No. 4,503,578 by Iwahashi, and US Patent No. 4,653,023 by Suzuki. ~~A limitation with the conventional sensing schemes is often inaccurate and unstable reference voltage levels. The conventional sensing schemes have reference voltage levels which cannot accurately track bit-line voltage levels through process, temperature, and voltage variations.~~

These approaches to a multi-bit ROM commonly have one of  $2^n$  different conductivity levels of each memory cell being determined during the manufacturing process by means of a customized mask that is valid for only one data pattern. Thus, for storing n different data information patterns, a

minimum of  $n$  different masks need to be produced and incorporated into a manufacturing process. Each time a data information pattern needs to be changed a new mask must be created and a new batch of semiconductor wafers processed. This dramatically increases the time between a data pattern change and the availability of a memory product programmed with that new data pattern.

Prior art electrically alterable multiple-bit per cell memory approaches store multiple levels of charge on a capacitive storage element, such as is found in a conventional dynamic random access memory (DRAM) or a charge coupled device (CCD). Such approaches are described in US Patent No. 4,139,910 by Anantha, US Patent No. 4,306,300 by Terman, US Patent No. 4,661,929 by Aoki, US Patent No. 4,709,350 by Nakagome, and US Patent No. 4,771,404 by Mano. All of these approaches use volatile storage, that is, the charge levels are not permanently stored. They provide  $2^n$  different volatile charge levels on a capacitor to define  $2^n$  different states corresponding to  $n$ -bits of data per memory cell. All of these approaches have the common characteristic that whatever information is stored on such a memory cell is volatile because such a cell loses its data whenever power is removed. Furthermore, these types of memory cells must be periodically refreshed as they have a tendency to lose charge over time even when power is maintained.

It would be advantageous to develop a multi-bit semiconductor memory cell that has the non-volatile characteristic of a mask programmable read-only-memory (ROM) and the electrically alterable characteristic of a multi-bit per cell DRAM. These characteristics combined in a single cell would provide a multi-bit per cell electrically alterable non-volatile memory (EANVM) capable of storing  $K^n$  bits of data, where " $K$ " is the base of the numbering system being used and " $n$ " is the number of bits to be stored in each memory cell. Additionally, it would be advantageous if the EANVM described above was fully compatible with conventional industry standard device programmers/erasers and programming/erasing algorithms such that a user can



program/erase the multi-bit per cell memory in a manner identical to that used for current single-bit per cell memory devices.

#### SUMMARY OF THE INVENTION

5 The present invention provides a multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two distinct states ~~and such states are compared to stable reference voltages. The stable reference voltages are generated by way of cells made during the same (or similar) process steps as the memory device.~~

10 In a specific embodiment, the present invention provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing  
15 input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system,  $n$  is a number of bits stored per cell, and  $K^n > 2$ . The present multi-level memory  
20 device also includes a memory cell programming means for programming the multi-level cell means to a state corresponding to the input information. A comparator means for comparing the memory state of the multi-level cell means with the input information is also included. The input  
25 information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information.

30 An alternative specific embodiment also provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in  $K^n$  memory states, where  $K$  is a  
35 base of a predetermined number system,  $n$  is a number of bits stored per cell, and  $K^n > 2$ . A memory cell programming means for programming the multi-level cell means to a state

corresponding to the input information is also included. The present multi-level memory device further includes a comparator means for comparing the memory state of the multi-level cell means with the input information. The input information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information. A reference voltage means for defining the plurality of reference voltages is also included. The present reference voltage means is operably coupled to the comparator means.

~~In an alternative specific embodiment, the present invention provides an integrated circuit with a plurality of multi-level cells. The present integrated circuit includes a multi-level memory cell for storing input information for an indefinite period of time as a discrete state of said multi-level memory cell. The multi-level memory cell stores information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per multi-level memory cell, wherein  $K^n > 2$ . The present integrated circuit also includes a memory cell programming circuit for programming the multi-level memory cell to a memory state corresponding to the input information. A comparator for comparing the memory state of the multi-level memory cell with the input information is also included. The input information corresponds to one of a plurality of reference voltages. The comparator means further generates a control signal indicative of the memory state as compared to the input information. The present integrated circuit also includes a reference voltage cell for providing the one plurality of reference voltages. The reference voltage cell is operably coupled to the comparator. The multi-level memory cell is defined by one of the plurality of multi-level cells and the reference voltage cell is defined by another of the plurality of multi-level cells.~~

~~A further embodiment provides an integrated circuit device with a plurality of multi-level cells. The plurality~~

of multi-level cells defines a multi-level memory cell and a ~~reference voltage cell.~~

#### BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

Fig. 1 is a generic schematic representation of a non-volatile floating gate memory cell.

Fig. 2 is a block diagram of a prior art single-bit memory system.

Fig. 3 is a timing diagram of the voltage threshold of a prior art single-bit per cell EANVM system being programmed from an erased "1" state to a programmed "0".

Fig. 4 is a timing diagram of the bit line voltage of a prior single-bit per cell EANVM during a read operation. It illustrates waveform levels for both the programmed and erased conditions.

Fig. 5 is a block diagram of an M x N memory array implementing a multi-bit per cell EANVM system.

Fig. 6 is a block diagram for reading a multi-bit per cell EANVM system.

Fig. 7 shows the bit line voltage during a read cycle as a function of time for a 2-bit per cell EANVM which has been programmed to one of four possible states, (0, 0), (1, 0), (0, 1) and the fully erased condition (1, 1). Four separate voltage levels are represented on this figure, each representing one of the four possible states. Only one of these would be present for any given read operation.

Fig. 9 is a timing diagram which illustrates the voltage threshold of a 2-bit per cell EANVM being erased from a fully programmed (0, 0) state to one of the other three possible states.

Fig. 8 is a block diagram of a multi-bit per cell system combining program/verify and read circuitry.

Fig. 9 is a timing diagram for the voltage threshold for a 2-bit per cell EANVM being programmed from a fully erased (1,1) state to one of the other three possible states.

Fig. 11 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using fixed width program pulses.

Fig. 12 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses fixed width program pulses.

Fig. 13 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using variable width program pulses.

Fig. 14 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses variable width program pulses.

~~Fig. 15 is a simplified diagram of voltages for a 2-bit per memory cell according to the present invention.~~

Fig. 16 is a simplified voltage generator circuit diagram of a voltage divider arrangement for generating multiple reference voltages according to the present invention.

Fig. 17 illustrates the reference voltages of Fig. 16 according to the present invention.

Fig. 18 is a simplified voltage generator circuit diagram for an array showing reference voltage columns connected to pull-up devices according to the present invention.

Fig. 19 is a simplified voltage generator circuit diagram for obtaining reference voltages with use of pull-up devices and a voltage divider according to a preferred embodiment of the present invention.

Fig. 20 is a simplified diagram of a voltage generator circuit according to an alternative embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the specific embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the specific  
 5       embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover various alternatives, modifications and equivalents, which may be included within  
 10       the spirit and scope of the invention as defined by the appended claims.

In general, the invention described here allows n-bits of information to be stored on and read from an Electrically Alterable Non-Volatile Memory (EANVM). This is  
 15       accomplished by electrically varying the conductivity of the channel of a floating gate FET to be within any one of  $K^n$  conductivity ranges where "K" represents the base of the numbering system being employed (in a binary system, "K" equals 2). The conductivity range is then sensed and encoded.  
 20       This forms the basis of an n-bit EANVM memory cell. The floating gate FET conductivity is electrically modified by using ~~conventional~~ external programming hardware and algorithms which supply ~~conventional~~ signals and voltages to the EANVM memory device.

25       These external signals and voltages are then modified internal to the device to provide an internally controlled program/verify cycle which incrementally stores electrons on the floating gate until the desired conductivity range is achieved. For the purpose of illustration, the n-bit  
 30       per cell descriptions will assume a binary system which stores 2-bits per memory cell.

## I. PRIOR ART SINGLE-BIT EANVM DEVICES

Fig. 1 is a generic schematic representation of a non-volatile floating gate memory cell 10. It is not intended  
 35       that this schematic drawing is in any way indicative of the device structure. It is used to illustrate the fact that this invention refers to an FET memory cell which uses an

electrically isolated, or floating, gate 14 to store charged particles for the purpose of altering the voltage threshold and hence channel conductivity of the FET memory cell 10.

A The FET memory cell 10 includes a control gate 12 which is used either to select the memory cell for reading or is used to cause electrons to be injected onto the floating gate 14 during the programming process. Floating gate 14 is an electrically isolated structure which can indefinitely store electrons. The presence or absence of electrons on floating gate 14 alters the voltage threshold of the memory cell 10 and as a result alters the conductivity of its channel region. A drain region 16 of the FET is coupled to a source region 18 by a channel region 19. When the floating gate 14 is fully erased and the control gate 12 has been selected, the channel region 19 is in the fully "on", or high conductivity, state. When the floating gate 14 is fully programmed the channel region 19 is in the fully "off", or low conductivity state.

Fig. 2 is a block diagram of a prior art conventional single-bit EANVM memory system 30. The memory system 30 stores a single bit of information in an EANVM cell 32. The cell 32, as described in Fig. 1, is selected for reading or writing when a row, or word, select signal is applied to a control gate terminal 34. A source terminal 36 for the FET of the cell 32 is connected to a reference ground potential. A drain terminal 38 is connected through a pull-up device 39 to a voltage  $V_{pull-up}$  at a terminal 40. Terminal 38 serves as the output terminal of the cell 32. When the cell 32 stores a "1" bit, the channel of the FET is in a low conductivity, or high impedance, state so that the voltage at terminal 38 is pulled-up to the voltage level  $V_{pull-up}$  on terminal 40. When the cell 32 stores a "0" bit, the channel of the FET is in a high conductivity, or low impedance, state so that the voltage at terminal 38 is pulled-down by the ground potential at terminal 36.

For reading the value of the single-bit stored in the cell 32, a sense amplifier 42 compares the voltage at terminal 38 with a reference voltage  $V_{ref}$  at terminal 43. If

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a "0" is stored on the EANVM cell 32, the cell will be in a low conductivity state and as a result the voltage at terminal 38 is above the reference voltage at terminal 43. For a "0" stored in the cell 32, the output terminal 44 of the sense amplifier 42 will be a low voltage which will be transmitted through an output buffer 46 to a terminal 48 and then coupled to the I/O terminal 50 as a logical "0". If a "1" is stored on the EANVM cell 32, the cell is in a high conductivity state and as a result the voltage at terminal 38 is below the reference voltage at terminal 43. The output of the sense amplifier 42 will be a high voltage which will be transmitted to the I/O terminal 50 as a logical "1".

For writing the value of an information bit stored in the cell 32, it is assumed that the cell 32 is in the erased, or fully "on", state which corresponds to a logical "1". The I/O terminal 50 is connected to the input terminal of an input latch/buffer 52. The output of the input latch/buffer 52 is connected to an enable/disable terminal 54 of a program voltage switch 56. The program voltage switch 56 provides a bit-line program voltage on a signal line 58 connected to terminal 38. Another output from the program voltage switch 56 is the word line program voltage on a signal line 62, which is connected to the control gate 34 of the EANVM cell 32. When a logical "0" is present at terminal 54 of the program voltage switch 56 from the output of Input Latch/Buffer 52 and when the program voltage switch 56 is activated by a program pulse on a signal line 62 from a program pulse 66, activated by a PGM/Write signal, the program voltage switch 56 provides the Program Voltage  $V_{pp}$  from a terminal 68 to the control gate 34 of the EANVM cell 32. The program voltage switch 56 also biases the drain of the EANVM cell 32 to a voltage, typically between 8 to 9 volts, and the gate of the EANVM cell 32 to the program voltage  $V_{pp}$ , typically 12 volts. Under these conditions, electrons are injected onto the floating gate by a phenomenon known as hot electron injection. This programming procedure raises the voltage threshold of the EANVM cell which increases its source-drain impedance. This continues until the FET memory

cell 32 is effectively turned off, which corresponds to a "0" state. When a "1" is present on terminal 54 from the output of the Input Latch/Buffer 52 and when the PGM/Write is enabled, the signal line 58 is driven low and programming is inhibited and the "1", or erased, state is maintained.

Fig. 3 is a timing diagram of a prior-art single-bit EANVM cell 32, as described in connection with Figure 2. The timing diagram shows the change in voltage threshold of the EANVM cell 32, as controlled by the word line and bit line programming voltages, which are illustratively shown as a single signal and which are both controlled by the PGM/Write signal. The memory cell is being programmed from the fully erased "1" state to the fully programmed "0" state. For the duration of the PGM/Write pulse, the bit and word line program voltages, which need not be the same, are respectively applied to the source connected to the bit line 38 and to the control gate 34 of the memory cell 32. As electrons are injected onto the floating gate, the voltage threshold of the memory cell begins to increase. Once the voltage threshold has been increased beyond a specific threshold value as indicated by the dashed horizontal line, the memory cell 32 is programmed to a "0" state.

Note that Fowler-Nordheim tunnelling can also be used instead of hot electron injection to place electrons on the floating gate. The multi-bit EANVM device described here functions with either memory cell programming technique. The prior art programming algorithms and circuits for either type of programming are designed to program a single-bit cell with as much margin as possible in as short a time as possible. For a single-bit memory cell, margin is defined as the additional voltage threshold needed to insure that the programmed cell will retain its stored value over time.

Fig. 4 is a timing diagram showing the bit line voltage at terminal 38 as a function of time during a memory read operation. In this example, prior to time  $t_1$  the bit line is charged to the  $V_{pull-up}$  condition. Note that it is also possible that the bit line may start at any other voltage level prior to time  $t_1$ . At time  $t_1$ , the EANVM cell 32 is

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selected and, if the cell 32 is in the erased or tilt state, the cell 32 provides a low impedance path to ground. As a result, the bit line is pulled down to near the ground potential provided at terminal 36 in Figure 2. If the EANVM cell 32 were in the "0" or fully programmed state, the bit line voltage would remain at the Vpull-up voltage after time t1. The voltage on the bit-line terminal 38 and the reference voltage Vref at terminal 43 are compared by the comparator 42, whose buffered output drives I/O terminal 50. When Vref is greater than the bit line voltage, the output on I/O terminal 50 is a logical "1". When Vref is lower than the bit line voltage, the output on I/O terminal 50 is a logical "0".

## II. MEMORY ARRAY FOR A MULTI-BIT EANVM SYSTEM

Fig. 5 is a block diagram of a multi-bit per cell EANVM system 100 which includes an M x N array of memory cells. The cells are typically shown as a floating gate FET, or EANVM, 102, as described in Fig. 1. The array uses similar addressing techniques, external control signals, and I/O circuits as are used with currently available single bit per cell EANVM devices such as EPROM, EEPROM, FLASH, etc. devices. Row Address signals are provided at input terminals 103A and Column Address signals are provided at input terminals 103B.

Each of the EANVM cells in a row of cells has its source connected to a ground reference potential and its drain connected to a column bit line, typically shown as 106. Each of the columns is connected to a pull-up device, as indicated by the block 105. All of the control gates of a row are connected to a row select, or word, line, typically shown as 104. Rows are selected with a row select circuit 108 and columns are selected with a column select circuit 110. Sense amplifiers 112 are provided for each of the selected columns. Decode/encode circuits 114 and n-bit input/output latches/buffers 116 are also provided. A PGM/Write signal is provided at an input terminal 118 for activating a mode control circuit 120 and a timing circuit 122.

A significant feature of this n-bit per cell system 100 as compared to a single-bit per cell implementation

is that the memory density is increased by a factor of  $n$ , where  $n$  is the number of bits which can be stored on an individual multi-bit memory cell.

### III. BASIC READ MODE OF AN N-BIT MEMORY CELL

Fig. 6 shows a binary system 150 for reading the state of an  $n$ -bit floating gate memory cell 102, as described in Fig. 1, according to the invention, where  $n$  is the number of bits stored in the memory cell. For this example,  $n$  is set to 2 and one of four states of the memory cell must be detected. The four possible states being, (0,0), (0,1), (1,0), or (1,1). Detecting which state is programmed requires a 4-level sense amplifier 152. This amplifier includes three sense amplifiers 154, 156, 158 each of which have their negative input terminals connected to the output terminal 106 of the memory cell 102. Sense amplifier 154 has a reference voltage Ref 3 connected to its positive input terminal. Sense amplifier 156 has a reference voltage Ref 2 connected to its positive input terminal. Sense amplifier 158 has a reference voltage Ref 1 connected to its positive input terminal. The voltage references are set such as follows:  $V_{\text{pull-up}} > \text{Ref 3} > \text{Ref 2} > \text{Ref 1}$ . The respective output signals S3, S2, S1 of the three sense amplifiers drive an encode logic circuit 160, which encodes the sensed signals S3, S2, S1 into an appropriate 2-bit data format. Bit 0 is provided at an I/O terminal 162 and Bit 1 is provided at an I/O terminal 164. A truth table for the encode logic circuit 160 is as follows:

T/MOX

	S3	S2	S1	I/O 1	I/O 0	State
	L	L	L	0	0	(0,0)
	H	L	L	1	0	(1,0)
30	H	H	L	0	1	(0,1)
	H	H	H	1	1	(1,1)

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During a read operation of an n-bit memory cell, the levels of the respective output signals S3, S2, S1 of the sense amplifiers 154, 156, 158 are determined by the conductivity value to which the memory cell had been set during a programming operation. A fully erased EANVM cell 102 will be in its lowest threshold voltage state, or the highest conductivity state. Consequently, all of the reference voltages will be higher ~~in voltage~~ than the bit line voltage at terminal 106, resulting in a (1,1) state. A fully programmed EANVM cell 102 will be in its highest threshold voltage state, or its lowest conductivity state. Consequently, all reference voltages will be lower ~~in voltage~~ than the bit line voltage at terminal 106, resulting in a (0,0) state. The intermediate threshold states are encoded as is illustrated in the truth table for the logic circuit 160. Fig. 7 shows the bit line voltage as a function of time at terminal 106, during a read cycle, for a binary 2-bit per memory cell. For purposes of illustration, each of the four possible waveforms corresponding to the four possible programmed states of the memory cell are shown. During a read cycle only the waveform corresponding to the programmed state of the EANVM cell would occur. For example, 25 assume the EANVM memory cell 102 has been programmed to a (1,0) state. Prior to time t1, because the EANVM cell 102 has not yet been selected or activated, the bit line 106 is pulled-up to Vpull-up. At time t1, 22 the EANVM cell is selected using conventional memory address decoding techniques. Because the EANVM cell has been programmed to a specific conductivity level by the charge on the floating gate, the bit line is pulled down to a specific voltage level corresponding to the amount of current that the cell can sink at this specific conductivity level. When this point is reached at time t2 the bit line voltage stabilizes at a voltage level Vref3 between reference voltages Ref 3 and Ref 2 which correspond to a (1,0) state. When the EANVM cell 102 is de-selected, the bit line voltage will return to its pulled-up condition. Similarly, the bit-line voltage stabilizes at Vref2 for the 0,1 state for the other specific conductivity levels, or at zero volts for

the 1,1 state. Fig. 8 is a block diagram of an n-bit memory cell system 200. For purposes of illustration a binary 2-~~20~~ bit per cell system is shown. However, ~~it is intended that~~ the concepts of the invention extend to systems where n is greater than 2. It is also intended that the invention include any system where the EANVM memory cell has more than two states. For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system. Some of the components of this system 200 are shown and described with the same reference numerals for the components of Figure 6 for the read mode of operation. It is intended that these same reference numerals identify the same components. The system 200 includes a memory cell 102, as described in Figure 1, with a bit line output terminal ~~106~~ <sup>108</sup>. For the read mode of operation, a ~~3~~ <sup>2</sup>-level sense amplifier 152 with read reference voltages Ref 1, Ref 2, and Ref 3 and an encoder 160 is provided. Read data is provided at a Bit I/O terminal 162 and at a Bit ~~1~~ <sup>2</sup> I/O terminal 164. For the write mode of operation, a verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of the analog comparator 202. The verify reference voltages are chosen so that as soon as the bit line voltage on bit line 106 is greater than the verify reference voltage the threshold of the EANVM cell 102 is set to the proper threshold corresponding to the memory state to which it is to be programmed. To this end the verify reference voltages Vref1, Vref2, Vref3, and Vref4 are set such that Vref4 is above Ref 3, Vref3 is between Ref 3 and Ref 2, Vref2 is between Ref 1 and Ref 2, and Vref1 is below Ref 1. During a normal read operation, the bit line voltage will settle midway between the read reference voltages to insure that the memory contents will be read accurately. The verify reference voltage select circuit 222 is controlled by the 2-output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O terminals 162 and 164. The V signal input terminal of the analog comparator ~~202~~ <sup>202</sup> is connected to the bit line output terminal ~~106~~ <sup>108</sup> of the multi-level memory cell 102. The output signal from the analog

comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal line 206 from the program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 208 provides the bit-line programming voltage to the bit-line terminal 108 of EANVM cell 102. After the program/verify timing circuit 208 is enabled by a PGM/Write signal provided on signal line 212 from a PGM/Write terminal 214, the timing circuit 208 provides a series of program/verify timing pulses to the program voltage switch 220 on a signal line 210. The pulse widths are set to control the programming process so that the voltage threshold of the EANVM cell 102 is incrementally altered by controlling the injection of charge onto the floating gate of the EANVM cell. Each programming cycle increases the voltage threshold and, as a result, decreases the conductance of the memory cell 102. After each internal program cycle is complete, as indicated by signal line 210 going "high", the program voltages are removed via the program voltage switch 220 and a verify cycle begins. The voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 108 with the selected verify reference voltage from the verify reference voltage select circuit 222. When the bit line voltage exceeds that supplied by the verify reference voltage select circuit 222, the output signal 204 from the comparator 202 will then disable the program voltage switch 220 ending the programming cycle. For this embodiment of the invention, during a write operation, comparison of the current memory cell analog contents with the analog information to be programmed on the memory cell 102 is performed by the analog comparator 202. The verify reference voltage select circuit 222 analog output voltage X is determined by decoding the output of the n-bit input latch/buffer 224. The Y input signal to the analog comparator 202 is taken directly from the bit line terminal 108. Note that the level sense/encode circuits 152, 160, and reference voltage select circuit 222 may be completely independent, as indicated in the drawing.

Alternatively, they may be coupled together to alternately time share common circuit components. This is possible because the ~~2~~<sup>3</sup> level sense/encode circuits 152 and 160 are used in the read mode of operation while the verify reference voltage select circuit 222 is used only in the write/verify mode of operation.

#### IV. BASIC WRITE MODE FOR A MULTI-BIT PER CELL EANVM SYSTEM

In the write mode, a binary n-bit per cell EANVM system must be capable of electrically programming a memory cell to  $2^n$  uniquely different threshold levels. In the two-bit per cell implementation, because it is assumed that the cell starts from the erased (1,1) state, it is only necessary to program three different thresholds (Vt1, Vt2, and Vt3) which define the (0,1), (1,0), and (0,0) states. Vt1 is the threshold required such that in the read mode, the bit line voltage will fall between Ref 1 and Ref 2. Vt2 is the threshold required such that in the read mode, the bit line voltage will fall between Ref 2 and Ref 3. Vt3 is the threshold required such that in the read mode, the bit line voltage will be greater than Ref 3.

Fig. 9 illustrates the change in voltage threshold for a 4-level, or 2-bit EANVM cell as the floating gate is being charged from an erased (1,1) threshold state to any one of the three other possible states. In prior art single-bit memory cells where there are only two states, the design objective is to provide enough charge to the floating gate to insure that the cell's voltage threshold is programmed as high as possible, as shown in Figure 3. Because there is no upper threshold limit in a single-bit per cell system, overprogramming the cell will not cause incorrect data to be stored on the memory cell.

*could be appreciated from*  
As illustrated by Figure 9, in an n-bit per cell system the memory cell must be charged to a point so that the voltage threshold is within a specific voltage threshold range. In this example, where the cell is being programmed to a (1,0) state, the proper threshold range is defined as being

above a threshold level  $V_{t2}$  and as being below a threshold level  $V_{t3}$ .

To accomplish this n-level programming it is necessary to add to or modify the prior art EANVM circuitry. Figure 8 shows the additional or modified circuits, including a reference voltage select, an n-bit latch/buffer, a program/verify timing circuit, and a comparator. The comparator can be either digital or analog.

Fig. 10 illustrates the voltage threshold of an EANVM cell as the floating gate is being erased from a (0,0) state. Standard EANVM programming operating procedure calls for a memory cell to be erased prior to being programmed. This erasure can be performed at the byte, block, or chip level and can be performed by electrical, UV, or other means. In this type of system the cell would be completely erased to a (1,1) state prior to initiating a programming cycle. If a system has the capability to erase an individual memory cell, then it is not necessary to erase all of the cells of a group prior to initiating a programming operation. It is then possible to incrementally erase an individual memory cell, as necessary, to program the cell to the appropriate voltage threshold as is indicated by the waveforms labelled (1,0) and (0,1).

Fig. 11 is a timing diagram which illustrates how a 2-bit EANVM cell of Figure 8 is programmed from an erased (1,1) state to a (1,0) state using the timing circuitry 208 to generate fixed length timing pulses. A low logic level state of the PGM/Write signal on signal line 212 enables the timing circuit 208. When enabled at time  $t_1$ , the timing circuit 208 provides an internal fixed-width low level internal PGM timing pulse on signal line 210 to the program voltage switch 220. For the duration of the low state of the internal PGM timing pulse, the bit line and word line program voltage outputs on lines ~~216~~<sup>218</sup> and 206 will be raised to their respective programming voltage levels as shown in Figure 11. During this programming process, charge is added to the floating gate of the memory cell 102. When the internal PGM timing pulse from timing circuitry 208 switches to a high level, the programming

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voltages are removed and a verify cycle begins. For this example, verify reference voltage Vref3 is compared with the bit line voltage. This internally controlled program/verify cycle repeats itself until the bit line voltage on terminal 102 exceeds Vref3. At this time, t2, the EANVM cell 102 is verified to have been programmed to a (1,0) state and programming is halted by the comparator 222 providing a disable signal on signal line 204 to the program voltage switch 220.

Fig. 12 illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1,1) to a partially "off" state (1, 0) using fixed length program pulses. When the externally applied PGM/Write pulse is applied at time t1, the program/verify timing circuit 208 first initiates a verify cycle to determine the current status of the memory cell 102. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, Vpull-up. Although, prior to time t1, the bit line voltage could be pre-set to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage, Vref3 in this example, corresponding to the data to be programmed, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first fixed length programming pulse ends, a verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between ground potential and Ref1. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues until the bit-line voltage exceeds the selected verify reference voltage, in this case Vref3, which indicates a memory state of (1,0), at time t2.

Fig. 13 illustrates how a 2-bit EANVM cell is programmed from an erased (1,1) state to a (1,0) state using variable length programming pulses. The internal PGM pulses for this implementation start with a low state longer than for fixed-width implementation of Figures 11 and 12. The low-state pulse widths grow progressively shorter as the memory

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cell approaches the appropriate voltage threshold. This approach requires more precise control than the fixed length approach. However, programming times can be greatly reduced on average.

Fig. 14 illustrates the bit line voltage of a 2-bit per cell EANVM as it is being programmed from a fully erased, or fully "on", state (1,1) to a partially "off" state (1,0) using variable length program pulses. When the externally applied PGM/Write pulse goes to an active low level at time t1, the program/verify timing circuit 208 first initiates a verify cycle to determine the current status of the memory cell 102. This is indicated by the bit line voltage being pulled to a ground condition from, in this example, vpull-up. Although, prior to time t1, the bit line voltage could be pre-set to any voltage level. Once the cell has been determined to be at a condition below the verify reference voltage corresponding to the data to be programmed, Vref3 in this example, the first program cycle is initiated. This is represented by the bit line voltage being pulled up to Vprogram. After the first variable length programming pulse is over, another verify cycle begins. This is represented by the bit line voltage being pulled down to a point midway between Ref1 and Ref2. During each successive verify cycle the bit line voltage is observed to incrementally increase. This program/verify cycle continues until the bit-line voltage surpasses the selected verify reference voltage, in this case Vref3 which indicates a memory state of (1,0), at time t2.

Accordingly, the programming process for an n-bit per cell EANVM uses program/verify cycles, to incrementally program a cell. The duration<sup>5</sup> of these cycles are determined by the timing circuit 208. A key element of the system is to provide a programming scheme which provides for accurate programming of the memory cell 102. This is accomplished by matching the pulse widths of the timing pulses of the timing circuitry 208 to the program time of the EANVM cell being used. As indicated in Figures 11 and 13, a desired voltage threshold actually falls within a range of threshold voltages. If the program pulses are too long, then too much charge may

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be added to the floating gate of the memory cell 102. This may result in an overshoot of the target voltage threshold, resulting in incorrect data being stored in the memory cell.

The programming pulse width is set such that if the voltage threshold of the cell 102 after the (n-1) programming pulse is at a point just below the target voltage threshold, then the (n)th, or final, program pulse will not cause an overshoot resulting in an overprogrammed condition for a memory cell.

Fig. 8 may also use a digital comparator rather than the analog comparator 202 shown in Figure 8. The digital comparator would use the encoded data from the encode circuitry 160 as the input to the comparator represent the ~~current contents of the EAVM cell 102~~. The verify reference voltage select 222 would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed. Otherwise, the function of the comparator within the system remains the same.

## V. EMBODIMENTS TO ESTABLISH REFERENCE VOLTAGES

A multi-level (or multi-bit) memory device which contains more than one bit of information per memory cell needs accurate and stable reference voltages. The reference voltages allow a multi-level memory cell to be correctly read over various process, voltage, and temperature ranges. The reference voltages must be implemented into the integrated circuit which can accurately sense the multi-level voltage levels of the memory cells as well as track each memory array voltage level as it drifts with the process, voltage, and temperature variations. An unstable or inaccurate reference voltage tends to cause problems such as an improper voltage level read of a bit line, and the like from a memory cell.

In a 2-bit per memory cell embodiment, the memory cell includes four voltage levels V0, V1, V2, and V3 at each of the bit lines as illustrated by Figure 15. To uniquely detect each of the four voltage levels, it is necessary to generate at least three reference voltages, each of the

reference voltages falling between memory bit line voltage levels. When V0, V1, V2, and V3 represent the four bit line voltage levels, the reference voltages VREF0, VREF1, AND VREF2 fall between V0 and V1, V1 and V2, and V2 and V3, respectively. Preferably, the reference voltages VREF0, VREF1, and VREF2 fall halfway between V0 and V1, V1 and V2, and V2 and V3, respectively. Each reference voltage is also set to provide a clear and accurate reference level, which can be used as a reference for the bit line voltage.

In a specific embodiment, a method for establishing reference voltages for a non-volatile multi-bit memory array is provided. Merely by way of example, the present method is applied to the manufacture of a non-volatile multi-bit memory array such as a masked ROM array, an EANVM memory array, and the like. The present method calls for reference voltage sources and in particular reference voltage lines and cells which are fabricated simultaneously with the standard memory cell array. Alternatively, the present method may call for reference voltage sources and in particular reference voltage lines and cells which are fabricated by way of the same method (but at a different step) as the standard memory cell array. By way of the present method, stable reference voltages are established which track bit line voltages in memory cells through voltage, temperature, and process variations.

In a masked ROM embodiment, for example, the present method calls for reference voltages to be generated using memory cells which have been programmed in the same fashion and preferably in exactly the same fashion as the cells in the standard memory array itself. In the present masked ROM embodiment whose memory cells are programmed using a Vt implant, the memory cells within the reference voltage generator circuit will be implanted at the same time with preferably the same implant dosage as the ROM cells within the standard memory array. This means the implant dosage of the reference voltage cell is substantially the same as the memory cell for the bit line in the standard memory array. The reference voltage level is also substantially the same as the bit line voltage level, that is, assuming the same voltage is

applied to both the reference voltage cell and the bit line cell. As show in Fig. 16 for example, memory cells within the reference voltage generator circuit include field effect transistors 1103, 1104, 1105, 1106, 1107, and 1108. A ROM cell in a memory array may include transistor 1102 coupled to a bit line.

In the present embodiment, the reference voltage is moved to a voltage point away from the bit line voltage. This allows the multi-bit memory device to sense the relative voltage difference between the bit line and the reference voltage line, and then decode the programmed cell accordingly. By way of the same implant step, the reference voltage tracks the bit line voltage over process, voltage, and temperature variations, and is therefore stable.

In the present invention, a selected voltage difference exists between the voltage reference levels and memory bit line voltage levels such that they do not interfere with each other. The voltage reference and sensing circuitry are able to detect a single unique voltage level out of four possible levels, in a 2-bit per memory cell configuration for example. Referring to Fig. 15, if VREF0 was inadvertently raised to the level of VREF1, a non-programmed memory state of (1,1) is easy read. Unfortunately, if the memory cell was programmed to an intermediate state of (1,0), the relation between VREF0 to VREF1 makes it difficult to differentiate between the two levels. As a result, the output is often unreliable and the like. Accordingly, the present invention relies upon either a voltage divider arrangement, a pull-up device arrangement, or the like, and combinations thereof to create desired reference voltage levels. Although the present invention is described in the masked ROM embodiment, the present invention may also be applied to any multi-bit memory array such as an EANVM memory array, and the like.

Fig. 16 is a simplified reference voltage generator circuit in a voltage divider arrangement 1200 for generating multiple reference voltages according to the present invention. In a 2-bit per cell embodiment, a multi-level memory cell includes at least four bit line voltage levels V0,

V2, V3, and V4. Each of the four bit line voltage levels is detected by way of three reference voltage levels, each of which falls between two adjacent bit line voltage levels. The voltage divider arrangement includes a VREF0 column 1204, a VREF1 column 1206, and a VREF2 column 1208. Each column includes at least a pull-up voltage VPULLUP. A bit line column 1202 is also shown for illustrative purposes. The bit line column is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either V0, V1, V2, or V3, depending upon the particular application. A plurality of rows 1212, 1214 (or SELECT lines) are also shown. The SELECT line 1212 includes a plurality of field effect transistors 1109, and the SELECT line 1214 includes a plurality of field effect transistors 1101. Each of the columns also includes a WORD line 1216 operably coupled to each column through field effect transistors 1102, 1103, 1104, 1106, 1107, and 1108. The field effect transistors 1102, 1103, 1104, 1106, 1107, and 1108 include a source/drain region at V, V0, V1, V2, V3, respectively. The field effect transistors may include an NMOS device, a PMOS device, and the like.

As shown, each pair V0 and V1, V1 and V2, and V2 and V3 connect together with a voltage divider arrangement to generate intermediate reference voltages VREF0, VREF1, and VREF2, respectively. By way of the field effect transistors 1103, 1104, and application of voltage at the WORD line and the SELECT line 1212, the reference voltage VREF0 is at a voltage level between about V0 and about V1. By way of application of voltage at the WORD line and SELECT line 1212, the reference voltage VREF1 is between about V1 and about V2. Similarly, by way of application of voltage at the WORD line and the SELECT line 1212, the reference voltage VREF2 is between about V2 and about V3.

Fig. 17 illustrates the reference voltage levels of for example Fig. 16 according to the present invention. The voltage divider arrangement defines the reference voltages as follows:

$$VREF0 = (V0 + V1)/2$$

$$VREF1 = (V1 + V2)/2$$

$$VREF2 = (V2 + V3)/2$$

5 The reference voltages VREF0, VREF1, and VREF2 fall between V0 and V1, V1 and V2, and V2 and V3, respectively. Accordingly, the present multi-bit memory device provides reference voltages which do not overlap with the bit line voltages. In addition, the reference voltages VREF0, VREF1, and VREF2 track well with the memory bit lines over process, voltage, and temperature variations. Preferably, each of the reference  
10 voltages fall exactly halfway between adjacent bit line voltage levels.

Fig. 18 is a simplified voltage generator circuit diagram 1400 of an array showing reference voltage columns connected to pull-up devices according to the present  
15 invention. Each of the pull-up devices is a field effect transistor such as an NMOS device, a PMOS device, and the like. Preferably, the pull-up device is a PMOS device. A bit line column 2002 is also shown for illustrative purposes. The  
20 bit line column is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either V0, V1, V2, or V3, depending upon the particular application. The bit line also includes a field effect transistor 1102 and a word line 2016 operably coupled to the  
25 field effect transistor.

The voltage generator circuit includes a plurality of reference voltage column lines 2004, 2006, 2008, each at the same voltage level on one end VPULLUP, a plurality of field effect transistors 1101, 1109, and a reference voltage  
30 at the other end VREF0, VREF1, and VREF2. Between field effect transistors 1101, 1109 are cells which include field effect transistors 1103, 1105, and 1107. The field effect transistors 1103, 1105, and 1107 include source/drain regions coupled to V0, V1, and V2, and source/drain regions coupled to  
35 column lines 2004, 2006, and 2008, respectively. A word line connects in parallel to each of the field effect transistor (1103, 1105, and 1107) gates. A plurality of SELECT lines

2012, 2014 connect to the transistor (1109, 1101) gates. The bit line and reference voltage lines include pull-up devices 1110, 1111, 1112, and 1113, respectively. The pull-up devices create the reference voltage levels and memory bit line voltage level for sensing multi-levels on the memory bit line.

5 The pull-up devices are defined on the reference voltage lines. A pull-up device is also defined on the bit lines in the memory array. The desired reference voltages VREF0, VREF1, and VREF2 can be made by modifying the size and/or number of pull-ups such as field effect transistors and the like. The reference voltages are preferably at voltage levels corresponding to ones illustrated by Fig. 16 for example. Preferably, the pull-ups are added at the point where reference signals (corresponding to reference voltages) feed directly into a sense amplifier circuit, and not on each bit line. Determining the appropriate pull-up device size can occur on a trial and error basis during the course of circuit simulation. Other types of pull-up devices or circuitry such as capacitor and resistor combinations, and the like may also be used. Of course, the type of pull-up device and its configuration depend upon the particular application.

20 The embodiment of Fig. 18 generally provides a wider voltage range, than the embodiment of Fig. 17. The circuit for each reference voltage is no longer substantially dependent upon a maximum voltage range on the bit line. The effective voltage range can be scaled up across a wider range through use of selected pull-up devices. This provides for a greater margin of manufacture by the wider range between the voltages. The increased voltage range insures that an adequate signal is available to sense the difference between the memory bit line voltage and that of the reference voltage. As previously noted, the pull-up device is preferably a PMOS device and the like.

30 Fig. 19 is a simplified voltage generator circuit diagram 1600 for obtaining reference voltages with use of pull-up devices and a voltage divider according to a preferred embodiment of the present invention. A bit line column 1602 is also shown for illustrative purposes. The bit line column

is a portion of the standard memory cell array. As noted above, the bit line produces a voltage at either V0, V1, V2, or V3, depending upon the particular application. The bit line also includes a field effect transistor 1102 and a word line 1616 operably coupled to the field effect transistor.

The voltage generator circuit diagram includes a plurality of reference voltage columns 1111, 1112, 1113, a plurality of field effect transistors 1612, 1614 coupled to SELECT lines, and a plurality of field effect transistors 1103, 1104, 1105, 1106, 1107, 1108 in each cell coupled to a WORD line 1616. Also shown are a plurality of pull-up devices 1111, 1112, and 1113 for a VREF0 line 1604, a VREF1 line 1606, and a VREF2 line 1608, respectively. The embodiment provides for a voltage divider arrangement such that each reference voltage tracks the bit line voltage in variations to process, temperature, voltage, and the like. In addition, the embodiment provides for each of the reference voltages VREF0, VREF1, and VREF2 to be conditioned by way of respective pull-up devices. A pull-up device 1110 may also condition the voltage at the bit line 1602.

Fig. 20 illustrates a simplified reference voltage generator circuit diagram 2000 according to the present invention. A bit line 2009 with four memory cells 2001, 2003, 2005, and 2007, each of which is programmed to one of four different threshold voltages (V0, V1, V2, V3) representing the possible states in a two bit per cell memory array is shown for illustrative purposes. The bit line is operable coupled through field effect transistors in the memory cells 2001, 2003, 2005, and 2007. The bit line also includes a select line, and word lines 0, 1, 2, and 3.

The reference voltage generator circuit includes reference voltage lines 2013, 2015, and 2017, for VREF0, VREF1, and VREF2, respectively. The reference voltage generator circuit includes cells 2019 which define a reference voltage array 2021. The reference voltage array includes bit lines 2023 (or reference voltage lines 2013, 2015, and 2017) which were preferably identical in fabrication to the bit lines such as the bit line 2009 in the memory array. For



example, the bit lines 2023 in the reference voltage array and the memory array are made by way of the same (or similar) processing steps.

5 The cells 2019 in the reference voltage array are programmed to one of four possible voltage thresholds V0, V1, V2, and V3. Optionally, the bit line in the reference voltage array which contains cells programmed to the highest threshold voltage V3 may be omitted, as cells programmed to a voltage threshold higher than the voltage on the word line will  
10 effectively be an open circuit. This memory bit line in the reference voltage array may be replaced by a voltage source, typically representing the highest voltage potential used in the particular integrated circuit.

15 In the present embodiment, the cell (or cells 2001, 2003, 2005, and 2007) in the memory array is programmed by way of a selected threshold voltage such as V0 and the like. All of the cells in the reference voltage array using the same threshold voltage is preferably programmed at the same time (or the same method) as the cell (or cells) in the memory  
20 array. For example, a cell(s) 2001 at a threshold voltage of V0 in the memory array is programmed by way of implant or the like at the same step as the cells 2025 at a threshold voltage of V0 in the reference voltage array. The cell(s) 2003 at a threshold voltage of V1 in the memory array is programmed by  
25 way of implant or the like at the same step as the cells 2027 at a threshold voltage of V1 in the reference voltage array. The cell(s) 2005 at a threshold voltage of V2 in the memory array is programmed by way of implant or the like at the same step as the cells 2029 at a threshold voltage of V2 in the  
30 reference voltage array. Other threshold voltages 2007 may be programmed into the cells by way of similar programming techniques and the like. The selected programming technique may include a single threshold voltage implant or multiple threshold voltage implants corresponding to a series  
35 programming steps. An example of such programming step can be any suitable technique known in the art.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of

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illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were  
5 chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended  
10 that the scope of the invention be defined by the claims appended hereto and their equivalents.

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WHAT IS CLAIMED IS:

- 5 *Sub*  
*AN*
1. A multi-level memory device comprising:  
a multi-level cell means for storing input  
information for an indefinite period of time as a discrete  
state of said multi-level cell means; said multi-level cell  
means storing information in  $K^n$  memory states, where  $K$  is a  
base of a predetermined number system and  $n$  is a number of  
bits stored per cell, wherein  $K^n > 2$ ;  
memory cell programming means for programming said  
10 multi-level cell means to a memory state corresponding to said  
input information;  
comparator means for comparing said memory state of  
said multi-level cell means with said input information, said  
input information corresponding to one of a plurality of  
15 reference voltages; said comparator means further generating a  
control signal indicative of said memory state as compared to  
said input information.
  2. The device of claim 1 wherein said plurality of  
reference voltages are one less than said  $K^n$  memory states.
  - 20 3. The device of claim 1 wherein each of said plurality  
of reference voltages is between two of said  $K^n$  memory states.
  4. The device of claim 1 further comprising a reference  
voltage means for defining said plurality of reference  
voltages.
  - 25 5. The device of claim 4 wherein said reference voltage  
means includes a pull-up device operably coupled to a  
reference voltage line to provide one of said plurality of  
reference voltages.
  6. The device of claim 5 wherein said reference voltage  
30 means comprises a voltage divider.
  7. The device of claim 6 wherein said voltage divider  
comprises a reference voltage line operably coupled to a first
- 25*

voltage and a second voltage to provide a reference voltage between said first voltage and said second voltage, said first voltage and said second voltage corresponding to two of said  $K^n$  memory states.

5 8. The device of claim 7 wherein said reference voltage line is operably coupled to said first voltage and said second voltage through a first voltage line and a second voltage line, said first voltage line coupled to said first voltage through a first transistor and said second voltage line coupled to said second voltage through a second transistor.

10 9. The device of claim 8 wherein said reference voltage line is operably coupled to a pull-up device, said pull-up device being adapted to said reference voltage line to provide said reference voltage.

15 10. The device of claim 9 wherein said pull-up device comprises a field effect transistor.

11. A multi-level memory device comprising:  
multi-level cell means for storing input information for an indefinite period of time as a discrete state of said  
20 multi-level cell means, said memory cell means storing information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per cell, wherein  $K^n > 2$ ;

25 multi-level cell programming means for programming said multi-level cell means to a state corresponding to said input information;

30 comparator means for comparing said memory state of said multi-level cell means with said input information, said input information corresponding to one of a plurality of reference voltages, said comparator means further generating a control signal indicative of said memory state as compared to said input information; and

reference voltage means for defining said plurality of reference voltages, said reference voltage means operably coupled to said comparator means.

5 12. The device of claim 11 wherein said reference voltage means is a voltage divider.

13. The device of claim 11 wherein said reference voltage means includes a pull-up device operably coupled to a reference voltage line to provide one of said plurality of reference voltages.

10 14. The device of claim 11 wherein said reference voltages track said information in  $K^n$  memory states.

15 15. The device of claim 11 wherein said voltage divider comprises a reference voltage line operably coupled to a first voltage and a second voltage to provide a reference voltage between said first voltage and said second voltage, said first voltage and said second voltage corresponding to two of said  $K^n$  memory states.

20 16. The device of claim 15 wherein said reference voltage line is operably coupled to said first voltage and said second voltage through a first voltage line and a second voltage line, said first voltage line coupled to said first voltage through a first transistor and said second voltage line coupled to said second voltage through a second transistor.

25 17. The device of claim 15 wherein said reference voltage line is fabricated during a same step as a bit-line.

30 18. The device of claim 15 wherein said reference voltage line is operably coupled to a pull-up device, said pull-up device being adapted to said reference voltage line to provide said reference voltage.

19. The device of claim 18 wherein said pull-up device comprises an field effect transistor.

20. The device of claim 19 wherein said reference voltages track said information in  $K^n$  memory states through selected temperature and voltage variations.

21. An integrated circuit comprising a plurality of multi-level cells, said integrated circuit comprising:  
a multi-level memory cell for storing input information for an indefinite period of time as a discrete state of said multi-level memory cell, said multi-level memory cell storing information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per multi-level memory cell, wherein  $K^n > 2$ ;  
memory cell programming circuit for programming said multi-level memory cell to a memory state corresponding to said input information;  
a comparator for comparing said memory state of said multi-level memory cell with said input information, said input information corresponding to one of a plurality of reference voltages, said comparator means further generating a control signal indicative of said memory state as compared to said input information; and  
a reference voltage cell for providing said one plurality of reference voltages, said reference voltage cell operably coupled to said comparator;  
wherein said multi-level memory cell being defined by one of said plurality of multi-level cells and said reference voltage cell being defined by another of said plurality of multi-level cells.

22. An integrated circuit device comprising a plurality of multi-level cells, (said plurality of multi-level cells defining a multi-level memory cell and a reference voltage cell.)

23. An integrated circuit comprising a plurality of multi-level cells, said integrated circuit comprising:

a multi-level memory cell for storing input information for an indefinite period of time as a discrete state of said multi-level memory cell, said multi-level memory cell storing information in  $K^n$  memory states, where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per multi-level memory cell, wherein  $K^n > 2$ ;

memory cell programming circuit for programming said multi-level memory cell to a memory state corresponding to said input information;

a comparator for comparing said memory state of said multi-level memory cell with said input information, said input information corresponding to one of a plurality of reference voltages, said comparator means further generating a control signal indicative of said memory state as compared to said input information; and

a reference voltage cell for providing said one plurality of reference voltages, said reference voltage cell operably coupled to said comparator;

wherein said multi-level memory cell being defined by one of said plurality of multi-level cells and said reference voltage cell being defined by another of said plurality of multi-level cells, said multi-level memory cell being programmed during a same step as said reference voltage cell.

ADD  
A87

## DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL** the specification of which   X   is attached hereto or        was filed on        as Application Serial No.        and was amended on        (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

## Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes <u>      </u> No <u>      </u>
			Yes <u>      </u> No <u>      </u>

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Date of Filing	Status
08/071,816	June 4, 1993	<u>      </u> Patented <u>  X  </u> Pending <u>      </u> Abandoned
07/652,878	February 8, 1991	<u>  X  </u> Patented <u>      </u> Pending <u>      </u> Abandoned

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Richard T. Ogawa, Reg. No. 37,692  
Gary T. Aka, Reg. No. 29,037

Send Correspondence to:  TOWNSEND and TOWNSEND KHOURIE and CREW Steuart Street Tower One Market Plaza, 20th Floor San Francisco, CA 94105	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)  Name: Richard T. Ogawa Reg. No. 37,692 Telephone: 415 326-2400
--	---

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(Page 1 of 2)



Full Name of Inventor 1	Last Name Banks	First Name Gerald	Middle Name or Initial J.	
Residence & Citizenship	City Fremont	State/Foreign Country California	Country of Citizenship U.S.A.	
Post Office Address	Post Office Address 200 Pawnee Place	City Fremont	State/Country CA	Zip Code 94539
Full Name of Inventor 2	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor 3	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Gerald J. Banks		
Date	Date	Date

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AS ORIGINALLY FILED

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365/189.01  
Fears

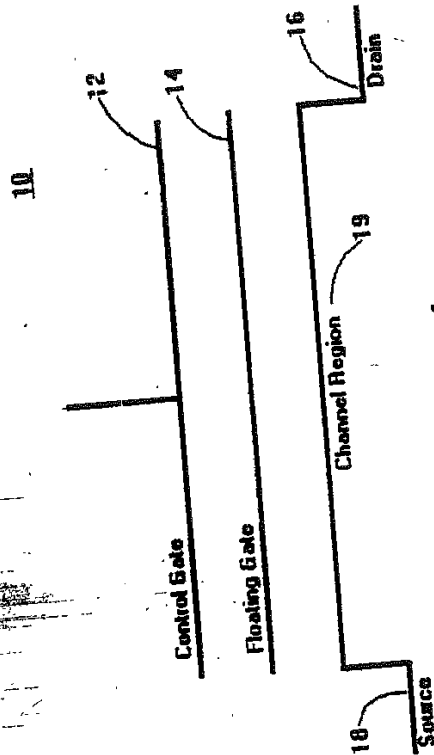
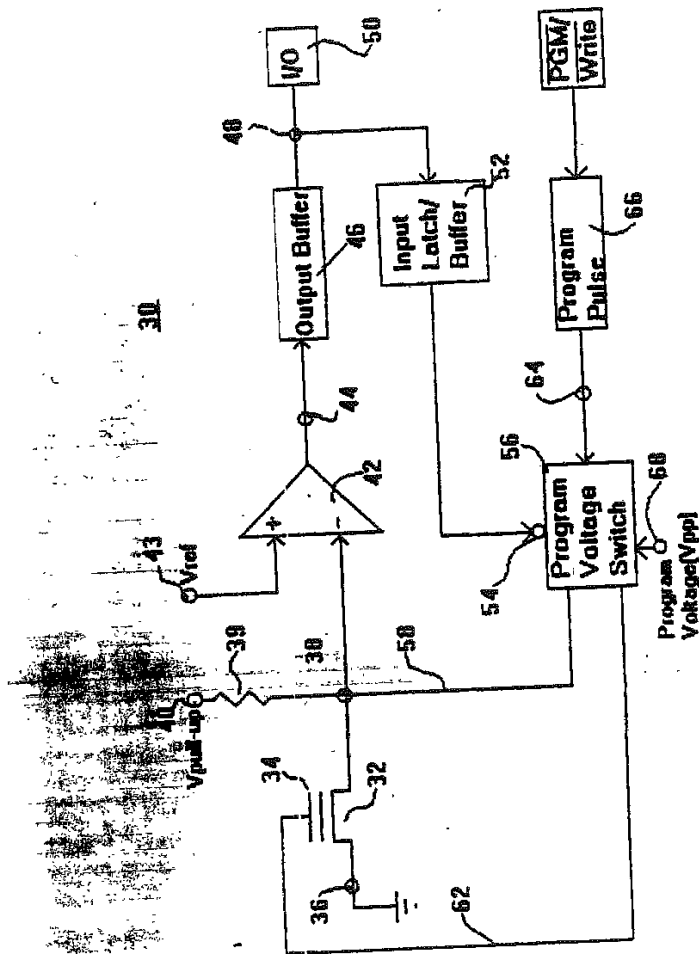


Figure 1

30



Prior Art  
Figure 2

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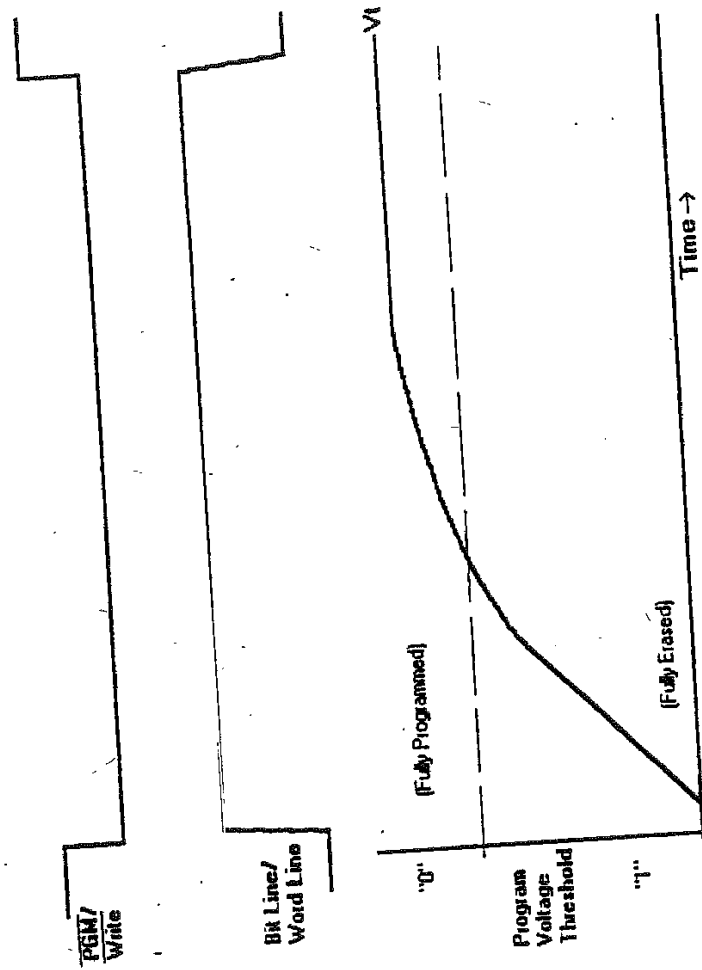
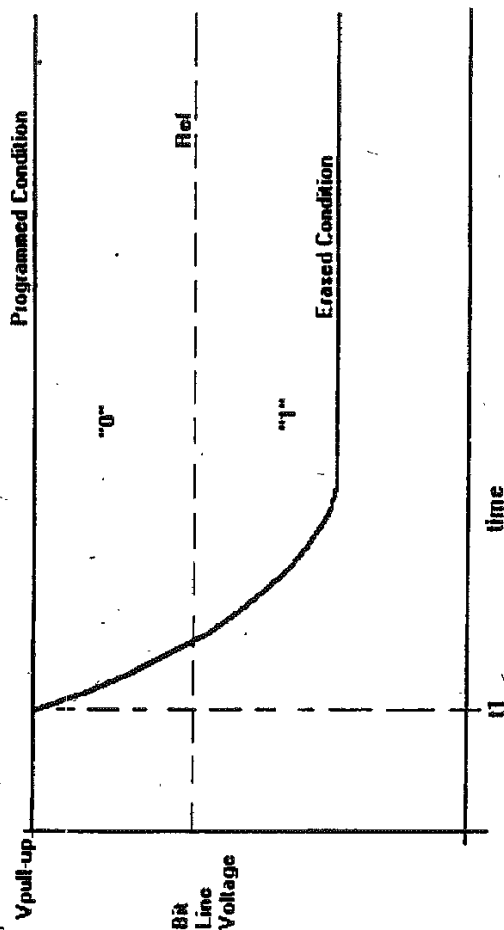


Figure 3



Prior Art Read  
Figure 4

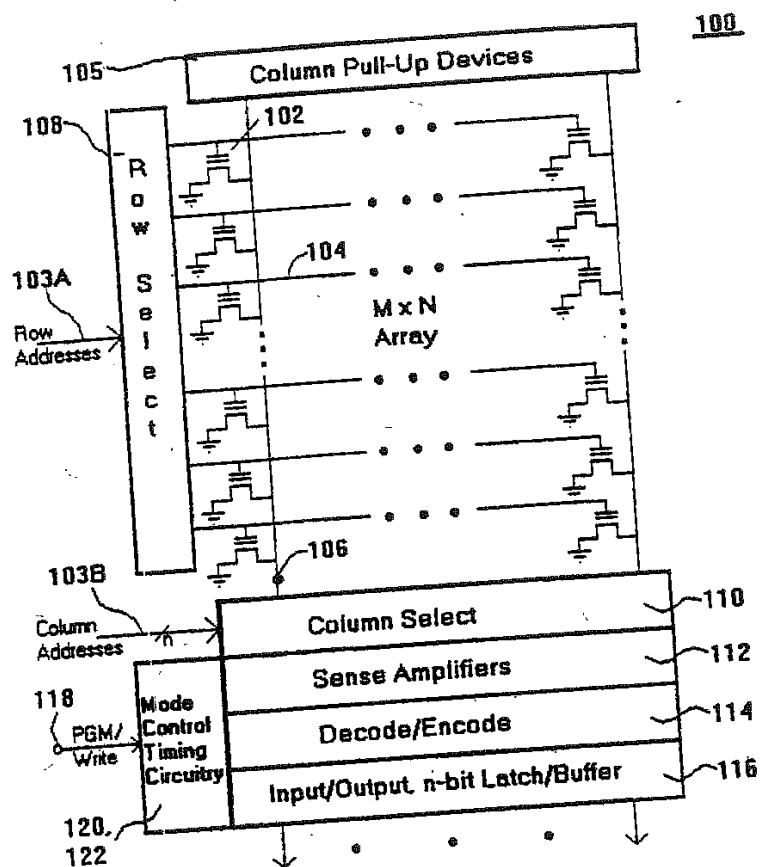


Figure 5

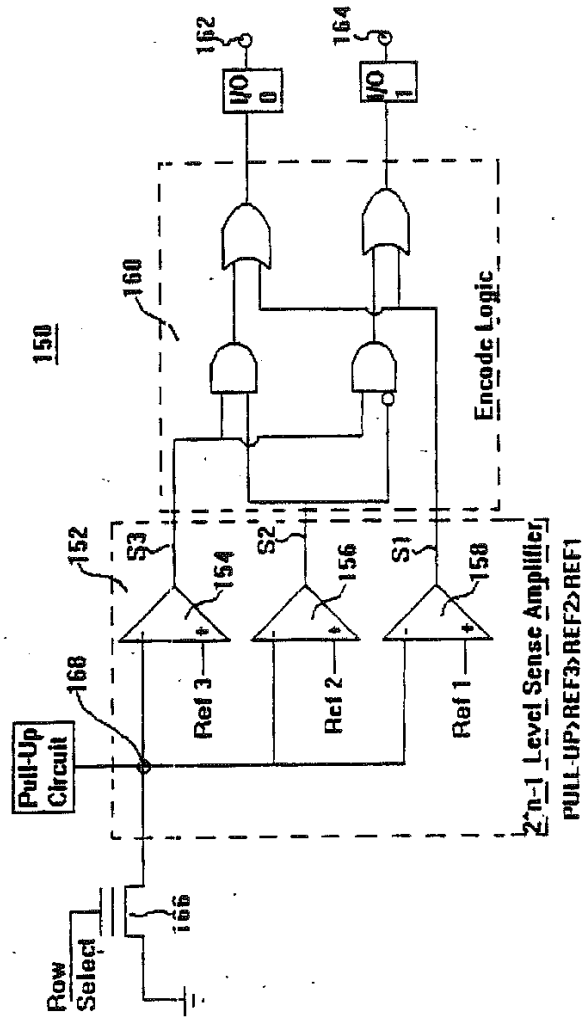


Figure 6

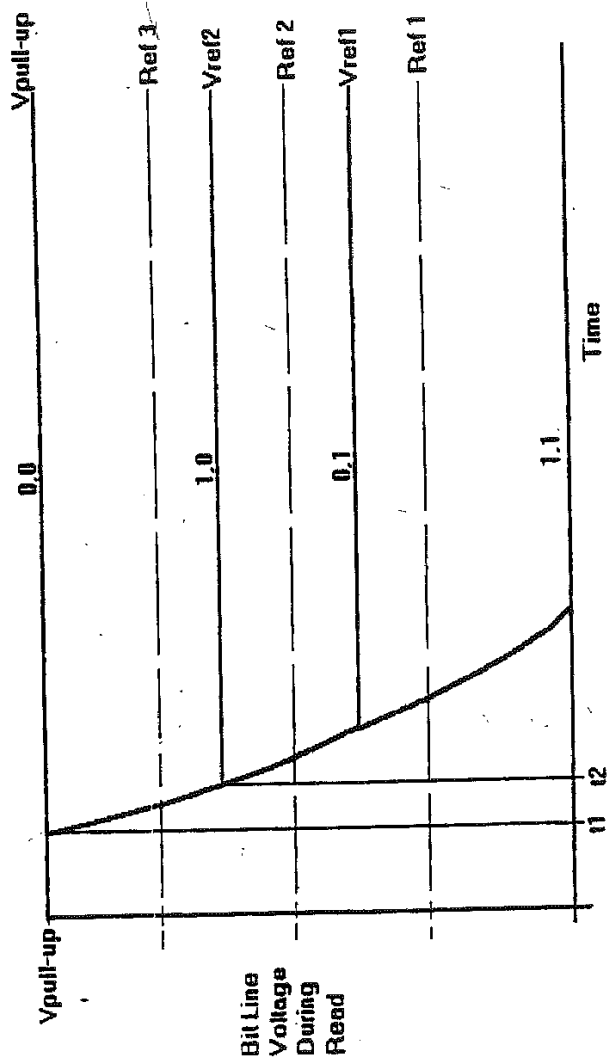


Figure 7



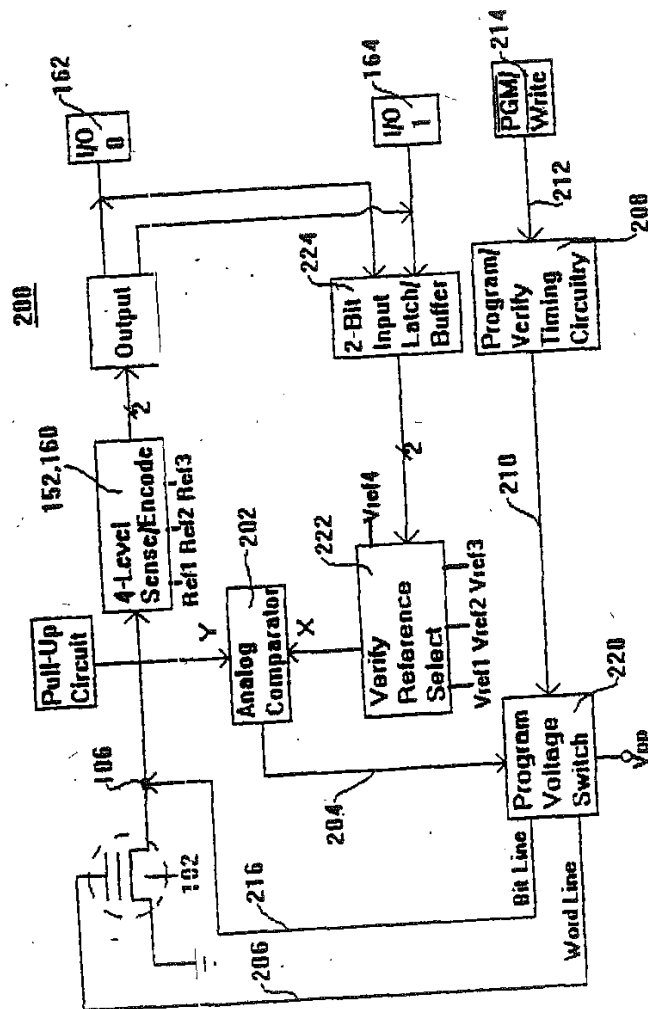


Figure 8

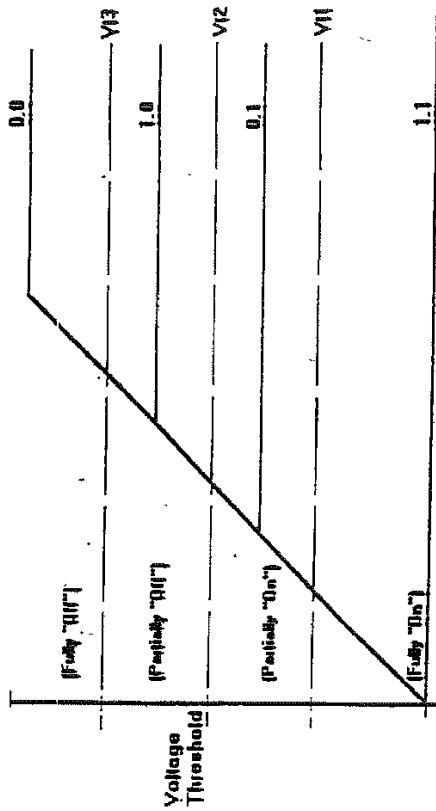


Figure 9

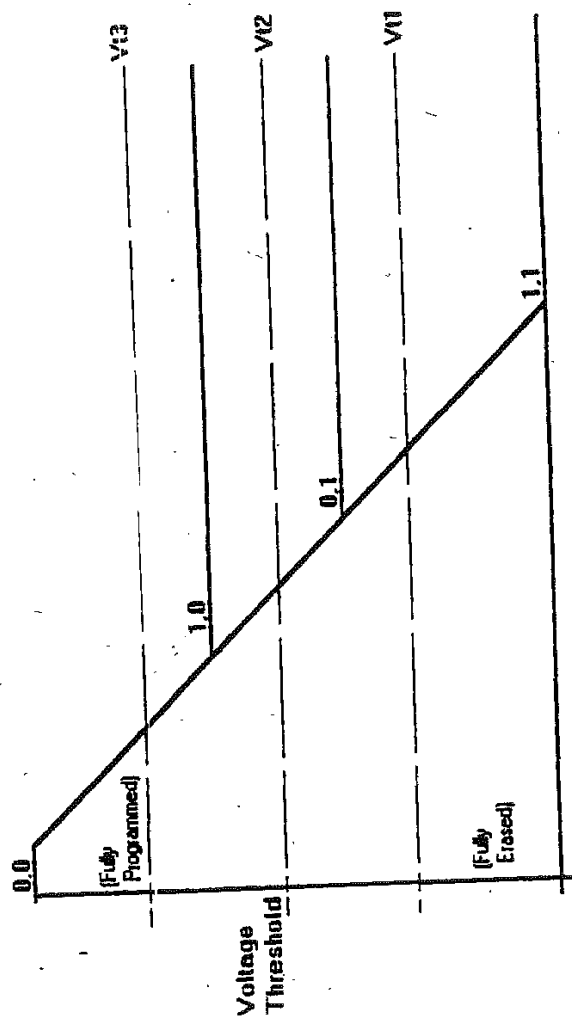


Figure 10

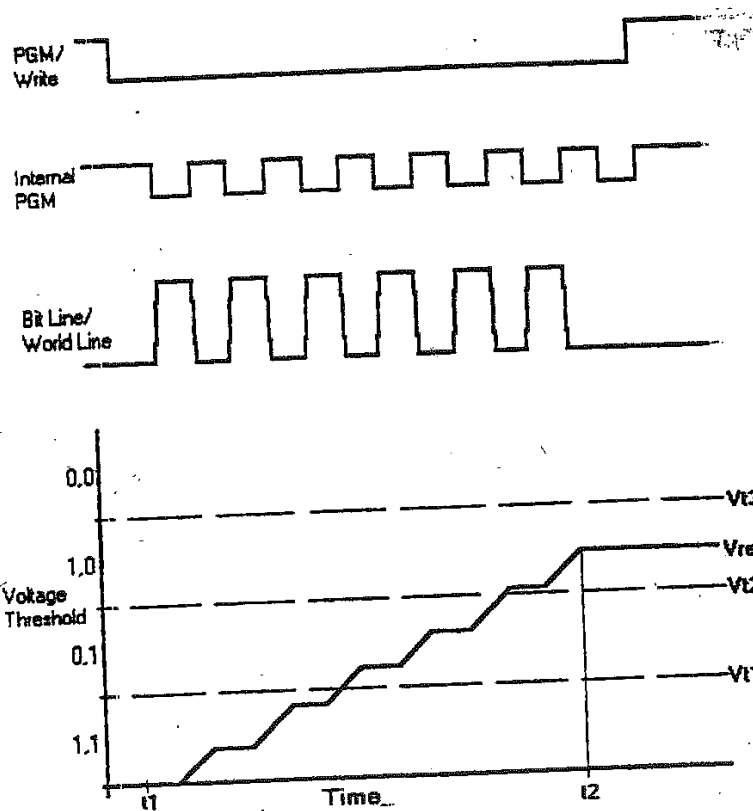


Figure 11

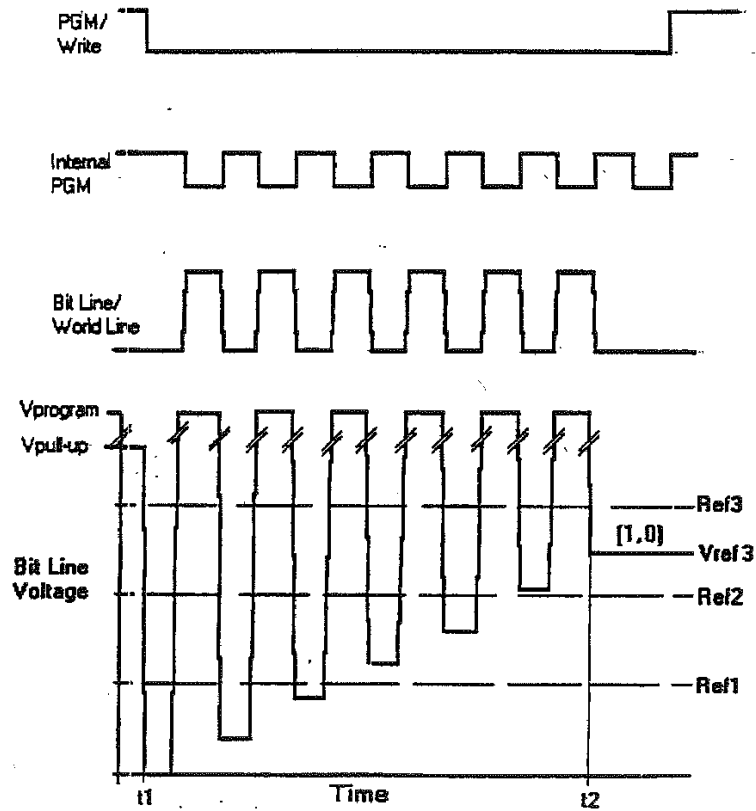


Figure 12

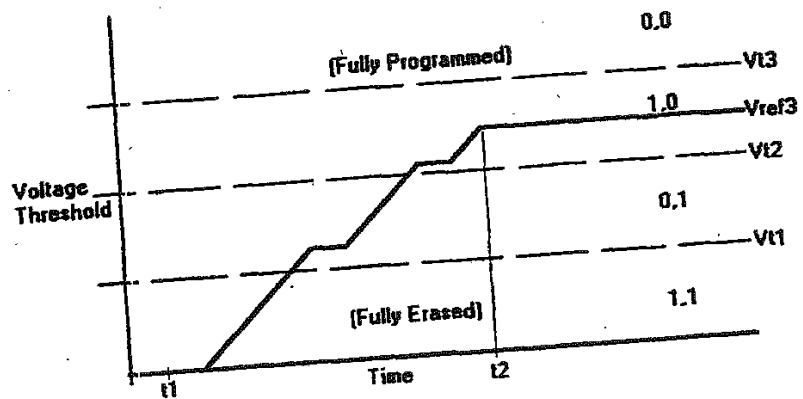
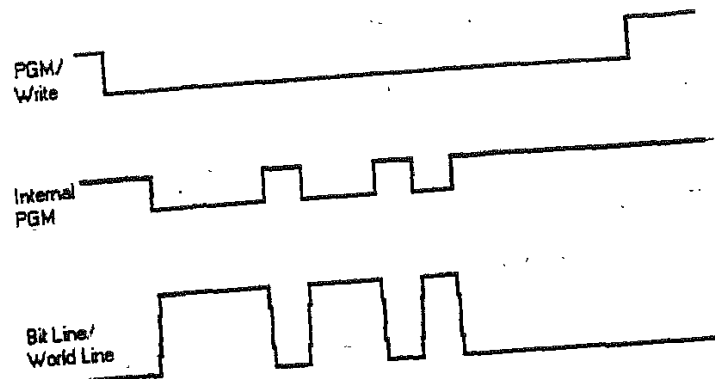


Figure 13

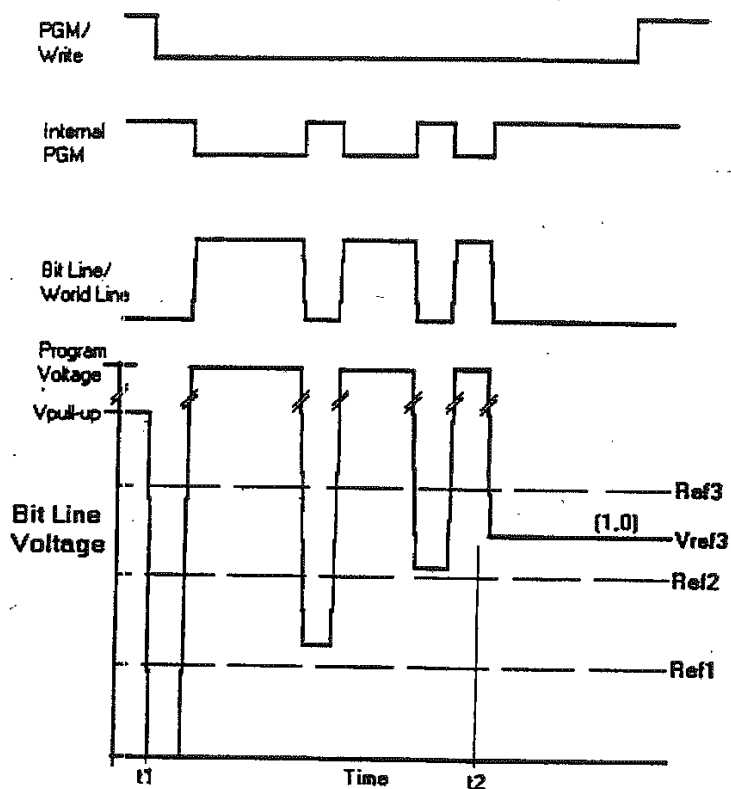


Figure 14

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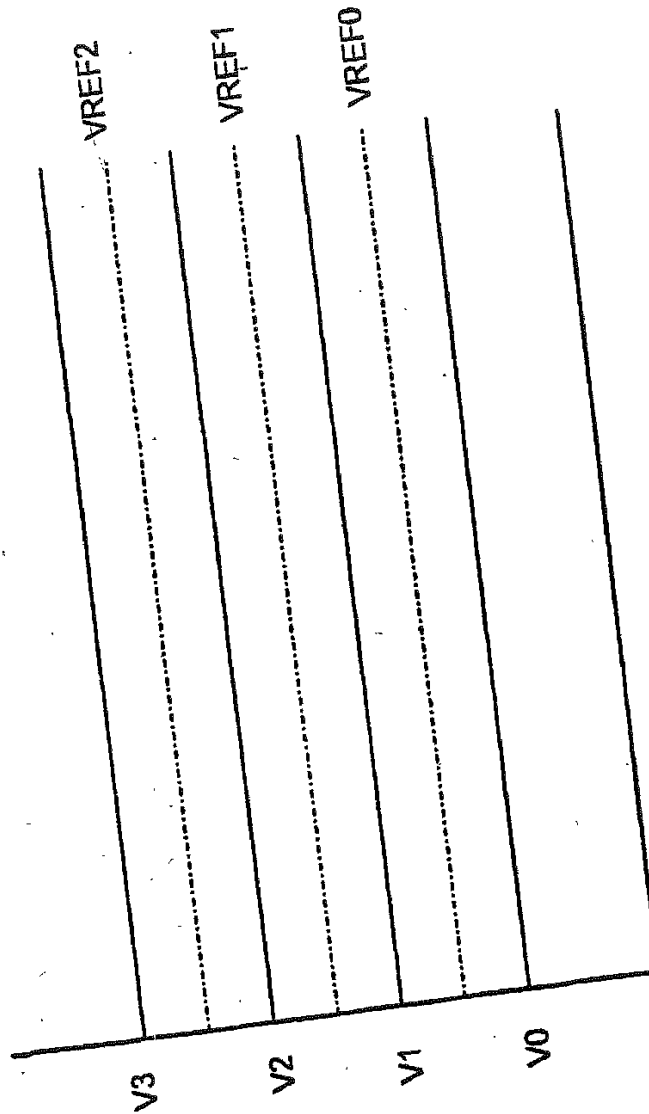


FIG. 15



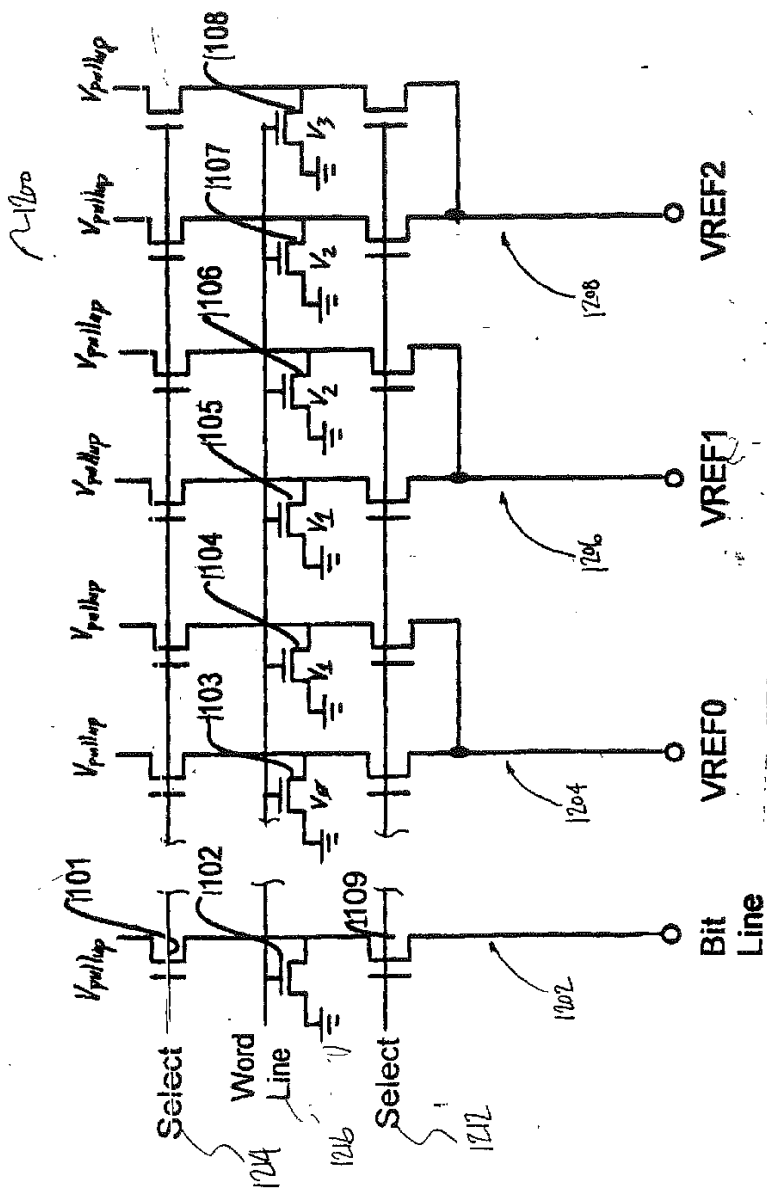


FIG. 16

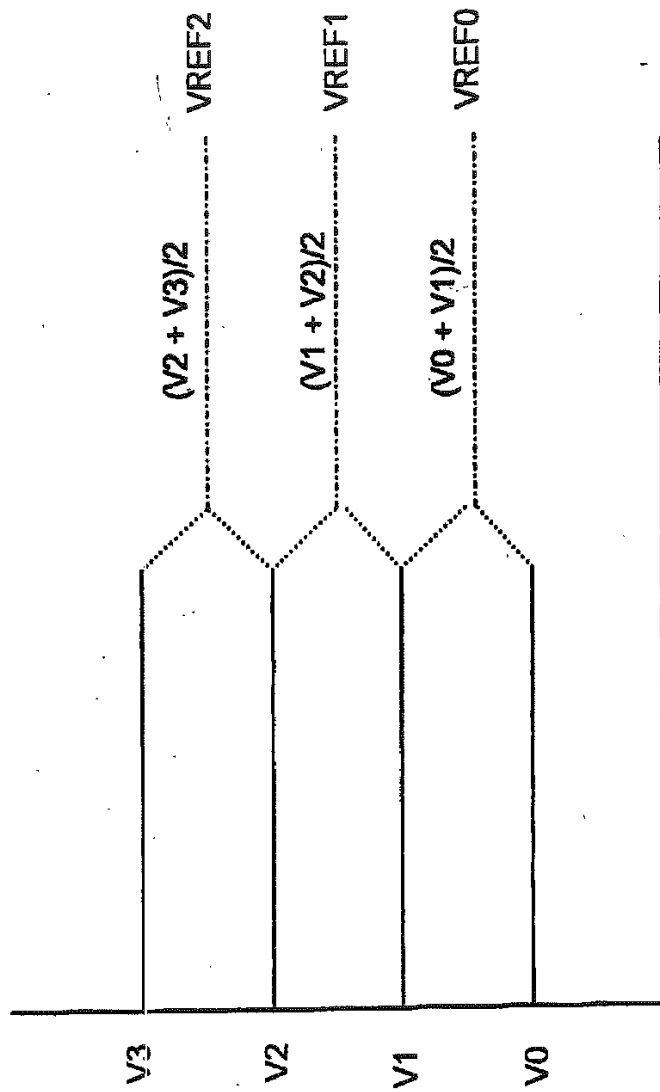


FIG. 17

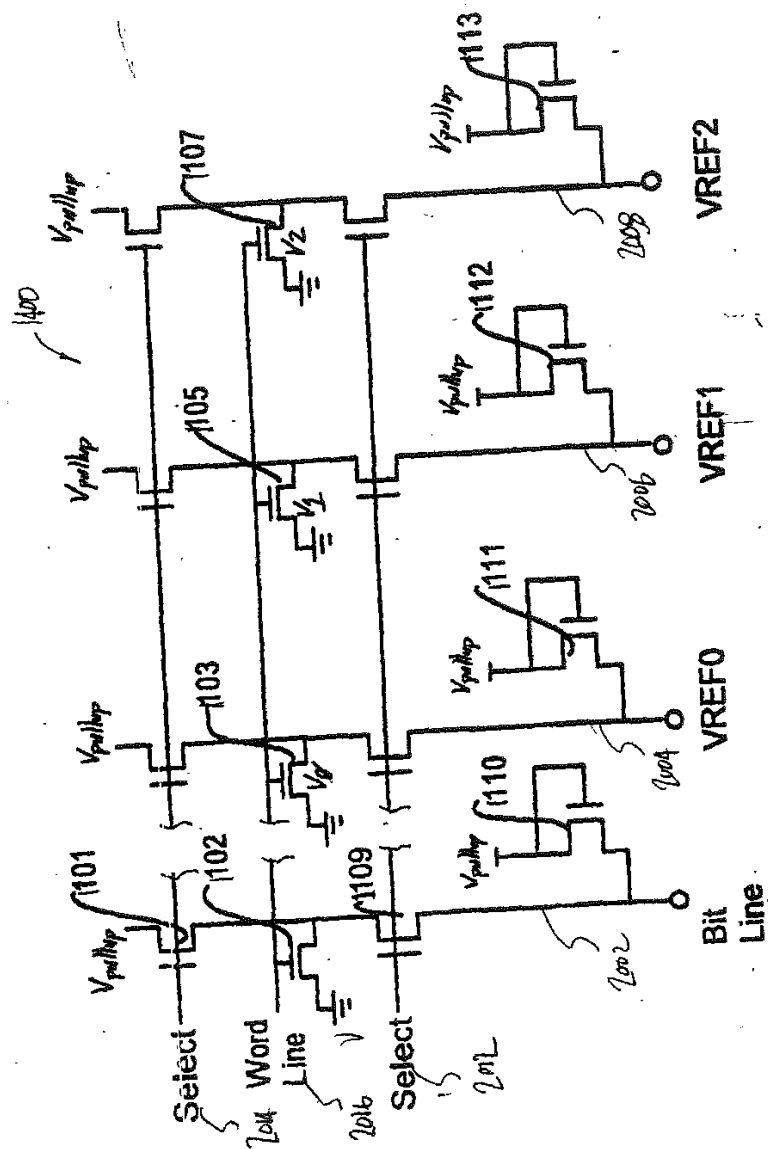
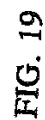


FIG. 18

19/2



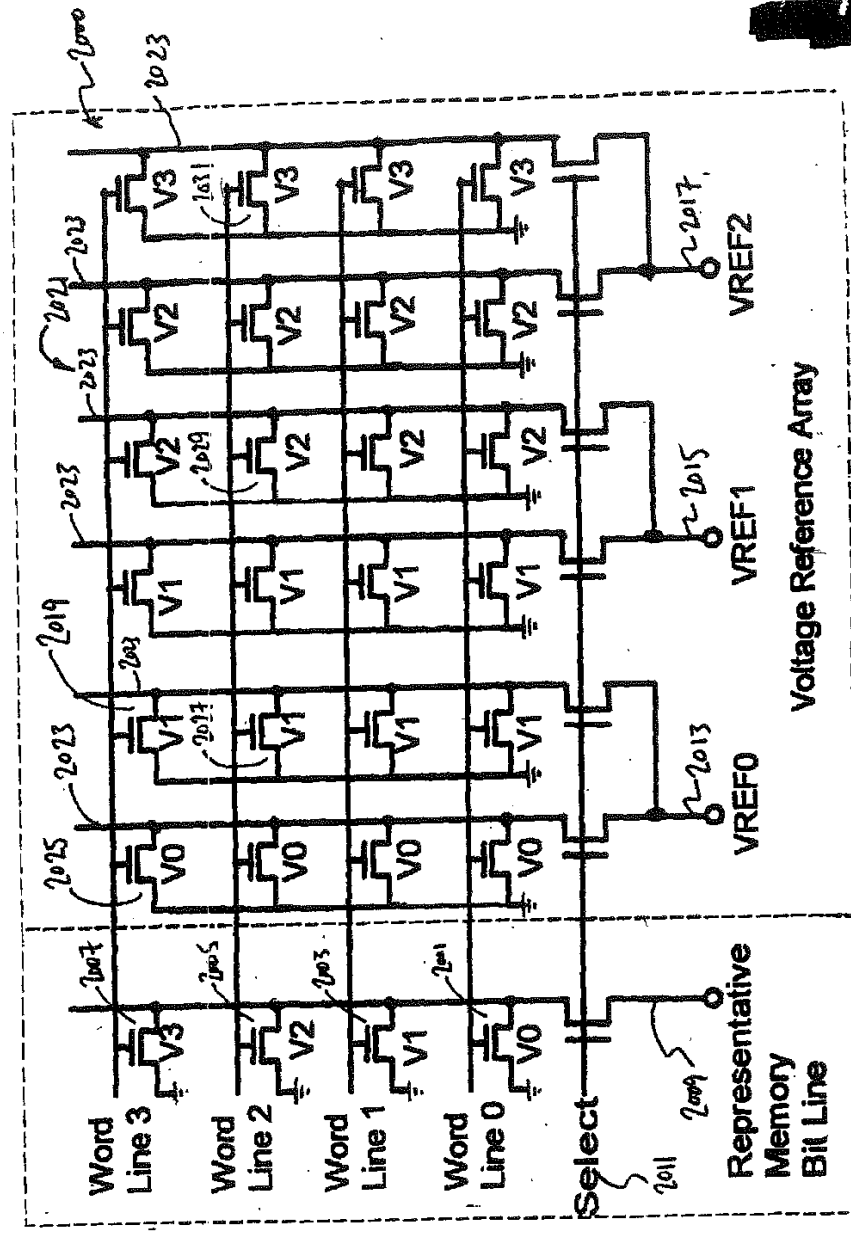


FIG. 2D

TOWNSEND and TOWNSEND KHOURIE and CREW

Stewart Street Tower  
One Market Plaza  
San Francisco, CA 94105  
(415) 543-9600

PATENT APPLICATION  
COMMISSIONER OF PATENT AND TRADEMARKS  
Washington, D. C. 20231



08-410 0

Atty. Docket No. 16176-1-1

"Express Mail" Label No. TB 174 786 359 US

Date of Deposit 2/27/95

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D. C. 20231

By Richard T. Ogawa

Sir:

Transmitted herewith for filing is the  
☐ patent application of  
☐ design patent application of  
☒ continuation-in-part patent application of

100  
Inventor: Gerald J. Banks

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL

Enclosed are:

- ☒ 20 sheet(s) of ☐ formal ☒ informal drawing(s).
- ☐ An assignment of the invention to \_\_\_\_\_
- ☒ A ☐ signed ☒ unsigned Declaration & Power of Attorney.
- ☐ A ☐ signed ☐ unsigned Declaration.
- ☐ A Power of Attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ A certified copy of a \_\_\_\_\_ application.
- ☐ Information Disclosure Statement under 37 CFR 1.97.
- ☐

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

Telephone:  
(415) 543-9600  
APPNOFEE-TRN 1292

Richard T. Ogawa  
Reg. No.: 37,692  
Attorneys for Applicant



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
ASSISTANT SECRETARY AND COMMISSIONER  
OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

April 04, 1995

Richard T. Ogawa  
Townsend & Townsend, Khourie and Crew  
Steuart Street Tower, 20th Fl.  
One Market Plaza  
San Francisco, CA 94105

Newly Assigned Application No.: 08/410,200  
Applicant: Gerald J. Banks  
Title: Electrically Alterable  
Non-volatile Memory  
within Bits per call  
Docket No.:

**NOTICE OF NEWLY ASSIGNED APPLICATION NUMBER**

The above-identified patent application was previously erroneously assigned Application Number 29/035,674 through an administrative error. The new application number assigned to the application is listed in the heading of this letter. Please correct your records and refer to the new application number in all future correspondence to the Patent and Trademark Office.

The Office sincerely regrets any inconvenience that this situation has caused you. If you have any questions about this matter, please contact me at (703) 308-3164.

Sincerely,

*D. Dotson*  
Deborah Dotson  
Initial Review Division



I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail (label no. 7B174786414US) in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20131, on 8/7/95

By [Signature]

PATENT

Attorney Docket No. 16176-000110

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

/Gerald J. Banks

Serial No.: 08/410 200  
~~08/405,821~~

Filed: March 6, 1995

/For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL

Examiner: Unassigned

Art Unit: Unassigned

COMMUNICATION

Attn: Application Branch  
Assistant Commissioner for Patents  
Washington, D.C. 20231

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GROUP 330

Sir:

Applicant's undersigned attorney has noted that the filing date entered by the Application Branch on the Notice to File Missing Parts of Application has been designated as March 6, 1995 and not February 27, 1995. The application was mailed using proper Express Mail procedures on February 27, 1995 and is, accordingly, entitled to a filing date of February 27, 1995. Copies of the filed postcard and the Patent Application Transmittal/Fee Sheet are enclosed as Exhibits I, and II, respectively. No return postcard was received from the Patent Office mailroom. It is requested that the Patent Office correct their records or advise if for any reason it believes Applicant is not entitled to the February 27, 1995 filing date.

Respectfully submitted,

[Signature]  
Richard T. Ogawa  
Reg. No. 37,892

TOWNSEND and TOWNSEND and CREW  
One Market Plaza  
Steuart Street Tower, 20th Floor  
San Francisco, California 94105  
(415) 326-2400

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161761-1.com



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RECEIPT WILL BE MAILED TO YOU  
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PATENT APPLICATION  
FILING ACKNOWLEDGMENT

Mailing Date: February 27, 1995 Attorney: RTO/sam  
File No.: 16176-1-1  
Inventor(s): Gerald J. Banks  
Title: Electrically Alterable Non-Volatile Memory with N-Bits Per Memory Cell  
Declaration \_\_\_\_\_ Power of Attorney (unsigned)  
☒ Combined Declaration & Power of Attorney  
☐ Assignment \_\_\_\_\_ Small Entity Decl.  
No. Pages of Description: 29  
No. Pages of Appendix: 5  
No. Pages of Claims: 1  
No. Pages of Abstract: 20  
No. Sheets of Drawings: \_\_\_\_\_  
Microfiche Appendix: \_\_\_\_\_

Please stamp the date of receipt of the enclosed documents and return this card to addressee

EXHIBIT 1

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail (label no. TB174786414US) in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8/18/95



PATENT

Attorney Docket No. 16176-000110

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Gerald J. Banks

Serial No.: 08/410,200  
08/405,821

Filed: March 6, 1995

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL

Examiner: Unassigned

Art Unit: Unassigned

TRANSMITTAL OF PROCESSING AND RETENTION FEE UNDER 37 CFR \$1.78(a) and 1.21(l)

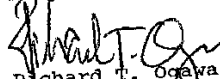
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

So that Applicant may claim benefit of the above-referenced application filing date in Application's co-pending application filed August 7, 1995, Applicant authorizes the Commissioner to charge the processing and retention fee under 37 CFR \$1.21(l) of \$130.00, and any other fees associated with this paper, to Deposit Account 20-1430. This Transmittal of Processing and Retention Fee is submitted in triplicate.

If a telephone interview would help expedite this matter, please telephone the undersigned at (415) 326-2400.

Respectfully submitted,

  
Richard T. Ogawa  
Reg. No. 37,692

TOWNSEND and TOWNSEND and CREW  
One Market Plaza  
Steuart Street Tower, 20th Floor  
San Francisco, California 94105  
(415) 326-2400

RTO/kaa  
16176-1-PRO.RET



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
--------------------	-------------	-----------------------	------------------------

08/410,200 02/27/95 BANK

16176-1-1

0232/0418  
TOWNSEND AMI TOWNSEND KHOURIE AND CREW  
STUART STREET TOWER  
ONE MARKET PLAZA  
SAN FRANCISCO 94105

DATE MAILED: 0000

**NOTICE TO FILE MISSING PARTS OF APPLICATION  
FILING DATE GRANTED**

Remailed 7/8/96  
04/18/95

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of \$130 for large entities or \$65 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e).

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is \$1,078.

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER**, within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

1. ☐ The statutory basic filing fee is: ☒ missing ☐ insufficient. Applicant as a ☒ large entity ☐ small entity, must submit \$730 to complete the basic filing fee.
2. ☒ Additional claim fees of \$218 as a ☒ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
3. ☐ The oath or declaration:  
☐ is missing.  
☐ does not cover the newly submitted items.  
  
An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date is required.
4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
5. ☒ The signature(s) to the oath or declaration is/are: ☒ missing; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration:  
  
An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.
7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of \$ under 37 CFR 1.17(k), unless this fee has already been paid.
8. ☐ A \$ processing fee is required since your check was returned without payment. (37 CFR 1.21(m)).
9. ☐ Your filing receipt was mailed in error because your check was returned without payment.
10. ☐ The application does not comply with the Sequence Rules. See attached Notice to Comply with Sequence Rules 37 CFR 1.821-1.825.
11. ☐ Other.

Direct the response to Box Missing Part and refer any questions to the Customer Service Center at (703) 308-1202.

**A copy of this notice MUST be returned with the response.**

OFFICE COPY

FORM PTO-1533 (REV. 11-94)



I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231,

on September 6, 1996  
TOWNSEND and TOWNSEND and CREW

By Alison Elvinger

PATENT

Attorney Docket No. 16176-000110

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
Gerald J. Banks	)	Examiner: Unassigned
Serial No.: 08/410,200	)	Art Unit: Unassigned
Filed: February 27, 1995	)	PETITION TO EXTEND TIME UNDER
For: ELECTRICALLY ALTERABLE	)	37 CFR §1.136(a)
NON-VOLATILE MEMORY WITH	)	
N-BITS PER MEMORY CELL	)	

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Applicant petitions the Assistant Commissioner for Patents to extend the time for response to the Notice to File Missing Parts, dated July 8, 1996 for one month, from August 8, 1996 to September 8, 1996. An appropriate response to the notice in the form of a Response to Notice of Missing Parts is enclosed herewith.

Please charge \$55.00, pursuant to 37 CFR §1.17, to the Deposit Account No. 20-1430. Please charge any additional fees or credit overpayment to the above Deposit Account. This Petition is submitted in triplicate.

Date: 9/5/96

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8th Floor  
San Francisco, California 94111-3834  
(415) 326-2400  
RTO:de

rto\work\16176\1-Text.txt

Respectfully submitted,

Richard T. Ogawa  
Richard T. Ogawa  
Reg. No. 37,692

510 16176-000110 Dkt. 09/06 14:00:00  
54104 2.5 21.0001

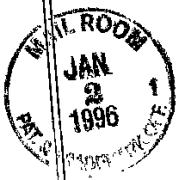
0300 4-24-95 #3 A/2

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By Alison Elzingre

PATENT

Attorney Docket No. 16176-000110



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: )  
Gerald I. Banks )  
Serial No.: 08/410,200 )  
Filed: March 6, 1995 )  
For: ELECTRICALLY ALTERABLE )  
NON-VOLATILE MEMORY WITH )  
N-BITS PER CELL )

Examiner: Unassigned  
Art Unit: Unassigned

COMMUNICATION

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MAY 17 1996  
UNITED STATES PATENT AND TRADEMARK OFFICE

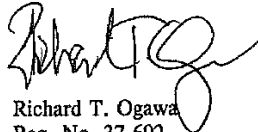
Attn: Application Branch  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Applicant's undersigned attorney has noted that the Serial Number assigned to the present application was incorrect. In particular, the Notice of Missing Parts recited a Serial No. 08/405,821. A letter mailed April 4, 1995 by the PTO referred to an incorrect Serial No. 29/035,674, which does not seem to exist anywhere. A copy of this letter is enclosed as Exhibit I. This letter also referred to Serial No. 08/410,200 as being the correct serial number. Please be advised that the correspondence mailed August 7, 1995 by Applicant referred to Serial No. 08/405,821, which is believed to be incorrect at this time. This correspondence should have Serial No. 08/410,200, which Applicant's

attorney believes is now the correct serial number.

Respectfully submitted,



Richard T. Ogawa  
Reg. No. 37,692

TOWNSEND and TOWNSEND and CREW  
One Market Plaza  
Steuart Street Tower, 20th Floor  
San Francisco, California 94105  
(415) 326-2400

RTO:de  
1617611-1-2nd.com



014-76-00011005  
UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
ASSISTANT SECRETARY AND COMMISSIONER  
OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
200 PTC

April 04, 1995

RECEIVED  
55 APR 10 6 19 24

Richard T. Ogawa  
Townsend & Townsend, Khourie and Crew  
Steuart Street Tower, 20th Fl.  
One Market Plaza  
San Francisco, CA 94105

Newly Assigned Application No.: 08/410,200  
Applicant: Gerald J. Banks  
Title: Electrically Alterable  
Non-volatile Memory  
within Bits per call  
Docket No.:

NOTICE OF NEWLY ASSIGNED APPLICATION NUMBER

The above-identified patent application was previously erroneously assigned Application Number 29/035,674 through an administrative error. The new application number assigned to the application is listed in the heading of this letter. Please correct your records and refer to the new application number in all future correspondence to the Patent and Trademark Office.

The Office sincerely regrets any inconvenience that this situation has caused you. If you have any questions about this matter, please contact me at (703) 308-3164.

Sincerely,

*D. Dotson*  
Deborah Dotson  
Initial Review Division

EXHIBIT I

Transmittal Letter

TOWNSEND and TOWNSEND and  
Steuart Street Tower  
One Market Plaza  
San Francisco, CA 94105  
(415) 326-2400



Atty. Docket No. 16176-1-1

Date December 29, 1995

In re application of: Gerald J. Banks

Serial No.: 08/410,200

Filed: March 6, 1995

Group Art Unit: Not assigned

For: ELECTRICALLY ALTERABLE NON-  
VOLATILE MEMORY WITH N-BITS  
PER MEMORY CELL

I hereby certify that this is being deposited with  
the United States Postal Service as first class  
mail in an envelope addressed to: Assistant  
Commissioner for Patents, Washington, D. C.  
20231.

Date: December 29, 1995

Marianne Edgingre

ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

Sir:

Transmitted herewith are the following documents:

- 1) Transmittal Letter (in trip.);
- 2) Communication;
- 3) Postcard.

Please charge Deposit Account No. 20-1430 as follows:

☒ Any additional fees associated with this paper or during the pendency of this application.

2 copies of this sheet are enclosed.

TOWNSEND and TOWNSEND and CREW

Richard T. Ogawa  
Richard T. Ogawa  
Reg. No.: 37,692  
Attorneys for Applicant

rf0\work\16176\1-1-comm.fm





I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:  
Assistant Commissioner for Patents,  
Attn: Box Missing Parts, Washington, D.C. 20231,  
on

September 6, 1996  
TOWNSEND and TOWNSEND and CREW

By Reine Elzinga

PATENT

Attorney Docket No. 16176-000110

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Gerald J. Banks

Serial No.: 08/410,200

Filed: February 27, 1995

For: ELECTRICALLY ALTERABLE  
NON-VOLATILE MEMORY WITH  
N-BITS PER MEMORY CELL

Examiner: Unassigned

Art Unit: Unassigned

TRANSMITTAL LETTER - RESPONSE  
TO NOTICE OF MISSING PARTS

Attn: Box Missing Parts  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts of Application - Filing Date  
Granted dated July 8, 1995, enclosed are the following to be made of record in the above-  
identified application:

- 1) Petition to Extend Time;
- 2) Executed Declaration and Power of Attorney;
- 3) Verified Statement Claiming Small Entity Status;
- 4) Copy of Notice of Missing Parts;
- 5) Postcard.

Please charge Deposit Account No. 20-1430 for the following fees:

(a) Filing Fee (§ 1.16(a))(Small Entity) \$375.00

(b) Excess Claims Fees (§ 1.16(b), (c)):

23 - 20 = 3 x 11.00 = 33.00

5 - 3 = 2 x 39.00 = 78.00

(c) Missing Parts Surcharge (§1.16(e)) \$ 65.00

**TOTAL FEES TO BE CHARGED \$551.00**

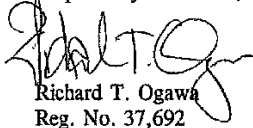
Gerald J. Banks  
Serial No.: 08/410,200  
Page 2

PATENT

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment to Deposit Account No. 20-1430 for this paper and during the prosecution of this application. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,

Date: 9/15/98

  
Richard T. Ogawa  
Reg. No. 37,692

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8th Floor  
San Francisco, California 94111-3834

(415) 326-2400  
Fax (415) 326-2422

RTO:de

rto\work\16176\J-1mp.res

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL** the specification of which        is attached hereto or X was filed on February 27, 1995 as Application Serial No. 08/410,203 and was amended on        (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
			Yes <u>      </u> No <u>      </u>
			Yes <u>      </u> No <u>      </u>

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Date of Filing	Status
08/071,816	June 4, 1993	<u>X</u> Patented <u>      </u> Pending <u>      </u> Abandoned
07/652,878	February 8, 1991	<u>X</u> Patented <u>      </u> Pending <u>      </u> Abandoned

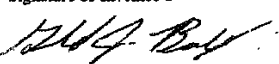
**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

2 Richard T. Ogawa, Reg. No. 37,692  
Gary T. Aka, Reg. No. 29,037

Send Correspondence to:  <u>TOWNSEND and TOWNSEND and CREW LLP</u> <u>Two Embarcadero Center, 8th Floor,</u> <u>San Francisco, CA 94111-3834</u>	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)  Name: <u>Richard T. Ogawa</u> Reg. No. <u>37,692</u> Telephone: <u>(415) 326-2400</u>
--	--

Full Name of Inventor 1	Last Name <b>Banks</b>	First Name <b>Gerald</b>	Middle Name or Initial <b>J.</b>	
Residence & Citizenship	City <b>Fremont</b>	State/Foreign Country <b>California CA</b>	Country of Citizenship <b>U.S.A.</b>	
Post Office Address	Post Office Address <b>200 Pawnee Place</b>	City <b>Fremont</b>	State/Country <b>CA</b>	Zip Code <b>94539</b>
Full Name of Inventor 2	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code
Full Name of Inventor 3	Last Name	First Name	Middle Name or Initial	
Residence & Citizenship	City	State/Foreign Country	Country of Citizenship	
Post Office Address	Post Office Address	City	State/Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  <b>Gerald J. Banks</b>	Signature of Inventor 2	Signature of Inventor 3
Date <b>8/13/96</b>	Date	Date

4  
VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY  
STATUS (37 CFR 1.9(f) and 1.27(b)) - INDEPENDENT INVENTOR

Applicant or Patentee: Gerald J. Banks  
Application or Patent No.: 08/410,200  
Filed or Issued: February 27, 1995  
Title: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office regarding the invention entitled ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL described in:

☐ the specification herewith.  
☒ Application No. 08/410,200, filed February 27, 1995  
☐ Patent No. \_\_\_\_\_, issued \_\_\_\_\_

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is listed below:\*

☐ No such person, concern, or organization  
☐ Persons, concerns or organizations listed below\*

\*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

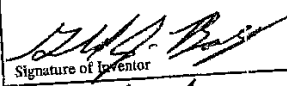
NAME \_\_\_\_\_  
ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME \_\_\_\_\_  
ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME \_\_\_\_\_  
ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF INVENTOR: Gerald J. Banks	NAME OF INVENTOR:	NAME OF INVENTOR:
	Signature of Inventor	Signature of Inventor
Date: <u>8/13/96</u>	Date:	Date:



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
08/410,200	02/27/95	BANK	16176-1-1

08/410,200 02/27/95 BANK 16176-1-1

0232/0418  
TOWNSEND AND TOWNSEND KHOURIE AND CREW  
STEUART STREET TOWER  
ONE MARKET PLAZA  
SAN FRANCISCO 94105

DATE MAILED: 0000

Remained 7/8/96  
02/18/95

### NOTICE TO FILE MISSING PARTS OF APPLICATION FILING DATE GRANTED

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of \$ 130 for large entities or \$ 65 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e).

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is \$ 1,078.

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER**, within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

1. ☐ The statutory basic filing fee is: ☐ missing ☐ insufficient. Applicant as a ☒ large entity ☐ small entity, must submit \$ 730 to complete the basic filing fee.
2. ☒ Additional claim fees of \$ 218 as a ☒ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
3. ☐ The oath or declaration:  
☐ is missing.  
☐ does not cover the newly submitted items.  

An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date is required.
4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
5. ☒ The signature(s) to the oath or declaration is/are: ☒ missing; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration:  

\_\_\_\_\_ An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.
7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of \$ \_\_\_\_\_ under 37 CFR 1.17(k), unless this fee has already been paid.
8. ☐ A \$ \_\_\_\_\_ processing fee is required since your check was returned without payment. (37 CFR 1.21(m)).
9. ☐ Your filing receipt was mailed in error because your check was returned without payment.
10. ☐ The application does not comply with the Sequence Rules. See attached Notice to Comply with Sequence Rules 37 CFR 1.821-1.825.
11. ☐ Other.

Direct the response to Box Missing Part and refer any questions to the Customer Service Center at (703) 308-1202.

**A copy of this notice MUST be returned with the response.**

FORM PTO-1538 (REV. 11-84)

COPY TO BE RETURNED WITH RESPONSE



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER 410200	FILING DATE 02/27/95	FIRST NAMED APPLICANT BANKS	ATTORNEY DOCKET NO. G 16176-1-1
------------------------------	-------------------------	--------------------------------	------------------------------------

TOWNSEND AND TOWNSEND AND CREW  
TWO EMBARCADERO CENTER  
8TH FLOOR  
SAN FRANCISCO CA 94111-3834

EXAMINER FEARS, T	
ART UNIT 2511	PAPER NUMBER 5
DATE MAILED: 12/17/96	

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

### OFFICE ACTION SUMMARY

- ☐ Responsive to communication(s) filed on \_\_\_\_\_
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.
- A shortened statutory period for response to this action is set to expire \_\_\_\_\_ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

#### Disposition of Claims

- ☒ Claim(s) 1-23 is/are pending in the application.
- Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- ☒ Claim(s) 1-4, 11, 12, 14 & 21-23 is/are rejected.
- ☒ Claim(s) 5-10, 13, & 15-20 is/are objected to.
- ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

#### Application Papers

- ☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☒ The drawing(s) filed on 2-27-95 is/are objected to by the Examiner.
- ☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. § 119

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Serial Code/Serial Number) \_\_\_\_\_
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

- ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e):

#### Attachment(s)

- ☐ Notice of Reference Cited, PTO-892
- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s) \_\_\_\_\_
- ☐ Interview Summary, PTO-413
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Notice of Informal Patent Application, PTO-152

- SEE OFFICE ACTION ON THE FOLLOWING PAGES -

\* U.S. GPO: 1986-410-235/40060

Note the drafting criticism.

Claim 22 is rejected as being non-statutory, 35 USC 112. No structure is recited, "cells" and "defining" are readable ~~and~~ mental concepts.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 11, 12, 14 and 21-23 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Suzuki et al.

These claims are drawn to a basic multi-level memory with comparator as shown by Suzuki et al.

Banks is cited as of interest.

Any inquiry concerning this communication should be directed to Terrell Fears at telephone number (703) 308-0956.

Fears/tj

Dec. 12, 1996



TERRELL W. FEARS  
PRIMARY EXAMINER  
GROUP 2500



TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 2-82)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 410200	GROUP/UNIT 2511	ATTACHMENT TO PAPER NUMBER 5	
NOTICE OF REFERENCES CITED				APPLICANT(S) BANKS			
U.S. PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
A	4809224	2-89	Suzuki et al	365	168		
X B	5218569	6-93	BANKS	365	189.01		
C							
D							
E							
F							
G							
H							
I							
J							
K							
FOREIGN PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. PP. DWG. SPEC.
L							
M							
N							
O							
P							
Q							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
R							
S							
T							
U							
EXAMINER <i>fur</i>				DATE 12/96			
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)							

## File History Report

☐ Paper number \_\_\_\_\_ is missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available.

☒ The following page(s) **Draftperson's Patent Drawing Review** of paper number **5** is/are missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available

Additional comments: \_\_\_\_\_



2501

Approved for use through 10/31/99. PTO/SB/10 (10-99)  
OMB 0651-0031  
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE  
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS**  
**(37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN**

Docket Number (Optional)  
181414/US

Applicant or Patentee: G. J. Banks  
Application or Patent No.: 38/410,200  
Filed or Issued: February 27, 1995  
Title: Electrically Alterable Non-Volatile Memory with N-Bits  
Per Memory Cell

I hereby declare that I am

- ☐ the owner of the small business concern identified below;  
☒ an official of the small business concern empowered to act on behalf of the concern identified below.

NAME OF SMALL BUSINESS CONCERN BTG USA INC.

GROUP 2500

ADDRESS OF SMALL BUSINESS CONCERN 2200 Renaissance Boulevard  
Gulph Mills, PA 19406

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 37 CFR 1.21.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

- ☐ the specification filed herewith with title as listed above.  
☒ the application identified above.  
☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:

- ☒ no such person, concern, or organization exists.  
☐ each such person, concern, or organization is listed below.

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Madhuri H. Malkani

TITLE OF PERSON IF OTHER THAN OWNER Senior VP & General Counsel

ADDRESS OF PERSON SIGNING BTG USA INC. 2200 Renaissance Boulevard

SIGNATURE [Signature] DATE 03/03/97

Burden Hour Statement: This form is estimated to take 0.3 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

181414/US

GROUP 25.00

**Burden Hour Statement:** This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.**

RECEIVED  
ALLOWED FILES/CORRESP  
P/PIPI NOV 20 1964

.05/07/87

14:15

2703 528 2457

SHAPIRO

+++ BTG USA INC.

0003/010

*7/Revised by assignee*  
*June*

A-8751514-97

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Filed: February 27, 1995

Group Art Unit: 2511

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

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MAY 09 1997

GROUP 2500

\* \* \*

REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

We, the Assignee of the entire right, title, and interest in and to the above-identified invention and application for Letters Patent, hereby revoke any Powers of Attorney previously granted in this application, and hereby appoint Nelson H. Shapiro, Reg. No. 17,095, Mitchell W. Shapiro, Reg. No. 31,568, and Andrew E. Rawlins, Reg. No. 34,702 of the firm of Shapiro and Shapiro, Reg. No. 18,810, our attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, all correspondence to be addressed to Shapiro and

05/07/97 14:15 703 528 2457

SHAPIRO

BTG USA INC.

004/010

Shapiro, 1100 Wilson Boulevard, Suite 1701, Arlington,  
Virginia 22209.

BTG USA Inc.

Date: 5/8/97

Signature: Bruce G. Bowman  
Name: Bruce G. Bowman  
Title: Vice President / Legal & Patents

05/07/97 14:18 703 528 2457 SHAPIRO +++ BTG USA INC. 005/010

A-8753

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Group Art Unit: 2511

Filed: February 27, 1995

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

\* \* \*

STATEMENT UNDER 37 C.F.R. § 3.73(b)

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MAY 09 1997  
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Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir: -

BTG USA Inc., a corporation duly organized under the laws of Delaware, certifies that it is the Assignee of the entire right, title, and interest in and to the above-identified patent application by virtue of an Assignment from the inventor of said patent application. A copy of said Assignment is attached.

The undersigned has reviewed said Assignment and, to the best of the undersigned's knowledge and belief, title is in said Assignee.

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

The undersigned hereby declares that all statements made herein of the undersigned's own knowledge are true, and

05/07/97 14:18 703 528 2457

SHAPIRO

+++ BTG USA INC.

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that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

BTG USA Inc.

Date: 5/8/97

Signature: Bence G. Beanston

Name: Bence G. Beanston

Title: Vice President / Legal & Patents



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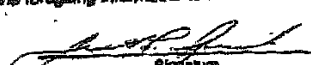
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BTG USA INC.

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FORM PTO-1595 (Rev. 5/92) USPS No. 585 (40011) (net. 4001)		RECORDATION FORM COVER PATENTS ONLY		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	
To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.					
1. Name of conveying party(ies): <b>GERALD J. BANKS</b>  Additional name(s) of conveying party(ies) attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No		2. Name and address of receiving party(ies) Name: <b>BTG USA INC.</b> Internal Address: _____  Street Address: <b>2200 RENAISSANCE BLVD.</b>  City: <b>GULPH MILLS</b> State: <b>PA</b> ZIP: <b>19406</b>  Additional name(s) & address(es) attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No			
3. Nature of conveyance: <input checked="" type="checkbox"/> Assignment <input type="checkbox"/> Merger <input type="checkbox"/> Security Agreement <input type="checkbox"/> Change of Name <input type="checkbox"/> Other _____  Execution Date: <b>February 13, 1997</b>					
4. Application number(s) or patent number(s): If this document is being filed together with a new application, the execution date of the application is: _____ A. Patent Application No.(s) <b>08/410,200</b> <b>08/511,659</b> B. Patent No.(s) <b>5,218,569</b> <b>5,394,362</b> Additional numbers attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No					
5. Name and address of party to whom correspondence concerning document should be mailed: Name: <b>BTG USA INC.</b> Internal Address: <b>PATENT DEPARTMENT</b>  Street Address: <b>2200 RENAISSANCE BLVD.</b>  City: <b>GULPH MILLS</b> State: <b>PA</b> ZIP: <b>19406</b>		6. Total number of applications and patents involved: <b>4</b>  7. Total fee (37 CFR 3.41)..... <b>\$100.00</b> <input type="checkbox"/> Enclosed <input checked="" type="checkbox"/> Authorized to be charged to deposit account  8. Deposit account number: <b>02-3900</b> (Attach duplicate copy of this page if paying by deposit account)			
DO NOT USE THIS SPACE					
9. Statement and signature. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. <b>Joel F. Spivack Reg. 24,179</b> Name of Person Signing  Signature Total number of pages including cover sheet, attachments, and document: <b>2/26/97</b> Date Mail documents to be recorded with required supporting information to: Commissioner of Patents & Trademarks, Box Assignments Washington, D.C. 20231					

APPENDIX A  
"ASSIGNMENT"

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WHEREAS, Gerald J. Banks, an individual having his place of business at 200 Pawnee Place, Fremont, CA 94539, as Assignor, is sole owner of the following inventions:

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL, having United States Patent Number 5,218,569, issued on June 8, 1993; and

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL, having United States Patent Number 5,394,362, issued on February 28, 1995; and

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL, an application for a United States Letter Patent filed on February 27, 1995, having Serial Number 08/410,200; and

ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER MEMORY CELL, an application for a United States Letter Patent filed on August 7, 1995, having Serial Number 08/511,659.

WHEREAS, BTG USA INC., a Corporation of Delaware, whose post office address is Renaissance Business Park, 2200 Renaissance Boulevard, Gulph Mills, PA 19406 as Assignee, is desirous of securing the entire right, title and interest in and to these inventions in all countries throughout the world, and in and to issued United States Letters Patent; and to any applications for United States Letters Patent on these inventions; and to the Letters Patent to be issued upon such applications;

NOW THEREFORE, be it known that for good and valuable consideration, hereby acknowledged to have been received by the Assignor, the Assignor has sold, assigned, transferred, and set over, and does hereby sell, assign, transfer, and set over unto the Assignee, its lawful successors and assigns, the Assignor's entire right, title, and interest in and to these inventions, together with any patent application which has been or may hereafter be filed thereon, and/or issued patent and all divisions, continuations, and continuations-in-part thereof, and all Letters Patent of the United States which may be granted thereon, and all reissues thereof, and all choses in action which may be based thereon, and all rights to claim and contest priority on the basis of any such application, and all applications for Letters Patent which have been or may hereafter be filed for these inventions in any foreign country and all Letters Patent which have been or may hereafter be granted on these inventions in any foreign country, and all extensions, renewals, and reissues thereof; and the Assignor hereby authorizes and requests the Commissioner of Patents of the United States and any official of any foreign country whose duty it is to issue patents on applications as described above, to issue all Letters Patent for these inventions to Assignee, its successors and assigns, and/or to assign already issued Letters Patent to Assignee in accordance with the terms of this Assignment;

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+++ BTG USA INC.

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AND, the Assignor HEREBY covenants that the Assignor has the full right to convey the interest assigned by this Assignment, has not conveyed any interest in the inventions or right to practice the inventions to any third party, and the Assignor has not executed and will not execute any Agreement in conflict with this Assignment;

AND, the Assignor HEREBY further covenants and agrees that the Assignor will, without further consideration, communicate with Assignee, its successors and assigns, any facts known to the Assignor respecting these inventions, and testify in any legal proceeding, sign all lawful papers when called upon to do so, execute and deliver any and all papers that may be necessary or desirable to perfect the title to these inventions in said Assignee, its successors and assigns, execute all divisional, continuation, and reissue applications, make all rightful oaths and generally do everything possible to aid Assignee, its successors, and assigns, to obtain and enforce proper patent protection for these inventions in the United States and any foreign country, it being understood that any expense incident to the execution of such papers shall be borne by the Assignee, its successors and assigns.

IN TESTIMONY WHEREOF, an authorized representative of Assignor and Assignee have each hereunto set their hands this 13 day of February 1997.

By:

  
Gerald J. Banks

By:

  
Anthony V. Lando  
Sr. VP & General Manager

05/07/97 14:17 703 528 2457

SHAPIRO

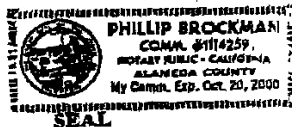
+++ BTG USA INC.

010/010

**ACKNOWLEDGEMENT BY NOTARY PUBLIC:**

State of California County of Alameda ss:

BE IT REMEMBERED, that on February 12, 1997, before me, the subscriber, personally appeared Gerald J. Banks to me known to be the person described in and who executed the foregoing Assignment, and acknowledged that he executed the same as his free act and deed.



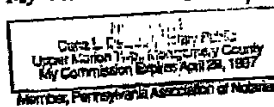
*[Signature]*  
(Notary Public)  
My Commission Expires: October 20, 2000

Commonwealth of Pennsylvania, County of Chester ss:

BE IT REMEMBERED, that on February 4, 1997, before me, the subscriber, personally appeared Anthony V. Lando, who, being by me duly sworn on their oaths, depose and makes proof to my satisfaction, that he is an officer of BTG USA Inc., the corporation named as Assignee in the within Assignment, that he is the Senior Vice President and General Manager, of said corporation; and that said Assignment is hereby signed and delivered by them as and for the voluntary act and deed of said corporation, in the presence of deponent, who thereupon subscribed her name hereto as attesting witness.

*[Signature]*  
(Notary Public)  
My Commission Expires: April 28, 1997

SEAL





UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/410200	02/27/95	BANKS	16176-1-1

TOWNSEND AND TOWNSEND AND CREW  
TWO EMBARCADERO CENTER  
8TH FLOOR  
SAN FRANCISCO CA 94111-3834

EXAMINER
FEARS, TERRELL
ART UNIT
2511

DATE MAILED: 05/14/97

- This is in response to the Power of Attorney filed 05/07/97
- ☐ 1. The Power of Attorney to you in this application **has been revoked** by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.
  - ☒ 2. The Power of Attorney to you in this application **has been revoked** by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).
  - ☐ 3. The withdrawal as attorney in this application **has been accepted**. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

*Desia Johnson*  
This is a communication from the  
Patent and Trademark Office

- ☒ 4. The Power of Attorney in this application **is accepted**. Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.
- ☐ 5. The Power of Attorney in this application **is not accepted** for the reason(s) checked below:
  - ☐ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.
  - ☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
  - ☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
  - ☐ d. The signature of \_\_\_\_\_, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.
  - ☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent & Trademark Office.
  - ☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.

SHAPIRO AND SHAPIRO  
1100 WILSON BLVD., STE. 1701  
ARLINGTON VA 22209

*Desia Johnson*  
This is a communication from the  
Patent and Trademark Office

THIS COPY IN THE APPLICATION FILE COPY A

*Power to Inspect*  
A-8753 #9  
5/14/97  
*PC*

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Group Art Unit: 2511

Filed: February 27, 1995

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

\* \* \*

POWER TO INSPECT AND MAKE COPIES

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Kindly permit Elliott R. Greenwald of Elliott R.  
Greenwald and Associates to inspect and make copies in the  
above noted matter.

Respectfully submitted,

SHAPIRO AND SHAPIRO  
Attorneys for Applicant

By: *AER*  
Andrew E. Rawlins  
Reg. No. 34,702

AER:lmb

1100 Wilson Boulevard  
Suite 1701  
Arlington, Virginia 22209  
Tel: (703) 276-0700

May 9, 1997

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GROUP 2500

*Approved  
Shawn S. Hopper  
5-14-97*



FTO/SB/82 (8-96)

Approved for use through 9/30/99. OMB 0651-0035

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REVOCATION/APPOINTMENT OF POWER OF ATTORNEY OR AUTHORIZATION OF AGENT		Docket Number (Optional) 181414/US
In re Application of G.J. Banks		
Application Number 08/410,200		Filed 02/27/95
Group Art Unit 2511	Examiner T.W. Fears	

To: Assistant Commissioner for Patents  
Washington, DC 20231

1. ☐ I hereby revoke all previous powers of attorney or authorization of agents in the above identified application.

2. ☐ I hereby revoke less than a l previous powers of attorney or authorization of agents in the above application. Revocation applies to the following person(s): (give name(s) and registration number(s))

3. ☒ I/we hereby appoint the following person(s) as my/our attorney(s) or agent(s) to prosecute said application, and to transact all business in the Patent and Trademark Office connected therewith: (give name(s) and registration number(s))  
Andy Rawlins Reg. No. 34,702  
Shapiro & Shapiro  
1100 Wilson Boulevard, Suite 1701  
Arlington, VA 22209


4. ☐ The correspondence address is NOT affected by this communication.

☒ Change the correspondence address and direct all future correspondence to:  
Andy Rawlins  
Shapiro & Shapiro  
1100 Wilson Boulevard, Suite 1701  
Arlington, VA 22209

I am the:

☐ Applicant(s) (signatures of all applicants are required).

☒ Assignee of record of the entire interest.  
Certification under 37 CFR 3.73(b) ☐ is enclosed.  
☒ has already been filed in this application.

 04/01/97  
Signature Date

Address: BTG USA Inc.  
2200 Renaissance Boulevard  
Gulph Mills, PA 19406

Madhuri H. Malkani, Sr. VP &  
Typed or printed name General Counsel

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.



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A-8753  
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PATENT APPLICATION 6/3/97  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Filed: February 27, 1995

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS  
PER CHLL

Group Art Unit: 2511

Examiner: T. Fears

\* \* \*

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion  
as to materiality or prior art effect, the documents listed  
on the attached Form PTO-1449 are hereby cited.

A check for \$230.00 is attached to cover the fee set  
forth in 37 C.F.R. § 1.17(p).

Respectfully submitted,  
SHAPIRO AND SHAPIRO  
Attorneys for Applicant

AER:sjl

1100 Wilson Blvd.  
Suite 1701  
Arlington, VA 22209  
(703) 276-0700

May 15, 1997

By:   
Andrew E. Rawlins  
Reg. No. 34,702  
350 1st St. N.E. 03610200  
1 123 230.00 41



FORM PTO-1449		Atty. Docket No.		Serial No.	
LIST OF DOCUMENTS CITED BY APPLICANT		A-8753		08/410,200	
Applicant Gerald J. BANKS					
Filing Date February 27, 1995				Group 2511	

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date
	AA 4,192,014	03/04/80	Craycraft	365	104	
	AB 4,357,685	11/02/82	Daniele et al.	365	189	
	AC 4,964,079	10/16/90	Devin	365	168	
	AD 5,172,330	12/15/92	Mehrotra et al.	365	185	
	AE 5,262,984	11/16/93	Noguchi et al.	365	185	
	AF 3,801,965	04/02/74	Keller et al.	340	173R	
	AG 4,004,159	01/18/77	Rai et al.	307	238	
	AH 4,054,864	10/18/77	Audaire et al.	340	173R	
	AI 4,090,258	05/16/78	Cricchi	365	184	
	AJ 4,122,541	10/24/78	Uchida	365	154	
	AK 4,139,910	02/13/79	Anantha et al.	365	183	

Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation
	AL WO82/02276	07/08/82	WIPO			
	AM WO82/02976	09/02/82	WIPO			
	AN WO90/01984	03/08/90	WIPO			
	AO 2,630 574	10/27/89	France			Abstract
	AP 0 390 404	10/03/90	Europe			
	AQ					

AR	M. Bauer et al., A Multilevel-Cell 32Mb Flash Memory, 1995 IEEE International Solid-State Circuits Conference, Session 7, Paper TA7.7.
AS	John A. Bayliss et al., The Interface Processor for the 32b Computer, 1981 IEEE International Solid-State Circuits Conference, February 1981, at 116-117.

Examiner	Date Considered
<i>[Signature]</i>	9-97

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449				Atty. Docket No. A-8753		Serial No. 08/410,200	
LIST OF DOCUMENTS CITED BY APPLICANT				Applicant Gerald J. BANKS			
				Filing Date February 27, 1995		Group 2511	
Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date	
	AA*	4,149,270	04/10/79 Cricchi et al.	365	222		
	AB*	4,181,980	01/01/80 McCoy	365	45		
	AC*	4,272,830	06/09/81 Moench	365	45		
	AD*	4,287,570	09/01/81 Stark	365	104		
	AE*	4,300,210	11/10/81 Chakravarti et al.	365	45		
	AF*	4,306,300	12/15/81 Terman et al.	365	45		
	AG*	4,327,424	04/27/82 Wu	365	104		
	AH*	4,388,702	06/14/83 Sheppard	365	104		
	AI*	4,415,992	11/15/83 Adlhoeh	365	94		
	AJ*	4,449,203	05/15/84 Adlhoeh	365	104		
	AK*	4,462,088	07/24/84 Giuliani et al.	365	105		
Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation	
	AL*						
	AM*						
	AN*						
	AO*						
	AP*						
	AQ*						
	AR*	Christoph Bleiker & Hans Melchior, A Four-State EEPROM Using Floating-Gate Memory Cells, IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987, at 260-263.					
	AS*	Raymond A. Heald & David A. Hodges, Multilevel Random-Access Memory Using One Transistor Per Cell, IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 4, August 1976, at 519-528.					
Examiner <i>[Signature]</i>				Date Considered 9-17			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

<b>FORM PTO-1449</b> <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>				Atty. Docket No. A-8753		Serial No. 08/410,200	
Applicant Gerald J. BANKS							
Filing Date February 27, 1995						Group 2511	



  

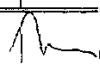
Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date
	AA^ 4,495,602	01/22/85	Sheppard	365	104	
	AB^ 4,503,518	03/05/85	Iwahashi	365	104	
	AC^ 4,558,241	12/10/85	Suzuki et al.	307	530	
	AD^ 4,578,777	03/25/86	Fang et al.	365	184	
	AE^ 4,586,163	04/29/86	Koike	365	104	
	AF^ 4,627,027	12/02/86	Rai et al.	365	45	
	AG^ 4,653,023	03/24/87	Suzuki et al.	365	104	
	AH^ 4,661,929	04/28/87	Aoki et al.	365	189	
	AI^ 4,709,350	11/24/87	Nakagome et al.	365	45	
	AJ^ 4,733,394	03/22/88	Giebel	371	21	
	AK^ 4,771,404	09/13/88	Mano et al.	365	189	

Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation
AL^						
AM^						
AN^						
AO^						
AP^						
AQ^						

	AR^	David A. Rich, A Survey of Multivalued Memories, IEEE Transactions on Computers, Vol. C-35, No. 2, February 1986, at 99-106.
	AS^	R.S. Withers et al., Nonvolatile Analog Memory in MNOS Capacitors, IEEE Electron Device Letters, Vol. EDL-1, No. 3, March 1980, at 42-45.

Examiner 	Date Considered 9-9
---	------------------------

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449				Atty. Docket No. A-8753		Serial No. 08/410,200	
LIST OF DOCUMENTS CITED BY APPLICANT				Applicant Gerald J. BANKS			
				Filing Date February 27, 1995		Group 2511	
Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date	
	AA# 4,799,195	01/17/89	Iwahashi et al.	365	185		
	AB# 4,847,808	07/11/89	Kobatake	364	104		
	AC# 4,853,892	08/01/89	Hori	365	49		
	AD# 4,890,259	12/26/89	Simko	365	45		
	AE# 4,914,631	04/03/90	Johnson et al.	365	189.11		
	AF# 4,989,179	01/29/91	Simko	365	45		
	AG# 5,021,999	06/04/91	Kohda et al.	365	168		
	AH# 5,043,940	08/27/91	Harari	365	168		
	AI# 5,095,344	03/10/92	Harari	357	23.5		
	AJ# 5,163,021	11/10/92	Mehrotra et al.	365	185		
	AK# 5,258,958	11/02/93	Iwahashi et al.	365	210		
Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation	
	AL#						
	AM#						
	AN#						
	AO#						
	AP#						
	AQ#						
	AR#						
	AS#						
	AT#						
Examiner <i>[Signature]</i>				Date Considered <i>7-87</i>			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

<b>FORM PTO-1449</b> <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>				Atty. Docket No. A-8753		Serial No. 08/410,200	
				Applicant Gerald J. BANKS			
				Filing Date February 27, 1995		Group 2511	

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date
AA'	5,268,870	12/07/93	Harari	365	218	
AB'	5,293,560	03/08/94	Harari	365	185	
AC'	5,321,655	06/14/94	Iwahashi et al.	365	200	
AD'	5,351,210	09/27/94	Saito	365	189.01	
AE'	5,422,845	06/06/95	Ong	365	185	
AF'	5,432,735	07/11/95	Parks et al.	365	168	
AG'	5,434,825	07/18/95	Harari	365	185	
AH'	5,440,505	08/08/95	Fazio et al.	365	45	
AI'	5,444,656	08/22/95	Bauer et al.	365	189.01	
AJ'	5,450,363	09/12/95	Christopherson et al.	365	205	
AK'	5,457,650	10/10/95	Sugiura et al.	365	184	

Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation
AL'						
AM'						
AN'						
AO'						
AP'						
AQ'						

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AT'	

Examiner 	Date Considered 9-17
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<b>FORM PTO-1449</b>  <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>				Atty. Docket No. A-8753		Serial No. 08/410,200	
				Applicant Gerald J. BANKS			
				Filing Date February 27, 1995		Group 2511	

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date
AA~	5,469,384	11/21/95	Lacey	365	185.13	
AB~	5,475,693	12/12/95	Christopherson et al.	371	10.2	
AC~	5,485,422	01/16/96	Bauer et al.	365	168	
AD~	5,497,119	03/05/96	Tedrow et al.	327	540	
AE~	5,506,813	04/09/96	Mochizuki et al.	365	230.03	
AF~	5,508,958	04/16/96	Fazio et al.	365	185.19	
AG~	5,515,317	05/07/96	Wells et al.	395	427	
AH~	5,523,972	06/04/96	Rashid et al.	365	185.22	
AI~	5,539,690	07/23/96	Talreja et al.	365	185.22	
AJ~	5,541,896	07/30/96	Hasbun	365	230.01	
AK~	5,544,118	08/06/96	Harari	365	218	

Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation
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AP~						
AQ~						

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AS~	
AT~	

Examiner 	Date Considered 9-97
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FORM PTO-1449				Atty. Docket No. A-8753		Serial No. 08/410,200	
LIST OF DOCUMENTS CITED BY APPLICANT				Applicant Gerald J. BANKS			
				Filing Date February 27, 1995		Group 2511	
Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date	
AA	5,550,772	08/27/96	Gill	365	185.03		
AB	5,568,439	10/22/96	Harari	365	218		
AC	5,583,812	12/10/96	Harari	365	185.33		
AD	5,594,691	01/14/97	Bashir	365	189.09		
AE	5,596,527	01/21/97	Tomloka et al.	365	185.20		
AF	3,660,819	05/02/72	Frohman-Bentchkowsky	317	235R		
AG	5,295,255	03/15/94	Malecek et al.	395	425		
AH							
AI							
AJ							
AK							
Examiner Initial	Document Number	Date	Country	Class	Sub-class	Translation	
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AN							
AO							
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AQ							
AR							
AS							
AT							
Examiner			Date Considered				
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							



11/4/97  
A-8753  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Group Art Unit: 2511

Filed: February 27, 1995

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

LETTER PROPOSING DRAWING CHANGES

*OK For Entry*  
Assistant Commissioner for Patents  
Washington, D.C. 20231

ATTENTION: Official Draftsman

Sir:

Attached are prints of Figs. 2, 6-8, and 15-20 showing  
proposed changes in red. Upon receipt of the approval of  
the Examiner and a Notice of Allowance, the changes will be  
made formally.

Respectfully submitted,  
SHAPIRO AND SHAPIRO  
Attorneys for Applicant

MWS:JTW:lmb  
1100 Wilson Blvd.  
Suite 1701  
Arlington, VA 22209  
Tel: (703) 276-0700

By: *Mitchell W. Shapiro*  
Mitchell W. Shapiro  
Reg. No. 31,568

June 17, 1997

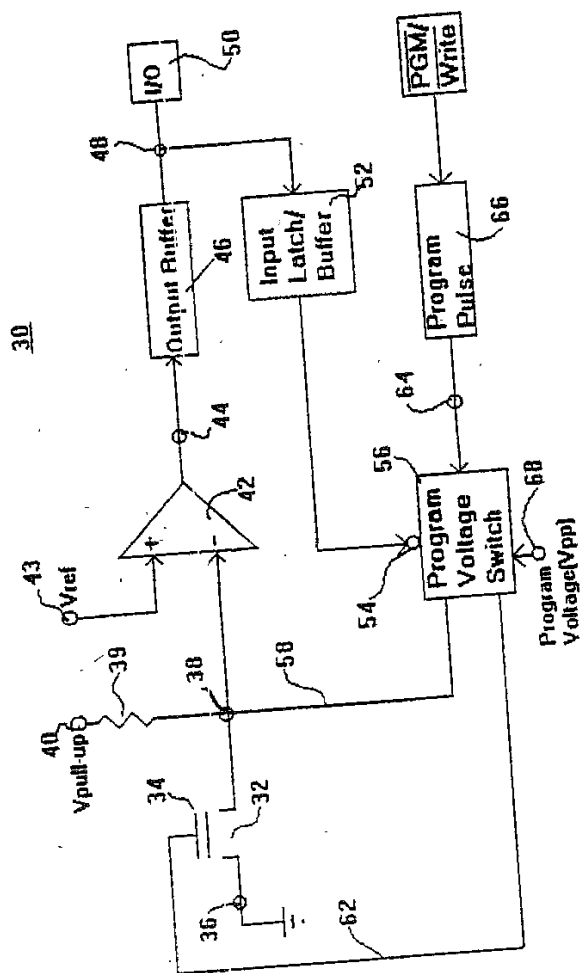
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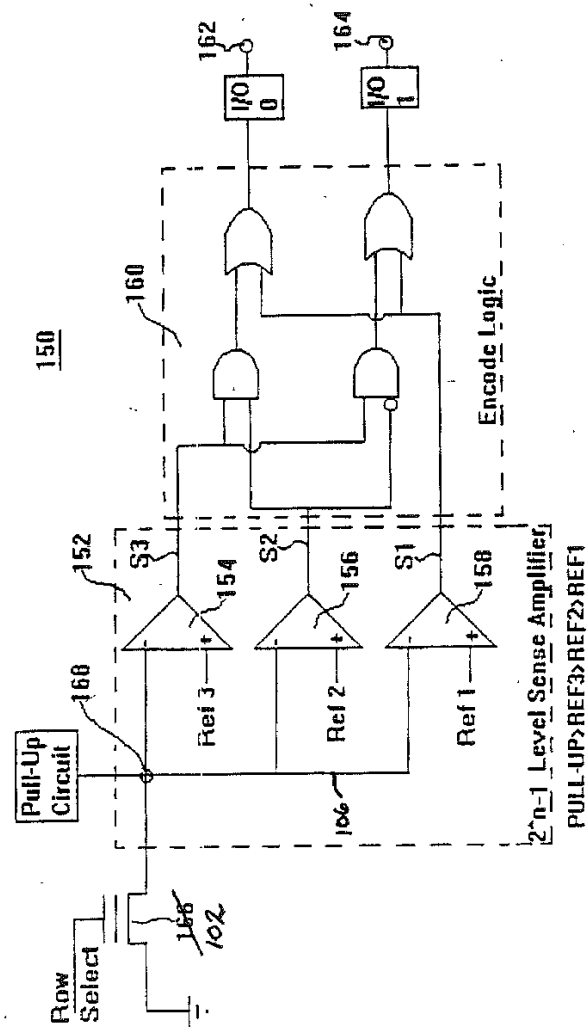
*Mitchell W. Shapiro*  
Mitchell W. Shapiro

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GROUP 2511





Prior Art  
Figure 2



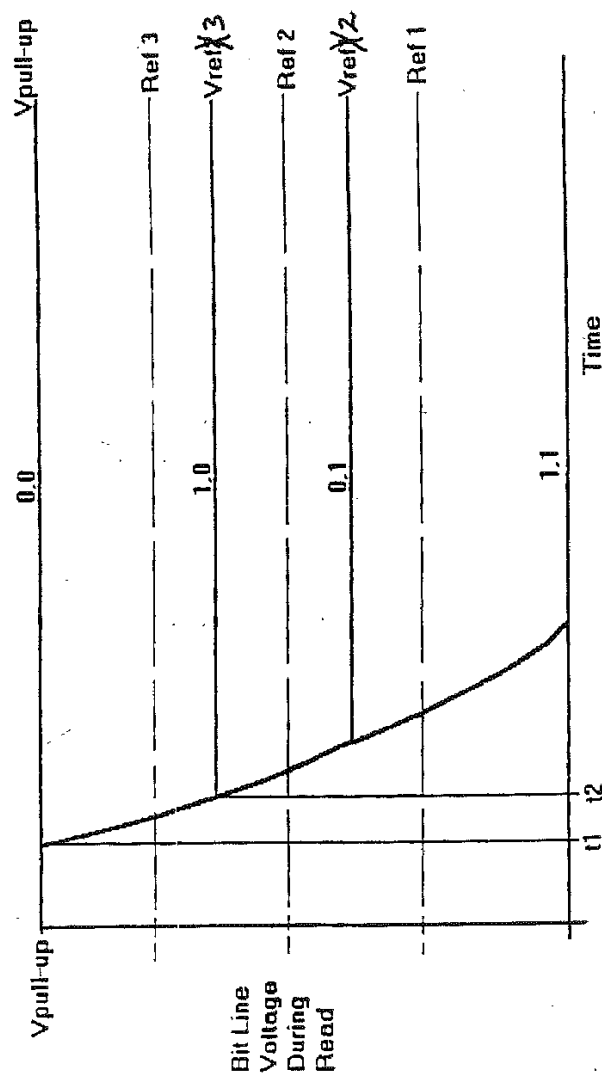


Figure 7

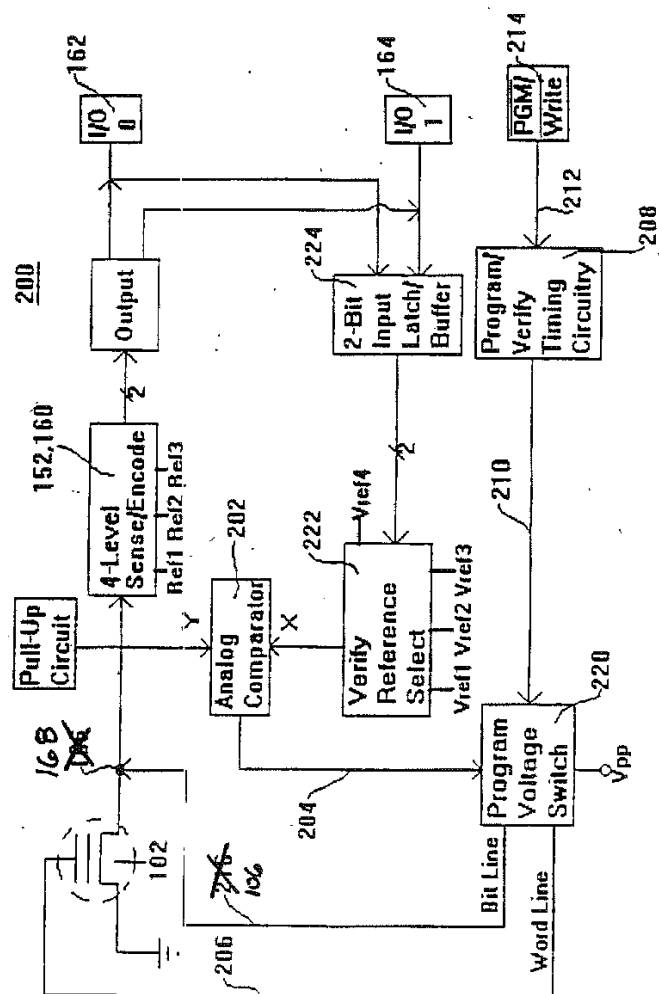
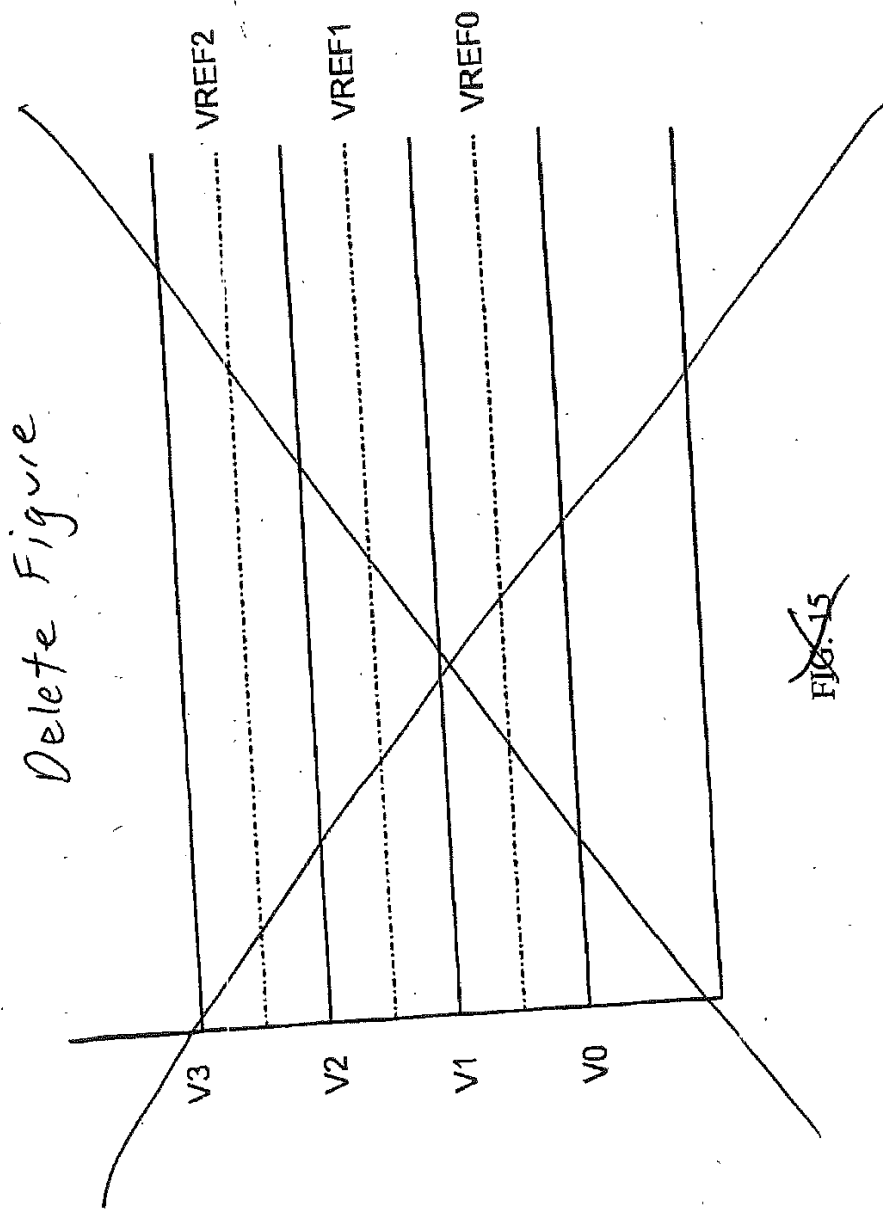
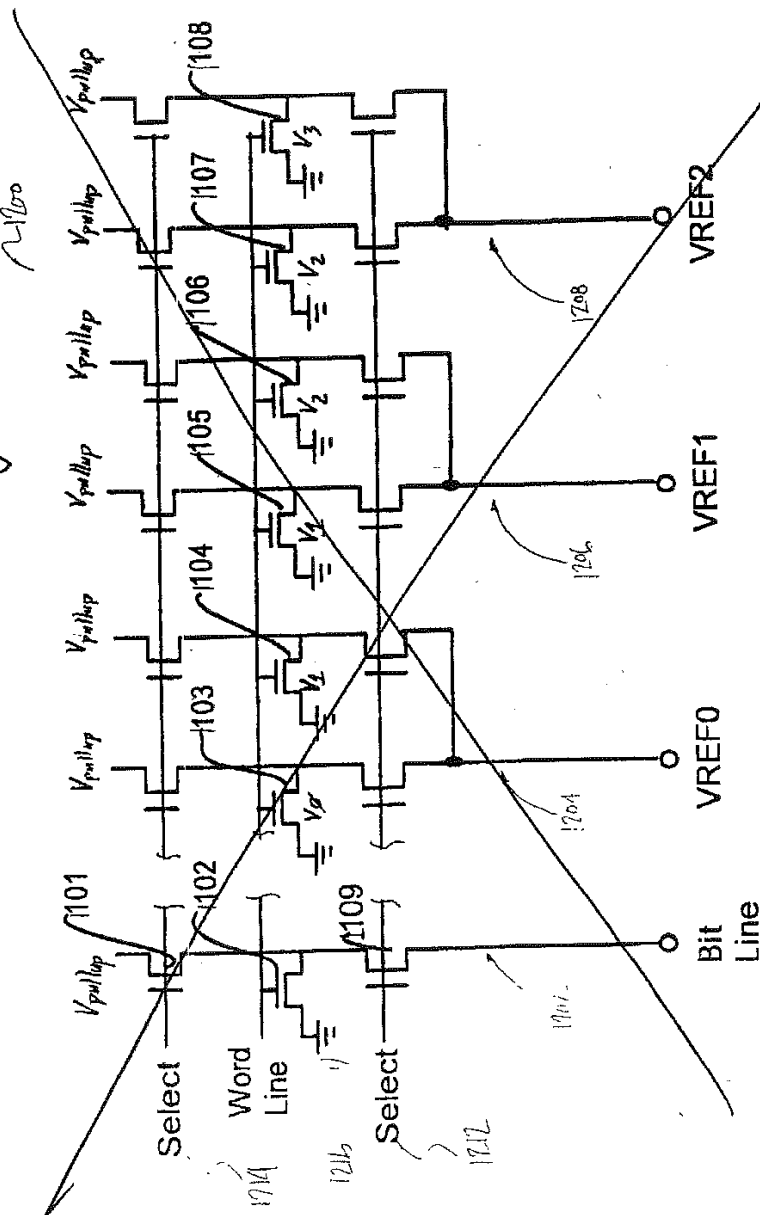


Figure 8



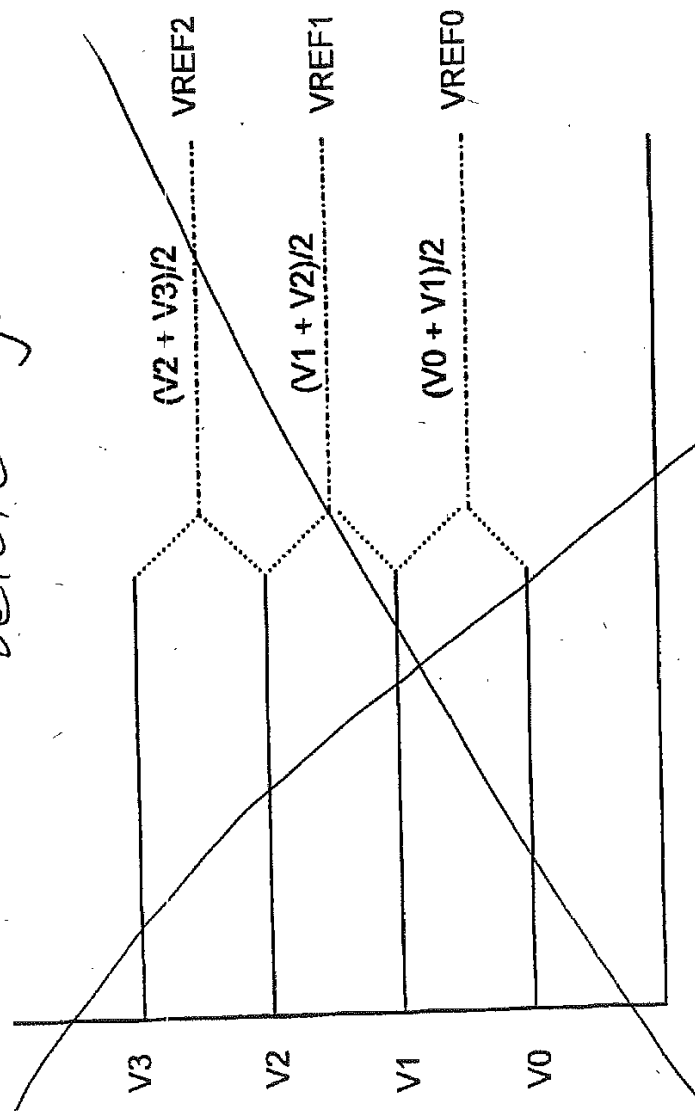
~~FIG. 15~~

Delete Figure



~~FIG. 16~~

Delete Figure



~~FIG. 17~~

Delete Figure

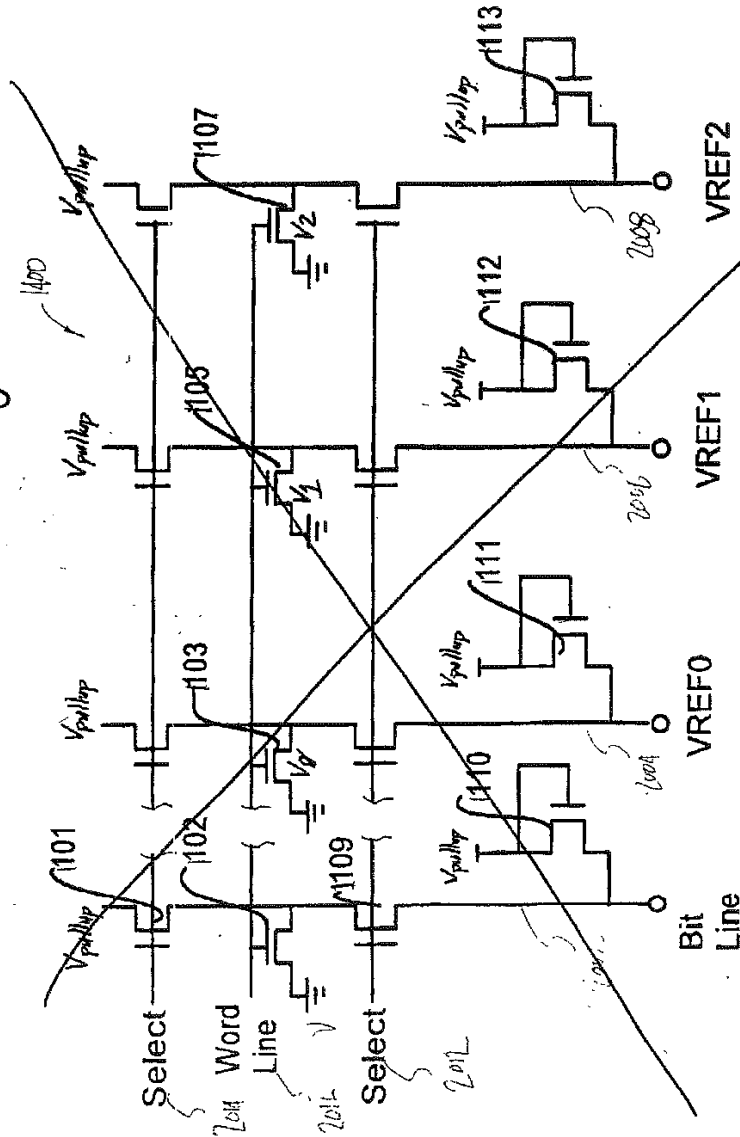
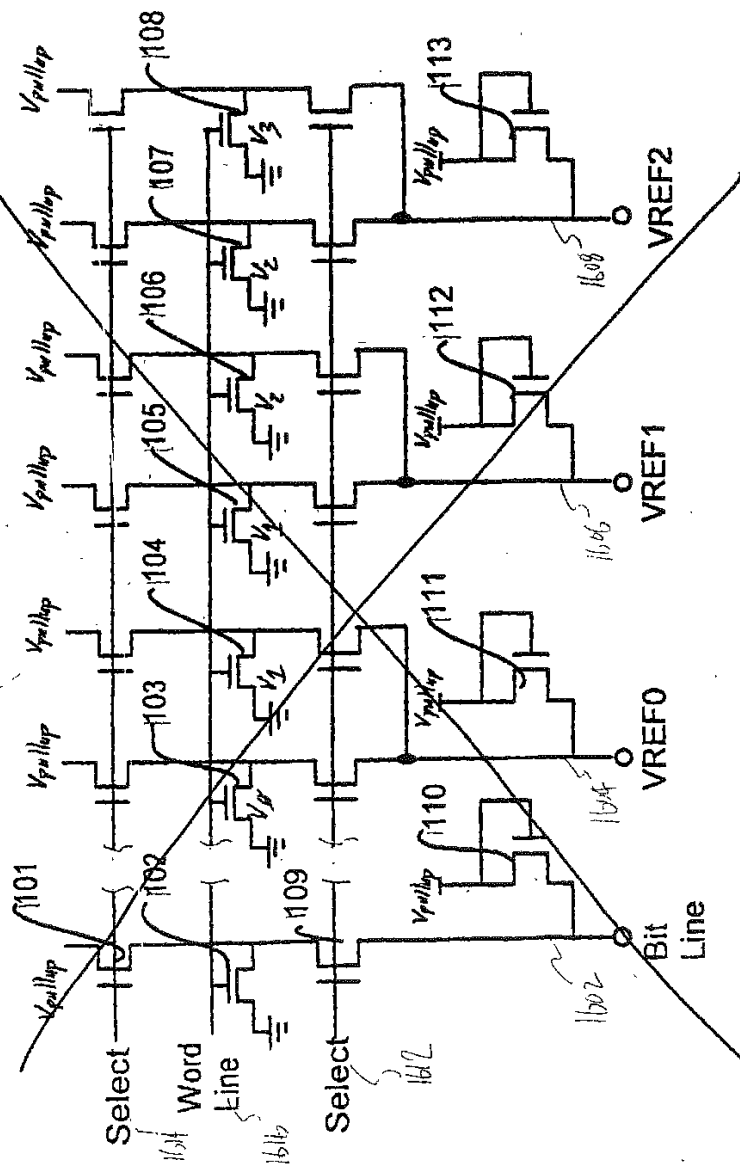


FIG. 18



Delete Figure



~~FIG. 19~~

Delete Figure

The diagram illustrates a Voltage Reference Array (FIG. 2D) used in a memory device. It features a grid of transistors arranged in four word lines (Word Line 0, Word Line 1, Word Line 2, Word Line 3) and four bit lines (Select, Representative Memory Bit Line, and two unlabeled bit lines). Each word line is connected to a series of transistors (V0, V1, V2, V3) in a specific sequence. The Select line is connected to the gates of the transistors in the first column. The Representative Memory Bit Line is connected to the gates of the transistors in the second column. The other two bit lines are connected to the gates of the transistors in the third and fourth columns. The transistors are labeled V0, V1, V2, and V3, with their gates connected to the word lines. The gates of the transistors in the first column are connected to the Select line. The gates of the transistors in the second column are connected to the Representative Memory Bit Line. The gates of the transistors in the third and fourth columns are connected to the word lines. The drains of the transistors in the first column are connected to the Select line. The drains of the transistors in the second column are connected to the Representative Memory Bit Line. The drains of the transistors in the third and fourth columns are connected to the word lines. The gates of the transistors in the first column are connected to the Select line. The gates of the transistors in the second column are connected to the Representative Memory Bit Line. The gates of the transistors in the third and fourth columns are connected to the word lines. The drains of the transistors in the first column are connected to the Select line. The drains of the transistors in the second column are connected to the Representative Memory Bit Line. The drains of the transistors in the third and fourth columns are connected to the word lines. The gates of the transistors in the first column are connected to the Select line. The gates of the transistors in the second column are connected to the Representative Memory Bit Line. The gates of the transistors in the third and fourth columns are connected to the word lines. The drains of the transistors in the first column are connected to the Select line. The drains of the transistors in the second column are connected to the Representative Memory Bit Line. The drains of the transistors in the third and fourth columns are connected to the word lines.

FIG. 2D

~~FIG 20~~



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AP 257

A-8753  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Filed: February 27, 1995

Group Art Unit: 2511

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

PETITION FOR EXTENSION OF TIME

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

It is respectfully requested that the time now set for response be extended, retroactively, by three months. The required petition fee for a small entity is submitted herewith. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper to Deposit Account No. 19-1510.

Respectfully submitted,

SHAPIRO AND SHAPIRO  
Attorneys for Applicant

By: Mitchell W. Shapiro  
Mitchell W. Shapiro  
Reg. No. 31,568

MWS:lmb

1100 Wilson Blvd.  
Suite 1701  
Arlington, Virginia 22209  
Tel: (703) 276-0700

June 17, 1997

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Mitchell W. Shapiro  
Mitchell W. Shapiro

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A-8753  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Serial No.: 08/410,200

Group Art Unit: 2511

Filed: February 27, 1995

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH  
N-BITS PER CELL

B/A  
7/17/97  
W.

\* \* \*

AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 17,  
1996, please amend this application as indicated below.

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GROUP 2500

IN THE DRAWINGS:

Please delete Figs. 15-20.

IN THE SPECIFICATION:

Page 1:

line 5, change "continuation-in-part" to  
--division--;  
line 15, change "providing" to --programming and/or  
verifying programming of-- and change "device" to  
--device.--;  
line 16, delete the line in its entirety.

A'

20

08 00 74  
0 250 00  
07/14/1997 08:19:00  
02 FC 2503

Page 2:

line 28, delete "A limitation with the";  
lines 29-33, delete the lines in their entirety.

Page 4:

line 8, change "states" (first occurrence) to  
--states.-- and delete the remainder of the line.  
lines 9-11, delete the lines in their entirety.

Page 5:

lines 12-37, delete the lines in their entirety.

Page 6:

lines 1-2, delete the lines in their entirety;  
lines 30-33, delete the lines in their entirety.

Page 7:

after line 3, insert the following paragraph:

--Fig. 10 is a timing diagram which illustrates the  
voltage threshold of a 2-bit per cell EANVM being erased  
from a fully programmed (0,0) state to one of the other  
three possible states.--;

lines 16-34, delete the lines in their entirety.

Page 8:

line 22, delete "conventional";  
line 23, delete "conventional".

Page 9:

line 4, change "a-control" to --a control--.

Page 12:

line 11, change "0" to --"1"--;

line 17, after "in" insert --connection with--.

Page 13:

line 7, after "in" insert --connection with--;

line 12, change "4" to --3--;

line 14, change "106" to --168--.

Page 14:

line 8, delete "in voltage";

line 9, change "106" to --168--;

line 12, delete "in voltage";

line 13, change "106" to --168--;

line 17, change "106" to --168--;

line 20, change ".During" to --. During--;

line 22, delete "25";

line 25, delete "22";

line 33, change "Vref2" to --Vref3--;

line 37, change "Vref1" to --Vref2-- and delete

"for";

line 38, delete "the other specific conductivity levels".

Page 15:

line 2, delete "20";  
line 3, delete "it is intended that";  
line 13, delete the semicolon ";";  
line 14, change "106" to --168--;  
line 15, change "4" to --3--;  
line 18, change "I 1/0" to --1 I/O--;  
line 21, change "the" to --an--;  
line 26, change "5202" to --202--;  
line 37, change "106" to ---168---

Page 16:

line 5, change "206" to --106 constitutes the bit

A3 line and";

line 7, change "106" to --168-- and change "the"  
to --a--;

line 8, after "on" insert --a--;

line 20, change "Program Voltage Switch" to

--program voltage switch--;

line 23, change "106" to --168--;

line 34, after "224" insert (n = 2 in the

A4 illustrative form)--;

line 36, change "106" to --168-- and change "4" to

--3--.

Page 17:

line 3, change "4" to --3--.

line 22, change "illustrated by" to --will be appreciated from--.

Page 18:

line 34, change "216" to --106--.

Page 19:

line 5, change "106" to --168--;

line 7, change "222" to --202--;

line 18, change "Although" to --More generally--.

Page 20:

line 27, change "vref3" to --Vref3--;

line 30, change "duration" to --durations--.

Page 21:

line 13, after "160" insert AS --, which represents the current contents of the EANVM cell 102,--;

line 14, delete "current contents of the EANVM cell 102";

lines 20-37, delete the lines in their entirety.

Pages 22-27:

Delete the pages in their entirety.

29



Page 28:

lines 1-36, delete the lines in their entirety.

IN THE ABSTRACT OF THE DISCLOSURE:

Please substitute the abstract on the appended separate sheet for the original abstract.

IN THE CLAIMS:

Please cancel Claims 2-23 without prejudice.

- 1 1. (Amended) A multi-level memory device comprising:  
2 [a] an electrically alterable non-volatile multi-level  
3 memory cell [means] for storing input information in a  
4 corresponding one of [for an indefinite period of time as a  
5 discrete state of said multi-level cell means, said memory  
6 cell means storing information in] K<sup>n</sup> predetermined memory  
7 states of said multi-level memory cell, where K is a base of  
8 a predetermined number system, [and] n is a number of bits  
9 stored per cell, [wherein] and K<sup>n</sup> > 2;  
10 memory cell programming means for programming said multi-  
11 level memory cell [means to a memory state corresponding to]  
12 in accordance with said input information;  
13 reference voltage selecting means for selecting one of a  
14 plurality of reference voltages in accordance with said  
15 input information, each of said reference voltages  
16 corresponding to a different one of said predetermined  
17 memory states; and

18 comparator means for comparing [said memory state] a  
19 voltage of said multi-level memory cell with the selected  
20 reference voltage [means with said input information, said  
21 input information corresponding to one of a plurality of  
22 reference voltages], said comparator means further  
23 generating a control signal indicating whether the state of  
24 said multi-level memory cell is the state corresponding  
25 [indicative of said memory state as compared] to said input  
26 information.

Please add the following claims:

1 ~~24~~. A device according to Claim 1, wherein each memory  
2 state is bounded by one or more voltage values, and each  
3 reference voltage differs from the voltage value or values  
4 bounding the corresponding memory state.--

1 ~~25~~. Multi-level memory apparatus, comprising  
2 an electrically alterable non-volatile memory cell having  
3 more than two predetermined memory states;  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating  
6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell; and  
9 a comparator which compares a signal corresponding to the  
10 state of said memory cell with the selected reference signal

11 to verify whether said memory cell is programmed to the  
12 state indicated by said information.--

1 <sup>4</sup>  
--26. Apparatus according to Claim <sup>3</sup>25, wherein said  
2 comparator compares a bit line signal of said memory cell  
3 with the selected reference signal.--

1 <sup>5</sup>  
--27. Apparatus according to Claim <sup>3</sup>25, wherein said  
2 comparator compares a bit line voltage of said memory cell  
3 with a voltage of the selected reference signal.--

148 1 <sup>6</sup>  
--28. Multi-level memory apparatus, comprising:  
2 an electrically alterable non-volatile memory cell having  
3 more than two predetermined memory states;  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating  
6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell; and  
9 a verifying device which detects a parameter indicating  
10 the state of said memory cell and verifies whether said  
11 memory cell is programmed to the state indicated by said  
12 information based on the detected parameter and the selected  
13 reference signal.--

1       <sup>7</sup>  
--~~25~~. Apparatus according to Claim <sup>6</sup> ~~25~~, wherein said  
2       verifying device detects said parameter at a bit line  
3       terminal of said memory cell.--

1       <sup>8</sup>  
--~~30~~. Apparatus according to Claim <sup>6</sup> ~~30~~, wherein said  
2       parameter is a bit line voltage of said memory cell.--

1       <sup>9</sup>  
--~~31~~. Multi-level memory apparatus, comprising:  
2       an electrically alterable non-volatile memory cell having  
3       more than two predetermined memory states;  
4       a selecting device which selects one of a plurality of  
5       predetermined reference signals in accordance with  
6       information indicating a memory state to which said memory  
7       cell is to be programmed, each reference signal  
8       corresponding to a different memory state of said memory  
9       cell;  
10      a programming signal source which applies a programming  
11      signal to said memory cell; and  
12      a comparator which compares a signal corresponding to the  
13      state of said memory cell with the selected reference signal,  
14      to verify whether said memory cell is programmed to the  
15      state indicated by said information.--

AS

1       <sup>10</sup>  
--~~32~~. Apparatus according to Claim <sup>9</sup> ~~32~~, wherein said  
2       comparator compares a bit line signal of said memory cell  
3       with the selected reference signal.--

1           <sup>11</sup>  
--~~33~~<sup>9</sup>. Apparatus according to Claim ~~31~~<sup>9</sup>, wherein said  
2   comparator compares a bit line voltage of said memory cell  
3   with a voltage of the selected reference signal.--

1           <sup>12</sup>  
--~~34~~<sup>12</sup>. Multi-level memory apparatus, comprising:  
2   an electrically alterable non-volatile memory cell having  
3   more than two predetermined memory states;  
4   a selecting device which selects one of a plurality of  
5   reference signals in accordance with information indicating  
6   a memory state to which said memory cell is to be  
7   programmed, each reference signal corresponding to a  
8   different memory state of said memory cell;  
9   a programming signal source which applies a programming  
10   signal to said memory cell; and  
11   a verifying device which detects a parameter indicating  
12   the state of said memory cell and which verifies whether  
13   said memory cell is programmed to the state indicated by  
14   said information based on the detected parameter and the  
15   selected reference signal.--

1           <sup>13</sup>  
--~~35~~<sup>12</sup>. Apparatus according to Claim ~~34~~<sup>12</sup>, wherein said  
2   verifying device detects said parameter at a bit line  
3   terminal of said memory cell.--

1           <sup>14</sup>  
--~~36~~<sup>12</sup>. Apparatus according to Claim ~~34~~<sup>12</sup>, wherein said  
2   parameter is a bit line voltage of said memory cell.--

15  
1     ~~37~~. Multi-level memory apparatus, comprising:  
2     an electrically alterable non-volatile memory cell having  
3     more than two predetermined memory states;  
4     a selecting device which selects one of a plurality of  
5     reference signals in accordance with information indicating  
6     a memory state to which said memory cell is to be  
7     programmed, each reference signal corresponding to a  
8     different memory state of said memory cell;  
9     a programming signal source which applies a programming  
10    signal to said memory cell; and  
11    a control device which controls the application of said  
12    programming signal to said memory cell based on the selected  
13    reference signal.--

16  
1     ~~38~~. Apparatus according to Claim <sup>15</sup>37, wherein said  
2     control device detects a parameter indicating the state of  
3     said memory cell, verifies whether said memory cell is  
4     programmed to the state indicated by said information based  
5     on the detected parameter and the selected reference signal,  
6     and controls the application of said programming signal to  
7     said memory cell based on a result of the verification.--

17  
1     ~~39~~. Apparatus according to Claim <sup>15</sup>37, wherein said  
2     control device compares a signal corresponding to the state  
3     of said memory cell with the selected reference signal and  
4     controls the application of said programming signal to said  
5     memory cell based on a result of the comparison.--

18  
1 --40. Apparatus for verifying programming of an  
2 electrically alterable non-volatile memory cell having more  
3 than two predetermined memory states, comprising:  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating  
6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell; and  
9 a comparator to compare a signal corresponding to the  
10 state of said memory cell with the selected reference signal  
11 to verify whether said memory cell is programmed to the  
12 state indicated by said information.--

19 18  
1 --41. Apparatus according to Claim 40, wherein the  
2 signal corresponding to the state of said memory cell is a  
3 bit line signal of said memory cell.--

20 18  
1 --42. Apparatus according to Claim 40, wherein the  
2 signal corresponding to the state of said memory cell is a  
3 bit line voltage of said memory cell.--

21  
1 --43. Apparatus for verifying programming of an  
2 electrically alterable non-volatile memory cell having more  
3 than two predetermined memory states, comprising:  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating

6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell; and  
9 a verifying device to detect a parameter indicating the  
10 state of said memory cell and to verify whether said memory  
11 cell is programmed to the state indicated by said  
12 information based on the detected parameter and the selected  
13 reference signal.--

1 <sup>22</sup>  
--<sup>44</sup>. Apparatus according to Claim <sup>21</sup>~~43~~, wherein said  
2 parameter is a bit line signal parameter of said memory  
3 cell.--

1 <sup>23</sup>  
--<sup>45</sup>. Apparatus according to Claim <sup>21</sup>~~43~~, wherein said  
2 parameter is a bit line voltage of said memory cell.--

1 <sup>24</sup>  
--<sup>46</sup>. Apparatus for programming an electrically  
2 alterable non-volatile memory cell having more than two  
3 predetermined memory states, comprising:  
4 a selecting device which selects one of a plurality of  
5 predetermined reference signals in accordance with  
6 information indicating a memory state to which said memory  
7 cell is to be programmed, each reference signal  
8 corresponding to a different memory state of said memory  
9 cell;  
10 a programming signal source to apply a programming signal  
11 to said memory cell; and



12 a comparator to compare a signal corresponding to the  
13 state of said memory cell with the selected reference signal  
14 to verify whether said memory cell is programmed to the  
15 state indicated by said information.---

1 <sup>25</sup>  
--~~47~~. Apparatus according to Claim <sup>24</sup>~~46~~, wherein the  
2 signal corresponding to the state of said memory cell is a  
3 bit line signal of said memory cell.---

1 <sup>26</sup>  
--~~48~~. Apparatus according to Claim <sup>24</sup>~~46~~, wherein the  
2 signal corresponding to the state of said memory cell is a  
3 bit line voltage of said memory cell.---

1 <sup>27</sup>  
--~~49~~. Apparatus for programming an electrically  
2 alterable non-volatile memory cell having more than two  
3 predetermined memory states, comprising:  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating  
6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell;  
9 a programming signal source to apply a programming signal  
10 to said memory cell; and  
11 a verifying device to detect a parameter indicating the  
12 state of said memory cell and to verify whether said memory  
13 cell is programmed to the state indicated by said

14 information based on the detected parameter and the selected  
15 reference signal.--

1 <sup>28</sup>  
--~~50~~. Apparatus according to Claim <sup>27</sup>~~45~~, wherein said  
2 parameter is a bit line signal parameter of said memory  
3 cell.--

1 <sup>29</sup>  
--~~51~~. Apparatus according to Claim <sup>27</sup>~~45~~, wherein said  
2 parameter is a bit line voltage of said memory cell.--

1 <sup>30</sup>  
--~~52~~. Apparatus for programming an electrically  
2 alterable non-volatile memory cell having more than two  
3 predetermined memory states, comprising:  
4 a selecting device which selects one of a plurality of  
5 reference signals in accordance with information indicating  
6 a memory state to which said memory cell is to be  
7 programmed, each reference signal corresponding to a  
8 different memory state of said memory cell;  
9 a programming signal source to apply a programming signal  
10 to said memory cell; and  
11 a control device to control the application of said  
12 programming signal to said memory cell based on the selected  
13 reference signal.--

1 <sup>31</sup>  
--~~53~~. Apparatus according to Claim <sup>30</sup>~~52~~, wherein said  
2 control device is constructed to detect a parameter  
3 indicating the state of said memory cell, to verify whether

4 said memory cell is programmed to the state indicated by  
5 said information based on the detected parameter and the  
6 selected reference signal, and to control the application of  
7 said programming signal to said memory cell based on a  
8 result of the verification.--

1 <sup>32</sup>  
--~~54~~. Apparatus according to Claim <sup>30</sup>~~52~~, wherein said  
2 control device is constructed to compare a signal  
3 corresponding to the state of said memory cell with the  
4 selected reference signal, and to control the application of  
5 said programming signal to said memory cell based on a  
6 result of the comparison.--

198 <sup>33</sup>  
1 --~~55~~. A method of verifying programming of an  
2 electrically alterable non-volatile memory cell having more  
3 than two predetermined memory states, said method  
4 comprising:  
5 selecting one of a plurality of reference signals in  
6 accordance with information indicating a memory state to  
7 which said memory cell is to be programmed, each reference  
8 signal corresponding to a different memory state of said  
9 memory cell; and  
10 comparing a signal corresponding to the state of said  
11 memory cell with the selected reference signal to verify  
12 whether said memory cell is programmed to the state  
13 indicated by said information.--

1       <sup>34</sup>  
--56. A method according to Claim <sup>33</sup>55, wherein said  
2       comparing includes comparing a bit line signal of said  
3       memory cell with the selected reference signal.--

1       <sup>35</sup>  
--57. A method according to Claim <sup>33</sup>55, wherein said  
2       comparing includes comparing a bit line voltage of said  
3       memory cell with a voltage of the selected reference  
4       signal.--

1       <sup>36</sup>  
--58. A method of verifying programming of an  
2       electrically alterable non-volatile memory cell having more  
3       than two predetermined memory states, said method  
4       comprising:  
5       selecting one of a plurality of reference signals in  
6       accordance with information indicating a memory state to  
7       which said memory cell is to be programmed, each reference  
8       signal corresponding to a different memory state of said  
9       memory cell;  
10       detecting a parameter indicating the state of said memory  
11       cell; and  
12       verifying whether said memory cell is programmed to the  
13       state indicated by said information based on the detected  
14       parameter and the selected reference signal.--

1       <sup>37</sup>  
--59. A method according to Claim <sup>36</sup>58, wherein said  
2       parameter is detected at a bit line terminal of said memory  
3       cell.--

1           <sup>38</sup>  
--~~50~~. A method according to Claim ~~50~~<sup>36</sup>, wherein said  
2       parameter is a bit line voltage of said memory cell.--

1           <sup>39</sup>  
--~~61~~. A method of programming an electrically alterable  
2       non-volatile memory cell having more than two predetermined  
3       memory states, said method comprising:  
4       selecting one of a plurality of predetermined reference  
5       signals in accordance with information indicating a memory  
6       state to which said memory cell is to be programmed, each  
7       reference signal corresponding to a different memory state  
8       of said memory cell;  
9       applying a programming signal to said memory cell; and  
10       comparing a signal corresponding to the state of said  
11       memory cell with the selected reference signal to verify  
12       whether said memory cell is programmed to the state  
13       indicated by said information.--

1           <sup>40</sup>  
--~~62~~. A method according to Claim ~~61~~<sup>39</sup>, wherein said  
2       comparing includes comparing a bit line signal of said  
3       memory cell with the selected reference signal.--

1           <sup>41</sup>  
--~~63~~. A method according to Claim ~~61~~<sup>39</sup>, wherein said  
2       comparing includes comparing a bit line voltage of said  
3       memory cell with a voltage of the selected reference  
4       signal.--

1 <sup>42</sup>  
--~~64~~. A method of programming an electrically alterable  
2 non-volatile memory cell having more than two predetermined  
3 memory states, said method comprising:  
4 selecting one of a plurality of reference signals in  
5 accordance with information indicating a memory state to  
6 which said memory cell is to be programmed, each reference  
7 signal corresponding to a different memory state of said  
8 memory cell;  
9 applying a programming signal to said memory cell;  
10 detecting a parameter indicating the state of said memory  
11 cell; and  
12 verifying whether said memory cell is programmed to the  
13 state indicated by said information based on the detected  
14 parameter and the selected reference signal.--

1 <sup>43</sup>  
--~~65~~. A method according to Claim <sup>42</sup>~~64~~, wherein said  
2 parameter is detected at a bit line terminal of said memory  
3 cell.--

1 <sup>44</sup>  
--~~66~~. A method according to Claim <sup>42</sup>~~64~~, wherein said  
2 parameter is a bit line voltage of said memory cell.--

1 <sup>45</sup>  
--~~67~~. A method of programming an electrically alterable  
2 non-volatile memory cell having more than two predetermined  
3 memory states, said method comprising:  
4 selecting one of a plurality of reference signals in  
5 accordance with information indicating a memory state to

6 which said memory cell is to be programmed, each reference  
7 signal corresponding to a different memory state of said  
8 memory cell;  
9 applying a programming signal to said memory cell; and  
10 controlling the application of said programming signal to  
11 said memory cell based on the selected reference  
12 signal.---

AS  
1 <sup>46</sup>~~--68~~. A method according to Claim <sup>45</sup>~~67~~, including  
2 detecting a parameter indicating the state of said memory  
3 cell, verifying whether said memory cell is programmed to  
4 the state indicated by said information based on the  
5 detected parameter and the selected reference signal, and  
6 wherein the application of said programming signal is  
7 controlled based on a result of said verifying.---

1 <sup>47</sup>~~--69~~. A method according to Claim <sup>45</sup>~~67~~, including  
2 comparing a signal corresponding to the state of said memory  
3 cell with the selected reference signal, and wherein the  
4 application of said programming signal is controlled based  
5 on a result of said comparing.---

REMARKS

Favorable reconsideration of this application, as  
amended, is respectfully requested.

Applicant respectfully requests an endorsed copy of Form PTO-1449 from the Information Disclosure Statement dated May 15, 1997.

Figs. 15-20 and the related disclosure have been cancelled without prejudice.<sup>1</sup> As the remaining subject matter of the present application is supported by the parent application, the present application has been redesignated as a divisional application. It is respectfully requested that the Office update the continuing data of this application accordingly. Applicant reserves the right to present claims related to the invention of Figs. 15-20 in a further divisional application.

Claim 1 has been amended more specifically to address certain features of the subject matter for which Applicant intends to obtain patent protection in the present application. Claims 2-23 have been cancelled.<sup>2</sup> Claims 24-69 have been added in order to provide more comprehensive patent protection. As will be explained hereinafter, amended Claim 1 and newly presented Claims 24-69 distinguish patentably from Suzuki et al. (Suzuki), which was cited in the outstanding rejection of Claim 1 under 35 U.S.C. § 102.

Amended Claim 1 recites a multi-level memory device. The memory device comprises an electrically alterable non-

---

<sup>1</sup> A separate Letter Proposing Drawing Changes is being filed concurrently.

<sup>2</sup> The rejection of Claim 22 as being directed to allegedly non-statutory subject matter is, of course, mooted by the cancellation of that claim.



volatile multi-level memory cell for storing input information in a corresponding one of  $K^n$  predetermined memory states of the cell, where  $K$  is a base of a predetermined number system,  $n$  is a number of bits stored per cell, and  $K^n > 2$ , and memory cell programming means for programming the cell in accordance with the input information. The device further comprises reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with the input information, each of the reference voltages corresponding to a different one of the predetermined memory states of the cell. Comparator means is also provided, for comparing a voltage of the cell with the selected reference voltage, and the comparator means generates a control signal indicating whether the state of the cell is the state corresponding to the input information.

It is apparent that Suzuki neither teaches nor suggests a multi-level memory device having the aforementioned features of Claim 1. Note, for example, that Suzuki discloses a conventional ROM which is not electrically alterable, whereas the memory device of Claim 1 utilizes an electrically alterable non-volatile memory. Further, Suzuki lacks any suggestion whatsoever of the reference voltage selecting means and comparator means, both as now defined.

Accordingly, the rejection of Claim 1 should be withdrawn. New dependent Claim 24 distinguishes patentably from Suzuki on at least the same basis as Claim 1.

As will be evident, the invention as defined in new Claims 25-69, distinguishes patentably from Suzuki in relation to its (the invention's) application to an electrically alterable non-volatile memory cell having more than two predetermined memory states, the selection of one of a plurality of reference signals in accordance with information indicating a memory state to which the cell is to be programmed (each reference signal corresponding to a different memory state of the cell), and use of the selected reference signal to verify programming of the cell or to control programming of the cell.

An allowance of this application is believed to be in order.

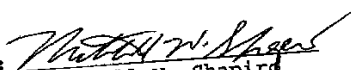
A check for \$704.00 is attached in payment of the required fees for excess claims.

The Commissioner is hereby authorized to charge to Deposit Account No. 19-1510 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and

has not been requested separately, such extension is hereby requested.

Respectfully submitted,

SHAPIRO AND SHAPIRO  
Attorneys for Applicant

By:   
Mitchell W. Shapiro  
Reg. No. 31,568

MWS:JTW:sjl

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Suite 1701  
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Tel: (703) 276-0700

June 17, 1997  
slat

Certificate of Mailing

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Mitchell W. Shapiro

---

ABSTRACT OF THE DISCLOSURE

5 An electrically alterable, non-volatile multi-bit memory cell has  $K^n$  predetermined memory states ( $K^n > 2$ ), where K is a base of a predetermined number system and n is a number of bits stored per cell. Programming of the cell is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal.

---



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

410200			
APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

02/410,200 02/27/95 BANKS

2581/0919

SHAPIRO AND SHAPIRO  
1100 WILSON BLVD., STE. 1701  
ARLINGTON VA 22209

16176-1-1

EXAMINER

ARTWORKS

PAPER NUMBER

DATE MAILED: 2511

09/19/97

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

### NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Amendment of 7-16-97

☒ The allowed claim(s) is/are 1, 8, 24-69

☐ The drawings filed on \_\_\_\_\_ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. \_\_\_\_\_

☒ including changes required by the proposed drawing correction filed on 19 June 1997, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

#### Attachment(s)

☐ Notice of References Cited, PTO-812

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

TERRELL W. FEARS  
PRIMARY EXAMINER  
GROUP 2500



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

25MAR/0919

SHAPIRO AND SHAPIRO  
1100 WILSON BLVD., STE. 1701  
ARLINGTON VA 22205

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/415-288	02/21/95	047	WEARS, T	2511 09/19/97
First Named Applicant	BANKS, J. L.	671,511	671,511	

TITLE OF INVENTION: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH 4-BITS PER CELL

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 16176-1-1	365-189.010	R96	UTILITY	YES	\$645.00	12/19/97

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.**

**THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.**

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- All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0851-0033)

# PART B—ISSUE FEE TRANSMITTAL

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Assistant Commissioner for Patents  
Washington, D.C. 20231

202600

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(Depositor's name)

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SHAPIRO AND SHAPIRO  
1100 WILSON BLVD., STE. 1701  
ARLINGTON VA 22209

25ML/0919

DEC 13 1997

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/410,200	02/27/95	047	FEARS, T	2511 09/19/97
First Named Applicant	BANKS, GERALD J.			
TITLE OF INVENTION: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL				

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 16176-1-1	363-187.010	R96	UTILITY	YES	1645.00 660.00	12/19/97

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Shapiro and Shapiro  
2  
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type). PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE BTG USA Inc.

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Gulph Mills, PA

Please check the appropriate assignee category indicated below (will not be printed on the patent)  
☐ individual ☒ corporation or other private group entity ☐ government

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(Authorized Signature) Mitchell W. Shapiro (Date) 12/18/97  
Reg. No. 31,568

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PTOL-85B (REV.10-95) Approved for use through 08/31/99. OMB 0851-0033

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE



25A1  
25X1

A-8753  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Gerald J. BANKS

Serial No.: 08/410,200

Group Art Unit: 2511

Filed: February 27, 1995

Examiner: T. Fears

For: ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS  
PER CELL

Allowed: September 19, 1997

Batch No.: R96

\* \* \*

TRANSMITTAL OF CORRECTED FORMAL DRAWINGS

Assistant Commissioner for Patents  
Washington, D.C. 20231

ATTENTION: Official Draftsperson

Sir:

Attached are four (4) sheets of formal drawings,  
corrected as required. The Commissioner is hereby  
authorized to charge any fees under 37 C.F.R. §§ 1.16 and  
1.17 that may be required by this paper to Deposit Account  
No. 19-1510.

Respectfully submitted,

SHAPIRO AND SHAPIRO  
Attorneys for Applicant

MWS:slm

1100 Wilson Blvd.  
Suite 1701  
Arlington, VA 22209  
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November 26, 1997

By: Mitchell W. Shapiro  
Mitchell W. Shapiro  
Reg. No. 31,568



APPROVED	O.G. FIG
BY	CLASS SUBCL
DRAFTSMAN	

5764571

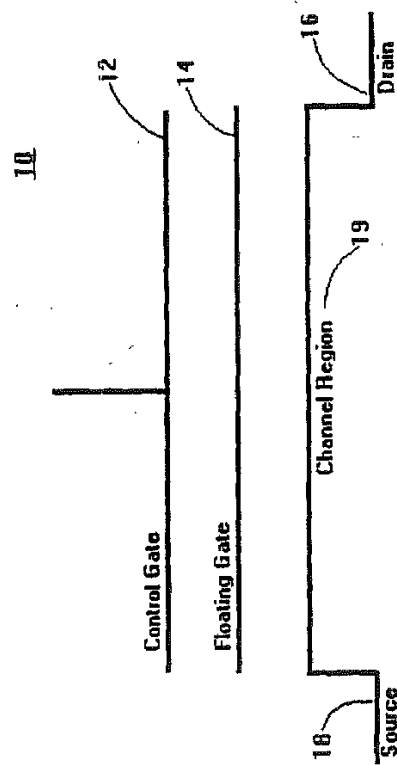


Figure 1



APPROVED	O.G. FIG.
BY	CLASS SUBC
DRAFTSMAN	

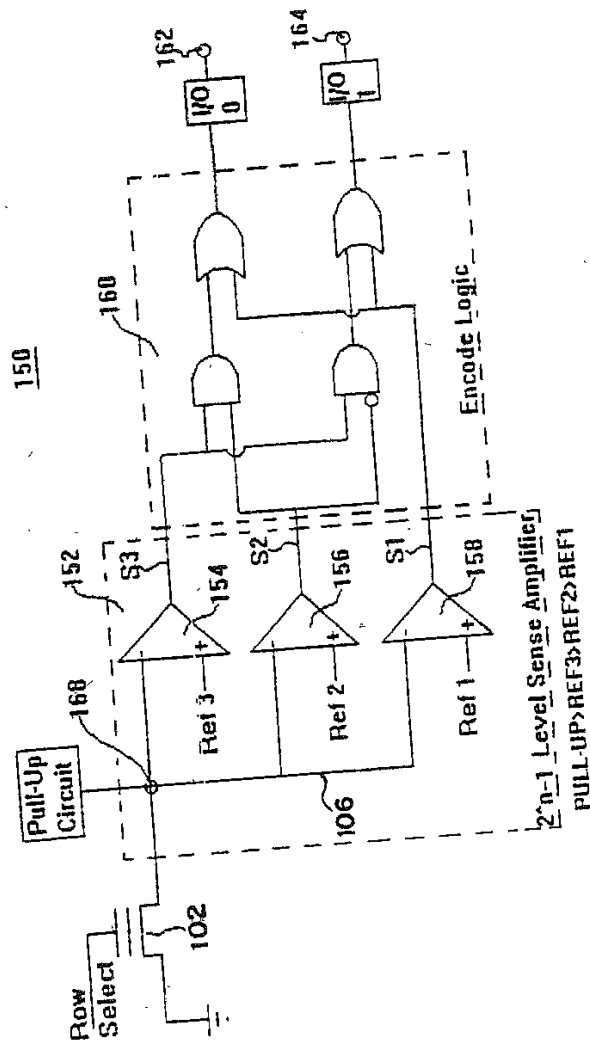


Figure 6

APPROVED	O.G. FIG
BY	CLASS SUBC
DRAFTSMAN	

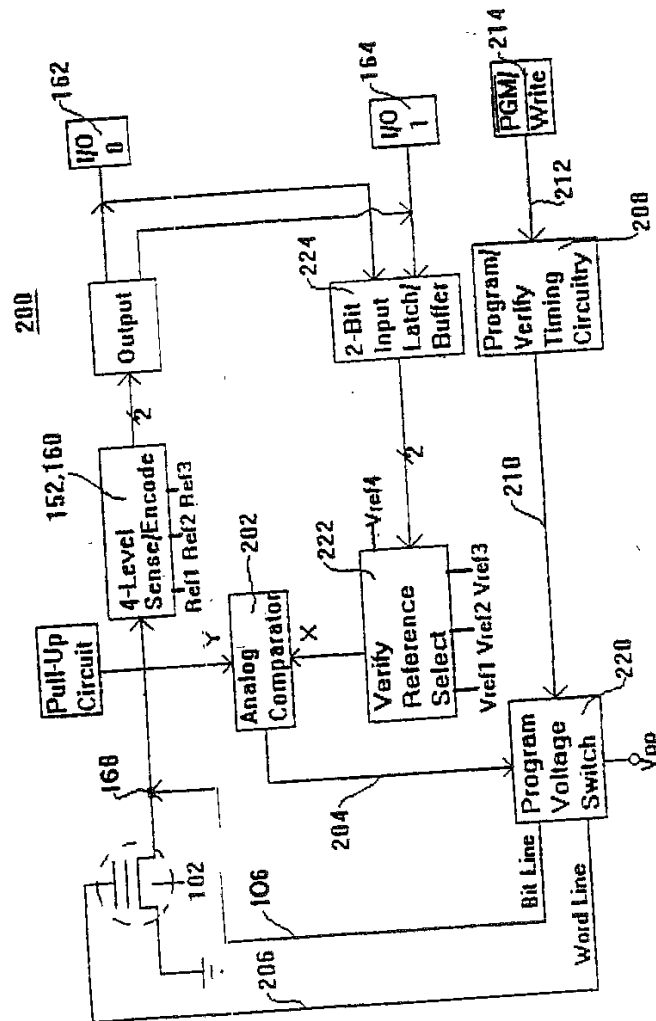


Figure 8

265-125

40 233  
EP  
OCT 1990

**HUGHES** ★ **U14** 90-299328/40 ★EP-390-404-A  
Sense amplifier determining logic state of cell - receives current during sensing with output latch switched into one state by comparison with reference current

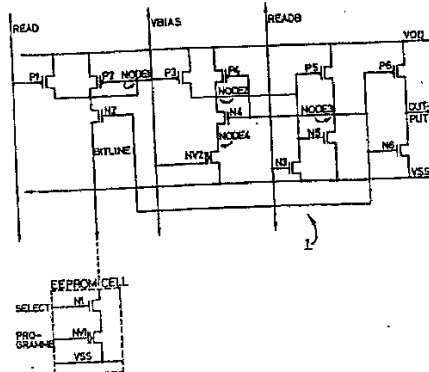
HUGHES MICROELTRN 29.03.89-GB-007045  
(03.10.90) G11c-07/06 G11c-16/06

20.03.90 as 302995 (2059MN) (E) No-SR.Pub R(DE FR GB IT NL)  
The amplifier determines the logic state of a semiconductor memory cell eg. a non volatile memory whose logic state is written or read by Fowler Nordheim tunneling from the transistor floating gate. The memory cell consists of a transistor switch NN2) for receiving current during sensing from the memory cell (NV1) with a non volatile transistor (NV2) providing a reference current.

A bistable latch is switched into one of its states depending on the result of the comparison and a feedback from the latch to the gate of the switch transistor to isolate the amplifier from the memory cell.

**ADVANTAGE** - Is faster and less sensitive to bit line capacitance.  
(4pp Dwg.No.1/1)  
N90-230218

**U14-A7A**



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The  
United  
States  
of  
America



PTO UTILITY GRANT

Paper Number 15

**The Commissioner of Patents  
and Trademarks**

*Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.*

*Therefore, this*

**United States Patent**

*Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.*

*If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.*

*If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to an statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.*

*Bruce Lehman*  
Commissioner of Patents and Trademarks

Attest

*Mary J. Green*

Form PTO-1634 (Rev. 2/97)

(RIGHT INSIDE)

**PATENT APPLICATION FEE DETERMINATION RECORD**  
Effective October 1, 1994

Application or Docket Number

410200

**CLAIMS AS FILED - PART I**

	(Column 1)	(Column 2)
FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	23 minus 20 =	* 3
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT		

\* If the difference in column 1 is less than zero, enter "0" in column 2

**SMALL ENTITY**

RATE	FEE
	365.00
x\$11=	
x38=	
+120=	
TOTAL	

**OTHER THAN SMALL ENTITY**

RATE	FEE
	730.00
x\$22=	66
x76=	152
+240=	
TOTAL	948

**CLAIMS AS AMENDED - PART II**

	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 20	Minus ** 23	= 28
Independent	* 16	Minus *** 5	= 11
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

**SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$11=	283
x38=	440
+120=	
TOTAL ADDIT. FEE	243

**OTHER THAN SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$22=	
x76=	
+240=	
TOTAL ADDIT. FEE	

**AMENDMENT B**

	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

**SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$11=	
x38=	
+120=	
TOTAL ADDIT. FEE	

**OTHER THAN SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$22=	
x76=	
+240=	
TOTAL ADDIT. FEE	

**AMENDMENT C**

	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

**SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$11=	
x38=	
+120=	
TOTAL ADDIT. FEE	

**OTHER THAN SMALL ENTITY**

RATE	ADDITIONAL FEE
x\$22=	
x76=	
+240=	
TOTAL ADDIT. FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.  
\*\* If the "Highest Number Previously Paid For" in THIS SPACE is less than 20, enter "20."  
\*\*\* If the "Highest Number Previously Paid For" in THIS SPACE is less than 3, enter "3."  
The Highest Number Previously Paid For (Total or Independent) is the highest number found in the appropriate box in column 1.

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

FORM PTO-875  
(Rev. 10/94)





## MPI Family Report (Family Bibliographic and Legal Status)

In the MPI Family report, all publication stages are collapsed into a single record, based on identical application data. The bibliographic information displayed in the collapsed record is taken from the latest publication.

Report Created Date: 2009-01-13

Name of Report:

Number of Families: 1

Comments:

### Table of Contents

1.	US5764571A 19980609 BTG USA INC US Electrically alterable non-volatile memory with N-bits per cell .....	26
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## Family1

65 records in the family, collapsed to 44 records.

AT336069T 20060915

[ no drawing available]

(GER) SPEICHERVORRICHTUNG MIT  
PROGRAMMIERBARER NICHTFLUECHTIGER  
MULTIBITSPEICHERZELLE UND VORRICHTUNG UND  
VERFAHREN ZUM ABGRENZEN VON  
SPEICHERZUSTAENDEN DER ZELLE

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: AT 01126898 T

Filing Date: 19971211

Issue/Publication Date: 20060915

Abstract: NotAvailable

Priority Data: US 97591997 19971121 A;

IPC (International Class): G11C01606; G11C01604; G11C01602; G11C01156

ECLA (European Class): G11C01156D; G11C01156D2; G11C01156D4

### Legal Status:

Date	+/-	Code	Description
20070215	(-)	RER	CEASED AS TO PARAGRAPH 5 LIT. 3 LAW INTRODUCING PATENT TREATIES

## AU5600998A 19990615

(ENG) Memory apparatus including programmable non-volatile  
multi-bit memory cell, and apparatus and method for  
demarcating memory states of the cell

[ no drawing available]

Assignee: BTG USA INC

Inventor(s): BANKS GERALD J

Application No: AU 5600998 D

Filing Date: 19971211

Issue/Publication Date: 19990615

Abstract: NotAvailable

Priority Data: US 97591997 19971121 A X; US 9722809 19971211 W V;

IPC (International Class): G11C01156

### Legal Status:

Date	+/-	Code	Description
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MicroPatent Patent Index - an enhanced INPADOC database

20000803

(-)

MK6

APPLICATION Lapsed SECTION 142(2)(F)/REG. 8.3(3) - PCT  
APPLIC. NOT ENTERING NATIONAL PHASE**DE69736493D1 20060921**(GER) Speichervorrichtung mit programmierbarer  
nichtfluechtiger Multibitspeicherzelle und Vorrichtung und  
Verfahren zum Abgrenzen von Speicherzuständen der Zelle

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: DE 69736493 A

Filing Date: 19971211

Issue/Publication Date: 20060921

Abstract: NotAvailable

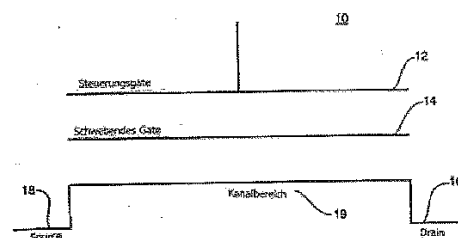
Priority Data: US 97591997 19971121 A;

IPC (International Class): G11C01606; G11C01156; G11C01602; G11C01604

ECLA (European Class): G11C01156D; G11C01156D2; G11C01156D4

## Legal Status:

Date	+/-	Code	Description
20070621	( )	8327	CHANGE IN THE PERSON/NAME/ADDRESS OF THE PATENT OWNER New owner name: BTG INTERNATIONAL INC., WEST CONSHOHOCKEN, PA., US;
20070830	(+)	8364	NO OPPOSITION DURING TERM OF OPPOSITION

**DE69736493T2 20070329**(GER) Speichervorrichtung mit programmierbarer  
nichtfluechtiger Multibitspeicherzelle und Vorrichtung und  
Verfahren zum Abgrenzen von Speicherzuständen der Zelle

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: DE 69736493 T

Filing Date: 19971211

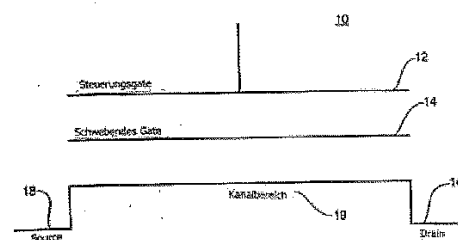
Issue/Publication Date: 20070329

Abstract: NotAvailable

Priority Data: US 97591997 19971121 A;

IPC (International Class): G11C01606; G11C01156; G11C01602; G11C01604

ECLA (European Class): G11C01156D; G11C01156D2; G11C01156D4



MicroPatent Patent Index - an enhanced INPADOC database

**Legal Status:**

Date	+/-	Code	Description
20070621	( )	8327	CHANGE IN THE PERSON/NAME/ADDRESS OF THE PATENT OWNER New owner name: BTG INTERNATIONAL INC., WEST CONSHOHOCKEN, PA., US;
20070830	(+)	8364	NO OPPOSITION DURING TERM OF OPPOSITION

EP1211692B1 20060809  
EP1211692A3 20040331  
EP1211692A2 20020605

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: EP 01126898 A

Filing Date: 19971211

Issue/Publication Date: 20060809

**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** EP 97952391 19971211 A 3; US 97591997 19971121 A;

**Related Application(s):** 97952391.7 19971211 1032938 EP;

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D2; G11C01156D4

**Designated Countries:**

---Designated States: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Andersson, Bjoern E. Awapatent AB, P.O. Box 5117, 200 71 Malmoe, SE SE

**Legal Status:**

Date	+/-	Code	Description
20060809	( )	AC	DIVISIONAL APPLICATION (ART. 76) OF: Corresponding patent document: 1032938; Country code of corresponding patent document: EP; Kind code of corresponding patent document: P;

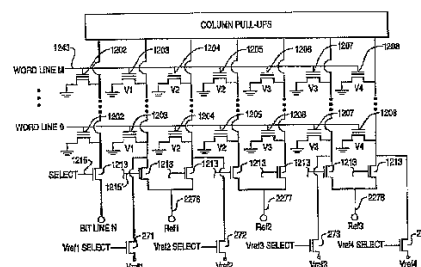


FIG. 22



20060809	(+)	AK	DESIGNATED CONTRACTING STATES: Kind code of corresponding patent document: B1; List of designated states: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE;
20060809	(+)	AX	EXTENSION OF THE EUROPEAN PATENT TO List of countries concerned with an event: AL LT LV MK RO SI;
20060809	(-)	PG25	LAPSED IN A CONTRACTING STATE ANNOUNCED VIA POSTGRANT INFORM. FROM NAT. OFFICE TO EPO Corresponding country code for PRS Code (EP REG): AT; : LAPSE BECAUSE OF FAILURE TO SUBMIT A TRANSLATION OF THE DESCRIPTION OR TO PAY THE FEE WITHIN THE PRESCRIBED TIME-LIMIT; Effective date: 20060809;
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20060809	(-)	PG25	LAPSED IN A CONTRACTING STATE ANNOUNCED VIA POSTGRANT INFORM. FROM NAT. OFFICE TO EPO Corresponding country code for PRS Code (EP REG): FI; : LAPSE BECAUSE OF FAILURE TO SUBMIT A TRANSLATION OF THE DESCRIPTION OR TO PAY THE FEE WITHIN THE PRESCRIBED TIME-LIMIT; Effective date: 20060809;
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20060906	( )	REG	REFERENCE TO A NATIONAL CODE Corresponding country code for PRS Code (EP REG): IE; Corresponding EP Code 1 for PRS Code (EP REG): FG4D;
20060921	( )	REF	CORRESPONDS TO: Corresponding patent document: 69736493; Country code of corresponding patent document: DE; Publication date of corresponding patent document: 20060921; Kind code of corresponding patent document: P;
20061018	(+)	PGFP	POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE Corresponding country code for PRS Code (EP REG): GB; Payment date: 20061018; Year of fee payment: 10;



20061031	(+)	PGFP	POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE Corresponding country code for PRS Code (EP REG): NL; Payment date: 20061031; Year of fee payment: 10;
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20061117	(+)	PGFP	POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE Corresponding country code for PRS Code (EP REG): FR; Payment date: 20061117; Year of fee payment: 10;
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EP1715490A1 20061025

(ENG) A non-volatile semiconductor memory

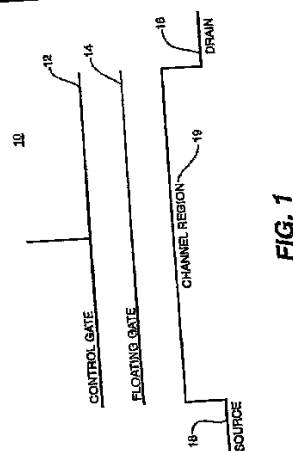
Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: EP 06118606 A

Filing Date: 19971211

Issue/Publication Date: 20061025



**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the





programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** EP 01126898 19971211 A 3 Y; EP 97952391 19971211 A 3 Y; US 97591997 19971121 A Y;

**Related Application(s):** 01126898.4 1211692 20011112

**IPC (International Class):** G11C01606; G11C01156; G11C01602; G11C01604

**ECLA (European Class):** G11C01156; G11C01156; G11C01156

**Designated Countries:**

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Andersson, Bjoern E. 00088803

Awapatent AB, P.O. Box 5117 200 71 Malmoe

SE

**Legal Status:**

Date	+/-	Code	Description
20061025	( )	AC	DIVISIONAL APPLICATION (ART. 76) OF: Corresponding patent document: 1211692; Country code of corresponding patent document: EP; Kind code of corresponding patent document: P;
20061025	( )	AC	DIVISIONAL APPLICATION (ART. 76) OF: Corresponding patent document: 1032938; Country code of corresponding patent document: EP; Kind code of corresponding patent document: P;
20061025	(+)	AK	DESIGNATED CONTRACTING STATES: Kind code of corresponding patent document: A1; List of designated states: AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR;
20061025	(+)	AX	EXTENSION OF THE EUROPEAN PATENT TO List of countries concerned with an event: AL BA HR MK YU;
20070606	(+)	17P	REQUEST FOR EXAMINATION FILED Effective date: 20070425;
20070627	(+)	17Q	FIRST EXAMINATION REPORT Effective date: 20070530;
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20070704	(+)	AXX	PAYMENT OF EXTENSION FEES List of extension states: MK; Payment date: 20070425;



EP1032938A1 20000906

(ENG) MEMORY APPARATUS INCLUDING PROGRAMMABLE NON-VOLATILE MULTI-BIT MEMORY CELL, AND APPARATUS AND METHOD FOR DEMARCATING MEMORY STATES OF THE CELL

Assignee: BTG INT INC US

Inventor(s): BANKS GERALD J US

Application No: EP 97952391 A

Filing Date: 19971211

Issue/Publication Date: 20000906

Abstract: (ENG) NotAvailable

Priority Data: US 9722809 19971211 W V; US 97591997 19971121 A X;

IPC (International Class): G11C01156

Designated Countries:

---Designated States: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Publication Language: ENG

Filing Language: ENG

Agent(s): Wiklund, Erik

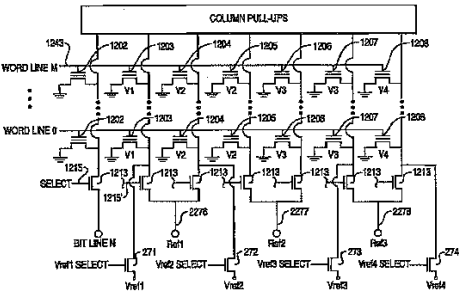
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AWAPATENT AB, Box 5117 200 71 Malmoe

SE

Legal Status:

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20020904	(+)	17Q	FIRST EXAMINATION REPORT Effective date: 20020719;
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**JP2001524732T 20011204**

**NotAvailable**

**Application No:** JP 2000522592 T

[ no drawing available]

**Filing Date:** 19971211

**Issue/Publication Date:** 20050914

**Abstract:** NotAvailable

**Priority Data:** US 9722809 19971211 W W; US 97591997 19971121 A;

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**Legal Status:** There is no Legal Status information available for this patent

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**JP3735082B2 20060111**  
**JP3735082B2 20060111**  
**JP2003030995A 20030131**

**NotAvailable**

**Application No:** JP 2002132946 A

[ no drawing available]

**Filing Date:** 20020508

**Issue/Publication Date:** 20060111

**Abstract:** NotAvailable

**Priority Data:** US 97591997 19971121 A;

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**Legal Status:** There is no Legal Status information available for this patent

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**US6584012B2 20030624**  
**US2002186587A1 20021212**

**(ENG) Electrically alterable non-volatile memory with N-bits per cell**

**Assignee:** BTG INTERNAT INC US

[ no drawing available]

**Inventor(s):** BANKS GERALD J US

**Application No:** US 16040202 A

**Filing Date:** 20020604

**Issue/Publication Date:** 20030624

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 16040202 20020604 A A; US 79404101 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01; 01 01; 01 01 01; 01 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156; G11C01156; G11C01156

**US Class:** 36518503; 36518522

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Le, Vu A.

**Legal Status:** There is no Legal Status information available for this patent



US6714455B2 20040330  
US2002196661A1 20021226

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 18883502 A

Filing Date: 20020705

Issue/Publication Date: 20040330

**Abstract:** (ENG) <p>Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals may be dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.</p>

**Priority Data:** US 18883502 20020705 A A; US 89354501 20010629 A A; US 73393700 20001212 A A; US 49313900 20000128 A A; US 41131599 19991004 A A; US 97591997 19971121 A A; US 41020095 19950227 A A;

**Related Application(s):** 09/893545 20010629 6434050 US A GRANTED (PATENT) 09/733937 20001212 6353554 US A GRANTED (PATENT) 09/411315 19991004 6246613 US A GRANTED (PATENT) 08/975919 19971121 6002614 US A GRANTED (PATENT); 09/493139 20000128 ABANDONED; 08/410200 19950227 5764571 US A GRANTED (PATENT)

**IPC (International Class):** G11C01606

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

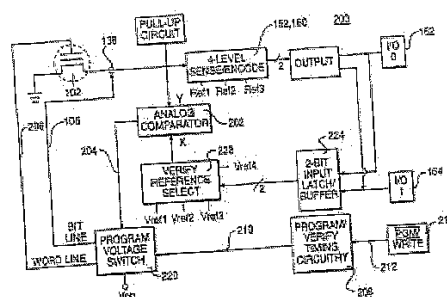
**US Class:** 36518522; 36518524; 36518529

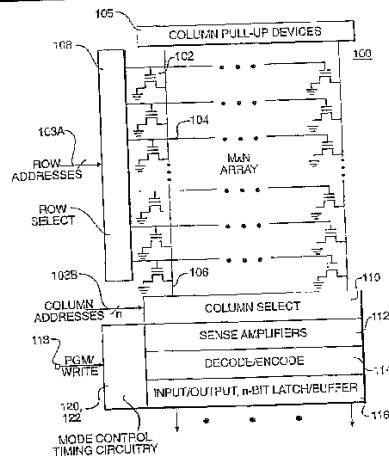
**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Elms, Richard

**Examiner Assistant:** Nguyen, Hien

**Legal Status:** There is no Legal Status information available for this patent



**US6104640A 20000815****(ENG) Electrically alterable non-volatile memory with N-bits per cell****Assignee:** BTG INTERNATIONAL INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 19520198 A**Filing Date:** 19981118**Issue/Publication Date:** 20000815

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 08/911731 19970815 US PENDING; 08/410200 19950227 US PENDING; 08/071816 19930604 US PENDING; 07/652878 19910208 US PENDING

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518501; 365168; 36518905; 36518915; 36518916; 36523001; 36523312

**Publication Language:** ENG

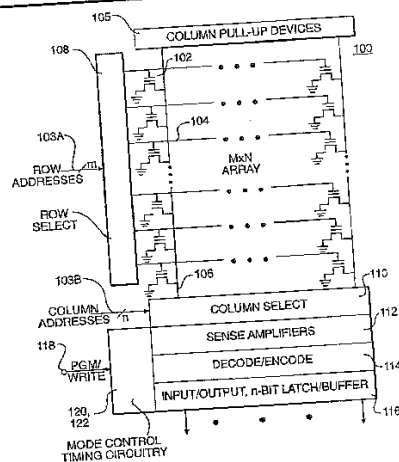
**Filing Language:** ENG

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



**US6014327A 20000111****(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell****Assignee:** BTG INTERNATIONAL INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 31174899 A**Filing Date:** 19990514**Issue/Publication Date:** 20000111

**Abstract:** (ENG) <p>Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.</p>

**Priority Data:** US 31174899 19990514 A I; US 97591997 19971121 A R; US 41020095 19950227 A R; US 7181693 19930604 A R; US 65287891 19910208 A R;

**Related Application(s):** 08/975919 19971121 PENDING 08/071816 19930604 5394362 GRANTED; 07/652878 19910208 5218569 GRANTED; 08/410200 19950227 5764571 GRANTED

**IPC (International Class):** G11C01300

**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01156D

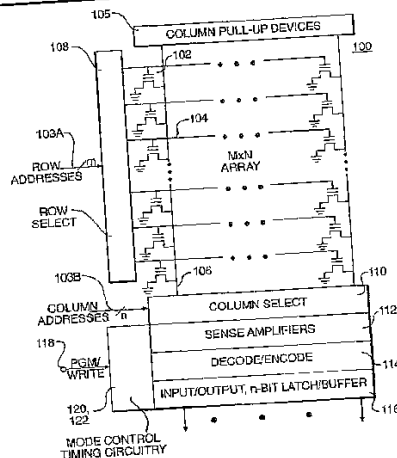
**US Class:** 36518503; 365168

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



**US6011716A 20000104****(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell****Assignee:** BTG INTERNATIONAL INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 31174999 A**Filing Date:** 19990514**Issue/Publication Date:** 20000104

**Abstract:** (ENG) <p>Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.</p>

**Priority Data:** US 31174999 19990514 A I; US 97591997 19971121 A R; US 41020095 19950227 A R; US 7181693 19930604 A R; US 65287891 19910208 A R;

**Related Application(s):** 08/975919 19971121 PENDING 08/071816 19930604 5394362 GRANTED; 07/652878 19910208 5218569 GRANTED; 08/410200 19950227 5764571 GRANTED

**IPC (International Class):** G11C01300

**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01156D

**US Class:** 36518503; 365168

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent





**US6118692A 20000912**

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

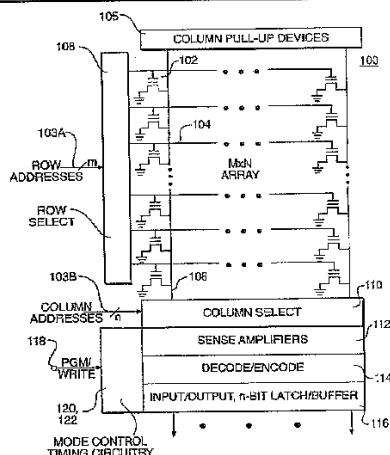
Assignee: BTG INTERNATIONAL INC US

Inventor(s): BANKS GERALD J US

Application No: US 31175099 A

Filing Date: 19990514

Issue/Publication Date: 20000912



**Abstract:** (ENG) <p>Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.</p>

**Priority Data:** US 31175099 19990514 A R; US 97591997 19971121 A R; US 41020095 19950227 A R; US 7181693 19930604 A R; US 65287891 19910208 A R; US 19520198 19981118 A R; US 91173197 19970815 A R;

**Related Application(s):** 08/975919 19971121 6002614 GRANTED 08/071816 19930604 5394362 GRANTED 08/911731 19970815 5872735 GRANTED 08/410200 19950227 5764571 GRANTED; 911731 19970815; 07/652878 19910208 5218569 GRANTED 09/195201 19981118 PENDING; 08/410200 19950227 5764571 GRANTED

**IPC (International Class):** G11C01300

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518503; 365168

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**US Post Issuance:**

--US Certificate of Correction: 20020827 20020917 a Certificate of Correction was issued for this patent

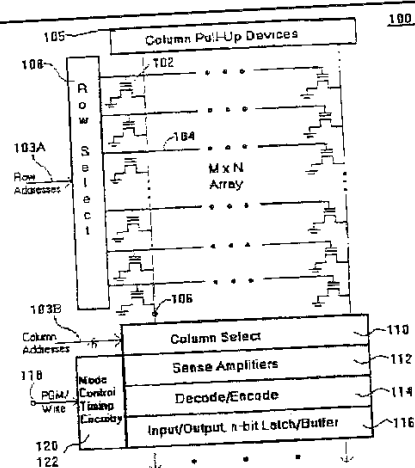
**Legal Status:**

Date	+/-	Code	Description
20020827		CC	CERTIFICATE OF CORRECTION



MicroPatent Patent Index - an enhanced INPADOC database

The block diagram illustrates the internal structure and control logic of a non-volatile memory array. The array is organized into rows and columns. Each row contains a series of memory cells, each consisting of a word line (e.g., 102, 104, 106) and a bit line (e.g., 206, 208, 210). The cells are connected to a common source line (100) and a common drain line (101). The array is controlled by a word line driver (103) and a bit line driver (105). The word line driver is connected to a word line (102) and a word line (104). The bit line driver is connected to a bit line (206) and a bit line (208). The array is also connected to a pull-up circuit (107) and a pull-down circuit (109). The pull-up circuit is connected to a word line (102) and a word line (104). The pull-down circuit is connected to a bit line (206) and a bit line (208). The array is controlled by a word line decoder (110) and a bit line decoder (112). The word line decoder is connected to a word line (102) and a word line (104). The bit line decoder is connected to a bit line (206) and a bit line (208). The array is also connected to a sense amplifier (114) and a sense amplifier (116). The sense amplifier (114) is connected to a word line (102) and a word line (104). The sense amplifier (116) is connected to a bit line (206) and a bit line (208). The array is controlled by a word line driver (103) and a bit line driver (105). The word line driver is connected to a word line (102) and a word line (104). The bit line driver is connected to a bit line (206) and a bit line (208). The array is also connected to a pull-up circuit (107) and a pull-down circuit (109). The pull-up circuit is connected to a word line (102) and a word line (104). The pull-down circuit is connected to a bit line (206) and a bit line (208). The array is controlled by a word line decoder (110) and a bit line decoder (112). The word line decoder is connected to a word line (102) and a word line (104). The bit line decoder is connected to a bit line (206) and a bit line (208). The array is also connected to a sense amplifier (114) and a sense amplifier (116). The sense amplifier (114) is connected to a word line (102) and a word line (104). The sense amplifier (116) is connected to a bit line (206) and a bit line (208).

**US5764571A 19980609****(ENG)** Electrically alterable non-volatile memory with N-bits per cell**Assignee:** BTG USA INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 41020095 A**Filing Date:** 19950227**Issue/Publication Date:** 19980609

**Abstract:** (ENG) An electrically alterable, non-volatile multi-bit memory cell has  $Kn$  predetermined memory states ( $Kn > 2$ ), where  $K$  is a base of a predetermined number system and  $n$  is a number of bits stored per cell. Programming of the cell is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal.

**Priority Data:** US 41020095 19950227 A I; US 7181693 19930604 A I; US 65287891 19910208 A R;

**Related Application(s):** 01 01; 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01156D

**US Class:** 36518907; 365168; 365201; 365205; 365207

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Shapiro and Shapiro

**Examiner Primary:** Fears, Terrell W.

**Assignments Reported to USPTO:**

**Reel/Frame:** 08382/0105 **Date Signed:** 19970213 **Date Recorded:** 19970303  
**Assignee:** BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS PENNSYLVANIA 19406

**Assignor:** BANKS, GERALD J.

**Corres. Addr:** BTG USA INC. JOEL F. SPIVAK PATENT DEPARTMENT 2200 RENAISSANCE BLVD.  
 GULPH MILLS, PA 19406

**Brief:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

**Reel/Frame:** 09350/0610 **Date Signed:** 19951010 **Date Recorded:** 19980728  
**Assignee:** BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS  
 PENNSYLVANIA 19406

**Assignor:** BRITISH TECHNOLOGY GROUP USA INC.; BTG USA INC.

**Corres. Addr:** BTG INTERNATIONAL INC. JOEL F. SPIVAK 2200 RENAISSANCE BOULEVARD  
 GULPH MILLS, PA 19406

**Brief:** CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).



Legal Status:			Description
Date	+/-	Code	ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name: BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS, P; Effective date: 19970213;
19970303	( )	AS02	
19970303	( )	AS02	ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name: BANKS, GERALD J.; Effective date: 19970213;

**US6246613B1 20010612**

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

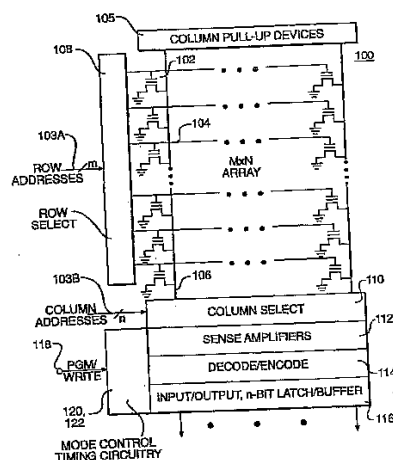
Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 41131599 A

Filing Date: 19991004

Issue/Publication Date: 20010612



**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** US 41131599 19991004 A A; US 97591997 19971121 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518915; 36518522

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**US Post Issuance:**

--US Certificate of Correction: 20020611



**Legal Status:**

Date	+/-	Code	Description
20020611	( )	CC	CERTIFICATE OF CORRECTION

**US6724656B2 20040420**  
**US2003202378A1 20031030**

(ENG) Electrically alterable non-volatile memory with n-bits per cell

**Assignee:** BTG INTERNAT INC US

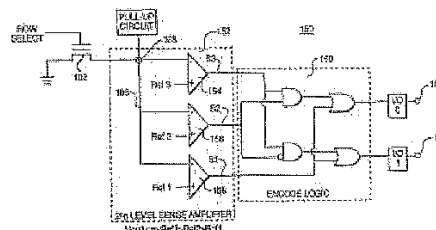
**Inventor(s):** BANKS GERALD J US

**Application No:** US 42873203 A

**Filing Date:** 20030505

**Issue/Publication Date:** 20040420

**Abstract:** (ENG) <p>An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell can be performed without actually reading the memory state of the cell during the programming operation. A plurality of the memory cells are preferably arranged in a matrix of rows and columns disposed substantially in a rectangle, with a plurality of word lines coupled with memory gate electrodes intersecting a first side of the rectangle substantially perpendicularly, a plurality of bit lines coupled with memory drain-source current paths intersecting a second side of the rectangle substantially perpendicularly (the second side also substantially perpendicularly intersecting the first side), a row select circuit being disposed at the first side for coupling with the word lines, and peripheral circuitry including a column select circuit and a sense circuit being disposed at the second side.</p>



**Priority Data:** US 42873203 20030505 A A; US 16040202 20020604 A A; US 79404101 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 10/160402 20020604 6584012 US A GRANTED (PATENT) 09/794041 20010228 6404675 US A GRANTED (PATENT) 09/493138 20000128 6243321 US A GRANTED (PATENT) 09/195201 19981118 6104640 US A GRANTED (PATENT) 08/911731 19970815 5872735 US A GRANTED (PATENT) <RDA division> 08/410200 19950227 5764571 US A GRANTED (PATENT) 08/071816 19930604 5394362 US A GRANTED (PATENT); 07/652878 19910208 5218569 US A GRANTED (PATENT)

**IPC (International Class):** G11C01604

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518501; 36518503

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Le, Vu Anh

**Legal Status:** There is no Legal Status information available for this patent

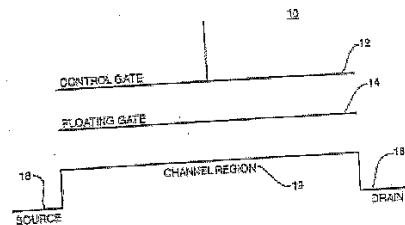


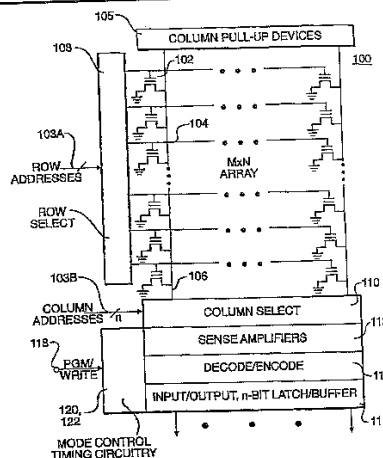
**US2006221687A1 20061005****(ENG) Electrically alterable non-volatile memory with n-bits per cell****Assignee:** BTG INTERNAT INC**Inventor(s):** BANKS GERALD J US**Application No:** US 44622206 A**Filing Date:** 20060605**Issue/Publication Date:** 20061005

**Abstract:** (ENG) <p num="0000">An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell can be performed without actually reading the memory state of the cell during the programming operation. A plurality of the memory cells are preferably arranged in a matrix of rows and columns disposed substantially in a rectangle, with a plurality of word lines coupled with memory gate electrodes intersecting a first side of the rectangle substantially perpendicularly, a plurality of bit lines coupled with memory drain-source current paths intersecting a second side of the rectangle substantially perpendicularly (the second side also substantially perpendicularly intersecting the first side), a row select circuit being disposed at the first side for coupling with the word lines, and peripheral circuitry including a column select circuit and a sense circuit being disposed at the second side. </p>

**Priority Data:** US 7181693 19930604 A 3; US 16040202 20020604 A 3; US 19520198 19981118 A 3; US 41020095 19950227 A 3; US 42873203 20030505 A 3; US 44622206 20060605 A; US 49313800 20000128 A 3; US 65287891 19910208 A 1; US 79404101 20010228 A 3; US 80828604 20040325 A 3; US 91173197 19970815 A 3;

**Related Application(s):** 11/446222 20060605 10/808286 20040325 7075825 US GRANTED 10/808286 20040325 10/428732 20030505 6724656 US GRANTED 10/428732 20030505 10/160402 20020604 6584012 US GRANTED 10/160402 20020604 09/794041 20010228 6404675 US GRANTED 09/794041 20010228 09/493138 20000128 6243321 US GRANTED 09/493138 20000128 09/195201 19981118 6104640 US GRANTED 09/195201 19981118 08/911731 19970815 5872735 US GRANTED 08/911731 19970815 08/410200 19950227 5764571 US GRANTED 08/410200 19950227 08/071816 19930604 5394362 US GRANTED; 08/071816 19930604 07/652878 19910208 5218569 US GRANTED

**IPC (International Class):** G11C01604**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01612; G11C01634V4**US Class:** 36518503**Publication Language:** ENG**Legal Status:** There is no Legal Status information available for this patent

**US6243321B1 20010605****(ENG)** Electrically alterable non-volatile memory with n-bits per cell**Assignee:** BTG INT INC**Inventor(s):** BANKS GERALD J US**Application No:** US 49313800 A**Filing Date:** 20000128**Issue/Publication Date:** 20010605

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 49313800 20000128 A A; US 19520199 19991118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518521; 36518524; 36518529; 36518915; 365207; 365218; 36523311; 36523317

**Publication Language:** ENG

**Filing Language:** ENG

**Examiner Primary:** Fears, Terrell W.

**US Post Issuance:**

--US Certificate of Correction: 20020723

**Legal Status:**

Date	+/-	Code	Description
20020723	( )	CC	CERTIFICATE OF CORRECTION



**US6343034B2 20020129**  
**US2001019500A1 20010906**

**(ENG) Electrically alterable non-volatile memory with n-bits per cell**

[ no drawing available]

**Assignee:** BTG INTERNAT INC US

**Inventor(s):** BANKS GERALD J US

**Application No:** US 49314000 A

**Filing Date:** 20000128

**Issue/Publication Date:** 20020129

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without reading out the cell.

**Priority Data:** US 49314000 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01; 01 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518915; 36523002

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**US Post Issuance:**

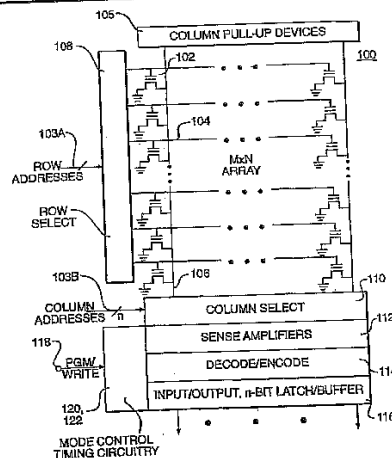
--US Certificate of Correction: 20020528

**Legal Status:**

Date	+/-	Code	Description
20020528	()	CC	CERTIFICATE OF CORRECTION





**US6356486B1 20020312****(ENG) Electrically alterable non-volatile memory with n-bits per cell****Assignee:** BTG INTERNAT INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 58696700 A**Filing Date:** 20000605**Issue/Publication Date:** 20020312

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signals which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 58696700 20000605 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518915; 365045; 3651851; 3651852; 36518905; 36518916; 3652101; 36521012; 365218; 36523311

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



**US5218569A 19930608****(ENG)** Electrically alterable non-volatile memory with n-bits per memory cell

[ no drawing available]

**Assignee:** BANKS GERALD J US**Inventor(s):** BANKS GERALD J US**Application No:** US 65287891 A**Filing Date:** 19910208**Issue/Publication Date:** 19930608

**Abstract:** (ENG) <p>The bit storage density of an Electrically Alterable Non- Volatile Memory (EANVM) cell is improved by increasing the number of bits that are stored on an individual memory cell, without increasing the size and complexity of the memory cell, by allowing a non-volatile memory cell to assume 2 n discrete memory states. A multi-bit memory cell uses a floating gate FET which is electrically programmed to 2 n different thresholds. The 2 n different conductivity states of the FET are provided as information storage states for the cell.</p>

**Priority Data:** US 65287891 19910208 A I;**IPC (International Class):** G11C01300**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01156D**US Class:** 36518521; 365045; 36518519; 3651852; 36518522; 36518529; 365186**Examiner Primary:** Fears, Terrell W.**Assignments Reported to USPTO:****Reel/Frame:** 08382/0105 **Date Signed:** 19970213 **Date Recorded:** 19970303**Assignee:** BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS PENNSYLVANIA 19406**Assignor:** BANKS, GERALD J.**Corres. Addr:** BTG USA INC. JOEL F. SPIVAK PATENT DEPARTMENT 2200 RENAISSANCE BLVD. GULPH MILLS, PA 19406**Brief:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).**Reel/Frame:** 09350/0610 **Date Signed:** 19951010 **Date Recorded:** 19980728**Assignee:** BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS PENNSYLVANIA 19406**Assignor:** BRITISH TECHNOLOGY GROUP USA INC.; BTG USA INC.**Corres. Addr:** BTG INTERNATIONAL INC. JOEL F. SPIVAK 2200 RENAISSANCE BOULEVARD GULPH MILLS, PA 19406**Brief:** CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).**Legal Status:****Date**  
19970303

+/-

**Code**  
AS02**Description**

ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name:  
BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS, P;  
Effective date: 19970213;  
ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name:  
BANKS, GERALD J.; Effective date: 19970213;

19970303

AS02



**US5394362A 19950228****(ENG)** Electrically alterable non-volatile memory with N-bits per memory cell

[ no drawing available]

**Assignee:** BANKS; GERALD J. US**Inventor(s):** BANKS GERALD J US**Application No:** US 7181693 A**Filing Date:** 19930604**Issue/Publication Date:** 19950228

**Abstract:** (ENG) <p>The bit storage density of an Electrically Alterable Non- Volatile Memory (EANVM) cell is improved by increasing the number of bits that are stored on an individual memory cell, without increasing the size and complexity of the memory cell, by allowing a non-volatile memory cell to assume  $2^n$  discrete memory states. A multi-bit memory cell uses a floating gate FET which is electrically programmed to  $2^n$  different thresholds. The  $2^n$  different conductivity states of the FET are provided as information storage states for the cell.</p>

**Priority Data:** US 7181693 19930604 A R; US 65287891 19910208 A R;**Related Application(s):** 07/652878 19910208 5218569 GRANTED**IPC (International Class):** G11C01140**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4**US Class:** 36518503; 36518519; 3651852; 36518522; 36518524; 36518528; 36518533**Agent(s):** Townsend and Townsend Khourie and Crew**Examiner Primary:** Fears, Terrell W.**Assignments Reported to USPTO:****Reel/Frame:** 08382/0105 **Date Signed:** 19970213 **Date Recorded:** 19970303**Assignee:** BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS PENNSYLVANIA 19406**Assignor:** BANKS, GERALD J.**Corres. Addr:** BTG USA INC. JOEL F. SPIVAK PATENT DEPARTMENT 2200 RENAISSANCE BLVD.  
GULPH MILLS, PA 19406**Brief:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).**Reel/Frame:** 09350/0610 **Date Signed:** 19951010 **Date Recorded:** 19980728**Assignee:** BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS  
PENNSYLVANIA 19406**Assignor:** BRITISH TECHNOLOGY GROUP USA INC.; BTG USA INC.**Corres. Addr:** BTG INTERNATIONAL INC. JOEL F. SPIVAK 2200 RENAISSANCE BOULEVARD  
GULPH MILLS, PA 19406**Brief:** CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).**Legal Status:****Date** +/-**Code**  
AS02**Description**ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name:  
BTG USA INC. 2200 RENAISSANCE BLVD. GULPH MILLS, P;  
Effective date: 19970213;

MicroPatent Patent Index - an enhanced INPADOC database

19970303

AS02

ASSIGNMENT OF ASSIGNOR'S INTEREST New owner name:  
BANKS, GERALD J.; Effective date: 19970213;

US2002034097A1 20020321  
US6353554B1 20020305

(ENG) Memory apparatus including programmable non-volatile  
multi-bit memory cell, and apparatus and method for  
demarcating memory states of the cell

[ no drawing available]

Assignee: BANKS GERALD J. US

Inventor(s): BANKS GERALD J US

Application No: US 73393700 A

Filing Date: 20001212

Issue/Publication Date: 20020321

**Abstract:** (ENG) <p>Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout. </p>

**Priority Data:** US 73393700 20001212 A A; US 49313900 20000128 A A; US 41131599 19991004 A A; US 97591997 19971121 A A; US 41020095 19950227 A A;

**Related Application(s):** 09/411315 19991004 6246613 US GRANTED 08/975919 19971121 6002614 US GRANTED; 09/493139 20000128; 08/410200 19950227 5764571 US GRANTED

**IPC (International Class):** G11C01134

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518503

**Legal Status:** There is no Legal Status information available for this patent



The block diagram illustrates the internal structure and control logic of a non-volatile memory array. The array is organized into rows and columns, with word lines (102, 104, 106) and bit lines (200, 202, 204) intersecting at memory cells (108). The control logic includes a pull-up circuit (130) connected to the word lines, a 4-level sense/amplifier (132) connected to the bit lines, and a 2-bit input latch/buffer (224) connected to the sense/amplifier. A program voltage switch (210) is connected to the word lines and a program verify timing circuitry (212) is connected to the bit lines. The control logic also includes a 4-level sense/amplifier (132) and a 2-bit input latch/buffer (224). The control logic is connected to a data input/output (102) and a program verify timing circuitry (212).

**US6327189B2 20011204**  
**US2001008489A1 20010719**

**(ENG) Electrically alterable non-volatile memory with n-bits per cell**

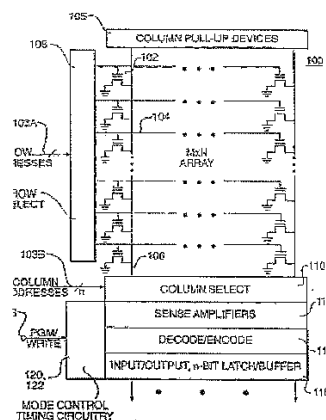
**Assignee:** BTG INTERNAT INC US

**Inventor(s):** BANKS GERALD J US

**Application No:** US 79403101 A

**Filing Date:** 20010228

**Issue/Publication Date:** 20011204



**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 79403101 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01; 01 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518518; 36518914; 365218

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**US Post Issuance:**

--US Certificate of Correction: 20020416

**Legal Status:**

Date	+/-	Code	Description
20020416	( )	CC	CERTIFICATE OF CORRECTION



MicroPatent Patent Index - an enhanced INPADOC database

US6324121B2 20011127  
US2001006477A1 20010705

(ENG) Electrically alterable non-volatile memory with n-bits per cell

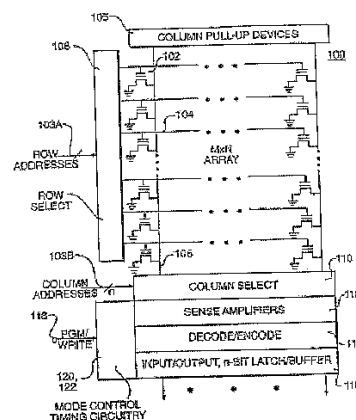
Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 79403201 A

Filing Date: 20010228

Issue/Publication Date: 20011127



**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 79403201 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01; 01 01; 01 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36523314; 36518914; 365218

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



US6404675B2 20020611  
US2001006478A1 20010705

(ENG) Electrically alterable non-volatile memory with n-bits per cell

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 79404101 A

Filing Date: 20010228

Issue/Publication Date: 20020611

**Abstract:** (ENG) <p>An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.</p>

**Priority Data:** US 79404101 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 07/652878 19910208 5218569 US A GRANTED (PATENT)

**IPC (International Class):** G11C01604

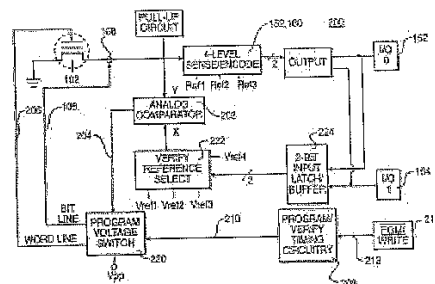
**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518503; 365168; 36518522

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Le, Vu A.

**Legal Status:** There is no Legal Status information available for this patent





**US6344998B2 20020205**  
**US2001040824A1 20011115**

**(ENG) Electrically alterable non-volatile memory with N-Bits per cell**

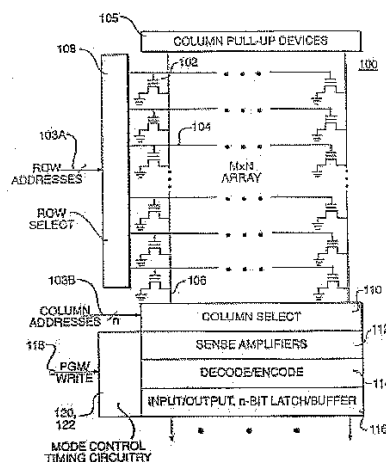
**Assignee:** BTG INTERNAT INC US

**Inventor(s):** BANKS GERALD J US

**Application No:** US 79404201 A

**Filing Date:** 20010228

**Issue/Publication Date:** 20020205



**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 79404201 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01; 01 01 01; 01 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 3651852; 36518522; 36518529; 36518907; 36518915; 365205; 365218; 36523001; 36523311; 36523317

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



US6339545B2 20020115  
US2001033512A1 20011025

(ENG) Electrically alterable non-volatile memory with n-bits per cell

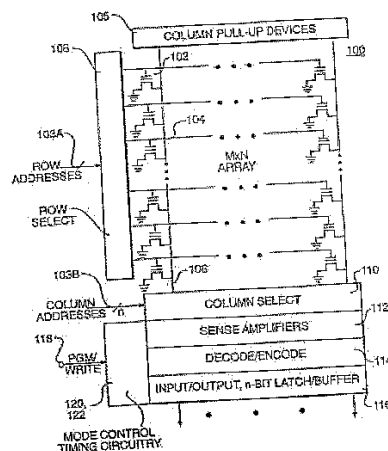
Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 79404301 A

Filing Date: 20010228

Issue/Publication Date: 20020115



**Abstract:** (ENG) <p>An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.</p>

**Priority Data:** US 79404301 20010228 A A; US 49313800 20000128 A A; US 19520198 19981118 A A; US 91173197 19970815 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 07/652878 19910208 5218569 US A GRANTED (PATENT)

**IPC (International Class):** G11C01300

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518503; 365201; 365207

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent



US6870763B2 20050322  
US2004242009A1 20041202

(ENG) Electrically alterable non-volatile memory with n-bits per cell

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 80828404 A

Filing Date: 20040325

Issue/Publication Date: 20050322

**Abstract:** (ENG) <p>An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell can be performed without actually reading the memory state of the cell during the programming operation. A plurality of the memory cells are preferably arranged in a matrix of rows and columns disposed substantially in a rectangle, with a plurality of word lines coupled with memory gate electrodes intersecting a first side of the rectangle substantially perpendicularly, a plurality of bit lines coupled with memory drain-source current paths intersecting a second side of the rectangle substantially perpendicularly (the second side also substantially perpendicularly intersecting the first side), a row select circuit being disposed at the first side for coupling with the word lines, and peripheral circuitry including a column select circuit and a sense circuit being disposed at the second side.</p>

**Priority Data:** US 7181693 19930604 A 3; US 16040202 20020604 A 3; US 19520198 19981118 A 3; US 41020095 19950227 A 3; US 42873203 20030505 A 3; US 49313800 20000128 A 3; US 65287891 19910208 A 1; US 79404101 20010228 A 3; US 80828404 20040325 A Z; US 91173197 19970815 A 3;

**Related Application(s):** 10/428732 20030505 6724656 US A GRANTED (PATENT) 10/160402 20020604 6584012 US A GRANTED (PATENT) 09/794041 20010228 6404675 US A GRANTED (PATENT) 09/493138 20000128 6243321 US A GRANTED (PATENT) 09/195201 19981118 6104640 US A GRANTED (PATENT) 08/911731 19970815 5872735 US A GRANTED (PATENT) 08/410200 19950227 5764571 US A GRANTED (PATENT) 08/071816 19930604 5394362 US A GRANTED (PATENT); 07/652878 19910208 5218569 US A GRANTED (PATENT)

**IPC (International Class):** G11C01604

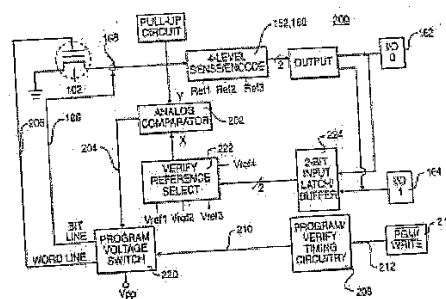
**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518501; 36518503

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Le, Vu A.

**Legal Status:** There is no Legal Status information available for this patent



MicroPatent Patent Index - an enhanced INPADOC database

**US7075825B2 20060711**  
**US2004179397A1 20040916**

**(ENG) Electrically alterable non-volatile memory with n-bits per cell**

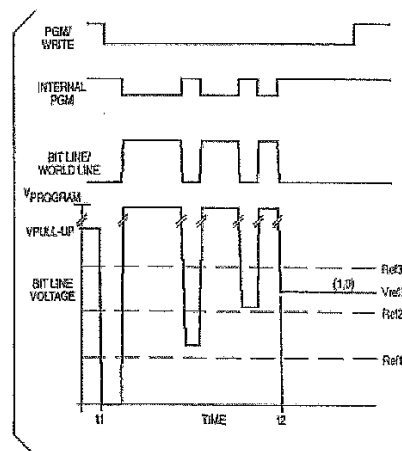
**Assignee:** BTG INTERNAT INC US

**Inventor(s):** BANKS GERALD J US

**Application No:** US 80828604 A

**Filing Date:** 20040325

**Issue/Publication Date:** 20060711



**Abstract:** (ENG) <p num="0000">An electrically alterable, non-volatile memory cell has more than two memory states that can be programmed selectively. Programming of the cell can be performed without actually reading the memory state of the cell during the programming operation. A plurality of the memory cells are preferably arranged in a matrix of rows and columns disposed substantially in a rectangle, with a plurality of word lines coupled with memory gate electrodes intersecting a first side of the rectangle substantially perpendicularly, a plurality of bit lines coupled with memory drain-source current paths intersecting a second side of the rectangle substantially perpendicularly (the second side also substantially perpendicularly intersecting the first side), a row select circuit being disposed at the first side for coupling with the word lines, and peripheral circuitry including a column select circuit and a sense circuit being disposed at the second side.</p>

**Priority Data:** US 7181693 19930604 A 3; US 16040202 20020604 A 3; US 19520198 19981118 A 3; US 41020095 19950227 A 3; US 42873203 20030505 A 3; US 49313800 20000128 A 3; US 65287891 19910208 A 1; US 79404101 20010228 A 3; US 80828604 20040325 A; US 91173197 19970815 A 3;

**Related Application(s):** 10/808286 10/428732 20030505 6724656 US A 10/428732 10/160402 20020604 6584012 US A 10/160402 09/794041 20010228 6404675 US A 09/794041 09/493138 20000128 6243321 US A 09/493138 09/195201 19981118 6104640 US A 09/195201 08/911731 19970815 5872735 US A 08/911731 08/410200 19950227 5764571 US A 08/410200 08/071816 19930604 5394362 US A; 08/071816 07/652878 19910208 5218569 US A

**IPC (International Class):** G11C00700; G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518519; 36518503

**Publication Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Le, Vu A.

**Legal Status:** There is no Legal Status information available for this patent



MicroPatent Patent Index - an enhanced INPADOC database



**US2008239829A1 20081002**

**(ENG) MEMORY APPARATUS INCLUDING  
PROGRAMMABLE NON-VOLATILE MULTI-BIT  
MEMORY CELL, AND APPARATUS AND METHOD FOR  
DEMARCATING MEMORY STATES OF THE CELL**

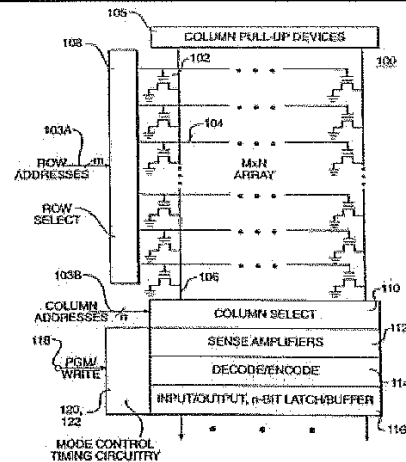
**Assignee:** BANKS GERALD J

**Inventor(s):** BANKS GERALD J US

**Application No:** US 87668307 A

**Filing Date:** 20071022

**Issue/Publication Date:** 20081002



**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals may be dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** US 87668307 20071022 A N; US 40714806 20060420 A 1 N; US 94419404 20040920 A 3 Y; US 74289003 20031223 A 3 Y; US 18883502 20020705 A 3 Y; US 89354501 20010629 A 3 Y; US 73393700 20001212 A 3 Y; US 49313900 20000128 A B Y; US 41131599 19991004 A 3 Y; US 97591997 19971121 A 3 Y; US 41020095 19950227 A 2 Y;

**Related Application(s):** 11/407148 20060420 7286414 US; 10/944194 20040920 7068542 US; 10/742890 20031223 7006384 US; 10/188835 20020705 6714455 US; 09/893545 20010629 6434050 US; 09/733937 20001212 6353554 US; 09/493139 20000128 US ABANDONED; 09/411315 19991004 6246613 US; 08/975919 19971121 6002614 US; 08/410200 19950227 5764571 US

**IPC (International Class):** G11C01604

**ECLA (European Class):** G11C01156D4; G11C01156D2; G11C01628; G11C01630; G11C01634V4

**US Class:** 36518529; 3651852; 36518522

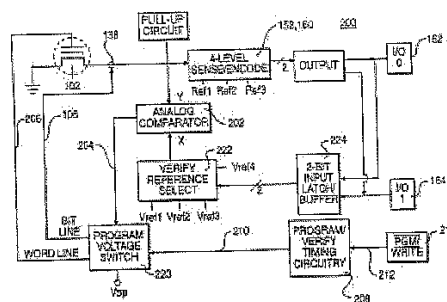
**Publication Language:** ENG

**Filing Language:** ENG

**Legal Status:** There is no Legal Status information available for this patent



MicroPatent Patent Index - an enhanced INPADOC database



US6381172B2 20020430  
US2001055222A1 20011227

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

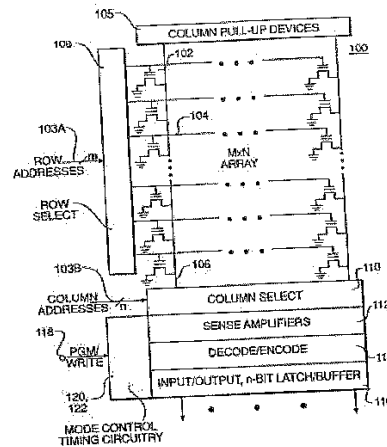
Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 89413401 A

Filing Date: 20010629

Issue/Publication Date: 20020430



**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals may be dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** US 89413401 20010629 A A; US 73393700 20001212 A A; US 49313900 20000128 A A; US 41131599 19991004 A A; US 97591997 19971121 A A; US 41020095 19950227 A A;

**Related Application(s):** 01 01; 01 01; 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518503; 365168; 36518907; 36518915

**Publication Language:** ENG

**Filing Language:** ENG

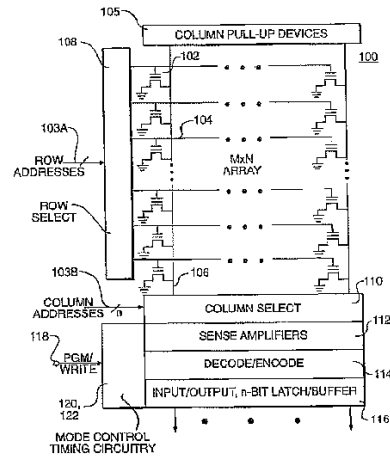
**Agent(s):** Miles Stockbridge P.C.

**Examiner Primary:** Fears, Terrell W.

**Legal Status:** There is no Legal Status information available for this patent





**US5872735A 19990216****(ENG) Electrically alterable non-volatile memory with N-bits per cell****Assignee:** BTG INTERNATIONAL INC US**Inventor(s):** BANKS GERALD J US**Application No:** US 91173197 A**Filing Date:** 19970815**Issue/Publication Date:** 19990216

**Abstract:** (ENG) An electrically alterable, non-volatile memory cell has more than 2 memory states that can be programmed selectively. Programming of the cell is conducted by applying a plurality of programming signals having different characteristics to the cell. The programming signals include at least a first programming signal which programs the cell by a first increment and a subsequent programming signal which programs the cell by a second increment smaller than the first increment. As the cell is being programmed to a selected state, its programming status is verified independently of reference values bounding the memory states. For this purpose, a signal indicative of the programming status (e.g., the cell's bit line signal) is compared with a reference signal corresponding to the selected state but having a value different from the reference value or values bounding the selected state. The programming operation can thus be controlled without actually reading the memory state of the cell.

**Priority Data:** US 91173197 19970815 A R; US 41020095 19950227 A R; US 7181693 19930604 A R; US 65287891 19910208 A R;

**Related Application(s):** 01 01; 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518916; 365207; 365218

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Shapiro and Shapiro

**Examiner Primary:** Fears, Terrell W.

**Assignments Reported to USPTO:**

**Recl/Frame:** 09350/0610 **Date Signed:** 19951010 **Date Recorded:** 19980728

**Assignee:** BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS  
PENNSYLVANIA 19406

**Assignor:** BRITISH TECHNOLOGY GROUP USA INC.; BTG USA INC.

**Corres. Addr:** BTG INTERNATIONAL INC. JOEL F. SPIVAK 2200 RENAISSANCE BOULEVARD  
GULPH MILLS, PA 19406

**Brief:** CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

**Legal Status:**

Date	+/-	Code	Description



MicroPatent Patent Index - an enhanced INPADOC database

19980728	( )	AS01	CHANGE OF NAME New owner name: BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD; Effective date: 19951010;
19980728	( )	AS01	CHANGE OF NAME New owner name: BRITISH TECHNOLOGY GROUP USA INC.; Effective date: 19951010;
19980728	( )	AS01	CHANGE OF NAME New owner name: BTG USA INC.; Effective date: 19980601;

**US7068542B2 20060627**  
**US2005030816A1 20050210**

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

Assignee: BTG INTERNAT INC US

Inventor(s): BANKS GERALD J US

Application No: US 94419404 A

Filing Date: 20040920

Issue/Publication Date: 20060627

**Abstract:** (ENG) <p num="0000">Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals may be dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.</p>

**Priority Data:** US 18883502 20020705 A 3; US 41020095 19950227 A 2; US 41131599 19991004 A 3; US 49313900 20000128 A B; US 73393700 20001212 A 3; US 74289003 20031223 A 3; US 89354501 20010629 A 3; US 94419404 20040920 A; US 97591997 19971121 A 3;

**Related Application(s):** 10/944194 10/742890 20031223 PENDING 10/742890 10/188835 20020705 6714455 US A 10/188835 09/893545 20010629 6434050 US A 09/893545 09/733937 20001212 6353554 US A 09/493139 09/411315 19991004 6246613 US A 09/411315 08/975919 19971121 6002614 US A; 09/733937 09/493139 20000128 ABANDONED; 08/975919 08/410200 19950227 5764571 US A

**IPC (International Class):** G11C01604; G11C01156

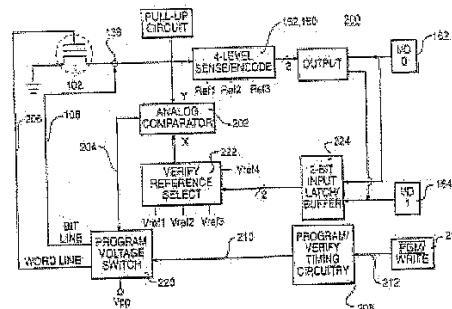
**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518529; 3651852; 36518522

**Publication Language:** ENG

**Agent(s):** Miles & Stockbridge P.C.

**Examiner Primary:** Dinh, Son T.



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**Examiner Assistant:** Nguyen, Hien

**Legal Status:** There is no Legal Status information available for this patent

**WO9927539A1 19990603**

**(ENG) MEMORY APPARATUS INCLUDING PROGRAMMABLE NON-VOLATILE MULTI-BIT MEMORY CELL, AND APPARATUS AND METHOD FOR DEMARCATING MEMORY STATES OF THE CELL**

**Assignee:** BTG USA INC US

**Inventor(s):** BANKS GERALD J

**Application No:** US 9722809 W

**Filing Date:** 19971211

**Issue/Publication Date:** 19990603

**Abstract:** On délimite les états de mémoire d'une cellule de mémoire multi-bits en générant des signaux de référence de lecture ayant des niveaux qui constituent des frontières entre les états de mémoire. Ces signaux de référence de lecture dépendent des niveaux de signaux de référence de programmation utilisés pour commander la programmation de la cellule de mémoire. La cellule de mémoire peut ainsi être programmée sans lecture de son état de mémoire au cours du processus de programmation, les marges de programmation étant assurées par la dépendance des signaux de référence de lecture par rapport aux signaux de référence de programmation. Les deux ensembles de signaux de référence peuvent être générés par des cellules de référence qui détectent les variations des caractéristiques opérationnelles de la cellule de mémoire associées à des variations de conditions du type température et tensions du système, de façon à accroître la fiabilité de lecture et de programmation de la mémoire.

**Priority Data:** US 97591997 19971121 A I;

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D2; G11C01156D4; G11C01156D

**Designated Countries:**

-----Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW

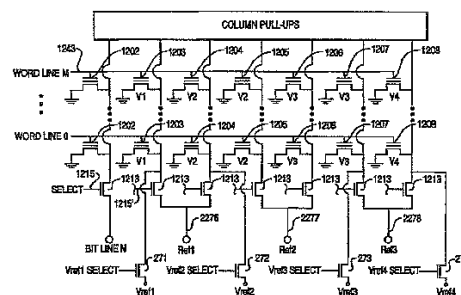
-----Regional Treaties: AM AT AZ BE BF BJ BY CF CG CH CI CM DE DK ES FI FR GA GB GH GM GN GR IE IT KE KG KZ LS LU MC MD ML MR MW NE NL PT RU SD SE SN SZ TD TG TJ TM UG ZW

**Publication Language:** ENG

**Agent(s):** SHAPIRO, Mitchell, W. Suite 1701, 1100 Wilson Boulevard, Arlington, VA 22209 US

**Legal Status:**

Date	+/-	Code	Description
19990603	(-)	AK	DESIGNATED STATES Kind code of corresponding patent document: A1; List of designated states: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW;



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19990603	(+)	AL	DESIGNATED COUNTRIES FOR REGIONAL PATENTS Kind code of corresponding patent document: A1; List of designated states: GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG;
19990804	( )	121	EP: THE EPO HAS BEEN INFORMED BY WIPO THAT EP WAS DESIGNATED IN THIS APPLICATION
19990826	( )	DFPE	REQUEST FOR PRELIMINARY EXAMINATION FILED PRIOR TO EXPIRATION OF 19TH MONTH FROM PRIORITY DATE (PCT APPLICATION FILED BEFORE 20040101)
20000323	( )	REG	REFERENCE TO NATIONAL CODE Corresponding country code for PRS Code (EP REG): DE; Corresponding EP Code 1 for PRS Code (EP REG): 8642;
20000520	( )	ENP	ENTRY INTO THE NATIONAL PHASE IN: Corresponding country code for PRS Code (EP REG): KR; Corresponding patent document: 2000 2000705519; Kind code of corresponding patent document: A;
20000520	( )	ENP	ENTRY INTO THE NATIONAL PHASE IN: Corresponding country code for PRS Code (EP REG): KR; Corresponding patent document: 2000 2000705519; Kind code of corresponding patent document: A;
20000520	(+)	WWE	WIPO INFORMATION: ENTRY INTO NATIONAL PHASE Corresponding patent document: 1020007005519; Country code of corresponding patent document: KR;
20000620	(-)	WWE	WIPO INFORMATION: ENTRY INTO NATIONAL PHASE Corresponding patent document: 1997952391; Country code of corresponding patent document: EP;
20000906	(+)	WWP	WIPO INFORMATION: PUBLISHED IN NATIONAL OFFICE Corresponding patent document: 1997952391; Country code of corresponding patent document: EP;
20010416	(+)	WWP	WIPO INFORMATION: PUBLISHED IN NATIONAL OFFICE Corresponding patent document: 1020007005519; Country code of corresponding patent document: KR;
20010521	( )	NENP	NON-ENTRY INTO THE NATIONAL PHASE IN: Corresponding country code for PRS Code (EP REG): CA;
20030130	(-)	WWW	WIPO INFORMATION: WITHDRAWN IN NATIONAL OFFICE Corresponding patent document: 1997952391; Country code of corresponding patent document: EP;
20050629	(+)	WWG	WIPO INFORMATION: GRANT IN NATIONAL OFFICE Corresponding patent document: 1020007005519; Country code of corresponding patent document: KR;



**US6002614A 19991214**

(ENG) Memory apparatus including programmable non-volatile multi-bit memory cell, and apparatus and method for demarcating memory states of the cell

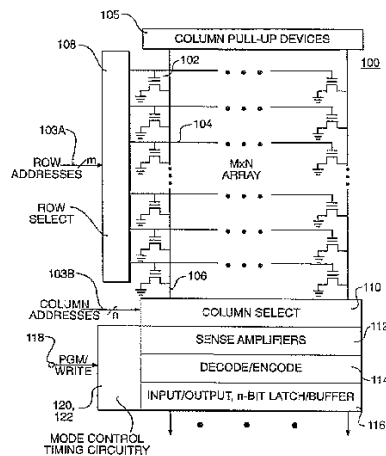
Assignee: BTG INTERNATIONAL INC US

Inventor(s): BANKS GERALD J US

Application No: US 97591997 A

Filing Date: 19971121

Issue/Publication Date: 19991214



**Abstract:** (ENG) Memory states of a multi-bit memory cell are demarcated by generating read reference signals having levels that constitute boundaries of the memory states. The read reference signals are dependent upon the levels of programming reference signals used for controlling the programming of the memory cell. The memory cell can thus be programmed without reading out its memory state during the programming process, with programming margins being assured by the dependence of the read reference signals on the programming reference signals. Both sets of reference signals may be generated by reference cells which track variations in the operating characteristics of the memory cell with changes in conditions, such as temperature and system voltages, to enhance the reliability of memory programming and readout.

**Priority Data:** US 97591997 19971121 A A; US 41020095 19950227 A A; US 7181693 19930604 A A; US 65287891 19910208 A A;

**Related Application(s):** 01 01; 01 01; 01 01 01

**IPC (International Class):** G11C01156

**ECLA (European Class):** G11C01156D; G11C01156D2; G11C01156D4

**US Class:** 36518914; 36518909

**Publication Language:** ENG

**Filing Language:** ENG

**Agent(s):** Vorys, Sater, Seymour and Pease LLP

**Examiner Primary:** Fears, Terrell W.

**Assignments Reported to USPTO:**

**Reel/Frame:** 09082/0072 **Date Signed:** 19980301 **Date Recorded:** 19980320

**Assignee:** BTG USA INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS PENNSYLVANIA 19406

**Assignor:** BANKS, GERALD J.

**Corres. Addr:** SHAPIRO AND SHAPIRO MITCHELL W. SHAPIRO 1100 WILSON BOULEVARD, SUITE 1701 ARLINGTON, VA 22209

**Brief:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

**Reel/Frame:** 09350/0610 **Date Signed:** 19951010 **Date Recorded:** 19980728

**Assignee:** BTG INTERNATIONAL INC. 2200 RENAISSANCE BOULEVARD GULPH MILLS PENNSYLVANIA 19406



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**Assignor:** BRITISH TECHNOLOGY GROUP USA INC.; BTG USA INC.

**Corres. Addr:** BTG INTERNATIONAL INC. JOEL F. SPIVAK 2200 RENAISSANCE BOULEVARD  
GULPH MILLS, PA 19406

**Brief:** CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

**Legal Status:** There is no Legal Status information available for this patent

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# USPTO Maintenance Report

Patent Bibliographic Data				01/13/2009 05:55 PM	
Patent Number:	5764571		Application Number:	08410200	
Issue Date:	06/09/1998		Filing Date:	02/27/1995	
Title:	ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY WITH N-BITS PER CELL				
Status:	12th year fee window opens: 06/09/2009			Entity:	Large
Window Opens:	06/09/2009	Surcharge Date:	12/10/2009	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:	1553	MAINTENANCE FEE DUE AT 11.5 YEARS			
Surcharge Fee Code:					
Most recent events (up to 7):	11/14/2005 Payment of Maintenance Fee, 8th Year, Large Entity. 03/05/2002 Payment of Maintenance Fee, 4th Year, Large Entity. 03/05/2002 Surcharge for Late Payment, Large Entity. 02/04/2002 Refund - Payment of Maintenance Fee, 4th Year, Large Entity. 01/02/2002 Maintenance Fee Reminder Mailed. 10/18/2001 Payor Number Assigned. 04/26/2001 Pat Hldr no Longer Claims Small Ent Stat as Small Business. --- End of Maintenance History ---				
Address for fee purposes:	COMPUTER PACKAGES, INC. 414 HUNGERFORD DRIVE ROCKVILLE, MD 20850				