

DECLARATION OF R. JACOB BAKER, Ph.D.

I, R. Jacob Baker, hereby declare as follows:

1. My name is R. Jacob Baker. My findings as set forth herein, are based on my education and background in the fields discussed below.
2. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Micron”) to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition (“Petition”) concerning U.S. Patent No. 5,764,571 (the “’571 patent”). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.
3. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

I. Education, Experience, Publications, and Awards

4. As indicated in my *curriculum vitae*, attached as **Exhibit 1**, I currently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering with Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and

1998, both at University of Idaho. I have been teaching electrical engineering since 1991.

5. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

6. As further described in my CV, I am a licensed Professional Engineer in the State of Idaho and have more than 25 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of Flash memory while at Micron. My efforts resulted in more than a dozen Flash-memory related patents. Among many other experiences, I led the development of the delay-locked loop (DLL) in the late 90s so that Micron products could transition to the DDR memory standard. I also provided technical assistance with Micron's acquisition of Photobit during 2001 and 2002. This assistance included help transitioning the manufacture of CIS products into Micron's DRAM process technology. I have worked as a consultant at other companies designing memory chips, including Sun, Oracle, and Contour Semiconductor. I have worked at other companies designing CISs, including

Aerius Photonics and Lockheed-Martin. I am currently working on the design of CISs and memory as a consultant for OmniVision.

7. I have taught courses in integrated circuit design (analog, digital, mixed-signal, etc.), linear circuits, microelectronics, communication systems, and fiber optics. As a professor, I have been the main advisor to five Doctoral students and over 50 Masters students.

8. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (three editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and co-authored, more than 75 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on over 135 granted U.S. patents in integrated circuit design including flash memory, DRAM, and CMOS image sensors.

9. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

10. I have also received the IEEE Circuits and Systems Education Award (2011), the IEEE Power Electronics Best Paper Award (2000), and I am a Fellow of the IEEE for contributions to memory circuit design.

11. In addition, I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award the two years I have been at UNLV.

12. I have also given over 50 invited talks at conferences and Universities in the areas of integrated circuit design including: AMD, Arizona State University, Beijing Jiaotong University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), École Polytechnique de Montréal, Georgia Tech, Hong Kong University of Science and Technology, Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey, ITESM (Mexico), Iowa State University, Laval University, Lehigh University, Princeton University, Temple University, University of Alabama, University of Arkansas, University of Buenos Aires (Argentina), University of Illinois, Urbana-Champaign, Utah State University, University of Nevada, Las Vegas, University of Houston, University of Idaho, University of Nevada, Reno, University of Macau, University of Toronto,

University of Utah, Yonsei University (Seoul, Korea), University of Maryland, IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), the Franklin Institute, Georgia Tech, National Semiconductor, AMI semiconductor, Micron Technology, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Tower (Israel), Foveon, ICySSS keynote, Xilinx, etc.

II. Materials Considered

13. In addition to reviewing U.S. Patent No. 5,764,571, I also reviewed and considered:

the prosecution history of the '571 patent;

U.S. Patent No. 5,394,362;

U.S. Patent No. 5,218,569;

U.S. Appl. Ser. No. 07/337,579;

U.S. Patent No. 5,172,338;

U.S. Patent No. 4,952,821;

U.S. Patent No. 5,319,348;

U.S. Patent No. 5,095,344;

U.S. Patent No. 5,218,246;

U.S. Patent No. 4,809,224;

U.S. Patent No. 5,991,517;

U.S. Patent No. 4,964,079;

“An Experimental 2-bit / Cell Storage DRAM for Macrocell or Memory-on-Logic Application” by Furuyama et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 2, April 1989;

“MACMILLAN DICTIONARY OF MICROCOMPUTING,” Third Edition (1985);

April 27, 2010, Tutorial Transcript, *MLC Flash Memory Devices and Products Containing Same*, Inv. No. 337-TA-683, (January 19, 2011) (Completed);

“Fundamentals of Digital Systems Design,” by Rhyne, 1973;

“VLSI Design Techniques for Analog and Digital Circuits,” by Geiger, Allen, and Strader, McGraw-Hill, March 1989;

“An Introduction to Analog and Digital Communications,” by Simon S. Haykin (1989);

U.S. Patent No. 4,415,992;

Japanese Patent Application Kokai No. S62-34398 (A);

U.S. Patent No. 4,449,203; and

U.S. Patent No. 5,119,330.

14. My compensation is not based on the resolution of this matter. My findings, as explained below, are based on my education, experience, and background in the fields discussed above.

III. Level of Ordinary Skill in the Art

15. In my opinion, a person of ordinary skill in the art (POSITA) at the time of the claimed invention(s) would have had a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least 2-3 years of experience in the development and use of memory devices and systems. An individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems (*e.g.*, 1-2 years).

16. I reserve the right to amend or supplement this declaration if the Board adopts a definition of a person of ordinary skill other than that described above, which may change my conclusions or analysis.

17. My opinions below explain how a POSITA would have understood the technology described in the references I have identified herein around the 1991 time period.

IV. Applicable Legal Standard

A. Claim Construction

18. I have been informed that in an *inter partes* review proceeding, the

claims of a patent are to be given their broadest reasonable meaning as they would be understood by a POSITA, consistent with the specification of the patent. I have been informed that the '571 patent will expire on June 9, 2015. I have been informed that when a patent is set to expire during the pendency of an *inter partes* review the standard for claim construction shifts from the broadest reasonable interpretation standard to the district court's *Markman* standard. Under a *Markman* standard, I have been informed that the claims of a patent are to be given their meaning as understood by a POSITA at the time of invention in light of the patent's intrinsic evidence (*e.g.*, specification and prosecution history) and, when appropriate, extrinsic evidence (*e.g.*, technical dictionaries). The constructions proposed herein are consistent with the specification and claims (*i.e.*, the intrinsic evidence) and therefore should not be affected by the standard applied.

B. Anticipation and Obviousness

19. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference.

20. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was

patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). I further have been informed that a claim is invalid under 35 U.S.C. § 102(e) if an invention described by that claim was disclosed in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

21. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to one of ordinary skill in the art, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. For purposes of my analysis, and because I know of no indication from the patent owner or others to the contrary, I have applied a date of February 8, 1991, as the date of invention in my obviousness analyses, although in many cases the same analysis would hold true even at an earlier time than February 8, 1991.

22. I have been informed that a claim can be obvious in light of a single

prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

C. Means Plus Function Terms

23. I have been informed that a claim limitation may be written in “means plus function” or “112(6)” format. I have been informed that a claim limitation using the term “means” and including functional language is presumed to invoke 35 U.S.C. § 112(6). I have been informed that a claim limitation written in the means plus function format is literally met if the element in the prior art corresponding to the means plus function limitation (i) performs the same function recited in the means plus function limitation (ii) using the same structure disclosed in the patent

specification for performing the recited function, or its statutory equivalent. A prior art structure is a statutory equivalent to a structure disclosed in the patent specification if it performs exactly the same function, in substantially the same way, to achieve substantially the same result. I understand that a structural equivalent for a means plus function limitation must have been available at the time of the issuance of the claim.

V. Background of the Technology

24. Computer memories can be classified as volatile and non-volatile. Volatile memories, such as DRAM, SRAM, SDRAM, and DDR-DRAM, only store data while powered by the system they are in, and lose the data stored therein when the power is turned off. Non-volatile memories retain their stored data even without power. Examples of non-volatile memories and memory systems include magnetic tape, magnetic and optical drives, read only memories (ROMs), electrically programmable read only memories (EPROMs), and electrically erasable programmable read-only memories (EEPROMs).

25. Flash memory technology can store one bit of data in each transistor cell of the memory, or it can be made to store more than one bit of data in each memory cell. Flash memory that stores one bit per cell is typically called single level cell or SLC memory. Flash memory that stores two bits per cell is typically called MLC, for multi-level cell memory. Flash memories have been developed

that store three bits per cell, and even four bits per cell. However, as the number of bits stored in a flash memory cell increases, the programming speed decreases, the reliability and longevity of the memory decreases, and the error rate increases.

Some of the earliest MLC flash memory patents and publications include Japanese Patent Application Kokai No. S62-34398 (A) to Kitamura; and U.S. Patent Nos. 5,095,344 to Harari and 5,172,338 to Mehrotra, Harari, et al., which were filed in the mid to late 1980s.

VI. Brief Summary of the '571 Patent

26. Generally, I understand that the '571 patent is directed to MLC devices, and more particularly to systems and techniques for reading, programming, and verifying the programming of MLC devices. *See* Ex. 1001 at Abstract, 7:9-43, 9:60-10:37. More specifically, the '571 patent is directed to an electrically alterable, non-volatile memory device. *See* Ex. 1001 at 4:21-23. The '571 patent describes electrically alterable as “electrically varying the conductivity of the channel of a floating gate FET [by applying programming pulses to the cell] to be within any one of K^n conductivity ranges The conductivity range is then sensed and encoded. This forms the basis of an n-bit EANVM memory cell.” *See* Ex. 1001 at 4:21-33. As such, an electrically alterable memory cell includes one in which programming the cell, *e.g.*, by applying programming pulses to change the conductivity of the channel of a floating gate, changes its threshold voltage and

thus can change its memory state. Non-volatile memory cells are cells that maintain their memory state even after power is removed from the memory device. *See* Ex. 1001 at 2:21-28.

27. To this end, the '571 patent describes a process for reading the current memory state of a memory cell by comparing the bit line voltage of the memory cell to each of three reference voltages that delineate between the various memory states. *See* Ex. 1001 at 7:9-8:11. The '571 patent describes this reading process in the context of a memory cell having four possible memory states, which allows the memory cell to store two bits of information. The four memory states (*i.e.*, (0,0), (1,0), (0,1), and (1,1) in two-bit form) of the memory cell are distinguished by the three reference voltages (Ref 1, Ref 2, and Ref 3), which are shown and described with reference to Figure 7.

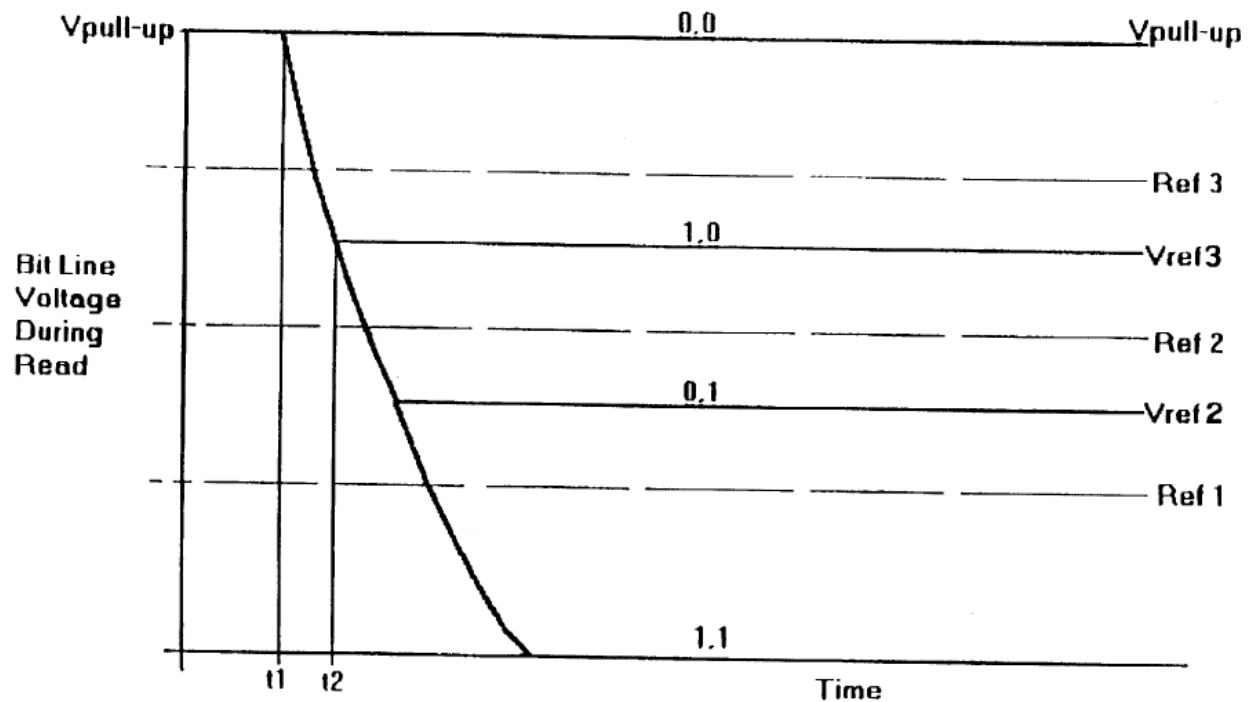


Figure 7

28. The '571 patent instructs that the Sense Amplifier 152 and Encode Logic 160, collectively described below and in Figure 8 as the 4-Level Sense/Encode circuit 152, 160 ("Read Circuit"), can determine the memory state of the cell based on the comparison results of the memory cell bit line voltage to each of the reference voltages (Ref1, Ref2, Ref3). *See* Ex. 1001 at 7:15-43.

29. More specifically, the '571 patent describes that the Read Circuit uses three sense amplifiers to make the necessary three comparisons of the reference voltages to the bit line voltage. The three sense amplifiers 154, 156 and 158 are shown in Figure 6. *See id.*

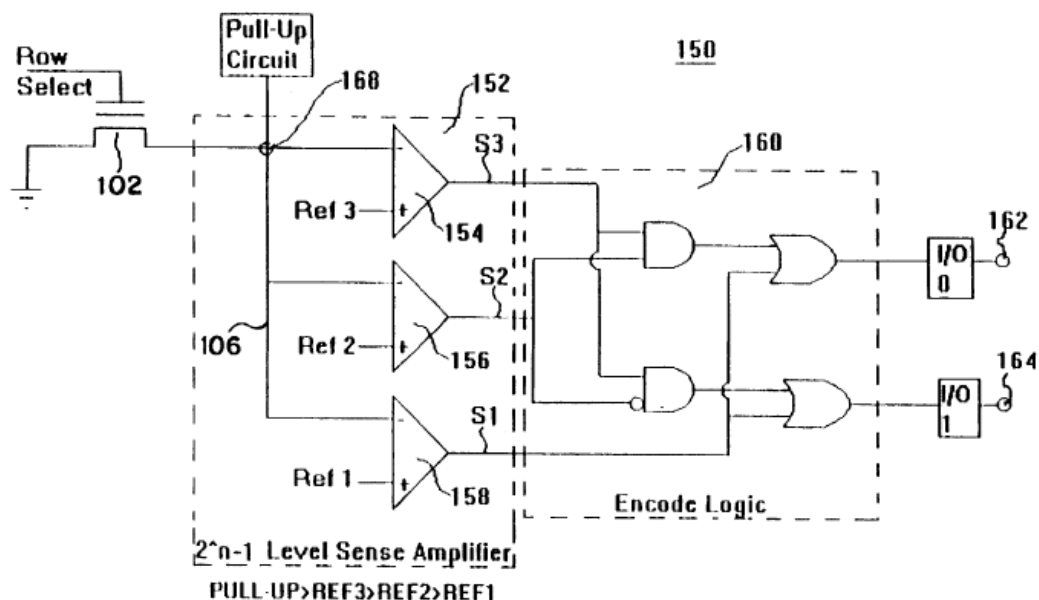


Figure 6

30. Each sense amplifier compares the bit line voltage of the memory cell from the memory cell's output terminal 168 to the sense amplifier's respective reference voltage. *See id.* For example, sense amplifier 154 compares the bit line voltage to reference voltage Ref 3, sense amplifier 156 compares the bit line voltage to reference voltage Ref 2, and sense amplifier 158 compares the bit line voltage to reference voltage Ref 1. The encode logic 160 uses the outputs/comparison results from the three sense amplifiers to encode the results into two-bit form representing the current memory state of the memory cell, *e.g.*, based on the encode logic shown at col. 7, lines 30-38 of the '571 patent.

31. Generally, the '571 patent describes the programming and verification of a memory cell as an iterative process. *See id.* at 10:14-36. Each iteration of the

process includes a programming pulse applied to the memory cell followed by a check to determine if the last programming pulse placed the memory cell into its desired memory state, as further described below. *See id.* If the check indicates that the memory cell is correctly programmed to its desired memory state then programming ends. *See id.* However, if the check indicates that the cell is not correctly programmed then additional programming and verification steps are carried out until the cell is determined to be correctly programmed. *See id.*

32. Figure 11 illustrates an example iterative programming and verification process of the '571 patent.

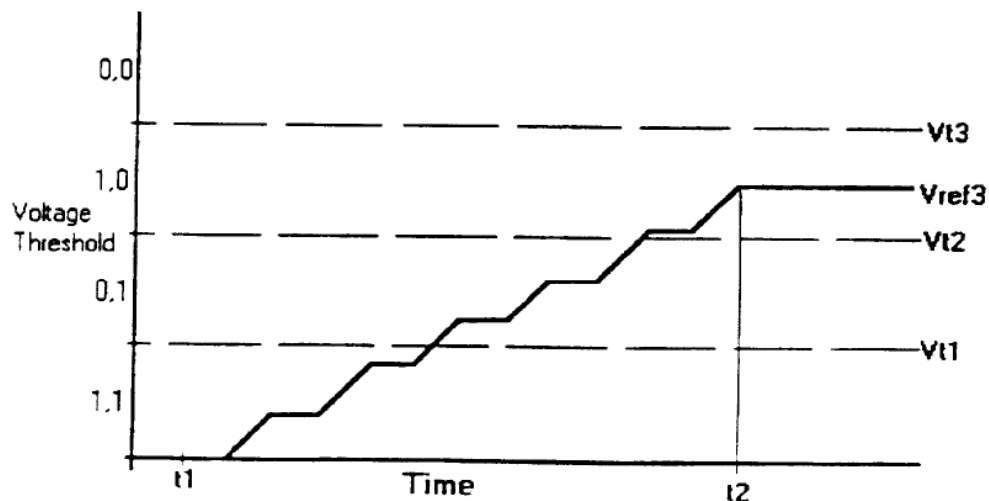


Figure 11

33. In this example, the memory cell is being programmed from an erased (1,1) memory state to a desired (1,0) memory state through a series of programming pulses represented as stair steps up the voltage threshold y-axis. *See*

id. Each stair step corresponds to a programming pulse increasing the voltage of the memory cell (*e.g.*, threshold voltage or bit line voltage, which is representative of the threshold voltage). *See id.* After each programming pulse (*e.g.*, stair step), a verification process determines if the memory cell is in its desired memory state. If not, programming continues. *See id.*

34. The verification process determines if the memory cell is in its desired memory state by comparing the memory cell's bit line voltage, which is representative of the cell's threshold voltage¹ and increases after each programming pulse, to a reference voltage representing the desired memory state. *See id.* Here in Figure 11, the reference voltage for memory state (1,0) is Vref3, as Vref3 is in the voltage window defining state (1,0), *i.e.*, the voltage window defined by Vt2 and Vt3. *See id.* Each memory state has a different reference voltage particularly representing that memory state. *See id.* at 8:26-40. For

¹ A memory cell's threshold voltage cannot readily be measured directly. There are known (or determinable) relationships between a memory cell's threshold voltage and the signal on its bit line. The bit line signal is a representation of, but different from, the threshold voltage, and can be used as a proxy for the threshold voltage in determining the current memory state of the cell. This is applicable to the '571 patent, Kitamura and Mehrotra.

example, a reference voltage Vref2 representing memory state (0,1) would be in the voltage window defined by Vt1 and Vt2. *See id.* Thus if the desired memory state was (0,1), the verification process would compare the memory cell's bit line voltage to Vref2 to determine if the memory cell has been correctly programmed.

35. The '571 patent further describes the programming and verification process with respect to Figure 8.

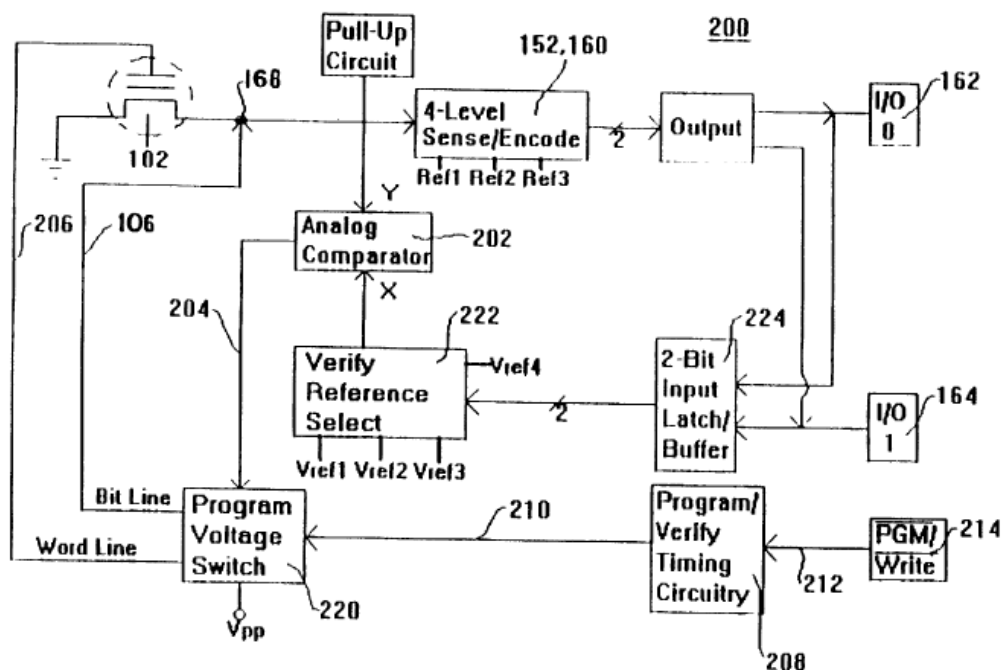


Figure 8

36. The '571 patent describes that the verification process can be performed through either analog or digital comparators. In one implementation, the '571 patent describes that the verification process can be performed with use of the Verify Reference Select device 222 and the Analog Comparator 202. *See Ex. 1001 at 9:64-65, 8:64-9:18, 11:49-58.* In this implementation, the Analog

Comparator 202 compares the bit line voltage of the memory cell, representing the current memory state of the cell, with the reference voltage, representing the desired memory state of the cell, to determine when the cell is correctly programmed. *See id.* The Comparator 202 receives the current memory state of the cell from the output terminal 168 in the form of an analog bit line voltage/signal, and receives the reference voltage corresponding to desired memory state from the Verify Reference Select device 222 in the form of an analog signal. *See id.*

37. The Verify Reference Select device 222 determines which reference voltage to select, *e.g.*, Vref1, Vref2, Vref3 or Vref4, based on the output from the 2-Bit Input Latch/Buffer 224. *See id.* The 2-Bit Input Latch/Buffer 224, in turn, receives the inputs corresponding to the input information/desired memory state from I/O terminals 162 and 164. *See id.* Thus the Verify Reference Select device 222 selects the reference signal, to pass to the Comparator 202, corresponding to the input information/desired memory state. It's worthy to note that the process of using a digital input to select, and output, an analog voltage is often called digital-to-analog conversion which can be abbreviated as DAC or D/A.

38. When the Comparator 202 determines that the bit line voltage of the memory cell exceeds the reference signal corresponding to the desired memory

state, the Comparator 202 generates an output signal to disable the Program Voltage Switch 220,² thereby ending programming. *See id.* at 9:3-7.

39. As mentioned above, in addition to an analog implementation, the '571 patent also describes a digital implementation of the Comparator 202. *See id.* at 11:49-58; 9:64-65. More particularly, the '571 patent instructs that in this digital implementation, the digital comparator uses the digital, encoded data, representing the current memory state of the memory cell, from the encode circuitry 160. *See id.* at 11:49-58. The encode circuitry 160 receives its input from the sense amplifier 152. *See id.* The input into the digital comparator for the current memory state of the memory cell is a digital signal representing the two-bits from the sense/encode circuitry 152, 160, which is analogous information to the bit line voltage from output terminal 168 used in the analog comparator implementation.

40. The other input to the digital comparator, representing the desired memory state and analogous to the selected reference voltage in the analog implementation, *e.g.*, Vref1, Vref2, Vref3 or Vref4, is an encoded, digital voltage from the Verify Reference Select device 222. *See id.* This encoded, digital voltage is based on the output of the 2-Bit Input Latch/Buffer 224 and represents

² The Program Voltage Switch 220 and the Program/Verify Timing Circuit 208 manage the programming pulses. *See id.* at 8:50-57.

the desired memory state/input information. *See id.* The '571 patent notes that, beyond the above changes, the function of the comparator remains the same. *See id.*

41. Notably, the '571 patent describes no other device(s) or process(es) that manipulate or change the output of the Verify Reference Select device 222 into the digital signal needed by the digital comparator or that otherwise select which digital signal, corresponding to the input information, to send to the digital comparator. Thus a POSITA would understand that in this digital comparator implementation the Verify Reference Select device 222 selects the particular one digital signal corresponding to the desired memory state to provide to the digital comparator.

42. The encoded, digital signal from the Verify Reference Select device 222, representing the desired memory state of the cell, could be selected and provided to the digital comparator in several well-known ways. For example, if the output of the 2-Bit Input Latch/Buffer 224 received by the Verify Reference Select device 222 is a (1,0), representing the third of four possible memory states, and the memory device uses a scheme where a 5 Volt signal corresponds to a “1” bit and a 0 Volt signal corresponds to a “0” bit, then the Verify Reference Select

device 222 would select a 5 Volt, 0 Volt reference signal³ to represent the (1,0) memory state.

43. Conversely, if the output of the 2-Bit Input Latch/Buffer 224 was (1,1), (0,1) or (0,0) then the Verify Reference Select device 222 would respectively select a 5 Volt, 5 Volt signal; a 0 Volt, 5 Volt signal; or a 0 Volt, 0 Volt signal to send to the comparator. Thus the reference signals corresponding to the various memory states are predetermined, *e.g.*, based on number of desired memory states and the encoding scheme, and the Verify Reference Select device 222 selects the one of these reference signals that corresponds to the desired memory state consistent with the output of the 2-Bit Input Latch/Buffer 224. Unless the memory device system parameters change, the reference signals will not change. Based on

³ Based on the specific design of the circuit, a POSITA at the time of the '571 patent invention would have understood that the Verify Reference Select device 222 could send the reference signal in serial or parallel manner. For example, for the 5 Volt, 0 Volt reference signal the Verify Reference Select device 222 could serially send a 5 Volt waveform followed by a 0 Volt waveform to the comparator as the digitally encoded (1,0) reference signal. Likewise, the Verify Reference Select device 222 could send in parallel the reference signal to the comparator via a 5 Volt waveform on a first data line and a 0 Volt waveform on a second data line.

the above-described disclosure of the '571 patent, the claims of the '571 patent, and for the reasons presented below in Section VII, it is my opinion that a POSITA would understand that the '571 patent's claims cover both digital and analog implementations as described above.

44. As depicted in Figure 8 above, the 4-Level Sense/Encode circuit 152, 160 and the Verify Reference Select device 222 are shown as separate components/functions. However, the '571 patent describes that the 4-Level Sense/Encode circuit 152, 160 and the Verify Reference Select circuit 222 can be “coupled together to . . . time share common circuit components.” *See id.* at 9:19-24. Such coupling would allow the program/verify process to share components and function with the read process.

VII. Claim Terms of the '571 Patent

A. Reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information

45. Claim 1 recites a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states.” I understand that a claim limitation using the term “means” and including functional language is presumed to invoke 35 U.S.C. § 112(6) and be a means-plus-function limitation. This limitation includes the term “means” and

functional language, *e.g.*, selecting one of a plurality of reference voltages in accordance with said input information. Therefore I understand that this limitation is presumed to be a means-plus-function limitation.

46. As such, I understand that the '571 patent must disclose a structure to perform the recited function, which, as mentioned above, could be in the context of either an analog or digital implementation. The '571 patent describes that the “voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 168 with the selected verify reference voltage from the verify reference voltage select circuit 222.” *See id.* at 8:66-9:3. “The verify reference voltage select circuit 222 analog output voltage X is determined by decoding the output of the n-bit input latch/buffer 224 (n=2 in the illustrative form).” *See id.* at 9:11-14.

47. “The verify reference voltage select 222 would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed.” *See id.* at 11:54-57. “For the write mode of operation, a verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202.” *See id.* at 8:26-29. Figure 8 also shows the Verify Reference Select circuit 222 provides the reference signal “X” to the Comparator 202. Thus I understand

that the corresponding structure for this limitation is the Verify Reference Select circuit 222.

48. Additionally, the '571 patent describes an analog output as a “signal.” *See* Ex. 1001 at 8:26-29 (“verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202”). The '571 patent also describes a “signal” in terms of a digital signal (*e.g.*, a “low logic level state” signal). *See* Ex. 1001 at 10:17-19 (“A **low logic level state** of the PGM/Write **signal** on signal line 212 enables the timing circuit 208.”) (emphasis added).

49. As noted above, the '571 patent describes that the Verify Reference Select circuit 222 can select and provide analog or digital reference signals to the comparator, depending on the particular implementation of the comparator, *i.e.*, analog or digital. In addition to the explicit disclosure teaching that the reference voltage can be an analog signal, as shown above, the '571 patent also specifically instructs—in the digital implementation context—that the Verify Reference Select circuit 222 could provide a digital voltage reference signal to the comparator. *See id.* at 11:54-55 (the “verify reference voltage selection [circuit] 222 would provide the voltage to be encoded with the input [information]” to the comparator). As such, a POSITA would understand that “selecting one of a plurality of reference

voltages” includes selecting reference voltages in the digital or analog context as both analog and digital signals can be represented through voltages.

50. A POSITA would have interpreted this feature to be broad enough to include and be met by a device or process that takes input information (*e.g.*, in an *n*-bit form) and selects, for a given cell’s program/verify cycle, a reference voltage from multiple reference voltages such that the selected reference voltage uniquely represents the input information.⁴ The reference voltage provided by the reference voltage selecting means can be an analog voltage or it can be a digital voltage. Reference voltage selection in digital form would include selecting a reference voltage in accordance with the input information, *e.g.*, for (1,1) two-bit information input, selecting for the reference voltage a 5 Volt, 5 Volt encoded voltage waveform representing the (1,1) input information.

⁴ I understand that when a patent is set to expire during the pendency of an *inter partes* review then the standard for claim construction shifts from the broadest reasonable interpretation standard to the district court’s *Markman* standard. The construction I propose is consistent with the specification and claims (what I understand is commonly referred to as the “intrinsic evidence”) and therefore should not be affected by the standard applied.

B. A selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed

51. Several claims recite this or a substantially similar limitation, including claims 9, 12, and 30. For the reasons presented in Section VII(A), a POSITA would have interpreted this feature to be broad enough to include and be met by a device or process, that takes input information (*e.g.*, in an *n*-bit form) and selects, for a given cell's program/verify cycle, a reference voltage from multiple reference voltages such that the selected reference voltage uniquely represents the input information. The reference voltage provided by the reference voltage selecting means can be an analog voltage or it can be a digital voltage. Reference voltage selection in digital form would include selecting a reference voltage in accordance with the input information, *e.g.*, for (1,1) two-bit information input, selecting for the reference voltage a 5 Volt, 5 Volt encoded voltage waveform representing the (1,1) input information.

C. Selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed

52. Several claims recite this or a substantially similar limitation, including claims 42 and 45. For the reasons presented in Section VII(A), a

POSITA would have interpreted this feature to be broad enough to include, and be met by, a process that takes input information (*e.g.*, in an n-bit form) and selects, for a given cell's program/verify cycle, a reference voltage from multiple reference voltages such that the selected reference voltage uniquely represents the input information. The reference voltage provided by the reference voltage selecting means can be an analog voltage or it can be a digital voltage. Reference voltage selection in digital form would include selecting a reference voltage in accordance with the input information, *e.g.*, for (1,1) two-bit information input, selecting for the reference voltage a 5 Volt, 5 Volt encoded voltage waveform representing the (1,1) input information.

D. Reference voltage(s) / Reference signal(s)

53. The '571 patent discloses that the reference voltages/signals, from the limitations described above from Sections VII(A)-(C), can be either digital or analog signals. For example, in the analog context, the '571 patent describes that the “verify reference voltage select circuit 222 provides an **analog voltage reference level signal X** to one input terminal of an analog comparator 202.” *See* Ex. 1001 at 8:26-29 (emphasis added). In the digital context, the '571 patent discloses that the reference voltage can be an encoded digital signal, as described in connection with the implementation of a digital comparator. *See id.* at 11:50-56 (the “verify reference voltage select [circuit] 222 would provide **the voltage to be**

encoded with the input coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed.”) (emphasis added).

54. In the digital context, the ’571 patent describes no other device(s) or process(es) that change the reference signal selected by the verify reference voltage select circuit 222, which should be in an encoded, digital form for use by the digital comparator. In the digital context, for example, each of the “plurality of reference voltages” could be voltage signals of 0 Volts, 0 Volts; 0 Volts, 5 Volts; 5 Volts, 0 Volts; and 5 Volts, 5 Volts. Each of these voltage signals would correspond to a different memory state, *e.g.*, (0,0), (0,1), (1,0), and (1,1).

55. As noted above, the ’571 patent describes an analog output as a “signal.” *See* Ex. 1001 at 8:26-29 (“verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202”) (emphasis added). Further, the ’571 patent also describes a “signal” as a digital signal. *See* Ex. 1001 at 10:17-19 (“A low logic level state of the PGM/Write signal on signal line 212 enables the timing circuit 208.”). Thus the ’571 patent describes that the selected reference voltage(s)/reference signal(s) can be either in either analog or digital form.

56. The notion that a signal or voltage can be either analog or digital is supported by literature that would have been available to a POSITA around 1991. For example, the 1985’s MacMillan Dictionary of MicroComputing defines a

“signal” as “[a] visible, audible, or other conveyor of information” and as “[a] detectable impulse (voltage, current, magnetic field, or light impulse) by which information is communicated through an electronic or optical means, or over wire, cable, microwave, or laser beams.” *See* Ex. 1009 at page 5. MacMillan defines a digital “bit” as “1. Most commonly, a unit of information equalling [sic] one binary decision, or the designation of one of two possible and equally likely values or states. It is usually conveyed as a 1 or 0 of anything that can be used to store or convey information (such as 1 or 0, yes or no). . . . 3. A single pulse in a group of pulses.” *See id.* at page 4. Clearly, a POSITA in 1991 would understand that both digital and analog input(s)/output(s) are signals, as each falls under the signal’s “conveyor of information” definition, and that a signal can be in a voltage form, as a signal is defined as including a voltage impulse.

57. Further, the specification of the ’571 patent does not make any distinction between the terms “reference signal(s)” and “reference voltage(s).” *See* Ex. 1001 at Abstract (“Programming of the cell is verified by selecting a reference signal corresponding to the information to be stored and comparing a signal of the cell with the selected reference signal.”), 8:66-9:3 (“The voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 168 with the selected verify reference voltage from the verify reference voltage select circuit 222.”).

58. As such⁵, a person of ordinary skill in the art would have interpreted this feature to be broad enough to include and be met by either a digital reference voltage/signal or an analog reference voltage/signal.

VIII. Claimed Subject Matter of the '571 Patent Disclosed by Prior Art

59. In this section, I will compare the '571 patent claims with certain prior art references that disclose and/or render obvious the subject matter claimed by the '571 patent.

60. I am informed that Kitamura, Japanese Unexamined Patent Application Publication No. S62-34398, qualifies as prior art under 35 U.S.C. § 102(b). Specifically, I am informed that the publication date of Kitamura (Ex. 1010) is February 14, 1987, and that Kitamura was filed on August 8, 1985. I am informed that both Kitamura's publication date and priority date predate by more than one year the earliest priority date of the '571 patent (February 8, 1991).

⁵ I understand that when a patent is set to expire during the pendency of an *inter partes* review then the standard for claim construction shifts from the broadest reasonable interpretation standard to the district court's *Markman* standard. The construction I propose is consistent with the specification and claims (what I understand is commonly referred to as the "intrinsic evidence") and therefore should not be affected by the standard applied.

61. I am informed that Mehrotra, U.S. Patent No. 5,172,338, qualifies as prior art under 35 U.S.C. § 102(e). Specifically, I am informed that the filing date of Mehrotra (Ex. 1004) is April 11, 1990, and that Mehrotra claims priority to and is a continuation-in-part of U.S. Appl. Ser. No. 07/337,579 filed on April 13, 1989⁶. I am informed that both Mehrotra's filing date (April 11, 1990) and priority date (April 13, 1989) predate the earliest priority date of the '571 patent (February 8, 1991).

62. I am informed that Harari, U.S. Patent No. 5,095,344, qualifies as prior art under 35 U.S.C. § 102(e). Specifically, I am informed that the filing date of Harari (Ex. 1014) is June 8, 1988, and thus Harari's filing date (June 8, 1988) pre-dates the earliest priority date of the '571 patent (February 8, 1991).

63. I am informed that Kokubun, U.S. Patent No. 4,952,821, qualifies as prior art under 35 U.S.C. § 102(e) and/or 102(a). Specifically, I am informed that the filing date of Kokubun (Ex. 1005) is June 13, 1988, and that Kokubun claims priority to Japanese Appl. No. 62-145186 filed on June 12, 1987. Kokubun's filing date (June 13, 1988) and claimed priority date (June 12, 1987) predate the earliest

⁶ I am informed that U.S. Appl. Ser. No. 07/337,579 fully supports the disclosures of Mehrotra relied on in the Petition thereby entitling Mehrotra to the priority date of April 13, 1989.

priority date of the '571 patent (February 8, 1991). In addition, I am informed that Kokubun was patented (August 28, 1990) before the earliest priority date of the '571 patent (February 8, 1991).

64. I am informed that Lee, U.S. Patent No. 5,319,348, qualifies as prior art under 35 U.S.C. § 102(e). Specifically, I am informed that the priority date of Lee (Ex. 1006) is September 14, 1990 and that Lee's priority date (September 14, 1990) pre-dates the earliest priority date of the '571 patent (February 8, 1991).

A. All Challenged Claims are Obvious in View of Kitamura

65. Kitamura (Japanese Unexamined Patent Application Publication No. S62-34398 having a filing date of August 8, 1985) describes a programmable (*e.g.*, electrically alterable), multi-bit per cell, non-volatile memory device. *See* Ex. 1010 at ¶¶ [01], [05]-[08], [12]. Specifically, Kitamura describes a two-bit (*i.e.*, four memory state), non-volatile memory cell that is programmed by iteratively applying writing/programming pulses to the memory cell until the output voltage (V_o) on its bit line, which represents the cell's threshold voltage, is raised to a level that exceeds a reference voltage representing the desired memory state. *See* Ex. 1010 at ¶¶ [05]-[08].

66. Like the '571 patent, Kitamura describes a two-bit, four memory state memory cell and processes to read, program and verify the programming of the memory cell. *See* Ex. 1010 at ¶¶ [01], [05]-[12]. The structure and operation of

the Kitamura memory device can be described with reference to Kitamura's Fig. 1.

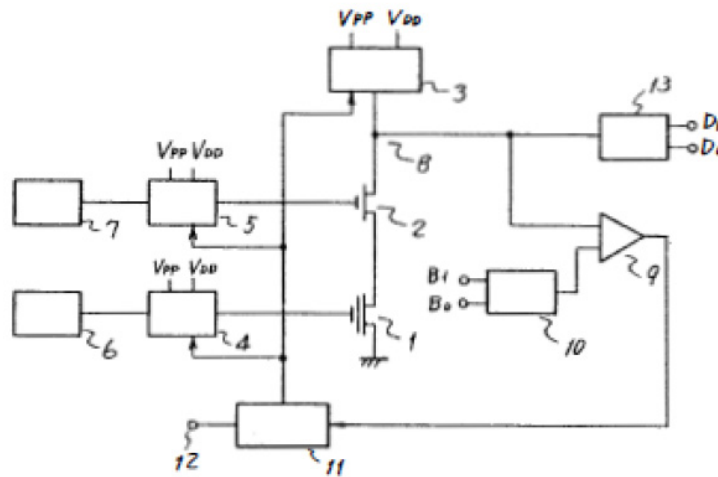


FIG. 1

- | | |
|--------------------------------|---|
| 1 floating gate MOS transistor | 9 comparator |
| 2 MOS transistor 2 | 10 D/A conversion circuit |
| 3 load circuit | 11 read/write switching signal generation circuit |
| 4, 5 driver circuit | 12 mode switching terminal |
| 6, 7 address decoder | 13 A/D conversion circuit |

67. Kitamura's memory cell 1 can be read from read point 8, the bit line of memory cell 1⁷, through transistor 2 when transistor 2 is turned on and acts as a

⁷ Kitamura's bit line is connected to the drain of the memory cell 1. It was well known by a POSITA at the effective filing date of the '571 patent that a memory cell's memory state could be determined based on the signal on the memory cell's bit line. See Ex. 1014 at 25:64-26:17; Figure 11e.

direct connection.⁸ *See* Ex. 1010 at ¶ [07] (“8 is a read point from the memory cell 1”). The analog signal (*e.g.*, voltage) on the memory cell’s bit line is representative of its current memory state (as determined by the cell’s threshold voltage). *See* Ex. 1010 at ¶ [09] (“Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3.”). Fig. 3 shows the relationship between the memory cell 1’s bit line voltage at read point 8 (V_O) and its threshold voltage (V_T).

68. Continuing, Kitamura describes memory cell 1 can be read at read point 8 by the comparator 9, during the data read/write process (programming and verification process), as well as by the A/D conversion circuit 13. *See* Ex. 1010 at

⁸ To “read” memory cell 1, Kitamura describes that memory cell 1 is selected through address decoders 6 and 7 and a read mode signal is provided to switching terminal 12, which causes read/write switching signal generation circuit 11 to output read/write signals. These signals cause driver circuits 4 and 5 to provide corresponding read signals (V_{DD}) to memory cell 1 and transistor 2 and cause load circuit 3 to couple a read signal (V_{DD}) to the memory cell 1 on its bit line. *See* Ex. 1010 at ¶¶ [07], [08], [10]. This sequence enables the memory cell’s memory state to be read at read point 8. *See id.*

¶¶ [07], [08], [10]. When data is read the A/D conversion circuit 13, in turn, converts the analog bit line voltage into a two-bit digital output, D₀ and D₁, which represents the current memory state of the memory cell in digital format (where D₀ and D₁ collectively represent one of the four possible memory states). *See id.*

69. As with the '571 patent, Kitamura discloses an iterative programming and verification process. *See* Ex. 1010 at ¶¶ [06], [14] (a “memory element whose characteristic is continuously varied by writing; a circuit that alternately switches between a write mode and a read mode at regular time intervals; a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result.”).

70. Namely, Kitamura describes a repeating cycle of applying a programming/writing pulse to the memory cell 1, which changes the threshold voltage of the floating gate memory cell 1 (by changing its channel conductivity) and then comparing the bit line voltage⁹ of the memory cell 1 to a voltage corresponding to the desired memory state. *See* Ex. 1010 at ¶¶ [06]-[10], [13],

⁹ As noted above, the bit line signal is representative of the memory cell's threshold voltage and thus its current memory state.

[14]. When the comparison indicates that the memory cell is correctly programmed to the desired memory state, programming ends. *See id.*

71. More particularly, for a programming step in the above-described iterative programming and verification process, the address decoders 6 and 7 select memory cell 1 and a writing signal is provided to switching terminal 12. *See* Ex. 1010 at ¶¶ [07]-[08]. Switching terminal 12 then causes the read/write switching signal generation circuit 11 to output read/write signals that cause driver circuits 4 and 5 to provide corresponding write signals (*e.g.*, V_{PP}) to memory cell 1 and transistor 2 and cause load circuit 3 to couple a writing signal (V_{PP}) to the memory cell 1 on its bit line.¹⁰ *See* Ex. 1010 at ¶¶ [06]-[09]. Although, the '571 patent describes the Program Voltage Switch 220 device as providing programming pulses, it would be obvious to a POSITA to collectively use, for example, the read/write switching signal generation circuit 11, driver circuit 4, and load circuit 3 to perform a similar operation because doing so would result in the predictable (and described outcome in Kitamura and the '571 patent) of facilitating the programming the memory cell, which is a collective aim of the signal generation circuit 11, driver circuit 4, and load circuit 3 from Kitamura and the aim of the

¹⁰ This process allows the memory cell to be written to, and is similar to the programming process of the '571 patent.

'571 patent's Program Voltage Switch 220. Each additional programming/writing pulse from the driver circuit 4 raises the memory cell 1's threshold voltage as depicted in Fig. 2, with the threshold voltage (V_T) represented on the y-axis and time (t) represented on the x-axis. *See* Ex. 1010 at ¶¶ [09]-[10], [14].¹¹ Because the level of the threshold voltage defines the memory state of the cell 1, changing the threshold voltage level can change the memory state of the cell 1.

¹¹ Kitamura describes that increasing the duration of the programming/writing pulse applied to the memory cell (as opposed or in addition to increasing the magnitude of the pulse) increases the threshold voltage. *See* Ex. 1010 at ¶ [09] (“The relation between the write time t of the memory cell 1 and the threshold voltage V_T of the memory cell 1, which is given by the integrated value of the write period, is the relation shown in FIG. 2 under constant voltage conditions, and V_T rises as the write period lengthens.”)

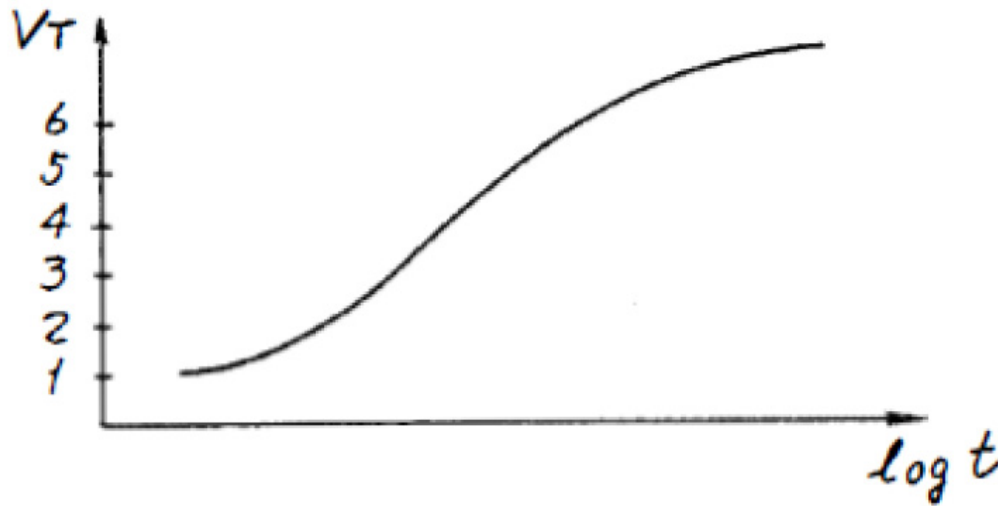


FIG. 2

72. After each programming/writing pulse, the comparator 9 verifies whether the last programming/writing pulse placed the memory cell 1 into the desired memory state. *See* Ex. 1010 at ¶¶ [09], [14]. To that end, the comparator 9 reads the bit line voltage of memory cell 1 from read point 8, which represents the current memory state of the cell 1, and compares that read point 8 voltage (V_O) to the output voltage of the D/A conversion circuit 10, which represents the desired memory state of the memory cell 1. *See id.*

73. If the comparator's output indicates that V_O exceeds the D/A conversion circuit 10 output voltage then the memory cell is determined to be correctly programmed to its desired memory state and the comparator's output causes the read/write switching signal generation circuit 11 to stop further programming. *See id.* ("Therefore, the V_O at this point is a voltage that

corresponds to the input digital signals B_1 and B_2 .”¹². If V_O does not exceed the D/A conversion circuit 10 output voltage then another programming/writing pulse will be applied and the iterative programming and verification process continues until the cell is correctly programmed. *See id.*

74. To provide the signal representative of the desired memory state, the D/A conversion circuit 10 (*i.e.*, digital-to-analog converter) takes the digital input information bits B_0 and B_1 , defining the desired memory state for the cell 1, and converts them into an analog value by selecting the analog signal that corresponds to the digital input information. *See* Ex. 1010 at ¶ [09]. Input information bits B_0 and B_1 can represent four distinct values and thus define four distinct memory states. Table 1 shows example inputs and outputs of the D/A conversion circuit 10. In this example, 1 Least Significant Bit (LSB) is 1 V. This is the voltage change between adjacent memory states. There is a 1/2 LSB level difference between the D/A conversion circuit 10 output voltage and the minimum/maximum A/D conversion circuit 13 input voltage. *See* Ex. 1010 at ¶ [11]. The “A/D Input Voltage Range” defines the range of analog voltages interpreted by the A/D conversion circuit 13 to be in a particular memory state. Kitamura describes that

¹² This appears to be a typographical error in paragraph nine and should instead refer to B_0 and B_1 .

the output of the D/A conversion circuit 10 is 1/2 LSB different from the borders of the memory state voltage ranges of the A/D conversion circuit 13 to place the respective outputs of the D/A conversion circuit 10 in the middle of the memory state voltage ranges of the A/D conversion circuit 13. *See id.* It is advantageous (and would have been well known to a POSITA at the effective filing date of the '571 patent) to configure the output values of the D/A conversion circuit 10 (*e.g.*, reference voltage signals) to be towards the middle of these ranges used to read the current state of the memory cell to reduce false reads by increasing the margining error between true and false reads. *See* Exhibit 1004 at 21:27-31.

B₀, B₁	D/A Output Voltage	Memory State	A/D Input Voltage Range
1, 1	0.5 Volts	1	0 to 1 Volts
0, 1	1.5 Volts	2	1 to 2 Volts
1, 0	2.5 Volts	3	2 to 3 Volts
0, 0	3.5 Volts	4	3 to 4 Volts

Table 1

75. In the example in Table 1, the reference voltages output by the D/A conversion circuit 10 to define memory states 1, 2, 3 and 4, respectively, are 0.5, 1.5, 2.5, and 3.5 Volts. For example, if the input information indicates that the desired memory state is 3 (B₀,B₁ = 1,0), the D/A would output 2.5 Volts to the comparator 9. The comparator 9 in turn would use 2.5 Volts to compare with the

read point 8 (V_o) voltage signal to determine if the cell 1 is correctly programmed to memory state 3.

76. Although the example in Table 1 is based on a linear D/A conversion circuit 10 (because the analog signal output voltages are linearly spaced at 1 Volt increments), non-linear (*e.g.*, 0.5, 1.1, 2.1 and 3.5 Volt output signals) and random D/A conversion circuits could also be used in Kitamura. For example, because of process or application strictures, the threshold voltages (or ranges) defining the memory states may be non-linearly spaced. This non-linearity, for example, may be the result of the threshold voltage not changing linearly with programming time. Non-linear and random D/A conversion circuits were well known in the art at the time of the '571 patent's effective filing date, and it would have been obvious to a POSITA to use such D/A conversion circuits in the memory device described by Kitamura to accommodate process or application requirements. *See* Exhibit 1013 at pages 5-11.

77. As noted above, the D/A conversion circuit 10 takes the digital input information bits B_0 and B_1 and converts them into an analog value by selecting the analog signal that corresponds to the digital input information. An illustrative selection process is described below with reference to the D/A conversion circuit of Exhibit Fig. A. *See* Exhibit 1012 at pages 15-17.

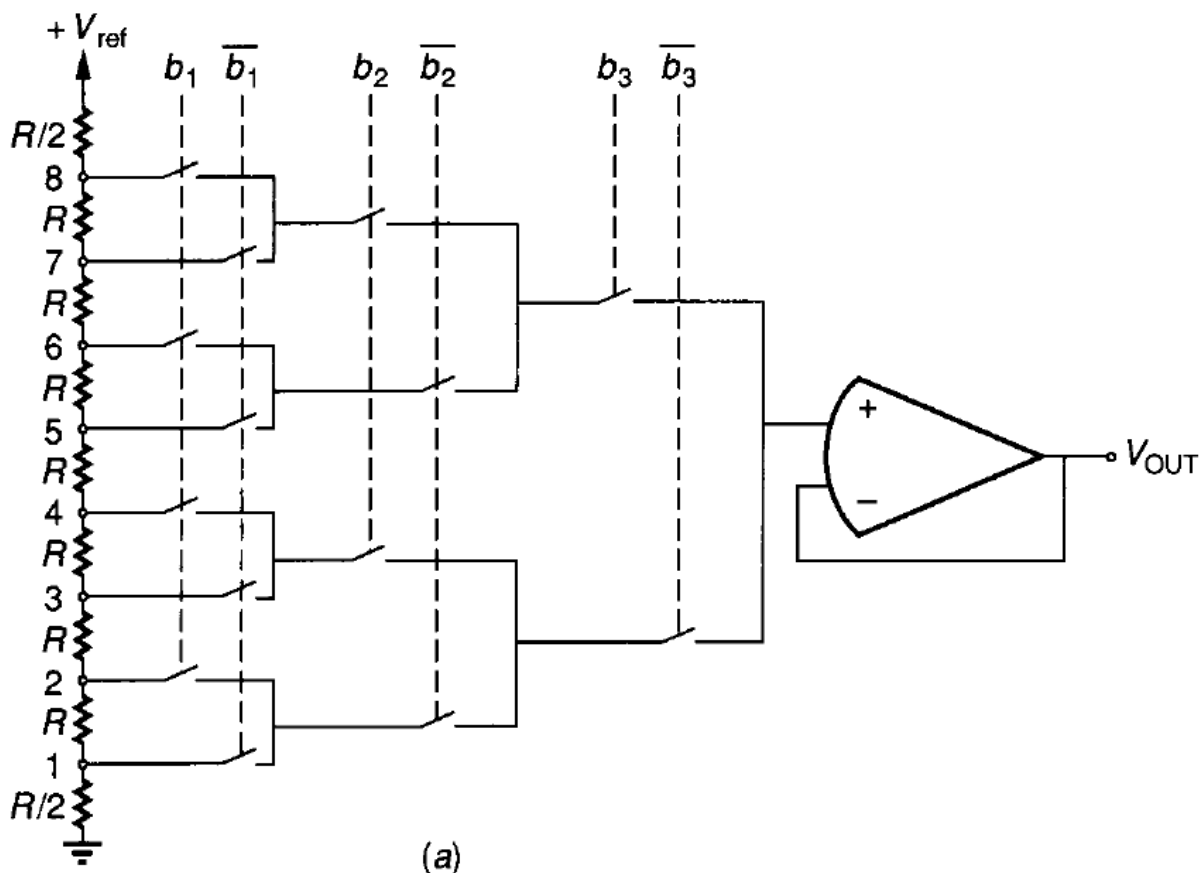


Exhibit Figure A

78. This figure depicts a three-bit (b_1 , b_2 and b_3) D/A conversion circuit. The values of these three bits would correspond to input information in Kitamura and the '571 patent (although three bits allow eight memory states as opposed to the two bits and four memory states of Kitamura). The eight possible values from

the set of three bits allow eight different voltage signals to be selected and output.¹³ *See id.* (“Each tap is connected to a switching tree whose switches are controlled by the bits of the digital word. If the i th bit is 1, then the switches controlled by b_i are closed. If the i th bit is 0, then the switches controlled by $\overline{b_i}$ are closed.”). Thus a controller in the D/A conversion circuit controls which switches to open or close (based on the input bits) to select a corresponding analog output voltage signal. The corresponding analog output voltage signals (*e.g.*, reference voltages) for the various input information possibilities can be readily set (or changed) by selecting (or changing) the values of the resistors (“R”) in the D/A conversion circuit and the value of V_{ref} .¹⁴

79. These possible output voltage signals are illustrated in Exhibit Fig. B. *See* Exhibit 1012 at page 16. In Kitamura, the two-bit information fed into the D/A conversion circuit 10 would analogously allow the D/A conversion circuit 10 to select among four output voltage signals. In this way the D/A conversion circuit

¹³ Although Kitamura describes two input information bits allowing for four possible memory states, the reference signal selection process in Kitamura is analogous to that described with reference to Exhibit Figures A and B.

¹⁴ Changing these values can result in linear, non-linear and random D/A conversion circuits.

10 of Kitamura selects an analog reference voltage signal, based on the input information B_0 and B_1 , to provide to the comparator 9 for programming verification purposes.

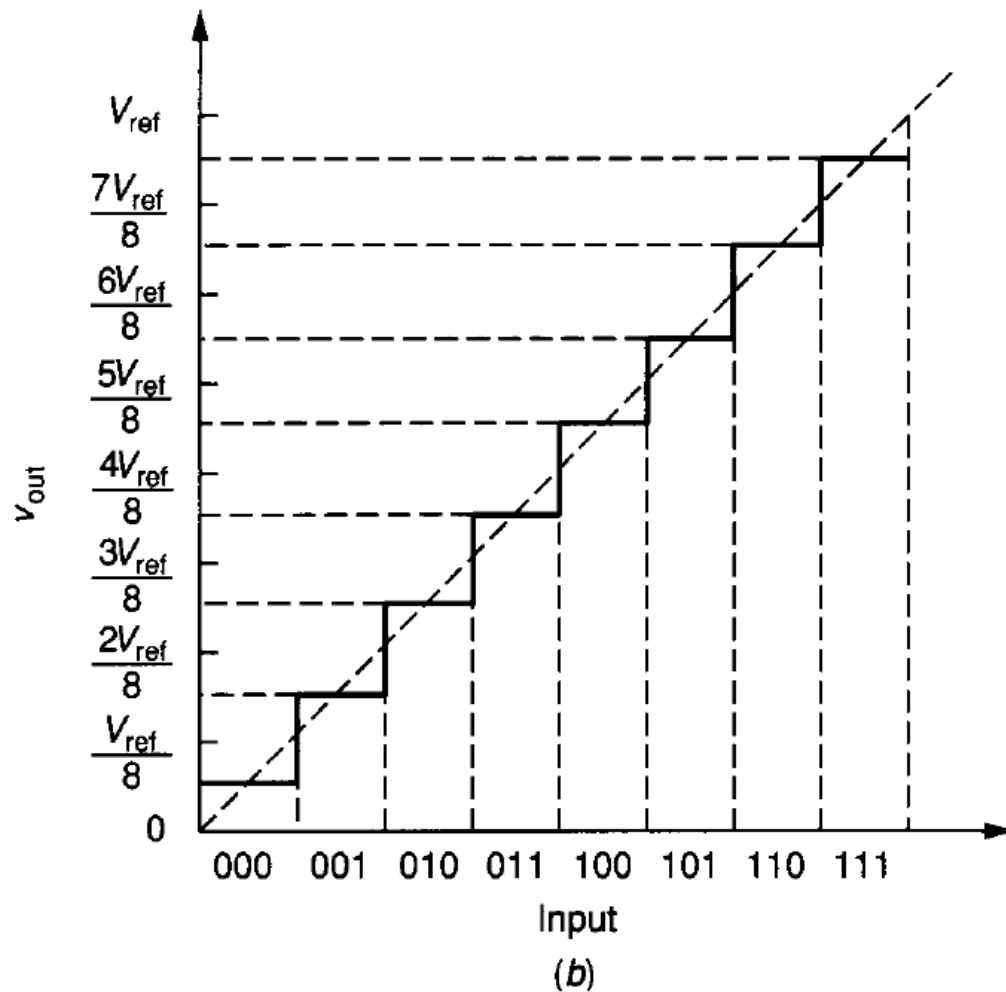


Exhibit Figure B

80. Therefore for the above reasons and those presented in the respective claim chart in the Petition (Chart I), which I hereby incorporate by reference, it is my opinion that a POSITA would find all Challenged Claims (as defined in the Petition) obvious in light of Kitamura.

B. All Challenged Claims are Obvious in View of Mehrotra

81. Mehrotra (U.S. Patent No. 5,172,338 having an effective filing date of April 13, 1989) discloses an electrically alterable, non-volatile memory device that has memory cells each capable of storing more than one bit of information, for example, memory cells each having four memory states to store two bits of information, *e.g.*, an MLC device. *See* Ex. 1004 at 2:14-15; 9:24-31.

82. As with the '571 patent, Mehrotra describes a process for reading the current memory state of a multilevel memory cell, programming the memory cell to a desired memory state and verifying the programming of the memory cell. *See id.* at 10:30-56; 18:62-20:51.

83. Mehrotra shows examples of four-memory state configurations in Figures 7A and 7B. Specifically, Figure 7A shows an example of partitioning a voltage threshold window of a memory cell to achieve four memory states, *i.e.*, (0,0), (0,1), (1,0), and (1,1).

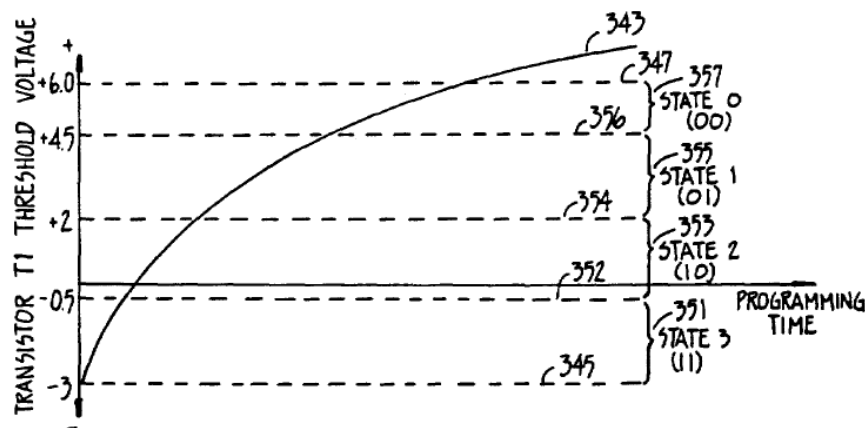
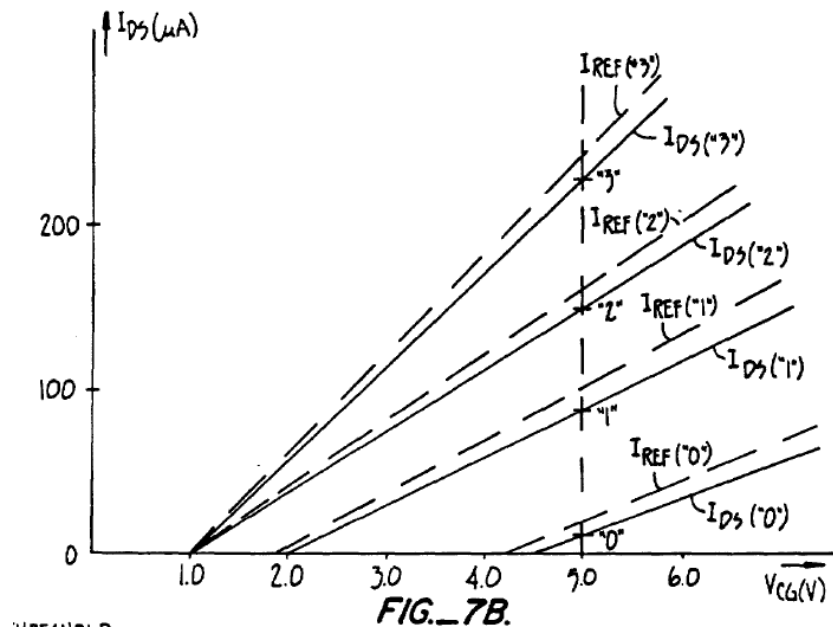


FIG. 7A.

84. Figure 7B shows an analogous four-memory state partitioning but based on a current threshold scheme.



85. Thus Mehrotra describes memory state schemes based on both voltage and current characteristics of a memory cell. Mehrotra also notes that for reliability purposes when reading the state of a cell, the reference signal can be

placed within the boundaries of the window defining the memory state.¹⁵ *See id.* at 21:27-31.¹⁶

86. Mehrotra emphasizes that either voltage or current can be used to “read” a memory cell: “The memory state of a cell may be determined by measuring the threshold voltage V_{T1} programmed therein. Alternatively, as set forth in co-pending patent application, Ser. No. 204,175, the memory state may conveniently be determined by measuring the differing conduction in the source-drain current I_{DS} for the different states.” Ex. 1004 at 10:30-36. Mehrotra

¹⁵ Mehrotra describes that the memory cell reading process can be used in the programming and verifying process to provide the current state of the memory cell for comparison to the desired state of the memory cell, as discussed in detail below. *See* Ex. 1004 at 10:50-56.

¹⁶ Harari (U.S. Patent No. 5,095,344 filed on June 8, 1988) also describes that the memory state reference signals can be placed well within the boundaries of the windows defining the memory states. *See* Ex. 1014 at 26:60-65 9 (“In a practical implementation of the circuit of FIG. 11e the reference levels $I_{REF,i}$ ($i=0,1,2$) may be somewhat shifted by a fixed amount during sensing to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed”).

describes that the read circuits 220 access the data path 105 (conveying bit line information from the addressable EEPROM array 60) to read the current state of the memory cell. *See* Ex. 1004 at 19:38-41, 19:66-68 (“the read circuits 220 access the N-channel data path 105 to read the states in the N chunk of [memory] cells.”).

87. As noted in the preceding paragraph, Mehrotra incorporates U.S. Pat. Appl. Ser. No. 204,175, which is the application that issued as Harari,¹⁷ as disclosing a current and voltage based memory cell reading process. Mehrotra also incorporates by reference Harari, and specifically notes that the disclosure in Harari centered on Figure 11e is pertinent to the memory cell read techniques of Mehrotra. *See id.* at 4:23-30 (“The subject matter herein is a further development of the EEprom array read techniques described in copending patent application Ser. No. 204,175, filed Jun. 8, 1988, by Dr. Eliyahou Harari, particularly the disclosure relating to FIG. 11e thereof. Application Ser. No. 204,175 is hereby expressly incorporated herein by reference, the disclosure with respect to the embodiments of FIGS. 11, 12, 13 and 15 being most pertinent.”). Figure 11e of Harari is reproduced below.

¹⁷ Harari also describes an MLC device with memory cells that can each store more than one bit of information. *See* Ex. 1014 at Abstract; 24:5-23.

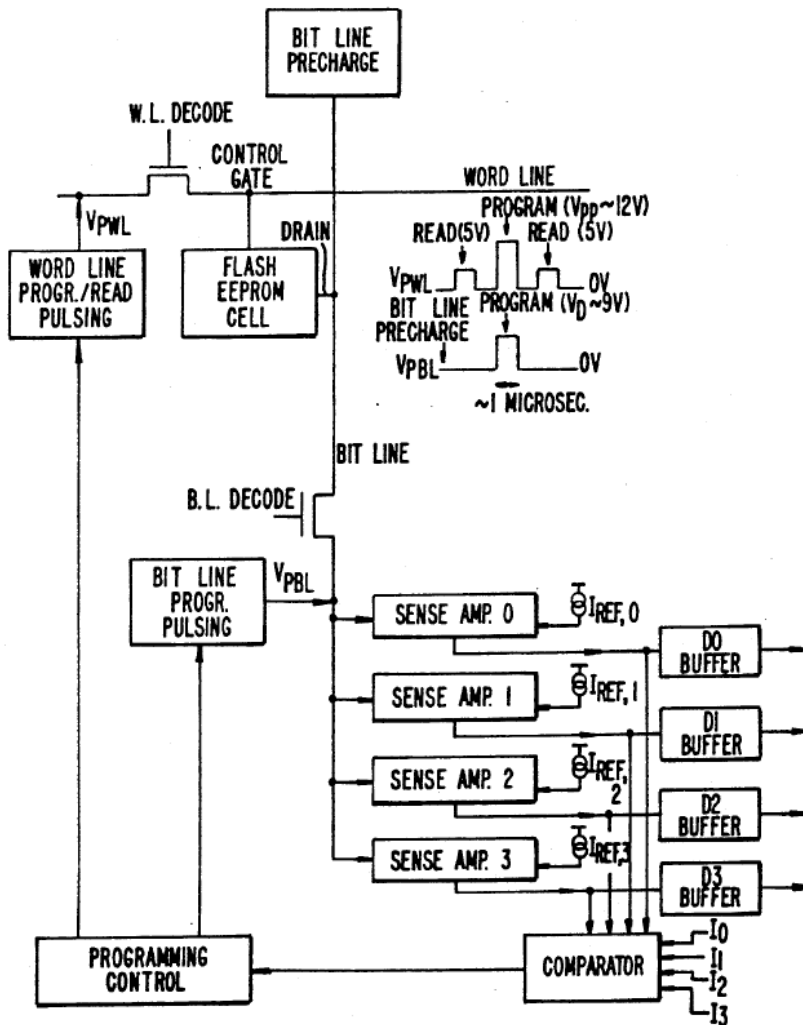


FIG.11e

88. Harari's Figure 11e is a sense amplifier-based circuit to read, *i.e.*, determine, the current memory state of a four-state memory cell. *See* Ex. 1014 at 25:65-26:17. The read circuit functions by comparing the output of the memory cell bit line,¹⁸ similar to the '571 patent, representing the current memory state of

¹⁸ The cell bit line can provide a memory cell current indicative of its memory state or a corresponding voltage, *e.g.*, sampled at an impedance element.

the memory cell, with four reference currents. Each of the reference currents (*i.e.*, I_{REF0} , I_{REF1} , I_{REF2} , I_{REF3}) corresponds to a different memory state, as shown in Mehrotra's Figure 7B, which is Figure 11c in Harari. *See id.* at 25:11-16, 26:5-17.

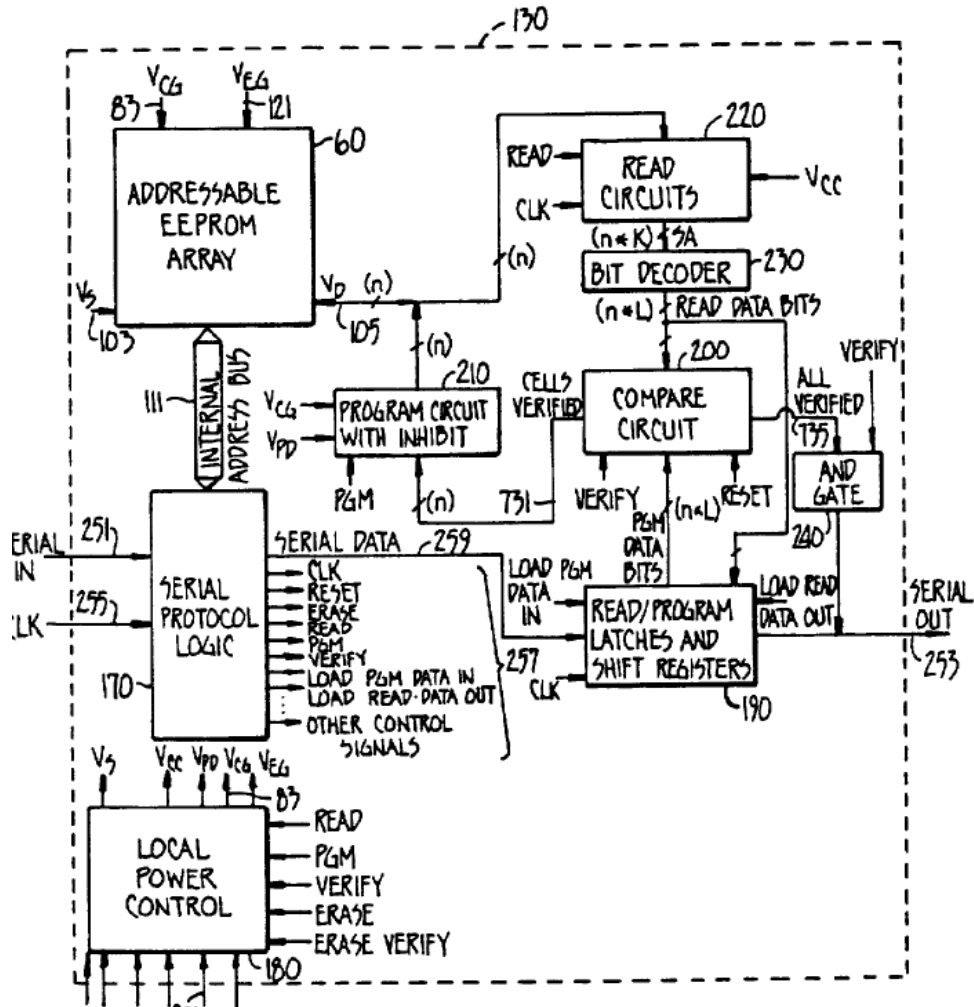
89. Each of the sense amplifiers (*i.e.*, Sense Amp. 0, Sense Amp. 1, Sense Amp. 2, and Sense Amp. 3) is connected (i) to the output of the memory cell bit line, which is connected to the drain of the memory cell and represents the current memory state of the memory cell,¹⁹ and (ii) to a respective different one of the reference currents. *See id.* Thus, in operation, the sense amplifiers collectively compare the output of the memory cell bit line to each of the reference currents, and the compare results are passed to buffers D_0 - D_3 . *See id.* These buffers can be analyzed to determine the memory state of the cell. For example, if the outputs of the sense amplifiers indicate that the output of the memory cell bit line is less than I_{REF3} but greater than the other reference currents then the cell is in the fourth memory state. *See Ex. 1004 at Figure 7B.* Or, if the outputs of the sense amplifiers indicate that the output of the memory cell bit line is less than all the reference currents then the cell is in the first memory state. *See id.*

¹⁹ As indicated by, for example, Harari, it was well known in art to sample the signal on a memory cell's bit line (*e.g.*, connected to the memory cell's drain) to determine the current memory state of the memory cell.

90. In addition to using four sense amplifiers to read the memory cell, and the '571 patent, Harari also discloses a read process that only uses three sense amplifiers and three reference currents, similar to the three sense amplifiers and three reference signals used in the read circuit disclosed in Figure 6 of the '571 patent. *See* Ex. 1014 at 26:51-55.

91. Harari also notes that voltage level sensing can be used instead of the above-described current level sensing to determine the memory state of the memory cell. *See id.* at 27:2-3.

92. Like the '571 patent, Mehrotra also describes an iterative programming and verification process. *See* Ex. 1004 at 3:64-4:5; 18:18-29; 19:26-20:36; Figure 15. More specifically, Mehrotra describes a programming process whereby a memory cell is first erased (*i.e.*, programmed to an erase state). *See id.* at 18:62-68. Next, a series of programming pulses, each followed by a programming verification step, are performed until the cell is verified as correctly programmed. *See id.* at 18:18-25, 18:62-68, 19:10-20:16. Mehrotra describes this process in more detail with reference to Figure 5, partially reproduced below.



93. With reference to Figure 5 above, the Program Circuit with Inhibit (“Program Circuit”) 210 provides the programming pulses.²⁰ See Ex. 1004 at 20:7-16, Figure 15. The Compare Circuit 200 controls the verification process, to determine if the memory cell is programmed to the desired memory state, as

²⁰ The Local Power Control device 180 (or controller 140) provides various programming-related signals to the memory device. See Ex. 1004 at 8:7-10.

further detailed below. *See id.* at 20:17-45. The Read Circuits 220 read the current state of the memory cell, as described above.

94. More specifically, the Program Circuit 210 applies programming pulses, one at a time, to a memory cell to be programmed. *See* Ex. 1004 at 3:64-4:5; 18:18-29; 19:26-20:36; Figure 15. After each pulse, the Compare Circuit 200 verifies whether the memory is correctly programmed to its desired memory state. *See id.* When the Compare Circuit 200 verifies that the memory cell is correctly programmed, it outputs a control signal on line 731 to the Program Circuit 210 indicating that the memory cell has been correctly programmed. *See id.* (“The N compare module's outputs such as 725, 727 are available at an N-channel output line **731** to be fed to the program circuit with inhibit 210 of FIG. 5”) (emphasis added). Such a control signal indicates when cell programming should end. *See id.* at 3:64-4:5; 18:18-29; 19:26-20:36; 20:67-21:5 (“Since the signal in line 731 is from the output of the cell compare module 701 shown in FIG. 16, it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states.”); Figure 15. Alternatively, if the Compare Circuit 200 determines that the memory cell is not yet correctly programmed then the iterative programming pulse/verify process continues until the memory cell is correctly programmed. *See id.*

95. Mehrotra describes, in part, that the reading and programming/verification processes can be performed by operating on “chunks” of memory cells in parallel such that, for example, multiple cells can be programmed at once. *See id.* As part of this parallel processing, Mehrotra further describes that the Compare Circuit 200 can compare the current state of a given memory cell, in digital form as binary bits, with the desired memory state, also represented in digital, binary bit form, and based on a bit-by-bit comparison determine if the cell has been correctly programmed. *See id.* at 20:2-16. For example, like the digital comparison process described in the ’571 patent, the Mehrotra comparator can compare a signal representing two-bit input information, *e.g.*, the desired memory state in two-bit form such as (1,0), with the current state of the memory cell in two-bit form from the Bit Decoder 230. *See id.* at 20:2-7.

96. As introduced above, Mehrotra describes that the Compare Circuit 200 receives a signal representing the current state of the memory cell from the Bit Decoder 230, which received its input from the Read Circuit 220. *See id.* The Compare Circuit 200 receives the reference signal, representing the input information in bit form, from the Read/Program Latches and Shift Registers circuit 190 (“RPLSR 190”). The RPLSR 190 receives the program information, *e.g.*, desired memory state information, via the “LOAD PGM DATA IN” input.

97. To provide the program information, *e.g.*, two-bit desired memory state information to the Compare Circuit 200, the RPLSR 190 must select and provide an encoded signal that represents the desired memory state to the Compare Circuit 200.²¹ Thus, for example, assuming a 0 Volts signal corresponds to a binary input (0) and a 5 Volts signal corresponds to a binary input (1) then for a (0,1) desired memory state the RPLSR 190 would select and provide a 0 Volts, 5 Volts reference signal²² to the Compare Circuit 200 corresponding to the (0,1) input information. Thus the RPLSR 190 must make a decision to select a 0 Volts, 5 Volts reference signal for the (0,1) input information/desired memory state, as

²¹ As was well known in the prior art, bit-represented digital information can be converted to an encoded signal, *e.g.*, voltage or current signal, to transmit between components. *See* Ex. 1008 at page 4.

²² Thus the reference signals corresponding to the various memory states are predetermined, *e.g.*, based on number of desired memory states and the encoding scheme, and the RPLSR 190 selects the one of these reference signals that corresponds to the desired memory state consistent with the “LOAD PGM DATA IN” information. If the reference signals were not predetermined the RPLSR 190 would not know which reference signals correspond to which memory states and “LOAD PGM DATA IN” information.

opposed to selecting a 0 Volts, 0 Volts; 5 Volts, 0 Volts; or 5 Volts, 5 Volts reference signal respectively corresponding to other program information/desired memory states (0,0); (1,0); or (1,1).²³

98. Although the embodiment in Figure 5 of Mehrotra focuses on a digital programming verification process through the Compare Circuit 200, it would have been obvious to a POSITA at the effective filing date of the '571 patent to implement an analog version. For example, Mehrotra itself shows an analog signal comparison implementation in the sense amplifiers used in the memory cell reading process. *See, e.g.*, Ex. 1004 at 11:20-12:20. Generally, analog voltage comparison implementations for EEPROM memory devices were well known in the art at the time the '571 patent was filed. For example, Kokubun describes such an analog comparison implementation. *See* Ex. 1005 at 1:10-20, 4:55-5:43.

99. More specifically, with respect to EEPROMs, Kokubun discloses that “[s]uch circuits require a voltage detection circuit for producing an internal reference voltage and for comparing a detected voltage with the reference voltage. The voltage detection circuit also includes means for adjusting the reference

²³ The correspondence between the reference signals selected by the RPSR 190 and the memory states are based on, for example, the number of desired memory states and the encoding scheme.

voltage.” *See id.* at 1:10-20. In this context Kokubun describes an analog voltage comparator 50 in the form of a differential amplifier. *See id.* at 4:67-5:27 and Figure 3 (*see* Differential Amplifier 50 in Figure 3 showing a comparison of a voltage at node N50 with a reference voltage at node N11.)

100. Lee also shows use of an analog comparator in a computer system memory device.²⁴ *See* Ex. 1006 at 2:34-65, 4:42-44 (“FIG. 3 depicts a static RAM, a N-bit MOS **analog comparator** 1, and a sense amplifier in a Tag RAM in accordance with the present invention.”) (emphasis added). Thus in the memory device field, use of analog signal comparators were well known to a POSITA.

101. Use of an analog comparator, instead of a digital comparator, has certain advantages that were also well known to a POSITA. For example, using an analog comparator over a digital one could reduce switching noise often associated with high-speed digital comparators (as would typically be found in a MLC device), minimize the use of complex digital circuitry (and associated cost and

²⁴ Like Lee, Mehrotra is directed to improving computer system memories. *See* Ex. 1004 at 2:41-44. A POSITA working in the memory device field would have knowledge of the then state of the art computer system memory technologies (including that of Lee and Mehrotra). Thus Lee and Mehrotra are analogous art and their teachings would be known to a POSITA.

comparatively large semiconductor die size for such circuitry), and reduce power supply bounce that would otherwise be inherent in low-noise digital comparator memory device implementations. *See, e.g.*, Ex. 1006 at 2:23-54, Figure 3.

Reducing noise improves the performance and reliability of a memory device, and reducing the complexity and/or size of the device improves the manufacturability and/or cost of the device. *See id.*

102. Mehrotra is also directed to providing reliable, accurate, low-cost and easy to manufacture memory devices. *See, e.g.*, Ex. 1004 at 2:26-44. Thus a POSITA would look to readily known and available technologies to achieve these goals, including implementing an analog program/verify comparison process, for example, as shown in Lee and/or Kokubun, as each shows the general knowledge of a POSITA.

103. An analog comparison implementation in Mehrotra can be explained with reference to Figure 5. For example, the data path 105²⁵ from the Addressable EEPROM Array 60, which includes the memory cells, provides the bit line signal from a given memory cell(s) to a first input of the analog comparator (*e.g.*, Compare Circuit 200). This bit line signal would represent the current memory

²⁵ The data path 105 represents the bit line(s) from the various memory cells in the Addressable EEPROM Array 60.

state of the memory cell, similar to that shown as the “Y” input to Analog Comparator 202 in Figure 8 of the ’571 patent.

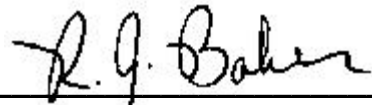
104. The second input to the analog comparator would come from a device that functions similarly to the RPLSR 190 device in that such a device would select and supply reference information/a signal representing the desired memory state of the memory cell, *e.g.*, based on the program data “LOAD PGM DATA IN” information provided to the RPSR 190. This second input is comparable to the “X” input to Analog Comparator 202 in Figure 8 of the ’571 patent. The output of the analog comparator would remain connected to the Program Circuit 210, and the program/verify process described by Mehrotra above would otherwise operate in a similar manner.²⁶

²⁶ Although Mehrotra describes that a serial memory cell reading process can be used in the programming and verification process, it also describes that a parallel memory cell reading process can alternatively be used in the programming and verification process. *See, e.g.*, Ex. 1004 at 19:1-20:51. Whether serial or parallel, either processing approach can readily be implemented through and is entirely consistent with an analog implementation, *e.g.*, through a multiple input analog comparator, which was well known in the prior art.

105. Therefore for the above reasons and those presented in the respective claim chart in the Petition (Chart II), which I hereby incorporate by reference, it is my opinion that a POSITA would find all Challenged Claims (as defined in the Petition) obvious in light of Mehrotra.

106. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: December 24, 2014

By: 

R. Jacob Baker, Ph.D., P.E.
Las Vegas, NV

EXHIBIT 1

R. JACOB (JAKE) BAKER, PH.D., P.E.

Professor of Electrical and Computer Engineering
University of Nevada, Las Vegas
Department of Electrical and Computer Engineering
Box 454026 • 4505 S. Maryland Parkway
Las Vegas, Nevada 89154-4026

(702) 895-4125 (office)

Email: rjacobbaker@gmail.com

Website: <http://CMOSedu.com/jbaker/jbaker.htm>

SUMMARY

- Active scholar (h-index of 32 and i10-index of 88) whose research is focused on:
 - High-speed interfaces for electro-optic, mixed-signal, and analog integrated circuits;
 - Design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide);
 - Analog and mixed-signal circuit techniques for nanometer CMOS; 3D packaging techniques
 - The design of instrumentation for scientific research
 - Delivery of circuit design education to off-campus students/engineers via the Internet.
- Mentor to:
 - Approximately 75 graduate students (major professor),
<http://CMOSedu.com/jbaker/students/students.htm>
 - Electrical and Computer Engineering Department faculty;
 - Engineers locally, nationally, and internationally;
 - New and established companies.
- Extensive leadership experience including:
 - Chair, Electrical and Computer Engineering Department, Boise State University;
 - Dealing with conflict, problems, and limited resources;
 - Leading the department through ABET accreditation;
 - Creation and implementation of both Master and Doctoral programs in ECE.
- Inventor with more than 200 granted or pending patents in integrated circuit design.
- Experienced integrated circuit designer and educator with significant industry experience. See additional information at <http://cmosedu.com/jbaker/projects/fund.htm>
- Textbook authorship and Internet contributions (see <http://CMOSedu.com>), that have helped tens of thousands of engineers around the world.
- Recognized by the IEEE Power Electronics Society with the Best Paper Award in 2000 (*IEEE Transactions on Power Electronics*) from PhD dissertation work.
- International known in the field of integrated circuit design, recipient of many honors including the Terman Award, the IEEE CAS Education Award, and IEEE Fellow.

EDUCATION

Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*

M.S. and B.S. in Electrical Engineering: May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, and the Air Force Research Lab.
- Current research interests are:
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories
 - Analog and mixed-signal circuit design for communication systems, synchronization, and data conversion especially using the K -Delta-1-Sigma modulator
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
 - Reconfigurable electronics design using nascent memory technologies
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Methods to deliver circuit design education to industry and off-campus students, see videos here
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

- 2013 - present:** Working with National Security Technologies, LLC,) on the Design of Integrated electrical/photonic application specific integrated circuit (ASIC) design.
- 2013 - present:** Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.
- 2010 - 2013:** Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.
- 2013:** Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.
- 2012:** Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, and infrared imaging systems.
- 2010 - 2012:** Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodectors in standard CMOS.
- 2009 - 2010:** Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.
- 2009 - 2010:** Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.
- 1994 - 2008:** Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory using the MJT memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line.
- Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging.
- Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).
- January 2008:** Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.
- May 1997 - May 1998:** Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips.
- Summer 1998:** Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.
- Summers 1994 - 1995:** Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble shooting electric motors on mining equipment.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services are listed below. I have been deposed eight times and given testimony at one trial.

Skadden, Arps, Slate, Meagher & Flom LLP & Affiliates (Palo Alto, CA)

Case – ALFRED T. GIULIANO, Chapter 7 Trustee of the Ritz Estate; CPM ELECTRONICS INC.; E.S.E. ELECTRONICS, INC. and MFLASH, INC., on Behalf of Themselves and All Others Similarly Situated v. SanDisk Corp.

Case Number – California, ND (Oakland) 4:10-cv-02787. Fourth amended complaint filed on September 24, 2014.

Case Subject Matter - Non-volatile semiconductor flash memory.

Work Performed – Provided expert consulting services.

Ropes & Gray LLP (East Palo Alto, CA, New York, NY, and Washington, DC)

Case – Macronix International Co., Ltd. v. Spansion, Inc., Aerohive Networks, Allied Telesis, Ciena, Delphi Automotive, Polycom, Ruckus Wireless, ShoreTel, Tellabs, and TiVo

Case Number – ITC Investigation No. 337-TA-922. Complaint filed on June 27, 2014.

Case Subject Matter - Devices containing non-volatile memory and products containing the same.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Quinn Emanuel Urquhart & Sullivan, LLP (San Francisco, CA and Washington, DC)

Case – Freescale Semiconductor, Inc. v. MediaTek, Inc., et. al.

Case Number – ITC Investigation No. 337-TA-920. Amended complaint filed on May 27, 2014.

Case Subject Matter - Semiconductor integrated circuits and devices containing the same.

Work Performed – Provided expert consulting services.

Ropes & Gray LLP (Washington, DC)

Case – Macronix International Co., Ltd. v. Spansion, Inc., et al.

Case Number – Virginia, ED 3:13-cv-00679. Complaint filed on November 20, 2013.

Case Subject Matter - Non-volatile semiconductor flash memory.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Cooley LLP (San Diego, CA)

Case – HSM Portfolio LLC and Technology Properties Limited LLC v. Fujitsu, AMD, Qualcomm, Inc.,

Elpida, SK Hynix, Micron, ProMOS, SanDisk, Sony, ST Micro, Toshiba, ON, and Zoran

Case Number – Delaware, 1:11-cv-00770. Third amended complaint filed on June 28, 2013.

Case Subject Matter - Semiconductor sensing circuits.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto and San Diego, CA)

Case – Cypress Semiconductor Corporation v. GSI Technology, Inc.

Case Number – California, ND 3:13-cv-02013. Complaint filed on May 1, 2013.

Case Subject Matter - Semiconductor static random access memory (SRAM) circuit design.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, and declaration for inter partes reexamination.

Amin, Turocy & Watson LLP (San Francisco, CA)

Case – InvenSense, Inc. v. STMicroelectronics, Inc.

Case Subject Matter - Analog signal processing circuitry used in Microelectromechanical systems (MEMS) capacitive sensors.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reexamination.

Montgomery McCracken Walker & Rhoads LLP (Philadelphia, PA)

Case – Simon Nicholas Richmond v. Winchance Solar Fujian Technology, Target, Creative Industries, et. al.

Case Number – New Jersey, 3:13-cv-01954. Amended complaint filed on March 27, 2013.

Case Subject Matter - Circuitry including solar cells, re-chargeable batteries, energy conversion for solar lighting.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Alston & Bird, DLA Piper, Gibson Dunn, Katten, O'Melveny, Orrick, and WilmerHale (various locations in the USA)

Case – Freescale v. Funai, CSR, Zoran, MediaTek, Vizio, Sanyo, TPF, Top Victory Electronics, Envision Peripherals, AmTRAN, and Marvell

Case Number – Texas, WD 1:12-cv-00644. Amended complaint filed on January 14, 2013.

Case Subject Matter - Semiconductor circuitry for voltage regulators, bus terminations, packaging, and signal processing.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, and Markman tutorial.

Amin, Turocy & Watson LLP (San Jose and San Francisco, CA)

Case – InvenSense, Inc. v. Robert Bosch GmbH

Case Subject Matter - Microelectromechanical systems (MEMS) sensor design and manufacture.

Work Performed – Provided expert consulting services in 2013.

Morrison & Foerster LLP (Los Angeles, Palo Alto, and San Francisco, CA)

Case – STMicroelectronics, Inc. v. InvenSense, Inc.

Case Number – California, ND 3:12-cv-02475. Complaint filed on May 16, 2012.

Case Subject Matter - Microelectromechanical systems (MEMS) sensors including Gyroscopes and accelerometers.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for SK Hynix, Inc. on matters relating to investigation of certain patents owned by Round Rock Research LLC
Case Subject Matter - Semiconductor random access memory.
Work Performed – Provided expert consulting services in 2012.

Keker & Van Nest LLP (San Francisco, CA)

Case – Round Rock Research LLC v. SanDisk Corp.
Case Number – Delaware, 1:12-cv-00569. Complaint filed on May 3, 2012.
Case Subject Matter - Semiconductor non-volatile flash memory.
Work Performed – Provided expert consulting including: invalidity analysis, non-infringement analysis, expert reports, and was deposed.

Perkins Coie LLP (San Diego, CA)

Case – ASUS Computer International v. Round Rock Research LLC
Case Number – California, ND 3:12-cv-02099. Complaint filed on April 26, 2012.
Case Subject Matter - Semiconductor memory and image sensors.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, expert reports, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Dr. Michael Jaffe' as insolvency administrator for Qimonda AG v. LSI, Atmel Corp, Cypress, MagnaChip, and ON Semiconductor
Case Number – California, ND 3:12-cv-03166. Complaint filed January 10, 2012.
Case Subject Matter - Semiconductor processing and manufacturing.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Useful Arts IP (Cupertino, CA)

Case – Tezzaron (formerly Tachyon Semiconductor) v. Elm Technology Corporation
Case Number – Patent Interference No. 105,859. Declared December 1, 2011.
Case Subject Matter - Packaging of semiconductors and through semiconductor vias.
Work Performed – Patent interference, wrote declaration, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Nanya Technology Corporation v. Elpida Memory, Inc. and Kingston Technology Company, Inc.
Case Number – ITC Investigation No. 337-TA-821. Complaint filed on November 21, 2011.
Case Subject Matter - Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting and reports on validity, infringement, and domestic industry. Also provided declarations and was deposed.

Morgan, Lewis & Bockius LLP (Washington, DC)

Case – Elpida Memory, Inc. v. Nanya Technology Corporation
Case Number – ITC Investigation No. 337-TA-819. Complaint filed on November 15, 2011.
Case Subject Matter - Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting and reports on infringement, domestic industry, and validity. Also provided Markman tutorial, declarations, deposition, and testimony at the trial.

Ropes & Gray LLP (New York, NY)

Case – Intellectual Ventures v. Sendai Nikon Corporation
Case Number – Delaware, 1:11-cv-01025. Complaint filed October 26, 2011.
Case Subject Matter - Image sensor design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Farella Braun + Martel LLP (San Francisco, CA)

Case – Round Rock Research LLC v. Dell, Inc.

Case Number – Delaware, 1:11-cv-00976. Complaint filed on October 14, 2011.

Case Subject Matter - Semiconductor DRAM design and manufacture.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Latham & Watkins LLP (San Francisco, CA)

Case – Altera Corp. v. LSI Corp. and Agere Systems, Inc.

Case Number – California, ND 4:11-cv-03139. Complaint filed on June 24, 2011.

Case Subject Matter - Semiconductor devices including phase-locked loops and clock recovery circuits.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Fish & Richardson P.C. (Washington, DC)

Case – Spansion LLC v. Samsung Electronics Co., Ltd., Apple, Inc., Nokia Corp., PNY Technologies, Inc. Research In Motion Corporation, Transcend Information Inc.

Case Number – ITC Investigation No. 337-TA-735. Complaint filed on August 6, 2010.

Case Subject Matter - Semiconductor flash memory manufacture and design.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Jones Day LLP (Palo Alto, CA)

Case – LSI and Agere, Inc. v. Xilinx, Inc.

Case Number – New York, SD 1:09-cv-09719. Complaint filed on November 23, 2009.

Case Subject Matter - Semiconductor digital design and clocking.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Morrison & Foerster LLP (New York, NY)

Case – Innervation, Inc. et al v. Fujitsu Microelectronics America, Inc., Sony Corporation of America, Toshiba America Electronics Components, Inc., and Freescale Semiconductor, Inc.

Case Number – Maryland, 1:09-cv-01416. Complaint filed on May 29, 2009.

Case Subject Matter - Semiconductor circuit layout.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Wilson Sonsini Goodrich & Rosati P.C. (Palo Alto, CA)

Case – Panavision Imaging, LLC, v. OmniVision Technologies, Inc., Canon U.S.A., Inc., Micron Technology, Inc., Aptina Imaging Corporation, and Aptina, LLC.

Case Number – California, CD 2:09-cv-01577. Complaint filed on March 6, 2009.

Case Subject Matter - CMOS image sensor design and manufacture.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and wrote declaration.

McDermott Will & Emery (Menlo Park, CA)

Case – Volterra Semiconductor Corp. v. Primarion & Infineon Technologies North America & Infineon Technologies, A.G.

Case Number – California, ND 3:08-cv-05129. Complaint filed on November 12, 2008.

Case Subject Matter - High-performance analog and mixed-signal power management semiconductors.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and was deposed.

pre-2008 Miscellaneous minor expert witness work, was deposed twice.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

ASEE member

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013) Societies: Circuits and Systems, Education, Instrumentation and Measurement, Solid State Circuits

Member of the honor societies Eta Kappa Nu and Tau Beta Pi

Licensed Professional Engineer

HONORS AND AWARDS

- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2013 - 2014
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013 and 2014
- IEEE Fellow for contributions to the design of memory circuits - 2013
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- Elevated to Senior member of the IEEE, 1997
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-present), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as the Technology Editor (2012-2014) and Editor-in-Chief (2015 - present) for the *IEEE Solid-State Circuits Magazine*, as a Distinguished Lecturer for the SSCS (2013-2014), and as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015.

ARMED FORCES

6 years United States Marine Corps reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge, October 23, 1987

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition" *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) **Over 50,000 copies of this book's three editions in print.**

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 978-0-470-18475-2

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0-7803-6014-1

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 1999. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 1999. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

INVITED TALKS AND SEMINARS

Have given invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), Foveon, the Franklin Institute, Georgia Tech, Hong Kong University of Science and Technology, ICySSS keynote, IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lehigh University, Micron Technology (more than a dozen), Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx

(Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2014-2015) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, \$90,000
- Baker, R. J., (2014-2015) "Silicon Photonic-Electronic System Level Integration," U.S. Air Force/DOD, \$54,607
- Baker, R. Jacob, (2013-2014) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, \$162,074
- Baker, R. Jacob, (2013) "Design Software Setup," Department of Energy, National Security Technologies, LLC, \$10,999
- Campbell, K. A. and Baker, R. J., (2009-2012) "Reconfigurable Electronics and Non-Volatile Memory Research" funded by the Air Force Research Laboratory, \$2,790,081
- Baker, R. J., (2010-2012) "Dual Well Focal Plane Array (FPA) Sensor," U.S. Navy, \$31,500
- Baker, R. J., (2011) "Readout-Integrated Circuit (ROIC) Development in Support of Corrugated Quantum Well Infrared Photo-detector (C-QWIP) Focal Plane Arrays (FPA) for Tactical Applications," U.S. Army, \$27,000
- Baker, R. J., (2011) "Monolithic CMOS LADAR Focal Plane Array (FPA) with a Photonic High-Speed Output Interface," U.S. Air Force/DOD, \$50,002
- Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2008-2010) "Radiation Resistant Phase Change Memory and Reconfigurable Electronics," NASA. \$1,500,000
- Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2007) "Reliability Investigations of Radiation Resistant, Multi-State Phase-Change Memory," NASA. \$726,768
- Baker, R. J., et. al., (2006-2010) "Establishment of a Doctoral Degree Program in Electrical and Computer Engineering in Electrical and Computer Engineering," Micron Foundation. \$5,000,000
- Baker, R. J., (2005-2006) "Advanced Processing Techniques for Fabrication of 3-D Microstructures for Future Electronic Devices," DARPA, N66001-01-C-8034, \$125,000
- Baker, R. J., (2004-2005) "Multi-Purpose Sensors for Detection and Analysis of Contaminants" EPA, X-97031102, \$75,000
- Baker, R. J., (2001-2006) Multi-University Research Initiative (MURI), "The effects of radio frequency pulses on electronic circuits and systems," Air Force Research Laboratory, \$350,000.

GRANTED US PATENTS

137. Baker, R. J., "Reference current sources," **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.
134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.

130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougall, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
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123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
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119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
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117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
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111. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **8,042,012**, October 18, 2011.
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98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.

97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.
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93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
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91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
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89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
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84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
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79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.

71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.
66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.
62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
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58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
54. Baker, R. J., "High speed low power input buffer," **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., "Method for stabilizing or offsetting voltage in an integrated circuit," **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,909,656**, June 21, 2005.
51. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **6,888,771**, May 3, 2005.
49. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,885,580**, April 26, 2005.
48. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,882,578**, April 19, 2005.
47. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,870,784**, March 22, 2005.
46. Baker, R. J., "Sensing method and apparatus for a resistive memory device," **6,859,383**, February 22, 2005.
45. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,856,564**, February 15, 2005.

44. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,856,532**, February 15, 2005.
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41. Baker, R. J., "Resistive memory element sensing using averaging," **6,822,892**, Nov. 23, 2004.
40. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **6,813,208**, Nov. 2, 2004.
39. Baker, R. J., "Wordline driven method for sensing data in a resistive memory array," **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., "Methods and apparatus for measuring current as in sensing a memory cell," **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., "Method and apparatus for sensing resistance values of memory cells," **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., "Producing walking one pattern in shift register," **6,771,249**, August 3, 2004.
31. Baker, R. J., "Sensing method and apparatus for resistance memory device," **6,741,490**, May 25, 2004.
30. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **6,704,881**, March 9, 2004.
29. Baker, R. J., "Method and system for writing data in an MRAM memory device," **6,687,179**, February 3, 2004.
28. Baker, R. J., "High speed digital signal buffer and method," **6,683,475**, January 27, 2004.
27. Baker, R. J., "High speed low power input buffer," **6,600,343**, July 29, 2003.
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25. Baker, R. J., "Sensing method and apparatus for resistive memory device," **6,577,525**, June 10, 2003.
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23. Baker, R. J., "High-speed digital signal buffer and method," **6,538,473**, March 25, 2003.
22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
21. Baker, R. J., "Resistive memory element sensing using averaging," **6,504,750**, January 7, 2003.
20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.
18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.

15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
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12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
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6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
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