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Japanese Patent Application Kokai No. S62-34398 (A)

A handwritten signature in black ink, appearing to read 'R. Blair Sly', with a large, stylized flourish extending from the bottom right.

R. Blair Sly
Principal
ION Translations, LLC
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ION Ref. 7897

940 Dwight Way
Suite One
Berkeley, CA 94710
510.841.5000

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(54) Title of Invention: NON-VOLATILE MEMORY

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(72) Inventor: KITAMURA, Yoshinari 33-1 Shiba 5 chome, Minato-ku, Tokyo
c/o NEC Corporation

(71) Applicant: NEC Corporation 33-1 Shiba 5 chome, Minato-ku, Tokyo

(74) Agent: UCHIHARA, Shin; Patent Attorney

SPECIFICATION

1. Title of the Invention

NON-VOLATILE MEMORY

2. Claims

[01] A non-volatile memory that includes a semiconductor non-volatile memory element whose characteristic is continuously varied by writing; a circuit that alternately switches between a write mode and a read mode at regular time intervals; a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that converts an analog signal that has been read into a digital signal.

3. Detailed Description of the Invention

Field of Industrial Utilization

[02] The present invention relates to a non-volatile memory.

Prior Art

[03] Floating gate MOS and MNOS memory elements have seen practical application as non-volatile memories in the past, but these could only store one bit of information per memory element.

Problems Which the Invention is Intended to Solve

[04] The conventional non-volatile memory mentioned above required memory elements equal in number to the number of bits of memory, which make it difficult to increase the degree of integration, and high price was another drawback.

[05] It is an object of the present invention to reduce the number of memory elements and lower the price by storing a plurality of bits in a single memory element.

Means Used to Solve the Above-Mentioned Problems

[06] The non-volatile memory of the present invention comprises a semiconductor non-volatile memory element whose characteristic is continuously varied by writing; a circuit that alternately switches between a write mode and a read mode at regular time intervals; a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal; a circuit that compares a read level from a memory cell to the level of the analog signal, and ends a write operation according to this result; and an A/D conversion circuit that inversely converts an analog signal that has been read into a digital signal.

Working Examples

[07] The present invention will now be described through reference to the drawings. FIG. 1 is a circuit diagram of a working example of the present invention. 1 is a memory cell constituted by a floating gate MOS transistor, 2 is a MOS transistor, 3 is a load circuit that switches between a write-use high voltage power supply (V_{PP}) and a read-use low voltage power supply (V_{DD}), 4 and 5 are driver circuits that output a high voltage during writing and a low voltage during reading by switching the power supply between V_{PP} and V_{DD} , 6 and 7 are address decoders, 8 is a read point from the memory cell 1, 9 is a comparator, 10 is a two-bit D/A conversion circuit, 11 is a read/write switching signal generation circuit, 12 is a read/write switching terminal, and 13 is a two-bit A/D conversion circuit.

[08] When data is written, first an address for selecting the memory cell 1 is provided from the outside to the address decoders 6 and 7, and a write mode signal is provided to the mode switching terminal 12. This write mode signal causes the read/write switching signal generation circuit 11 to generate read/write signals that periodically repeat a write period whose level is one binary value and a read period whose level is the other binary value. In the write period, a voltage close to V_{PP} is outputted from the drivers 4 and 5 and provided to the memory cell 1 and the MOS transistor 2, and in the read period, a voltage close to V_{DD} is outputted and provided to the memory cell 1 and the MOS

transistor 2. The switching circuit 3 supplies V_{PP} during the write period, and V_{DD} during the read period, to the read point 8.

[09] The relation between the write time t of the memory cell 1 and the threshold voltage V_T of the memory cell 1, which is given by the integrated value of the write period, is the relation shown in FIG. 2 under constant voltage conditions, and V_T rises as the write period lengthens. Since the floating gate MOS transistor 1 and the MOS transistor 2 constitute a ratio circuit with the load circuit 3, when the V_T of the floating gate MOS transistor 1 changes, the output voltage (V_O) of the read point 8 changes as shown in FIG. 3. Meanwhile, the two-bit input digital signals B_0 and B_1 to be written are converted by the D/A conversion circuit 10 into analog signals, and the operation is continued with write/read signals while lower than these analog signals, but when the comparator 9 determines that V_O is higher than the analog signals from the D/A conversion circuit 10, the read/write switching signal generation circuit 11 halts the output of the write/read signals and ends the write operation. Therefore, the V_O at this point is a voltage that corresponds to the input digital signals B_1 and B_2 .

[10] Meanwhile, when data is read, an address for selecting the memory cell 1 is provided from the outside to the address decoders 6 and 7, and a read mode signal is provided to the mode switching terminal 12. This read mode signal causes the read/write switching signal generation circuit 11 to output the write/read signals, and causes the driver circuits 4 and 5 to provide a voltage close to V_{DD} to the memory cell 1 and the MOS transistor 2. The previously stored output voltage of the read point 8 is outputted through the A/D conversion circuit 13 as two-bit digital signals D_0 and D_1 .

[11] The D/A conversion circuit 10 and the A/D conversion circuit 13 preferably share a voltage dividing element and a reference voltage supply (for the purpose of making their characteristics uniform), and there is preferably a level difference of $1/2$ LSB between the D/A conversion characteristics of the circuit 10 and the A/D conversion characteristics of the circuit 13 in order to maximize the operating margin.

[12] The working example in FIG. 1 shows the circuit of a one-element, two-bit non-volatile memory, but the MOS transistors 2 can be connected in parallel, the memory cells 1 can be connected in parallel to the individual MOS transistors 2, and corresponding address decoders and drivers can be provided to constitute a memory having the desired number of memory elements.

[13] In the above working example, an EPROM element constituted by a floating gate MOS transistor was used as the memory element, but an EEPROM element constituted by MNOS or tunnel injection, or any other element can be used instead.

Effect of the Invention

[14] As described above, with the present invention, writing and reading are repeated at short periods until the output voltage to an element whose V_T or other such characteristic that continuously varies with write time coincides with a voltage obtained by subjecting a plurality of bits of digital signal to D/A conversion, and this allows a

plurality of bits of digital data to be written to the memory cell transistor of a single element, and allows a non-volatile memory to be obtained in which there are fewer memory cells in relation to the number of bits.

4. Brief Description of the Drawings

FIG. 1 is a circuit diagram of a working example of the present invention;

FIG. 2 is a graph of the memory cell 1 in FIG. 1; and

FIG. 3 is a graph of the voltage at the read point in FIG. 1.

- 1 floating gate MOS transistor
- 2 MOS transistor
- 3 load circuit
- 4, 5 driver circuit
- 6, 7 address decoder
- 9 comparator
- 10 D/A conversion circuit
- 11 read/write switching signal generation circuit
- 13 A/D conversion circuit

Agent: UCHIHARA, Shin; Patent Attorney [seal]

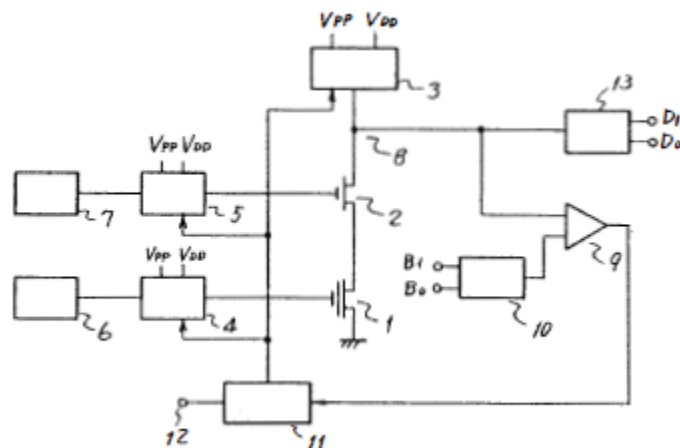


FIG. 1

- 1 floating gate MOS transistor
- 2 MOS transistor 2
- 3 load circuit
- 4, 5 driver circuit
- 6, 7 address decoder
- 9 comparator
- 10 D/A conversion circuit
- 11 read/write switching signal generation circuit
- 12 mode switching terminal
- 13 A/D conversion circuit

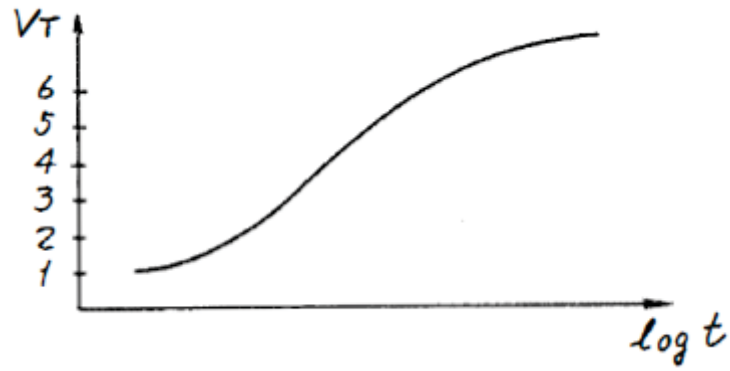


FIG. 2

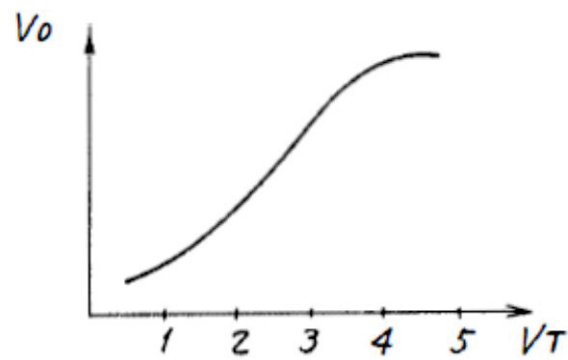


FIG. 3