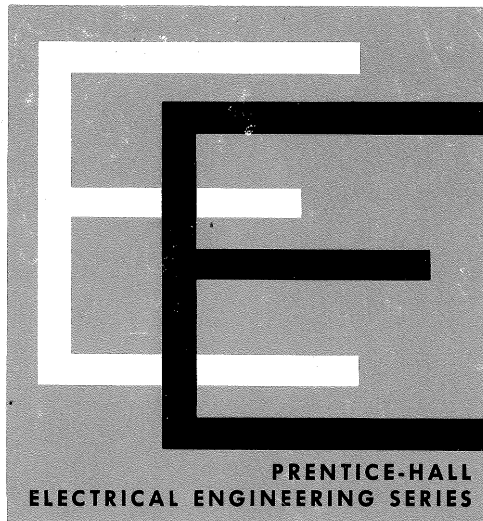


V. THOMAS RHYNE

Fundamentals of Digital Systems Design

COMPUTER APPLICATIONS IN ELECTRICAL ENGINEERING SERIES

Franklin F. Kuo,
Editor



PRENTICE-HALL
ELECTRICAL ENGINEERING SERIES

FUNDAMENTALS OF DIGITAL SYSTEMS DESIGN

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11 Analog/Digital Conversion

11.0 Introduction

The concept of a generalized digital system is introduced in Chapter 1 (see Fig. 1-0). The input and output signals that are received and/or generated by such a system are shown to be of two types: digital signals and analog signals. Some digital systems deal only with digital signals. Data-processing computers are a common example. Their input data come from punched cards, paper tape, digital magnetic tape, or some other digital media. Computed output data are printed or punched or recorded in some other digital fashion.

In many digital systems, however, nondigital (analog) information must be received, processed, and returned to the user. Typical analog data include temperature, pressure, force, speed, or other continuous descriptors of real-world conditions. These types of signals are first converted into an appropriate form by transducers. Electrical transducers that convert their input variable into a voltage or current are used in conjunction with electronic digital systems. Other types of transducers are in use, however, such as those having a pressure output that are used with fluidic digital systems.

The output signals from the transducers are converted into digital form by *analog-to-digital converters* (ADCs). The digital code words that are produced by this conversion describe the input conditions to the digital system. These code words are processed by the system in order to produce the desired output data.

In many situations output data must be converted back into a continuous form. Typical examples of this requirement are systems whose digital outputs

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must actuate a servo or a cathode-ray-tube display. These systems are called *digital-to-analog* converters.

This chapter discusses digital-to-analog conversion. The emphasis is upon the design of these converters in chapters 1-7. The design of these converters is discussed in detail. As a result, the section on digital-to-analog conversion is kept to a minimum. Considerations kept to a minimum. Sources are provided.

It is also significant that the digital-to-analog converter is available from commercial sources. Logical circuitry already available may therefore be considered. Systems that must be designed are those where the effect that the wide variety of devices has had upon these devices is no longer significant.

11.1 Digital-to-Analog Conversion

Figure 11-0 is a generalized block diagram of a digital-to-analog converter that is to be converted into a digital-to-analog converter.

Figure 11-0. A Voltage-to-Analog Converter

DAC. The internal circuitry of the bits of the digital code word, V_{out} .

The output voltage is random, linear, or nonlinear. The coded inputs are of this type of tabular data. The constructed as shown in a relay that connects the words are decoded by the signals is buffered by an output. It can be used if the DAC

must actuate a servo system, drive a meter or an X-Y recorder, or operate a cathode-ray-tube display unit. The devices that perform this conversion are called *digital-to-analog converters* (DACs).

This chapter discusses the basic concepts of digital-to-analog and analog-to-digital conversion. Voltage-oriented converters are considered. The major emphasis is upon the logic aspects of operating these devices and of using them in conjunction with digital systems that have been designed à la Chapters 1-7. The design of DACs is really more electronic than digital in nature. As a result, the section on digital-to-analog conversion is brief, with electronic considerations kept to a minimum. References to more detailed information sources are provided.

It is also significant that a wide variety of DACs and ADCs are now available from commercial sources, with all the necessary electronics and logical circuitry already designed and conveniently packaged. These devices may therefore be considered as predesigned components rather than as subsystems that must be designed and constructed. This situation is similar to the effect that the widespread availability of flip-flops, gates, and other logical devices has had upon digital design, in that the component-level design of these devices is no longer required, or expected, of a digital systems designer.

11.1 Digital-to-Analog Conversion

Figure 11-0 is a general diagram of a voltage-output DAC. The digital code word that is to be converted into analog form is applied to the input of the

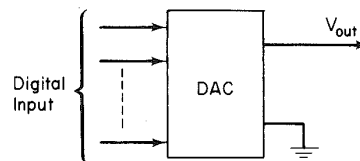


Figure 11-0. A Voltage-output Digital-to-Analog Converter

DAC. The internal circuitry of the DAC interprets the TRUE/FALSE values of the bits of the digital code word and produces the appropriate output voltage, V_{out} .

The output voltage can be related to the digital input in three ways: random, linear, or nonlinear. A random DAC must be defined by a tabulation of the coded inputs and the voltages that each should produce. An example of this type of tabulation is given in Table 11-0. A random DAC can be constructed as shown in Fig. 11-1. Each input code word is used to close a relay that connects the appropriate voltage to the DAC output. The code words are decoded by using normal combinational logic. Each of the logical signals is buffered by an appropriate relay driver circuit. Solid-state switching can be used if the DAC must operate at higher speeds.

Table 11-0: A Random DAC

Digital Input	Voltage Output (V)
000	+10.0
001	-10.0
010	+5.0
011	-3.0
100	-1.5
101	+3.6
110	+7.2
111	0.0

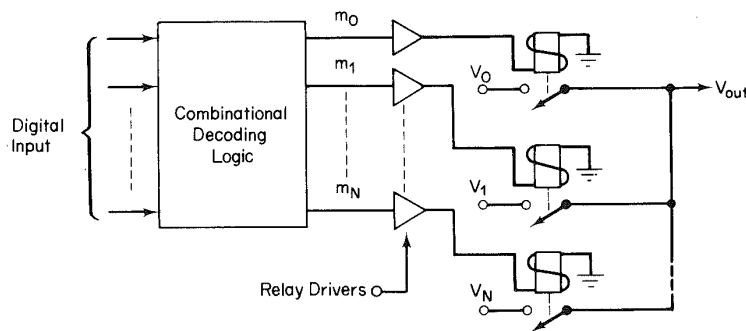


Figure 11-1. A Random DAC

A random DAC having n input bits may require as many as 2^n voltage sources and 2^n switches or relays. As the number of input bits increases, this requirement increases exponentially.

The random DAC may exhibit erratic behavior during the period just following a change in its digital input. An asynchronous change may cause the brief appearance of transition states at the input, and several relays or switches may be activated in rapid sequence. This will cause a rapid variation in V_{out} . Also, if two or more switches are closed at the same time, the short circuit that results may damage the switches or the voltage sources. Thus, the use of fully synchronous input changes or a unit-distance coding technique is generally advisable with a random DAC.

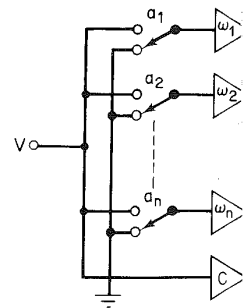
A linear DAC differs from the random DAC in that its output voltage is directly related to the magnitude represented by its digital input. Linear DACs can also be made to operate with signed numbers, with the polarity of the output voltage changing in accordance with the sign of the input code word.

A linear DAC can make a voltage increment, which is the digital input by the voltage can make; it is the quantization voltage. The DAC receives at its input. If the unit voltage is received of the DAC must be 2^n code words are allowed.

The voltage output $V_{max} \leq 2^n v$, or it can be a positive upper limit. in Table 11-1. The unit

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A linear DAC can be a random DAC in Fig. 1 by using a voltage sum in generalized form, in



A linear DAC can be characterized by two parameters. One is the *unit voltage increment*, which is the change in voltage that corresponds to increasing the digital input by one unit. This is the smallest change that the output voltage can make; it is also called the *step voltage*, the *unit voltage*, or the *quantization voltage*. The second parameter is the number of bits that the DAC receives at its input. An n -bit DAC can receive 2^n different code words. If the unit voltage is represented by v , then the range of the output voltage of the DAC must be $2^n v$ or less. It will be less than this value if not all the 2^n code words are allowed, as when BCD code is used as the input.

The voltage output from a linear DAC can begin at 0 and increase to $V_{\max} \leq 2^n v$, or it can be biased to work between a negative lower limit and a positive upper limit. A tabulation describing a typical linear DAC is given in Table 11-1. The unit voltage for this DAC is 0.1 V.

Table 11-1: A Three-Bit Binary DAC

Binary Input	Voltage Output (V)
000	0.0
001	0.1
010	0.2
011	0.3
100	0.4
101	0.5
110	0.6
111	0.7

A linear DAC can be constructed according to the schematic given for a random DAC in Fig. 11-1. A better approach, however, is to use a weighted code to represent the input quantity and to implement the DAC operation by using a voltage summing amplifier. This type of arrangement is shown, in generalized form, in Fig. 11-2. Only n switches, $n + 1$ fixed-gain voltage

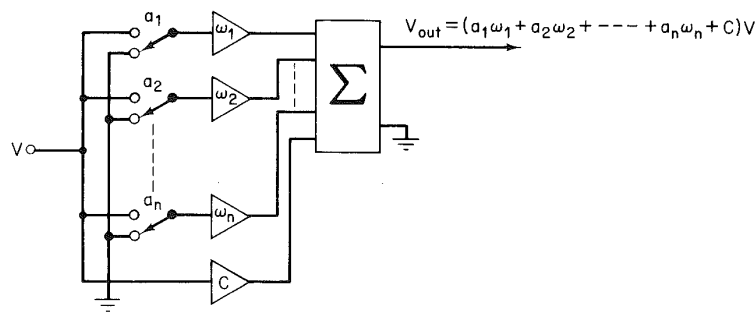
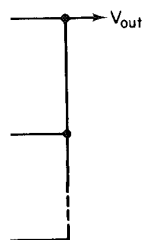


Figure 11-2. A Linear DAC



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amplifiers (one extra to allow for the bias constant, if the weighted code has one), and one voltage summing amplifier are required. Each TRUE bit of the input code word closes a switch, thereby applying a voltage that is proportional to the weight of that bit to the summing amplifier. Input bits that are FALSE leave their switches tied to 0. The summing amplifier adds the various voltages that it receives, including any fixed-bias voltage, and produces the output voltage.

EXAMPLE 11-0: Show a DAC that will operate with one digit of 8421 BCD code.

Answer: See Fig. E11-0.

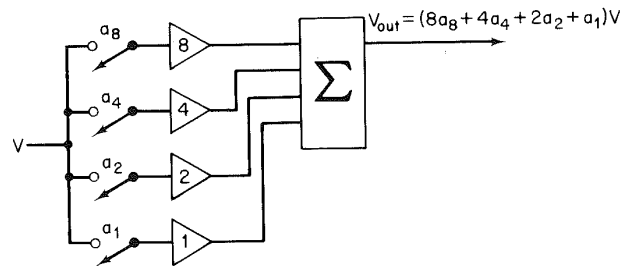


Figure E11-0

EXAMPLE 11-1: Show a DAC for use with one digit of the 6, 3, 1, -1 code.

Answer: See Fig. E11-1.

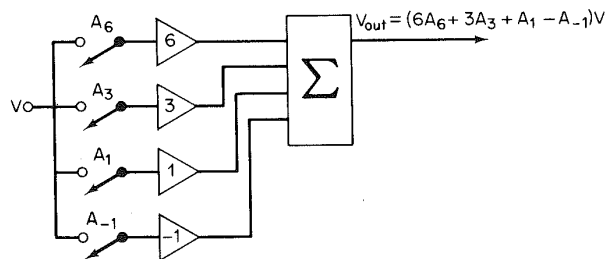
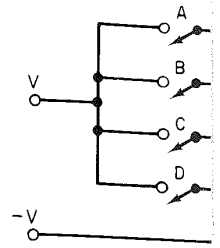


Figure E11-1

EXAMPLE 11-2: Show a DAC for use with one digit of the XS3 code.

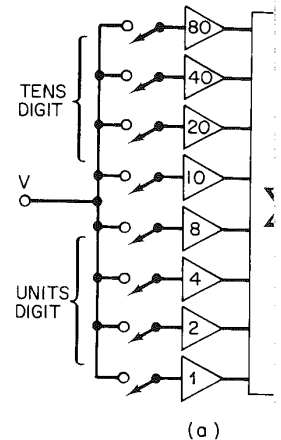
Answer: See Fig. E11-2.

Sec. 11.1



EXAMPLE 11-3: Show a DAC for use with one digit of the 8421 BCD code.

Answers: See Fig. E11-3.



A DAC of the type illustrated in Fig. E11-3(a) is called a *ladder decoder network*. The operational amplifier is used to sum the voltages during the voltage summation, thereby differing input impedance summing amplifier.

Also, special resistances and *ladder decoder network* voltage summing operation DACs are given in Refs. [1] through [4].

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$a_2 + a_1)V$

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XS3 code.

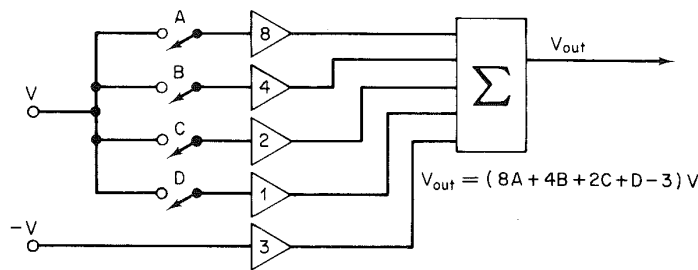


Figure E11-2

EXAMPLE 11-3: Show two ways to arrange a two-digit DAC for use with 8421 BCD code.

Answers: See Fig. E11-3a and b.

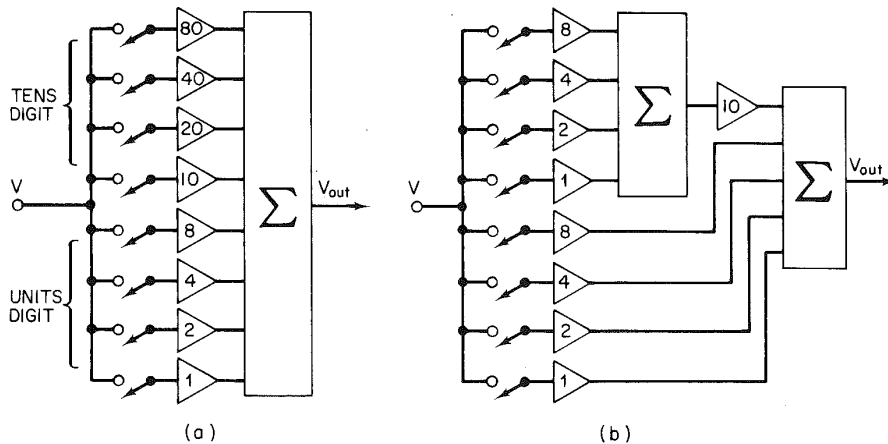


Figure E11-3a, b

A DAC of the type illustrated in Exs. 11-2 and 11-3 can be designed for any weighted code. The summing amplifier can be constructed from an operational amplifier. The various weighting voltages are then obtained by using a single voltage source and varying the gain that each input receives during the voltage summing process. This can be accomplished by using differing input impedances between the switched voltage sources and the summing amplifier.

Also, special resistance networks, notably the *weighted resistor network* and *ladder decoder networks*, can be used to perform both the weighting and voltage summing operations. Details on all of these facets of the design of DACs are given in Refs. [2], [3], and [4].

Linear DACs can be made to operate with signed codes as well. Figure 11-3 shows how an analog inversion amplifier (gain of -1) can be used to implement the conversion of a sign-and-magnitude number into its analog equivalent. The conversion of a sign-and-complement number is even easier, since the sign bit has a numerical weight just like the other bits. Figure 11-4 shows a five-bit DAC that operates with 2's complement binary input. A similar arrangement can be used with signed decimal numbers.

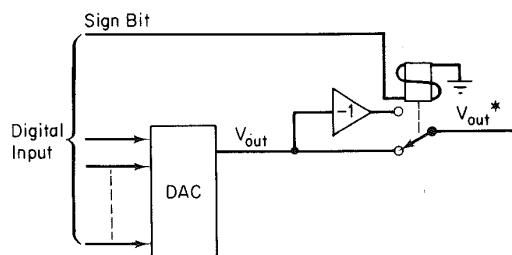


Figure 11-3. A DAC for use with Sign-and-Magnitude Code

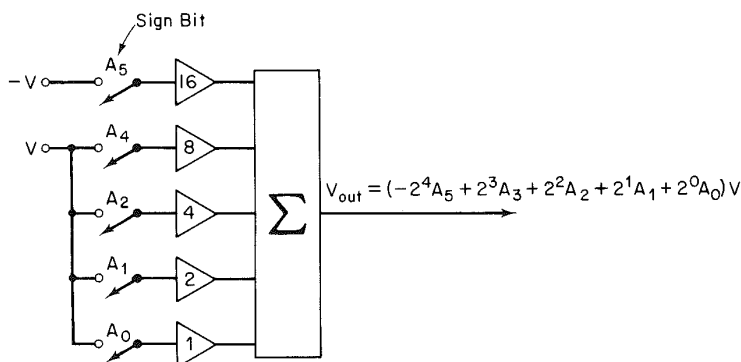


Figure 11-4. A 2's Complement DAC

The nonlinear DAC generates an output voltage that is nonlinearly related to the magnitude of its digital input. Typical input/output relationships include logarithmic and square-root converters. These types of DACs are used in special-purpose situations. Their design is not discussed herein.

Of major concern to the digital designer is the widening availability of DACs that are preengineered and packaged as complete conversion systems (Refs. [1] and [5]). These devices offer low cost and standardization. Most commercially available DACs are designed for use with binary or 8421 BCD input. This may require some code conversion prior to the input to the DAC. The component parts of the DAC, e.g., the voltage switches,

the weighting resistance is able as predesigned components into a "custo

11.2 Analog-to-Digital C

The analog-to-digital co digital-to-analog conversi component part of their oper is shown in Fig. 11-5. The

Input
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Figure 11-5. A Generalized

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The logical control sy comparator to determine b the DAC. This code is inc with the voltage input with than the quantization uni require a more complex D conversion.

The key to the opera logic seeks to find the dig voltage. There are severa between operational useful zation of each of these typ

11.2.1. The Ramp AD

in Fig. 11-6. The DAC is that is compatible with the counter being reset to 0. Th ter, with the counting co

s well. Figure 11-4 can be used to convert its analog input to digital. This is even easier, as shown in Figure 11-4. A similar input. A similar

the weighting resistance networks, or the summing amplifier, are also available as predesigned components. Thus, a designer can assemble off-the-shelf components into a "customized" DAC.

11.2 Analog-to-Digital Conversion

The analog-to-digital conversion process is closely related to its inverse, digital-to-analog conversion. In fact, almost all ADCs use a DAC as a component part of their operational hardware. A general diagram for an ADC is shown in Fig. 11-5. The voltage that is to be converted, or *digitized*, to use

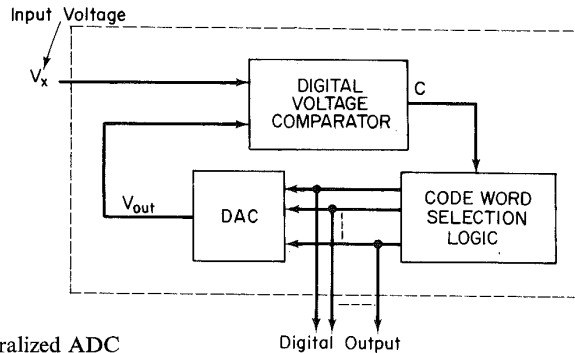


Figure 11-5. A Generalized ADC

the common jargon, is applied to the ADC. This voltage, V_x , is compared with the output from a DAC, V_{out} . The comparison device is a *digital voltage comparator*, which is usually a high-gain differential amplifier whose logical output, C , assumes one of the two logical voltage levels when $V_x < V_{out}$ and assumes the other voltage level when $V_x > V_{out}$.

The logical control system of the ADC uses the output signal from the comparator to determine how to change the digital code word that is driving the DAC. This code is increased or decreased until the DAC output agrees with the voltage input within some tolerance. This tolerance can be no better than the quantization unit of the DAC. Thus, a more accurate ADC will require a more complex DAC and will probably take more time to make its conversion.

The key to the operation of the ADC is the way in which its control logic seeks to find the digital code that most closely represents the input voltage. There are several common techniques, each offering a trade-off between operational usefulness and hardware complexity. The basic organization of each of these types is that shown in Fig. 11-5.

11.2.1. The Ramp ADC. The block diagram for a *ramp* ADC is shown in Fig. 11-6. The DAC is driven by an up-counter that counts in the code that is compatible with the DAC. The conversion process begins with the counter being reset to 0. The system clock is then used to increment the counter, with the counting continuing until the output of the DAC becomes