

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIFIED PATENTS INC.
Petitioner

v.

MLC INTELLECTUAL PROPERTY, LLC
Patent Owner

Case IPR2015-00517
Patent 5,764,571

**PATENT OWNER'S PRELIMINARY RESPONSE
TO PETITION**

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R § 42.107, Patent Owner MLC Intellectual Property, LLC (“MLC”) respectfully submits this preliminary response to Unified Patents, Inc.’s (“Unified”) Petition for *Inter Partes* Review (“Petition”). U.S. Patent No. 5,764,571 (the “’571 patent”), the patent that is the subject of Unified’s Petition, has been widely licensed by the world’s leading semiconductor companies, including Intel Corporation, Toshiba Corporation, Hynix Semiconductor, Inc., and Samsung Electronics Co. Ltd.

In August 2014, MLC sued Micron Technology, Inc. (“Micron”) for patent infringement. Micron is the lone holdout of the globe’s chief NAND Flash manufacturers, refusing to pay for the rights that its competitors recognized were necessary to the manufacture and sale of their flash memory products. On December 24, 2014, Micron filed a petition for *inter partes* review. Six days later, Unified, a self-described protector of technology sectors from the threat of “NPE litigation,” filed its Petition. The Unified Petition is identical to Micron’s Petition in IPR2015-00504 (the “Micron IPR”). As explained below, a trial should not be instituted in this matter because Unified cannot demonstrate that there is a reasonable likelihood that at least one of the challenged claims of the ’571 patent is unpatentable.

II. UNIFIED PATENTS

Unified is an organization that claims to address the risk and cost associated with litigation filed by non-practicing entities by protecting areas of technology, such as cloud storage and content delivery.

Companies in a technology sector subscribe to Unified's technology specific deterrence, and in turn, Unified performs many NPE-deterrent activities, such as analyzing the technology sector, monitoring patent activity (including patent ownership and sales, NPE demand letters and litigation, and industry companies), conducting prior art research and invalidity analysis, providing a range of NPE advisory services to its subscribers, sometimes acquiring patents, and sometimes challenging patents at the United States Patent and Trademark Office (USPTO).

Paper 1 at iv-2; *see also Unified Patents Inc. v. Dragon Intellectual Property, LLC*, IPR2014-01252, Paper 37 at 8 (Feb. 12, 2015) (same). In this case, Unified's deterrence activities include lifting the Micron Petition and photocopying the supporting exhibits. *See, e.g.*, Ex. 1003 at 1 ("My name is R. Jacob Baker . . . I have been retained on behalf of Petitioner Micron Technology, Inc. ("Micron") to provide this Declaration").

Despite filing the exact same petition as Micron and copying its exhibits, Unified strangely denies knowledge of the Micron proceeding. *See* Paper 1 at 3 ("Petitioner is not aware of any previous disclaimers, reexamination certificates or petitions for *inter partes* review of the '571 patent."). Even more bizarrely,

Unified then identifies that an exhibit in the Micron IPR was not available to it because the exhibit is confidential. *See id.* at iii (“Ex. 1011 Not used (Ex. 1011 in IPR2015-00504 is not available to Petitioner as it is confidential.)”).

III. TECHNOLOGY BACKGROUND AND INVENTOR’S SOLUTION

The ’571 patent is titled Electrically Alterable Non-Volatile Memory with N-Bits Per Cell. The patent was issued on June 9, 1998 and claims priority to an application filed on February 8, 1991. The ’571 patent is part of a portfolio related to memory technology known as Multi-Level Cells (MLC) flash. The entire patent portfolio is owned by MLC and was developed by one of MLC’s members, Gerald Banks.

The ’571 is directed to a multi-level electrically alterable non-volatile memory device that includes memory cells with more than two predetermined memory states. *See* Ex. 1001, Col. 2:50-53 (“The present invention provides a multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two distinct states.”). Non-volatile memory stores bits of information when power is removed. The ’571 patent also is directed to a method of programming the MLC devices, and to reliable ways of verifying the programming. *See id.*, Col. 2:61-66 (“The present multi-level memory device also includes a memory cell programming means for programming the multi-level cell means to a state corresponding to the input

information. A comparator means for comparing the memory state of the multi-level cell means with the input information is also included.”).

MLC enables the storage of two or more bits of data in a single memory cell. One memory cell storing two bits may be programmed to four different memory states: 00, 01, 10, and 11. This is an improvement on conventional single-level cells that store only one bit of information and can be programmed to two memory states: 1 or 0. At the time of the invention, “prior art electrically alterable multiple-bit per cell memory approaches store[d] multiple levels of charge on a capacitive storage element, such as is found in a conventional dynamic random access memory (DRAM) or a charge coupled device (CCD).” *Id.*, Col. 2:13-17. But “[a]ll of these approaches use volatile storage, that is, the charge levels are not permanently stored.” *Id.*, Col. 2:21-22; *see also id.*, Col. 2:25-28 (“All of these approaches have the common characteristics that whatever information is stored on such a memory cell is volatile because such a cell loses its data whenever power is removed.”). As the patent recognized, “[i]t would be advantageous to develop a multi-bit semiconductor memory cell that has the non-volatile characteristic of a mask programmable read-only-memory (ROM) and the electrically alterable characteristic of a multi-bit per cell DRAM.” *Id.*, Col. 2:31-35.

The ’571 patent, therefore, describes an improvement over the prior art by providing a memory device that can be programmed electrically to store multiple

bits of data per cell while maintaining the programmed data when power is removed. Non-volatile MLC flash memory is a cost-effective, high density storage solution typically found in consumer electronic products, including digital cameras, smart phones, USB memory sticks, solid state drives and portable music players.

IV. THE DIGITAL-TO-ANALOG CONVERSION CIRCUIT OF KITAMURA DOES NOT DISCLOSE A “REFERENCE VOLTAGE SELECTING MEANS.”

Unified contends that Claim 1, 9, 10, 12, 30, 42, and 45 are obvious under 35 U.S.C. § 103 over an unexamined Japanese patent application publication no. S62-34398 to Yoshinari Kitamura (hereinafter “Kitamura” or “the Kitamura Reference”). Paper 1 at 4. Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires a number of threshold inquiries. The level of ordinary skill in the art must be established. The scope and content of the prior art must be determined, and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966).

If a single element of the claim is absent from the prior art, the claims cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int'l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 409 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int'l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case No. IPR2012-00001, Paper 15 at 15 (P.T.A.B. Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations). As explained below, Unified has not established a reasonable likelihood that at least one of the challenged claims of the '571 patent is unpatentable because the alleged prior art plainly does not disclose all claim limitations.

Claim 1 of the '571 patent claims the following:

1. A multi-level memory device comprising:

an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;

memory cell programming means for programming said multi-level memory cell in accordance with said input information;

reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said

input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and

comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.

Ex. 1001, Claim 1. The Petition plainly fails to disclose a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information.”

Unified purports to identify the “reference voltage selecting means” as a digital-to-analog conversion circuit. Paper 1 at 29 (identifying the “selecting device” as a “D/A conversion circuit 10”); 35 (“a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal”). Based on the evidence and arguments submitted, Unified cannot persuasively demonstrate that a digital-to-analog conversion circuit makes a selection of any type, let alone a selection of a plurality of reference voltages. There is no evidence of record, aside from Unified’s conclusory, self-serving statements that makes this so.

The Kitamura Reference discloses that the digital-to-analog conversion circuit converts input digital signals (B_0 and B_1) and outputs an analog signal. *See* Ex. 1010 at ¶ [09] (“[T]he two-bit input digital signals B_0 and B_1 to be written are **converted** by the D/A conversion circuit 10 into analog signals,”) (emphasis

added). There is no disclosure in Kitamura that the digital-to-analog conversion circuit “selects” a reference signal. *See* Ex. 1010 at ¶ [01] (describing “a D/A conversion circuit that converts a plurality of bits of digital signal into an analog signal”).

Unified presents no evidence or reason to believe that the conversion of digital input signals to an analog signal involves a “selection” of “one of a plurality of reference voltages.” Aware of the problem, Unified seeks to overcome it by doing nothing more than saying there is a selection, but it never explains how there is a selection or what is selected. *See* Paper1 at 21-22 (“[T]he Kitamura memory device includes . . . a D/A (digital-to-analog) conversion circuit 10 to select (based on input bits B_0 and B_1) the reference signal/information corresponding to the desired memory state for the cell 1,”); 23 (“By way of example, if the values of input bits B_0 and B_1 are 1 and 0, respectively, the D/A conversion circuit 10 would select and provide an analog signal of 2.5 Volts to the comparator 9 to represent the memory state to which the memory cell 1 is to be programmed.”). Indeed, Unified resorts to simply flinging the idea of “selection” into its argument but cites nothing supporting the notion that the conversion circuit disclosed in Kitamura makes a “selection” rather than, as Kitamura explains, a “conversion.” *See* Paper 1 at 22 (“These desired memory state defining input bits are fed into the D/A conversion circuit 10. In turn, the D/A conversion circuit 10 converts the two

digital bits B_0 and B_1 to an analog signal by selecting the analog signal that corresponds to bits B_0 and B_1 .”).

Perhaps Unified’s argument lies in an improperly broad construction of the plain meaning of the term “selection.” *See, e.g.*, Paper 1 at 8 (“[A] person of ordinary skill in the art would have interpreted this feature to be broad enough to include and be met by a device or process that takes in-put information (*e.g.*, in an n-bit form) and selects, for a given cell’s program/verify cycle, a reference voltage from a plurality of reference voltages, where the selected reference voltage is based on the input information (*e.g.*, desired memory state).”). Typically, a claim in an IPR is given its “broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. §42.100(b). *See In re Prater*, 415 F.2d 1393, 1404-05 (C.C.P.A. 1969) (“[T]his court has consistently taken the tack that claims yet unpatented are to be given the broadest reasonable interpretation consistent with the specification during the examination of a patent application since the applicant may then amend his claims, the thought being to reduce the possibility that, after the patent is granted, the claims may be interpreted as giving broader coverage than is justified.”).

When a patent is set to expire during the pendency of an IPR, as the ’571 patent is here, then the standard for claim construction shifts from the broadest reasonable interpretation to the standard applied in district court. *In re Rambus*,

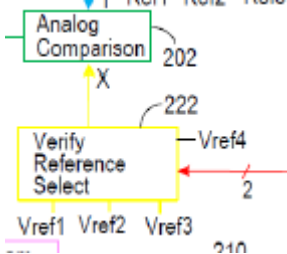
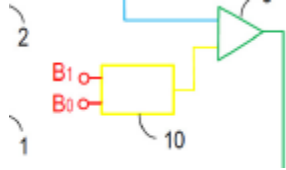
Inc., 694 F.3d 42, 46 (Fed. Cir. 2012) (“[T]he Board’s review of the claims of an expired patent is similar to that of a district court’s review.”) (citations omitted); *see also* Paper 1 at 5 n.2 (“When a patent is set to expire during the pendency of an *inter partes* review then the standard for claim construction shifts from the broadest reasonable interpretation standard to the *Markman* standard.”).

These two standards are not the same. District courts apply a different standard that gives terms of a patent their ordinary and customary meanings, not the broadest reasonable interpretation. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005); *Facebook, Inc. v. Pragmatus AV, LLC*, 582 Fed. Appx. 864, 869 (Fed. Cir. 2014) *reh’g denied* (Oct. 30, 2014) (non-precedential) (“The broadest reasonable interpretation of a claim term may be the same as or broader than the construction of a term under the Phillips standard. But it cannot be narrower.”). Unified suggests that its proposed claim constructions “should not be affected by the standard applied.” Paper 1 at 5 n.2. But any construction that seeks to define “selecting” as “converting” violates the principle that terms are given their ordinary and customary meaning.

The Kitamura Reference also fails to disclose “a plurality of reference voltages in accordance with said input information.” Indeed, the figures that Unified annotates that purport to demonstrate that there are no differences between

the '571 patent and Kitamura highlight this substantial distinction. *See* Paper 1 at 31.

Figure 8 of the '571 patent clearly shows the “plurality of reference voltages” that are selected by the “verify reference voltage selection circuit 222.” '571 patent, FIG. 8 (showing “Vref1,” “Vref2,” “Vref3,” and “Vref4”). Figure 1 of Kitamura shows nothing more than the digital-to-analog converter that converts the digital inputs (B_0 and B_1) into an analog waveform. Ex. 1010, FIG. 1.

'571 patent, FIG. 8	Ex. 1010, FIG. 1
	

Unified presents no persuasive argument or evidence that supports the position that Kitamura discloses a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information.” In the absence of such a showing, Unified has not carried its burden to establish a reasonable likelihood that any claim of the '571 patent will be found unpatentable.

V. THE RPLSR CIRCUIT OF MEHROTRA DOES NOT DISCLOSE A “REFERENCE VOLTAGE SELECTING MEANS”

Unified contends that claims 1, 9, 12, 30, 32, 42, and 45 are obvious over U.S. Patent No. 5,172,338 to Mehrotra *et al.* (hereinafter “Mehrotra” or “the

Mehrotra Reference”). Paper 1 at 4. During prosecution of the application that resulted in the ’571 patent, the applicant submitted Mehrotra in an Information Disclosure Statement on May 15, 1997. Ex. 1002 at 124-131. The reference was considered by the Examiner and appropriately was not the basis of a rejection. *Id.*

As discussed above, claim 1 of the ’571 patent requires “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states.” Unified has not established a reasonable likelihood that at least one of the challenged claims of the ’571 patent is unpatentable over the Mehrotra Reference because Mehrotra does not disclose or suggest that limitation. *See CFMT*, 349 F.3d at 1342 (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 409 F.2d at 985)).

Unified purports to identify the “reference voltage selection means” as a read/program latches and shift registers (RPLSR) circuit. Paper 1 at 41 (identifying that the Mehrotra memory device selects through the RPLSR); 49 (stating “the data is staged for programming the addressed cell by being sent via a serial data line 259 to a set of read/program latches and shift registers 190”). Unified cannot persuasively establish that a latch or shift register makes a selection.

The Mehrotra Reference discloses that data to be programmed into a memory cell are latched or stored in the RPLSR circuit. *See* Ex. 1004 at 19:27-56 (“The N*L data bits are ***stored*** in latches and shift registers 190 where the serial bits are converted to N*L parallel bits...”)(emphasis added); 19:65-66 (“In FIG 15(3), the N*L bits of parallel data is ***latched*** in latches 190.”)(emphasis added).

Unified presents no evidence that the ***latching*** or ***storing*** of data bits involves a “selection” or a selection of “one of a plurality of voltage references.” To overcome the problem, Unified merely states there is a selection and cites to its expert’s declaration. *See* Paper 1 at 41 (“To provide the desired memory state information to the Compare Circuit 200, the Mehrotra memory device *e.g.*, through the RPLSR 190, selects and provides a voltage or current signal(s) or waveform(s) that represents the desired memory state to the Compare Circuit 200.”)(citing Ex. 1003 ¶¶ 95-104). The cited paragraphs of Dr. Baker’s declaration contain similar conclusory statements and include no supporting evidence. *See* Ex. 1003 ¶ 97 (“To provide the program information, *e.g.*, two-bit desired memory state information to the Compare Circuit 200, the RPLSR must select and provide an encoded signal that represents the desired memory state to the Compare Circuit 200.”). Dr. Baker includes a footnote citing to a textbook excerpt for supposed support that the RPLSR circuit must “select and provide an encoded signal.” Ex. 1003 at 56 n.21. The referenced page is reproduced below:

2 INTRODUCTION

measured by a multitude of sensors. Communication makes it possible for computers to interact. The list of applications involving the use of communications in one way or another goes on.¹

In the most fundamental sense, *communication* involves implicitly the transmission of information from one point to another through a succession of processes, as described here:

1. The generation of a thought pattern or image in the mind of an originator.
2. The description of that thought pattern or image, with a certain measure of precision, by a set of aural or visual symbols.
3. The encoding of these symbols in a form that is suitable for transmission over a physical medium (channel) of interest.
4. The transmission of the encoded symbols to the desired destination.
5. The decoding and reproduction of the initial symbols.
6. The re-creation of the original thought pattern or image—with a definable degradation in quality—in the mind of a recipient, with the degradation being caused by imperfections in the system.

The form of communication just described involves a thought pattern or image originating in a human mind. Of course, there are many other forms of communication that do not directly involve the human mind in real time. In space exploration, for example, human decisions may enter only the commands sent to the space probe or to the computer responsible for processing images of far-away planets (e.g., Mars, Jupiter, Saturn) that are sent back by the probe. In computer communications, human decisions enter only in setting up the computer programs or in monitoring the results of computer processing.

Whatever form of communication is used, some basic signal-processing operations are involved in the transmission of information. The next section describes the different types of signals encountered in the study of communication systems. The signal-processing operations of interest are highlighted later in the chapter.

....1.2 SIGNALS AND THEIR CLASSIFICATIONS

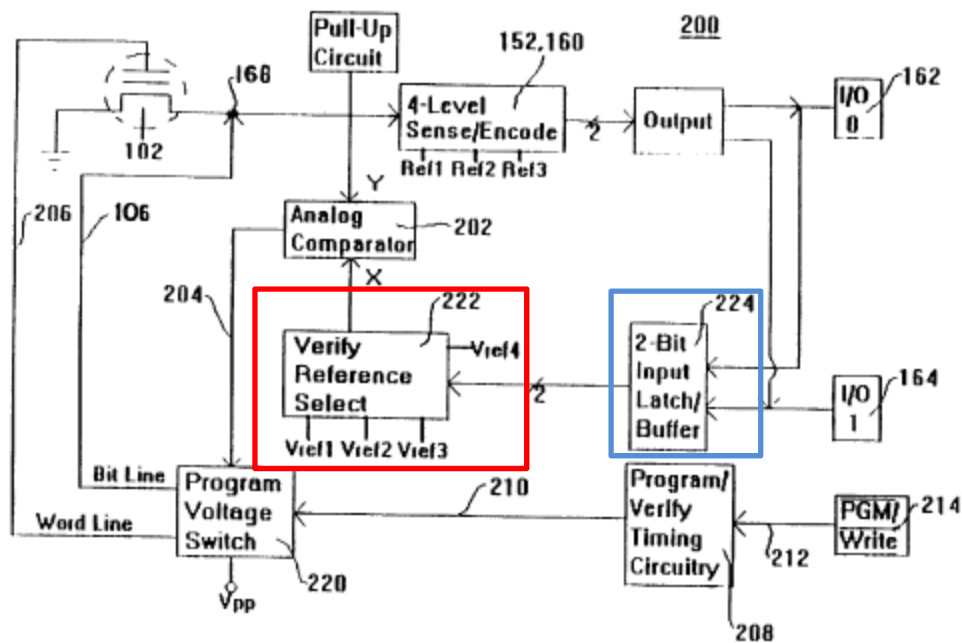
For our purposes, a *signal* is defined as a single-valued function of time that conveys information. Consequently, for every instant of time there is a unique value of the function. This value may be a real number, in which case we have a *real-valued signal*, or it may be a complex number, in which case we have a *complex-valued signal*. In either case, the independent variable (namely, time) is real-valued.

¹For an essay on communications, see Berkner (1962).

Ex. 1008 at 4. It is unclear what significance Exhibit 1008 holds, or how it is relevant to discussion of whether RPLSR 190 “selects” “one of a plurality of reference voltages.”

Unified and its expert attempt to insert the idea of “selection” into their argument, but cite nothing to support the contention that the RPLSR circuit disclosed in Mehrotra “selects” rather than “latches,” “stores,” or “stages for programming.” *See* Ex. 1004, FIG. 15; Col. 8:24-27 (“the data is staged for programming the addressed cell by being sent via a serial data line 259 to a set of read/program latches and shift registers 190.”). None of those functions is equivalent to “selecting” and Unified does not explain how it could be considered similar.

What is more, Figure 8 of the ’571 patent, reproduced and annotated below, distinguishes between the “verify reference select [circuit] 222” (outlined in red) and a “2-bit input latch/buffer 224” (outlined in blue). The ’571 patent states that the verify reference voltage selection circuit is controlled by the output of the latch/buffer circuit 22, *see* Ex. 1001, Col. 8:40-43 (“The verify reference voltage select circuit 222 is controlled by the 2-output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O terminals 162 and 164.”), but they are hardly the same.



Ex. 1001, FIG. 8. Mehrotra’s RPLSR circuit performs the same functions (*e.g.*, latching, storing, staging) as the “2-bit input latch buffer 224.” And since Unified purports to argue that the RPLSR circuit in Mehrotra is the verify reference select circuit of the ’571 patent, Unified cannot persuasively demonstrate that Mehrotra’s RPLSR circuit satisfies the “reference voltage selecting means” of the ’571 patent, the corresponding structure of which Unified admits is the verify reference select circuit 222. *See* Paper 1 at 6 (“The claimed function is ‘selecting one of a plurality of reference voltages in accordance with said input information’ and the corresponding structure described in the specification is the verify reference voltage select circuit 222.”).

The Mehrotra Reference also fails to disclose “a plurality of reference voltages in accordance with said input information.” As discussed and shown above, Figure 8 of the ’571 patent clearly shows the “plurality of reference voltages” that are selected by the “verify reference voltage selection circuit 222.” *See* Ex. 1001, FIG. 8 (the plurality of reference voltages denoted as “Vref1,” “Vref2,” “Vref3,” and “Vref4.”). Unified presents no persuasive argument or evidence that supports the position that Mehrotra discloses a “reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information.” In the absence of such a showing, Unified has not carried its burden to establish a reasonable likelihood that any claim of the ’571 patent will be found unpatentable.

VI. UNIFIED DOES NOT SEEK INSTITUTION OVER MEHROTRA IN COMBINATION WITH ANY OTHER REFERENCES.

Unified acknowledges that the Mehrotra Reference is limited to a digital implementation and turns to additional references to support its obviousness contention. *See* Paper 1 at 19 (“[T]he prior art references Kitamura, Mehrotra, *Lee, and Kokubun* show the features claimed in the ’571 patent were known and disclosed in several different contexts and through several different techniques.”) (emphasis added). Specifically, Unified relies on U.S. Patent No. 4,952,821 to Kokubun (“Kokubun”) and U.S. Patent No. 5,319,348 to Lee et al. (“Lee”) to disclose an analog comparison process. *Id.* at 44 (citing to Exhibits 1005

(Kokubun) and 1006 (Lee) to argue that “one of ordinary skill in the art would have been motivated to implement an analog version of the Mehrotra comparison process”). Unified’s expert points to Kokubun and Lee to cure the deficiencies in Mehrotra. *See* Exhibit 1003 at ¶¶ 98, 99, 100, 101 (citing to Kokubun as describing “such an analog comparison implementation”); ¶¶ 100, 101, 102, n.24 (citing to Lee as showing “use of an analog comparator in a computer system memory device”). Unified concedes that Mehrotra, unlike Kitamura, alone does not teach or suggest all of the limitations of the challenged claims. *See* Paper 1 at 59 (“As compared with using additional references (*e.g.*, Lee and/or Kokubun) to illustrate the analog verification process made obvious by Mehrotra, Kitamura explicitly describes such an analog implementation.”).

Unified has not demonstrated that Mehrotra is sufficient, without additional reference to Kokubun and Lee, to render the asserted claims the ’571 patent obvious. Moreover, Unified has not sought institution on grounds including Kokubun or Lee. *See* Paper 1 at 4 (seeking institution solely on Kitamura and Mehrotra). Even if it had properly requested institution on Mehrotra in combination with Kokubun and/or Lee, Unified has only attempted to show that separate elements of the ’571 patent were known in the art. *See Conopco, Inc. v. The Procter & Gamble Co.*, IPR2013-00509, Paper 10 at 12-13 (P.T.A.B. Feb. 12, 2014). Unified has not established that there is a reasonable likelihood that any

claim of the '571 patent will be found unpatentable.

VII. UNIFIED'S PETITION SHOULD BE DENIED BECAUSE IT IS DUPLICATIVE OF THE MICRON PETITION.

The Board may deny a duplicative petition like Unified filed in this case.

See 35 U.S.C. § 325(d) (“In determining whether to institute or order a proceeding under this chapter, chapter 30 or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”). The Board has discretion to deny a petition that would hinder the efficient administration of the Office. *See* 35 U.S.C. § 316(b) (“[T]he Director shall consider . . . the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.”).

In *Unified Patents, Inc. v. PersonalWeb Technologies & Level 3 Communications*, IPR2014-00702, Paper 13 (P.T.A.B. July 24, 2014), another proceeding initiated by Unified, the Board denied institution because the petition challenged claims that were already the subject of another *inter partes* review over the same prior art. *See PersonalWeb Techs.*, IPR2014-00702, Paper 13 at 7 (“We have discretion under 35 U.S.C. § 325(d) to reject a petition when the same or substantially the same prior art or arguments were presented previously in another proceeding before the Office.”); 8-9 (“Taking into consideration the efficient administration of the Office under 35 U.S.C. § 316(b) . . . we exercise our

discretion under 35 U.S.C. § 325(d) and deny the Petition in this proceeding because the same or substantially the same prior art and arguments were previously presented”). *See also Prism Pharma Co., Ltd. v. Choongwae Pharma Corp.*, IPR2014-00315 Paper 13 at 13 (P.T.A.B. Jul 8, 2014) (denying petition because “the same prior art and substantially the same arguments were presented to the Office previously”).

Here, Unified challenges each claim that is already the subject of Micron’s first filed petition in IPR2015-00504, requests the exact same grounds for review, and makes identical arguments. *Compare* Paper 1 at 4 *with* Paper 2 at 3 in IPR2015-00504. The Board should exercise its discretion under 35 U.S.C. § 325(d) and deny the Petition in this proceeding.

VIII. CONCLUSION

For the foregoing reasons, Unified has not established a reasonable likelihood that any claim of the ’571 patent will be found unpatentable. Unified’s Petition for IPR should be denied.

Dated: April 27, 2015

By: /s/ Jason S. Angell
Jason S. Angell
Reg. No. 51408
Counsel for Patent Owner

CERTIFICATE OF SERVICE

It is certified that a copy of the foregoing has been served on Petitioner via electronic mail transmission addressed to the person(s) at the address below:

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