

# Exhibit 1005

# A Digital Tuner for Wideband Receivers

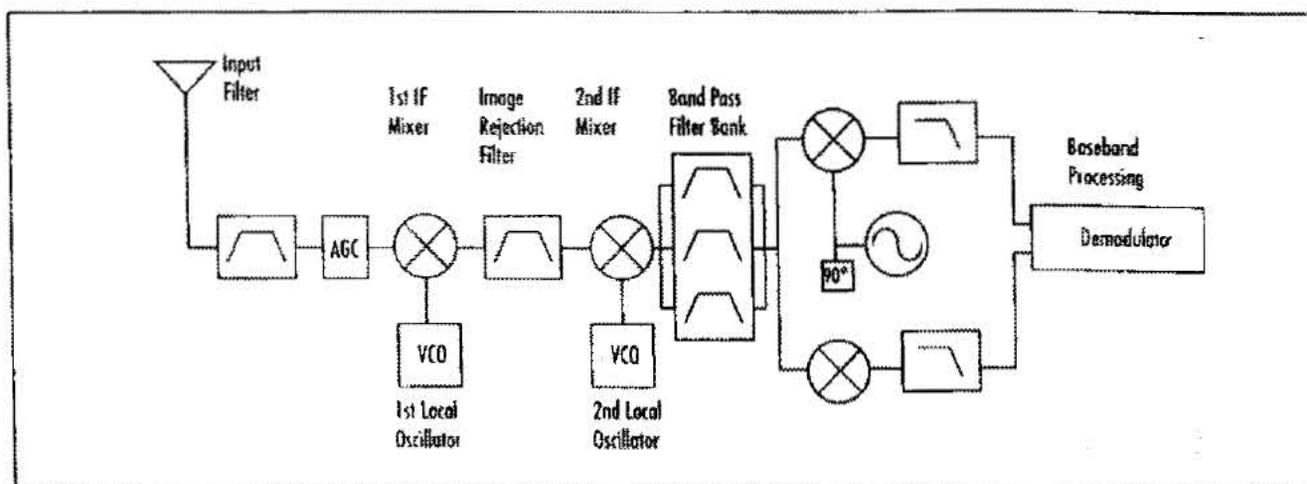


Figure 1: High level block diagram of a single channel receiver

By Clay Olmstead and Mike Petrowski

Advances in both analog to digital conversion (ADC) and VLSI technologies have opened the door for the use of DSP techniques over an expanding range of high sample rate applications. Foremost among these is the use of standard off the shelf DSP IC's as digital replacements for the analog intermediate frequency (IF) processing stage in wideband receivers. Using this approach, the designer can take advantage of operational stability over time and temperature offered by digital technology, while realizing performance and flexibility unmatched by older analog implementations.

In recent years there has been increasing interest in the topic of wideband receivers. These are receivers that can tune on a narrow band radio signal that exists in a broad spectrum of interest. The typical system in this application may be capable of extracting a signal as narrow as a few kHz out of a spectrum that spans tens, hundreds, or even thousands of MHz.

Because of the prohibitive cost of these receivers in the past, they were confined to use by the military, government agencies, and high end commercial users. Today however, more widespread commercial communications systems are dependent on cost effective implementations of receivers. Cellular telephones, mobile radio, and wireless LANs are but a few examples of potential applications for DSP.

To better understand alternative wideband receiver designs using DSP, first consider the structure of the single channel wideband receiver as shown in Figure 1. As implied by the name, the single channel receiver is designed to receive and decode information within a single frequency band at a time. For the purposes of this discussion it will be assumed that one frequency band corresponds to one channel with no distinction between a frequency band and logical channels. When information is to be received from a different channel, the receiver must be tuned to the new

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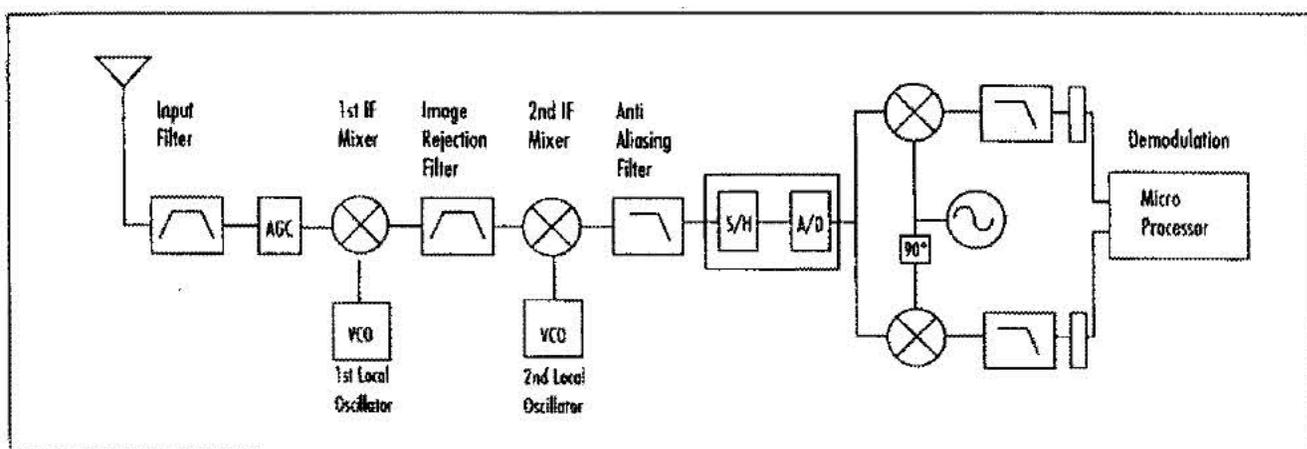


Figure 2: Top level block diagram of a wideband digital receiver with a digital second IF processing chain

channel. This class of system includes many commercial radios and cellular telephones. Further, the single channel receiver is the common denominator in other wideband receivers like channelizers and zoom spectrum analyzers that will be discussed later.

The single channel receiver is almost without exception a superheterodyne receiver with two IF stages as shown in Figure 1. The RF signal is received at the antenna and passes through a band pass filter, which attenuates interference from neighboring bands. The pass band of this filter must be wide enough to pass the entire frequency band that is to be examined at any one time, but the cutoff frequency must be balanced against the frequency of the first IF. In some cases the front end filter may have the capability to have tunable notch filters switched in. These eliminate known strong sources of interference within the band. This allows the user to utilize the full capabilities of the system in examining weak signals that are near the frequency of a strong signal.

The filtered signal is mixed with the first Local Oscillator (LO) in the first IF mixer. In most cases, the synthesizer generates a sine wave that serves as a coarse frequency tuner. The frequency of the LO is normally greater than that of the signal being received, so that the image frequencies fall

near the base band and above the LO frequency. The higher frequency component is filtered out by the image rejection filter. The inevitable imbalance in the mixer and mismatching between the mixer and the surrounding components cause the LO frequency to be mixed with itself so that there is also a spurious signal at twice the LO frequency that must be attenuated by the image rejection filter. The difference between the LO and the highest frequency of interest governs not only the width (and thus the complexity) of the image rejection filter, but also the width of the input filter. This is because input signals that are at the sum of the LO and the frequency of interest will also get mixed down to the base band.

In traditional analog systems, the signal would be mixed and filtered by a band pass filter to produce a base band output. The bandwidth of the band pass filter determines the narrow band width of the base band signal. At this point the sampling frequency of the output signal is assumed to be low enough to use a slow and inexpensive analog-to-digital converter (ADC), if a digital output is desired for subsequent processing. There are a number of limitations inherent in this approach. One of the problems is the physical limit on the spurious free dynamic range of the LO's. This problem is espe-

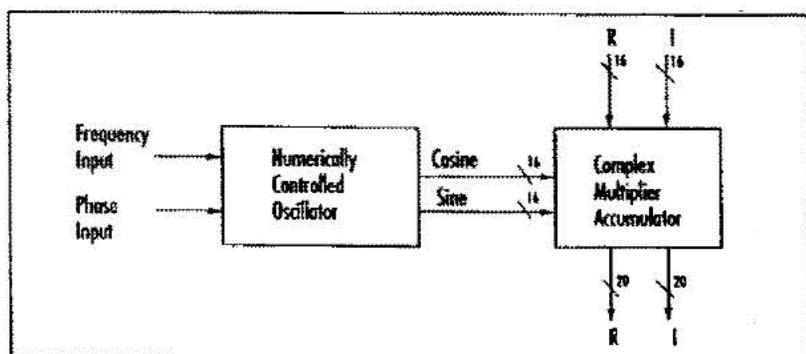


Figure 3: Top level block diagram of the Harris HSP45116 NCM. The Harris HSP45116 is composed of a Numerically Controlled Oscillator (NCO) followed by a Complex Multiplier/Accumulator (CMAC). The NCO is the digital equivalent of an analog VCO; the input is digital data that controls the frequency and the phase of the sinusoidal output. The output is a pair of digital data streams that represent the corresponding sine and cosine functions. The CMAC is the digital equivalent of a pair of analog mixers.

cially pronounced in the second LO. Other problems occur in the band pass filter after the second IF mixer. To change the output band width of the receiver the band pass filter must be replaced. One filter is required for each desired output band width. Also, since these are analog filters, they are severely limited in shape factor and maximum attenuation. This in turn limits the receiver's capability to block out adjacent channels. In high performance systems, these limits can be overcome by taking advantage of the capabilities of digital signal processing (DSP) as close to the antenna as possible. In most practical implementations, this means in the second IF processing chain.

With the advancement of ADC technology and the evolution of high performance DSP circuitry, the analog second IF processor functions can be replaced with the digital processing chain shown in Figure 3. Using this approach, the output of the ADC drives a digital mixer which modulates the data stream with  $e^{j\omega t}$  to shift the frequency band of interest to DC. This frequency translation decomposes the digital IF into a complex sample stream composed of in-phase and quadrature terms. The advantage of this technique is that the complex samples can preserve the magnitude and phase information of the equivalent real signal using one half the sample rate. Thus, the quadrature components can then be low pass filtered and decimated to the minimum sample rate required to represent the signal of interest.

As a result of the filtering operation, the wideband data stream is reduced from 10's of mega samples per second (MSPS) to as little as a few kilo samples per second (KSPS). The reduced data rate allows a variety of baseband processing functions to be performed by a standard DSP processor. In the past, implementation of a digital IF processor was limited by the amount of discrete hardware required to perform the filtering, signal synthesis, and baseband processing functions. Today, this task is simplified by a high dynamic range digital down converter available in a three chip set.

Digital IF processing begins immediately after the second IF section. The sample and hold (S/H) and analog to digital converter (ADC) sample the signal and convert it into a quantized signal. They are often considered one function, and indeed are integrated in a hybrid circuit or monolithic IC. This is one of the most difficult parts of the receiver circuit to specify, since the parameters of this function perturbate the design of the rest of the system.

#### Noise Sources

The noise specifications for S/H's and ADC's are usually categorized by two parameters: signal to noise ratio (SNR) and spurious free dynamic range (SFDR). Sources of noise in this circuit are random events in the transmission channel, imperfections in the analog electronics such as thermal noise, crosstalk and variations in the power supply, and inaccuracies in the S/H and ADC, such as aperture jitter, differential nonlinearity and quantization error. The SNR can be improved by the downstream narrow band filtering, assuming additive white Gaussian noise (AWGN). Wideband noise is spread evenly throughout the frequency band; since only a small part of the overall input spectrum will be passed through to the microprocessor, most of this noise is

filtered out and the user reaps the benefit of an improved signal to noise ratio.

Among the contributors to the spurious noise are slow rate limitations in the analog electronics, integral nonlinearity in the S/H and A/D. Also, in the case of digital down conversion, another contributing factor is quantization errors in the lookup tables for the sine and cosine. These can represent a more serious problem, since spurs that fall in the band of interest cannot be removed by narrowband filtering. In addition, the frequencies of the individual spurs vary when the parameters of the receiver are modified, such as when it is tuned to a new frequency. Various methods have been proposed to circumvent this problem, with the solution depending on the requirements of the system. For spectrum analyzers, the "brute force" approach is often necessary. In the approach, the performance of the system is specified by its worst case spur. Alternatively, noise may be added to the signal to randomize these spurs so that narrow band filtering will remove them.<sup>11</sup>

The high speed S/Hs and ADC's that are now commercially available have sample rates in the 1 to 10 MSPS range, with SNR's up to 90 dB and SFDR's above 70 dB. Faster sample rates are possible at reduced dynamic range. At 20 MSPS, SFDR's above 60 dB are possible, while converters in the 300 to 500 MSPS category have dynamic ranges on the order of 30 to 40 dB. The higher end of this level of performance is imple-

mented on hybrid and board level solutions, which carry prohibitive costs for many applications. Fortunately for the wideband system designer, only one ADC is required, per system. New monolithic solutions are approaching hybrid performance with 3 MSPS, 75 dB products currently available.

To be useful, this level of performance must be matched by high speed digital electronics, since currently available microprocessors fall short of processing these signals by one to two orders of magnitude. The gap between the digitized wideband signal and the computational power of a microprocessor is bridged by a digital down converter which extracts the narrow band signal of interest while reducing the data rate to the 10-100 KSPS range.

The sample rate of the ADC is usually 2.5 times the highest frequency component in the wideband IF signal. While the Nyquist criteria dictates a minimum sample rate of twice the highest frequency, practical implementations typically provide an oversampling margin to simplify the design of the anti-aliasing filter in front of the ADC.

The output of the ADC feeds the digital down converter which tunes and extracts the narrowband signal of interest from the wideband data stream. The down converter then is comprised of the HSP45116 Numerically Controlled Oscillator Modulator (NCOM)<sup>12</sup> and two HSP43220 Digital Decimating Filters (DDF's)<sup>13</sup> as shown in Figure 5. The NCOM takes the wideband input, digitized at rates up to 33MSPS, and translates the signal of interest to baseband by performing the digital equivalent of a VCO and quadrature mixer.

The quadrature components of the NCOM output are each filtered by the DDF's which implement a low pass filter while reducing the complex sample rate to match the frequency content of

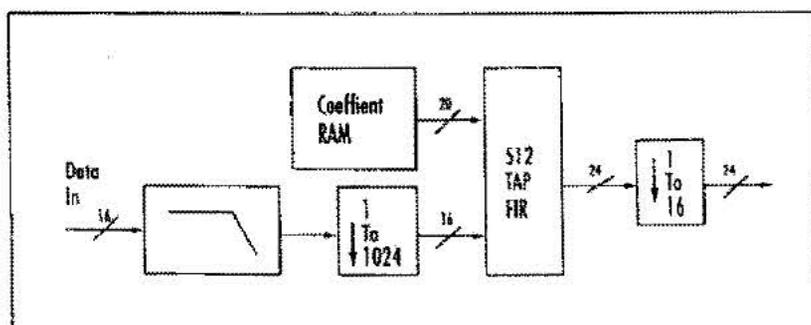


Figure 4: Top level block diagram of the Harris HSP43220 DDF

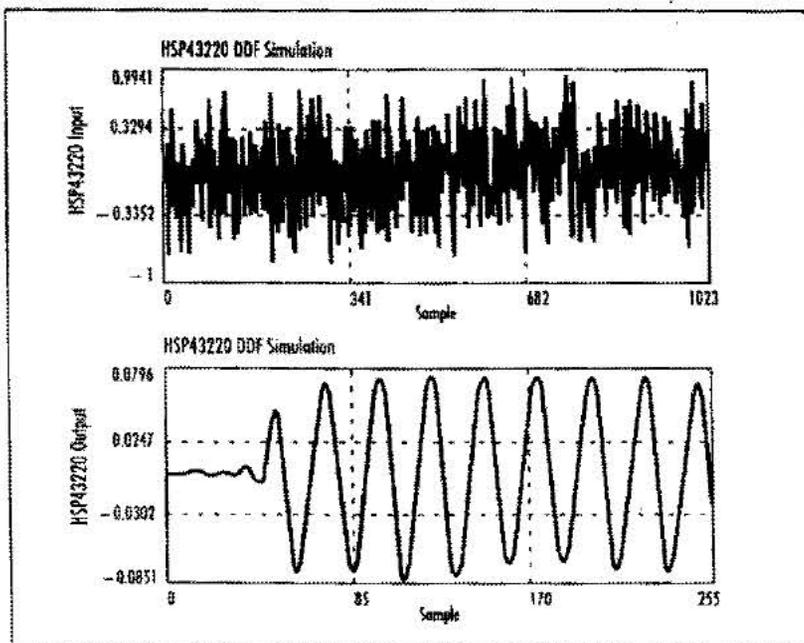


Figure 5: SNR improvement through bandwidth reduction

the extracted signal. For example, if the IF processor is extracting a 4 KHz wide voice grade channel out of a wideband input sampled at 33MSPS, the DDF could reduce the output sample rate to approximately 5 complex KSPS. With the sample rate thus reduced, baseband processing like demodulation and spectral analysis can be performed by standard DSP processors.

The NCOM multiplies a 16 bit complex input by samples of an internal LO which has the form  $e^{j\omega t}$ . The resulting output is a complex signal that has been spectrally shifted by the internal LO. The LO has spectral purity of more than 90dB and can be tuned from  $-fs/2$  to  $fs/2$  with an accuracy of more than .007Hz. A phase offset to .01 degrees may be added to the LO for applications requiring coherent down conversion. A standard micro-processor interface provides a control mechanism that allows modification of LO frequency or phase in less than .1ps. A top level block diagram on the NCOM is shown in Figure 7.

The NCOM functions as the digital equivalent of the second IF mixer. It has a number of advantages. These include the

digital benefits of operational stability over time and temperature, the ability to change tuning frequency or adjust oscillator phase in less than a microsecond, and the spectral purity of the LO. In addition, the fine tuning resolution of the NCOM can compensate for coarse tuning steps in the first IF section which simplifies the design of the receivers analog front end.

The DDF consists of a cascade of two lowpass filter stages. The first stage performs coarse low pass filtering while providing programmable decimation to 1024. The second stage consists of a 512 tap Finite Impulse Response (FIR) filter which narrows and shapes the passband while providing additional decimation of up to 16. Together, both stages yield a combined decimation of up to 16384 with stopband attenuation of up to 120dB. As with the NCOM, the DDF can be rapidly reconfigured via a standard microprocessor interface.

The flexibility and performance of the DDF make it a desirable replacement for the analog filter(s) following the second IF mixer. In systems where the second IF filter stage consists of a bank of filters to support various operational modes, cost and board space can be saved by reconfiguring a single DDF to implement the filter required by each operational mode. An added benefit is that the DDF typically achieves filter shape factors of 1.5:1 in contrast to the 3:1 and 4:1 shape factors typical of analog solutions. The shape factor improvement is often accompanied by stopband attenuation of more than 90dB versus the typical 50-70dB seen in analog approaches. The FIR filter section of the DDF can be used to equalize the magnitude response of the analog front end by using a multiband filter design package to generate a customized response for the FIR.

While precision filtering is required in any high performance digital receiver, the high

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order of decimation provided by the DDF simplifies practical implementations while improving channel selectivity. The ability of the DDF to reduce the sample rate from the 10's of MSPS required for wideband tuning to the KSPS required to represent the narrow band signal of interest allows baseband processing to be performed by a DSP microprocessor. As a result, the designer has the luxury of performing demodulation and signal analysis using software algorithms.

The reduction of the sample rate to meet the Nyquist criteria of the extracted channel also increases channel SNR prior to baseband processing. This is because the noise outside the band of interest, depending on filter characteristics, may be attenuated by 96 dB or more by the DDF's anti-alias filtering. If it is assumed that the noise power has a uniform spectral distribution, as would be the case for quantization or thermal noise, the improvement in SNR, processing gain, is expressed as

$$\text{SNR improvement (dB)} = 10 \cdot \log(BW_i/BW_o),$$

where  $BW_o$  is the output bandwidth and  $BW_i$  is the input bandwidth. For example, if a real 10 MHz signal digitized at a 25.6 MSPS is filtered to a bandwidth of 10 KHz and decimated by a factor of 2048 to yield an output data rate of 12.5 complex KSPS the corresponding improvement in SNR would exceed 33dB. The decomposition of the real input signal into a complex data stream allows for an automatic 3dB processing gain because the double sided real input signal can be represented by a single sided using half of the input bandwidth.

The processing gain achieved, as expressed in SNR improvement, allows the user to trade off ADC requirements against the filtering and decimation capabilities of the DDF. For example, the quantization noise introduced by an 8 bit ADC is much greater than that for a 16 bit ADC, however, an 8 bit ADC may be adequate

for the application if enough SNR improvement can be realized through sample rate reduction. If spurious free dynamic range is a key requirement, high resolution ADC's may be required since bandwidth reduction has no effect the in band spurs.

The tuning and filtering capabilities offered the by the digital tuner chip set improve of existing receiver structures while making new structures possible. Using a structure similar to the one shown in Figure 2, signals within a 13MHz IF may be downconverted to baseband and filtered by the DDF's to extract signals with bandwidths from 100's of Hz to a few 100KHz. The quadrature output of the digital tuner may feed a DSP capable of implementing various demodulation algorithms which include AM, FM, FSK, PSK, etc. In addition to providing a platform which is capable of implementing any number of software based demodulation types, the digital receiver structure also offers flexibilities like programmable filtering, tuning, gain control, and activity detection to.

The digital tuner chipset can simplify the implementation of channelized receivers while increasing channel selectivity. This structure ingests a large portion the of spectrum and tunes on several narrow frequency bands simultaneously. As shown in Figure 6, the channelized receiver is constructed with multiple sets of similar hardware that tune to the center frequencies of many channels of interest. The channels may have varying bandwidths and may be post processed by dedicated hardware or time multiplexed for post processing by the same hardware. Examples of this type of system are transmultiplexers and the cell sites for cellular telephones.

The digital tuner structure can also be used to simplify the implementation of a zoom spectrum analyzer as shown in Figure 7. In this application, a large FFT is used to determine the frequency content

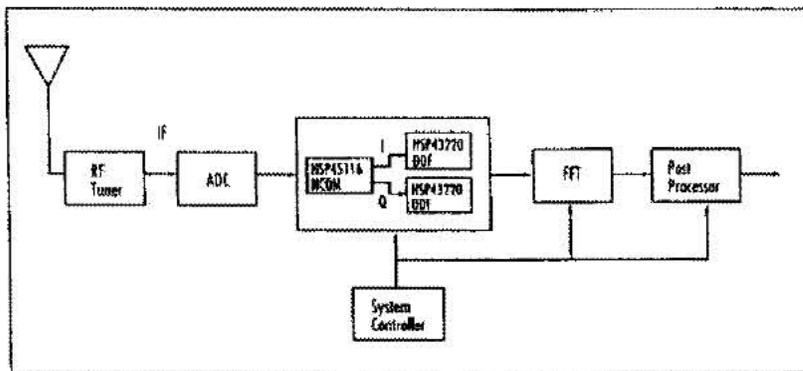
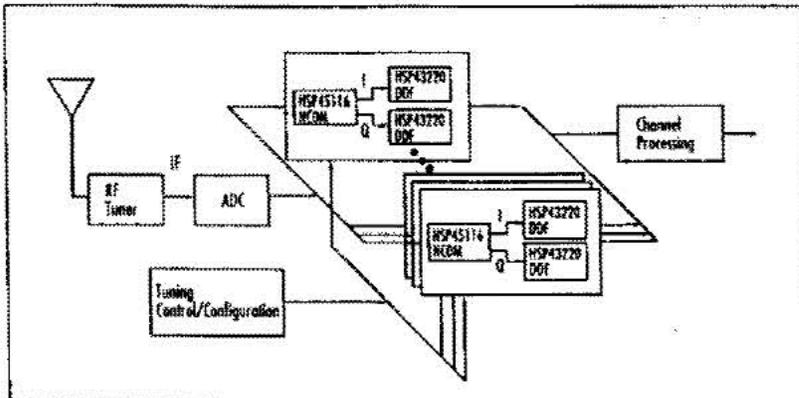


Figure 6 (upper): Wideband channelized receiver.

Figure 7 (lower): Zoom Spectrum Analyzer

of a signal in very fine frequency bands. The size of the FFT, and hence the processing complexity, is determined by the required frequency resolution of the FFT bins which is given by  $f_s/(\text{FFT Size})$ . Thus, by minimizing the sample rate, the size of the FFT can be reduced while preserving the same frequency resolution. The sample rate is minimized by using the INCOM and DDF to shift the band of interest to DC while reducing the sample rate to meet the Nyquist criteria of the signal band.

As an example, consider examining a 25KHz signal band centered at 4MHz, to a bin spacing of approximately 1 KHz. This would require the signal be digitized at approximately 10 MSPS. Assume that the FFT has 8192 points (assuming a radix 2 FFT) to yield an actual bin spacing of 1.22 KHz and a resolution of approximately 6 KHz as a result of window spread. Using the digital tuner chip set, the band of

interest can be shifted to DC while the data rate is decimated by a factor of 320 to yield an overall data rate of 31.25 complex KSPS. The resulting FFT size required to achieve the 1KHz bin spacing can now be reduced to 32 points, thus significantly reducing processor throughput demands.

With the advent of 10's of MSPS ADCs and VLSI implementations of a digital tuner, a first step in pushing DSP toward the antenna has been taken. Further advancements in the respective technology areas guarantee higher sampling rates coupled with higher levels of integration for digital tuning and demodulation. The declining cost of technology is making DSP a desirable alternative for an expanding spectrum of communication problems.

#### References

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- <sup>[2]</sup> Chester, D. B., Riley, C.A., Damerow, D.H., and Olmstead, C., "VLSI Implementation of a Wide Band, High Dynamic Range Digital Drop Receiver," *IEEE Proceedings of ICASSP 91, vol. D, pp. 1605-1608, Toronto, 1991.*
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#### About the Author:

Clay Olmstead is Staff Engineer, Applications; and Mike Olmstead is Lead Engineer, Applications; for Harris Semiconductor, Melbourne, FL. ■