Exhibit 1009

Silicon Labs v. Cresta Technology Sillab IPR Exhibit 1009

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON LABORATORIES, INC. Petitioner

v.

CRESTA TECHNOLOGY CORPORATION Patent Owner

> Case IPR Unassigned Patent 7,265,792 B2

Title: Television Receiver for Digital and Analog Television Signals

DECLARATION OF DOUGLAS HOLBERG IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,265,792

Mail Stop PATENT BOARD U.S. Patent Trial & Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450

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DECLARATION BY DOUGLAS HOLBERG

I, Douglas Holberg, hereby declare, affirm and state the following:

I. INTRODUCTION

1. The facts set forth below are known to me personally and I have firsthand knowledge of them. I am a U.S. citizen over eighteen years of age. I am fully competent to testify as to the matters addressed in this Declaration. I understand that this Declaration is being submitted along with a Petition for *inter partes* review of US Patent No. 7,265,792 ("the '792 patent").

2. I was asked to give my opinion on whether claims 18, 19, and 24–29 of the '792 patent ("the challenged claims") are unpatentable in view of certain prior art references. As described in detail in this Declaration, it is my opinion that each of those claims is rendered obvious by the prior art.

II. QUALIFICATIONS AND COMPENSATION

3. I have over 30 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Crystal Semiconductor, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when it acquired Cygnal, which I co-founded in 1999. I am a named inventor on 39 U.S. patents. I have held a variety of engineering positions over that time from circuit designer to Director of Engineering and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I earned my M.S.E. and Ph.D. degrees. A complete listing of my qualifications including a list of my patents is attached to this declaration as Appendix A.

4. My earliest experience with electronics began in High School where for three years, I took classes where I learned about radio and television architectures, built radios, repaired both radios and televisions. Concurrently, I was employed by a radio and television repair shop where I was paid to diagnose and repair radios and televisions. Naturally, this required intimate knowledge of the fundamental operation of radios and televisions of that era. I attended Texas A&M University where I studied electrical engineering with a focus on analog circuits for electives. One course (EE489) covered analog filters in detail from synthesis through implementation. Another course, Communications Circuits (EE428), covered radio receivers, oscillators, mixers, amplifiers, filters, transmitters, etc. A project of particular interest in EE428 was the design of a CB radio receiver using a standard broadcast-band AM receiver. This project involved designing a ~9 MHz, oscillator driving into a non-linear amplifier and filtering all but the third harmonic (~27 MHz) to mix with a signal derived from an antenna so that a ~27 MHz CB channel would mix to a frequency in the standard AM broadcast band. The AM receiver then performed the subsequent demodulation to audio so that CB radio communication was tuned and heard. I built this circuit in

the lab and demonstrated it to my professor—it worked—I received an A in my Communications Circuits class. Upon graduation, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated DTMF tone generator (both digital and analog components) for which I acquired my first patent. After leaving Mostek, I joined a startup company as employee #2 where I designed a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter. This circuit used discrete-time switchedcapacitor technology operating transistors in subthreshold region. My next project was to design a universal switched capacitor filter (CS7008) comprising four biquad filters, each individually programmable. Coefficients for the each biquad filter were stored in an external PROM and upon power up, the memory of the PROM was indexed to load the coefficients of each biquad from the PROM to volatile memory on board the filter chip. During this same period, I was coauthoring the book "CMOS Analog Circuit Design" which was published in first edition in 1987. I enrolled in a masters/Ph.D. program and for the next five years worked on the application of bipolar technology to DRAM sense amplifier architectures and circuit simulation algorithms. Upon graduating with a Ph.D. I went to work for Crystal Semiconductor/Cirrus Logic where I designed highfrequency synthesizers (60 MHz) for read-channel circuits reading magnetic media (hard disk drives). I managed a group making CCD interface circuits for digital

camera applications as well as television encoder chips. Upon leaving Cirrus, I started a company developing mixed-signal microcontrollers. Though I was a founder/CTO/VP Engineering, we had a small group, so I also acted as a circuit designer and layout designer as needed. I designed a novel A/D converter for which I received a patent, designed Δ Vbe temp sensors, I/O pads (both design and layout) as well as other miscellaneous circuits. My company was purchased by Silicon Labs where I remained employed as a manager of the microcontroller group at first, followed by a role as VP of Technology where I managed the CAD group and the developed design methodologies for the designers at Silicon Labs. I left Silicon Labs in 2008 and began a consulting career in the area of patents and intellectual property. Based on my experience, both professional and educational, I believe I am more than qualified to give the opinions expressed herein.

5. I am being compensated at my normal rate of \$275 per hour for my work in connection with this matter. My compensation is not dependent in any way on the contents of this Declaration, the substance of any further opinions or testimony that I may provide, or the ultimate outcome of this matter.

III. MATERIALS CONSIDERED

6. In forming the opinions expressed herein, I have reviewed and considered numerous documents, including the following materials:

Exhibit 1001U.S. Patent No. 7,265,792, titled "Television Receiver for
Digital and Analog Signals," to Favrat et al. ("the '792

patent").

Exhibit 1002	Return of Service in <i>Cresta Technology Corporation v.</i> <i>Silicon Laboratories, Inc. et al.</i> , Case No. 1:14-cv-00078 before the United States District Court for the District of Delaware (January 28, 2014) ("Return of Service").
Exhibit 1003	Complaint in ITC Investigation No. 377-TA-910 (January 28, 2014) ("ITC Complaint").
Exhibit 1004	European Patent Application No. EP 0696854, titled "Broadcast Receiver Adapted for Analog and Digital Signals," assigned to Thomson Multimedia S.A. (" <i>Thomson</i> ").
Exhibit 1005	Clay Olmstead & Mike Petrowski of Harris Semiconductor, <i>A Digital Tuner for Wideband Receivers</i> , DSP Applications Magazine, Sep. 1992 ("Harris").
Exhibit 1006	Al Lovrich & Ray Simar, Jr., "Implementation of FIR/IIR Filters with the TMS32010/TMS32020," Application Report: SPRA003A (Texas Instruments 1989) ("TI App Note").
Exhibit 1007	U.S. Patent Application No. 2004/0061804, titled "Broadband Receiver Having a Multistandard Channel Filter," to Favrat et al. ("the '585 application").
Exhibit 1008	U.S. Patent 5,381,357, titled "Complex Adaptive FIR Filter," to Wedgwood et al. ("Grumman").
Exhibit 1009	Declaration of Douglas Holberg ("Holberg Dec.").
Exhibit 1010	Excerpts of the prosecution file history of the '792 patent.
Exhibit 1011	U.S. Patent 6,377,316, titled "Tuner with Switched Analog and Digital Modulators," to Mycynek et al. ("Zenith").
Exhibit 1012	U.S. Patent 5,999,567, titled "Method for Recovering a Source Signal from a Composite Signal and Apparatus Therefor," to Torkkola. ("Torkkola").

- Exhibit 1013 U.S. Patent 6,263,222, titled "Signal Processing Apparatus," to Diab et al. ("Diab").
- Exhibit 1014
 Order No. 50 in ITC Investigation No. 337-TA-910, "Initial Determination Granting Cresta Technology Corporation's Corrected Motion to Partially Terminate Investigation as to U.S. Patent No. 7,251,466 and Certain Claims of U.S. Patent Nos. 7,075,585 and 7,265,792" (November 12, 2014).
- Exhibit 1015 U.S. Patent 6,725,463, titled "Dual Mode Tuner for Co-Existing Digital and Analog Television Signals," to Birleson. ("Birleson").
- Exhibit 1016 Advanced Television Systems Committee, "ATSC Digital Television Standard" (September 16, 1995).
- Exhibit 1017 U.S. Patent 5,796,442, titled "Multi-Format Television Receiver," to Gove et al. ("Gove").
- Exhibit 1018 U.S. Patent Application No. 2002/0057366, titled "Decoder Device and Receiver Using the Same," to Oku et al. ("Oku").
- Exhibit 1019 U.S. Patent No. 4,872,054, titled "Video Interface for Capturing an Incoming Video Signal and Reformatting the Video Signal," to Gray et al. ("Gray").
- Exhibit 1020 U.S. Patent No. 6,600,747, titled "Video Monitor Multiplexing Circuit," to Sauber ("Sauber").
- Exhibit 1021 U.S. Patent No. 6,804,497, titled "Partitioned Radio-Frequency Apparatus and Associated Methods," to Kerth et al. ("Kerth").
- Exhibit 1022 European Patent Application No. EP 94300649.4, titled "Digital Filtering, Data Rate Conversion and Modem Design," filed January 28, 1994, to Terrell ("Terrell").
- Exhibit 1023 U.S. Patent No. 6,124,898, titled "Digital Television Receiver with Equalization Performed on Digital Intermediate-

Frequency Signals," to Patel et al. ("Patel").

- Exhibit 1024 U.S. Patent No. 6,411,136, titled "Differential Line Driver," to Nianxiong et al. ("Ericsson").
- Exhibit 1025 U.S. Patent No. 7,394,857, titled "Flexible Versatile Low-Cost Wireline Transmit Driver," to Maulik et al. ("Maulik").
- Exhibit 1026 U.S. Patent No. 4,595,910, titled "Digital-to-Analog Converter Useful in a Television Receiver," to Wine ("Wine").
- Exhibit 1027 U.S. Patent No. 4,292,597, titled "Circuit for Converting Single-Ended Input Signals to a Pair of Differential Output Signals," to Niimura et al. ("Niimura").
- Exhibit 1028 The Authoritative Dictionary of IEEE Standards Terms, pp. 87, 912, IEEE Press (2000).
- Exhibit 1029 U.S. Patent No. 6,332,028, titled "Dual-Processing Interference Cancelling System and Method," to Marash ("Marash").
- Exhibit 1030 U.S. Patent No. 6,142,942, titled "Ultrasound Imaging System and Method Employing an Adaptive Filter," to Clark ("Clark").
- Exhibit 1031 U.S. Patent No. 6,400,598, titled "Programmable Circuit Devices with Low Voltage Differential Signaling Capabilities," to Nguyen et al. ("Nguyen").
- Exhibit 1032 Microsoft Computer Dictionary, pp. 269, 270, Microsoft Press (5th ed. 2002).
- Exhibit 1033James Karki, "Fully-Differential Amplifiers," Application
Report: SLOA054D (Texas Instruments 2002) ("Karki").
- Exhibit 1034 Stephen Kempainen, "Low-Voltage Differential Signaling (LVDS)," Application Note 1382-6 (Agilent Technologies May 20, 2002) ("Kempainen").

- Exhibit 1035 "High-Bandwidth LVDS Support in APEX Devices," M-SS-APEXLVDS-02 (Altera Corporation 2000) ("Altera").
- Exhibit 1036 "LVDS Owner's Manual: Low-Voltage Differential Signaling," 3d Ed., 550062-003 (National Semiconductor January 2004) ("National Semiconductor").
- Exhibit 1037 "Product Specification for TDA10021HT DVB-C channel receiver," (Philips Semiconductors, October 1, 2001) ("TDA10021HT").
- Exhibit 1038 "TDA10046HT Single-Chip DVB-T channel decoder," Docment order No. 9397 750 0922 (Philips Semiconductors, May 2002) ("TDA10046HT").
- Exhibit 1039 "Pre-Trial Brief of the Office of Unfair Import Investigations" in ITC Investigation No. 337-TA-910 (Redacted) (November 10, 2014).
- Exhibit 1040 Excerpts of "Hearing, Vol. 5" in ITC Investigation No. 337-TA-910 (December 5, 2014) (cross-examination of Dr. Caloyannides).

IV. THE '792 PATENT

A. Introduction

7. The '792 patent, titled "Television Receiver for Digital and Analog Television Signals," was filed July 1, 2004 and originally assigned to Xceive Corp. (Ex. 1001). After Xceive's business faltered, Cresta Technology Corp. ("Patent Owner") purchased certain of Xceive's assets including the '792 patent on October 10, 2011. (Ex. 1003, p.4). In January 2014, Patent Owner sued Petitioner and

several of its customers for infringing three of the patents it acquired from Xceive. (*Id.*).

8. The '792 patent builds on the earlier '585 patent (application publication Exhibit 1007). Both are directed towards a television signal receiver and, in particular, "a broadband television signal receiver for receiving multi-standard analog television and digital television signals." (*Compare* Ex. 1001, 1:6–10 *with* Ex. 1007 at [0002]). In fact, as described further below, the Examiner rejected many of the original '792 patent claims as "being anticipated" by the published '585 patent application. (Ex. 1010 at 75 (citing "Favrat et al.," US2004/0061804 A1, published April 1, 2004)).

9. As described in IPR2014-00728 and IPR2014-00809, Thomson Multimedia anticipated the move to DSP-based, multi-format television signal receivers long before Xceive filed the application that resulted in its '585 patent. (*See* Ex. 1004). By the time Xceive filed its '792 application, it conceded that the industry had already addressed this perceived need. (Ex. 1001, 2:4–5 ("Television receivers for receiving both analog and digital television signals are being developed.")). In particular, Xceive acknowledged that U.S. Pat. No. 6,369,857 to Balaban described "digitizing the intermediate frequency signal and processing the digitized signal using two separate processing circuitry—one for the analog television signal and one for digital television signal." (*Id.* at 2:15–20).

10. As a result, the '792 application pivoted to focus on the output circuitry. Specifically, the '792 application describes several iterations of a "signal output circuit," labeled "140" in Fig. 1 (below). (Ex. 1001, 6:49–51).



11. "[R]eceiver 100 can provide output signals in either analog or digital format on one or more output terminals." (Ex. 1001, 4:20–22). This output circuit at issue in the '792 patent merely converts the "processed IF signals" into "the desired output signals." (*Id.* at 6:49–51). Figure 2 illustrates several other "desired output signals" including analog v. digital, single-ended v. differential, or serial v. parallel. (*Id.* at Fig. 2, 7:34–35 ("Turning now to FIG. 2 where alternate embodiments of the signal output circuit are shown.")).

12. Challenged claim 18, for example, recites several of these "desired output signals." (*See* Ex. 1001, claim 18). This claim is drawn toward outputting either a digital or analog television signal on two output terminals. To do so, claim 18 recites coupling two output terminals to either a differential digital television signal or a single-ended analog television signal. (*Id.* at claim 18). Because a

television will either be analog or digital at a given time, claim 18 reduces the number of pins for an output circuit that drives either an analog or digital television monitor.

13. Outputting either a differential signal or single-ended signal on the same set of pins to drive either an analog or digital monitor has been known well before July 1, 2004, the date the '792 patent was filed. (*See e.g.*, Sauber Ex, 2010 at 1:35–37; 4:24–36) At least by 1998, connecting a computer system to both digital and analog monitors was "disadvantageous because the system 100 will have two sets of signal lines from the video controller and two connectors." (Sauber, Ex. 1020 at 3:39-42). Sauber recognized that either a differential digital signal or an analog signal could be coupled to either an analog or digital monitor or a digital monitor." (*Id.* at 1:8-12, 1:60-67). Thus, the use of the same pair of pins for coupling a differential signal to a digital monitor and a single-ended signal to a nanalog monitor was not novel when the '792 patent was filed.

14. A person of ordinary skill in the art would know that "signals may constitute single-ended or differential signals, as desired." (Kerth, Ex. 1021 at 8:57-58). Differential signals can be continuous (analog) or discrete (digital). Regardless of whether analog or digital, Differential signaling provides many advantages, including rejection of common mode ground noise, doubling in the output voltage swing, a reduction in harmonic distortion, and substrate and coupled noise rejection. (Karki, Ex. 1033). Many of these advantages are applicable to digital signal processing, including processing of digital and analog television signals. Kerth discloses using differential signaling to transmit differential I and Q signals to a baseband processor to "further reduce interference effects among circuit partitions." (Kerth Fig. 4, 10:53-58). Sauber discloses a differential circuit for inputting differential digital signals to a digital monitor. (Sauber at 4:24–31).

15. Differential signaling such as low voltage differential signaling (LVDS) was well-suited for digital television applications. (Kempainen, Ex. 1034, p. 1 ("In addition, data streams for digital video, HDTV, and color graphics are requiring higher and higher bandwidth. The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is analog Low-Voltage Differential Signaling (LVDS) that designers are choosing to drive these high-speed transmission lines."); *see also* Altera, Ex. 1035, (LVDS Applications include "Audio and video digital signal processing" and "MPEG stream processing"); National Semiconductor, Ex. 1036, at 1-1 and 1-5 (Table 1.2) (LVDS applications include set top boxes and satellite systems)). One of the driving factors for the use of LVDS in digital television systems, including HDTV, was its high data rate

requirements. "Whenever you need high-speed data transfer (100Mb/s and higher), LVDS offers a solution." (Ex. 1034).

16. The specific type of driver circuits, the interconnection of driver circuits, and the use of single- or differential signaling are mere design choices driven by input and output requirements of the circuit, including high speed data transfer rates (Ex. 1034 at 1), reduced common mode rejection noise (Ex. 1036 at 2-1), and lower electromagnetic interference (Ex. 1036 at 4-5). Input and output requirements are in turn driven by commercial and marketing factors, such as the type of television set (analog or digital) that will display the received RF signal. (Ex. 1037 (Philips TDA10021HT) and Ex. 1038 (Philips TDA10046HT)).

17. Furthermore, converting an output signal from one desired output form to another is not patentable. A person of ordinary skill in the art ("POSITA") would know that a digital-to-analog converter ("DAC") would be necessary if the desired output format was analog instead of digital. (*See* Ex. 1026, "Digital-to-Analog Converter useful in a television receiver"). Likewise, a POSITA would know that a single- to differential-ended converter was necessary to convert a signal ended output to a differential output, if a differential output was desired. (*See* Ex. 1027, Abstract ("A circuit that is particularly adapted to convert a single-ended input signal to a pair of differential output signals," which finds ready application in "a color saturation control circuit in a color television receiver.)";

see also Ex. 1001, 4:3–7 ("When signal input terminal 102 is a differential terminal, receiver 100 further includes a balun transformer to convert the differential input signals into a single-ended signal, as is well understood by one of ordinary skill in the art.")).

18. In this case, the choice of the desired output signal format and the use of a common pair of pins for either analog or digital television is driven by the desire for a "cheaper," "faster," "smaller," "or more efficient" television receiver, namely, commercial and marketing issues, as the '792 patent concedes. (*Id.* at 2:22–24 ("It is further desired that such a dual-format television receiver be cost effective to manufacture and provides high quality video and audio performance."); 6:51–56 ("A configuration for signal output circuit 140 can be selected based on factors such as the desired pin count for receiver 100 and the desired format for the output signals.")). It is my opinion, that all of the claimed options are well within the grasp of a POSITA, as evidenced by the legions of prior art references using these options.

B. Prosecution History of the '792 Patent

19. As part of my analysis, I reviewed the prosecution history of the '792 patent before the United States Patent and Trademark Office. In the first office action, claims 1–4, 11, 12, and 30–34 were rejected under 35 U.S.C. § 102(b) as anticipated by the published '585 patent application (Ex. 1007). Claims 5, 10, 13,

and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '585 application in view of Oku (Ex. 1018). Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '585 application in view of Oku, in further view of Gray (Ex. 1019). Claims 6–9, 15, and 18–29 were indicated to contain allegedly allowable subject matter. (Ex. 1010, pp. 75–77).

20. In response to the first office action, the applicant amended claim 1 to recite the limitations formerly of claim 24. (Ex. 1010, p. 84). The applicant also amended all of the other claims to depend from claim 1. Because the subject matter of claim 24 had been indicated as allowable, the applicant argued that independent claim 1 and all depending claims were therefore allowable. The applicant cancelled claim 24 as well as claims 31–34 and requested allowance of all remaining claims.

21. The Examiner then allowed all remaining claims in the application (Ex. 1010 at 99), despite the fact that the limitation added to claim 1 by amendment was clearly taught in the '585 application. For example, claim 11 of the '585 application is virtually identical to the allegedly allowable subject matter. (*See* Ex. 1007 at claim 11 "wherein said signal processor applies one of a plurality of finite impulse response filters"). Clearly the Examiner should have maintained his rejection even in light of the amendment.

C. Person of Ordinary Skill in the Art

22. I have considered certain issues from the perspective of a person of ordinary skill in the art. It is my opinion, based upon a review of the file history of the '792 patent, that a person of ordinary skill in the art to the '792 patent, as of July 1, 2004, the time of the alleged invention of the '792 patent ("POSITA") would have held at least a Masters of Science or higher degree in electrical engineering, have at least four years of experience with mixed signal system design, including analog front ends and subsequent digital signal processing of various analog and digital signal formats of video and audio content.

D. Claim Construction

23. I am informed that the claims in an *inter partes* review should be given their "broadest reasonable construction in light of the specification" as commonly understood by a person of ordinary skill in the art.

Board's Previous Constructions

24. In the previously filed proceeding, IPR2014-00809, I understand that the Board construed the following terms as follows:

- RF Signals—"Signals having a frequency between 10 kHz and 100 GHz";
- Format—"analog and digital signals are examples of distinct formats";

- Baseband signal—"a signal without transmission modulation"; and
- Signal Processor—"a digital module that processes signals in the digital domain."

IPR2014-00809, Paper 10 at 7–9. I agree that each of the constructions adopted by the Board is appropriate to the present proceeding.

Additional Term

25. "**Indexes**"—Another term I believe requires further explanation for purposes of this Petition is the "indexes" term as used in claim 24. Specifically, "wherein the plurality of finite impulse response filters are stored in memory, and the signal processor indexes the memory to retrieve one of the plurality of finite impulse response filters." (Ex. 1001, claim 24).

26. As disclosed in the '792 patent, the format/standard selection circuit, depending on its state, selects "between the several analog and digital television formats and standards." (Ex. 1001, 6:21–23). Based on the standard selection tcircuit, The DSP applies a filter function. The "coefficients of the filter functions are stored in a look-up table in a memory 132 in DSP circuit 130. DSP 131 retrieves the coefficients from memory 132 to be applied to the incoming digital signals." (*Id.* at 5:60–63). The signal processor indexes or points to a block of memory when retrieving a set of coefficients. This usage of the term indexing is consistent with the plain and ordinary meaning of that term. (*See* Microsoft

Computer Dictionary, Ex. 1032, pp. 269, 270 (defining the verb "index" as "1. In data storage and retrieval, to create and use a list or table that contains reference information, pointing to stored data. . . . 3. In indexed file storage, to find files stored on disk by using an index of file locations (addresses). 4. In programming and information processing, to locate information stored in a table by adding an offset amount, called the index, to the base address of the table.")). Accordingly, it is my opinion that the broadest reasonable construction of the term "indexes" is its plain and ordinary meaning.

Patent Owner's Proposed Constructions

27. In its Patent Owner response in IPR2014-00809, Patent Owner offers constructions for several terms. As discussed below in detail, I do not agree with the Patent Owner's proposed constructions because they do not reflect the plain and ordinary meaning of those terms to a POSITA.

28. "**Input RF signal**"—Patent Owner proposes to construe this term as "a signal that is an incoming signal that comes out of the medium of propagation and is external to the frequency conversion circuit without any processing by the frequency conversion circuit." (IPR2014-00809, Paper No. 35 at 9–12). I do not agree that Patent owner's proposed construction reflects the broadest reasonable construction of that term in light of the specification. Rather, Patent Owner is attempting to read its strained construction of "RF signals" as a limitation into the claim. I disagree with this proposed construction for the reasons discussed below.

29. First, the specification uses the term "input signal" in a number of places. (See, e.g., Ex. 1001, 4:3-7, 6:22-31, 14:44). In each case, the term is used in its plain and ordinary manner, *i.e.*, as a signal that is input to a circuit. (See id.). The specification refers in several places to an "input RF signals." (See, e.g., Ex. 1001 at Abstract, 1:43, 2:32–40, 4:53–56, 5:52). In each instance, this term is used simply to indicate that the signal that is input to the circuit is an RF signal. I agree that RF stands for "radio frequency," as noted in the specification itself. (Ex. 1001, 1:36)). A POSITA understood that radio frequency or RF refers to "signals having a frequency between 10 kHz and 100 GHz." (Ex. 1028, p. 912 (2000)). The specification does not equate "input RF signals" to the source of those signals or the medium over which the signal is propagated. (Id.) In fact, the specification uses permissive language when it describes the source of those signals. (Ex. 1001) at 3:57–59 ("a dual-format television receiver 100 includes a signal input terminal 102 for receiving incoming RF signal"). In my opinion, the patent specification does not require signal input terminal 102 only receive input RF signals directly

"out of a medium of propagation external and is external to the tuner without any processing by the tuner," as required by Patent Owner's construction.¹

30. I also disagree with Patent Owner's proposed construction because it has no support in the art. All television signals undergo multiple frequency conversions over multiple mediums between the data source and the claimed frequency conversion circuit, such that identifying any point before the input of the claimed frequency conversion circuit as the "medium of propagation" under Patent Owner's proposed construction is vague, arbitrary, and ambiguous.

31. A person of ordinary skill in the art would have understood that the signal path from a television source (*e.g.*, camera filming a live event) and a television receiver would have multiple frequency conversions over many different mediums. For example, the camera might convert the signal to one frequency to be transmitted to a local uplink center, which would convert it to a second frequency for uplink to a satellite, which would convert it to a third frequency as a downlink to a super head end, which would convert it to a fourth frequency for

¹ It is my opinion that Patent Owner's proposed construction in this case is also inconsistent with the construction that it proposed in the ITC. (Ex. 1039, p. 15 ("input RF television signal(s)")). While improperly limited to "television," Patent Owner concedes that the term should otherwise be given its plain and ordinary meaning.

fiber optic transmission to a local node (which may be the outside of a home for a system like Verizon FiOS), which converts it to a fifth frequency for transmission over coaxial cable into the home. Thus, one of ordinary skill in the art would understand, and in fact assume, that the claimed input RF signal would necessarily have been processed and converted many times over many different mediums before it is input to the claimed frequency conversion circuit.

32. I understand that the claims use the term "input RF signals" in its plain and ordinary way. Claim 1 requires "receiving an input RF signal." (Ex. 1001, claim 1). For example, claim 1 makes no mention of the source of those input signals. The first element of the claim is the "frequency conversion circuit" that receives these signals. Claim 29 notes that "the input RF signal comprises an RF signal received from terrestrial broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission." This makes clear that the source or the medium of the input RF signal is not a limitation on the claim. Counsel has informed me that the presence of limitation in dependent claim "strongly implies" that such a limitation is not "inherently" part of the term in the original claim.

33. "a frequency conversion circuit for receiving input RF signals and for converting said input RF signals to an intermediate frequency signal"— Patent Owner proposes that this term means "frequency conversion circuit that receives an incoming signal that comes out of the medium of propagation and is external to the tuner without any processing." (IPR2014-00809, Paper No. 35 at 12–13). I disagree. Patent Owner's argument is based on its erroneous construction of the phrase "input RF signal." As discussed above with respect to "input RF signals," it is my opinion that Patent Owner's construction does not reflect the broadest reasonable construction of this term in light of the specification. Instead, the term should be given its plain and ordinary meaning in light of the specification.

34. "the input RF signal encoding information in one of a plurality of television signal formats"—Patent Owner proposes that this term "requires receiving one television format RF signal at a time." (IPR2014-00809, Paper No. 35 at 13). I disagree. This proposed construction—which is unsupported in Patent Owner's response—is erroneous. It is my opinion that a POSITA would interpret "a" or "an" in patent claim containing the transitional phrase "comprising" or "including" as "one or more." The '792 patent provides no basis for construing the indefinite article "a" to mean "only one," rather than its plain and ordinary meaning of "one or more." Such a construction does not reflect the broadest reasonable construction of this term and should be rejected.

35. "a signal processor for processing . . . in accordance with the television signal format . . . the signal processor applies one of a plurality of

finite impulse response filters . . . each of the plurality of finite impulse filters corresponding to a format"—Patent Owner proposes to construe these terms such that "the signal processor processes only one format and does not process a plurality of formats in parallel." (IPR2014-00809, Paper No. 35 at 14). I disagree. This proposed construction—which is unsupported in Patent Owner's response—is also erroneous. The '792 patent provides no basis for construing the indefinite article "a" to mean "only one," rather than its plain and ordinary meaning of "one or more." It is my opinion that a POSITA would interpret "a" or "an" in patent claim containing the transitional phrase "comprising" or "including" as "one or more." As a result, the Patent Owner's proposed construction does not reflect the broadest reasonable construction of this term and should be rejected.

V. OPINIONS RELATING TO EACH OF THE GROUNDS

36. Independent claim 1 recites a television receiver. All of the challenged claims 18, 19, 24–29 depend from independent claim 1. I provide a detailed explanation below for each ground for each of the challenged claims.

A. Foundational Claim

Claim 1 is rendered obvious by Thomson in view of Harris

- Preamble—"A television receiver comprising"
- 37. In my opinion, the preamble of claim 1 is not a claim limitation.

38. However, even assuming the preamble of claim 1 is a claim limitation, Thomson clearly, in my opinion, describes the claimed "television

receiver." (Ex. 1004 at 1:3–4 ("invention relates to a broadcast receiver")). Thomson describes a "multi-standard tuner" capable of receiving television signals transmitted in the form of a satellite broadcast, terrestrial, and cable transmissions in the range of "950-1750 MHz." (*See id.* at 1:55–2:19). It is my opinion that Thomson teaches this element.

• "a frequency conversion circuit"

39. Thomson likewise describes a circuit that receives an incoming satellite signal "of about 2 GHZ" and, via a multi-stage frequency down conversion process, converts that signal to a signal having a lower frequency. (Ex. 1004 at 1 "Gist of the Invention"; 2:30–33). For at least these reasons, it is my opinion that Thomson teaches this element.

 "for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF)"

40. The Thomson "multi-standard tuner" receives the RF signal from an "outdoor" satellite unit, which "supplies the satellite channels already downconverted in a frequency band covering 950-1750 MHz." (Ex. 1004 at 1:55–60). Because I understand that the Board construed "RF signals" as "signals having a frequency between 10 kHz and 100 GHz," Thomson teaches this element under the Board's construction of "RF signals." IPR2014-00809, Paper 10 at 7–9. As explained in Thomson, this RF signal is converted to a "140 MHz Sat-IF signal" that forms the "IF_{SAT}" input to the circuit shown in circuit above in Fig. 1. (Ex. 1004 at 2:17–19, Fig. 1). This signal then gets further "down-converted" by "mixer stage 2" into "an IF signal of around 75 MHz (see Figs. 2d and 2e)." (*Id.* at 2:53–57). Therefore, it is my opinion that Thomson teaches this element under the Board's construction.

41. Further, it is my opinion that Thomson discloses this limitation even under Patent Owner's improperly narrow construction, in that Thomson discloses a signal (input to mixer 2) that is an incoming signal (with respect to mixer 2) that comes out of the medium of propagation (the signal line between SAW filter 1 and mixer 2) and is external to the frequency conversion circuit (mixer 2) without any processing by the frequency conversion circuit (mixer 2).

> "the input RF signal encoding information in one of a plurality of television signal formats"

42. Thomson teaches that the "multi-standard tuner" can receive RF signals in a plurality of formats, including "analog or digital ones." (*See, e.g.,* Ex. 1004 at 1:42–43). The '792 patent likewise identifies "analog or digital" as two different television signal "format[s]." (*Id.* at 1:30). For at least these reasons, it is my opinion that Thomson teaches this element.

 "an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof"

25

43. The filtered output of the AGC amplifier 5 in Thomson is coupled to an analog-to-digital converter ("A/D") 7. (Ex. 1004 at Fig. 1). The "A/Dconverter [is] necessary for the digiti[z]ing" of the bandpass-filtered intermediate frequency signal output of AGC 5. (Ex. 1004 at 1:47; *see also* Fig. 1). As the name implies, A/D 7 converts the filtered IF signal to, in the words of claim 1, "a digital representation thereof." Fig. 1 shows that "A/D 7" has a sampling frequency of "f_s." Thomson further teaches that in one embodiment the "A/D converter (7) operates with a sampling frequency of about 100MHz." (*Id.* at 4:14– 16). For at least these reasons, it is my opinion that Thomson teaches this element.

• "a signal processor for"

44. It is my opinion that Thomson teaches this element under the Board's construction of "signal processor". Thomson discloses an adaptive bandpass filter that is a digital module that processes signals in the digital domain. Thomson describes a "bandpass filter 8" that has "an adaptively controlled bandwidth" that passes the analog TV encoded information in the case of analog formatted signal or the digital TV encoded information in the case of digital formatted signal. (Ex. 1004 at 3:16–25). The adaptive filter 8 makes this selection based on the "TV standard" input to the filter. (*Id.* at Fig. 1). By disclosing an adaptive bandpass filter that processes an input or output signal (*e.g.*, it filters an analog or digital TV signal), it is my opinion that Thomson teaches a signal processor.

45. In my opinion, the adaptive filter of Thomson satisfies the Board's construction of "signal processor." The Board construed "signal processor to mean "a digital module that processes signals in the digital domain." IPR2014-00809, Paper 10 at 7–9. The Thomson bandpass filter is a digital module because it is a circuit that receives digital input signals that are output from the A/D 7. It processes those digital input signals in the digital domain (as opposed to the analog domain) to produce a bandlimited output signal. (*Id.*). Accordingly, Thomson satisfies the Board's definition for a "signal processor." (*Id.*).

• "processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate frequency signal, each of the plurality of finite impulse response filters corresponding to a format of the input RF signal"

46. Thomson discloses a signal processor that implements an adaptive filter having varying bandpass frequencies. Harris discloses a signal processor that implements a finite impulse response (FIR) filter. It is my opinion that it would have been obvious to a POSITA to incorporate the FIR filter of Harris into the adaptive filter of Thomson.

47. It is my opinion that the adaptive filter in Thomson processes intermediate frequencies according to the format of an input RF signal. An adaptive filter is a filter which can change its characteristics by changing its filter coefficients. (*See* Ex. 1029 and Ex. 1030 at 2:19–23 ("Generally, an adaptive filter is a filter having a transfer function that can be adjusted, or changed, based on the sampled signal statistics, or signal features, associated with an input or output signal.")). The transfer function of the Thomson adaptive filter is illustrated in the frequency map of Fig. 2(g) (reproduced below):



(Ex. 1004 at Fig. 2). The upper and lower bounds of the Thomson filter vary or "adapt" according to the format of the input RF signal, as indicated by the "TV Standard" input to the filter. (*See also* Ex. 1004 at 3:16–19 ("bandpass filter 8 (see Fig. 2g) with an adaptively controlled bandwidth selects the desired signal"), Fig. 1).

48. The status of the "TV standard" input determines the function of the bandpass filter: the filter executes one filter function if the RF input signal is an analog TV format, or another filter function if it is in a digital TV format. (*See also* Ex. 1004 at Fig. 1 ("TV Standard" input to "filter 8"); *see also* (Ex. 1004 at 3:16–18 ("bandpass filter 8 (Fig. 2g) with an adaptively controlled bandwidth

selects the desired signal with a minimal remainder of adjacent channel signals.")). Accordingly, it is my opinion that the Thomson filter 8 is adapted to the particular TV format (e.g., analog or digital), receives the "digital representations of said intermediate signals" output by the A/D 7, processes those digital representations according to its transfer function "in accordance with said format of said input RF signal," as indicated by the TV standard input, and "generat[es] digital output signals indicative of information encoded in said input RF signal." While Thomson does not explicitly disclose the use of FIR filters, Harris does.

49. Harris describes a processor-based FIR filter that can function as an adaptive filter. For example, Harris discloses the following digital decimation filter ("DDF") including a finite impulse response filter:



(Ex. 1005 at 4). The Harris digital decimation filter ("DDF") includes a "512 TAP FIR" filter coupled to a "coefficient RAM" that stores the FIR filter coefficients. (*Id.*). The DDF "can be rapidly reconfigured via a standard microprocessor

interface." (*Id.* at 5). In other words, this filter, combined with a microprocessor, can retrieve the FIR filter coefficients from memory and store those in the "coefficient RAM." just like the '792 Patent (Ex. 1001 at 5:59–63 ("In one embodiment, the coefficients of the filter functions are stored in a look-up table in memory 132 in DSP circuit 130. DSP 131 retrieves the coefficients from memory 132 to be applied to the incoming digital signals.")). Harris further teaches that if this filter is used in "systems where the second IF filter state consists of a bank of filters to support various operational modes, cost and board space can be saved be [sic:by] *reconfiguring a single DDF to implement the filter required by each operational mode.*" (Ex. 1005 at 5 (emphasis added)).

50. It would have been obvious for one of ordinary skill in the art to incorporate the FIR filters of Harris into the Thomson adaptive filter and render this claim limitation obvious. Although both FIR and infinite impulse response (IIR) filters were well known in the art, (*See, e.g.*, Ex. 1006), in my opinion a POSITA would have been motivated to choose a FIR filter over an IIR filter for several reasons. This is so because a FIR filter produces "a linear phase, and only FIR filters can be designed to have linear phase," which is a critical parameter in audio and video applications such as Thomson. (TI App Note, Ex. 1006 at 21). Moreover, the '792 patent refers to a prior art ATSC A-53 specification teaching a linear FIR filter, namely a "filter response . . . as a raised root cosine with 0.1152

roll-off." (Ex. 1001, 6:39-41; see also Ex. 1016, Fig. 12, p. 58 ("linear phase raised cosine Nyquist filter" which would necessitate a FIR filter implementation)). FIR filters also are less sensitive to coefficient quantization and are thus generally more stable than IIR filters. It is my opinion that the FIR implementation of Harris would be an obvious design choice in the Thomson application because both Harris and Thomson solve similar problems, namely tuning an adaptive filter to the input format or operational mode of the system. Harris also explicitly teaches that the "declining cost of technology is making DSP a desirable alternative for an expanding spectrum of communication problems." (Ex. 1005 at 7). It is my opinion that a POSITA would have interpreted that suggestion to include digital television such as in Thomson. For these reasons, a POSITA would have been motivated to use the FIR filters of Harris to implement the plurality of filter functions for the adaptive filter of Thomson, thereby rending this limitation obvious.

51. I agree with Patent Owner's expert in the ITC litigation, Dr. Caloyannides, who testified that a POSITA would by default use a FIR filter design:

Q: You would agree that a person of ordinary skill would, by default, use a FIR filter to implement filter 8 in Boie because a FIR filter is a simpler conceptually, mathematically and analytically; correct?

A: That is correct that it would be the simpler filter to implement for the reasons you stated.

Q: And because of those reasons, a person of ordinary skill would by default use a FIR filter; correct?

A: Well, a person of ordinary skill in the art at the time of the patent would be inclined to use a FIR filter.

(Ex. 1040 at 1232:14–24).

52. Because such a well-known combination would have had a reasonable expectation of success (*See* Ex. 1023, 6:1–5, 15:51–54 (implementing adaptive FIR filters using a "filter coefficient computation apparatus")), in my opinion a POSITA would be motivated to make such a combination, and thus Thomson and Harris disclose this limitation.

 "a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals."

53. Thomson discloses an output circuit including a plurality of demodulators, each coupled to receive output signals from said signal processor. (Ex. 1004 at Fig. 1 showing FM-demodulator 9 and QPSK-demodulator (12, 13) connected in parallel to receive the output signals from the adaptive bandpass filter 8 (i.e. "said signal processor")). Thomson discloses that the "FM-demodulator (9)" demodulates the digital signals encoding information in the analog TV format
and the "QPSK-demodulator (12, 13)" demodulates the digital signals encoding information in the digital TV format. (Ex. 1004 at 4:10–11). Therefore, in my opinion, Thomson discloses demodulators receiving output signals from the processor and outputting signals corresponding to received digital television signals.

54. Thomson discloses a TV receiver that receives TV signals having both audio and video components. "The FM demodulator 9 converts the IF signal into the CVBS signal and the subcarrier modulated sound signals." (Thomson, Ex. 1004 at 3:19–21). Thomson further discloses "synchronous demodulators 12, 13 for QPSK quadrature demodulation and low pass filters 14, 15 providing signal Q, I at outputs of circuit 4." (Id. at 2:41–44). In my opinion, one of ordinary skill in the art would understand that the video and audio information of digital TV signals (e.g., as MPEG) may be digitally encoded in a single signal, and also that the Q and I baseband signal components must carry both the video and audio information for the TV signals of Thomson to serve the expressly disclosed purpose of a digital TV receiver. For at least these reasons, Thomson teaches this element. Accordingly, in my opinion, the combination of Thomson and Harris render claim 1 invalid.

B. Ground 1: Claim 29 is obvious over Thomson in view of Harris.

• "29. The television receiver of claim 1, wherein the input RF signal comprises an RF signal received from terrestrial

broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission."

55. Thomson discloses that the multistandard receiver can receive satellite broadcast, terrestrial, and cable transmissions. (Ex. 1004 at 1:55–2:3). Because Thomson discloses that the input RF signal can be received from a satellite broadcast, a terrestrial broadcast, and a cable broadcast, it is my opinion that this claim is rendered obvious by Thomson in view of Harris.

C. Ground 2: Claim 24 is obvious over Thomson and Harris in view of Grumman.

 "24. The television receiver of claim 1, wherein the plurality of finite impulse response filters are stored in a memory and"

56. Claim 24 adds a well-known approach of implementing digital FIR

filters, namely indexing a set of FIR filter coefficients stored in memory. Grumman describes the structure of "a complex Finite-Impulse-Response filter with adaptive weights for processing complex digital data having real and imaginary input data portions." (Grumman, Ex. 1008, 3:31–34). The adaptive weights (coefficient data values) of the FIR filters "are stored in two memory storage banks for access by the filter or host processor," (*Id.* at 4:7–9), or are "stored in alternative memory storage banks." (*Id.* at 4:9–14). Thus, Grumman discloses the storage of two sets of coefficients, each set corresponding to a separate FIR filter. This two bank architecture allows the filter to operate with data present in one memory bank while the other memory bank "is being updated with

the new set of coefficients." (Ex. 1008 at 11:25–29). Figs. 1a and 1b of Grumman are depicted below. The coefficients for the two FIR filters are stored in BANK 0 and BANK 1. The output of swap circuitry 38 controls access to BANK 0 or BANK 1. By outputting a "0," swap circuitry selects BANK 0, else, by outputting a "1," swap circuitry selects BANK 1. (Ex. 1008 at Fig. 7c).



(Ex. 1008 at Figs 1a and 1b). Because Grumman discloses storing coefficients for two FIR filters in memory, one set of coefficients for one FIR filter stored in BANK 0 and another set of coefficients for another FIR filter stored in BANK 1, it is my opinion that this limitation is met by Grumman. (*See also id.* at "BANK 0" and "BANK 1" in Fig. 1B).

 "the signal processor indexes the memory to retrieve one of the plurality of finite impulse response filters."

57. It is my opinion that Grumman discloses a signal processor that indexes memory to retrieve FIR filter coefficients via "weight swapping," which results in changing access of the adaptive weight data from one memory bank 24 to the other memory bank. (Ex. 1008, 9:10–15). Weight swapping circuitry performs the weight swapping function by providing "timing and control signals necessary to accomplish the weight swapping function in the real and imaginary coefficient/coefficient update memory banks 24 and 27." (Id. at 9:63-67). Weight swapping with a two-bank architecture provides efficiency because it allows one FIR filter to retrieve and operate with data present in one coefficient memory bank, while the alternative memory bank is being updated with a new set of coefficients. (Id. at 10:67–11:10). Just as the '792 patent indexes memory to retrieve a selected set of coefficients from one of a plurality of FIR filters, the signal processor of Grumman (e.g., the real processing circuity 17 and imaginary processing circuitry 16) indexes memory by swapping between BANK 0 and BANK 1 to retrieve a selected set of adaptive weights corresponding to a unique FIR filter. (See id. at 9:10–15, Fig. 7c). "It is a further objective to provide a complex adaptive FIR filter that is able to do complex adaptive digital filtering without having to interrupt or stop the filtering process when the weight coefficients are being updated." (Ex. 1008 at 3:3–6). Thus, Grumman's FIR filter architecture is very efficient,

especially in the context of minimizing any delays caused by selecting a different set of FIR coefficients by indexing memory.

58. It is my opinion that a person of ordinary skill in the art would have been motivated to implement the FIR filter of Harris using the Grumman architecture. Because digital FIR filter processing requires operating on coefficient weights, digital FIR filter processing requires both processor and memory resources. A natural design choice for a person of ordinary skill in the art would have been to store the set of coefficients of a plurality of FIR filters in memory using an index for easy and efficient access by a processor as taught by Grumman. Moreover, in addition to Grumman, Terrell teaches a FIR filter that selectively retrieves FIR filter coefficients from memory, including a look up table. (See Ex. 1022 at 6:35–43, 6:43–48, 6:53–56, 21:19–51, 25:13–24 Fig. 11, Fig. 15). The Grumman FIR filters permit processing of "complex digital signals more quickly efficiently" where speed requirements would otherwise prohibit and "commercially available FIR filters." (Ex. 1008 at 2:55–62). The Grumman FIR filter "architecture takes maximum advantage of the time available to do the required calculations." (Id. at 2:68–3:2). In short, storing FIR filter coefficients in memory as does Grumman, yields a plurality of FIR filters that minimize delay when switching between different FIR filters. Accordingly, it is my opinion that a POSITA would have been motivated to implement the adaptive filter of Thomson using the FIR filter disclosures of Harris and Grumman, especially in light of the ease and efficient approach of indexing memory storing a set of FIR filter coefficients. For at least these reasons, the combination of Thomson, Harris, and Grumman renders this claim obvious.

D. Ground 2: Claim 25 is obvious over Thomson and Harris in view of Grumman.

 "25. The television receiver of claim 1, wherein the signal processor comprises a first computing unit and a second computing unit,"

59. Claim 25 is drawn to a signal processor that processes the real and imaginary parts of the finite impulse response in parallel. Such a claim is not novel or unobvious in light of Grumman. Grumman discloses a "FIR filter having an internal processing architecture that features two parallel data paths, one which filters the real data stream of the complex signal and another which filters the complex data stream." (Ex. 1008 at 2:63–3:2). "The first data path includes a first plurality of adaptive weight circuits for multiplying the real input data by predetermined coefficients to generate a set of multiplication results." (*Id.* at 3:36–39). "The second path includes a second plurality of adaptive weight circuits for multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the real set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the imaginary input data by predetermined coefficients to generate a set of multiplying the real field. The field of the field o

imaginary processing circuit 16." (*Id.* at 7:32–35). Thus, in my opinion, Grumman discloses a first computing unit and a second computing unit.

• "the first computing unit processing a real part of the finite impulse response filter operation"

60. Grumman discloses "a complex adaptive FIR filter having an internal processing architecture that features two parallel data paths, one which filters the real data stream of the complex signal and another which filters the complex data stream." (Ex. 1008 at 2:63–3:2). The first data path "filters the real data stream," (*Id.* at 2:66), and "process[es] the real input data portion of the input complex data" (*Id.* at 3:34–36). The real processing circuit 17 processes the real portion of the finite impulse response filter function. (*Id.* at 8:1–6, 6:64–7:10, Fig. 2, 5:44–56). Thus, in my opinion, Grumman discloses a first computing unit that processes the real part of the finite impulse response filter operation.

 "while the second computing unit processing an imaginary part of the finite impulse response filter operation."

61. Grumman discloses "a complex adaptive FIR filter having an internal processing architecture that features two parallel data paths, one which filters the real data stream of the complex signal and another which filters the complex data stream." (Ex.1008 at 2:63–3:2). The second data path "filters the imaginary data stream," (*Id.* at 5:7–11), and "process[es] the imaginary input data portion of the input complex data" (*Id.* at 3:39–41). The imaginary processing circuit 16

Silicon Labs v. Cresta Technology Sillab IPR Exhibit 1009 processes the imaginary portion of the finite impulse response function. (*Id.* at 8:6–8, 7:1–10, Fig. 2). Thus, in my opinion, Grumman discloses a second computing unit that processes the imaginary part of the finite impulse response filter operation.

A person of ordinary skill in the art would have been motivated to 62. implement the adaptive filter in Thomson according to the highly efficient real and imaginary parallel implementation of Grumman. As discussed with respect to claim 24 a person of ordinary skill in the art would have been motivated to combine Thomson, Harris, and Grumman. Grumman's adaptive FIR filter architecture is very efficient, especially in the context of minimizing any delays caused by selecting a different set of FIR coefficients by indexing memory. (Ex. See Ex. 1008, claims 10, 11 (showing that a POSITA would have been motivated to combine Grumman with Thomson)). Grumman discloses "a complex adaptive FIR filter that is able to do complex adaptive digital filtering without having to interrupt or stop the filtering process when the weight coefficients are being updated." (Ex. 1008 at 3:3-6). The Grumman FIR filters permit processing of "complex digital signals more quickly and efficiently" where speed requirements would otherwise prohibit "commercially available FIR filters." (Id. at 2:55-62). The Grumman FIR filter "architecture takes maximum advantage of the time available to do the required calculations." (Ex. 1008 at 2:68-3:2). Because of the

computational efficiency of Grumman in implementing adaptive FIR filters, it is my opinion that a POSITA would have been motivated to implement the adaptive filter of Thomson using the FIR filter disclosures of Harris and Grumman. It is my opinion that for at least these reasons, the combination of Thomson, Harris, and Grumman renders this claim obvious.

E. Ground 3: Claim 26 is obvious over Thomson and Harris in view of Zenith.

 "26. The television receiver of claim 1, further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the input RF signal and"

63. Thomson discloses a "signal processor" that has a "standard selection" input. It is my opinion that this "standard selection" signal provides an explicit suggestion to a POSITA that a format/standard selection circuit should be used to generate this signal. Because the construction of such a circuit was well-known to those skilled in the art, however, Thomson did not explicitly teach how to construct that circuit. Nonetheless, it is my opinion that Zenith provides an exemplary embodiment of a "format/standard selection circuit" that a POSITA would have been motivated to use to generate the "select signal" in Thomson.

64. Zenith "relates generally to television receivers and specifically to television receivers that are capable of receiving both analog and digital signals." (Ex. 1011, 1:7–10). The output of the tuner is selectively coupled to either an

analog demodulator or a digital demodulator. (*Id.* at Figs. 1–3). The selective coupling of the tuner to either the analog or digital demodulator is determined by the type of signal (analog or digital) received. (*Id.* at 3:13–15 ("As in Fig. 1 embodiment, microprocessor 22 controls the operation of switch 42 in accordance with the type of signal (analog or digital) that is received.").



65. Zenith discloses the actual details of a format/standard selection circuit for generating a select signal based on the format of the incoming RF signal as shown in Fig. 2. If "the presence of syncs corresponding to a demodulated analog type signal," is detected by sync detector 20, "microprocessor 22 routes the IF signal from tuner 12 to analog demodulator 16." (Ex. 1011, 2:38–41). Otherwise, "[i]n the absence of syncs corresponding to a demodulated analog type signal, microprocessor causes switch 14 . . . to couple the IF signal to digital

demodulator 18." (*Id.* at 2:42–45). It is my opinion that detecting syncs in the demodulated analog television signal would include detecting one or more of the horizontal or vertical sync signals. Since these sync signals are uniquely tied to a specific television standard, sync detection results in the identification of a specific television standard.

66. Accordingly, in my opinion, the Zenith microprocessor is a format/standard selection circuit that generates a select signal (output of microprocessor 22) that is indicative of the format (analog or digital) of the input RF signal and is coupled to the signal processor when combined with Thomson to generate the select signal in Thomson.

 "the signal processor selecting a finite impulse response filter in response to the select signal."

67. As described above, Thomson describes an adaptive bandpass filter that selects a particular filter in response to the "TV standard" input signal. Harris discloses a reconfigurable, reprogrammable signal processor that implements a plurality of FIR filters, each corresponding to a particular operating mode. (Ex. 1005, p. 6 ("the digital receiver structure also offers flexibilities like programmable filtering")). Accordingly, it is my opinion that Harris discloses a signal processor selecting a finite impulse response in response to the select signal of Thomson.

68. As discussed with respect to claim 1, a person of ordinary skill in the art would have been motivated to combine Thomson and Harris to implement the

adaptive filter of Thomson with the well-known FIR filters of Harris. That discussion is incorporated by reference herein and will not be repeated. In that case, the bandpass filter in Thomson would select the particular FIR filter function that corresponds to the incoming RF signal format, as indicated by the "TV standard" input.

69. A person of ordinary skill in the art would have been further motivated to combine Zenith with Harris and Thomson to implement a standard selection circuit as disclosed in Zenith to output the TV select signal of Thomson. Both Zenith and Thomson are directed toward a multistandard tuner capable of receiving both analog and digital television signals. (See Ex. 1011, 1:62-64 (an "object of the invention is to provide an improved low cost method of processing digital and analog television signals using a single tuner"); Ex. 1004, 1:29–33 ("It is an object of the invention to provide a broadcast receiver of the kind described which is suited for digital and analog input signals and using a common A/D converter only for analog and digital transmission via satellite.")). In my opinion, a receiver that can receive both analog and digital televisions signals must be able to identify the format or standard of the received signal for correct downstream processing. Fig. 2 of Zenith illustrates that the input to the analog or digital demodulator is controlled by a microprocessor, based on the format of the received RF signal. (Ex. 1011, Fig. 2, 3:13–15). Fig. 1 of Thomson shows an adaptive

filter 8 controlled by an input labeled "TV standard." (Ex. 1004 at Fig. 1). Just as Thomson needs to be aware of the TV standard, and thus the format of the input RF signal, for correct processing of the signal through the signal processor (band pass filter 8) (Ex. 1004, Fig. 1 (TV standard input controls band pass filter 8), 3:16–19 ("The following bandpass filter 8 (see Fig. 2g) with an adaptively controlled bandwidth selects the desired signal with minimal remainder of the adjacent channel signals.")), so does Zenith need to be aware of the standard and thus the format of the input RF signal (Ex. 1011, Fig. 2 (sync detector controlling microprocessor); 3:13–15 ("microprocessor 22 controls the operation of switch 42 in accordance with the type of signal (analog or digital) that is received")). Because Zenith and Thomson are directed to the same problem, a multistandard tuner capable of receiving and processing both digital and analog signals, each having different formats, it is my opinion that a POSITA would naturally look to the selection circuit in Zenith to generate the select signal in Thomson in light of the explicit suggestion to use a standard selection circuit in Thomson.

70. Accordingly, in my opinion, Thomson, Zenith and Harris would have been an obvious combination to a POSITA. Such an obvious combination could have been fashioned without undue experimentation by a POSITA because both the microprocessor and the sync detect circuit in Zenith were well-known circuits at the time. For at least these reasons, it is my opinion that claim 26 is obvious over Thomson, Harris, and Zenith.

F. Ground 3: Claim 28 is obvious over Thomson and Harris in view of Zenith.

"28. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal by detecting carrier signals identifying one of the formats of the input RF signals."

The standard selection circuit in the '792 patent automatically 71. provides "an auto-detection capability in receiver 100." (Ex. 1001, 6:7-11). One disclosed embodiment of doing so is to detect "in the baseband signals, the presence or absence of carrier signals which uniquely identify the television standards." (Id. at 6:11–15). The sync detector 20 and microprocessor 22 in Zenith perform this function. In Zenith "the presence of syncs associated with a demodulated analog signal is communicated to the microprocessor.") (Ex. 1011, 3:15–18). Just as in the '792 patent, by identifying syncs in the demodulated analog signal, Zenith identifies carrier signals in the input RF signal. (Id.). Moreover, the detected carrier signals identify the incoming RF signal as either analog or digital television signals. (Id. at 3:12–15). Accordingly, in my opinion, the output select signal of microprocessor 22 is generated by detecting the syncs, which are carrier signals in the input RF signal identifying the type of format of the input RF signal. Thus, it is my opinion, that the select signal in Zenith (output of microprocessor 22) is generated by sync detect 20, which detects carrier signals in the input RF signal identifying said format of said input RF signal.

72. As discussed above with respect to claim 26, in my opinion, a person of ordinary skill in the art would have been motivated to combine the carrier detection circuit of Zenith with Thomson and Harris to generate the select signal of Thomson. That discussion is incorporated by reference in its entirety and will not be duplicated herein. Thus, in my opinion, the combination of Thomson, Harris, and Zenith renders claims 28 invalid.

G. Ground 4: Claim 27 is obvious over Thomson and Harris in view of Zenith and Birleson.

 "27. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user."

73. User selection has long been the preferred method of controlling a television. From the earliest days of remote control, it is my opinion that users have been providing an input signal to a circuit that generates a select signal that is used to control the configuration of a television. Due to the proliferative nature of user control of television channel viewing, user selection of a channel is the predominant factor determinative of the format of the incoming RF.

74. Birleson (Ex. 1015) discloses an automatic carrier detect (ACD) circuit that "determines whether the signal being processed is in the digital or analog format." (Ex. 1015 at 10:52–54). The signal is tested by the ACD when

the channel is changed or alternatively the ACD testing can be initiated by a user, causing the selection circuit to generate the select signal: "ACD testing may be automatic or user-initiated. For example, a television system may provide a function on a remote control which allows the user to select the 'test mode.'" (Ex. 1015, 11:27-31; see also Ex. 1017 at 4:19-20 ("In other cases, the input format will have to be manually selected by the viewer.")). Birleson provides several examples a user-initiated generation of a standard select signal, for example, when the ACD is operating in "test mode," it "either switches SIFFb 109 out or leaves it in the signal path depending on whether an analog or digital signal is detected." (Ex. 1015 at 11:24–26). Signal testing by automatic carrier detection (ACD) circuit in Birleson may be initiated by a channel change. (Id. at 11:20–26). The ACD circuit detects "whether the incoming channel is an analog signal or digital signal." (Ex. 1015 at 10: 52-54). Besides changing the channel, a user could initiate signal testing by changing the input source. (Ex. 1015 at 11:29-30 (signal testing initiated in response to "an operator switching the input from an antenna or cable line to a videotape recorder or laser 25 disk player")). Furthermore, the "television system may provide a function on a remote control which allows the user to select the 'test mode'" (Id. at 11:34-37). In each of these examples in Birleson, the ACD circuit in test mode generates a select signal based on whether the input RF signal is an analog or digital signal. (Id. at 10:52–54 ("Fig. 3 shows

automatic carrier detection (ACD) circuit 30. The function of ACD circuit is to detect whether the incoming channel is an analog signal or digital signal.")). Thus, it is my opinion that Birleson discloses a "format/standard selection circuit generates the select signal in response to an input signal from a user."

75. An obvious design choice to a person of ordinary skill in the art, in my opinion, would be to generate the select signal in Thomson in response to the most common type of input, namely user input, such as input from a remote television control. Moreover, in my opinion, responding to user input is an obvious design choice to try because such input is one of a finite set of inputs to which Thomson could respond. Thus, a POSITA would be motivated to combine the user input functionality from Birleson with the select circuit of Zenith, along with Thomson to generate a select signal in response to an input signal from a user. (*Id.*). Accordingly, it is my opinion that the combination of Thomson in view of Zenith, and further in view of Birleson renders this claim obvious.

H. Ground 5: Claim 18 is obvious over Thomson and Harris in further view of Oku, Ericsson, and Nguyen.

76. Claim 18 is drawn to well-known circuit designs using well-known circuit elements—digital-to-analog converters, driver circuits, and single-ended and differential signaling—for providing either a differential output for a digital television signal format or single-ended output for an analog television format. Such circuit elements and signaling have been used in digital television tuners well

before the '792 patent. As shown below, the combination of claim elements of claim 18 are not novel or non-obvious, and thus claim 18 should be canceled as invalid.

 "18. The television receiver of claim 1, wherein the signal output circuit comprises: a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals";

77. Oku discloses a television receiver including a first digital-to-analog converter (*e.g.*, DAC 21 in Fig. 4) for receiving processed digital signals and converting those digital signals to analog output signals. (Ex. 1018, ¶ [0046], Fig. 4). Fig. 4 of Oku is shown below.

FIG. 4



Accordingly, in my opinion, Oku teaches this element.

Silicon Labs v. Cresta Technology Sillab IPR Exhibit 1009 "a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;"

78. The television receiver of Oku also includes a first driver circuit (*e.g.*, driving circuit 22 in Fig. 4) for driving analog output signals from DAC 16 to an output terminal. (Ex. 1018 at ¶¶ [0046] and [0066]). Accordingly, it is my opinion that Oku teaches this element.

"a second driver circuit for driving the analog output signals from the first digital-to-analog converter, the second driver circuit comprising a differential output driver circuit having a first differential output terminal and a second differential output terminal, the first differential output terminal being coupled to the first output terminal and the second differential output terminal being coupled to a second output terminal";

79. Oku discloses a second driver circuit (output circuit 26 of Fig. 4) for driving the analog output signals from DAC 21. (Ex. 1018 at Fig. 4). Because digital television circuits frequently used differential inputs, it is my opinion that a person of ordinary skill in the art would have been motivated to use differential signaling, a well-known design choice. (*See also* Kerth, Ex. 1021, Fig. 4 (showing use of differential signaling)). Such a choice would provide numerous advantages, including reduced interference effects or noise within a circuit, increased output voltage swing, ideal for low-voltage systems, integrated circuit is easier to use, and reduced even-order harmonics. (*See* Karki, Ex. 1033, p. 3)).

80. One such differential driver is disclosed in Fig. 2 of Ericsson. (Ericsson, Ex. 1024 at Fig. 2). The differential line driver in Ericsson receives input from a digital-to-analog converter and outputs a pair of current outputs. (Ericsson, Ex. 1024, 2:23–24, 2:31–32).

81. Maulik is another prior art reference that discloses a differential driver receiving input from a digital-to-analog converter. "Transmit driver 10 is shown throughout, including Fig. 2 as being a differential transmit driver." (Maulik, Ex. 1025, 2:48–49, Fig. 2). The "transmit driver 10 provides two current outputs iN and iP (respectively, representing the negative current and the positive current) which flow on lines 16 and 18 to external components block 12." (Ex. 1025 at 2:51–54).

82. Thus, in my opinion, the combination of Oku and Ericsson disclose this element.

 "a second analog-to-digital converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals;"

83. Oku discloses a second digital-to-analog converter (DAC 16) which receives processed digital output signals from the signal processor. (Ex. 1018 at Fig. 4). Although the output of DAC 16 is coupled to driving circuit 17 to drive a monitor, in my opinion, it would have been a mere design choice to input digital

signals encoding audio information into a digital-to-analog converter when audio signals are desired. Accordingly, it is my opinion that this element is met by Oku.

 "a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto the second output terminal,"

84. This element recites a third driver circuit whose output is connected to the second output terminal. This element, together with the preceding element, recites a structure in which the first and second output terminals are multiplexed or coupled to either (1) the first and third driver circuits or (2) the second differential driving circuit.

85. Oku discloses a third driver circuit (driving circuit 17 of Fig. 4) for driving the analog output signals from a second digital-to-analog converter (DAC 16) onto the second output terminal. (Ex. 1018 at Fig. 4). Oku discloses many different embodiments of output circuitry including multiple driver circuits. (*See e.g.*, Figs. 1, 5, 6, 7, 9–11). The specific configuration of output circuitry is dependent on the desired design factors. In the case of claim 18, the receiver can be connected to a component that receives an analog signal corresponding to an input RF signal that has either of analog or digital television format, but not both. In my opinion, a person of ordinary skill in the art would naturally choose to design a circuit that multiplexes the output lines connected to the differential and two single-ended drivers to reduce the pin count. Such a multiplexing architecture

is shown in Nguyen, which discloses a driving circuit architecture that is selectively controlled by control logic so that two input/output (I/O) pins are coupled to either (1) a differential driver (element 600), or (2) two single-ended drivers (elements 60). (Ex. 1031 at Fig. 7, 8:28-33). Thus, it is my opinion that it would have been obvious to a POSITA to combine the analog differential driver as disclosed in Ericsson with the drivers disclosed in Oku using the multiplexing architecture of Nguyen.

• "wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format; and the first output terminal provides video information encoded in the input RF signal and the second output terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format."

86. This element recites the multiplexing function, namely, (1) when the input RF signal has a digital television format, the signals on the first and second output terminals are indicative of video and audio information and (2) when the input RF signal has an analog television format, the signal on first output terminal provides video information and the signal on the second output terminal provides audio information. It is my opinion that such a multiplexing scheme would have

been an obvious design choice to a POSITA because the outputs are normally mutually exclusive.

87. Thomson discloses a television receiver that outputs audio and video information in the form of I and Q signals when the input RF signal has a digital television format. (Ex. 1004 at Fig. 1, 2:39–44). Furthermore, when the input RF signal to the Thomson receiver has a digital television format, the input signal to the synchronous demodulators 12 and 13 (and also the output from bandpass filter 8) in Thomson is a digital IF signal that includes audio and video information that may be output. (Ex. 1004 at Fig. 1, 2:39–44). Moreover, when the input RF signal has an analog television format, Thomson outputs video information (CVBS) and audio information (smod1 and smod2). (Ex. 1004 at Fig. 1). It is my opinion that a person of ordinary skill in the art would understand that these signals are logical candidates to multiplex on the same output terminals because they are mutually exclusive, *i.e.*, they do not exist simultaneously. A POSITA would further understand that these signals could be multiplexed onto the same terminals with output based on whether the input RF signal is in analog or digital television format to reduce the pin count of the circuit. Accordingly, in my opinion, a POSITA having knowledge of the receiver teachings of Thomson and Harris would be familiar with the basic driver and D/A structures such as Oku and

Ericsson, and the Nguyen multiplexing architecture. This fundamental knowledge of a POSITA renders the "wherein" claim element invalid.

88. A person of ordinary skill in the art would be motivated to combine Harris, Thomson, Oku, Ericsson, and Nguyen. As discussed previously with respect to claim 1, a person of ordinary skill in the art would be motivated to implement the adaptive filter 7 of Thomson using the FIR filters of Harris. Moreover, claim 18 relates to outputting either a differential output or two singleended signals on the first and second output terminals. In my opinion, because the signals relating to analog or digital formats are mutually exclusive (i.e., the receiver is only outputting either an analog or digital television signal) when two output terminals are shared for outputting the video and audio signals, signals would be present on the output terminals from only one of (1) the differential driver when the television signal corresponding to a digital format or (2) the two single-ended drivers when the television format corresponds to an analog format. To reduce the number of input/output pins, it is my opinion that a person of ordinary skill would be motivated to use the architecture of Nguyen to selectively couple either a differential driver or two single-ended drivers to two output lines to reduce the number of lines because it would result in a lower cost design.

89. In my opinion, the details of the actual output circuit, including the digital-to-analog and driver circuits are mere design choices within the knowledge

of a person of ordinary skill in the art. Oku discloses many different embodiments of output circuitry including multiple driver circuits, e.g., in Figs. 1, 4, 6, 7, 9–11. The particular configuration of a digital-to-analog converter and driving circuit, as discussed above is a mere design choice, well within the knowledge of one of ordinary skill in the art. When the input RF signal has a digital television format, the output of the bandpass filter 8 of Thomson drives a first digital-to-analog converter (disclosed in Oku), which in turn, drives a differential driver (disclosed in Ericsson). Alternatively, when the input RF signal has an analog television format, the output of the analog demodulator 9 drives the first digital-to-analog converter, which in turn drives a first driver (disclosed in Oku (Ex. 1018)), and the output of smod1 or smod2 drives a second analog-to-digital converter (disclosed in Oku (Ex. 1018)), which in turn drives a second driver (disclosed in Oku (Ex. 1018)). The outputs of the differential and first and second drivers are multiplexed together using the architecture disclosed in Nguyen (Ex. 1031). Accordingly, in my opinion, the combination of Thomson, Harris, Oku, Ericsson, and Nguyen, and render claim 18 invalid.

I. Ground 5: Claim 19 is obvious over Thomson and Harris in further view of Oku, Ericsson, and Nguyen.

• "19. The television receiver of claim 18, wherein the signal output circuit further comprises: a low pass filter coupled between the first digital-to-analog converter and the first and

second driver circuits, the low pass filter providing low pass filtering function."

90. Including a low pass filter at the output of a digital-to-analog converter is a mere design choice based on the properties of the DAC and downstream circuitry. A low-pass filter smoothes out waveforms and reduces or eliminates high-frequency noise which may be introduced by the electronic circuitry including the DAC. Such high-frequency noise may result in unwanted EM radiation. Because EM radiation of consumer electronics is highly regulated, a POSITA would be motivated to use a low-pass filter at the output and reduce this possibility. This design choice is within the skill of a POSITA and would lead to predictable results. It is my opinion that it would be obvious to one of ordinary skill in the art to provide low-pass filtering of a baseband signal for attenuation of unwanted frequencies being output by baseband audio and video signal outputs. Accordingly, Thomson, Harris, Oku, Ericsson, and Nguyen render claim 19 invalid.

J. Summary Claim Charts for Challenged Claims

91. A detailed listing of further disclosures of Thomson, Harris, Grumman, Zenith, Birleson, and this Declaration relevant to the claim elements at issue in this Petition appears in the claim charts below.

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VI. CONCLUSION

92. In summary, it is my opinion that claims 18, 19, and 24–29 are obvious in view of certain prior art references.

93. It is my opinion that the combination of Thomson and Harris renders Claim 29 obvious.

94. It is my opinion that the combination of Thomson, Harris, and Grumman render Claims 24 and 25 obvious.

95. It is my opinion that the combination of Thomson, Harris, and Zenith render Claims 26 and 28 obvious.

96. It is my opinion that the combination of Thomson, Harris, Zenith, and Birleson renders Claim 27 obvious.

97. It is my opinion that the combination of Thomson, Harris, and Oku, Ericsson, and Nguyen render Claims 18 and 19 obvious.

98. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

Silicon Labs v. Cresta Technology Sillab IPR Exhibit 1009 99. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available.

VII. ACKNOWLEDGEMENT

100. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements or the like may jeopardize the validity of the patent or any patent issuing thereon.

Signed in Wimberley, Texas on January 26, 2015

Way he Dally

Douglas Holberg

APPENDIX A

Douglas R. Holberg, Ph.D. 820 Camino de Rancho, Wimberley, TX. 78676 (512) 970-4007 ip@holberg.org

Education

B.S.E.E. - 1977, Texas A&M University, College Station, TX.M.S.E. - 1989, The University of Texas, Austin, TX.Ph.D. - 1992, The University of Texas, Austin, TX.

Experience

Intellectual Property Technical Consultant -

Jan 2008 – Present: Principal Patent analysis for licensing (offensive and defensive) Technical support for patent prosecution Patent review for valuation

Silicon Laboratories -

Jun 2005 – Jan 2008: V. P. of Technology Dec 2003 – Jun 2005: Director of Engineering, MCU Products

Cygnal Integrated Products - Feb. 1999 to Dec 2003 (acquired by Silicon Labs Dec 2003)

Vice President of Engineering, Chief Technical Officer, Co-founder Concurrent to the position at Cygnal, I served as Adjunct Assistant Professor at the University of Texas at Austin, and Technical Advisory Boards for Silicon Metrics and Celite Systems.

Adjunct Assistant Professor, University of Texas as Austin - 1995-2001

Taught "CMOS Analog Circuit Design" Graduate class: EE397K and Undergraduate class: EE338L

Crystal Semiconductor Corp. - Sep. 1996 to Feb. 1999

Director of Imaging and Video Products (CCD interface, CMOS imagers, TV encoders, etc.)

Crystal Semiconductor Corp. - Oct. 1992 to Sep. 1996

Design Manager for VLSI mixed-signal products including telecommunications and disk drive read channel devices.

Independent Consultant - Aug. 1987 to Oct. 1992

Taught a short-course entitled "CMOS Analog Integrated Circuit Design" in Berlin, Germany twice per year as a part of the "Berlin Continuing Engineering Education Program." In addition, this course was taught at Analog Devices BV, Ireland, Aug. 1990.

Lectured at Baylor University's Department of Engineering (Spring '89, Spring '91).

Consultant for Advanced Micro Devices, Crystal Semiconductor, and other companies on projects relating to switched-capacitor filters, operational amplifiers, latchup, and the ISDN analog interface.

Crystal Semiconductor Corp. - Oct. 1984 to Aug. 1987

Project leader on the CS7008 Universal Filter--a universal programmable filter using novel switched-capacitor techniques. This design was completed in a 3µm silicon-gate double-polysilicon CMOS process.

Texas Micro Engineering, Inc. - June 1980 to Oct. 1984

Project leader on TME3030 Sense Amplifier/Filter--a dual-channel switched-capacitor filter circuit to be used in a medical electronic application. Performed extensive device characterization of MOS transistors. This work included characterization of noise performance and characterization of transistors operating in weak inversion.

Mostek, Inc., Carrollton, TX. - Jan. 1978 to June 1980

Circuit designer. Served as project leader on MK5387 DTMF generator.

Inventions

1.	8,010,819	Microcontroller unit (MCU) with power saving mode
2.	7,719,595	Preview mode low resolution output system and method
3.	7,660,968	Reconfigurable interface for coupling functional input/output blocks to limited number of I/O pins
4.	7,613,901	Comparators in IC with programmably controlled positive / negative hysteresis level and open-
		drain/push-pull output coupled to crossbar switch or rising/falling edge interrupt generation
5.	7,511,465	Digital pulse width modulated power supply with variable LSB
6.	7,504,902	Precision oscillator having linbus capabilities
7.	7,504,900	Integrated circuit package including programmable oscillators
8.	7,502,883	USB integrated module
9.	7,498,962	Analog-to-digital converter with low power track-and-hold mode
10.	7,441,131	MCU with power saving mode
11.	7,421,251	Precise frequency generation for low duty cycle transceivers using a single crystal oscillator
12.	7,382,181	Method and apparatus for tuning GMC filter
13.	7,323,855	Digital pulse width modulated power supply with variable LSB
14.	7,315,200	Gain control for delta sigma analog-to-digital converter
15.	7,304,679	Preview mode low resolution output system and method
16.	7,289,145	Correlated double sampling variable gain amplifier circuit for use in a digital camera
17.	7,286,176	CCD imager analog processor systems and methods
18.	7,256,611	Cross-bar matrix with LCD functionality
19.	7,171,542	Reconfigurable interface for coupling functional input/output blocks to limited number of i/o pins
20.	7,164,311	Method and apparatus for tuning GMC filter
21.	7,061,421	Flash ADC with variable LSB
22.	6,950,047	Method and apparatus for combining outputs of multiple DACs for increased bit resolution
23.	6,922,164	SAR analog-to-digital converter with abort function
24.	6,891,487	Capacitor calibration in SAR converter
25.	6,879,004	High voltage difference amplifier with spark gap ESD protection
26.	6,724,336	Segmented D/A converter with enhanced dynamic range
27.	6,720,999	CCD imager analog processor systems and methods
28.	6,686,957	Preview mode low resolution output system and method
29.	6,617,934	Phase locked loop circuits, systems, and methods
30.	6,448,917	DAC using current source driving main resistor string
31.	6,400,300	D/A converter street effect compensation
32.	6,384,763	Segemented D/A converter with enhanced dynamic range
33.	6,288,661	A/D converter with voltage/charge scaling
34.	6,285,536	High voltage input pad system
35.	6,172,361	Methods for mounting an imager to a support structure and circuitry and systems embodying the same
36.	6,038,116	High voltage input pad system
37.	4,849,662	Switched-capacitor filter having digitally-programmable capacitive element
38.	4,492,927	Offset voltage compensation circuit
39.	4,390,754	Tone generator circuit

Currently have 26 pending applications in the PTO.

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Ka Y. Leung, Kafai Leung, Douglas R. Holberg, "A Dual Low Power ½ LSB INL 16b/1Msamples/s SAR A/D Converter with on-chip Microcontroller, *Proc. 2006 Asian Solid State Circuits Conference*, Nov 2006.

Welland, D.; Phillip, S.; Tuttle, T.; Ka Leung; Dupuie, S.; Holberg, D, et al., "Implementation of a digital read/write channel with EEPR4 detection," IEEE Transactions on Magnetics, Volume: 31, Issue: 2, 1995.

Welland, D.; Phillip, S.; Ka Leung; Anderson, K.; Armstrong, A.; Tuttle, T.; Dupuie, S.; Holberg, D.; et al., "An EEPR4 Read/Write Channel," Digest of the Magnetic Recording Conference 1994.

D. Welland, S. Phillip, K. Leung, G. Tuttle, S. Dupuie, D. Holberg, et al., "A Digital Read/Write Channel with EEPR4 Detection," *Proc. IEEE International Solid-State Circuits Conference*, Feb. 1994.

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Douglas R. Holberg, Santanu Dutta, Lawrence Pillage, "DC Parameterized Piecewise-Function Transistor Models for Bipolar and MOS Logic Stage Delay Evaluation," Proc. IEEE International Conference on Computer-Aided Design, Nov. 1990.

Douglas R. Holberg, "Digitally Programmable Filter Based on Standard Cell Design," IEEE Analog/Digital VLSI Workshop, Sept. 1986.

Tom Dille, Douglas Holberg, and Roger Taylor, "Programmable Filter Chip and its PC-Based Tools Offer New Analog Solutions," Electronic Design, May 29, 1986.

Books

Phillip E. Allen and Douglas R. Holberg, <u>CMOS Analog Circuit Design</u>, New York: Holt Rinehart, and Winston, ©1987.

Phillip E. Allen and Douglas R. Holberg, <u>CMOS Analog Circuit Design</u>, 2nd Ed, Oxford University Press, ©2002.

Phillip E. Allen and Douglas R. Holberg, <u>CMOS Analog Circuit Design</u>, 3rd Ed, Oxford University Press, ©2011.

Other Professional Activities

Served on the "Industrial Electronics Advisory Committee" for the University of Texas Instruction and Materials Center, University of Texas, Austin, 1988-1989.

Baylor University Board of Advocates, 2001 to 2003.

Member of IEEE

APPENDIX B

Claim Chart of United States Patent No. 7,265,792				
United States Patent No. 7,265,792	Invalidating References			
29. The television receiver of claim 1, wherein the input RF signal comprises an RF signal received from terrestrial broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission.	Thomson, Ex. 1004 at 1:55–2:3.			
24. The television receiver of claim 1, wherein the plurality of finite impulse response filters are stored in a memory, and	Grumman, Ex. 1008, 3:31–34, 4:7–14, 11:25–29, Figs. 1a, 1b, 7b, 7c.			
the signal processor indexes the memory to retrieve one of the plurality of finite impulse response filters.	Grumman, Ex. 1008, 2:55–62, 2:68–3:2, 3:3–6, 9:10–15, 9:63–67, 10:67–11:10.			
25. The television receiver of claim 1, wherein said signal processor comprises a first computing unit and a second computing unit,	Grumman, Ex. 1008, 2:63–3:2, 3:36–39, 3:41– 44, 7:32–35.			
the first computing unit processing a real part of the finite impulse response filter operation	Grumman, Ex. 1008, 2:63–3:2, 3:34–36, 5:44– 56, 6:64–7:10, 8:1–6, Fig. 2.			
while the second computing unit processing an imaginary part of the finite impulse response filter operation.	Grumman, Ex. 1008, 2:55–3:2, 3:3–6, 3:31–34, 5:7–11, 7:1–10, 8:6–8.			

26. The television receiver of claim 1 further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the	Zenith, Ex. 1011, 1:7–10, 2:38–45, 3:13–15, Figs 1–3.
the signal processor selecting a	Harris, Ex. 1005, p. 6.
response to the select signal.	Zenith, Ex. 1011, 1:62–64, Fig. 2.
	Thomson, Ex. 1004, 1:29–33, 3:13–19, Fig. 1.
27. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user.	Birleson, Ex. 1015, 10:52–54, 11:20–31, 11:34– 37
28. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal by detecting carrier signals identifying one of the formats of said input RF signals.	Zenith, Ex. 1011, 3:12–18, Fig. 1.
18. The television receiver of claim 1, wherein the signal output circuit comprises: a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;	Oku, Ex. 1018 ¶ [0046], Fig. 4.

a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;	Oku, Ex. 1018 at ¶¶ [0046], [0066].
a second driver circuit for driving the analog output signals from the first digital-to-analog converter, the second driver circuit comprising a differential output driver circuit having a first differential output terminal and a second differential output terminal, the first differential output terminal being coupled to the first output terminal and the second differential output terminal being coupled to a second output terminal;	 Oku, Ex. 1018 at Fig. 4. Ericsson, Ex. 1024 at 2:23–24, 2:31–32. Kerth, Ex. 1021 at Fig. 4 (showing level of ordinary skill in the art). Karki, Ex. 1033 at 3 (showing level of ordinary skill in the art). Maulik, Ex. 1025 at 2:48–49 and Fig. 2 (showing level of ordinary skill in the art.
a second analog-to-digital converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto the second output	Oku, Ex. 1018 at Fig. 4. Oku, Ex. 1018 at Figs. 1, 4, 5, 6, 7, 9–11. Nguyen, Ex. 1031 at Fig. 7, 8:28-33.

wherein the first and second	A POSITA would be motived to combine
output terminals provide	Thomson (television receiver), Harris (FIR
differential output signals	filters), Oku (DAC and drivers), Ericsson
indicative of video and audio	(differential driver), and Nguyen (architecture of
information encoded in the input	multiplexing a differential and two single-ended
RF signal when the input RF	drivers on a common set of pins).
signal has a digital television	
signal format; and the first	
output terminal provides video	
information encoded in the input	
RF signal and the second output	
terminal provides signals	
indicative of audio information	
encoded in the input RF signal	
when the input RF signal has an	
analog television signal format.	
The television receiver of claim	Including a low pass filter at the output of a
18, wherein the signal output	DAC is a mere design choice.
circuit further comprises: a low	
pass filter coupled between the	
first digital-to-analog converter	
and the first and second driver	
circuits, the low pass filter	
providing low pass filtering	
function.	