

Exhibit 1010



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Enclosed herewith for filing is a patent application, as follows:

Inventor(s): Pierre Favrat, Alain-Serge Porret, Dominique Python, Friederich Mombers, Richard P. Perring, Philippe Duc, Benito Carnero, Didier Margairaz
Title: Television Receiver for Digital and Analog Television Signals

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3 Sheet(s) of Drawings (Figs. 1, 2, 3A, and 3B)
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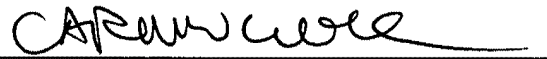
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Title	Television Receiver for Digital and Analog Television Signals	
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Television Receiver For Digital and Analog Television Signals

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FIELD OF THE INVENTION

[0001] The present invention relates to a television signal receiver, and in particular, the present invention relates to a broadband television signal receiver for receiving multi-standard analog television signals and digital television signals.

DESCRIPTION OF THE RELATED ART

[0002] A television (TV) or video recorder includes a television signal receiver (or television receiver) to receive terrestrial broadcast, cable television or satellite broadcast television signals and to process the television signals into the appropriate video signals for display or for recording. Television signals are transmitted in analog or digital formats and in accordance with a variety of standards. For analog television transmission, the NTSC (National Television Standards Committee) standard, the PAL (Phase Alternate Lines) standard, and the SECAM (Sequential Couleur Avec Memoire) standard are widely adopted. On the other hand, for digital television transmission, the DVB (Digital Video Broadcast) format and the

ATSC (Advanced Television Standards Committee) format are available. Because the different television formats and different television standards are incompatible, television receivers are traditionally made specifically for the analog or digital format and for a specific standard. Thus, televisions or video recording equipments are dedicated equipments which can only be used in the geographic regions in which the television standard is broadcasted.

[0003] The operation of a conventional television receiver includes two main components. First, the receiver receives the incoming television signal in radio frequency (RF) and converts the incoming RF signal to an intermediate frequency (IF) signal. Then, the receiver converts the IF signal to a video baseband signal and an audio baseband signal. The baseband signals are coupled to appropriate video and audio decoders to generate the display video signals (e.g. RGB) or sound. In general, the conventional television receiver includes a tuner for receiving the input RF signal and converting the RF signal to an IF signal by one or more frequency conversions. The frequency conversions are generally implemented as single or dual super-heterodyne conversions. In conventional television receivers, the intermediate frequency is dictated by the geographical area the receivers are to be used. Currently, there are five intermediate frequencies being used in the world. For example, in the United States, the IF is 41 to 47 MHz.

[0004] The conventional television receiver also includes a channel filter and a demodulator for converting the IF signal to video and audio baseband signals. The channel filter is typically a discrete filter implemented as a SAW (Surface

Acoustic Wave) filter. The shape of the SAW filter is designed specifically for the format (analog or digital TV) and the television standard (NTSC, PAL or SECAM) of the television signals being received. The demodulator is typically a dedicated component and designed specifically for a predetermined television signal format and a predetermined television standard. For analog television signal reception, the demodulator is a VIF/SIF module. The VIF/SIF module provides a video output called CVBS (Composite Video Baseband Signal) and audio outputs, such as MPX or A2. For digital television signal reception, the demodulator is a digital demodulator typically including a down-converter, an analog-to-digital converter and other supporting circuitry to perform the demodulation. The digital demodulator outputs data in a MPEG data stream.

[0005] Television receivers for receiving both analog and digital television signals are being developed. These dual-format television receivers are typically implemented by duplicating the hardware required for processing the analog television signals and digital television signals. For instance, it is known to implement a dual-format television receiver by using a bank of channel filters, each of the channel filters designed for a specific format and standard, and a bank of demodulators, each demodulator receiving filtered signals from a corresponding channel filter. A switch can be used to select the desired signal processing path including the desired channel filter and the associated demodulator. An alternate implementation, proposed by U.S. Patent 6,369,857 to Balaban, involves digitizing the intermediate frequency signal and processing the digitized signal using two separate processing

circuitry - one for the analog television signal and one for the digital television signal.

[0006] A television receiver for providing dual-format reception is desired. It is further desirable that such a dual-format television receiver be cost effective to manufacture and provides high quality video and audio performance.

SUMMARY OF THE INVENTION

[0007] According to one embodiment of the present invention, a television receiver includes a frequency conversion circuit, an analog-to-digital converter, a signal processor, and a signal output circuit. The frequency conversion circuit receives an input RF signal and converts the input RF signal to an intermediate frequency signal having an intermediate frequency (IF). The input RF signal encodes information in one of several television signal formats. The analog-to-digital converter samples the intermediate frequency signal and generates a digital representation thereof. The signal processor processes the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal and generates digital output signals indicative of information encoded in the input RF signal. Finally, the signal output circuit receives the digital output signals from the signal processor and provides one or more output signals corresponding to the digital output signals.

[0008] In one embodiment, the television signal formats include an analog television format and a digital television format. The signal output circuit can be configured to provide output signals corresponding to an analog television format or a

digital television format or both. In another embodiment, the television receiver is formed as a monolithic integrated circuit.

[0009] The present invention is better understood upon consideration of the detailed description below and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a schematic diagram of a dual-format television receiver according to one embodiment of the present invention.

[0011] Figure 2 is a block diagram illustrating alternate embodiments of the signal output circuit which can be incorporated in the dual-format television receiver of Figure 1.

[0012] Figure 3A is a block diagram of a dual-format television receiver system employing the television receiver of Figure 1 according to one embodiment of the present invention.

[0013] Figure 3B is a block diagram of a dual-format television receiver system employing the television receiver of Figure 1 according to an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] In accordance with the principles of the present invention, a dual-format television (TV) receiver for receiving analog and digital TV signals uses a single signal processing circuit for processing the received input RF television signal. The dual-format television receiver provides output signals indicative of the analog or digital television format of the

received television signal. The output signals can be coupled to demodulators and/or decoders to generate the baseband signals and subsequently the video/audio signals for display or recording. In one embodiment, the dual-format TV receiver includes a frequency conversion circuit (a tuner), a digitizing IF circuit, a digital signal processor (DSP) circuit and a signal output circuit. In one embodiment, the dual-format TV receiver provides a first output signal that is the video baseband signal for television signals transmitted in the analog format, a second output signal that is the audio baseband signal for television signals transmitted in the analog format, and a third output signal that is the digital television (DTV) low-IF signals for television signals transmitted in the digital format.

[0015] The dual-format television receiver of the present invention provides many advantages not realized by conventional television receivers. First, by processing all signals in the digital domain, the TV receiver of the present invention eliminates the need for analog components, such as SAW filters. Thus, the TV receiver of the present invention can be readily integrated in one integrated circuit to reduce the size and the manufacturing cost of the receiver. In one embodiment, the dual-format TV receiver is formed as a monolithic integrated circuit. As such, the receiver integrates a large part of the components for a television receiver system into a single integrated circuit. A television receiver system incorporating the dual-format television receiver of the present invention can thus be built with minimal components, reducing the size and the overall manufacturing cost of the television receiver system. Another advantage of the dual-format TV receiver of the present invention is that the digital signal processor circuit of the receiver uses

a single signal processing path to process television signals in either the analog format or the digital format. Thus, the need to duplicate components is entirely obviated. Finally, the digital signal processor circuit can be readily reconfigured to support multi-standard reception, thereby enabling the television receiver of the present invention to be used in any geographical area of interest.

[0016] Figure 1 is a schematic diagram of a dual-format television receiver according to one embodiment of the present invention. Referring to Figure 1, a dual-format television receiver 100 includes a signal input terminal 102 for receiving incoming RF signal, a first output terminal 104 for providing a first output signal for television signals transmitted in the analog format, a second output terminal 105 for providing a second output signal for television signals transmitted in the analog format, and a third output terminal 106 for providing a third output signal for television signals transmitted in the digital format. The signal input terminal and output terminals of receiver 100 can be configured as single-ended or differential terminals, depending on the applications.

[0017] In the present embodiment, signal input terminal 102 is a single-ended input terminal. In an alternate embodiment, a differential input terminal can also be used. When signal input terminal 102 is a differential input terminal, receiver 100 further includes a balun transformer to convert the differential input signals into a single-ended signal, as is well understood by one of ordinary skill in the art.

[0018] Furthermore, in the present embodiment, first and second output terminals 104, 105 are single-ended output

terminals while third output terminal 106 is a differential output terminal. Third output terminal 106 therefore includes two signal ports providing differential signals. In the present description, a differential output terminal is sometimes referred to as an "output terminal" but it is understood that the differential output terminal actually includes two signal ports. As will be described in more detail below, each of the output terminals of receiver 100 can be configured as either a differential output terminal or a single-ended output terminal or two single-ended output terminals can be used to provide differential output signals. Moreover, receiver 100 can provide output signals in either analog or digital format on one or more output terminals. Thus, the output signals corresponding to the video and audio signals for analog television signals can be provided in either analog or digital format and using single-ended or differential output terminals. Similarly, the output signals corresponding to the video and audio signals for digital television signals can be provided in either analog or digital format and using single-ended or differential output terminals.

[0019] Dual-format TV receiver 100 processes the incoming RF signal and provides output signals depending on the television format of the incoming RF signal. When the incoming RF signal is in the analog television format, receiver 100 provides first and second output signals which can be decoded to generate the video and audio signals for display. When the incoming RF signal is in the digital television format, receiver 100 provides the third output signal which can be demodulated and decoded to generate the video and audio signals for display. In one embodiment, the dual-format TV receiver 100 is formed as a monolithic integrated circuit. Thus, an integrated circuit implementing TV receiver

100 of the present invention can include as few as five pins in the present embodiment, apart from the power supply and ground pins. As will be discussed in more detail below, in other embodiments of the dual-format TV receiver of the present invention, an integrated circuit implementing TV receiver 100 of the present invention can include as few as three pins, apart from the power supply and ground pins.

[0020] Referring to Figure 1, receiver 100 includes a frequency conversion circuit 110 (or tuner circuit 110), a digitizing IF circuit 120, a digital signal processor (DSP) circuit 130 and a signal output circuit 140. Frequency conversion circuit 110 receives input RF signals on signal input terminal 102. The input RF signals can be received from terrestrial broadcast or cable transmissions. Frequency conversion circuit 110 operates to convert the input RF signal to an intermediate frequency (IF) signal using one or more frequency conversions. In the present illustration shown in Figure 1, the input RF signal is first coupled to a RF tunable filter 111 which is a bandpass filter. Then, the filtered signal is coupled to a variable gain low noise amplifier 112. The output signal of amplifier 112 is coupled to a bandstop filter 113 which is also known as a "notch filter." The output signal of bandstop filter 113 is then coupled to a mixer 114, controlled by a phase-locked loop 115. Mixer 114 operates to tune the filtered input RF signal to the desired frequency range in one or more frequency conversions and generate the IF signal. Frequency conversion circuit 110 provides the IF signal on a terminal 116 have a preselected intermediate frequency.

[0021] In accordance with the present invention, frequency conversion circuit 110 can be designed to generate IF signals having an intermediate frequency of any values. The IF used by tuner 110 can be the same as or different than the IF specified by the worldwide standards. Furthermore, as receiver 100 uses a single digital signal processor for signal processing, tuner 110 can use the same IF for receiving analog or digital television signals in any standards. The value of the IF in an integrated tuner is a matter of design choice. In one embodiment, the IF is selected to be 20 MHz or higher.

[0022] The IF signal generated by frequency conversion circuit 110 having a preselected intermediate frequency is provided to digitizing IF circuit 120 of receiver 100. Digitizing IF circuit 120 includes a bandpass filter 121, a variable gain amplifier 122 and an analog-to-digital converter (ADC) 123. The IF signal is filtered by bandpass filter 121. Then, amplifier 122 operates on the filtered IF signal for the purpose of regulating the dynamic range of ADC 123. ADC 123 operates to digitize the analog IF signal and provide a digital IF signal on a terminal 124. Receiver 100 thereby performs subsequent processing in the digital domain entirely. By applying the appropriate sampling frequency at ADC 123 and the appropriate signal processing functions at DSP circuit 130, receiver 100 can handle television signals in any format (analog or digital) and in any standard (e.g.: NTSC, PAL, SECAM, DVB or ATSC).

[0023] In the present embodiment, ADC 123 is a 10-bit converter and has a sampling rate of up to 40 megasamples per second. In other embodiments, ADC 123 can have other resolution and in most applications, a resolution of greater than 9 bits

will suffice. The sampling frequency of ADC 123 is selected based on the intermediate frequency of the IF signal and should be at least larger than twice the bandwidth of the intermediate frequency signal. The sampling frequency of ADC 123 can be adjusted by using a voltage controlled oscillator and a phase locked loop (not shown in Figure 1). In an alternate embodiment, a tuning control circuit (not shown) can be included for adjusting the sampling frequency of ADC 123. The tuning control circuit can receive a control signal external to receiver 100, such as a manual control signal from a user. The tuning control circuit can also perform auto-detection of the intermediate frequency of the IF signals and adjust the operating frequencies of the ADC accordingly.

[0024] After the IF signal is filtered and digitized, the digital representation of the signal is processed by a digital signal processor (DSP) 131 in DSP circuit 130. DSP 131 processes the digital IF signal according to the television format and standard to which the input RF signal is encoded. In the present illustration, DSP circuit 130 includes a format/standard selection circuit 133 for selecting between the several analog television standards and the several digital television standards. DSP 131 applies the appropriate filter function, such as an impulse response, to the digital IF signals received on terminal 124 depending on the state of format/standard selection circuit 133. In one embodiment, the coefficients of the filter functions are stored in a look-up table in a memory 132 in DSP circuit 130. DSP 131 retrieves the coefficients from memory 132 to be applied to the incoming digital signals.

[0025] DSP 131 is a programmable and reconfigurable processor. In the present embodiment, DSP 131 implements a finite impulse response (FIR) filter which is reconfigured based on the TV standard selected. Furthermore, in the present embodiment, DSP 131 includes two computing units to speed up the computation time. Specifically, the filtering operations of the real and imaginary parts in the frequency domain are carried out in parallel. In other embodiments, DSP 131 may include only one computing unit.

[0026] Format/standard selection circuit 133 can be implemented in one of many ways. The selection of the correct format and television standard can be made manually by the user of the television system, such as by activating a switch, or the selection can be made automatically by providing an auto-detection capability in receiver 100. In the present embodiment, auto-detection is implemented by detecting in the first and second output signals the presence or absence of carrier signals which uniquely identify the television formats and standards. For example, analog television signals can be identified by the analog visual carrier signal while digital television signals can be identified by the pilot carrier. A detection circuit can be included in receiver 100 for generating a signal which is fed back to format/standard selection circuit 133 indicating which television format and standard the input signal is encoded. In other embodiments, other means for selecting between the different formats and standards can be used.

[0027] When the input RF signal is an analog television signal, DSP 131 applies a video filter function and a sound filter function to the digitized signals to separate the video

signals from the audio signals. The video and sound filters can be implemented as FIR filters. DSP 131 can also implement other filter functions such as ghost cancellation for reducing the interference of the input signal. The filter response is then derived from the measured channel response. In the present embodiments, DSP 131 generates a processed IF signal on terminal 134 as the video baseband signal and a processed IF signal on terminal 135 as the audio baseband (or sound IF) signal.

[0028] When the input RF signal is a digital television signal, DSP 131 applies a filter function to the digitized signals. The filter function can be implemented as a FIR filter. An example is the ATSC-VSB standard where the filter response is specified as raised root cosine with 0.1152 roll-off (refer to the ATSC A-53 specification). Furthermore, additional filter functions, such as an equalizer for echo cancellation (multipath), can also be implemented in DSP 131. The filter response is then derived from the measured channel response. In the present embodiment, DSP 131 also performs a down-conversion function for converting the IF signal into a low IF signal.

[0029] The processed IF signals on terminals 134 and 135 are coupled to signal output circuit 140 to be converted into the desired output signals. In accordance with the present invention, signal output circuit 140 can assume various configurations to provide output signals in different formats. A configuration for signal output circuit 140 can be selected based on factors such as the desired pin count for receiver 100 and the desired format for the output signals. One useful feature of signal output circuit 140 is that the signal output circuit can be configured to provide output signals for analog TV format and

digital TV format simultaneously. That is, a first set of output signals can be provided for the television signals received in the analog television format and a second set of output signals can be provided for the television signals received in the digital television format so that television signals for both analog and digital formats can be displayed at the same time. Simultaneous display of analog and digital television signals is not possible in the conventional television receivers as the conventional television receivers carry out input or output switching operation to select only one of the two television signals to be processed.

[0030] Figure 1 illustrates one embodiment of a signal output circuit which can be incorporated in receiver 100 of the present invention. Other embodiments of the signal output circuit are shown in Figure 2. Referring first to Figure 1, signal output circuit 140 includes a digital-to-analog converter (DAC) 141 coupled to a low pass filter 142. The processed digital signals provided by DSP 131 on terminal 134 is coupled to DAC 141 to be converted back to analog format. The analog signal is filtered by low pass filter 142 to smooth out the signal. The filtered analog signal is coupled to a first driver 143 to provide a first output signal for analog television format on output terminal 104 and also to a second driver 144 to provide a third output signal for digital television format on output terminal 106. Meanwhile, DSP 131 also provides the processed digital sound signal on terminal 135 to a DAC 145. The output signal from DAC 145 is coupled to a third driver 146 to provide a second output signal on output terminal 105 for the analog television format. In the present embodiment, driver 143 and driver 146 are single-ended drivers while driver 144 is a differential output driver. In one

embodiment, driver 144 is a low voltage differential signaling driver.

[0031] As thus configured, signal output circuit 140 provides analog television signals on output terminals 104 and 105 and digital television signals on output terminal 106 which is a differential output terminals (2 signal ports). In the present embodiment, the first output signal is a Composite Video Baseband Signal (CVBS) for analog television signals and the second output signal is the audio baseband signal for analog television signals. The third output signal is a DTV low-IF signal for digital television signals.

[0032] Turning now to Figure 2 where alternate embodiments of the signal output circuit are shown. Referring to Figure 2, in a first alternate embodiment, a signal output circuit 340 includes a digital-to-analog converter (DAC) 341 receiving the processed digital IF signal. The output terminal of DAC 341 is coupled directly to a first driver 343 providing a first output signal being the video baseband signal (CVBS) for analog television and a second driver 344 providing the DTV low-IF signal for digital television. Signal output circuit 340 eliminates the low pass filter that is used in signal output circuit 140 of Figure 1. By providing DAC 341 with increased sample frequency, the low pass filter can be eliminated and signal output circuit 340 can be simplified as compared to signal output circuit 140. In signal output circuit 340, a DAC 345 coupled to a third driver 346 provides the audio baseband signal for analog television. Drivers 343 and 346 are single-ended drivers while driver 344 is a differential output driver.

[0033] In a second alternate embodiment, a signal output circuit 440 includes a digital-to-analog converter (DAC) 441 receiving the processed digital IF signal. The output terminal of DAC 441 is coupled directly to a first driver 443. DAC 441 and first driver 443 form the output signal path for the video baseband signals (CVBS) for analog television. A DAC 445 and a driver 446 form the output signal path for the audio baseband signals for analog television. For the digital television signals, signal output circuit 440 includes a serializer 442 for converting the processed digital IF signal from the DSP circuit into a serial digital data stream. In this manner, the digital signals for digital television can be provided to a digital demodulator through a serial digital interface. In signal output circuit 440, the serial digital data stream is coupled to a second driver 444 which is a differential output driver. In one embodiment, driver 444 is a low voltage differential signaling (LVDS) driver providing the DTV low-IF signal as low voltage differential signals.

[0034] In a third alternate embodiment, a signal output circuit 540 includes a first serializer 541 and a second serializer 542 so that the video signals from the signal output circuit are provided as serial digital interfaces. In this embodiment, first serializer 541 receives the processed digital IF signal and provides a serial digital data stream to a first driver 543. Driver 543 is a differential output driver and drives the serial digital data stream onto an output terminal 504. Serializer 542 and driver 544 form a parallel data path providing a serial digital data stream on an output terminal 506. The serial digital data on output terminal 504 can be coupled to a decoder circuit for decoding into video signals for analog

television. An analog-to-digital converter may be included in the decoder circuit to convert the serial digital data into an analog format. The serial digital data on output terminal 506 can be coupled to a digital demodulator and a decoder for demodulating and decoding the digital television signals. A DAC 545 and a driver 546 form the output signal path for the audio baseband signals for analog television.

[0035] In the signal output circuits described above, the signal output circuits are configured to provide separate output signals for the analog television signal and the digital television signal. In a fourth alternate embodiment, a signal output circuit 640 includes a single serializer 641 coupled to a driver 642 providing a serial digital data stream on a single output terminal 604. In the present embodiment, driver 642 is a differential output drive and output terminal 604 is a differential output terminal including two signal ports. A DAC 645 and a driver 646 form the output signal path for the audio baseband signals for analog television.

[0036] In signal output circuit 640, one output signal in differential format is provided on output terminal 607. The single serial digital data stream can be coupled through a serial digital interface to a demodulator circuit for demodulating the digital television signal or to a decoder circuit for decoding analog television signal. Alternately, the single serial digital data stream from signal output circuit 640 can be coupled to an integrated circuit incorporating both the digital demodulator circuit and the analog decoding circuit. In that case, the single output terminal 607 can be coupled to a single input terminal of the demodulator/decoder integrated circuit where the

demodulator/decoder integrated circuit provides an output signal for analog television and an output signal for digital television.

[0037] In the embodiments described above with reference to Figure 2, the serializer can implement any types of serial digital interface. For example, the serial digital interface can be an asynchronous interface or a synchronous interface. The serial digital interface can be a bit serial interface or can be implemented according to any known serial digital interface standards, including but not limited to ANSI/SMPTE 259M, ITU-R (CCIR) 601, 656, DVB-ASI (EN 50083-9).

[0038] Finally, in a fifth alternate embodiment, a signal output circuit 740 includes a DAC 741 receiving the processed digital IF signal. DAC 741 is coupled to a low-pass filter 742. The filtered analog output signal is provided to a first driver 743 and a second driver 744. Low-pass filter 742 is optional and is not needed when DAC 741 has a high sampling rate. A DAC 745 and a third driver 746 form the output signal path for the audio baseband signals for analog television. In the present configuration, the first, second and third drivers share a first output terminal 708 and a second output terminal 709. Because of the sharing of the output terminals, drivers 743, 744 and 746 are tristate drivers and can be selectively turned off so that only one driver drives the output terminal at a time. In this manner, the pin count for the dual-format television receiver is reduced while the receiver can still provide video/audio signals for either the analog or the digital television format. Specifically, first driver 743, being a single-ended driver, drives video baseband signals (CVBS) onto first output terminal

708. Third driver 746, being a single-ended driver, drives audio baseband signals for analog television onto second output terminal 709. When the analog video and audio television signals are to be displayed, driver 744 is turned off. Alternate, second driver 744, being a differential output driver, drives the differential DTV low-IF signal onto first and second output terminals 708 and 109. When the digital television signal is to be displayed, drivers 743 and 746 are turned off.

[0039] In the above embodiments, the signal output circuit generates the audio output signal for analog television using a DAC and a single-ended driver. This configuration is suitable when the sampling rate of the DAC is high enough so that no filtering of the converted analog signal is needed. In other embodiments, a low-pass filter can be added between the DAC and the single-ended driver. In that case, the sampling rate of the DAC can be reduced.

[0040] A salient feature of the dual-format television receiver of the present invention is the use of a single programmable digital signal processing path for processing the received television signal regardless of the television format and standard in which the television signal is transmitted. Furthermore, the receiver provides output signals for the analog or digital television signals simultaneously. The receiver of the present invention thus enables the construction of a dual-format TV receiver system for providing analog and digital television display signals. The receiver can be built as a monolithic integrated circuit providing a single chip solution to the tuner and signal processing function of an analog/digital TV receiver.

[0041] Figure 3A is a block diagram of a dual-format television receiver system employing dual-format television receiver 100 according to one embodiment of the present invention. Referring to Figure 3A, dual-format television receiver system 200 incorporates dual-format television receiver 100 for receiving and processing the incoming RF signal. In the present illustration, receiver 100 incorporates signal output circuit 140 (Figure 1), 340, 440 or 540 (Figure 2). Thus, receiver 100 provides a video baseband signal (CVBS) for analog television, an audio baseband signal (sound IF), and a DTV low-IF signal for digital television. TV receiver system 200 includes the back-end circuits for generating the display signals and the audio playback signals for the television display.

[0042] In the present embodiment, the video baseband signal (CVBS) from receiver 100 is coupled to a decoder circuit 202. Decoder circuit 202 can be implemented as a PAL/SECAM/NTSC decoder circuit. Decoder circuit 202 provides video output signals on an output terminal 204 which can be coupled to a television for display. The sound IF signal from receiver 100 is coupled to a sound decoder circuit 212 to provide the audio output signals on a terminal 214 which can be coupled to a television for playback. Finally, the DTV low-IF signal is coupled to a demodulator circuit 206 for digital demodulation. Typically, digital television signals are modulated in a VSB, QAM or COFDM scheme. Demodulator circuit 206 operates to demodulate the DTV low-IF signal and generates an MPEG data stream as an output signal. The MPEG data stream generated by demodulator circuit 206 is coupled to a MPEG decoder circuit 208 to be decoded into the video and audio signals on an output terminal

210. The video and audio signals can then be provided to a television for display and playback.

[0043] Figure 3A illustrates one embodiment of a dual-format TV receiver system which can incorporate the dual-format television receiver of the present invention. Other embodiments of the TV receiver system are possible. In particular, the configuration of TV receiver system will depend on the configuration of the signal output circuit used by television receiver 100. Figure 3B is a block diagram of a dual-format television receiver system employing television receiver 100 according to an alternate embodiment of the present invention.

[0044] Referring to Figure 3B, TV receiver system 250 includes receiver 100 which incorporates signal output circuit 740 (Figure 2). Thus, receiver 100 includes only two output terminals: a first output terminal 708 and a second output terminal 709. The two output terminals selectively provide the video baseband signals and audio baseband signals for analog television or the differential DTV low-IF signals. First output terminal 708 is coupled to a decoder circuit 252 for decoding analog television signals and to a demodulator circuit 256 for demodulating digital television signals. Demodulator circuit 256 is further coupled to a MPEG decoder circuit 258 to decode the MPEG data stream generated by the demodulator. Second output terminal 709 is coupled to a sound decoder circuit 262 for decoding sound IF signals for analog television. The second output terminal 709 is also coupled to demodulator circuit 256. When digital television signals are being processed by receiver 100, first and second output terminals 708, 709 functions as the differential output terminals providing the differential output signals indicative of

the DTV low-IF signal. TV receiver system 250 can be operated to provide either analog television signal display or digital analog television signal display.

[0045] The above detailed descriptions are provided to illustrate specific embodiments of the present invention and are not intended to be limiting. Numerous modifications and variations within the scope of the present invention are possible. For instance, Figure 2 illustrates various embodiments of the signal output circuit of the dual-format television (TV) receiver of the present invention. However, other embodiments of the signal output circuit are possible and Figure 2 is not intended to limit the configuration of the signal output circuit to those illustrated. As described above, the signal output circuit can provide output signals in either analog or digital format and the output terminals of the signal output circuit can be single-ended or differential output terminals. The present invention is defined by the appended claims.

CLAIMS

We claim:

1. A television receiver comprising:

a frequency conversion circuit for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF), the input RF signal encoding information in one of a plurality of television signal formats;

an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof;

a signal processor for processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal; and

a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals.

2. The television receiver of claim 1, wherein the plurality of television signal formats comprises an analog television format and a digital television format.

3. The television receiver of claim 1, wherein the television receiver is formed as a monolithic integrated circuit.

4. The television receiver of claim 1, wherein the signal output circuit provides a first output signal being a video

baseband signal corresponding to an analog television format and a second output signal being an audio baseband signal corresponding to the analog television format.

5. The television receiver of claim 4, further comprising:
a first decoder circuit coupled to decode the video baseband signal for providing video display signals corresponding to the analog television format; and
a second decoder circuit coupled to decode the audio baseband signal for providing audio signals corresponding to the analog television format.

6. The television receiver of claim 5, wherein the first decoder circuit comprises a PAL/SECAM/NTSC decoder circuit.

7. The television receiver of claim 1, wherein the signal output circuit provides a first output signal and a second output signal corresponding to the digital output signals, the first output signal and the second output signal being differential output signals corresponding to a digital television format.

8. The television receiver of claim 7, further comprising:
a demodulator circuit for demodulating the first output signal and the second output signal according to the television signal format of the input RF signal, the demodulator circuit generating video and audio baseband signals corresponding to the format of the input RF signal; and

a decoder circuit coupled to decode the video and audio baseband signals for providing video and audio display signals corresponding to the digital television format.

9. The television receiver of claim 8, wherein the video and audio baseband signals comprise a MPEG data stream and the decoder circuit comprises a MPEG decoder circuit.

10. The television receiver of claim 1, further comprising:
a bandpass filter coupled to receive the intermediate frequency signal from the frequency conversion circuit and generate a filtered intermediate frequency signal; and
a variable gain amplifier coupled to receive the filtered intermediate frequency signal and provide the amplified, filtered intermediate frequency signal to the analog-to-digital converter.

11. The television receiver of claim 1, wherein the signal output circuit provides output signals in an analog or a digital signal format.

12. The television receiver of claim 1, wherein the signal output circuit comprises one or more output terminals, each of the one or more output terminals of the signal output circuit comprises a single-ended output terminal or a differential output terminal.

13. The television receiver of claim 1, wherein the signal output circuit comprises:

a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;

a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;

a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a second output terminal;

a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a third output terminal,

wherein the first and second output terminals provide signals indicative of video and audio information encoded in the input RF signal and the third output terminal provides signals indicative of audio information encoded in the input RF signal.

14. The television receiver of claim 13, wherein the first driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to an analog television format, the analog output signals being video baseband signals; and the third driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to the analog television format, the analog output signals being audio baseband signals.

15. The television receiver of claim 13, wherein the second driver circuit comprises a differential output driver circuit for driving analog output signals corresponding to a digital television format, the analog output signals being DTV low-IF signals, and wherein the second output terminal comprises a first

differential output terminal and a second differential output terminal.

16. The television receiver of claim 13, wherein the signal output circuit further comprises:

a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.

17. The television receiver of claim 13, wherein the signal output circuit further comprises:

a low pass filter coupled between the second digital-to-analog converter and the third driver circuit, the low pass filter providing low pass filtering function.

18. The television receiver of claim 1, wherein the signal output circuit comprises:

a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;

a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;

a second driver circuit for driving the analog output signals from the first digital-to-analog converter, the second driver circuit comprising a differential output driver circuit having a first differential output terminal and a second differential output terminal, the first differential output terminal being coupled to the first output terminal and the second differential output terminal being coupled to a second output terminal;

a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto the second output terminal,

wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format; and the first output terminal provides video information encoded in the input RF signal and the second output terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format.

19. The television receiver of claim 18, wherein the signal output circuit further comprises:

a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.

20. The television receiver of claim 1, wherein the signal output circuit comprises:

a first serializer circuit coupled to receive the digital output signals from the signal processor and convert the digital output signals to a serial digital data stream;

a first driver circuit comprising a differential output driver for driving the serial digital data stream from the

first serializer onto a first output terminal and a second output terminal;

a first digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a third output terminal,

wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format and provide differential output signal indicative of video information when the input RF signal has an analog television signal format; and the third output terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format.

21. The television receiver of claim 20, wherein the first, second and third output terminals of the signal output circuit are coupled to a demodulator-decoder circuit, the demodulator-decoder circuit demodulating the serial digital data stream when the data stream corresponds to a digital television format and the demodulator-decoder circuit decoding the serial digital data stream when the data stream corresponds to an analog television format.

22. The television receiver of claim 20, wherein the signal output circuit further comprises:

a second digital-to-analog converter coupled to receive the digital output signals from the signal processor and convert the digital output signals to analog output signal; and

a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a fourth output terminal,

wherein the fourth output terminal provides signals indicative of video information encoded in the input RF signal when the input RF signal has an analog television signal format.

23. The television receiver of claim 20, wherein the signal output circuit further comprises:

a second serializer circuit coupled to receive the digital output signals from the signal processor and convert the digital output signals to a serial digital data stream; and

a third driver circuit comprising a differential output driver for driving the serial digital data stream from the second serializer onto a fourth output terminal and a fifth output terminal,

wherein the first and second driver circuits drive the serial digital data stream corresponding to a digital television format and the fourth and fifth driver circuits drive the serial digital data stream corresponding to an analog television format.

24. The television receiver of claim 1, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate

frequency signal, each of the plurality of finite impulse response corresponding to a format of the input RF signal.

25. The television receiver of claim 24, wherein the plurality of finite impulse response filters are stored in a memory, and the signal processor indexes the memory to retrieve one of the plurality of finite impulse response filters.

26. The television receiver of claim 24, wherein the signal processor comprises a first computing unit and a second computing unit, the first computing unit processing a real part of the finite impulse response filter operation while the second computing unit processing an imaginary part of the finite impulse response filter operation.

27. The television receiver of claim 24, further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the input RF signal and the signal processor selecting a finite impulse response filter in response to the select signal.

28. The television receiver of claim 27, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user.

29. The television receiver of claim 27, wherein the format/standard selection circuit generates the select signal by detecting carrier signals identifying one of the formats of the input RF signals.

30. The television receiver of claim 1, wherein the input RF signal comprises an RF signal received from terrestrial

broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission.

31. A method for receiving an input RF signal, comprising:
receiving the input RF signal encoding information in one of a plurality of television signal formats;
converting the input RF signal to an intermediate frequency signal having an intermediate frequency;
digitizing the intermediate frequency signal at a sampling frequency;
processing the digitized signals in accordance with the format of the input RF signal and generating digital output signals indicative of information encoded in the input RF signal; and
providing one or more output signals corresponding to the digital output signal at one or more output terminals.

32. The method of claim 31, wherein the plurality of formats comprise an analog television format and a digital television format.

33. The method of claim 31, wherein the processing the digital signals is performed in response to a select signal indicative of the format of the input RF signal.

34. The method of claim 33, further comprising:
generating the select signal by detecting carrier signals in the input RF signal identifying the format of the input RF signal.

ABSTRACT OF THE DISCLOSURE

A television receiver includes a frequency conversion circuit, an analog-to-digital converter, a signal processor, and a signal output circuit. The frequency conversion circuit receives an input RF signal in one of several television signal formats and converts the input RF signal to an intermediate frequency signal. The analog-to-digital converter samples the intermediate frequency signal and generates a digital representation thereof. The signal processor processes the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal and generates digital output signals indicative of information encoded in the input RF signal. Finally, the signal output circuit receives the digital output signals from the signal processor and provides one or more output signals corresponding to the digital output signals. The signal output circuit can be configured to provide output signals corresponding to an analog television format or a digital television format or both.

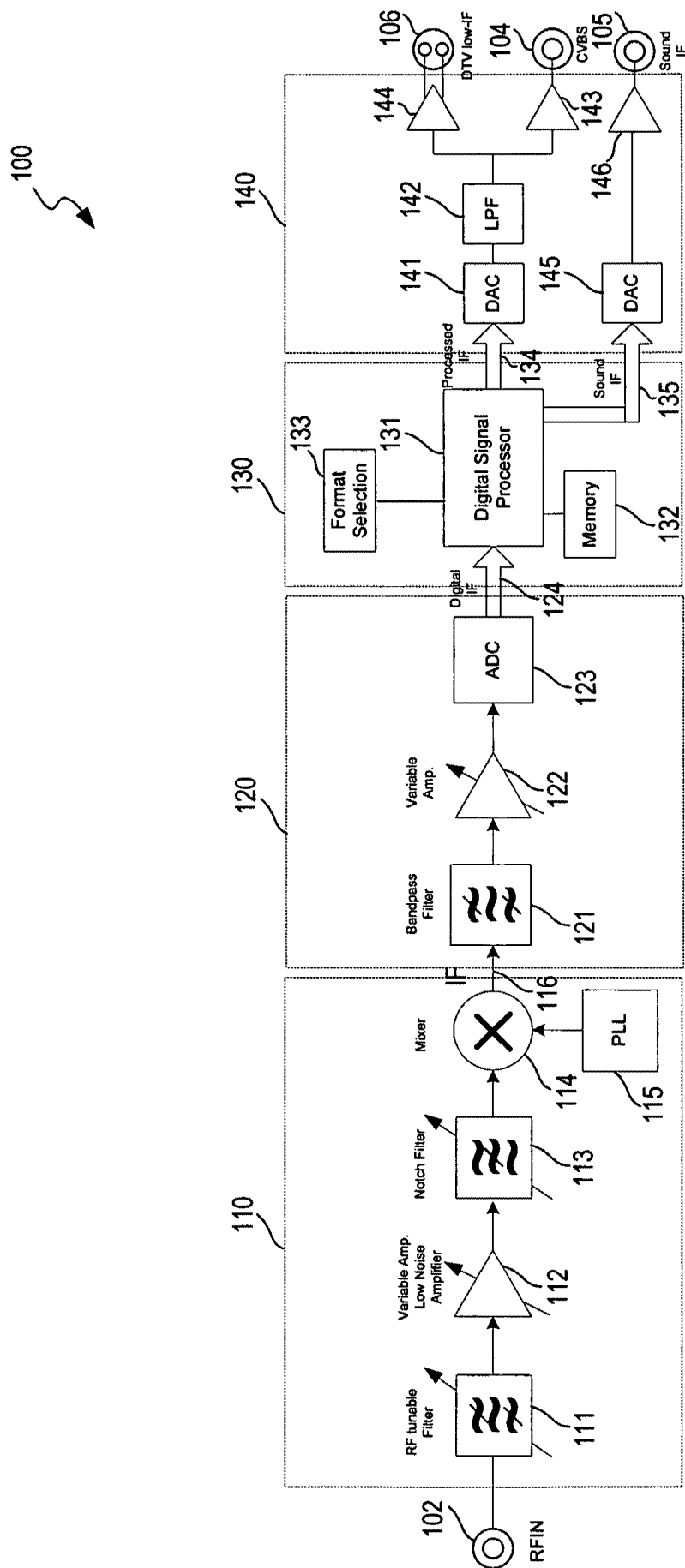


Figure 1

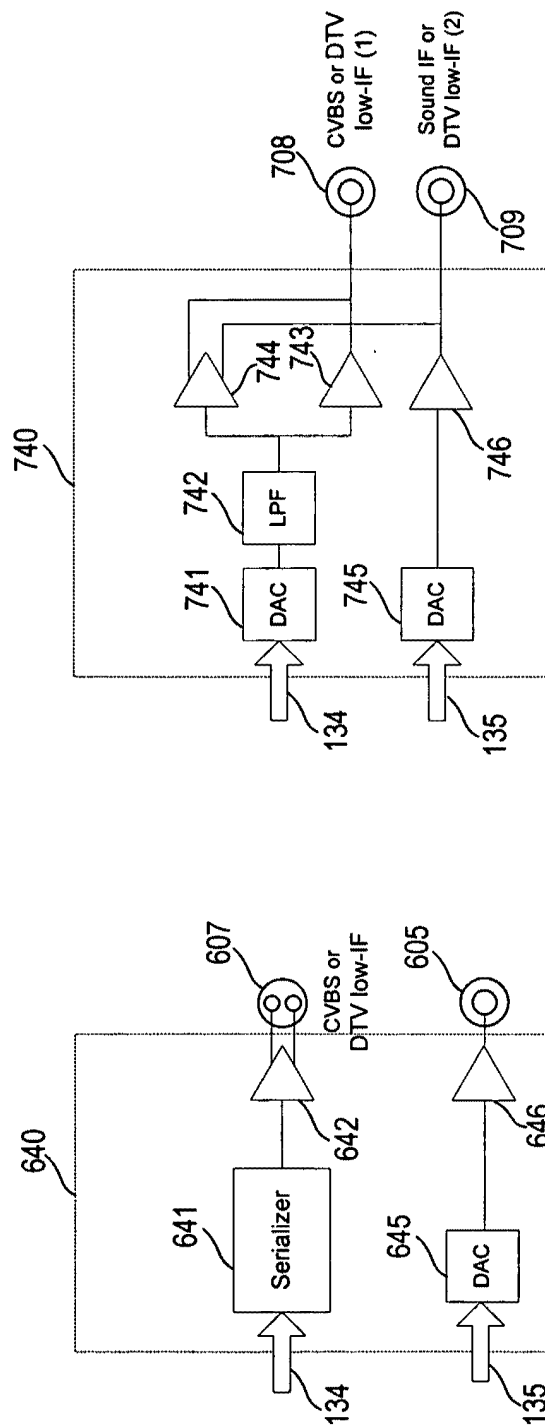
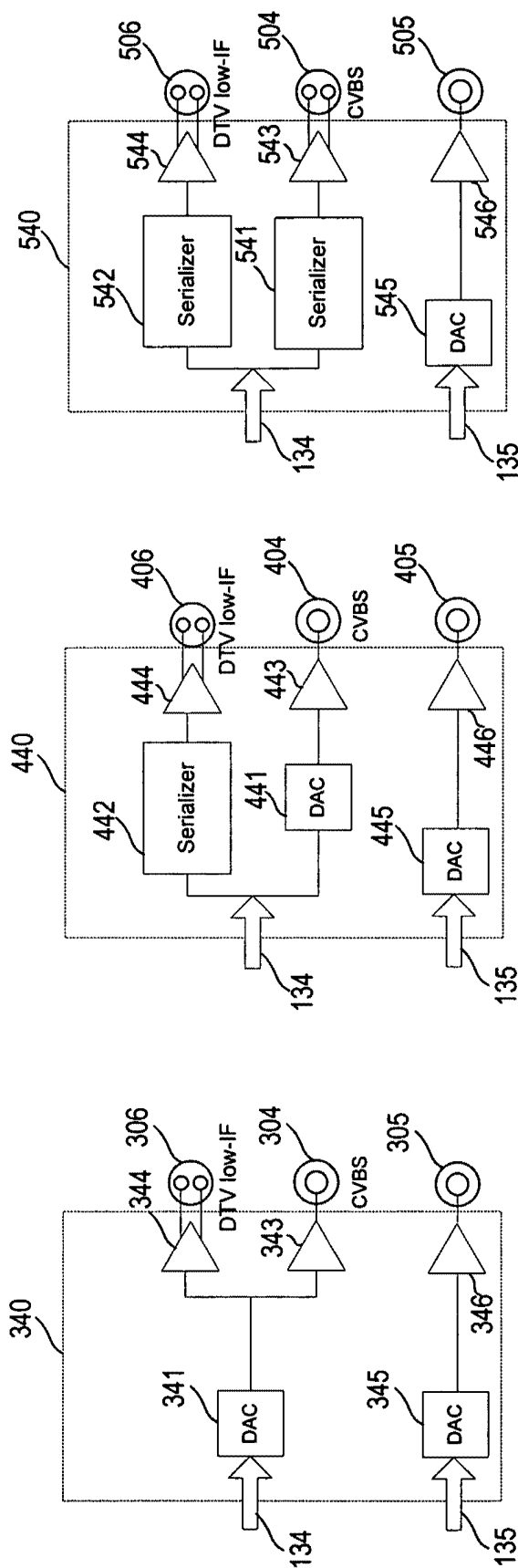


Figure 2

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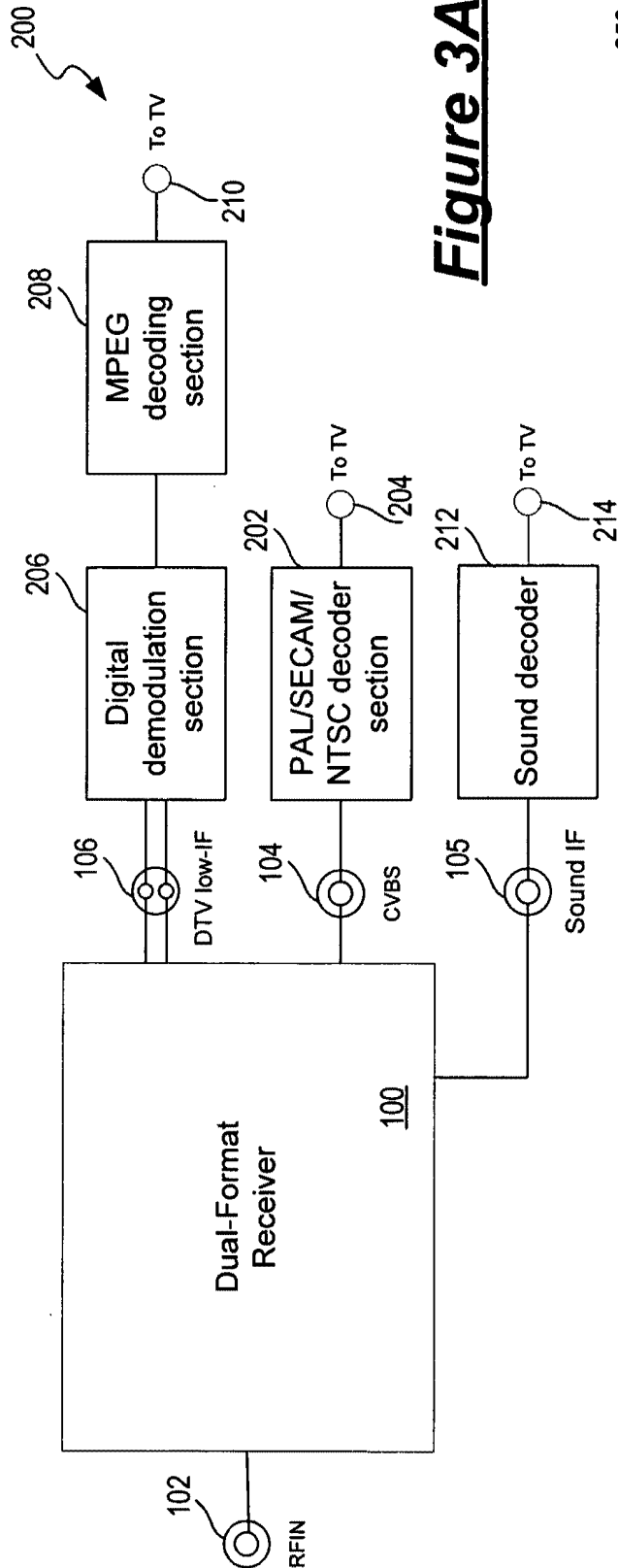


Figure 3A

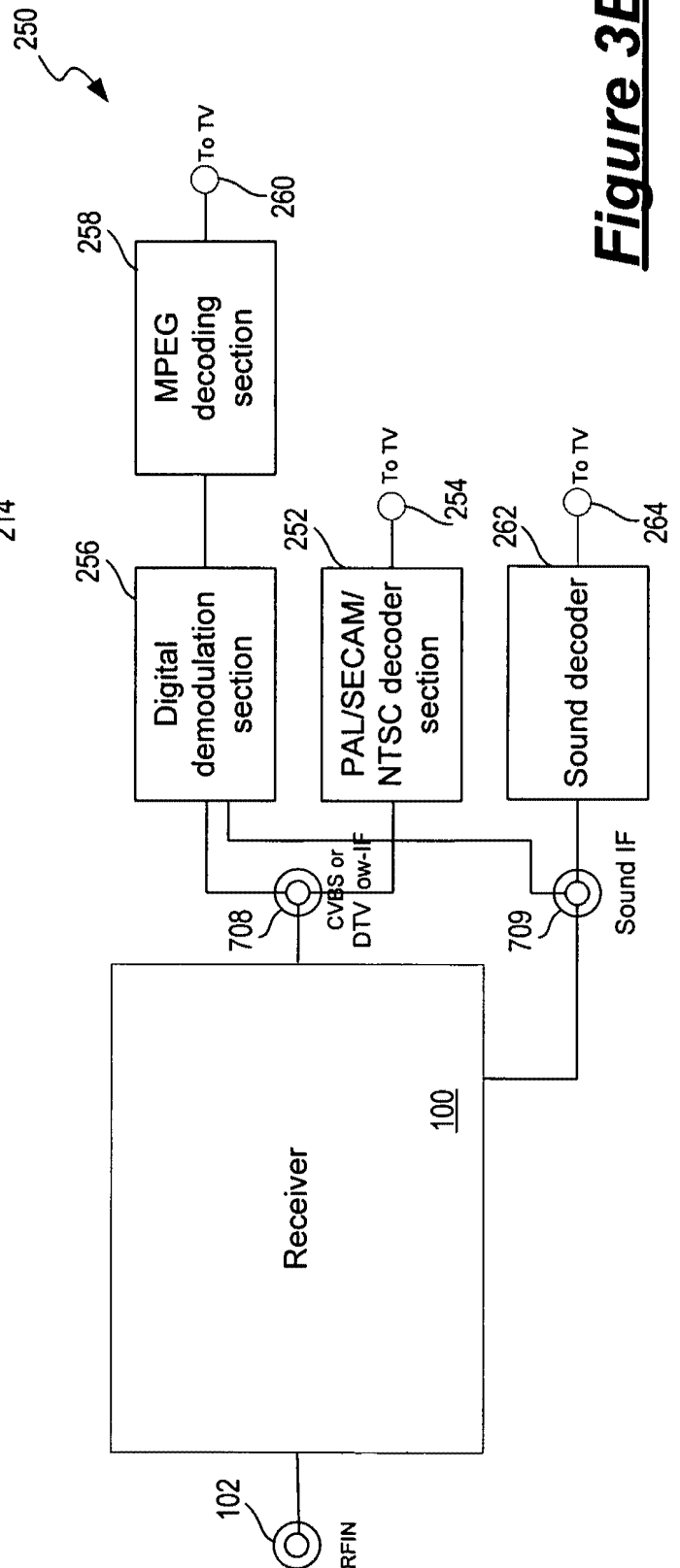


Figure 3B

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As a below named inventor, I hereby declare that:

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Television Receiver for Digital and Analog Television Signals

which (check) ☒ is attached hereto.
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☐ was filed on _____ as Application Serial No.
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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Inventor's Signature: 

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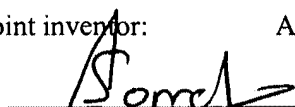
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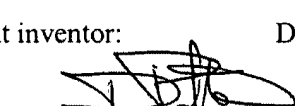
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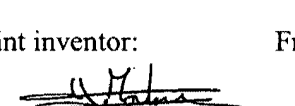
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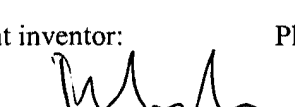
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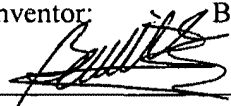
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Full name of seventh joint inventor: Benito Carnero

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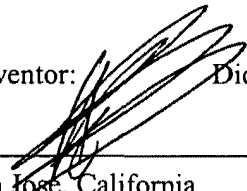
06/30/2004

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06/30/04

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Citizenship: Swiss

PATENT APPLICATION SERIAL NO. _____

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FEE RECORD SHEET

07/09/2004 AOSMAN1 00000006 502226 10884347

01 FC:2001	385.00 DA
02 FC:2202	126.00 DA

PTO-1556
(5/87)

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

10884347

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

TOTAL CLAIMS	34	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	34 minus 20 =	* 14
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

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(Column 1) (Column 2) (Column 3)

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+145=	
TOTAL	511

RATE	FEE
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TOTAL	

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TOTAL	
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RATE	ADDITIONAL FEE
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Serial No.:	10/884,347
Docket:	XCE-P005
Re:	Rescission of Previous NonPublication Request
Pages:	2 (including cover sheet)

Message:

Re: Applicant(s): Pierre Favrat, Alain-Serge Porret, Dominique Python, Friederich Mommers, Richard P. Perring, Philippe Duc, Benito Camero, Didier Margairaz
Assignee: Xceive Corporation
Title: Television Receiver for Digital and Analog Television Signals
Serial No.: 10/884,347
Examiner: Not yet known
Docket No.: XCE-P005
Filed: July 1, 2004
Group Art Unit: 2614

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Application Number	10/884,347
Filing Date	July 1, 2004
First Named Inventor	Pierre Favrat
Title	Television Receiver for Digital and Analog Television Signals
Atty Docket Number	XCE-P005
Group Art Unit	2614
Examiner	Not yet known

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10/884,347	07/01/2004	Pierre Favrat	XCE-P005

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Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 01/05/2006.

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If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

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LFW
Brian D. Ogonowsky
Carmen C. Cook
David C. Hsia
Rachel V. Leiterman



September 6, 2005

Mail Stop Amendment
Commissioner for Patents
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Re: Applicant(s): Pierre Favrat, Alain-Serge Porret, Dominique Python, Friederich Mombers,
Richard P. Perring, Philippe Duc, Benito Carnero, Didier Margairaz
Assignee: Xceive Corporation
Title: Television Receiver for Digital and Analog Television Signals
Serial No.: 10/884,347
Examiner: John W. Miller
Docket No.: XCE-P005
Filed: July 1, 2004
Group Art Unit: 2614

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- (1) Return Receipt Postcard;
- (2) This Transmittal Letter;
- (3) Information Disclosure Statement (1 page);
- (4) Forms PTO/SB/08A and PTO/SB/08B citing 5 references;
- (5) Two (2) Cited References;
- (6) Copies of the cited US Patent documents are not enclosed as the requirement under 37 CFR 1.98 (a)(2)(i) is waived.

- ☒ No additional fee is required.
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☐	Please charge our Deposit Account No. 502226 in the amount of	\$	0.00
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Carmen C. Cook 9/6/05
Attorney for Applicant(s) Date

Respectfully submitted,

Carmen C. Cook
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Attorney for Applicant(s)
Reg. No. 42,433

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant(s): Pierre Favrat, Alain-Serge Porret, Dominique Python, Friederich Mombers, Richard P. Perring, Philippe Duc, Benito Carnero, Didier Margairaz

Assignee: Xceive Corporation

Title: Television Receiver for Digital and Analog Television Signals

Serial No.: 10/884,347

Filing Date: July 1, 2004

Examiner: John W. Miller

Group Art Unit: 2614

Docket No.: XCE-P005

San Jose, California
September 6, 2005

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**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)**

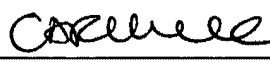
Dear Sir:

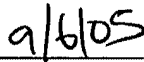
Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the document listed on the accompanying forms PTO/SB/08A and PTO/SB/08B are called to the attention of the Examiner for the above patent application. Copies of the cited foreign patent documents are enclosed. Copies of the cited US Patent documents are not enclosed as the requirement under 37 CFR 1.98 (a)(2)(i) is waived.

Citation of this document shall not be construed as:

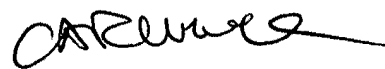
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Attorney for Applicant(s)

 9/6/05
Date

Respectfully submitted,



Carmen C. Cook
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Sheet	1	of	2
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Application Number	10/884,347
Filing Date	July 1, 2004
First Named Inventor	Pierre Favrat
Art Unit	2614
Examiner Name	John W. Miller
Attorney Docket Number	XCE-P005

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				
		EP 0 516 216 A2	5-19-1992	N. V. Philips		

Date Considered

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 2 of 2	Application Number	10/884,347
	Filing Date	July 1, 2004
	First Named Inventor	Pierre Favrat
	Art Unit	2614
	Examiner Name	John W. Miller
	Attorney Docket Number	XCE-P005

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		International Search Report including written opinion, 11 pages.	

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NL-5656 AA Eindhoven(NL)**(54) **Echo cancellation system.**

(57) A circuit architecture suitable for use in a television receiver which effectively performs a ghost or echo cancellation procedure on post-echo components and pre-echo components occurring within the transmission channel. The apparatus features a filter circuit architecture which can be configured under programmed control so as to partition groups of its filter sections to form IIR filters and FIR filters. The filter architecture is suitable for use in multi-circuit configurations and can be used with clustering algorithms to increase the efficiency and optimize the use of the available circuit architecture.

EP 0 516 216 A2

The invention relates to an echo cancellation system in which an information signal comprising a ghost cancellation reference (GCR) signal is received from a transmission path having a distortion characteristic which adds at least one echo component to the information signal.

In 1979 the IEEE published an article which has become a basic reference in the field of television echo (or "ghost") elimination. The article is entitled "A Tutorial On Ghost Cancellation In Television Systems" and was written by Walter Ciciora, Gary Sgrignoli and William Thomas and it is incorporated by reference herein.

Although the Ciciora article described the fundamental principles, apparatus and algorithms applicable to ghost cancellation, the state of the art has only recently progressed to the point of providing practical ways to implement and improve these basic concepts.

The European Patent Application EP-A-0,417,861 (PHA 21.520) provides an example of a signal processor architecture which can be programmed to perform varied filter and other complex digital processing operations utilizing programmed sequences of coefficients and control words. The non-prepublished European Patent Application EP-A-0,450,720 (PHJ 90.006) describes an echo cancellation apparatus which can effectively be implemented with the instant invention.

There are two main steps to the echo cancellation process. First the characteristics of the communications channel (which include the echo artifacts, if any) must be determined at the receiver. Once the channel characteristics are calculated, filters are used to implement the inverse channel to perform the echo cancellation. Because the channel characteristics may include more than one type of echo, each of which is preferably processed differently, a need exists for a circuit architecture, which among other things, provides the ability to programmably optimize a desired filter architecture for the derived channel characteristics with the speed necessary to be effective in a real time communications system. It is therefore an object of the invention, to provide a circuit architecture which lends itself to rapid filter array configuration under programmed control.

A received video signal contains echoes which are comprised of superimposed copies of the originally transmitted signal, which have different delay times and amplitudes. The strongest signal component represents the originally transmitted, or "main" signal component. Looking in the time domain, any copy component occurring before the main signal component is called a "pre-echo" component and any copy components occurring after the main signal component is called a "post-echo" component.

An infinite impulse response (IIR) filter is inherently causal in nature and therefore cannot be used to cancel pre-echoes. An IIR filter can, however, effectively be used to substantially cancel post-echoes.

A finite impulse response (FIR) filter, can be both causal and non-causal. The non-causality allows cancellation of pre-echoes. An FIR filter however, cannot perform ideally unless it is of infinite length. A practical (i.e. finite length) FIR filter will therefore only suppress, but not completely cancel, the pre-echoes. The longer the FIR filter however, the better the pre-echo will be suppressed. A practical echo cancellation circuit should include therefore, an FIR filter to suppress the pre-echoes followed by an IIR filter to suppress the remaining post-echoes. It is therefore another object of the invention to provide an echo cancellation circuit which includes both IIR and FIR filters for effective cancellation of both post-echoes and pre-echoes.

The bandwidth of a standard television channel, for example an NTSC channel, is about 4.2 MHz. Any digital processing therefore has to be done at a rate of 8.4 MHz or more in order to meet the Nyquist sampling criterion. Often the processing of composite baseband NTSC signals is done at a 14.32 MHz rate, which is four times the frequency of the color subcarrier. All echoes, for the most part, fall in a range of -3.5 μ s to + 45 μ s with respect to the main signal component in the time domain. For third order cancellation of pre-echoes therefore, the FIR filter should span about 10.5 μ s and the IIR filter should span about 45 μ s. At the 14.32 MHz sample rate for example, this would require the FIR filter to have 150 taps and the IIR filter 645 taps. These would be large and expensive filters. Fortunately, there is a tendency for the dispersed echo components to "cluster" and this property permits the design and use of filters (known as "sparse" filters) which do not require filters at every tap. Since echoes are dispersive, several taps are required to cancel them. Echoes with a phase shift in the RF domain, and echoes that do not exactly coincide with sample moments, also require multiple taps to be cancelled effectively. Tailing advantage of the tendency of the dispersed echoes to cluster, each echo can be cancelled by a cluster of filter taps. It is therefore another object of the invention to provide an architecture suitable for the implementation of sparse filters.

The instant invention comprises a circuit architecture which is suitable for use as an echo (ghost) cancellation circuit in conjunction with, or as part of, a television receiver. Principal aspects of the invention are set out in Claims 1, 5 and 7, while advantageous embodiments are set out in the subclaims.

One feature of the circuit architecture of the invention, is that it consists of a number of filter taps and a number of programmable delay lines which are assigned under programmed control.

Still another feature of the circuit architecture is that the taps can be clustered and positioned in time, to coincide with an echo component in order to substantially cancel it.

Another feature of the circuit architecture of the invention is that both FIR and IIR filters can be configured and a flexible FIR/IIR boundary can be configured under programmed control.

5 Still another feature of the circuit architecture of the invention is that the FIR/IIR boundary can be changed in real time so that the resources of the architecture are always optimally used.

Still another feature of the invention is that dual input and output busses are provided which enable the various filter sections to be assigned to either an FIR or IIR function.

Yet another feature of the circuit architecture of the invention is a common delay line.

10 Another feature of the circuit architecture of the invention is that it provides means for implementing a scaling algorithm in the calculation of coefficients to allow for greater bit accuracy in the filter processing.

The invention also comprises a method for selecting the coefficients for a clustered filter which is suitable for use with an embodiment of a sparse filter utilizing the circuit architecture of the invention.

These and other objects and aspects of the invention will be more apparent from and elucidated with 15 reference to the embodiments described hereinafter.

In the drawings:

Figure 1 is a block diagram of an echo cancellation subsystem utilizing both FIR and IIR filters;

Figure 2 is a block diagram of a color television receiver comprising an echo cancellation subsystem;

20 Figure 3 is a block diagram of an embodiment of an echo cancellation subsystem comprising the invention;

Figure 4 is a block diagram of the circuit architecture of the echo cancellation filter shown in Figure 3;

Figure 5 is a block diagram of the final adder circuit shown in Figure 4;

Figure 6 is a block diagram of the interface and global register circuit shown in Figure 4;

Figure 7 is a block diagram of the global delay circuit shown in Figure 4;

25 Figure 8 is a block diagram of the select circuit shown in Figure 4;

Figure 9 is a block diagram of a filter stage shown in Figure 4;

Figure 10 is a block diagram of one of the taps of the filter stage shown in Figure 9; and

Figure 11 is a block diagram of an embodiment of the filter circuit shown in Figure 4 utilizing two circuit blocks.

30 Because of the complex environment associated with terrestrial television broadcasting, the characteristics associated with echo phenomena can consist of a main signal component, a number of pre-echo signal components and a number of post-echo signal components. Because the number and variety of echo signal components change subject to changes within the communications channel and are therefore not easily predicted, an effective echo cancellation subsystem must be adaptive in nature and must be able to 35 periodically configure itself to meet the specific requirements of the echo pattern.

Figure 1 describes in block diagram form, an echo cancellation subsystem which includes both FIR and IIR filters. The FIR filter 15 is used to cancel pre-echo signal components and close post-echo components and the IIR filter 20 is used to cancel post-echo signal components. Video signals are received and digitized in A/D converter 10 and a ghost cancellation reference signal (GCR), periodically sent (during the vertical 40 blanking interval for example), is extracted and processed by the buffer 30 and processor 25 using an algorithm designed to provide the appropriate inverse channel coefficients to filters 15 and 20. The non-prepublished US Patent US-A-5,047,859 (PHA 21.622) describes a preferred method and apparatus for calculating the appropriate coefficients and is incorporated by reference herein.

Processor 25 is also used to configure the taps of the filter circuits 15 and 20 in order to more 45 efficiently match the clustered nature of the echo signal phenomena.

The analysis of the channel characteristics and the calculation of the necessary filter coefficients takes place each time the apparatus comprising the invention is turned on, each time the channel being received is changed and periodically after the GCR signals from a number of fields of the video signals are received and averaged. This can be every eight fields for example. After the channel coefficients are calculated, a 50 subset of the coefficients is chosen to reflect the clustering of the echo signals. A preferred clustering algorithm is detailed hereinbelow.

Each time the channel characteristics are analyzed, the respective numbers of pre and post-echo components are determined and the filter section resources of the filter circuit of the cancellation subsystem, in accordance with the instant invention, are optimized for maximum cancellation and efficiency 55 by providing configuration data which adapts the subsystem architecture into the required number of FIR and IIR filters.

After the configuration data and the coefficients are determined, they are sent to the filter circuit (as described more completely below).

Figure 2 describes in block diagram form, a color television receiver which includes an echo cancellation subsystem 100. An antenna on CATV signal from input 139 is applied to an RF tuner 140 and subsequently to an IF stage 141. IF stage 141 supplies sound signals to a sound processor 142 and CVBS (video) signals to an echo cancellation subsystem 100. The echo cancellation subsystem applies filtered CVBS signals to a color decoder 143 and to a vertical and horizontal deflection and high voltage circuit 144. Outputs of the decoder 143 and the circuit 144 are coupled to a color picture tube 145.

Figure 3 is a block diagram of a preferred embodiment of the echo cancellation subsystem 100 shown in Figure 2. As described in connection with Figure 3, a color baseband video signal including a periodic GCR signal is provided to buffer 151 from RF/IF demodulation stages 140 and 141 shown in Figure 2. Sync signals from the video signal are processed in known fashion by PLL 158 to provide a sampling clock signal for A/D converter 10 which receives the clamped and low pass filtered analog video signal from clamp and LPF circuits 153 and 154. An echo cancellation filter circuit 200 having an architecture in accordance with the invention, and preferably in the form of an integrated circuit, is used to provide the FIR and IIR filter sections. Filter circuit 200 is periodically reloaded with coefficients calculated by processor 25 which can be a microprocessor or digital signal processor (DSP). The algorithms used to derive the coefficients are stored in memory which can be part of the processor 25. The processor also provides control words which configure and implement the functions of the filter circuit 200 as described in more detail below. Processor 25 further receives clock signals from PLL 158 and synchronizing data (odd/even) from sync circuit 160, whose input is coupled to buffer circuit 151. Memory 155 is used to store the GCR during the calculation of the coefficients. Although memory 155 is shown at the output of filter circuit 200, the GCR in its unprocessed form is made available to the processor 25 by periodically bypassing the filter circuit 200. Placing the memory 155 at the filter circuit output allows the processed version of the GCR to be accessible to processor 25 as well. The output of filter circuit 200 is provided to D/A converter 35 and LPF/buffer 156.

Figure 4 is a detailed block diagram of the filter circuit 200 comprising an integrated circuit architecture in accordance with one embodiment of the invention. The filter circuit 200 comprises nine filter sections indicated as Sect 0-8. Each filter section comprises a section configuration register 600, an input select circuit 700 and a filter stage 800 comprising a plurality of taps (e.g. twenty). An interface circuit 900 receives data from processor 25 which includes coefficient data and configuration data, and provides control words and coefficients to the rest of the filter circuit 200. Final adder circuit 400 provides circuit input, output, summation and scaling functions for the filter circuit 200, under the control of control words provided by interface circuit 900. A global delay circuit 500 provides fixed delays for the FIR and IIR inputs as discussed in more detail below.

Filter circuit 200 operates alternatively in two modes under the control of processor 25. The first mode is the configuration mode during which configuration data and coefficients derived by processor 25 are loaded into filter circuit 200, and the second mode is the filter mode which is the normal operating mode in which echo cancellation takes place.

When a device comprising the invention, for example a television receiver, is first turned on, when the channel selector is activated, and periodically (i.e. every eight fields) during the operation of the device, the averaged GCR signal in memory 155 (Figure 3) is processed by processor 25. Coefficients are calculated by the processor 25 together with configuration data determining, among other things, which of the filter sections will be configured to form an FIR filter and which of the filter sections will be configured to form an IIR filter. The setting of time delays for each of the filter stages 200 is also controlled by the derived control data, so as to affect the placement in time of each of the limited number of taps in order to coincide with the pre- and post-echo components generated by the channel disturbances. During the configuration mode, configuration data and the coefficients are loaded into the filter stages. Once this is finished, the filter circuit is switched to the filter mode.

Configuration data as well as coefficients are provided to interface circuit 900 by processor 25 on two busses; an address bus labelled A <2:0> and a data bus labelled DATA <7:0>. A number of other inputs are provided to the interface circuit 900 to provide the necessary communication with other integrated circuits in the subsystem. The purpose of these inputs are summarized as follows:

The READ input specifies if the microprocessor cycle is a read or a write. This input is sampled, for example, at the rising edge of the STROBE signal.

The CS and CHIP-No. inputs are used in conjunction with the signal on one bit of A <2:0> to select one filter circuit 200 in a multi-circuit configuration. The CHIP-No. input is used to differentiate between the main and a cascade filter circuit 200 in multi-circuit implementations, shown for example in Figure 11. The CHIP-No. input is asserted for one of the circuits and deasserted for the other. These inputs are all sampled, for example, on the rising edge of the STROBE signal. A particular filter circuit 200 is selected only if CS is asserted and A <2> is equal to the CHIP-No. of the selected filter circuit. If this chip is selected, then A <1:0>

specifies which internal register of interface circuit 900 is read or written to.

The RESET signal resets the internal state of the chip, and the clock generators. All filter section configuration registers 600 are reset to a known state, and the input clock generator is reset and waits for the first CLK before starting up. All microprocessor requests in progress are aborted and ignored.

The STROBE signal clocks all the signals input to the interface circuit 900 except for RESET. The active edge of this clock is the rising edge, for example.

The configuration and operation of the filter circuit 200 will now be explained in the following example wherein three of the Sections (6-8) are configured to form a FIR filter and six of the Sections (0-5) are configured to form an IIR filter.

FILTER MODE

As shown in Figure 5, the video signal X from A/D converter 10 enters the filter circuit at the input 209 of final adder circuit 400, as a nine bit signed value. One sample is provided each sample clock time as generated by clock 158 (Figure 3). In order to conserve chip real estate the illustrated embodiment processes video input samples as eight bit words. For greater accuracy, it can however utilize a nine-bit sample input. To do so, input signal X is rounded and its range is limited in rounding and limiting circuits 401 and 403 respectively, so as to convert its nine bit signed value to an eight bit signed value. The eight bit value is then provided at output 211 and designated as a. Signal a is fed to global delay line 500 (Figure 4) shown in more detail in Figure 7.

In Figure 7, FIR delay line 511 processes signal a and provides two outputs, one being signal a with no delay, and one being a delayed version of signal a having a fixed delay of 64 sample times. The zero delay output appears on the first eight bits (203a) of bus 203 and the delayed output appears on the last eight bits (203b) of bus 203.

As shown in Figure 8, the delayed and non-delayed FIR input signals are provided to multiplexer 705 of input select circuit 700 (Figure 4). As discussed in more detail below, control word e comprises twelve control bits provided by the interface circuit 900 (Figure 4), to each section configuration register 600 (Figure 4). One control bit of control word e selects one of the two FIR input signals to multiplexer 705 to provide either a delayed or an undelayed signal a to a first input of multiplexer 707. The second input to multiplexer 707 is the IIR signal output (as discussed in more detail below).

As shown in Figure 4, each input select circuit 700 provides an input signal d to its respective filter stage 800. Signal d is a delayed version of the output of multiplexer 707 (Figure 8) which is selected by another control bit of control word e. The output of multiplexer 707 is coupled to local delay line 704 which provides an additional delay of from zero to 63 samples, selected by six control bits of control word e. Output signal d of local delay line 704 therefore is the sample X which has been rounded and limited and provided with a total amount of delay determined by the fixed delay provided by global delay line 500 (Figs. 4,7) and a programmable delay provided by delay line 704 (Figure 8). The effective delay for each of the filter sections 6, 7 and 8 may be different.

As stated above, the instant invention can be configured to perform both FIR and IIR filter functions. The boundary between the respective groups of filter sections, i.e. between section 5 and section 6 in the instant example is set by choosing a zero value as a sum or coefficient input 806 to the first filter stage (tap 0) of the 20 filter stages 810 of filter section 6 as shown in Figure 9. The filter stages 810 filter the samples d supplied from delay 704 of Figure 8, as shown in more detail in Figure 10 described below. Multiplexer 805 has two inputs. The first input 801 is either a coefficient provided during the configuration load mode or the cascade output 807 from the preceding filter section. The second input 811 to multiplexer 805 is a zero value. The output of multiplexer 805 is selected by another control bit of control word e.

In the instant example, the output of filter section 6 provided at its cascade/coefficient output 807 is coupled to cascade/coefficient input 801 of section 7 and the cascade/coefficient output 807 of filter section 7 is coupled to the cascade/coefficient input 801 of section 8.

The sum or coefficient output 812 of the last filter stage of filter section 6 is provided to the cascade/coefficient output 807 and to gates 813 and 814. Gate 813, when enabled by another control bit of control word e, passes the output to the FIR Sum bus 207. Sections 6, 7 and 8 thus form a continuous FIR filter with a total of 60 taps (20 each from sections 6, 7 and 8).

As shown in Figure 5, FIR Sum bus 207 is coupled to sealer 407 of final adder 400. During the sampling of the video signal, known scaling techniques can be used to increase the effective bit accuracy of the coefficients. Scaler 407, under the control of control word g, provides a compensating factor (as described in more detail below) to restore each sample to its proper level. Scaler 420 performs the same function on the IIR sum bus signal under the control of control word g.

The sealer 407 can be simple barrel shifter which functions as a multiplier. Its setting depends on the level of actual coefficients. The output of scaler 407 can then be added to a sealed version of the signal provided by the IIR Sum bus 205 (Figure 4) and the output of unity gain delay 405, in summer 408. The output of summer 408 is then rounded off and limited in circuits 409 and 410 respectively and provided as one input to multiplexer 415 which provides the nine bit output of filter circuit 200, Y (8:0). If in rounding out the signal the result is out of range this condition will be indicated by asserting a chip signal overflow flag OVERFL.

In Figure 4, filter sections 0 through 5 are configured to form an IIR filter. The output signal from summer 408 (Figure 5) is rounded off and limited in circuits 421 and 422 to form signal b which is coupled to IIR delay line 515 (Figure 7) of global delay circuit 500. Signal b, as provided by summer 408, provides the feedback loop necessary for an IIR filter.

As shown in Figure 7, delay line 515 provides eight fixed delay versions of signal b on bus 201, each having a different delay time from 0 to 448 samples. Bus 201 which provides the IIR input, is coupled to multiplexer 717 (Figure 8) of each input select circuit 700.

In the instant example, sections 0 through 5 (Figure 4) are arranged as an IIR filter. This, in effect, causes a clustering of the taps wherein the separation of the clusters will be determined by the difference in the effective delay values. The choice of delay is made by multiplexer 717 under the control of three control bits of control word e.

As shown in Figure 9, as in the case for the FIR filter sections, the first of the IIR sections, i.e. filter section 0, must have a zero value as a sum or coefficient input 806 to its first filter stage 810 (tap 0). As described above with respect to filter section 6 of the FIR filter, multiplexer 805 selects either the cascade/coefficient input 801 or a zero value 811, as the sum or coefficient input to tap 0 filter stage 810 of filter section 0, in response to a control bit of control word e. The sum or coefficient output 812 of filter section 5 is coupled to cascade coefficient output 807 and to gates 813 and 814. Gate 814, when enabled by another control bit of control word e, passes the output of filter section 5 to the IIR sum bus 205. The sum or coefficient output of filter section 0 feeds the sum or coefficient input of filter section 1 and so on in order to form, in this example, an IIR filter with 120 taps.

As shown in Figure 5, the IIR sum bus 205 is coupled to scaler 420 of the final adder 400 where it is sealed and added to the output of the FIR sealer 407 and the output of unity gain delay 405 in summer 408.

An input unity gain delay 405 consists of a delay which enables the setting of a position of a coefficient of value one. This position is considered the so-called unity gain tap in the FIR. The unity gain tap allows the use of a large scaler factor at the output of the FIR sum bus by removing the only large coefficient in the FIR filter. Multiplexer 415, under the control of a control bit of control word g, can be used to output an unprocessed but delayed version of the input video signal from input unity gain delay 405.

CONFIGURATION MODE

As shown in Figure 4 and described above, interface circuit 900 provides configuration data to each section configuration register 600 on bus 918 as well as to the final adder 400. It also provides coefficient data to each of the filter stages 800 on bus 915. Figure 6 shows a more detailed version of interface circuit 900 consisting of a plurality of registers providing 8 bits of coefficient data, 12 bits of configuration data and 4 bits of address data.

As viewed by a programmer, there are two levels of registers in the filter circuit 200. The first level consists of three registers 902, 904 and 906 which have respectively register addresses 0, 1 and 2. A fourth register 908 is also provided in the illustrated embodiment but is, at present, unused. The address provided at the A (2:0) port of interface circuit 900 determines which of these registers the data provided on the data port DATA (7:0) are written into. In a multi-circuit system such as the one illustrated in Figure 11, one bit (A (2)) selects the filter circuit 200, and the remaining bits (A (1:0)) selects the register (902, 904, 906 or 908). All registers 902-908 are coupled to a chip interface CIF.

The second level of registers in filter circuit 200 comprises:

- (a) a first group of registers comprising each register 815 present in each of the taps 810 (Figure 10) in each of the filter sections. Each register 815 actually comprises a plurality of holding registers (for example 180) for storing coefficients to be loaded into each tap (as explained in greater detail below);
- (b) a single global configuration register 910 (Figure 6) which is part of the interface circuit 900, which stores the configuration data forming control words h and g; and
- (c) a second group of registers comprising the nine section configuration registers 600, one for each filter section, which store the configuration data forming control word e.

Table I describes the addressing and bit assignment for registers 902 through 908. The registers 902 through 908 each store eight bits of data.

TABLE I

Address A (1:0)	Name	Bits	Usage of bits
0	Coefficient	(7:0)	Signed coefficient values
1	Configuration-Low	(7:0)	Low 8 bits of 12 bit configuration data
2	Configuration-High	(3:0)	Top 4 bits of 12 bit configuration data
	Global/Configuration Register Address	(7:4)	Internal address for selecting global or configuration register ("see Table II)
3	Test		Miscellaneous use

Register 902 holds eight bits of coefficient data provided to each of the filter stages 800 (Figure 4) as a coefficient input 815 on bus 915. Coefficient data is made available to interface circuit 900 at its DATA (7:0) port, from processor 25. The address provided at A (2:0) by the processor 25, selects register 902 as the destination for the coefficient data.

Configuration data is provided to eight bit registers 904 and register 906 from processor 25 through the DATA (7:0) port. Register 904 holds eight bits of configuration data and register 906 holds four bits of configuration data and an additional four address bits to select which of the second group of section coefficient registers 600 or the global register 910 receives the twelve bits of configuration data as described in Table II.

TABLE II

(7:4)	Selected Configuration Register
0	Filter section 0 configuration register
1	Filter section 1 configuration register
2	Filter section 2 configuration register
3	Filter section 3 configuration register
4	Filter section 4 configuration register
5	Filter section 5 configuration register
6	Filter section 6 configuration register
7	Filter section 7 configuration register
8	Filter section 8 configuration register
9	---- miscellaneous ----
10	---- miscellaneous ----
11	---- miscellaneous ----
12	---- miscellaneous ----
13	---- miscellaneous ----
14	Global configuration register
15	All (0 to 8) section configuration registers

The global register 910 provides control words g and h. Control word g provides the control bits to configure the final adder 400. Control word h, comprising the "md" and "ld-coef" signals, is provided to each of the filter taps 810 (as described below with reference to Figure 10). Control words g and h control the filter circuit functions as described in Table III below.

TABLE III

Bit	Usage	Control Word
<2:0>	FIR scale factor (1/1 to 1/16)	fig. 5-g (FIR scale 407)
<5:3>	IIR scale factor (1/1 to 1/16)	fig. 5-g (IIR scale 420)
<6>	Select bypassed output	fig. 5-g (bypass)
<7>	8-bit filter enable	
<8>	signed samples	
<9>	Load coefficient mode	fig. 10-md }
<10>	Load coefficient strobe	fig. 10-ld-coef} h
<11>	---- miscellaneous----	

Each of the configuration registers 600 provides a separate control word e to its respective filter section 800 thereby setting the mode of operation and value of parameters that are local to each of the filter sections as shown in Table IV.

TABLE IV

Bit	Usage	Control Word e
<5:0>	Input delay value (0-63 samples)	fig. 8 (delay value 704)
<6>	FIR - select global delay source	fig. 8 (fir inp sel.)
<8:6>	IIR-select global delay source	fig. 8(iir inp sel.)
<9>	FIR Enable	fig. 8 (fir/irr.sel.)
<10>	Output Enable	fig. 9 (enable 207 Σ FIR) fig. 9 (enable 205 Σ IIR)
<11>	Enable cascade	Figure 9 (mux 805)

The configuration mode of the filter circuit 200 is activated when a device comprising the circuit (for example a television receiver) is turned on. It also is activated each time the receiver is tuned to a different channel or when the periodic processing in processor 25 of the averaged GCR signal detects a change in the channel characteristics. How often the configuration mode is activated is directly related to the speed at which the processor can determine the channel characteristics and calculate the necessary configuration data and coefficients. One advantage of the invention as embodied in filter circuit 200 is that it can respond very quickly to changes in the channel characteristics determined by the processor 25.

When the receiver is first turned on, the GCR signals carried on a number of fields of the received signal are averaged and compared to a stored version of the transmitted GCR, by processor 25. The processor 25, using techniques known to those skilled in the art, processes and conditions the averaged GCR signal as required by the type of GCR signal being used. The channel characteristics are then determined using time domain analysis algorithms such as those described in the references incorporated herein, or others known in the art, in order to determine the location in time of the pre-echo components and post-echo components present in the received signal. This information determines the allocation of the filter sections in filter circuit 200 to FIR and IIR functions. The processor 25 also calculates the coefficients needed to create an ideal inverse channel characteristic.

Since the number of filter stages available in each filter section is limited, the processor must perform a clustering procedure which apportions the limited number of filter stages by effectively taking advantage of the tendency of the echo components to cluster in time. The procedure can use a preferred clustering algorithm such as the one described below. Other clustering algorithms which can also be used are known to those skilled in the art. The clustering algorithm creates a subset of the calculated coefficients and selects the necessary time delays, implemented in filter circuit 200, to select the filter stages 810 so as to coincide with the clustered echo components.

After the clustering procedure, a sequence of configuration data words including the necessary control words needed to set the FIR/IIR boundary, the scaling parameters (if used by the processor 25 in calculating the coefficients) and the delay parameters, are loaded into filter circuit 200 in order to configure it as required using the information provided in the Tables in conjunction with the example described above. The coefficients are then loaded into filter circuit 200 as follows:

1. A configuration data word is written into each of the section configuration registers 600 setting its Enable Cascade bit (see Table IV). All of the section configuration registers 600 are addressed by providing an address of fifteen on bits (7:4) of register 906 (see Table II). The contents of each section configuration register 600 thereby provides the set bit, i.e. bit eleven of control word e (see Table IV), as a sum select signal to multiplexer 805 to each filter stage 800 thereby connecting the "cas in /coef in" input to the " Σ in/coef in" input of the first filter tap 810 of each filter stage 800 so as to form a pipeline of all of the filter taps (i.e. 180 taps).

2. A configuration data word is written into the global configuration register 910 setting its load Coefficient Mode bit (see Table III). The global configuration register is addressed by providing an address of fourteen on bits (7:4) of register 906 (see Table II). The contents of the global configuration register 910 thereby provides the md (coefficient mode) bit of control word h to each filter tap 810. As shown in Figure 10, when set, the md bit selects the input provided to each multiplier 819. This selection is made in multiplexer 816 which has as one input the video samples provided by d during the filter mode and as another input, a stored zero value which is the input selected by the md bit in the configuration mode. The md bit is also coupled to multiplexer 818 which selects as a clock input to sum register 820, the clock signal from 158 during the filter mode and a "coef clk" signal during the configuration mode. The coef clk signal is used to toggle the coefficients into the pipelined filter stages as described below, and is derived by "ANDing" the STROBE signal provided to interface circuit 900 and a write signal to register 902 (which provides the coefficient data).

3. The coefficients are then sequentially written to register 902 and sequentially fed to the 180 pipelined filter taps 810. For example, a new coefficient is shifted into the filter tap 0 (i.e. tap 0 in filter section 0) when the coefficient register 902 is written to, and all other coefficients are shifted upward. The shifting of coefficients is accomplished by using register 820 in each filter tap which is clocked by the coef clk signal. After all of the coefficients are loaded, the holding register 815 of each filter tap 810 stores the coefficient to be loaded into the multiplier 819 of the respective filter stage. Note that the pipeline of 180 coefficient holding registers 815, needs no internal address select. Repeated writes to register 902 cause the data to move down the pipeline until all coefficients are initialized.

4. A configuration data word is written into the global configuration register 910 setting its Load Coefficient Strobe bit (see Table III). The global configuration register is addressed by providing an address of fourteen on bits (7:4) of register 906 (see Table II). The contents of the global configuration register 910 thereby provides the ld-coef (coefficient strobe) bit of control word h to each filter tap 810. As shown in Figure 10, the ld-coef bit when set, toggles register 815 and thereby provides the stored coefficient to the respective multiplier 819. Adder 817 adds the output of multiplier 819 to the Σ in/coef in signal and applies the sum to sum register 820.

5. A configuration data word is written into the global configuration register 910 resetting the Load Coefficient Strobe bit.

6. A configuration data word is written into the global configuration register 910 resetting the Load Coefficient Mode bit.

7. All of the filter section configuration registers are again loaded with the configuration data to set them to the desired configuration and parameters, as described in step 1.

Figure 11 describes the use of two filter circuits 301 and 302 (which are the same as filter circuit 200) connected in series ("cascaded") in order to create a larger filter circuit 300 with the resulting ability to provide a greater number of filter taps, i.e. 360 instead of 180 and the resulting expanded ability for IIR/FIR allocation and improved echo cancellation. The main circuit 301 of this multi-circuit embodiment has as its X (8:0) input the output from the A/D converter 10. The second circuit 302 has as its X (8:0) input, eight bits (Y (8:1)) of the filter output Y (8:0) and the single bit CASCADE X (0) output of the main circuit 301. The

CASCADE-X <O> output is used to convey rounding information to the cascade chips of multi-circuit implementations.

The CASCADE X <O> output is provided by logic circuit 425 of final adder 400 (Figure 5) of the main circuit 301. Circuit 425 has as inputs, the outputs of rounding circuits 409 and 421. The function of the logic circuit is to determine whether it is necessary to round out the data being transferred to the second circuit 302. This is done according to the following truth table where a 1 indicates that rounding occurred in the respective rounding circuit and a 0 indicates that no rounding was necessary.

	Rounding Circuit		X <O>
	409	421	

	0	0	0
	0	1	1
	1	0	0
	1	1	0

The CASCADE DATA <17:0> bidirectional port of second circuit 302 provides the feedback input to the CASCADE DATA <17:0> bidirectional port of main circuit 301 and the full nine bit Y <8:0> output of main circuit 301 provides the output of the multi-circuit filter circuit.

Clustering Algorithm

A N-taps full FIR filter has the following transfer function:

$$y(n) = \sum_{j=0}^{N-1} c_f(j) x(n - j).$$

As mentioned above, the circuit architecture of the invention can be more efficiently used by exploiting the fact that non-zero coefficients and thus multipliers are only required where there are echoes. This suggests a filter consisting of clusters of taps which can be randomly positioned relative to $C_f(0)$ ("tap zero"). That can be achieved by preceding each cluster of taps with a programmable delay line. The architecture of the invention described above provides the means for providing the necessary delay.

Given C clusters of M taps each (C and M being integers), the transfer function of a clustered FIR filter becomes

$$y(n) = \sum_{p=1}^C \sum_{q=0}^{M-1} Cl_c(p,q) x(n - \Delta_p - q) \quad (1)$$

where Δ_p is the delay achieved by the p-th delay line and $Cl_c(p,q)$ is the q-th coefficient in the p-th cluster. Alternatively, (1) can be written as where

$$y(n) = \sum_{j=0}^{N-1} c2_c(j) x(n - j) \quad (2)$$

$$C2_c(j) = \sum_{p=1}^C \sum_{q=0}^{M-1} Cl_c(p,q) \text{ with } \Delta_p + q = j \quad (3)$$

5

From (3), it follows that when there are no overlapping clusters (i.e. $|\Delta a - \Delta b| \geq M$, for each a,b), each coefficient $C2_c(j)$ corresponds to a single coefficient $Cl_c(p,q)$. When there is overlap however, coefficient $C2_c(j)$ may be the sum of several coefficients $Cl_c(p,q)$. Since the clustered filter will have fewer
 10 taps than the full filter ($CM < N$), it is an approximation of the latter. Finding the best approximation is an optimization problem which can be formalized as follows:

Given: $C_i[0..N-1]$ = coefficients for the full filter.

Wanted: $\Delta_{l..c}$ and $Cl_c(l..C, 0..M-1)$ = delay values and coefficients for the clustered filter, such that

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$$E = \frac{1}{N} \sum_{j=0}^{N-1} e(C_f(j), C2_c(j)) \quad (4)$$

20

is minimum. Here, $e(a,b)$ is some error function of a and b. For example, when $e := (a-b)^2$, (3) gives the Mean Square Error between C_f and $C2_c$.

Solving (4) mathematically is rather difficult. It would require a substantial computation effort, which is not desired in a real time system. The invention provides a practical rather than a mathematical solution,
 25 which combines the benefits of simple computations and excellent performance. Solving (4) means finding the best location for each of the C available clusters. That translates into finding the best values of $\Delta_{l..c}$.

It can be shown that there are

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$$\left[N - \frac{C}{M-1} \right] \quad (5)$$

ways to position C clusters of M taps over a total of N taps ($N > CM$). Since the desired cancellation range for video requires N to be rather large, the number of possible solutions is enormous. When for instance
 35 $N=512$, $C=15$, $M=8$, substitution in (5) shows there are $8 \cdot 10^{26}$ different settings of $\Delta_{l..c}$.

Below we describe a method for approximating the optimum delay settings which can be implemented in processor 25, for example. It has shown to be fast and give good results. The method is described in simplified form by means of pseudo-programming language. It's basic operation is to locate the peaks in C_f and then center the available clusters in Cl_c around these peaks.

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50

55

(M is even)

BEGIN

For j:=1 TO C DO

{do for each cluster j(j=1..C)}

BEGIN

$i_{peak} := \text{index}(\max\{ |C_r[i]| \})$:

{find peak in C_r , i_{peak} is index of peak}

$\Delta_j := i_{peak} - M/2$;

{center cluster j around peak}

IF $\{\Delta_j < 0\}$ THEN $\Delta_j = 0$;

{if cluster j exceeds lower array
boundary, put at boundary}

IF $\{\Delta_j > N-M\}$ THEN $\Delta_j = N-M$

{if cluster j exceeds upper array
boundary, put at boundary}

$C1_c[j, 0..M-1] = C_r[\Delta_j.. \Delta_j + M-1]$:

{copy coefficients from C_r to $C1_c$ }

$C_r[\Delta_j.. \Delta_j + M-1] = 0$;

{mark coefficients in C_r as used}

END

END

The foregoing disclosure and description of the invention is illustrative and explanatory thereof and various changes in the design and configuration, and the algorithms therewith, may be made within the scope of the appended claims without departing from the spirit of the invention.

Claims

1. A digital signal processing apparatus suitable for use as a filter circuit in a device which, after receiving and deriving a plurality of signal samples from a signal transmitted over a transmission path, identifies and substantially removes path induced distortion to said signal, wherein said device comprises a processor means for deriving a set of filter coefficients and a set of configuration control signals related to distortion components of said path induced distortion, said apparatus comprising:

a) first providing means for providing said control words and said coefficients to said apparatus;

b) second providing means for providing said signal samples to said apparatus and for providing processed samples from said apparatus, said second providing means comprising an unprocessed sample input, first and second processed sample inputs, and first and second sample outputs;

c) a plurality of filter sections each comprising:

i. means switchably coupled to said first and second sample outputs, for selecting as filter section input samples, one of said first and second sample outputs under the control of a second control signal;

ii. delay means coupled to said selecting means, for providing a delay to said filter section input samples;

iii. a filter stage comprising a plurality of taps, a first filter input coupled to said delay means for receiving said delayed filter section input samples, a first stage output, a second stage output switchably connected to said first processed sample input under the control of a first control signal, a third stage output switchably coupled to said second processed sample input under the control of a second control signal, and a second filter input switchably coupled to the first stage output of an adjacent filter stage; and

d) means for configuring a first group of said filter sections into a first filter and a second group of said filter sections into a second filter.

2. The apparatus of claim 1, wherein said first filter is an FIR filter and said second filter is an IIR filter.

3. The apparatus of claim 1 wherein said configuring means comprises means for providing a programmable delay to the samples provided by each of said first inputs.

4. The apparatus of claim 1 wherein said second providing means comprises means for coupling said apparatus to a second said apparatus.

5. A television receiver for use in an echo cancellation system in which a television signal comprising a plurality of frames each comprising a GCR signal, is transmitted over a transmission path having a distortion characteristic which adds at least one echo component to said signal, said receiver comprising:

(a) means for receiving said signal;

(b) means for periodically analyzing said GCR and for calculating a plurality of filter coefficients defining the inverse distortion characteristic of said transmission path and a plurality of control signals related to said at least one echo component; and

(c) a filter circuit coupled to said analyzing means, which is periodically provided with said coefficients and control signals and which comprises a plurality of filter sections which are configured, in response to said control signals, into a first filter suitable for substantially cancelling a first type of echo component and a second filter suitable for substantially cancelling a second type of echo component.

6. The receiver of claim 5, wherein said first filter is an FIR filter and said second filter is an IIR filter.

7. A digital signal processing apparatus suitable for use as a filter circuit in an echo cancellation system in which a television signal comprising a GCR signal is transmitted over a transmission path having a distortion characteristic which adds at least one echo component to said signal and comprises means for periodically analyzing said GCR and for calculating a plurality of filter coefficients defining the inverse distortion characteristic of said transmission path and a plurality of control signals related to said at least one echo component, wherein said signal processing apparatus is periodically provided with said coefficients and control signals and comprises a plurality of filter sections which are configured, in response to said control signals, into a first filter suitable for substantially cancelling a first type of echo component and a second filter suitable for substantially cancelling a second type of echo component.

8. The apparatus of Claim 7, wherein said first filter is an FIR filter and said second filter is an IIR filter.

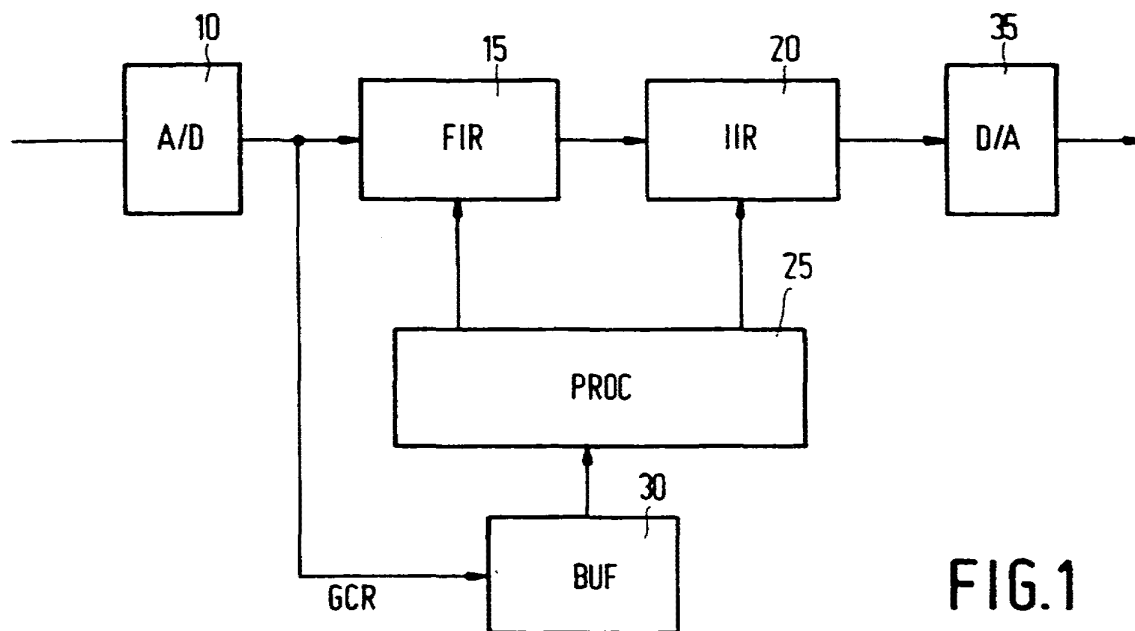


FIG. 1

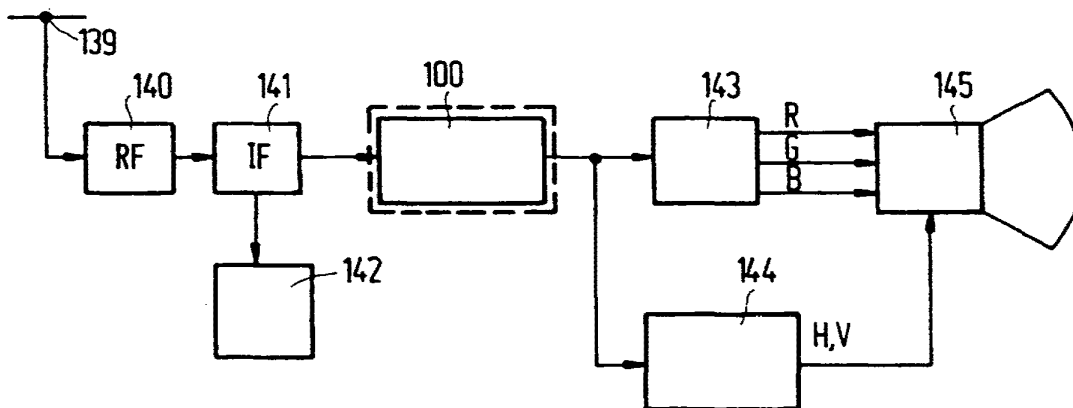


FIG. 2

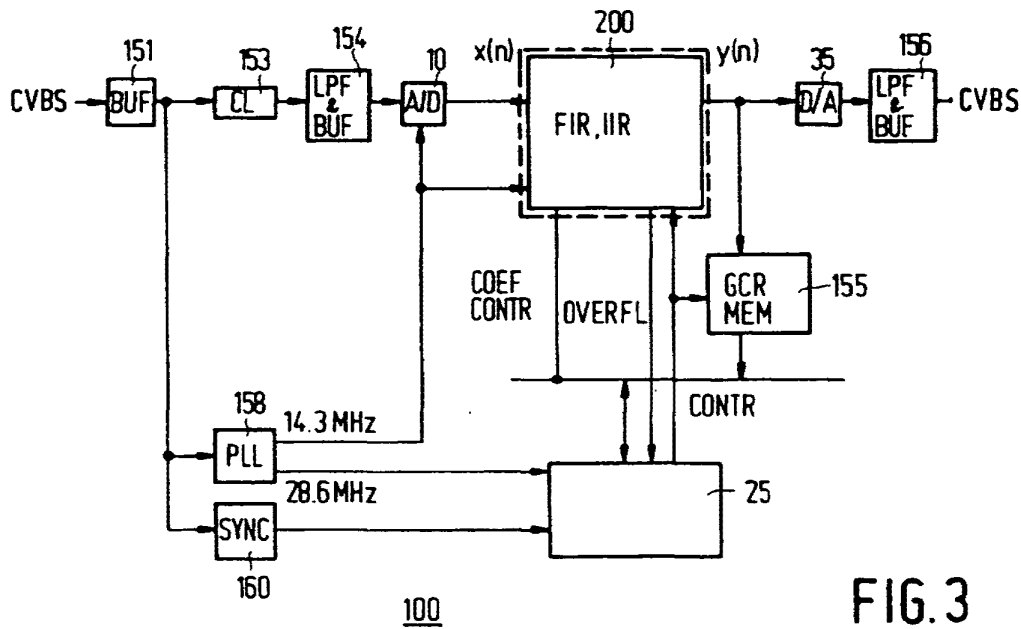


FIG. 3

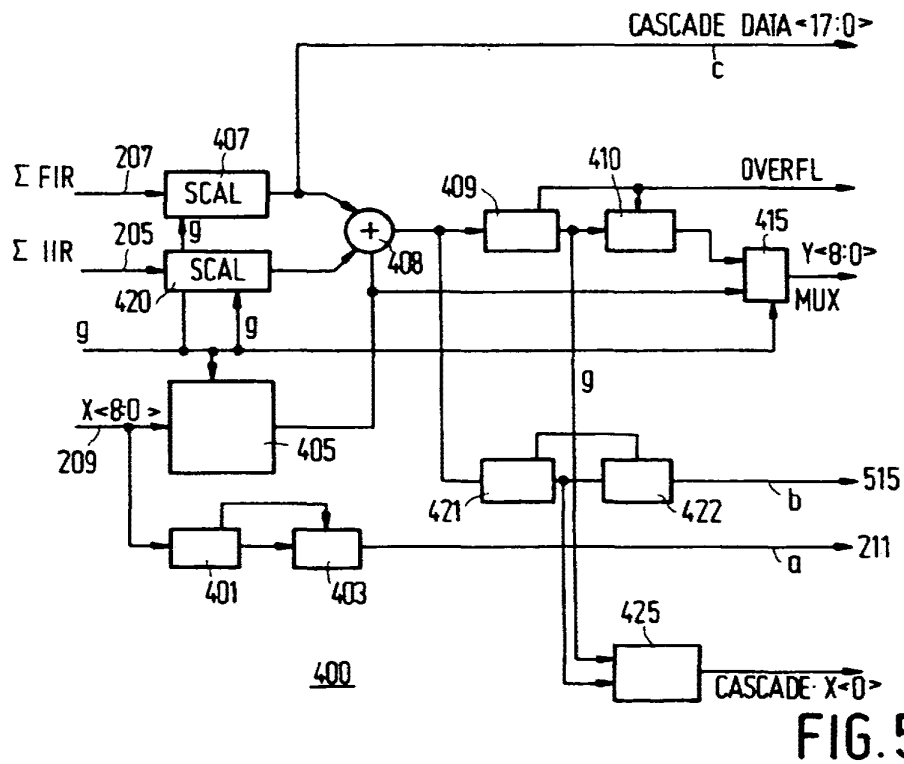
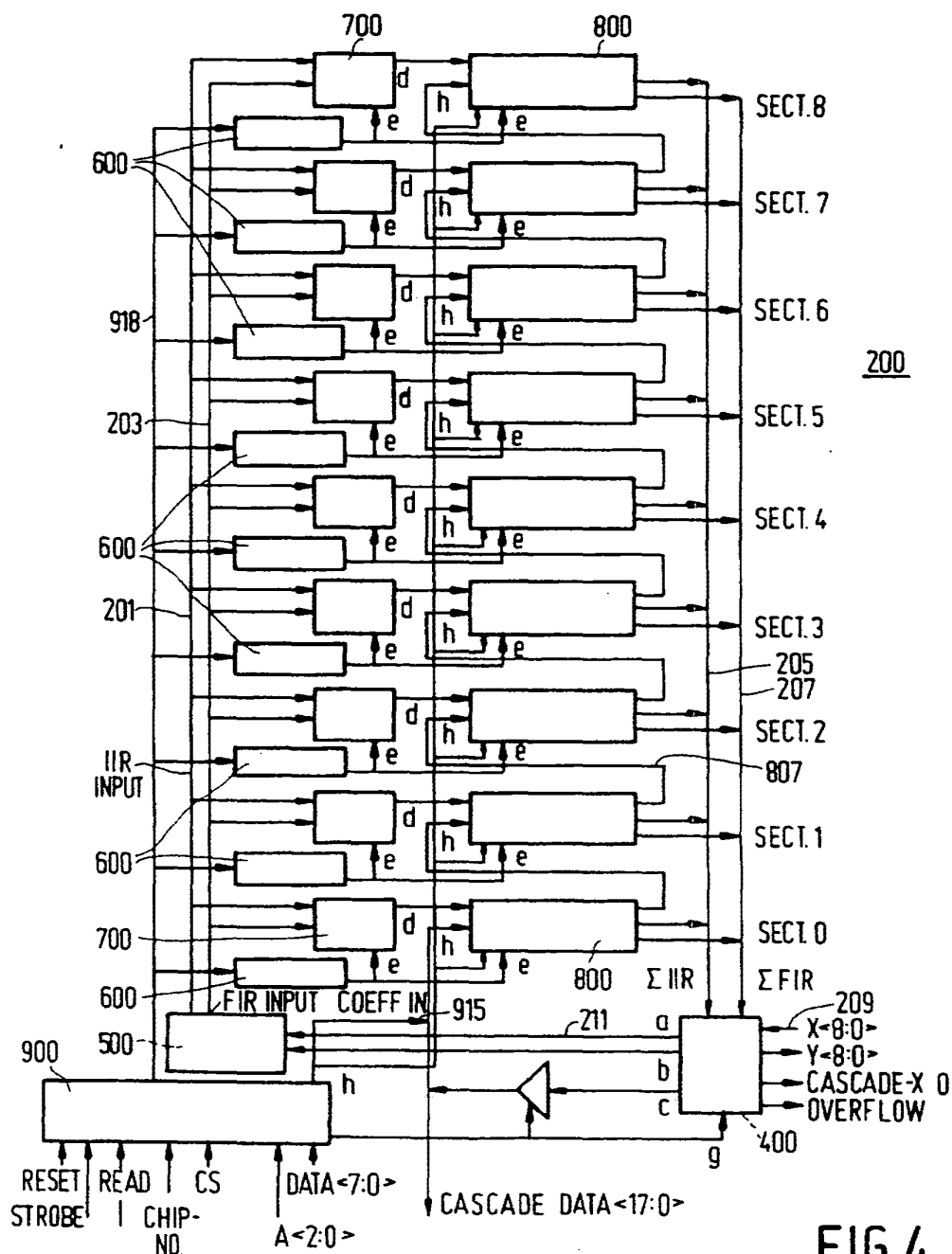


FIG. 5



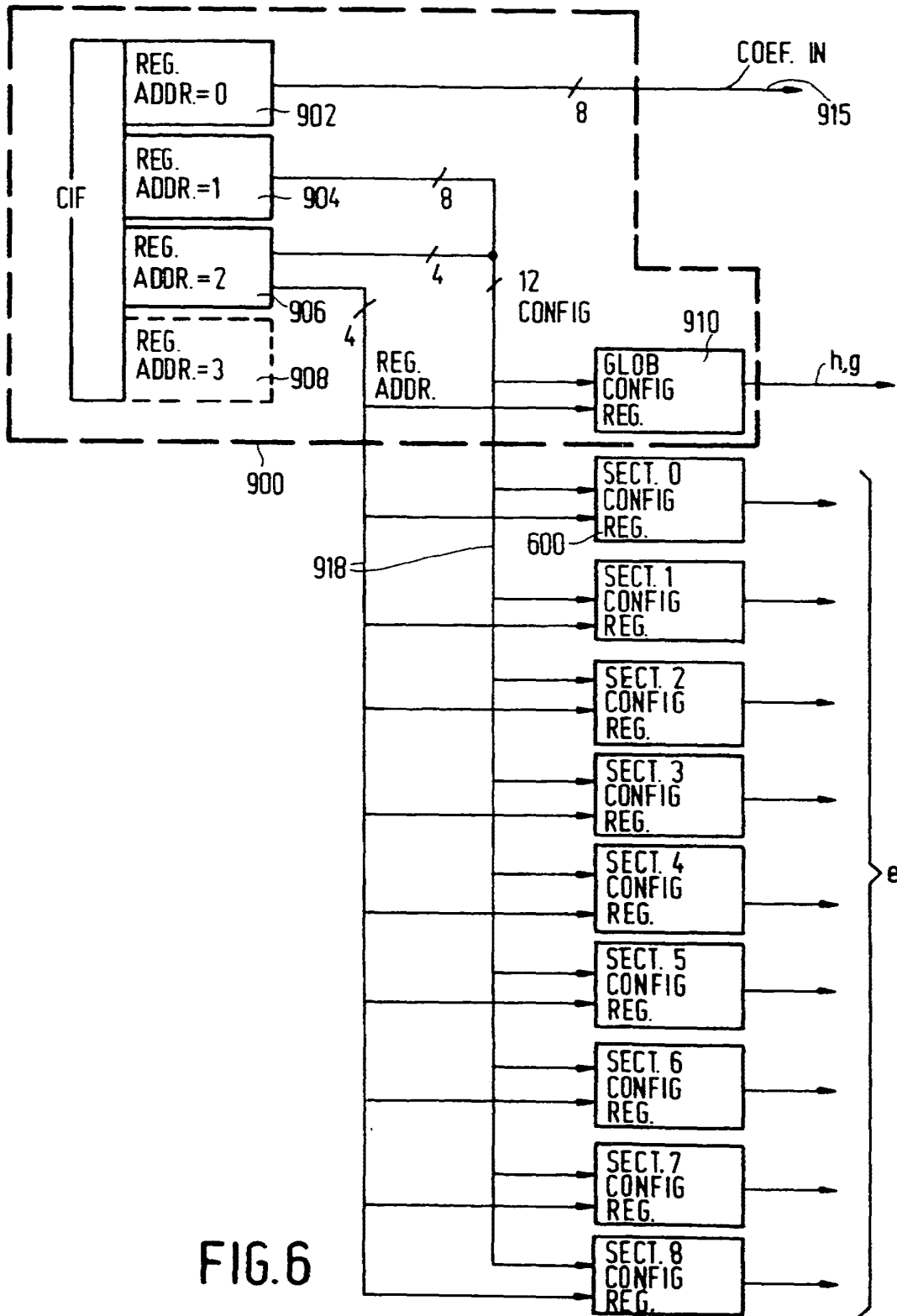


FIG. 6

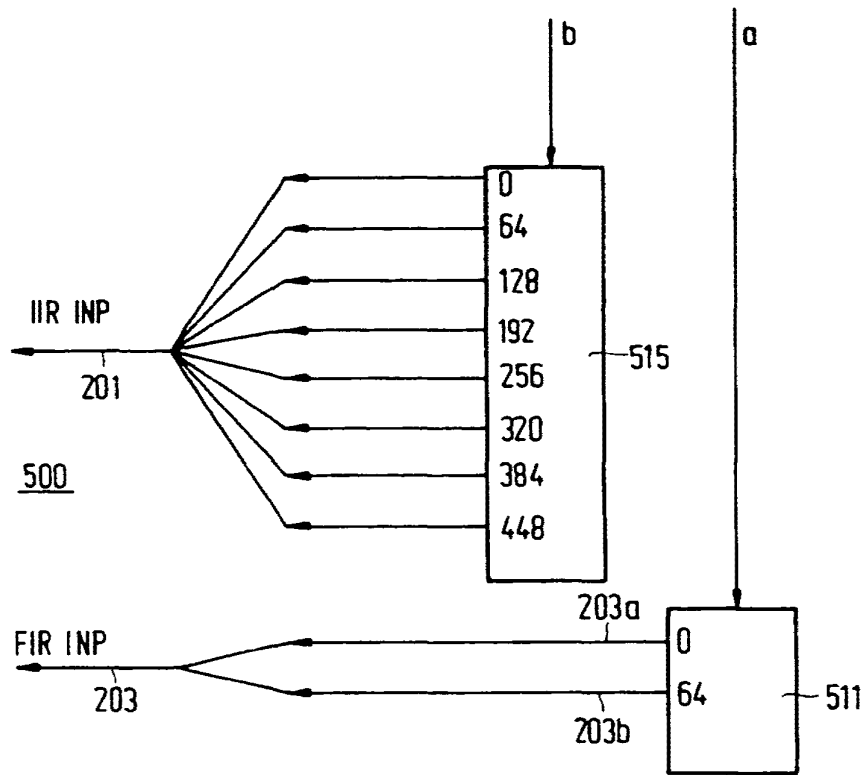


FIG. 7

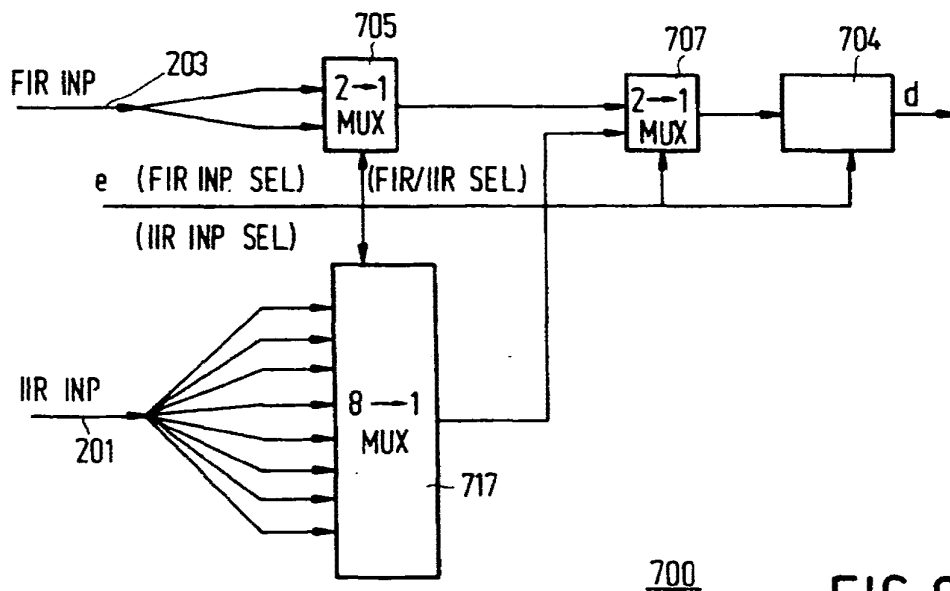


FIG. 8

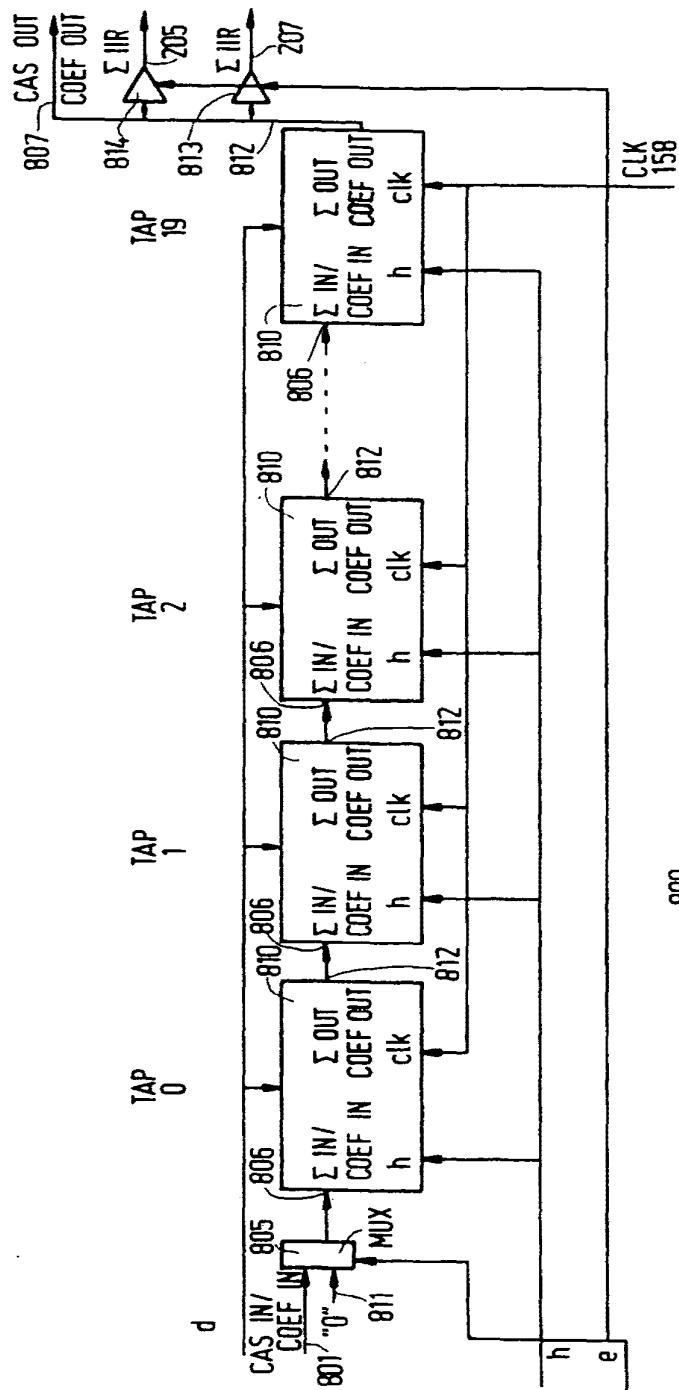


FIG. 9

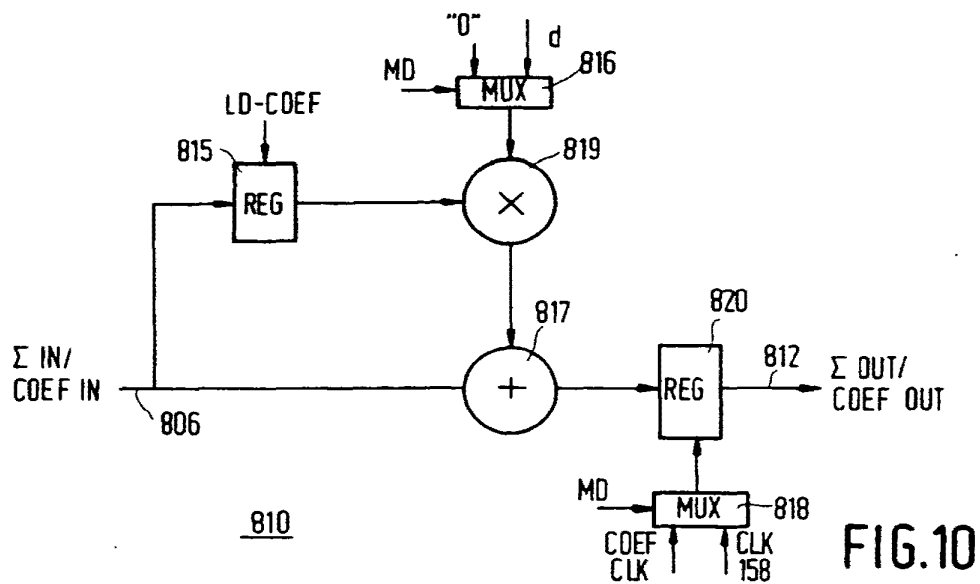


FIG. 10

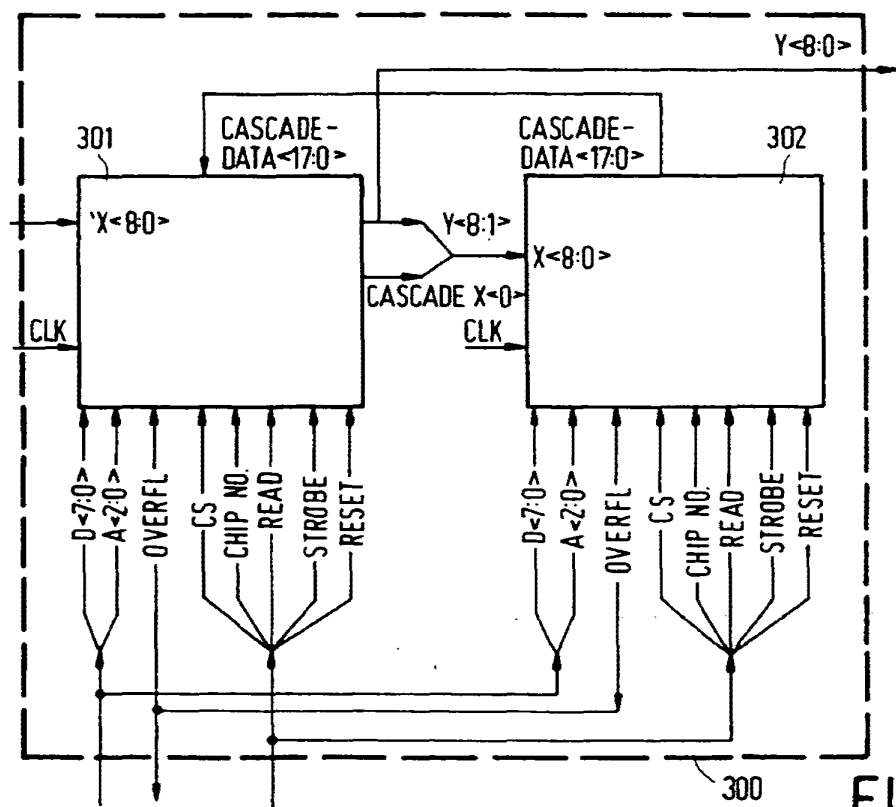


FIG. 11

(19)



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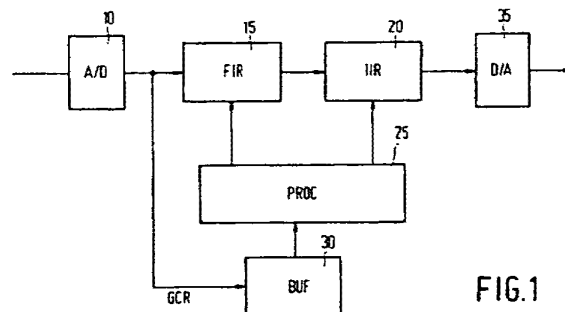
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NL-5656 AA Eindhoven (NL)**(54) **Echo cancellation system.**

(57) A circuit architecture suitable for use in a television receiver which effectively performs a ghost or echo cancellation procedure on post-echo components and pre-echo components occurring within the transmission channel. The apparatus features a filter circuit architecture which can be configured under programmed control so as to partition groups of its filter sections to form IIR filters and FIR filters. The filter architecture is suitable for use in multi-circuit configurations and can be used with clustering algorithms to increase the efficiency and optimize the use of the available circuit architecture.

**FIG.1****EP 0 516 216 A3**



European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP 92 20 1422

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,A	EP-A-0 448 352 (TOSHIBA) * column 6, line 9 - column 8, line 26 * * figure 4 * ---	1,2,4-8	H04N5/21 H04L25/03
A	US-A-4 698 680 (LEWIS, JR. ET AL.) * abstract; figure 7 * * column 12, line 14 - line 40 * ---	1-3,5,6	
A	US-A-4 344 089 (UTSUNOMIYA ET AL.) * abstract; figure 8 * ---	1	
A	PATENT ABSTRACTS OF JAPAN vol. 3, no. 103 (E-134)31 August 1979 & JP-A-54 81 019 (MATSUSHITA) 28 June 1979 * abstract * ---	1,3	
D,A	EP-A-0 417 861 (PHILIPS GLOEILAMPENFABRIEK) * page 2, line 1 - page 3, line 49 * -----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H04N H04L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 03 MAY 1993	Examiner BERWITZ P.
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10/884,347	07/01/2004	Pierre Favrat	XCE-P005	6856
32566 7590 01/31/2007 PATENT LAW GROUP LLP 2635 NORTH FIRST STREET SUITE 223 SAN JOSE, CA 95134			EXAMINER KOSTAK, VICTOR R	
			ART UNIT	PAPER NUMBER
			2622	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/31/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/884,347

Applicant(s)

FAVRAT ET AL.

Examiner

Victor R. Kostak

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 10-14, 16, 17 and 30-34 is/are rejected.
- 7) ☒ Claim(s) 6-9, 15 and 18-29 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 09/12/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____.

Art Unit: 2622

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 11, 12 and 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Favrat et al. (cited by applicant).

The television receiver of Favrat (noting Fig. 2) includes an input stage 54 that converts an RF signal into IF band, which received signal is in one of plural formats (at least by default). An A/D convertor 62 samples the IF signal and a subsequent DSP stage 64 performs digital processing in accordance with the format of the received RF signal. Downstream demodulation arrangement 66 carries out further processing to eventually reproduce the digital signal for presentation in either digital or analog form, thereby meeting claims 1, 11 and 31.

As for claims 2 and 32, the plural formats processable by Favrat or analog and digital signals (e.g. section [0002]).

As for claim 3, the receiver can be on a single chip (section [0038]).

Regarding claim 4, the downstream stage 66a provides baseband audio and video signals (Fig. 2) in analog form (section [0036]).

As for claim 12, signal output circuit comprises one or more single-ended output terminals, as shown.

Considering claims 33 and 34, processing of the digital signals is done in response to a select signal indicative of the format of the RF signal, such as by detecting the carrier (section [0030]).

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Favrat et al. in view of Balaban et al. (also cited by applicant).

It would have been obvious to ensure that the selected IF band is within the specific IF frequency such as by including a SAW filter as disclosed by Balaban (element 120 in Fig. 2), as well as assuring that the signal level is adequate for further processing for eventual reproduction, such as by maintaining its gain (stage 128 in Fig. 2 of Balaban).

3. Claims 5, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Favrat et al. in view of Oku et al. (also cited by applicant).

It would also have been obvious to one of ordinary skill in the art to provide respective decoding stages for the separate (and unique) video and audio components, as shown by Oku (e.g. Fig. 11), Favrat not getting into the details beyond the demodulation stages but mentioning such in passing: section [0036]), thereby meeting claim 5.

As for claim 13, it would also have been obvious to include plural DAC stages per respective audio and video signals, as well as respective driver stages (noting again Fig. 11 of Oku) to thereby provide additional reproduction options (Oku showing a display and a recorder, as well as a separate speaker).

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As for claim 14, the three DAC and driver channels include single-ended stages per the audio and video (and combination) channels.

4. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Favrat and Oku et al. as applied to claim 13, in further view of Gray et al.

Gray notes that the inclusion of a lowpass filter following a D/A convertor is typically done to make sure that conversion artifacts are removed (element 111 in Fig 9: col. 15 lines 21-25).

5. Claims 6-9, 15 and 18-29 appear allowable over the prior art.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is (571) 272-7348. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David W. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

Or faxed to:

(571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office whose telephone number is (703) 308-HELP.



Victor R. Kostak
Primary Examiner
Art Unit 2622

VRK



PTO/SB/08A (08-03)

Approved for use through 07/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Use as many sheets as necessary)

Sheet	1	of	2
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Complete if Known

Application Number	10/884,347
Filing Date	July 1, 2004
First Named Inventor	Pierre Favrat
Art Unit	2614
Examiner Name	John W. Miller
Attorney Docket Number	XCE-P005

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

/Victor Kostak/

Date Considered

01/29/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	10/884,347		
		Filing Date	July 1, 2004		
		First Named Inventor	Pierre Favrat		
		Art Unit	2614		
		Examiner Name	John W. Miller		
Sheet	2	of	2	Attorney Docket Number	XCE-P005

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
VK		International Search Report including written opinion, 11 pages.	

Examiner Signature	/Victor Kostak/	Date Considered	01/29/2007
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Notice of References Cited	Application/Control No. 10/884,347		Applicant(s)/Patent Under Reexamination FAVRAT ET AL.	
	Examiner Victor R. Kostak		Art Unit 2622	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,643,502	11-2003	Van De Plassche et al.	455/339
*	B	US-4,872,054	10-1989	Gray et al.	348/441
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.

10/884,347

Examiner

Victor R. Kostak

Applicant(s)/Patent under
Reexamination

FAVRAT ET AL.

Art Unit

2622

SEARCHED

Class	Subclass	Date	Examiner
348	554, 558, 725, 726, 705, 706	1/29/2007	VRK
375	316, 340,		
455	189.1		
	245.2		
	179.1		
	188.1		
	192.1		
	334		

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
EAST	1/29/2007	VRK
checked SN 10/236,645	1/29/2007	VRK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pierre Favrat, Alain-Serge Porret, Dominique Python, Friederich
Mombers, Richard P. Perring, Philippe Duc, Benito Carnero,
Didier Margairaz
Assignee: Xceive Inc.
Title: Television Receiver for Digital and Analog Television Signals
Serial No.: 10/884,347 Confirmation No.: 6856
Examiner: Victor R. Kostak Group Art Unit: 2622
Docket No.: XCE-P005 Filing Date: July 1, 2004

San Jose, California
April 17, 2007

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed January 31, 2007, Applicant submits the following amendments and remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Listing of Claims

The below listing of claims will replace all prior versions of claims in the application.

1. (Currently Amended) A television receiver comprising:
a frequency conversion circuit for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF), the input RF signal encoding information in one of a plurality of television signal formats;
an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof;
a signal processor for processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate frequency signal, each of the plurality of finite impulse response corresponding to a format of the input RF signal; and
a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals.
2. (Original) The television receiver of claim 1, wherein the plurality of television signal formats comprises an analog television format and a digital television format.
3. (Original) The television receiver of claim 1, wherein the television receiver is formed as a monolithic integrated circuit.
4. (Original) The television receiver of claim 1, wherein the signal output circuit provides a first output signal being a video baseband signal corresponding to an analog television format and a second output signal being an audio baseband signal corresponding to the analog television format.
5. (Original) The television receiver of claim 4, further comprising:

a first decoder circuit coupled to decode the video baseband signal for providing video display signals corresponding to the analog television format; and

a second decoder circuit coupled to decode the audio baseband signal for providing audio signals corresponding to the analog television format.

6. (Original) The television receiver of claim 5, wherein the first decoder circuit comprises a PAL/SECAM/NTSC decoder circuit.

7. (Original) The television receiver of claim 1, wherein the signal output circuit provides a first output signal and a second output signal corresponding to the digital output signals, the first output signal and the second output signal being differential output signals corresponding to a digital television format.

8. (Original) The television receiver of claim 7, further comprising:

a demodulator circuit for demodulating the first output signal and the second output signal according to the television signal format of the input RF signal, the demodulator circuit generating video and audio baseband signals corresponding to the format of the input RF signal; and

a decoder circuit coupled to decode the video and audio baseband signals for providing video and audio display signals corresponding to the digital television format.

9. (Original) The television receiver of claim 8, wherein the video and audio baseband signals comprise a MPEG data stream and the decoder circuit comprises a MPEG decoder circuit.

10. (Original) The television receiver of claim 1, further comprising:

a bandpass filter coupled to receive the intermediate frequency signal from the frequency conversion circuit and generate a filtered intermediate frequency signal; and

a variable gain amplifier coupled to receive the filtered intermediate frequency signal and provide the amplified, filtered intermediate frequency signal to the analog-to-digital converter.

11. (Original) The television receiver of claim 1, wherein the signal output circuit provides output signals in an analog or a digital signal format.

12. (Original) The television receiver of claim 1, wherein the signal output circuit comprises one or more output terminals, each of the one or more output terminals of the signal output circuit comprises a single-ended output terminal or a differential output terminal.

13. (Original) The television receiver of claim 1, wherein the signal output circuit comprises:

- a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;

- a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;

- a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a second output terminal;

- a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

- a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a third output terminal,

- wherein the first and second output terminals provide signals indicative of video and audio information encoded in the input RF signal and the third output terminal provides signals indicative of audio information encoded in the input RF signal.

14. (Original) The television receiver of claim 13, wherein the first driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to an analog television format, the analog output signals being video baseband signals; and the third driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to the analog television format, the analog output signals being audio baseband signals.

15. (Original) The television receiver of claim 13, wherein the second driver circuit comprises a differential output driver circuit for driving analog output signals corresponding to a digital television format, the analog output signals being DTV low-IF

signals, and wherein the second output terminal comprises a first differential output terminal and a second differential output terminal.

16. (Original) The television receiver of claim 13, wherein the signal output circuit further comprises:

a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.

17. (Original) The television receiver of claim 13, wherein the signal output circuit further comprises:

a low pass filter coupled between the second digital-to-analog converter and the third driver circuit, the low pass filter providing low pass filtering function.

18. (Original) The television receiver of claim 1, wherein the signal output circuit comprises:

a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;

a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;

a second driver circuit for driving the analog output signals from the first digital-to-analog converter, the second driver circuit comprising a differential output driver circuit having a first differential output terminal and a second differential output terminal, the first differential output terminal being coupled to the first output terminal and the second differential output terminal being coupled to a second output terminal;

a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto the second output terminal,

wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format; and the first output terminal provides video information encoded in the input RF signal and the second output

terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format.

19. (Original) The television receiver of claim 18, wherein the signal output circuit further comprises:

a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.

20. (Original) The television receiver of claim 1, wherein the signal output circuit comprises:

a first serializer circuit coupled to receive the digital output signals from the signal processor and convert the digital output signals to a serial digital data stream;

a first driver circuit comprising a differential output driver for driving the serial digital data stream from the first serializer onto a first output terminal and a second output terminal;

a first digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and

a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a third output terminal,

wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format and provide differential output signal indicative of video information when the input RF signal has an analog television signal format; and the third output terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format.

21. (Original) The television receiver of claim 20, wherein the first, second and third output terminals of the signal output circuit are coupled to a demodulator-decoder circuit, the demodulator-decoder circuit demodulating the serial digital data stream when the data stream corresponds to a digital television format and the demodulator-decoder circuit

decoding the serial digital data stream when the data stream corresponds to an analog television format.

22. (Original) The television receiver of claim 20, wherein the signal output circuit further comprises:

a second digital-to-analog converter coupled to receive the digital output signals from the signal processor and convert the digital output signals to analog output signal; and

a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a fourth output terminal,

wherein the fourth output terminal provides signals indicative of video information encoded in the input RF signal when the input RF signal has an analog television signal format.

23. (Original) The television receiver of claim 20, wherein the signal output circuit further comprises:

a second serializer circuit coupled to receive the digital output signals from the signal processor and convert the digital output signals to a serial digital data stream; and

a third driver circuit comprising a differential output driver for driving the serial digital data stream from the second serializer onto a fourth output terminal and a fifth output terminal,

wherein the first and second driver circuits drive the serial digital data stream corresponding to a digital television format and the fourth and fifth driver circuits drive the serial digital data stream corresponding to an analog television format.

24. (Cancelled)

25. (Currently Amended) The television receiver of ~~claim 24~~ claim 1, wherein the plurality of finite impulse response filters are stored in a memory, and the signal processor indexes the memory to retrieve one of the plurality of finite impulse response filters.

26. (Currently Amended) The television receiver of ~~claim 24~~ claim 1, wherein the signal processor comprises a first computing unit and a second computing unit, the first computing unit processing a real part of the finite impulse response filter operation while the

second computing unit processing an imaginary part of the finite impulse response filter operation.

27. (Currently Amended) The television receiver of ~~claim 24~~ claim 1, further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the input RF signal and the signal processor selecting a finite impulse response filter in response to the select signal.

28. (Original) The television receiver of claim 27, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user.

29. (Original) The television receiver of claim 27, wherein the format/standard selection circuit generates the select signal by detecting carrier signals identifying one of the formats of the input RF signals.

30. (Original) The television receiver of claim 1, wherein the input RF signal comprises an RF signal received from terrestrial broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission.

31-34: (Cancelled)

REMARKS

Claims 1-34 are pending in the case. Claims 1-5, 10-14, 16, 17 and 30-34 are rejected. Claims 6-9, 15 and 18-29 are objected to as being dependent upon a rejected base claim but are allowable if rewritten in independent form. In the present submission, claims 1 and 25-27 have been amended and claims 24 and 31-34 have been cancelled. Reconsideration is respectfully requested.

In the present submission, claim 1 has been amended to include the limitations of claim 24 and claim 24 is canceled. Since claim 24 is indicated to be allowable, claim 1 is therefore in condition for allowance. Claims 2-23 and 25-30, dependent upon claim 1, are also in condition for allowance. Claims 25-27 have been amended to update their claim dependency to claim 1.

Claims 31-34 have been cancelled and the rejection as to these claims is therefore moot.

After the present amendment, claims 1-23 and 25-30 are pending. The application is in condition for allowance and passage of the present case to allowance is respectfully requested. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

Certificate of Electronic Transmission

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office using EFS-Web on the date shown below.

/Carmen C Cook/	April 17, 2007
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

/Carmen C Cook/

Carmen C. Cook
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San Jose, CA 95134
Tel (408) 382-0480 x208
Fax (408) 382-0481

Electronic Acknowledgement Receipt

EFS ID:	1690086
Application Number:	10884347
International Application Number:	
Confirmation Number:	6856
Title of Invention:	Television receiver for digital and analog television signals
First Named Inventor/Applicant Name:	Pierre Favrat
Customer Number:	32566
Filer:	Carmen C. Cook
Filer Authorized By:	
Attorney Docket Number:	XCE-P005
Receipt Date:	17-APR-2007
Filing Date:	01-JUL-2004
Time Stamp:	15:49:06
Application Type:	Utility

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		XCE-P005-Resp-to-OA.pdf	123021	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment - After Non-Final Rejection	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
Warnings:			
Information:			
Total Files Size (in bytes):		123021	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

10884347

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

TOTAL CLAIMS	34	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	34 minus 20 =	14
INDEPENDENT CLAIMS	2 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A	4/17/07	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	29	Minus	30	= 1
	Independent	1	Minus	3	= 1
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1) (Column 2) (Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1) (Column 2) (Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐ OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	126
X43=	
+145=	
TOTAL	511

RATE	FEE
BASIC FEE	770.00
XS18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	1
X43=	
+145=	
TOTAL ADDIT. FEE	1

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10367	"intermediate frequency"	US-PGPUB	OR	ON	2007/05/11 09:26
L2	71417	television	US-PGPUB	OR	ON	2007/05/11 09:26
L3	2194	1 and 2	US-PGPUB	OR	ON	2007/05/11 09:27
L4	4678	"finite impulse"	US-PGPUB	OR	ON	2007/05/11 09:27
L5	10668	fir	US-PGPUB	OR	ON	2007/05/11 09:27
L6	11212	4 or 5	US-PGPUB	OR	ON	2007/05/11 09:27
L7	157	3 and 6	US-PGPUB	OR	ON	2007/05/11 09:27



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

32566 7590 05/21/2007

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

EXAMINER

KOSTAK, VICTOR R

ART UNIT

PAPER NUMBER

2622

DATE MAILED: 05/21/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/884,347	07/01/2004	Pierre Favrat	XCE-P005	6856

TITLE OF INVENTION: TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	08/21/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

32566 7590 05/21/2007

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/884,347	07/01/2004	Pierre Favrat	XCE-P005	6856

TITLE OF INVENTION: TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	08/21/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
KOSTAK, VICTOR R	2622	348-554000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 _____
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Silicon Labs v. Cresta Technology

Silabs IPR Exhibit 1010

PTOL-85 (Rev. 07/06) Approved for use through 05/31/2007.

OMB 0659-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/884,347	07/01/2004	Pierre Favrat	XCE-P005	6856
32566	7590	05/21/2007	EXAMINER	
PATENT LAW GROUP LLP 2635 NORTH FIRST STREET SUITE 223 SAN JOSE, CA 95134			KOSTAK, VICTOR R	
			ART UNIT	PAPER NUMBER
			2622	
DATE MAILED: 05/21/2007				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 517 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 517 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/884,347

Examiner

Victor R. Kostak

Applicant(s)

FAVRAT ET AL.

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on 04/17/07.
2. ☒ The allowed claim(s) is/are 1-23 and 25-30.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material

5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


Victor R. Kostak
Primary Examiner
Art Unit: 2622

Issue Classification 	Application/Control No. 10/884,347	Applicant(s)/Patent under Reexamination FAVRAT ET AL.
	Examiner Victor R. Kostak	Art Unit 2622

ISSUE CLASSIFICATION												
ORIGINAL				INTERNATIONAL CLASSIFICATION								
CLASS		SUBCLASS		CLAIMED				NON-CLAIMED				
348		554		H	04	N	3	/27				/
CROSS REFERENCES				H	04	N	5	/46				/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											
348	558							/				/
								/				/
								/				/
								/				/
								/				/
								/				/

----- (Assistant Examiner) (Date) <i>J. Douglas</i> 5/17/07 (Legal Instruments Examiner) (Date)	<i>L. Kostak</i> Victor R. Kostak 05/11/07 (Primary Examiner) (Date)	Total Claims Allowed: 29 <table border="1"> <tr> <td>O.G. Print Claim(s)</td> <td>O.G. Print Fig.</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>	O.G. Print Claim(s)	O.G. Print Fig.	1	1
O.G. Print Claim(s)	O.G. Print Fig.					
1	1					

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181		
2	2		32		62		92		122		152		182		
3	3		33		63		93		123		153		183		
4	4		34		64		94		124		154		184		
5	5		35		65		95		125		155		185		
6	6		36		66		96		126		156		186		
7	7		37		67		97		127		157		187		
8	8		38		68		98		128		158		188		
9	9		39		69		99		129		159		189		
10	10		40		70		100		130		160		190		
11	11		41		71		101		131		161		191		
12	12		42		72		102		132		162		192		
13	13		43		73		103		133		163		193		
14	14		44		74		104		134		164		194		
15	15		45		75		105		135		165		195		
16	16		46		76		106		136		166		196		
17	17		47		77		107		137		167		197		
18	18		48		78		108		138		168		198		
19	19		49		79		109		139		169		199		
20	20		50		80		110		140		170		200		
21	21		51		81		111		141		171		201		
22	22		52		82		112		142		172		202		
23	23		53		83		113		143		173		203		
	24		54		84		114		144		174		204		
24	25		55		85		115		145		175		205		
25	26		56		86		116		146		176		206		
26	27		57		87		117		147		177		207		
27	28		58		88		118		148		178		208		
28	29		59		89		119		149		179		209		
30	30		60		90		120		150		180		210		



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Bib Data Sheet

CONFIRMATION NO. 6856

SERIAL NUMBER 10/884,347	FILING OR 371(c) DATE 07/01/2004 RULE	CLASS 348	GROUP ART UNIT 2622	ATTORNEY DOCKET NO. XCE-P005
APPLICANTS Pierre Favrat, Milpitas, CA; Alain-Serge Porret, Sunnyvale, CA; Dominique Python, Sunnyvale, CA; Friederich Mombers, San Jose, CA; Richard P. Perring, San Jose, CA; Philippe Duc, Santa Clara, CA; Benito Carnero, Santa Clara, CA; Didier Margairaz, San Jose, CA;				
** CONTINUING DATA ***** <i>none vnu</i>				
** FOREIGN APPLICATIONS ***** <i>none vnu</i>				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED** SMALL ENTITY ** ** 08/18/2004				
Foreign Priority claimed ☐ yes ☒ no 35 USC 119 (a-d) conditions ☐ yes ☒ no ☐ Met after met Verified and Acknowledged <i>u mo</i> Allowance <i>u mo</i> Examiner's Signature Initials		STATE OR COUNTRY CA	SHEETS DRAWING 3	TOTAL CLAIMS 34
			INDEPENDENT CLAIMS 2	
ADDRESS 32566				
TITLE Television receiver for digital and analog television signals				
FILING FEE RECEIVED 511	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	

Search Notes



Application/Control No.

10/884,347

Examiner

Victor R. Kostak

Applicant(s)/Patent under Reexamination

FAVRAT ET AL.

Art Unit

2622

SEARCHED

Class	Subclass	Date	Examiner
348	554, 558, 725, 726, 705, 706	1/29/2007	VRK
375	316, 340,		
455	189.1		
	245.2		
	179.1		
	188.1		
	192.1		
	334		
up 2nd 5/11/07 VRK			

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
EAST interference search			
		5-11-07	VRK

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
EAST	1/29/2007	VRK
checked SN 10/236,645	1/29/2007	VRK
	5-11-07	VRK

Issue Classification 	Application/Control No. 10/884,347	Applicant(s)/Patent under Reexamination FAVRAT ET AL.
	Examiner Victor R. Kostak	Art Unit 2622

ISSUE CLASSIFICATION											
ORIGINAL				INTERNATIONAL CLASSIFICATION							
CLASS		SUBCLASS		CLAIMED				NON-CLAIMED			
348		554		H	04	N	3	/27			
CROSS REFERENCES				H	04	N	5	/46			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
348	558							/			/
								/			/
								/			/
								/			/
								/			/
								/			/

----- (Assistant Examiner) (Date) <i>J. Douglas</i> 5/17/07 (Legal Instruments Examiner) (Date)		<i>L. Kostak</i> Victor R. Kostak 05/11/07 (Primary Examiner) (Date)	Total Claims Allowed: 29
		O.G. Print Claim(s) 1	O.G. Print Fig. 1

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original		
1	1		31		61		91		121		151		181		
2	2		32		62		92		122		152		182		
3	3		33		63		93		123		153		183		
4	4		34		64		94		124		154		184		
5	5		35		65		95		125		155		185		
6	6		36		66		96		126		156		186		
7	7		37		67		97		127		157		187		
8	8		38		68		98		128		158		188		
9	9		39		69		99		129		159		189		
10	10		40		70		100		130		160		190		
11	11		41		71		101		131		161		191		
12	12		42		72		102		132		162		192		
13	13		43		73		103		133		163		193		
14	14		44		74		104		134		164		194		
15	15		45		75		105		135		165		195		
16	16		46		76		106		136		166		196		
17	17		47		77		107		137		167		197		
18	18		48		78		108		138		168		198		
19	19		49		79		109		139		169		199		
20	20		50		80		110		140		170		200		
21	21		51		81		111		141		171		201		
22	22		52		82		112		142		172		202		
23	23		53		83		113		143		173		203		
	24		54		84		114		144		174		204		
24	25		55		85		115		145		175		205		
25	26		56		86		116		146		176		206		
26	27		57		87		117		147		177		207		
27	28		58		88		118		148		178		208		
28	29		59		89		119		149		179		209		
29	30		60		90		120		150		180		210		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pierre Favrat et al.
Assignee: Xceive Inc.
Title: Television Receiver for Digital and Analog Television Signals
Serial No.: 10/884,347 Confirmation No.: 6856
Examiner: Victor R. Kostak Group Art Unit: 2622
Docket No.: XCE-P005 Filing Date: July 1, 2004

San Jose, California
July 31, 2007

Mail Stop Issue Fee
ATTN: Nadine Clark
Office of Patent Publication
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS
Notice of Allowance Mailed

In response to Notice to File Corrected Application Papers (Notice of Allowance Mailed) mailed July 19, 2007, Applicant submits the following:

1. Three (3) sheets of formal drawings, consisting of Figures 1, 2, 3A, and 3B, in the above-named application.
2. A copy of Notice to File Corrected Application Papers.

If there are any questions regarding these drawings, please call the undersigned at (408) 382-0480.

Certificate of Electronic Transmission

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office on the date shown below.

/Carmen C Cook/	July 31, 2007
Attorney for Applicant(s)	Date

Respectfully submitted,

/Carmen C Cook/

Carmen C Cook
Attorney for Applicant(s)
Reg. No. 42,433

100

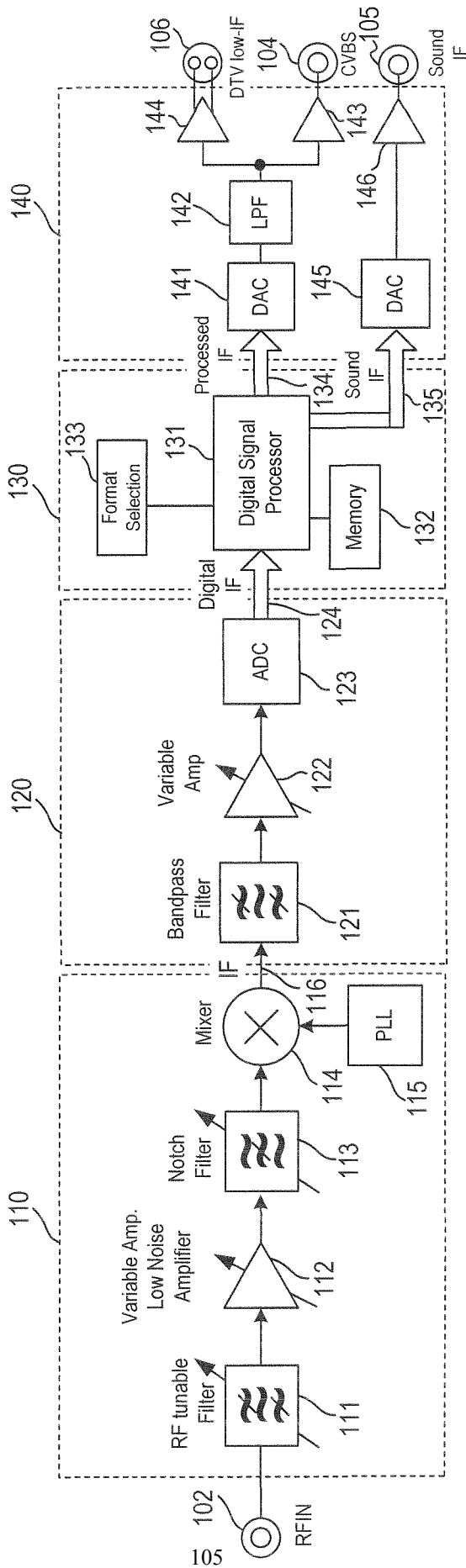


Fig. 1

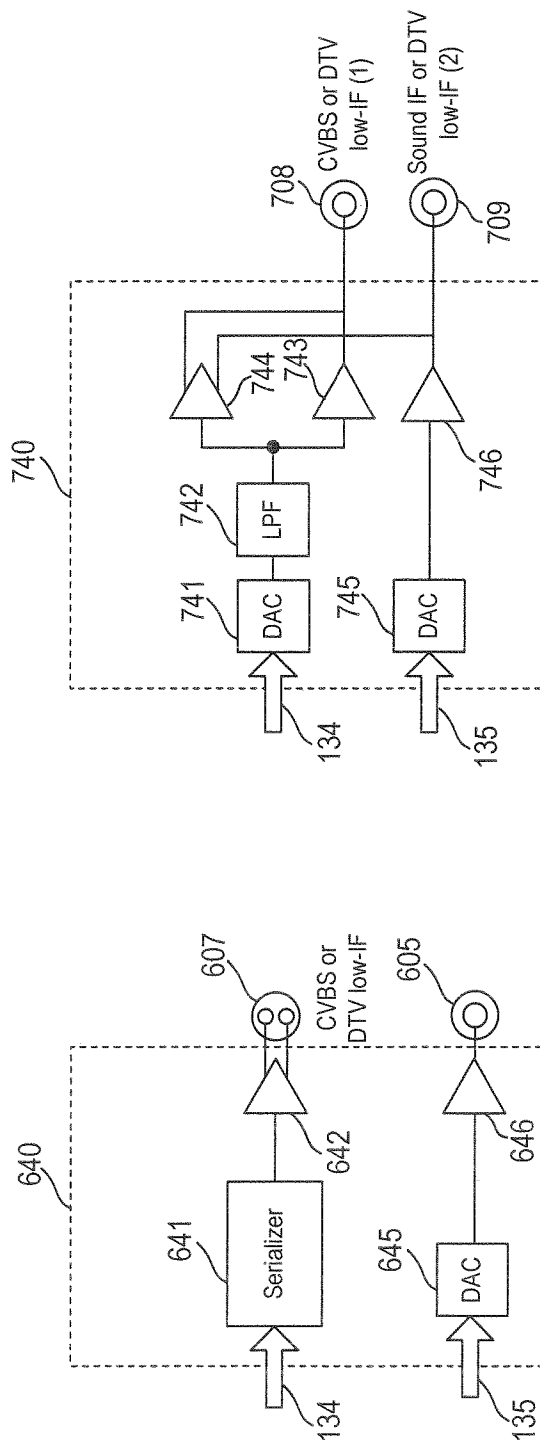
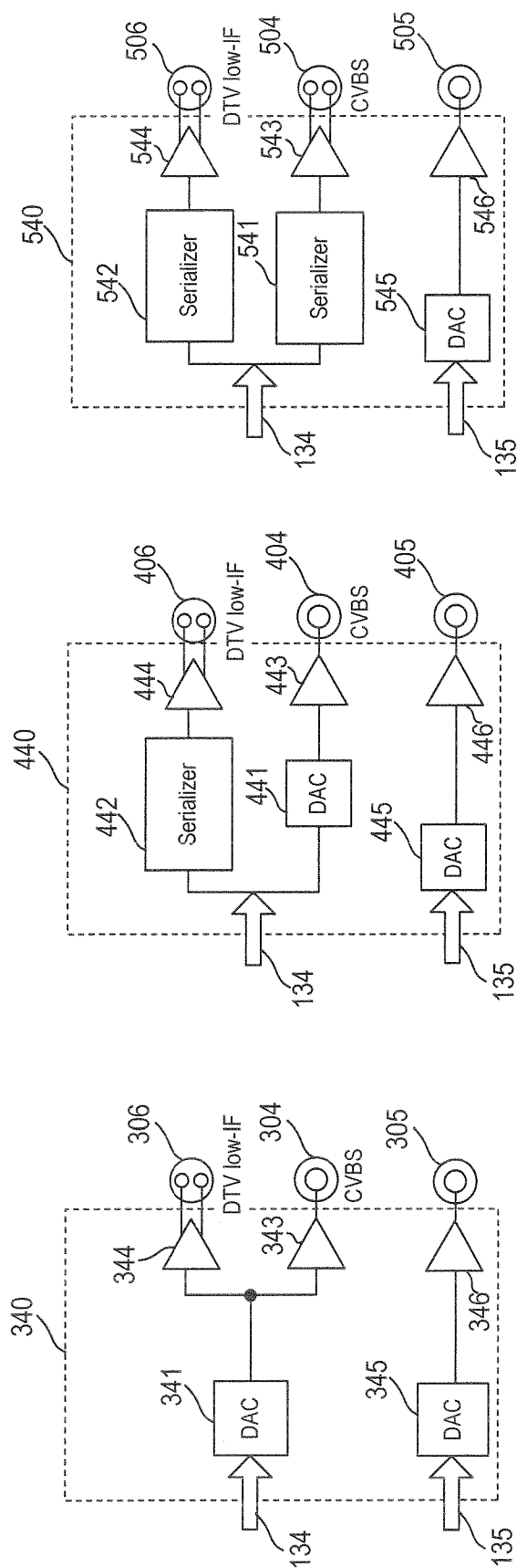
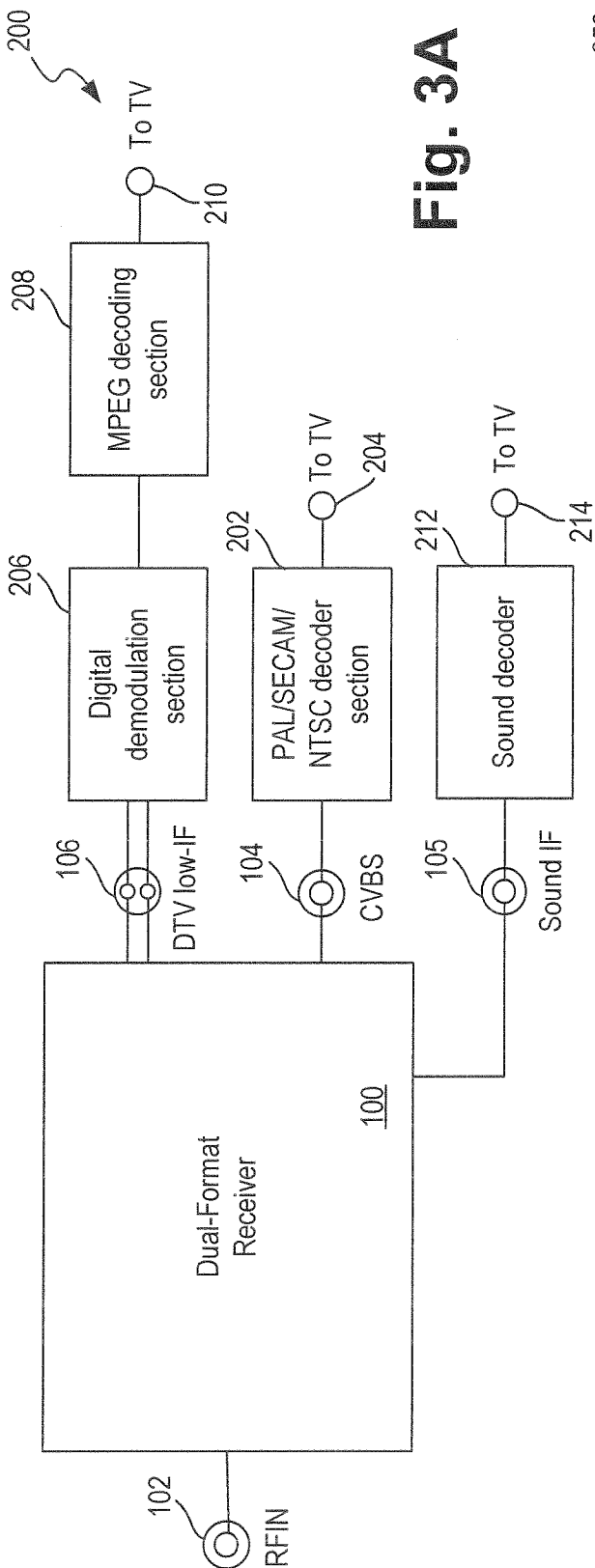
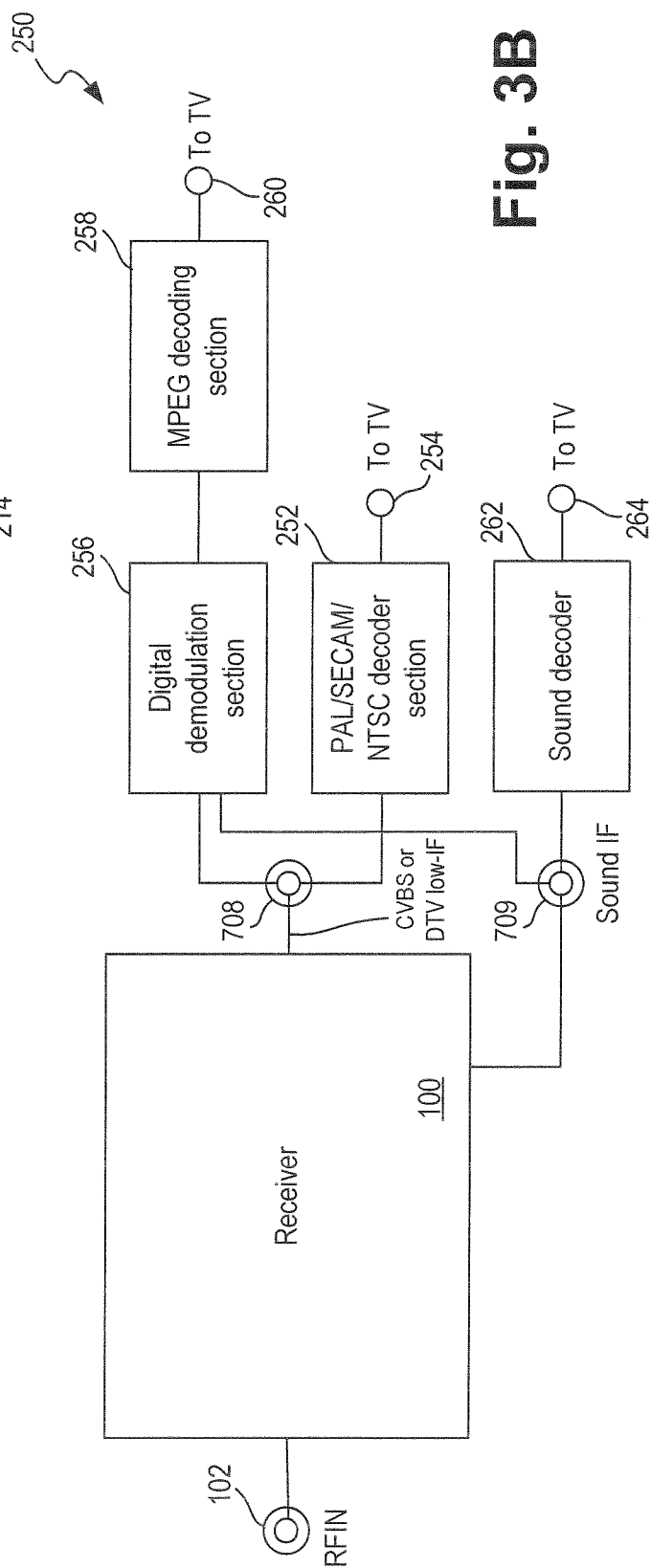


Fig. 2

**Fig. 3A****Fig. 3B**



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Serial No. 10/884,347
Applicant : Favrat, et al
Filing Date 07/01/2004
Date Mailed : 07/19/2007

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 60 days from the mail date of this Notice within which to correct the informalities indicated below. If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to reply will result in the application being ABANDONED. **This period for reply is NOT extendable under 37 CFR 1.136(a).**

See attachment.

*A copy of this notice **MUST** be returned with the reply. Please address response to
"Mail Stop Issue Fee, Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450".*

Nadine Clark

Office of Patent Publication
Phone: 703-308-9250, ext.144

Application No. 10/884,347 Drawings filed 7/1/04

IDENTIFICATION OF DRAWING DEFICIENCIES

- ☐ There are holes punched in the illustration. FIG(s) _____
- ☐ The character of the lines, numbers and letters are poor/ faded. FIG(s) _____
- ☐ The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s) _____
- ☐ A date stamp obscures part of the illustration. FIG(s) _____
- ☐ The drawing is solid black box or marred by black smudges, obliterations, or fax/copier marks. FIG(s) _____
- ☐ Figure number is duplicated/missing. Drawing sheet is missing. FIG(s). _____
- ☐ Numbers, letters, or reference characters in the drawing have been crossed out by hand and are illegibly handwritten. FIG(s) _____
- ☐ The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s) _____
- ☐ The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s) _____
- ☐ Missing data, part of the drawing is cut off, lead line no reference number FIG(s) _____
- ☐ The drawing is continued onto a second page (or more) without proper labeling under 37 CFR 1.81(u)(1). FIG(s) _____
- ☐ The drawing and/or the FIG. label contain(s) foreign language. FIG(s) _____
- ☐ Color drawings are present in this application but the following CFR 1.84 (a) requirements have not been met*:
 - ☐ Petition filed
 - ☐ Petition fee
 - ☐ 3 sets of color drawings
 - ☐ Color drawing paragraph

*If color drawings are not elected, then applicant **must respond** so stating. Also, references to color drawings in the specification, if any, must be amended.

COMMENTS: Please Submitt formal Drawings

Electronic Acknowledgement Receipt

EFS ID:	2032666
Application Number:	10884347
International Application Number:	
Confirmation Number:	6856
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS
First Named Inventor/Applicant Name:	Pierre Favrat
Customer Number:	32566
Filer:	Carmen C. Cook/Linda Richardson
Filer Authorized By:	Carmen C. Cook
Attorney Docket Number:	XCE-P005
Receipt Date:	31-JUL-2007
Filing Date:	01-JUL-2004
Time Stamp:	18:25:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	XCE-P005_Resp_Notice_File_Corrected_Papers.pdf	63403 f16e61ea45b6bdd05a7cba8e7f1664d705ece359	no	1

Warnings:

Information:					
2	Drawings	XCE-P005_Drawings.pdf	217971	no	3
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Warnings:					
Information:					
3	Miscellaneous Incoming Letter	XCE-P005_Copy_of_Notice_to_File_Corrected_Application_Papers.pdf	182670	no	2
			f961d92eb8c19ac767bfc375e165abbclc38be86		
Warnings:					
Information:					
Total Files Size (in bytes):			464044		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

32566 7590 05/21/2007

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
/Electronic Filing/ (Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/884,347 07/01/2004 Pierre Favrat XCE-P005 6856

TITLE OF INVENTION: TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional YES \$700 \$300 \$0 \$1000 08/21/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
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KOSTAK, VICTOR R 2622 348-554000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Patent Law Group LLP
2 Carmen C Cook
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Xceive Corporation

Santa Clara, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. ~~XXXXXXXXXXXX~~
☒ The Director is hereby authorized to charge the ~~XXXXXXXXXXXX~~, any deficiency, or credit any overpayment, to Deposit Account Number 502226 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Carmen C. Cook

Date 8/1/07

Typed or printed name Carmen C. Cook

Registration No. 42,433

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	10884347			
Filing Date:	01-Jul-2004			
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS			
First Named Inventor/Applicant Name:	Pierre Favrat			
Filer:	Carmen C. Cook/Linda Richardson			
Attorney Docket Number:	XCE-P005			
Filed as Small Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	700	700
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt

EFS ID:	2035617
Application Number:	10884347
International Application Number:	
Confirmation Number:	6856
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS
First Named Inventor/Applicant Name:	Pierre Favrat
Customer Number:	32566
Filer:	Carmen C. Cook/Linda Richardson
Filer Authorized By:	Carmen C. Cook
Attorney Docket Number:	XCE-P005
Receipt Date:	01-AUG-2007
Filing Date:	01-JUL-2004
Time Stamp:	14:44:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	8883
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Issue Fee Payment (PTO-85B)	XCE-P005_Issue_Fee_Transmittal.pdf	197228 5469f2fb7ad5ad4100a40eca41b2ba1e83892ebd	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8308 dbdf38cdb3dc64c9ddeef0bd807b7f53e3a60bd5	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			205536		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/884,347	09/04/2007	7265792	XCE-P005	6856

32566 7590 08/15/2007
PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 481 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Pierre Favrat, Milpitas, CA;
Alain-Serge Porret, Sunnyvale, CA;
Dominique Python, Sunnyvale, CA;
Friederich Mombers, San Jose, CA;
Richard P. Perring, San Jose, CA;
Philippe Duc, Santa Clara, CA;
Benito Carnero, Santa Clara, CA;
Didier Margairaz, San Jose, CA;

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:



Practitioners associated with the Customer Number:

23574

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

23574

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address:

Cresta Technology Corporation
3900 Freedom Circle, Suite 201
Santa Clara, CA 95054

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	11/4/2011
Name	George T. Haber	Telephone	(415) 370 4476
Title	CEO, Cresta Technology Corporation		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Cresta Technology Corporation

Application No./Patent No.: 7,265,792 Filed/Issue Date: 09/04/2007

Titled: Television Receiver for Digital and Analog Television Signals

Cresta Technology Corporation, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: Xceive Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 015548, Frame 0385, or for which a copy thereof is attached.

2. From: Xceive Corporation To: Xceive (Assignment for the benefit of creditors)

The document was recorded in the United States Patent and Trademark Office at
Reel 027007, Frame 0701, or for which a copy thereof is attached.

3. From: Xceive (Assignment for the benefit of creditors) To: Cresta Technology Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 027007, Frame 0769, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Andrei D. Popovici Reg. No. 42,401/

11/4/2011

Signature

Date

Andrei D. Popovici, Reg. No. 42,401

Patent Attorney

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	11349149
Application Number:	10884347
International Application Number:	
Confirmation Number:	6856
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS
First Named Inventor/Applicant Name:	Pierre Favrat
Customer Number:	32566
Filer:	Andrei D. Popovici
Filer Authorized By:	
Attorney Docket Number:	XCE-P005
Receipt Date:	07-NOV-2011
Filing Date:	01-JUL-2004
Time Stamp:	14:28:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	CRESTA-GeneralPofA-Signed-20111104.pdf	188904 cfb5cb5c19c259bf38c2be209b93f4f6e2b974b5	no	1

Warnings:

Information:

2	Assignee showing of ownership per 37 CFR 3.73(b).	XCE-P005-Statement-3-73b-sb0096-07-2009.pdf	430053 80527c4df80a07a3aa0bd602286e25441bd79806	no	2
Warnings:					
Information:					
Total Files Size (in bytes):				618957	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/884,347	07/01/2004	Pierre Favrat	XCE-P005

CONFIRMATION NO. 6856

POA ACCEPTANCE LETTER

23574
LAW OFFICE OF ANDREI D POPOVICI, P.C.
4020 MOORPARK AVE.
SUITE101
SAN JOSE, CA 95117



Date Mailed: 11/21/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/07/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/s/brahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/884,347	07/01/2004	Pierre Favrat	XCE-P005

32566
PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

CONFIRMATION NO. 6856
POWER OF ATTORNEY NOTICE



Date Mailed: 11/21/2011

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/07/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/s/brahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,265,792 B2

APPLICATION NO.: 10/884,347

ISSUE DATE : 09/04/2007

INVENTOR(S) : FAVRAT et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 11, line 1 (claim 1 line 18), insert -- filters -- after "response."

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Law Office of Andrei D. Popovici, P.C.
4030 Moorpark Ave., Suite 108, San Jose, CA 95117

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

In the Certificate of Corrections Branch

Applicant(s): FAVRAT et al.

Serial No.: 10/884,347

Filed: 07/01/2004

Patent No.: 7,265,792 B2

Issued: 09/04/2007

Title: Television Receiver for Digital and
Analog Television Signals

Group Art Unit:

Examiner:

Request for Certificate of Correction Under 37 C.F.R. 1.322/1.323

Certificate of Corrections Branch
Commissioner for Patents, Office of Patent Publication
P. O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Please correct the above-referenced patent as shown on the enclosed form PTO/SB/44.

The error listed herein is of a clerical or typographical nature or of minor character, and does not constitute new matter or require reexamination. See 37 C.F.R. 1.323 and MPEP 1481.

Applicant respectfully requests issuance of a Certificate of Correction under 37 C.F.R. 1.322 or 1.323 (see MPEP 1480, 1481).

Respectfully submitted,

Date: 10/09/2013

/Andrei D. Popovici Reg. No. 42,401/

Andrei D. Popovici
Reg. No. 42,401

Law Office of Andrei D. Popovici, P.C.
4030 Moorpark Ave., Suite 108, San Jose, CA 95117

Telephone: (650) 530-9989, Facsimile: (650) 530-9990, Email: andrei@apatent.com

Electronic Patent Application Fee Transmittal

Application Number:	10884347			
Filing Date:	01-Jul-2004			
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS			
First Named Inventor/Applicant Name:	Pierre Favrat			
Filer:	Andrei D. Popovici			
Attorney Docket Number:	XCE-P005			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of Correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	17087943
Application Number:	10884347
International Application Number:	
Confirmation Number:	6856
Title of Invention:	TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS
First Named Inventor/Applicant Name:	Pierre Favrat
Customer Number:	23574
Filer:	Andrei D. Popovici
Filer Authorized By:	
Attorney Docket Number:	XCE-P005
Receipt Date:	09-OCT-2013
Filing Date:	01-JUL-2004
Time Stamp:	19:35:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 100
RAM confirmation Number	6871
Deposit Account	502888
Authorized User	POPOVICI, ANDREI

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	XCE-P005-CertificateofCorrection-09-2007-sb0044-20131009.pdf	164277 5776fd9f55139b18398b07a46074e4cb8882cc53	no	2

Warnings:

Information:

2	Request for Certificate of Correction	XCE-P005-CertificateofCorrectionRequest.pdf	71165 581dc4ea66a369060208beb6d5c160050956d273	no	1
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Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	29756 b08a3daac46fe0075cc714950361ce5fbedde95	no	2
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Warnings:

Information:

Total Files Size (in bytes):	265198
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE : 11-29-13

TO SPE OF : ART UNIT 2622

SUBJECT : Request for Certificate of Correction for Appl. No.: 10/884347 Patent No.: 7265792

CofC mailroom date: 10-09-13

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

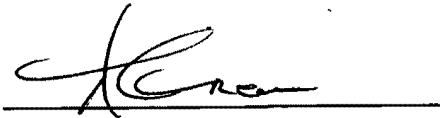
Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580



Note: _____

Angela Green 571.272.9005
CofC Branch 703-756-1814

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriate box.

☐ **Approved**

All changes apply.

☐ **Approved in Part**

Specify below which changes **do not** apply.

☐ **Denied**

State the reasons for denial below.

Comments: _____

SPE Silabs IPR Exhibit 1010
Silicon Labs v. Cresta Technology

Art Unit

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE : 11-29-13

TO SPE OF : ART UNIT 2622

SUBJECT : Request for Certificate of Correction for Appl. No.: 10/884347 Patent No.: 7265792

CofC mailroom date: 10-09-13

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square - 9D10-A
Palm Location 7580



Note: _____

Angela Green 571.272.9005
CofC Branch 703-756-1814

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriate box.

☒ **Approved**

All changes apply.

☐ **Approved in Part**

Specify below which changes **do not** apply.

☐ **Denied**

State the reasons for denial below.

Comments: Approved apply all changes

SPE /Jefferey Harold/

Art Unit 2422

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO.	DATE FILED 1/21/2014	U.S. DISTRICT COURT District of Delaware
PLAINTIFF Cresta Technology Corporation		DEFENDANT Silicon Laboratories, Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics Inc., and LG Electronics U.S.A., Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 US 7,075,585 B2	7/11/2006	Cresta Technology Corporation
2 US 7,265,792 B2	9/4/2007	Cresta Technology Corporation
3 US 7,251,466 B2	7/31/2007	Cresta Technology Corporation
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy
 Silicon Labs v. Cresta Technology
 Silabs IPR Exhibit 1010

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 1/21/2014	U.S. DISTRICT COURT District of Delaware
PLAINTIFF Cresta Technology Corporation		DEFENDANT MaxLinear, Inc., Sharp Corporation, Sharp Electronics Corporation, and VIZIO, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 US 7,075,585 B2	7/11/2006	Cresta Technology Corporation
2 US 7,265,792 B2	9/4/2007	Cresta Technology Corporation
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Silicon Copy 2—Upon filing of complaint adding patent(s), mail this copy to Director Copy 4—Case file copy
 Silabs IPR Exhibit 1010

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,265,792 B2
APPLICATION NO. : 10/884347
DATED : September 4, 2007
INVENTOR(S) : Favrat et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 11, line 1 (claim 1 line 18), insert -- filters -- after “response.”

Signed and Sealed this
Eleventh Day of March, 2014



Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office