

# EXHIBIT 1021



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**Kerth et al.**

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(54) **PARTITIONED RADIO-FREQUENCY APPARATUS AND ASSOCIATED METHODS**

(75) Inventors: **Donald A. Kerth**, Austin, TX (US); **Richard T. Behrens**, Lafayette, CO (US); **Jeffrey W. Scott**, Austin, TX (US); **G. Diwakar Vishakhadatta**, Austin, TX (US); **G. Tyson Tuttle**, Austin, TX (US); **Vishnu Shankar Srinivasan**, Austin, TX (US)

(73) Assignee: **Silicon Laboratories, Inc.**, Austin, TX (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 399 days.

(21) Appl. No.: **09/821,342**

(22) Filed: **Mar. 29, 2001**

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**Related U.S. Application Data**

(60) Provisional application No. 60/273,119, filed on Mar. 2, 2001, and provisional application No. 60/261,506, filed on Jan. 12, 2001.

(51) **Int. Cl.**<sup>7</sup> ..... **H04B 1/40**

(52) **U.S. Cl.** ..... **455/88; 455/74; 455/552.1; 455/114.2; 455/86**

(58) **Field of Search** ..... 455/74, 77, 86, 455/78, 83, 87, 88, 553.1, 556.1, 557, 141, 144, 147, 232.1, 223, 187.1, 189.1, 991.1, 191.3, 164.2, 333, 334, 127.4, 296, 300, 301; 375/334, 316, 322

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*Primary Examiner*—Nay Maung

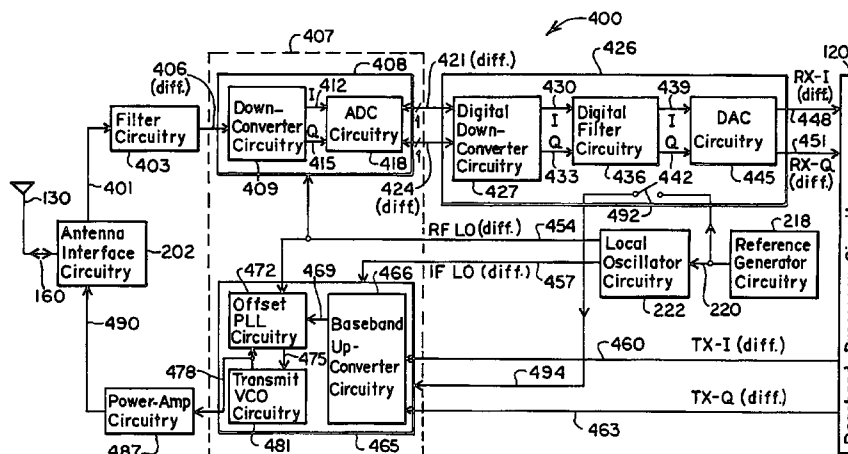
*Assistant Examiner*—John J Lee

(74) *Attorney, Agent, or Firm*—O'Keefe, Egan & Peterman, L.L.P.

(57) **ABSTRACT**

Radio-frequency (RF) apparatus includes receiver analog circuitry that receives an RF signal and provides at least one digital signal to receiver digital circuitry that functions in cooperation with the receiver analog circuitry. The receiver analog circuitry and the receiver digital circuitry are partitioned so that interference effects between the receiver analog circuitry and the receiver digital circuitry tend to be reduced.

**38 Claims, 19 Drawing Sheets**



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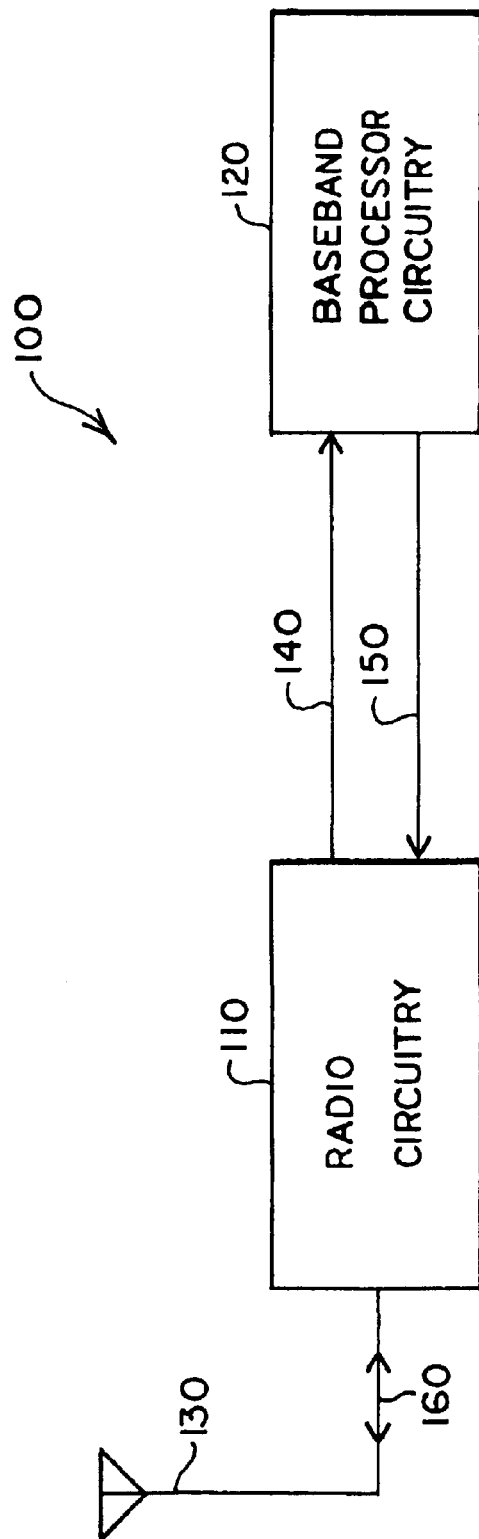


FIG. 1

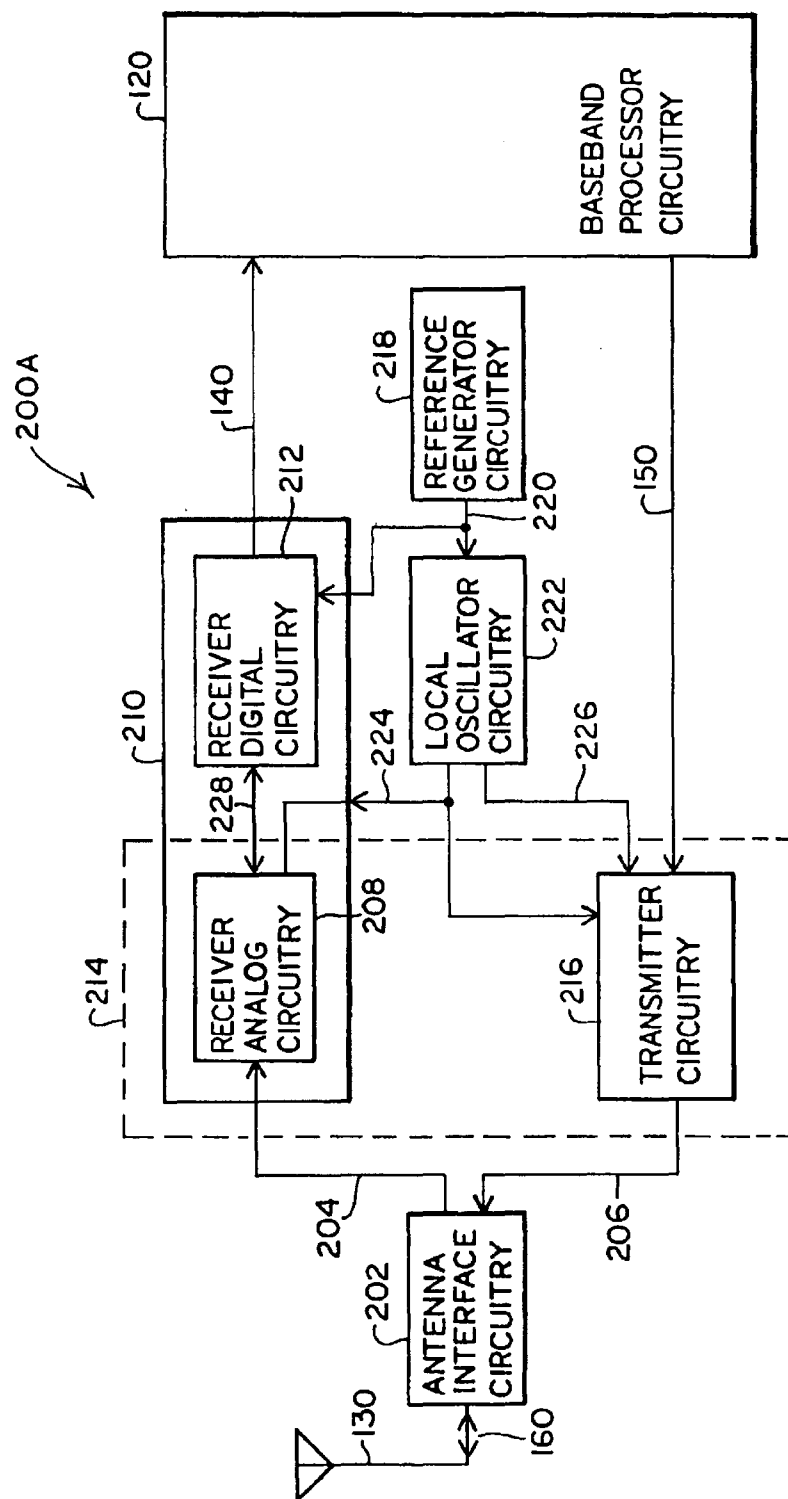


FIG. 2A

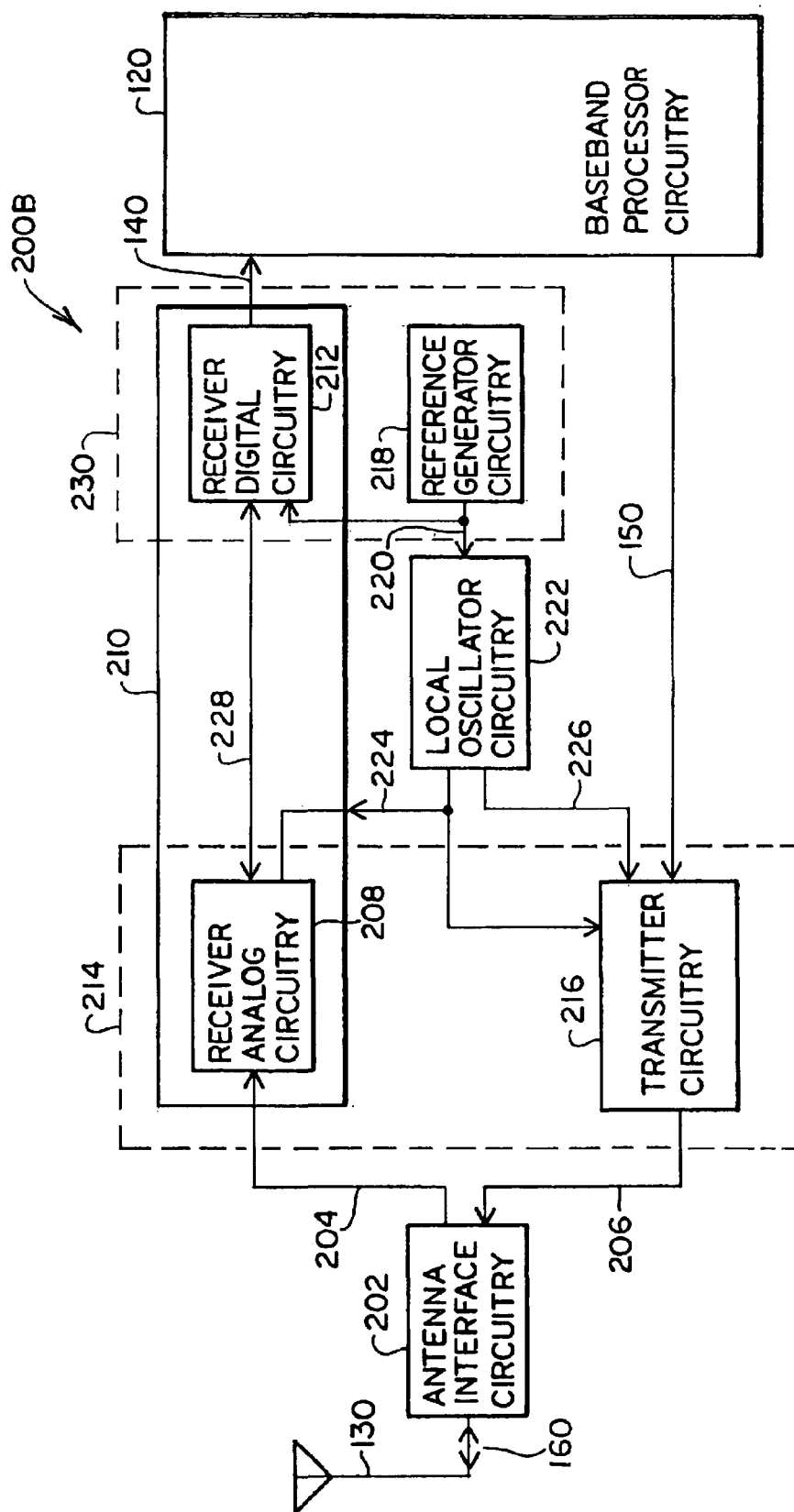


FIG. 2B



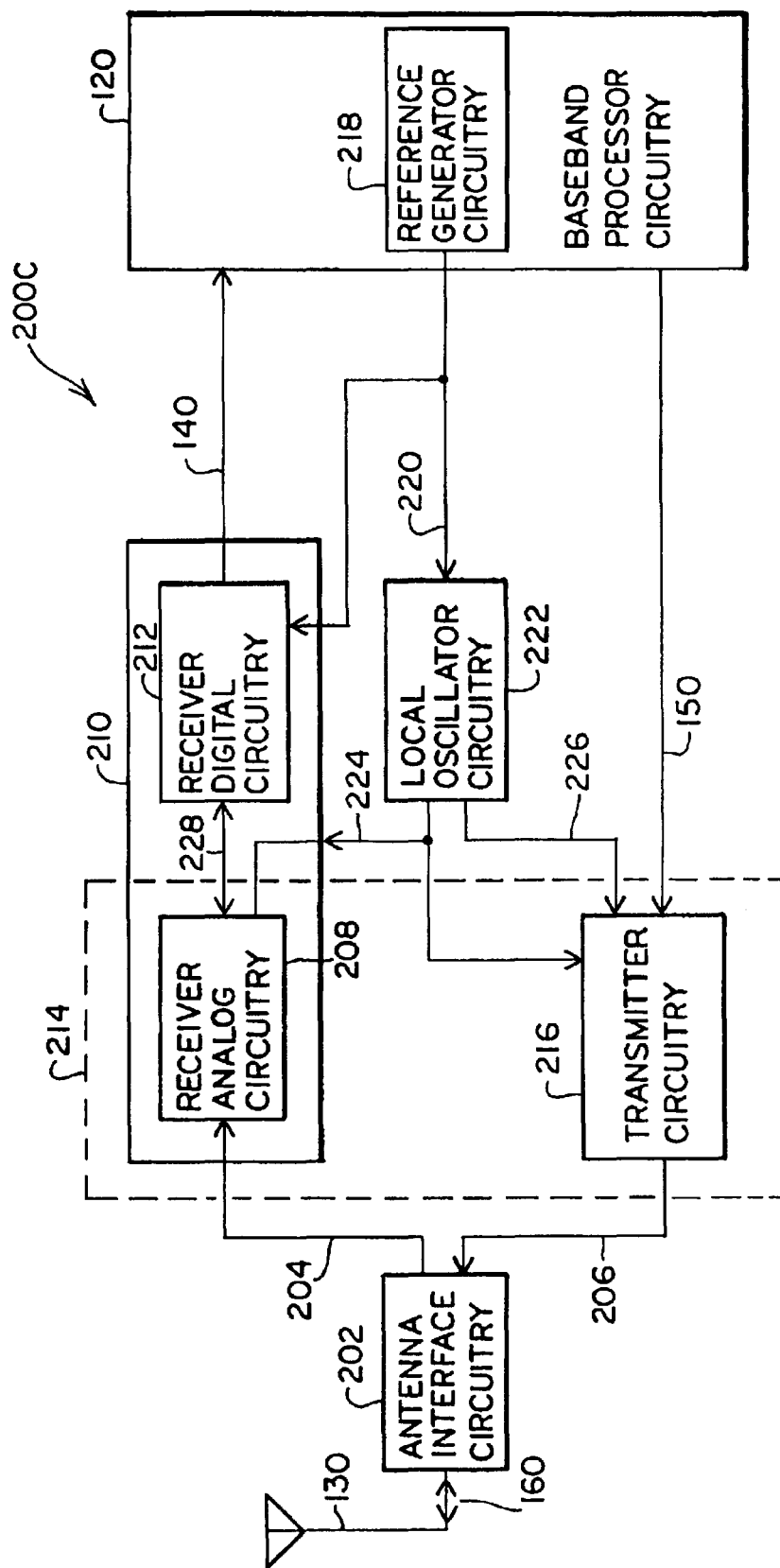


FIG. 2C

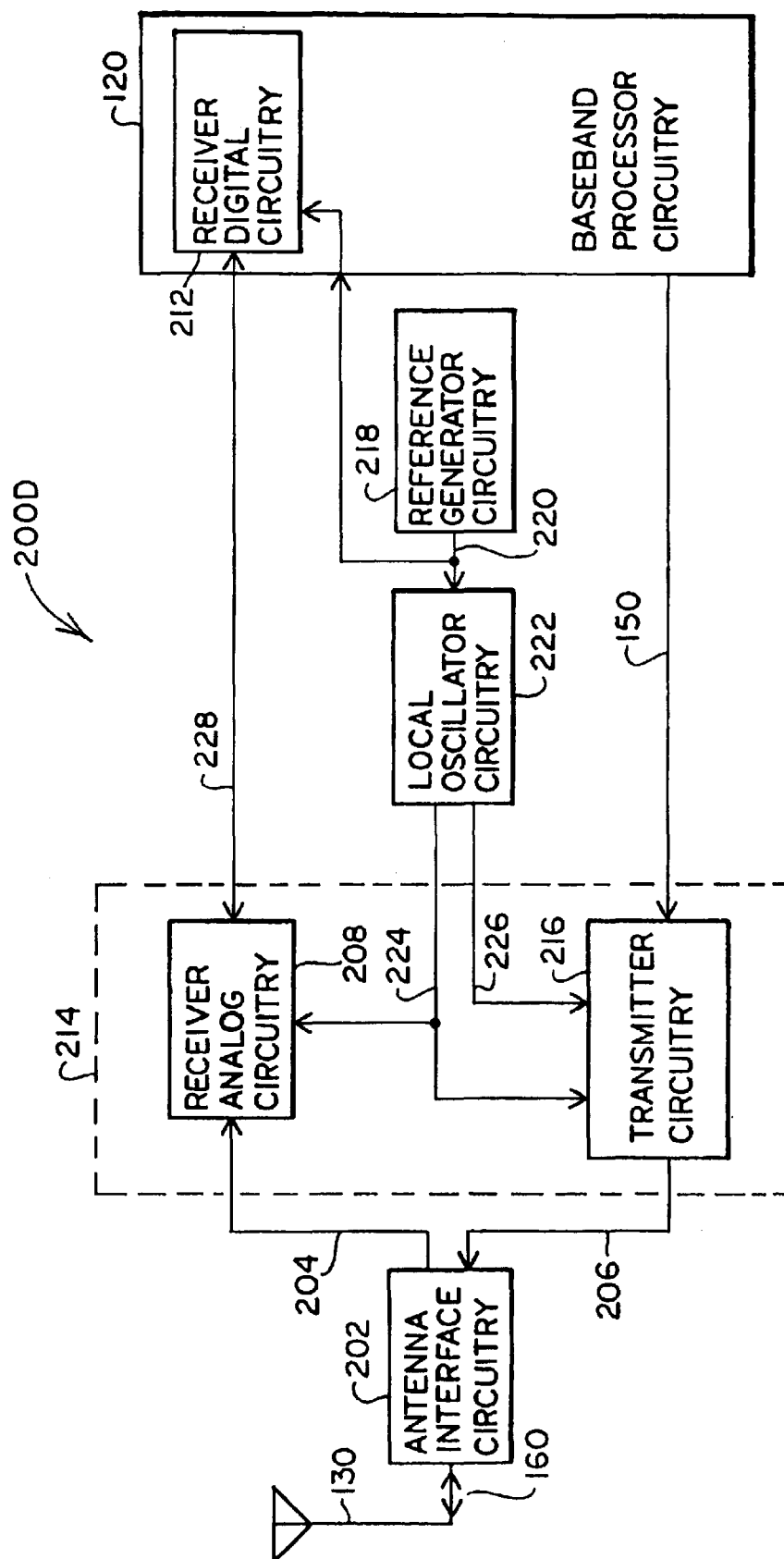


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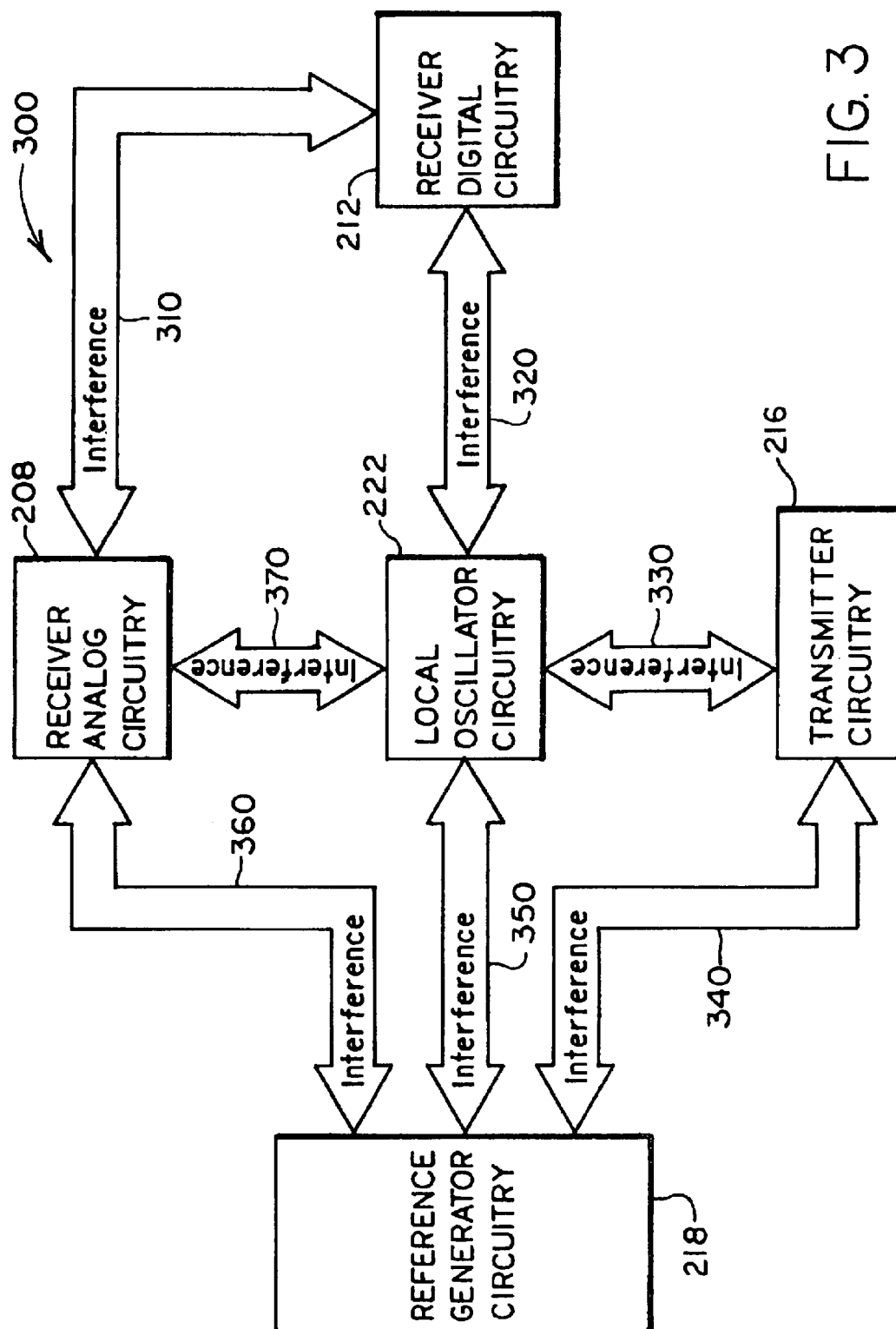


FIG. 3

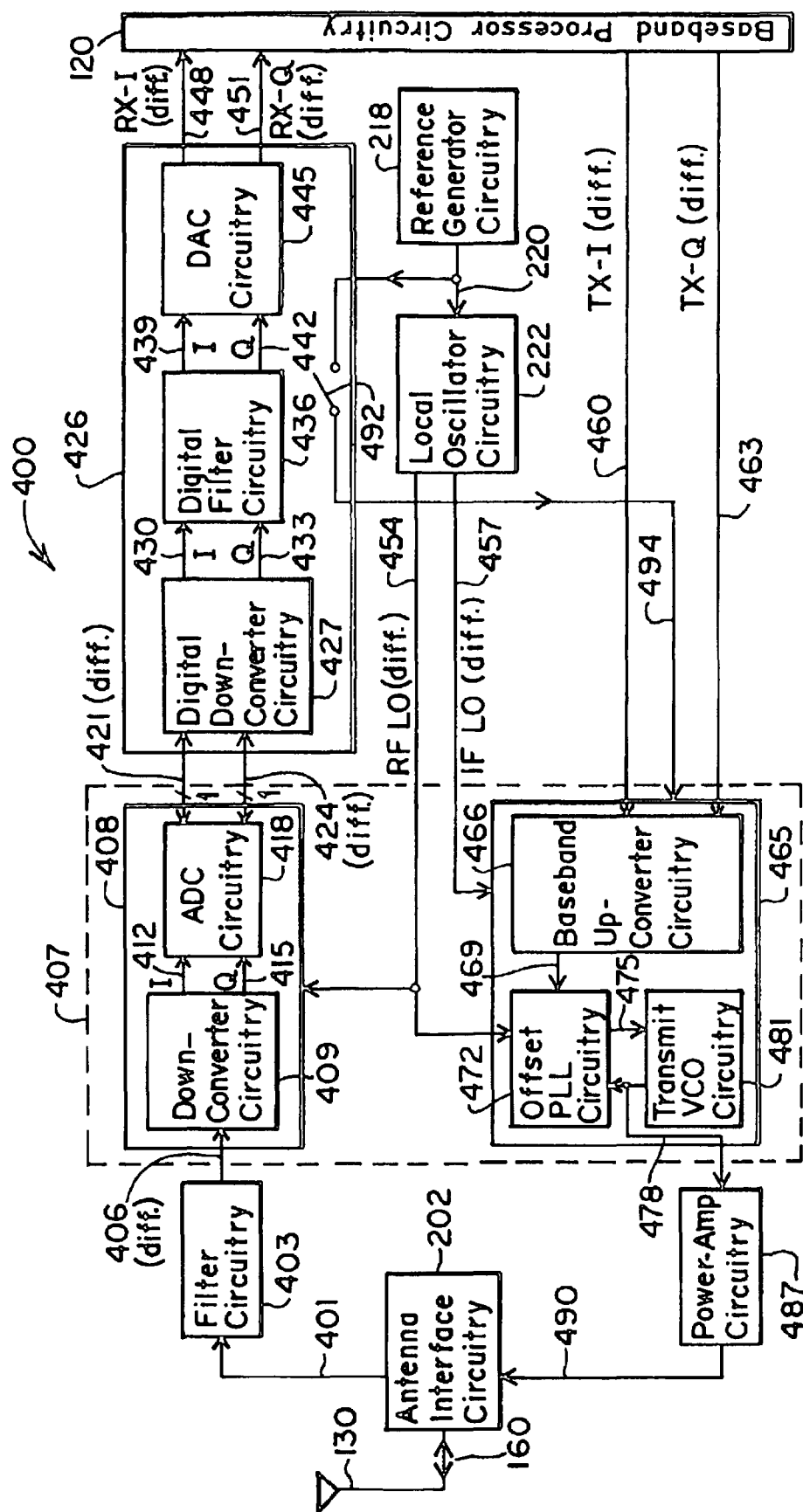


FIG. 4

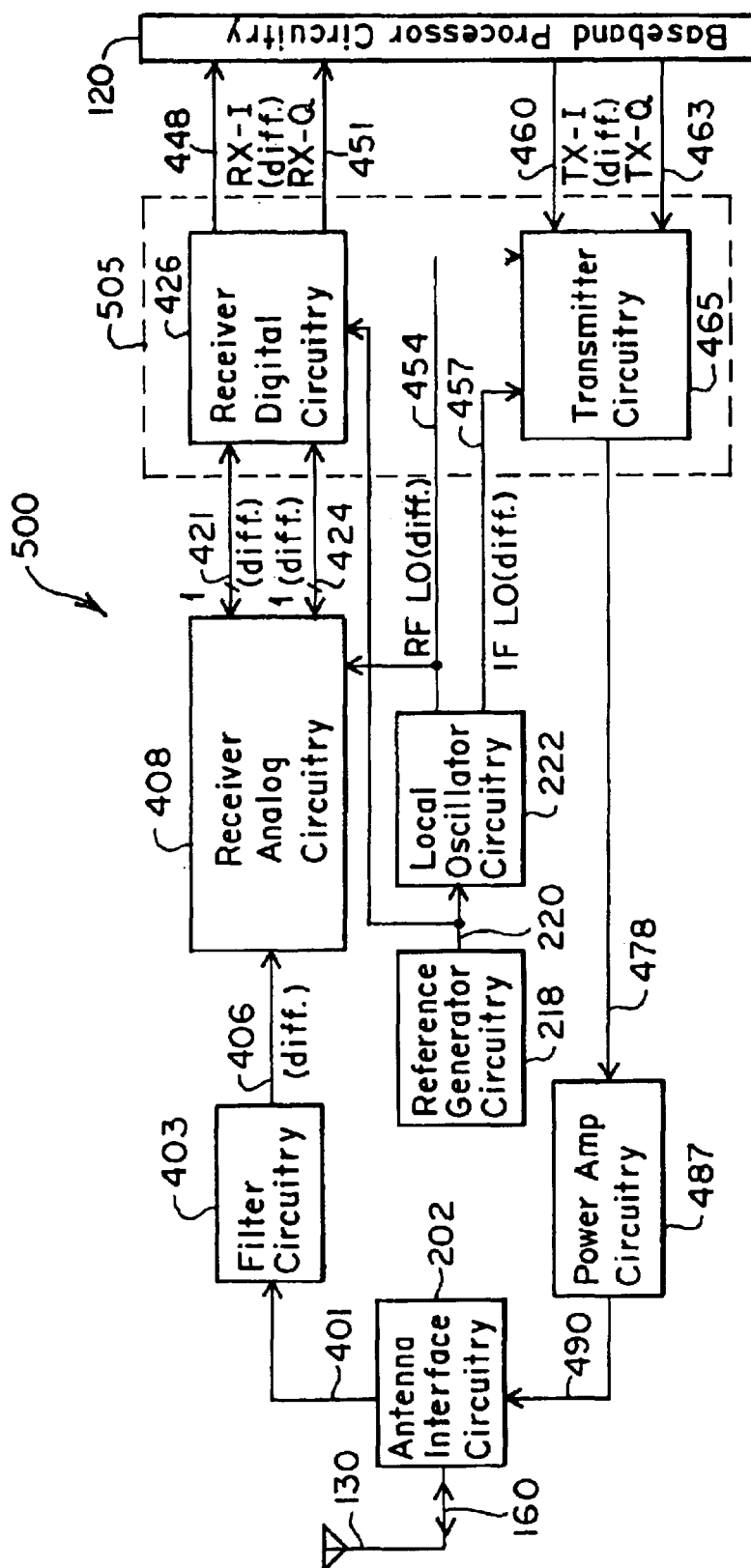


FIG. 5

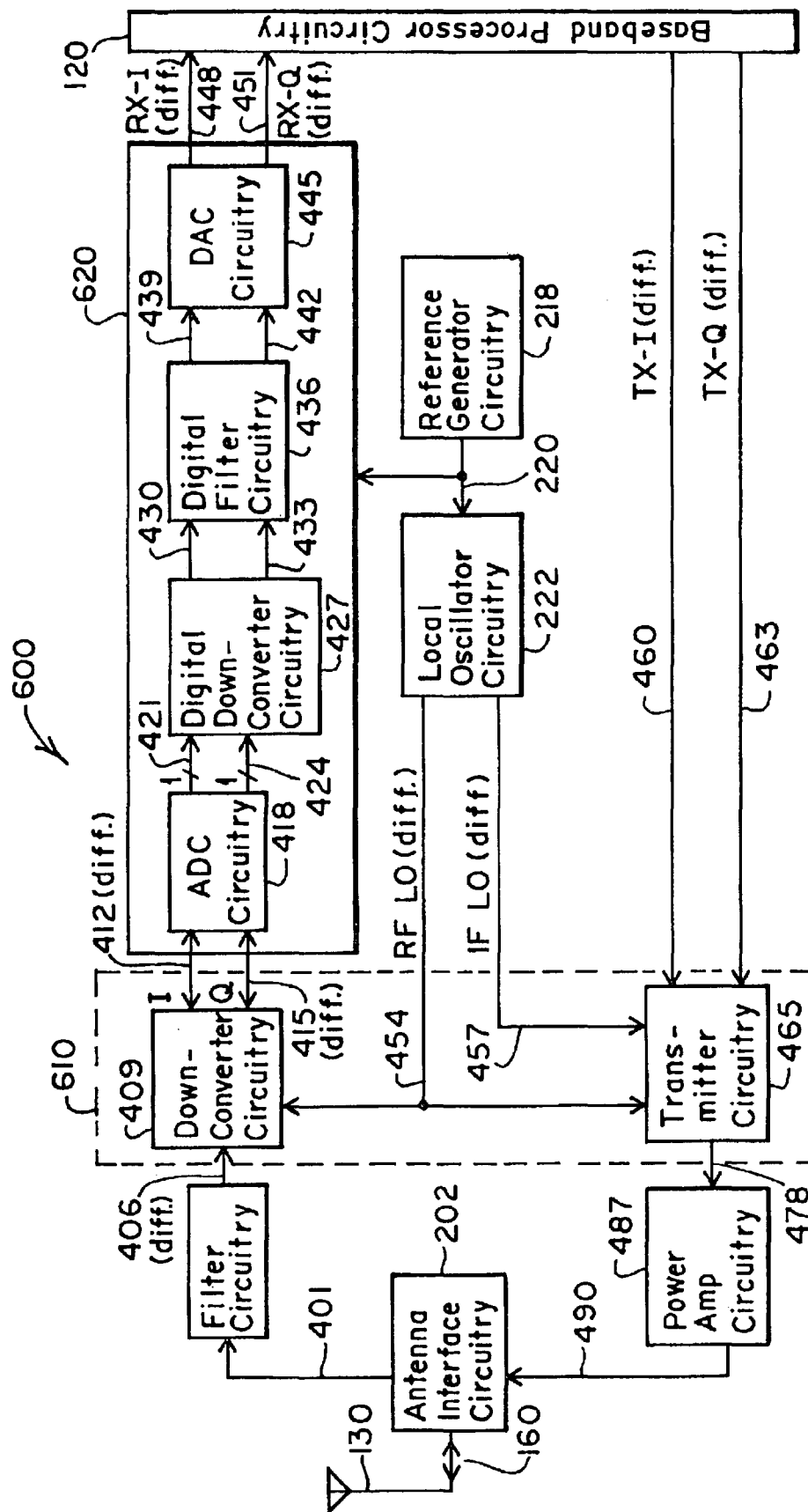


FIG. 6

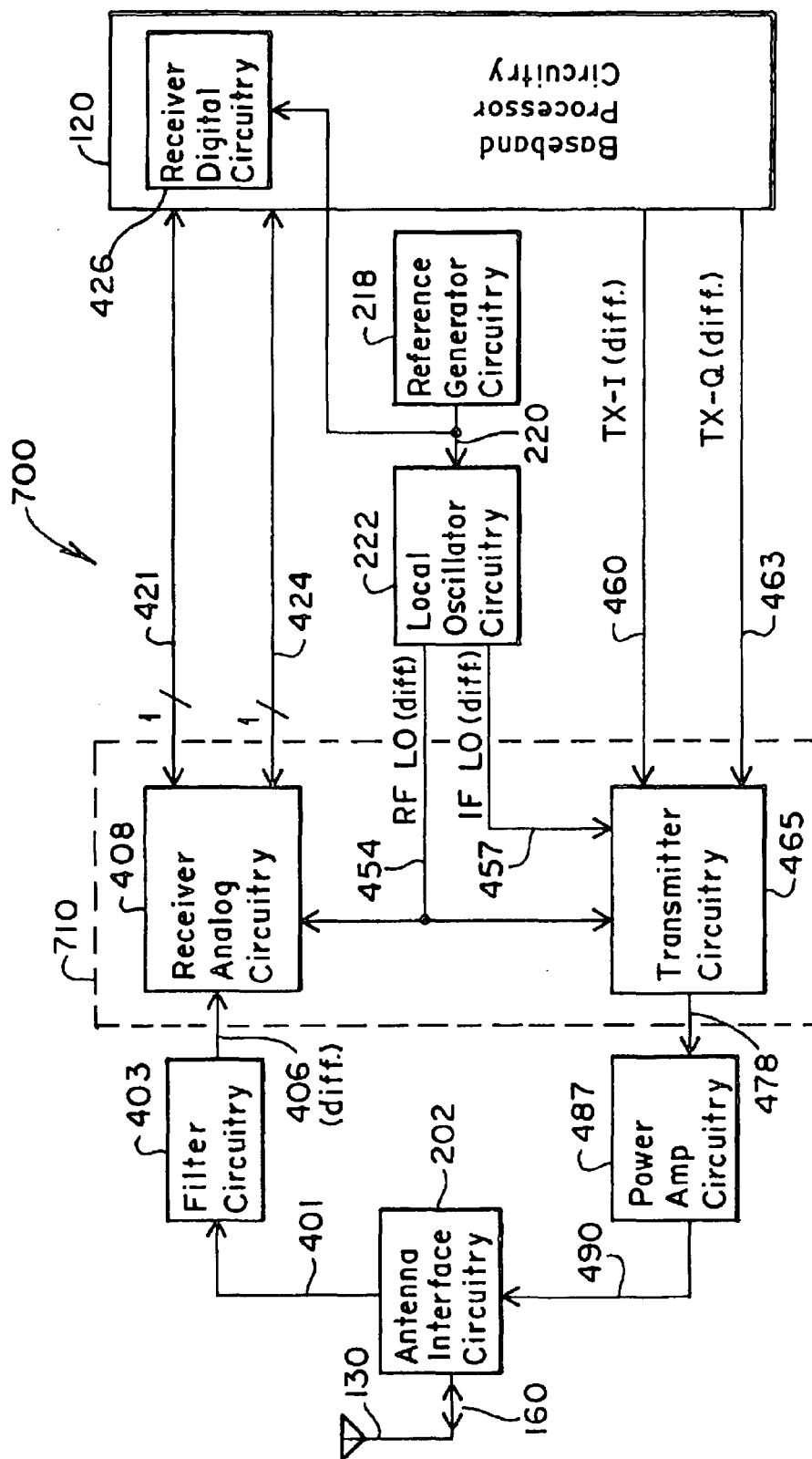


FIG. 7

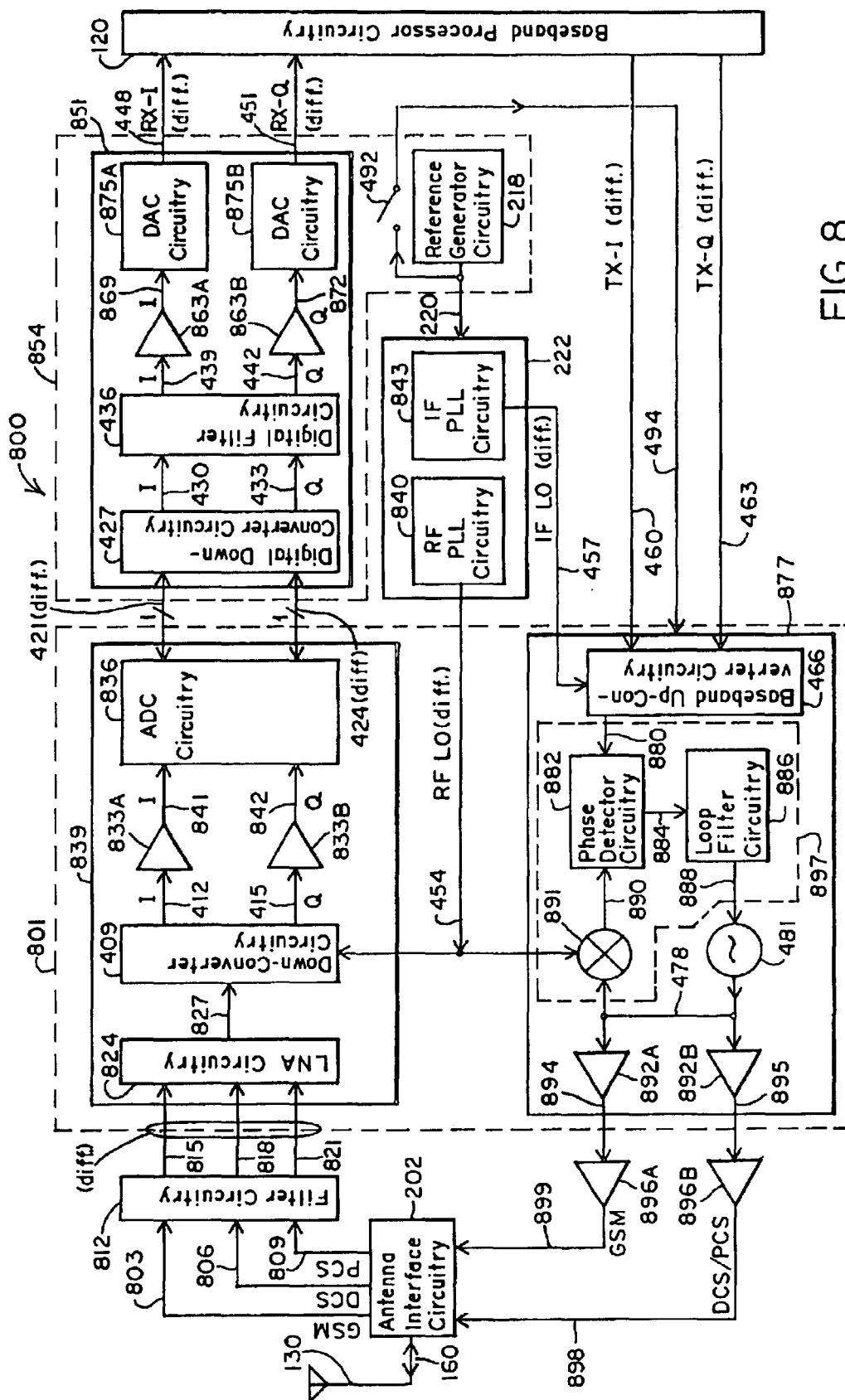


FIG. 8



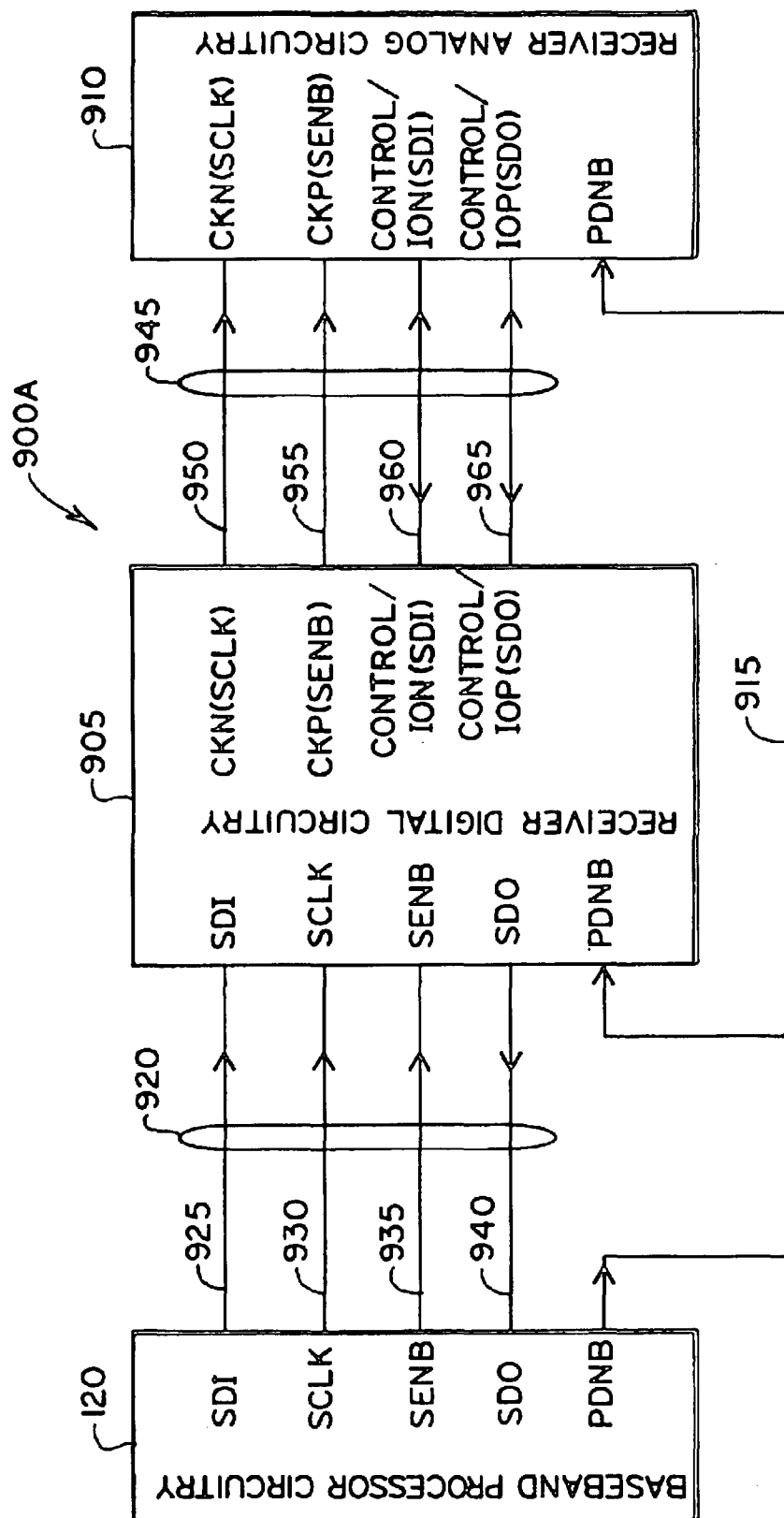


FIG. 9A

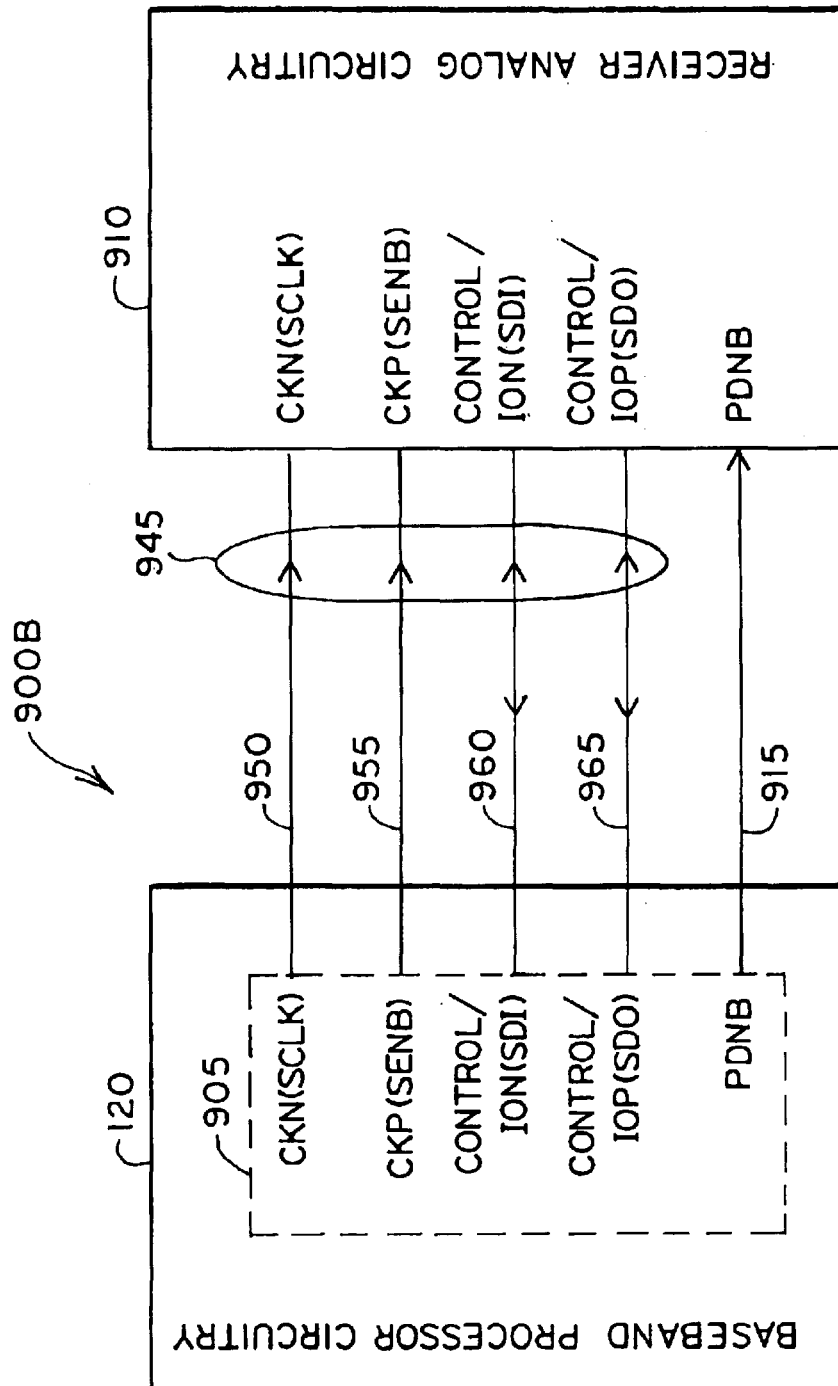
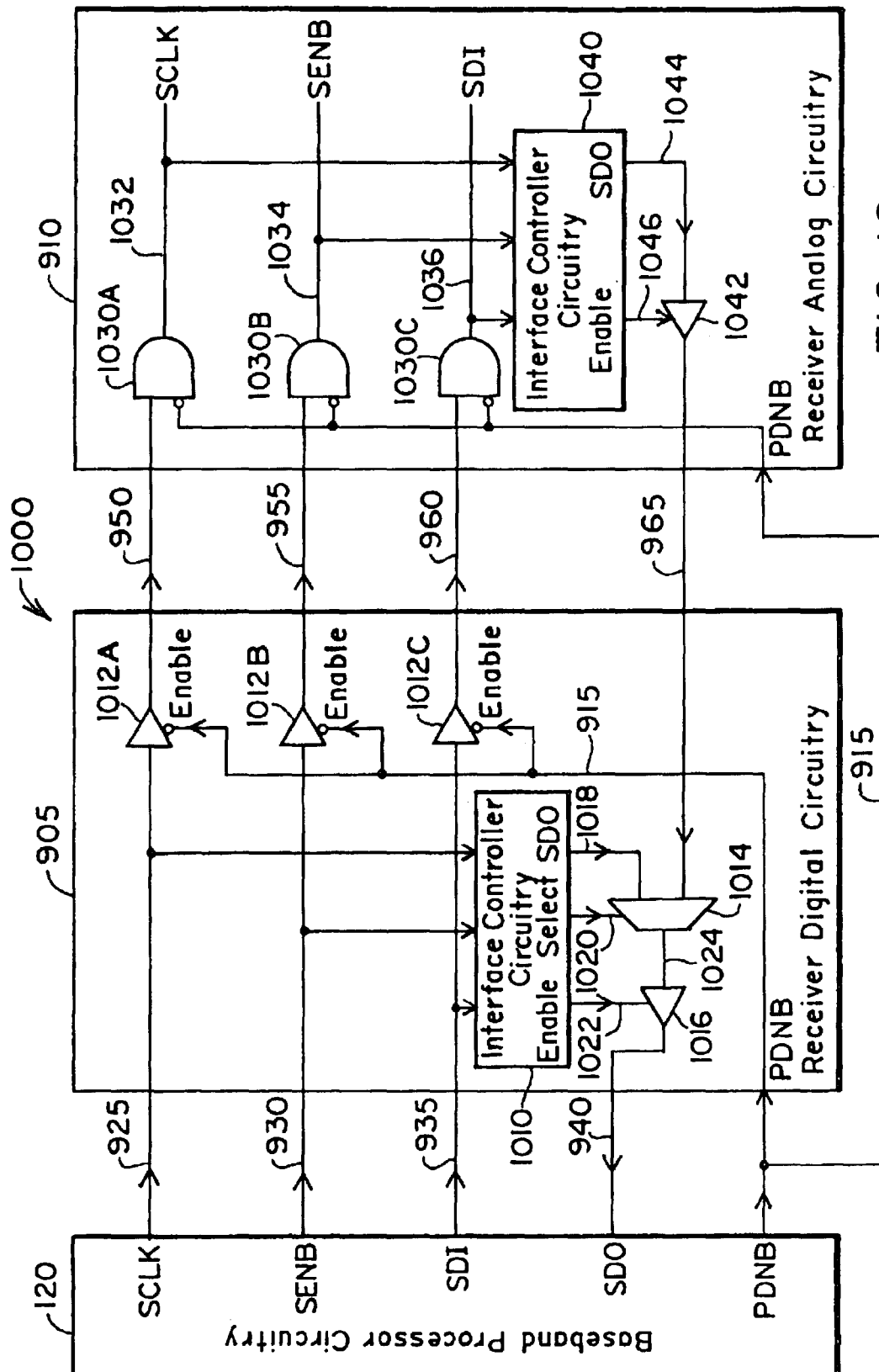


FIG. 9B



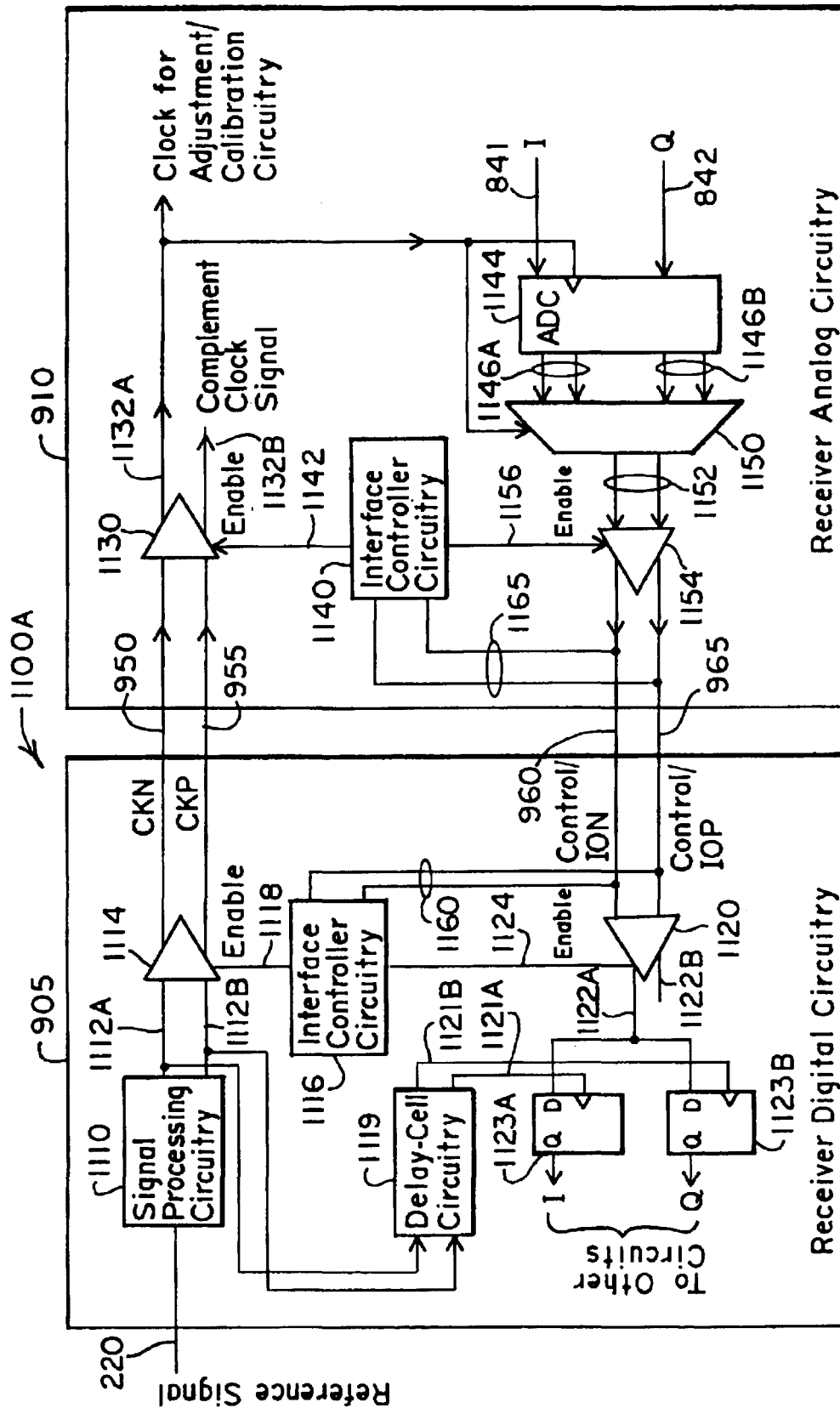


FIG. 11A

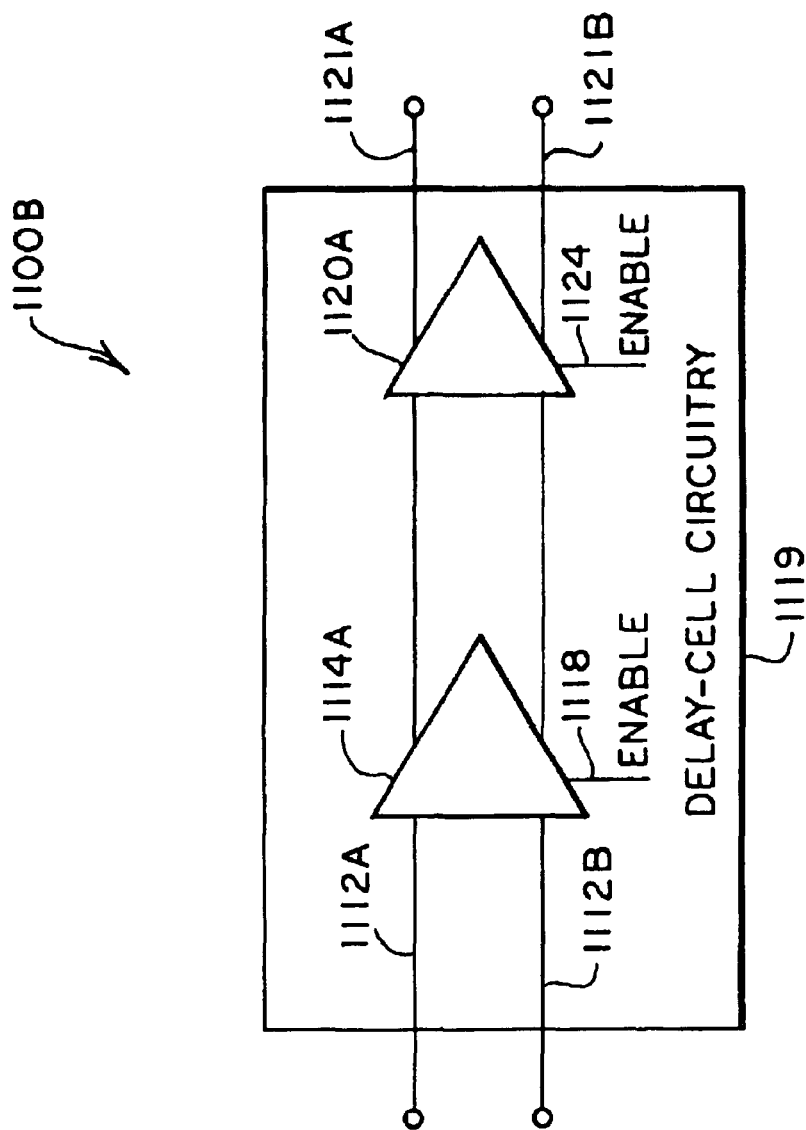


FIG. 11B

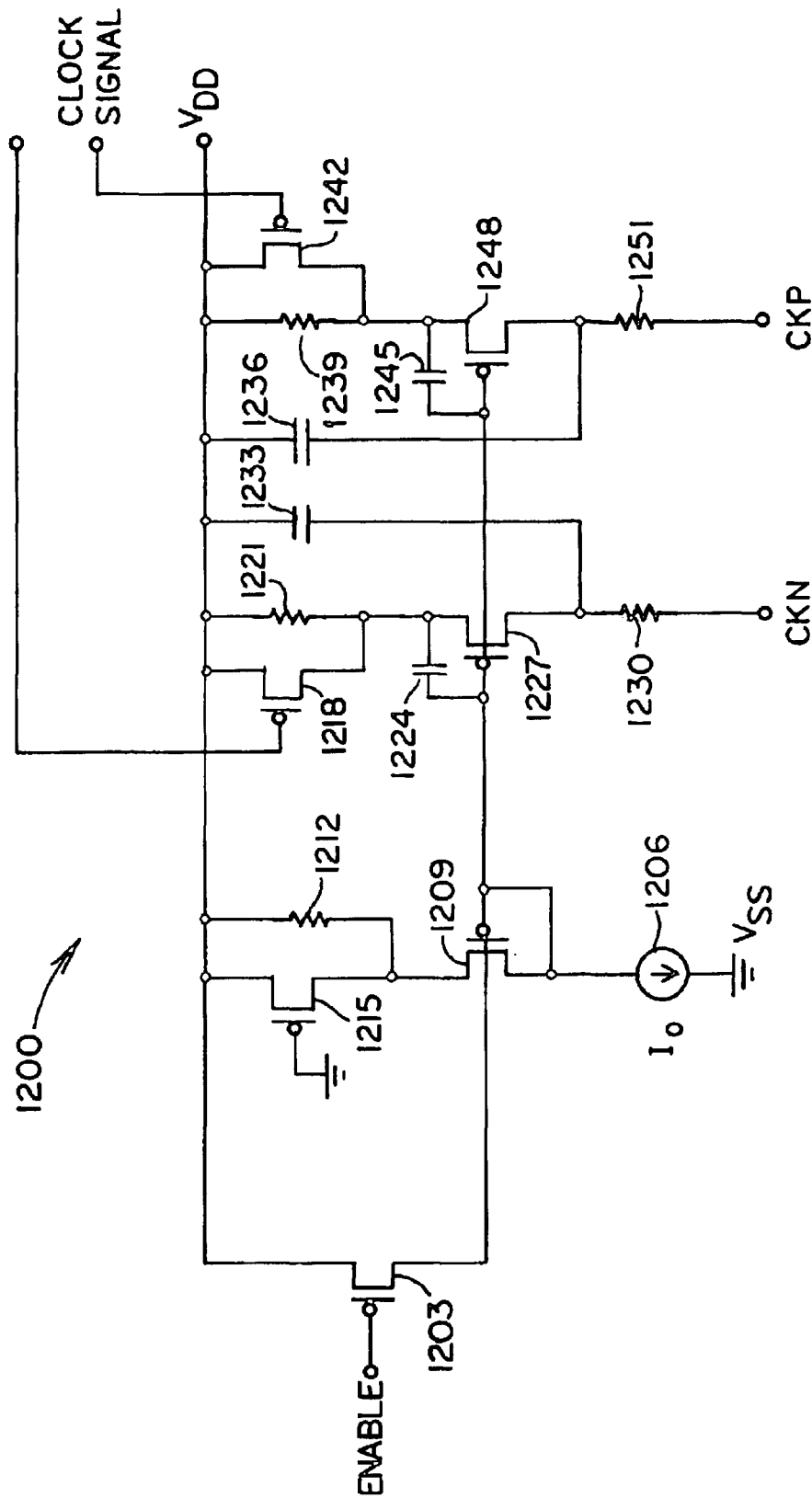


FIG. 12

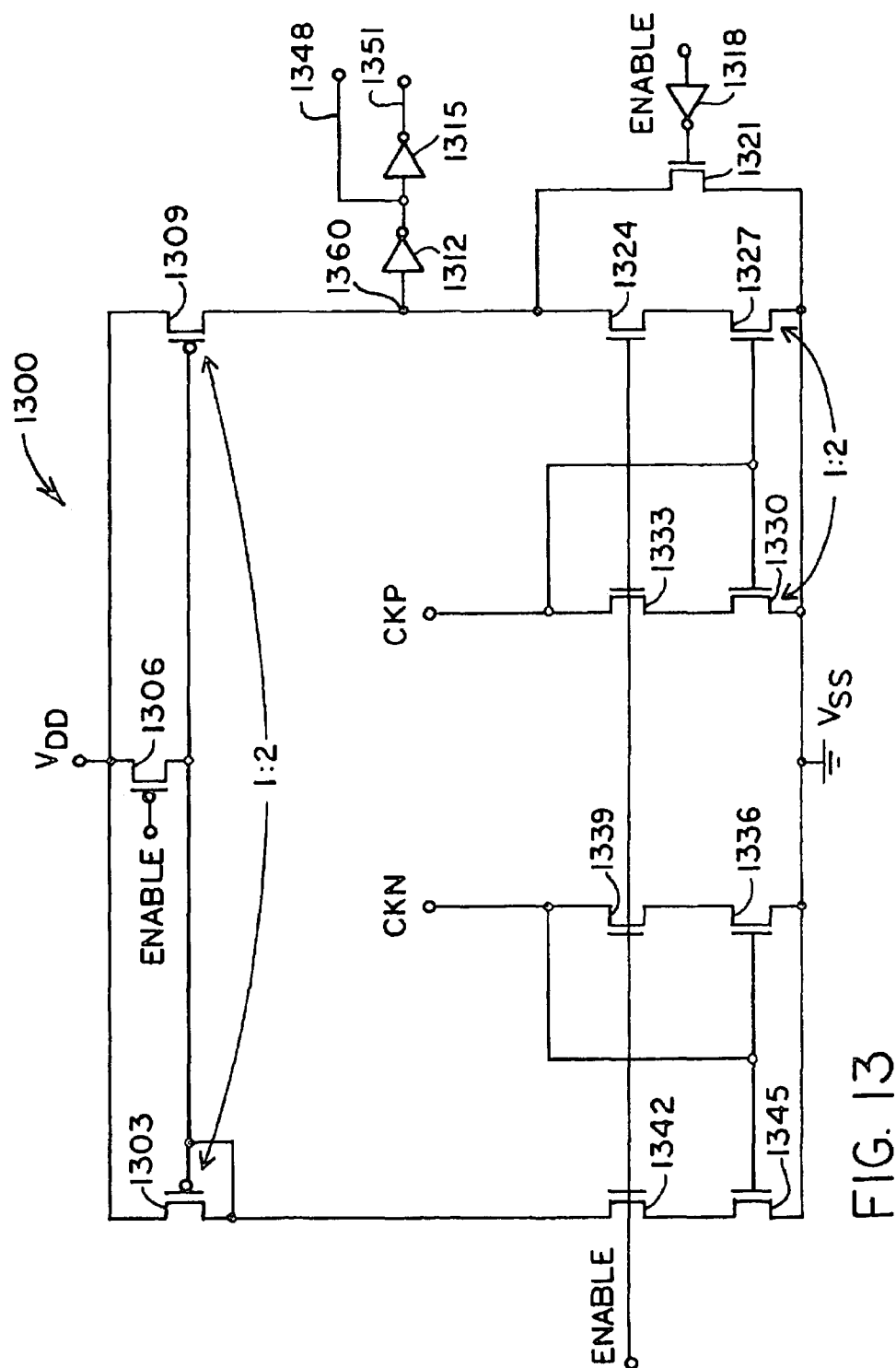


FIG. 13

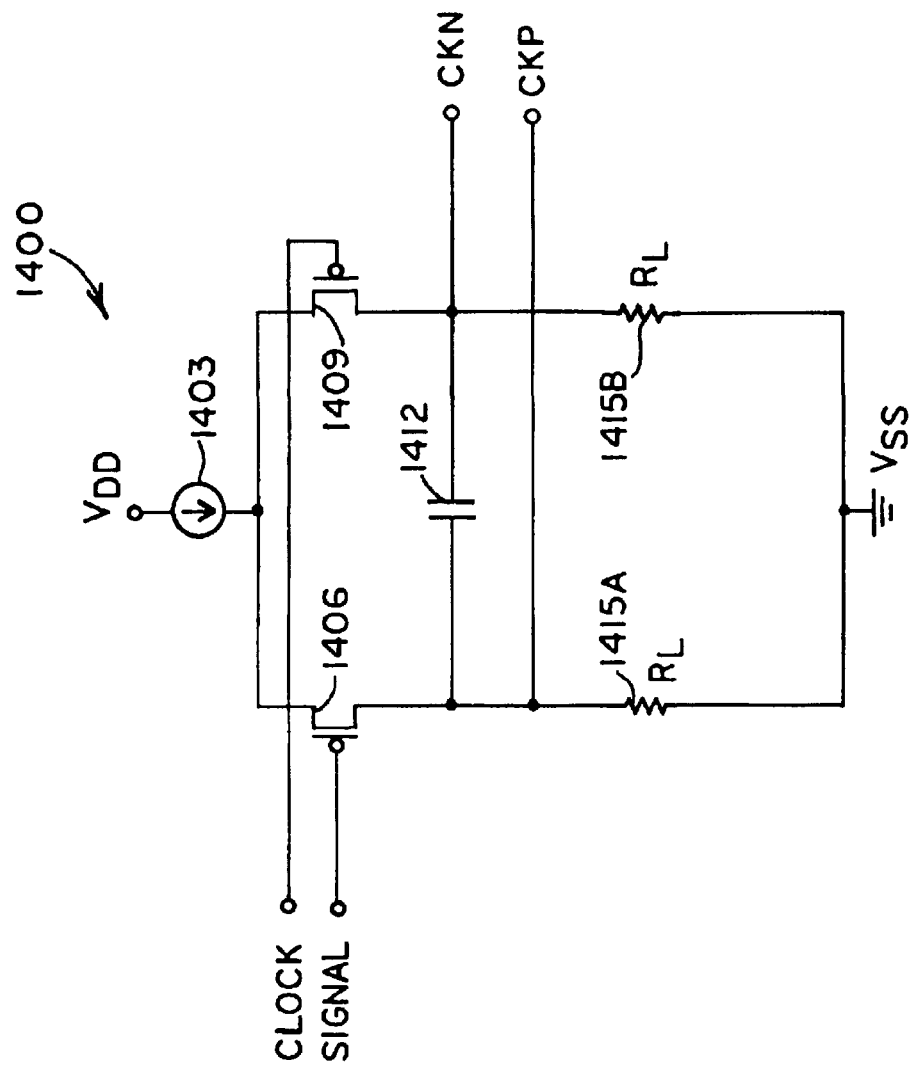


FIG. 14



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## PARTITIONED RADIO-FREQUENCY APPARATUS AND ASSOCIATED METHODS

### CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application claims priority to Provisional U.S. patent application Ser. No. 60/261,506, filed on Jan. 12, 2001. This patent application further claims priority to Provisional U.S. patent application Ser. No. 60/273,119, titled "Partitioned RF Apparatus with Digital Interface and Associated Methods," filed on Mar. 2, 2001. This patent application incorporates by reference the above provisional patent applications in their entirety.

Furthermore, this patent application relates to concurrently filed, commonly owned U.S. patent application Ser. No. 09/821,340, titled "Digital Interface in Radio-Frequency Apparatus and Associated Methods."

### TECHNICAL FIELD OF THE INVENTION

This invention relates to radio-frequency (RF) receivers and transceivers. More particularly, the invention concerns (i) ways of partitioning high-performance RF receiver or transceiver circuitry into circuit partitions so as to reduce interference effects among the circuit partitions, and (ii) circuits and protocols that facilitate interfacing among the circuit partitions.

### BACKGROUND

The proliferation and popularity of mobile radio and telephony applications has led to market demand for communication systems with low cost, low power, and small form-factor radio-frequency (RF) transceivers. As a result, recent research has focused on providing monolithic transceivers using low-cost complementary metal-oxide semiconductor (CMOS) technology. Current research has focused on providing an RF transceiver within a single integrated circuit (IC). For discussions of the research efforts and the issues surrounding the integration of RF transceivers, see Jacques C. Rudell et al., *Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems*, INVITED PAPER AT THE 1998 INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS, MONTEREY, CALIFORNIA; Asad A. Abidi, *CMOS Wireless Transceivers: The New Wave*, IEEE COMMUNICATIONS MAG., August 1999, at 119; Jan Crols & Michael S. J. Steyaert, 45 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING 269 (1998); and Jacques C. Rudell et al., *A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications*, 32 IEEE J. OF SOLID-STATE CIRCUITS 2071 (1997), all incorporated by reference here in their entireties.

The integration of transceiver circuits is not a trivial problem, as it must take into account the requirements of the transceiver's circuitry and the communication standards governing the transceiver's operation. From the perspective of the transceiver's circuitry, RF transceivers typically include sensitive components susceptible to noise and interference with one another and with external sources. Integrating the transceiver's circuitry into one integrated circuit would exacerbate interference among the various blocks of the transceiver's circuitry. Moreover, communication standards governing RF transceiver operation outline a set of requirements for noise, inter-modulation, blocking

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performance, output power, and spectral emission of the transceiver. Unfortunately, no method for addressing all of the above issues in high-performance RF receivers or transceivers, for example, RF transceivers used in cellular and telephony applications, has been developed. A need therefore exists for techniques of partitioning and integrating RF receivers or transceivers that would provide low-cost, low form-factor RF transceivers for high-performance applications, for example, in cellular handsets.

### SUMMARY OF THE INVENTION

This invention provides techniques for partitioning radio-frequency (RF) apparatus, for example, receivers or transceivers. In one embodiment, the RF apparatus comprises a first circuit partition that includes receiver analog circuitry that is configured to produce a digital receive signal from an analog radio-frequency signal. The RF apparatus also comprises a second circuit partition that includes receiver digital circuitry that is configured to accept the digital receive signal. The first and second circuit partitions are partitioned so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

In another embodiment, an RF transceiver according to the invention comprises a first circuit partition that includes receiver analog circuitry that is configured to accept a received RF signal and to provide at least one digital output signal. The first circuit partition also includes transmitter circuitry that is configured to receive at least one transmit input signal and to provide a transmit RF signal. The RF transceiver also comprises a second circuit partition that includes local-oscillator circuitry that is configured to accept a reference signal. The local oscillator circuitry is further configured to provide a radio-frequency (RF) signal to the receiver analog circuitry. The first circuit partition and the second circuit partition are partitioned so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

Another aspect of the invention relates to methods of partitioning RF apparatus, for example, receivers and transceivers. In one embodiment, the method includes providing a first circuit partition that comprises receiver analog circuitry, and utilizing the receiver analog circuitry to produce a digital receive signal from an analog RF signal. The method also includes providing a second circuit partition that comprises receiver digital circuitry, and utilizing the receiver digital circuitry to accept the digital receive signal. Finally, the method includes partitioning the first and second circuit partitions so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

In another embodiment, a method of partitioning an RF transceiver includes providing a first circuit partition that includes receiver analog circuitry and transmitter circuitry. The method further includes utilizing the receiver analog circuitry to accept a received RF signal and to provide at least one digital output signal, and utilizing the transmitter circuitry to receive at least one transmit input signal and to provide a transmit RF signal. The method also comprises providing a second circuit partition that includes local-oscillator circuitry, and utilizing the local-oscillator circuitry to accept a reference signal, and to provide a radio-frequency (RF) signal to the receiver analog circuitry. Finally, the method includes partitioning the first circuit partition and the second circuit partition so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

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## DESCRIPTION OF THE DRAWINGS

The appended drawings illustrate only exemplary embodiments of the invention and therefore do not limit its scope. The disclosed inventive concepts lend themselves to other equally effective embodiments. In the drawings, the same numerals used in more than one drawing denote the same, similar, or equivalent functionality, components, or blocks.

FIG. 1 illustrates the block diagram of an RF transceiver. The RF transceiver includes radio circuitry that operates in conjunction with baseband processor circuitry.

FIG. 2A shows RF transceiver circuitry partitioned according to the invention.

FIG. 2B depicts another embodiment of RF transceiver circuitry partitioned according to the invention. In this embodiment, the reference generator resides within the same circuit partition, or circuit block, as does the receiver digital circuitry.

FIG. 2C illustrates yet another embodiment of RF transceiver circuitry partitioned according to invention. In this embodiment, the reference generator circuitry resides within the baseband processor circuitry.

FIG. 2D shows another embodiment of RF transceiver circuitry partitioned according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 3 illustrates interference mechanisms among the various blocks of an RF transceiver. The embodiments of the invention in FIGS. 2A–2D, depicting RF transceivers partitioned according to the invention, seek to overcome, reduce, or minimize those interference mechanisms.

FIG. 4 shows a more detailed block diagram of RF transceiver circuitry partitioned according to the invention.

FIG. 5 illustrates an alternative technique for partitioning RF transceiver circuitry.

FIG. 6 shows yet another alternative technique for partitioning RF transceiver circuitry.

FIG. 7 depicts a more detailed block diagram of RF transceiver circuitry partitioned according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 8 illustrates a more detailed block diagram of a multi-band RF transceiver circuitry partitioned according to the invention.

FIG. 9A shows a block diagram of an embodiment of the interface between the receiver digital circuitry and receiver analog circuitry in an RF transceiver according to the invention.

FIG. 9B depicts a block diagram of another embodiment of the interface between the baseband processor circuitry and the receiver analog circuitry in an RF transceiver according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 10 illustrates a more detailed block diagram of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a serial interface.

FIG. 11A shows a more detailed block diagram of an embodiment of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a data and clock signal interface.

FIG. 11B illustrates a block diagram of an embodiment of a delay-cell circuitry that includes a clock driver circuitry in tandem with a clock receiver circuitry.

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FIG. 12 depicts a schematic diagram of an embodiment of a signal-driver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

FIG. 13 illustrates a schematic diagram of an embodiment of signal-receiver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

FIG. 14 shows a schematic diagram of another signal-driver circuitry that one may use to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

## DETAILED DESCRIPTION OF THE INVENTION

This invention in part contemplates partitioning RF apparatus so as to provide highly integrated, high-performance, low-cost, and low form-factor RF solutions. One may use RF apparatus according to the invention in high-performance communication systems. More particularly, the invention in part relates to partitioning RF receiver or transceiver circuitry in a way that minimizes, reduces, or overcomes interference effects among the various blocks of the RF receiver or transceiver, while simultaneously satisfying the requirements of the standards that govern RF receiver or transceiver performance. Those standards include the Global System for Mobile (GSM) communication, Personal Communication Services (PCS), Digital Cellular System (DCS), Enhanced Data for GSM Evolution (EDGE), and General Packet Radio Services (GPRS). RF receiver or transceiver circuitry partitioned according to the invention therefore overcomes interference effects that would be present in highly integrated RF receivers or transceivers while meeting the requirements of the governing standards at low cost and with a low form-factor. The description of the invention refers to circuit partition and circuit block interchangeably.

FIG. 1 shows the general block diagram of an RF transceiver circuitry **100** according to the invention. The RF transceiver circuitry **100** includes radio circuitry **110** that couples to an antenna **130** via a bi-directional signal path **160**. The radio circuitry **110** provides an RF transmit signal to the antenna **130** via the bi-directional signal path **160** when the transceiver is in transmit mode. When in the receive mode, the radio circuitry **110** receives an RF signal from the antenna **130** via the bi-directional signal path **160**.

The radio circuitry **110** also couples to a baseband processor circuitry **120**. The baseband processor circuitry **120** may comprise a digital-signal processor (DSP). Alternatively, or in addition to the DSP, the baseband processor circuitry **120** may comprise other types of signal processor, as persons skilled in the art would understand. The radio circuitry **110** processes the RF signals received from the antenna **130** and provides receive signals **140** to the baseband processor circuitry **120**. In addition, the radio circuitry **110** accepts transmit input signals **150** from the baseband processor **120** and provides the RF transmit signals to the antenna **130**.

FIGS. 2A–2D show various embodiments of RF transceiver circuitry partitioned according to the invention. FIG. 3 and its accompanying description below make clear the considerations that lead to the partitioning of the RF transceiver circuitry as shown in FIGS. 2A–2D. FIG. 2A illustrates an embodiment **200A** of an RF transceiver circuitry partitioned according to the invention. In addition to the elements described in connection with FIG. 1, the RF

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transceiver **200A** includes antenna interface circuitry **202**, receiver circuitry **210**, transmitter circuitry **216**, reference generator circuitry **218**, and local oscillator circuitry **222**.

The reference generator circuitry **218** produces a reference signal **220** and provides that signal to the local oscillator circuitry **222** and to receiver digital circuitry **212**. The reference signal **220** preferably comprises a clock signal, although it may include other signals, as desired. The local oscillator circuitry **222** produces an RF local oscillator signal **224**, which it provides to receiver analog circuitry **208** and to the transmitter circuitry **216**. The local oscillator circuitry **222** also produces a transmitter intermediate-frequency (IF) local oscillator signal **226** and provides that signal to the transmitter circuitry **216**. Note that, in RF transceivers according to the invention, the receiver analog circuitry **208** generally comprises mostly analog circuitry in addition to some digital or mixed-mode circuitry, for example, analog-to-digital converter (ADC) circuitry and circuitry to provide an interface between the receiver analog circuitry and the receiver digital circuitry, as described below.

The antenna interface circuitry **202** facilitates communication between the antenna **130** and the rest of the RF transceiver. Although not shown explicitly, the antenna interface circuitry **202** may include a transmit/receive mode switch, RF filters, and other transceiver front-end circuitry, as persons skilled in the art would understand. In the receive mode, the antenna interface circuitry **202** provides RF receive signals **204** to the receiver analog circuitry **208**. The receiver analog circuitry **208** uses the RF local oscillator signal **224** to process (e.g., down-convert) the RF receive signals **204** and produce a processed analog signal. The receiver analog circuitry **208** converts the processed analog signal to digital format and supplies the resulting digital receive signals **228** to the receiver digital circuitry **212**. The receiver digital circuitry **212** further processes the digital receive signals **228** and provides the resulting receive signals **140** to the baseband processor circuitry **120**.

In the transmit mode, the baseband processor circuitry **120** provides transmit input signals **150** to the transmitter circuitry **216**. The transmitter circuitry **216** uses the RF local oscillator signal **224** and the transmitter IF local oscillator signal **226** to process the transmit input signals **150** and to provide the resulting transmit RF signal **206** to the antenna interface circuitry **202**. The antenna interface circuitry **202** may process the transmit RF signal further, as desired, and provide the resulting signal to the antenna **130** for propagation into a transmission medium.

The embodiment **200A** in FIG. 2A comprises a first circuit partition, or circuit block, **214** that includes the receiver analog circuitry **208** and the transmitter circuitry **216**. The embodiment **200A** also includes a second circuit partition, or circuit block, that includes the receiver digital circuitry **212**. The embodiment **200A** further includes a third circuit partition, or circuit block, that comprises the local oscillator circuitry **222**. The first circuit partition **214**, the second circuit partition **212**, and the third circuit partition **222** are partitioned from one another so that interference effects among the circuit partitions tend to be reduced. The first, second, and third circuit partitions preferably each reside within an integrated circuit device. In other words, preferably the receiver analog circuitry **208** and the transmitter circuitry **216** reside within an integrated circuit device, the receiver digital circuitry **212** resides within another integrated circuit device, and the local oscillator circuitry **222** resides within a third integrated circuit device.

FIG. 2B shows an embodiment **200B** of an RF transceiver circuitry partitioned according to the invention. The embodi-

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ment **200B** has the same circuit topology as that of embodiment **200A** in FIG. 2A. The partitioning of embodiment **200B**, however, differs from the partitioning of embodiment **200A**. Like embodiment **200A**, embodiment **200B** has three circuit partitions, or circuit blocks. The first and the third circuit partitions in embodiment **200B** are similar to the first and third circuit partitions in embodiment **200A**. The second circuit partition **230** in embodiment **200B**, however, includes the reference signal generator **218** in addition to the receiver digital circuitry **212**. As in embodiment **200A**, embodiment **200B** is partitioned so that interference effects among the three circuit partitions tend to be reduced.

FIG. 2C illustrates an embodiment **200C**, which constitutes a variation of embodiment **200A** in FIG. 2A. Embodiment **200C** shows that one may place the reference signal generator **218** within the baseband processor circuitry **120**, as desired. Placing the reference signal generator **218** within the baseband processor circuitry **120** obviates the need for either discrete reference signal generator circuitry **218** or an additional integrated circuit or module that includes the reference signal generator **218**. Embodiment **200C** has the same partitioning as embodiment **200A**, and operates in a similar manner.

Note that FIGS. 2A–2C show the receiver circuitry **210** as a block to facilitate the description of the embodiments shown in those figures. In other words, the block containing the receiver circuitry **210** in FIGS. 2A–2C constitutes a conceptual depiction of the receiver circuitry within the RF transceiver shown in FIGS. 2A–2C, not a circuit partition or circuit block.

FIG. 2D shows an embodiment **200D** of an RF transceiver partitioned according to the invention. The RF transceiver in FIG. 2D operates similarly to the transceiver shown in FIG. 2A. The embodiment **200D**, however, accomplishes additional economy by including the receiver digital circuitry **212** within the baseband processor circuitry **120**. As one alternative, one may integrate the entire receiver digital circuitry **212** on the same integrated circuit device that includes the baseband processor circuitry **120**. Note that one may use software (or firmware), hardware, or a combination of software (or firmware) and hardware to realize the functions of the receiver digital circuitry **212** within the baseband processor circuitry **120**, as persons skilled in the art would understand. Note also that, similar to the embodiment **200C** in FIG. 2C, the baseband processor circuitry **120** in embodiment **200D** may also include the reference signal generator **218**, as desired.

The partitioning of embodiment **200D** involves two circuit partitions, or circuit blocks. The first circuit partition **214** includes the receiver analog circuitry **208** and the transmitter circuitry **216**. The second circuit partition includes the local oscillator circuitry **222**. The first and second circuit partitions are partitioned so that interference effects between them tend to be reduced.

FIG. 3 shows the mechanisms that may lead to interference among the various blocks or components in a typical RF transceiver, for example, the transceiver shown in FIG. 2A. Note that the paths with arrows in FIG. 3 represent interference mechanisms among the blocks within the transceiver, rather than desired signal paths. One interference mechanism results from the reference signal **220** (see FIGS. 2A–2D), which preferably comprises a clock signal. In the preferred embodiments, the reference generator circuitry produces a clock signal that may have a frequency of 13 MHz (GSM clock frequency) or 26 MHz. If the reference generator produces a 26 MHz clock signal, RF transceivers

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according to the invention preferably divide that signal by two to produce a 13 MHz master system clock. The clock signal typically includes voltage pulses that have many Fourier series harmonics. The Fourier series harmonics extend to many multiples of the clock signal frequency. Those harmonics may interfere with the receiver analog circuitry **208** (e.g., the low-noise amplifier, or LNA), the local oscillator circuitry **222** (e.g., the synthesizer circuitry), and the transmitter circuitry **216** (e.g., the transmitter's voltage-controlled oscillator, or VCO). FIG. **3** shows these sources of interference as interference mechanisms **360**, **350**, and **340**.

The receiver digital circuitry **212** uses the output of the reference generator circuitry **218**, which preferably comprises a clock signal. Interference mechanism **310** exists because of the sensitivity of the receiver analog circuitry **208** to the digital switching noise and harmonics present in the receiver digital circuitry **212**. Interference mechanism **310** may also exist because of the digital signals (for example, clock signals) that the receiver digital circuitry **212** communicates to the receiver analog circuitry **208**. Similarly, the digital switching noise and harmonics in the receiver digital circuitry **212** may interfere with the local oscillator circuitry **222**, giving rise to interference mechanism **320** in FIG. **3**.

The local oscillator circuitry **222** typically uses an inductor in an inductive-capacitive (LC) resonance tank (not shown explicitly in the figures). The resonance tank may circulate relatively large currents. Those currents may couple to the sensitive circuitry within the transmitter circuitry **216** (e.g., the transmitter's VCO), thus giving rise to interference mechanism **330**. Similarly, the relatively large currents circulating within the resonance tank of the local oscillator circuitry **222** may saturate sensitive components within the receiver analog circuitry **208** (e.g., the LNA circuitry). FIG. **3** depicts this interference source as interference mechanism **370**.

The timing of the transmit mode and receive mode in the GSM specifications help to mitigate potential interference between the transceiver's receive-path circuitry and its transmit-path circuitry. The GSM specifications use time-division duplexing (TDD). According to the TDD protocol, the transceiver deactivates the transmit-path circuitry while in the receive mode of operation, and vice-versa. Consequently, FIG. **3** does not show potential interference mechanisms between the transmitter circuitry **216** and either the receiver digital circuitry **212** or the receiver analog circuitry **208**.

As FIG. **3** illustrates, interference mechanisms exist between the local oscillator circuitry **222** and each of the other blocks or components in the RF transceiver. Thus, to reduce interference effects, RF transceivers according to the invention preferably partition the local oscillator circuitry **222** separately from the other transceiver blocks shown in FIG. **3**. Note, however, that in some circumstances one may include parts or all of the local oscillator circuitry within the same circuit partition (for example, circuit partition **214** in FIGS. **2A–2D**) that includes the receiver analog circuitry and the transmitter circuitry, as desired. Typically, a voltage-controlled oscillator (VCO) within the local oscillator circuitry causes interference with other sensitive circuit blocks (for example, the receiver analog circuitry) through undesired coupling mechanisms. If those coupling mechanisms can be mitigated to the extent that the performance characteristics of the RF transceiver are acceptable in a given application, then one may include the local oscillator circuitry within the same circuit partition as the receiver analog circuitry and the transmitter circuitry. Alternatively, if the

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VCO circuitry causes unacceptable levels of interference, one may include other parts of the local oscillator circuitry within the circuit partition that includes the receiver analog circuitry and the transmitter circuitry, but exclude the VCO circuitry from that circuit partition.

To reduce the effects of interference mechanism **310**, RF transceivers according to the invention partition the receiver analog circuitry **208** separately from the receiver digital circuitry **212**. Because of the mutually exclusive operation of the transmitter circuitry **216** and the receiver analog circuitry **208** according to GSM specifications, the transmitter circuitry **216** and the receiver analog circuitry **208** may reside within the same circuit partition, or circuit block. Placing the transmitter circuitry **216** and the receiver analog circuitry **208** within the same circuit partition results in a more integrated RF transceiver overall. The RF transceivers shown in FIGS. **2A–2D** employ partitioning techniques that take advantage of the above analysis of the interference mechanisms among the various transceiver components. To reduce interference effects among the various circuit partitions or circuit blocks even further, RF transceivers according to the invention also use differential signals to couple the circuit partitions or circuit blocks to one another.

FIG. **4** shows a more detailed block diagram of an embodiment **400** of an RF transceiver partitioned according to the invention. The transceiver includes receiver analog circuitry **408**, receiver digital circuitry **426**, and transmitter circuitry **465**. In the receive mode, the antenna interface circuitry **202** provides an RF signal **401** to a filter circuitry **403**. The filter circuitry **403** provides a filtered RF signal **406** to the receiver analog circuitry **408**. The receiver analog circuitry **408** includes down-converter (i.e., mixer) circuitry **409** and analog-to-digital converter (ADC) circuitry **418**. The down-converter circuitry **409** mixes the filtered RF signal **406** with an RF local oscillator signal **454**, received from the local oscillator circuitry **222**. The down-converter circuitry **409** provides an in-phase analog down-converted signal **412** (i.e., I-channel signal) and a quadrature analog down-converted signal **415** (i.e., Q-channel signal) to the ADC circuitry **418**.

The ADC circuitry **418** converts the in-phase analog down-converted signal **412** and the quadrature analog down-converted signal **415** into a one-bit in-phase digital receive signal **421** and a one-bit quadrature digital receive signal **424**. The ADC circuitry **418** provides the one-bit in-phase digital receive signal **421** and the one-bit quadrature digital receive signal **424** to the receiver digital circuitry **426**. As described below, rather than, or in addition to, providing the one-bit in-phase and quadrature digital receive signals to the receiver digital circuitry **426**, the digital interface between the receiver analog circuitry **408** and the receiver digital circuitry **426** may communicate various other signals. By way of illustration, those signals may include reference signals (e.g., clock signals), control signals, logic signals, hand-shaking signals, data signals, status signals, information signals, flag signals, and/or configuration signals. Moreover, the signals may constitute single-ended or differential signals, as desired. Thus, the interface provides a flexible communication mechanism between the receiver analog circuitry and the receiver digital circuitry.

The receiver digital circuitry **426** includes digital down-converter circuitry **427**, digital filter circuitry **436**, and digital-to-analog converter (DAC) circuitry **445**. The digital down-converter circuitry **427** accepts the one-bit in-phase digital signal receive **421** and the one-bit quadrature digital receive signal **424** from the receiver analog circuitry **408**. The digital down-converter circuitry **427** converts the

received signals into a down-converted in-phase signal 430 and a down-converted quadrature signal 433 and provides those signals to the digital filter circuitry 436. The digital filter circuitry 436 preferably comprises an infinite impulse response (IIR) channel-select filter that performs various filtering operations on its input signals. The digital filter circuitry 436 preferably has programmable response characteristics. Note that, rather than using an IIR filter, one may use other types of filter (e.g., finite impulse-response, or FIR, filters) that provide fixed or programmable response characteristics, as desired.

The digital filter circuitry 436 provides a digital in-phase filtered signal 439 and a digital quadrature filtered signal 442 to the DAC circuitry 445. The DAC circuitry 445 converts the digital in-phase filtered signal 439 and the digital quadrature filtered signal 442 to an in-phase analog receive signal 448 and a quadrature analog receive signal 451, respectively. The baseband processor circuitry 120 accepts the in-phase analog receive signal 448 and the quadrature analog receive signal 451 for further processing.

The transmitter circuitry 465 comprises baseband up-converter circuitry 466, offset phase-lock-loop (PLL) circuitry 472, and transmit voltage-controlled oscillator (VCO) circuitry 481. The transmit VCO circuitry 481 typically has low-noise circuitry and is sensitive to external noise. For example, it may pick up interference from digital switching because of the high gain that results from the resonant LC-tank circuit within the transmit VCO circuitry 481. The baseband up-converter circuitry 466 accepts an intermediate frequency (IF) local oscillator signal 457 from the local oscillator circuitry 222. The baseband up-converter circuitry 466 mixes the IF local oscillator signal 457 with an analog in-phase transmit input signal 460 and an analog quadrature transmit input signal 463 and provides an up-converted IF signal 469 to the offset PLL circuitry 472.

The offset PLL circuitry 472 effectively filters the IF signal 469. In other words, the offset PLL circuitry 472 passes through it signals within its bandwidth but attenuates other signals. In this manner, the offset PLL circuitry 472 attenuates any spurious or noise signals outside its bandwidth, thus reducing the requirement for filtering at the antenna 130, and reducing system cost, insertion loss, and power consumption. The offset PLL circuitry 472 forms a feedback loop with the transmit VCO circuitry 481 via an offset PLL output signal 475 and a transmit VCO output signal 478. The transmit VCO circuitry 481 preferably has a constant-amplitude output signal.

The offset PLL circuitry 472 uses a mixer (not shown explicitly in FIG. 4) to mix the RF local oscillator signal 454 with the transmit VCO output signal 478. Power amplifier circuitry 487 accepts the transmit VCO output signal 478, and provides an amplified RF signal 490 to the antenna interface circuitry 202. The antenna interface circuitry 202 and the antenna 130 operate as described above. RF transceivers according to the invention preferably use transmitter circuitry 465 that comprises analog circuitry, as shown in FIG. 4. Using such circuitry minimizes interference with the transmit VCO circuitry 481 and helps to meet emission specifications for the transmitter circuitry 465.

The receiver digital circuitry 426 also accepts the reference signal 220 from the reference generator circuitry 218. The reference signal 220 preferably comprises a clock signal. The receiver digital circuitry 426 provides to the transmitter circuitry 465 a switched reference signal 494 by using a switch 492. Thus, the switch 492 may selectively provide the reference signal 220 to the transmitter circuitry

465. Before the RF transceiver enters its transmit mode, the receiver digital circuitry 426 causes the switch 492 to close, thus providing the switched reference signal 494 to the transmitter circuitry 465.

The transmitter circuitry 465 uses the switched reference signal 494 to calibrate or adjust some of its components. For example, the transmitter circuitry 465 may use the switched reference signal 494 to calibrate some of its components, such as the transmit VCO circuitry 481, for example, as described in commonly owned U.S. Pat. No. 6,137,372, incorporated by reference here in its entirety. The transmitter circuitry 465 may also use the switched reference signal 494 to adjust a voltage regulator within its output circuitry so as to transmit at known levels of RF radiation.

While the transmitter circuitry 465 calibrates and adjusts its components, the analog circuitry within the transmitter circuitry 465 powers up and begins to settle. When the transmitter circuitry 465 has finished calibrating its internal circuitry, the receiver digital circuitry 426 causes the switch 492 to open, thus inhibiting the supply of the reference signal 220 to the transmitter circuitry 465. At this point, the transmitter circuitry may power up the power amplifier circuitry 487 within the transmitter circuitry 465. The RF transceiver subsequently enters the transmit mode of operation and proceeds to transmit.

Note that FIG. 4 depicts the switch 492 as a simple switch for conceptual, schematic purposes. One may use a variety of devices to realize the function of the controlled switch 492, for example, semiconductor switches, gates, or the like, as persons skilled in the art would understand. Note also that, although FIG. 4 shows the switch 492 as residing within the receiver digital circuitry 426, one may locate the switch in other locations, as desired. Placing the switch 492 within the receiver digital circuitry 426 helps to confine to the receiver digital circuitry 426 the harmonics that result from the switching circuitry.

The embodiment 400 in FIG. 4 comprises a first circuit partition 407, or circuit block, that includes the receiver analog circuitry 408 and the transmitter circuitry 465. The embodiment 400 also includes a second circuit partition, or circuit block, that includes the receiver digital receiver circuitry 426. Finally, the embodiment 400 includes a third circuit partition, or circuit block, that comprises the local oscillator circuitry 222. The first circuit partition 407, the second circuit partition, and the third circuit partition are partitioned from one another so that interference effects among the circuit partitions tend to be reduced. That arrangement tends to reduce the interference effects among the circuit partitions by relying on the analysis of interference effects provided above in connection with FIG. 3. Preferably, the first, second, and third circuit partitions each reside within an integrated circuit device. To further reduce interference effects among the circuit partitions, the embodiment 400 in FIG. 4 uses differential signals wherever possible. The notation "(diff.)" adjacent to signal lines or reference numerals in FIG. 4 denotes the use of differential lines to propagate the annotated signals.

Note that the embodiment 400 shown in FIG. 4 uses an analog-digital-analog signal path in its receiver section. In other words, the ADC circuitry 418 converts analog signals into digital signals for further processing, and later conversion back into analog signals by the DAC circuitry 445. RF transceivers according to the invention use this particular signal path for the following reasons. First, the ADC circuitry 418 obviates the need for propagating signals from the receiver analog circuitry 408 to the receiver digital circuitry

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426 over an analog interface with a relatively high dynamic range. The digital interface comprising the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424 is less susceptible to the effects of noise and interference than would be an analog interface with a relatively high dynamic range.

Second, the RF transceiver in FIG. 4 uses the DAC circuitry 445 to maintain compatibility with interfaces commonly used to communicate with baseband processor circuitry in RF transceivers. According to those interfaces, the baseband processor accepts analog, rather than digital, signals from the receive path circuitry within the RF transceiver. In an RF transceiver that meets the specifications of those interfaces, the receiver digital circuitry 426 would provide analog signals to the baseband processor circuitry 120. The receiver digital circuitry 426 uses the DAC circuitry 445 to provide analog signals (i.e., the in-phase analog receive signal 448 and the quadrature analog receive signal 451) to the baseband processor circuitry 120. The DAC circuitry 445 allows programming the common-mode level and the full-scale voltage, which may vary among different baseband processor circuitries.

Third, compared to an analog solution, the analog-digital-analog signal path may result in reduced circuit size and area (for example, the area occupied within an integrated circuit device), thus lower cost. Fourth, the digital circuitry provides better repeatability, relative ease of testing, and more robust operation than its analog counterpart. Fifth, the digital circuitry has less dependence on supply voltage variation, temperature changes, and the like, than does comparable analog circuitry.

Sixth, the baseband processor circuitry 120 typically includes programmable digital circuitry, and may subsume the functionality of the digital circuitry within the receiver digital circuitry 426, if desired. Seventh, the digital circuitry allows more precise signal processing, for example, filtering, of signals within the receive path. Eighth, the digital circuitry allows more power-efficient signal processing. Finally, the digital circuitry allows the use of readily programmable DAC circuitry and PGA circuitry that provide for more flexible processing of the signals within the receive path. To benefit from the analog-digital-analog signal path, RF transceivers according to the invention use a low-IF signal (for example, 100 KHz for GSM applications) in their receive path circuitry, as using higher IF frequencies may lead to higher performance demands on the ADC and DAC circuitry within that path. The low-IF architecture also eases image-rejection requirements, which allows on-chip integration of the digital filter circuitry 436. Moreover, RF transceivers according to the invention use the digital down-converter circuitry 427 and the digital filter circuitry 436 to implement a digital-IF path in the receive signal path. The digital-IF architecture facilitates the implementation of the digital interface between the receiver digital circuitry 426 and the receiver analog circuitry 408.

If the receiver digital circuitry 426 need not be compatible with the common analog interface to baseband processors, one may remove the DAC circuitry 445 and use a digital interface to the baseband processor circuitry 120, as desired. In fact, similar to the RF transceiver shown in FIG. 2D, one may realize the function of the receiver digital circuitry 426 within the baseband processor circuitry 120, using hardware, software, or a combination of hardware and software. In that case, the RF transceiver would include two circuit partitions, or circuit blocks. The first circuit partition, or circuit block, 407 would include the receiver analog circuitry 408 and the transmitter circuitry 465. A second circuit partition, or

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circuit block, would comprise the local oscillator circuitry 222. Note also that, similar to the RF transceiver shown in FIG. 2C, one may include within the baseband processor circuitry 120 the functionality of the reference generator circuitry 218, as desired.

One may partition the RF transceiver shown in FIG. 4 in other ways. FIGS. 5 and 6 illustrate alternative partitioning of the RF transceiver of FIG. 4. FIG. 5 shows an embodiment 500 of an RF transceiver that includes three circuit partitions, or circuit blocks. A first circuit partition includes the receiver analog circuitry 408. A second circuit partition 505 includes the receiver digital circuitry 426 and the transmitter circuitry 465. As noted above, the GSM specifications provide for alternate operation of RF transceivers in receive and transmit modes. The partitioning shown in FIG. 5 takes advantage of the GSM specifications by including the receiver digital circuitry 426 and the transmitter circuitry 465 within the second circuit partition 505. A third circuit partition includes the local oscillator circuitry 222. Preferably, the first, second, and third circuit partitions each reside within an integrated circuit device. Similar to embodiment 400 in FIG. 4, the embodiment 500 in FIG. 5 uses differential signals wherever possible to further reduce interference effects among the circuit partitions.

FIG. 6 shows another alternative partitioning of an RF transceiver. FIG. 6 shows an embodiment 600 of an RF transceiver that includes three circuit partitions, or circuit blocks. A first circuit partition 610 includes part of the receiver analog circuitry, i.e., the down-converter circuitry 409, together with the transmitter circuitry 465. A second circuit partition 620 includes the ADC circuitry 418, together with the receiver digital circuitry, i.e., the digital down-converter circuitry 427, the digital filter circuitry 436, and the DAC circuitry 445. A third circuit partition includes the local oscillator circuitry 222. Preferably, the first, second, and third circuit partitions each reside within an integrated circuit device. Similar to embodiment 400 in FIG. 4, the embodiment 600 in FIG. 6 uses differential signals wherever possible to further reduce interference effects among the circuit partitions.

FIG. 7 shows a variation of the RF transceiver shown in FIG. 4. FIG. 7 illustrates an embodiment 700 of an RF transceiver partitioned according to the invention. Note that, for the sake of clarity, FIG. 7 does not explicitly show the details of the receiver analog circuitry 408, the transmitter circuitry 465, and the receiver digital circuitry 426. The receiver analog circuitry 408, the transmitter circuitry 465, and the receiver digital circuitry 426 include circuitry similar to those shown in their corresponding counterparts in FIG. 4. Similar to the RF transceiver shown in FIG. 2D, the embodiment 700 in FIG. 7 shows an RF transceiver in which the baseband processor 120 includes the function of the receiver digital circuitry 426. The baseband processor circuitry 120 may realize the function of the receiver digital circuitry 426 using hardware, software, or a combination of hardware and software.

Because the embodiment 700 includes the function of the receiver digital circuitry 426 within the baseband processor circuitry 120, it includes two circuit partitions, or circuit blocks. A first circuit partition 710 includes the receiver analog circuitry 408 and the transmitter circuitry 465. A second circuit partition comprises the local oscillator circuitry 222. Note also that, similar to the RF transceiver shown in FIG. 2C, one may also include within the baseband processor circuitry 120 the functionality of the reference generator circuitry 218, as desired.

FIG. 8 shows an embodiment 800 of a multi-band RF transceiver, partitioned according to the invention.

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Preferably, the RF transceiver in FIG. 8 operates within the GSM (925 to 960 MHz), PCS (1930 to 1990 MHz), and DCS (1805 to 1880 MHz) bands. Like the RF transceiver in FIG. 4, the RF transceiver in FIG. 8 uses a low-IF architecture. The embodiment 800 includes receiver analog circuitry 839, receiver digital circuitry 851, transmitter circuitry 877, local oscillator circuitry 222, and reference generator circuitry 218. The local oscillator circuitry 222 includes RF phase-lock loop (PLL) circuitry 840 and intermediate-frequency (IF) PLL circuitry 843. The RF PLL circuitry 840 produces the RF local oscillator, or RF LO, signal 454, whereas the IF PLL circuitry 843 produces the IF local oscillator, or IF LO, signal 457.

Table 1 below shows the preferred frequencies for the RF local oscillator signal 454 during the receive mode:

TABLE 1

Band	RF Local Oscillator Frequency (MHz)
GSM	1849.8–1919.8
DCS	1804.9–1879.9
PCS	1929.9–1989.9
All Bands	1804.9–1989.9

Table 2 below lists the preferred frequencies for the RF local oscillator signal 454 during the transmit mode:

TABLE 2

Band	RF Local Oscillator Frequency (MHz)
GSM	1279–1314
DCS	1327–1402
PCS	1423–1483
All Bands	1279–1483

During the receive mode, the IF local oscillator signal 457 preferably has a frequency of 100 kHz. In preferred embodiments, during the transmit mode, the IF local oscillator signal 457 preferably has a frequency between 383 MHz and 427 MHz. Note, however, that one may use other frequencies for the RF and IF local oscillator signals 454 and 457, as desired.

The reference generator 218 provides a reference signal 220 that preferably comprises a clock signal, although one may use other signals, as persons skilled in the art would understand. Moreover, the transmitter circuitry 877 preferably uses high-side injection for the GSM band and low-side injection for the DCS and PCS bands.

The receive path circuitry operates as follows. Filter circuitry 812 accepts a GSM RF signal 803, a DCS RF signal 806, and a PCS RF signal 809 from the antenna interface circuitry 202. The filter circuitry 812 preferably contains a surface-acoustic-wave (SAW) filter for each of the three bands, although one may use other types and numbers of filters, as desired. The filter circuitry 812 provides a filtered GSM RF signal 815, a filtered DCS RF signal 818, and a filtered PCS RF signal 821 to low-noise amplifier (LNA) circuitry 824. The LNA circuitry 824 preferably has programmable gain, and in part provides for programmable gain in the receive path circuitry.

The LNA circuitry 824 provides an amplified RF signal 827 to down-converter circuitry 409. Note that, rather than using the LNA circuitry with a real output, one may use an LNA circuitry that has complex outputs (in-phase and quadrature outputs), together with a poly-phase filter cir-

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cuitry. The combination of the complex LNA circuitry and the poly-phase filter circuitry provides better image rejection, albeit with a somewhat higher loss. Thus, the choice of using the complex LNA circuitry and the poly-phase filter circuitry depends on a trade-off between image rejection and loss in the poly-phase filter circuitry.

The down-converter circuitry 409 mixes the amplified RF signal 827 with the RF local oscillator signal 454, which it receives from the RF PLL circuitry 840. The down-converter circuitry 409 produces the in-phase analog down-converted signal 412 and the quadrature in-phase analog down-converted signal 415. The down-converter circuitry 409 provides the in-phase analog down-converted signal 412 and the quadrature in-phase analog down-converted signal 415 to a pair of programmable-gain amplifiers (PGAs) 833A and 833B.

The PGA 833A and PGA 833B in part allow for programming the gain of the receive path. The PGA 833A and the PGA 833B supply an analog in-phase amplified signal 841 and an analog quadrature amplified signal 842 to complex ADC circuitry 836 (i.e., both I and Q inputs will affect both I and Q outputs). The ADC circuitry 836 converts the analog in-phase amplified signal 841 into a one-bit in-phase digital receive signal 421. Likewise, the ADC circuitry 836 converts the analog quadrature amplified signal 842 into a one-bit quadrature digital receive signal 424.

Note that RF transceivers and receivers according to the invention preferably use a one-bit digital interface. One may, however, use a variety of other interfaces, as persons skilled in the art who have read this description of the invention would understand. For example, one may use a multi-bit interface or a parallel interface. Moreover, as described below, rather than, or in addition to, providing the one-bit in-phase and quadrature digital receive signals to the receiver digital circuitry 851, the digital interface between the receiver analog circuitry 839 and the receiver digital circuitry 851 may communicate various other signals. By way of illustration, those signals may include reference signals (e.g., clock signals), control signals, logic signals, hand-shaking signals, data signals, status signals, information signals, flag signals, and/or configuration signals. Furthermore, the signals may constitute single-ended or differential signals, as desired. Thus, the interface provides a flexible communication mechanism between the receiver analog circuitry and the receiver digital circuitry.

The receiver digital circuitry 851 accepts the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424, and provides them to the digital down-converter circuitry 427. The digital down-converter circuitry 427 converts the received signals into a down-converted in-phase signal 430 and a down-converted quadrature signal 433 and provides those signals to the digital filter circuitry 436. The digital filter circuitry 436 preferably comprises an IIR channel-select filter that performs filtering operations on its input signals. Note, however, that one may use other types of filters, for example, FIR filters, as desired.

The digital filter circuitry 436 provides the digital in-phase filtered signal 439 to a digital PGA 863A and the digital quadrature filtered signal 442 to a digital PGA 863B. The digital PGA 863A and PGA 863B in part allow for programming the gain of the receive path circuitry. The digital PGA 863A supplies an amplified digital in-phase signal 869 to DAC circuitry 875A, whereas the digital PGA 863B supplies an amplified digital quadrature signal 872 to DAC circuitry 875B. The DAC circuitry 875A converts the



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amplified digital in-phase signal **869** to the in-phase analog receive signal **448**. The DAC circuitry **875B** converts the amplified digital quadrature signal **872** signal into the quadrature analog receive signal **451**. The baseband processor circuitry **120** accepts the in-phase analog receive signal **448** and the quadrature analog receive signal **451** for further processing, as desired.

Note that the digital circuit blocks shown in the receiver digital circuitry **851** depict mainly the conceptual functions and signal flow. The actual digital-circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For example, one may re-use (in time, for instance, by using multiplexing) the same digital circuitry to implement both digital PGA **863A** and digital PGA **863B**, as desired.

Note also that, similar to the RF transceiver in FIG. 4, the RF transceiver in FIG. 8 features a digital-IF architecture. The digital-IF architecture facilitates the implementation of the one-bit digital interface between the receiver digital circuitry **426** and the receiver analog circuitry **408**. Moreover, the digital-IF architecture allows digital (rather than analog) IF-filtering, thus providing all of the advantages of digital filtering.

The transmitter circuitry **877** comprises baseband up-converter circuitry **466**, transmit VCO circuitry **481**, a pair of transmitter output buffers **892A** and **892B**, and offset PLL circuitry **897**. The offset PLL circuitry **897** includes offset mixer circuitry **891**, phase detector circuitry **882**, and loop filter circuitry **886**. The baseband up-converter circuitry **466** accepts the analog in-phase transmit input signal **460** and the analog quadrature transmit input signal **463**, mixes those signals with the IF local oscillator signal **457**, and provides a transmit IF signal **880** to the offset PLL circuitry **897**. The offset PLL circuitry **897** uses the transmit IF signal **880** as a reference signal. The transmit IF signal **880** preferably comprises a modulated single-sideband IF signal but, as persons skilled in the art would understand, one may use other types of signal and modulation, as desired.

The offset mixer circuitry **891** in the offset PLL circuitry **897** mixes the transmit VCO output signal **478** with the RF local oscillator signal **454**, and provides a mixed signal **890** to the phase detector circuitry **882**. The phase detector circuitry **882** compares the mixed signal **890** to the transmit IF signal **880** and provides an offset PLL error signal **884** to the loop filter circuitry **886**. The loop filter circuitry **886** in turn provides a filtered offset PLL signal **888** to the transmit VCO circuitry **481**. Thus, the offset PLL circuitry **897** and the transmit VCO circuitry **481** operate in a feedback loop. Preferably, the output frequency of the transmit VCO circuitry **481** centers between the DCS and PCS bands, and its output is divided by two for the GSM band.

Transmitter output buffers **892A** and **892B** receive the transmit VCO output signal **478** and provide buffered transmit signals **894** and **895** to a pair of power amplifiers **896A** and **896B**. The power amplifiers **896A** and **896B** provide amplified RF signals **899** and **898**, respectively, for transmission through antenna interface circuitry **202** and the antenna **130**. Power amplifier **896A** provides the RF signal **899** for the GSM band, whereas power amplifier **896B** supplies the RF signal **898** for the DCS and PCS bands. Persons skilled in the art, however, will understand that one may use other arrangements of power amplifiers and frequency bands. Moreover, one may use RF filter circuitry within the output path of the transmitter circuitry **877**, as desired.

The embodiment **800** comprises three circuit partitions, or circuit blocks. A first circuit partition **801** includes the

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receiver analog circuitry **839** and the transmitter circuitry **877**. A second circuit partition **854** includes the receiver digital circuitry **851** and the reference generator circuitry **218**. Finally, a third circuit partition comprises the local oscillator circuitry **222**. The first circuit partition **801**, the second circuit partition **854**, and the third circuit partition are partitioned from one another so that interference effects among the circuit partitions tend to be reduced. That arrangement tends to reduce the interference effects among the circuit partitions because of the analysis of interference effects provided above in connection with FIG. 3. Preferably, the first, second, and third circuit partitions each reside within an integrated circuit device. To further reduce interference effects among the circuit partitions, the embodiment **800** in FIG. 8 uses differential signals wherever possible. The notation “(diff.)” adjacent to signal lines or reference numerals in FIG. 8 denotes the use of differential lines to propagate the annotated signals.

Note that, similar to the RF transceiver shown in FIG. 4 and described above, the embodiment **800** shown in FIG. 8 uses an analog-digital-analog signal path in its receiver section. The embodiment **800** uses this particular signal path for reasons similar to those described above in connection with the transceiver shown in FIG. 4.

Like the transceiver in FIG. 4, if the receiver digital circuitry **851** need not be compatible with the common analog interface to baseband processors, one may remove the DAC circuitry **875A** and **875B**, and use a digital interface to the baseband processor circuitry **120**, as desired. In fact, similar to the RF transceiver shown in FIG. 2D, one may realize the function of the receiver digital circuitry **851** within the baseband processor circuitry **120**, using hardware, software, or a combination of hardware and software. In that case, the RF transceiver would include two circuit partitions, or circuit blocks. The first circuit partition **801** would include the receiver analog circuitry **839** and the transmitter circuitry **877**. A second circuit partition would comprise the local oscillator circuitry **222**. Note also that, similar to the RF transceiver shown in FIG. 2C, in the embodiment **800**, one may include within the baseband processor circuitry **120** the functionality of the reference generator circuitry **218**, as desired.

Another aspect of the invention includes a configurable interface between the receiver digital circuitry and the receiver analog circuitry. Generally, one would seek to minimize digital switching activity within the receiver analog circuitry. Digital switching activity within the receiver analog circuitry would potentially interfere with the sensitive analog RF circuitry, for example, LNAs, or mixers. As described above, the receiver analog circuitry includes analog-to-digital circuitry (ADC), which preferably comprises sigma-delta-type ADCs. Sigma-delta ADCs typically use a clock signal at their output stages that generally has a pulse shape and, thus, contains high-frequency Fourier series harmonics. Moreover, the ADC circuitry itself produces digital outputs that the receiver digital circuitry uses. The digital switching present at the outputs of the ADC circuitry may also interfere with sensitive analog circuitry within the receiver analog circuitry.

The invention contemplates providing RF apparatus according to the invention, for example, receivers and transceivers, that include an interface circuitry to minimize or reduce the effects of interference from digital circuitry within the RF apparatus. FIG. 9A shows an embodiment **900A** of an interface between the receiver digital circuitry **905** and the receiver analog circuitry **910**. The interface includes configurable interface signal lines **945**. The base-



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band processor circuitry 120 in the transceiver of FIG. 9A communicates configuration, status, and setup information with both the receiver digital circuitry 905 and the receiver analog circuitry 910. In the preferred embodiments of RF transceivers according to the invention, the baseband processor circuitry 120 communicates with the receiver digital circuitry 905 and the receiver analog circuitry 910 by sending configuration data to read and write registers included within the receiver digital circuitry 905 and the receiver analog circuitry 910.

The receiver digital circuitry 905 communicates with the baseband processor circuitry 120 through a set of serial interface signal lines 920. The serial interface signal lines 920 preferably include a serial data-in (SDI) signal line 925, a serial clock (SCLK) signal line 930, a serial interface enable (SENB) signal line 935, and a serial data-out (SDO) signal line 940. The transceiver circuitry and the baseband processor circuitry 120 preferably hold all of the serial interface signal lines 920 at static levels during the transmit and receive modes of operation. The serial interface preferably uses a 22-bit serial control word that comprises 6 address bits and 16 data bits. Note, however, that one may use other serial interfaces, parallel interfaces, or other types of interfaces, that incorporate different numbers of signal lines, different types and sizes of signals, or both, as desired. Note also that, the SENB signal is preferably an active-low logic signal, although one may use a normal (i.e., an active-high) logic signal by making circuit modifications, as persons skilled in the art would understand.

The receiver digital circuitry 905 communicates with the receiver analog circuitry 910 via configurable interface signal lines 945. Interface signal lines 945 preferably include four configurable signal lines 950, 955, 960, and 965, although one may use other numbers of configurable signal lines, as desired, depending on a particular application. In addition to supplying the serial interface signals 920, the baseband processor circuitry 120 provides a control signal 915, shown as a power-down (PDNB) signal in FIG. 9A, to both the receiver digital circuitry 905 and the receiver analog circuitry 910. The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably use the power-down (PDNB) signal as the control signal 915 to configure the functionality of the interface signal lines 945. In other words, the functionality of the interface signal lines 945 depends on the state of the control signal 915. Also, the initialization of the circuitry within the receive path and the transmit path of the transceiver occurs upon the rising edge of the PDNB signal. Note that the PDNB signal is preferably an active-low logic signal, although one may use a normal (i.e., an active-high) logic signal, as persons skilled in the art would understand. Note also that, rather than using the PDNB signal, one may use other signals to control the configuration of the interface signal lines 945, as desired.

In the power-down or serial interface mode (i.e., the control signal 915 (for example, PDNB) is in the logic low state), interface signal line 950 provides the serial clock (SCLK) and interface signal line 955 supplies the serial interface enable signal (SENB). Furthermore, interface signal line 960 provides the serial data-in signal (SDI), whereas interface signal line 965 supplies the serial data-out signal (SDO). During this mode of operation, the transceiver may also perform circuit calibration and adjustment procedures, as desired. For example, the values of various transceiver components may vary over time or among transceivers produced in different manufacturing batches. The transceiver may calibrate and adjust its circuitry to take those variations into account and provide higher performance.

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In the normal receive mode of operation (i.e., the control signal, PDNB, is in the logic-high state), interface signal line 950 provides a negative clock signal (CKN) and interface signal line 955 supplies the positive clock signal (CKP). Furthermore, interface signal line 960 provides a negative data signal (ION), whereas interface signal line 965 supplies a positive data signal (IOP).

In preferred embodiments of the invention, the CKN and CKP signals together form a differential clock signal that the receiver digital circuitry 905 provides to the receiver analog circuitry 910. The receiver analog circuitry 910 may provide the clock signal to the transmitter circuitry within the RF transceiver in order to facilitate calibration and adjustment of circuitry, as described above. During the receive mode, the receiver analog circuitry 910 provides the ION and IOP signals to the receiver digital circuitry 905. The ION and IOP signals preferably form a differential data signal. As noted above, the transceiver disables the transmitter circuitry during the receive mode of operation.

In preferred embodiments according to the invention, clock signals CKN and CKP are turned off when the transmitter circuitry is transmitting signals. During the transmit mode, interface signal lines 960 and 965 preferably provide two logic signals from the receiver digital circuitry 905 to the receiver analog circuitry 910. The signal lines may provide input/output signals to communicate data, status, information, flag, and configuration signals between the receiver digital circuitry 905 and the receiver analog circuitry 910, as desired. Preferably, the logic signals control the output buffer of the transmit VCO circuitry. Note that, rather than configuring interface signal lines 960 and 965 as logic signal lines, one may configure them in other ways, for example, analog signal lines, differential analog or digital signal lines, etc., as desired. Furthermore, the interface signal lines 960 and 965 may provide signals from the receiver digital circuitry 905 to the receiver analog circuitry 910, or vice-versa, as desired.

In addition to using differential signals, RF transceivers according to the invention preferably take other measures to reduce interference effects among the various transceiver circuits. Signals CKN, CKP, ION, and IOP may constitute voltage signals, as desired. Depending on the application, the signals CKN, CKP, ION, and IOP (or logic signals in the transmit mode) may have low voltage swings (for example, voltage swings smaller than the supply voltage) to reduce the magnitude and effects of interference because of the voltage switching on those signals.

In preferred embodiments according to the invention, signals CKN, CKP, ION, and IOP constitute current, rather than voltage, signals. Moreover, to help reduce the effects of interference even further, RF transceivers according to the invention preferably use band-limited signals. RF transceivers according to the invention preferably use filtering to remove some of the higher frequency harmonics from those signals to produce band-limited current signals.

Table 3 below summarize the preferred functionality of the configurable interface signal lines 950, 955, 960, and 965 as a function of the state of the control signal 915 (for example, PDNB):

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TABLE 3

Signal Line	Control = 0	Control = 1 (During Reception)	Control = 1 (During Transmission)
950	SCLK	CKN	(CKN off)
955	SENB	CKP	(CKP off)
960	SDI	ION	Logic Signal
965	SDO	IOP	Logic Signal

Using configurable interface signal lines **945** in the interface between the receiver digital circuitry **905** and the receiver analog circuitry **910** allows using the same physical connections (e.g., pins on an integrated-circuit device or electrical connectors on a module) to accomplish different functionality. Thus, the configurable interface between the receiver digital circuitry **905** and the receiver analog circuitry **910** makes available the physical electrical connections available for other uses, for example, providing ground pins or connectors around sensitive analog signal pins or connectors to help shield those signals from RF interference. Moreover, the configurable interface between the receiver digital circuitry **905** and the receiver analog circuitry **910** reduced packaging size, cost, and complexity.

FIG. **9B** shows an embodiment **900B** that includes a configurable interface according to the invention. Here, the baseband processor circuitry **120** subsumes the functionality of the receiver digital circuitry **905**. The baseband processor circuitry **120** realizes the functionality of the receiver digital circuitry **905**, using hardware, software, or both, as desired. Because the baseband processor circuitry **120** has subsumed the receiver digital circuitry **905**, the baseband processor circuitry **120** may communicate with the receiver analog circuitry **910** using configurable interface signal lines **945**, depending on the state of the control signal **915** (e.g., the PDNB signal). The configurable interface signal lines **945** perform the same functions described above in connection with FIG. **9A**, depending on the state of the control signal **915**. As noted above, one may reconfigure the interface signal lines **960** and **965** during transmit mode to implement desired functionality, for example, logic signals.

FIG. **10** shows a conceptual block diagram of an embodiment **1000** of a configurable interface according to the invention within an RF transceiver in the power-down or serial interface mode (i.e., the control signal **915** is in a logic-low state). A logic low state on the control signal **915** enables the driver circuitry **1012A**, **1012B**, and **1012C**, thus providing the configurable serial interface signal lines **950**, **955**, and **960** to the receiver analog circuitry **910**. Similarly, the logic low state on the control signal **915** causes the AND gates **1030A**, **1030B**, and **1030C** to provide configurable interface signal lines **950**, **955**, and **960** to other circuitry within the receiver analog circuitry **910**. The outputs of the AND gates **1030A**, **1030B**, and **1030C** comprise a gated SCLK signal **1032**, a gated SENB signal **1034**, and a gated SDI signal **1036**, respectively.

Interface controller circuitry **1040** accepts as inputs the gated SCLK signal **1032**, the gated SENB signal **1034**, and the gated SDI signal **1036**. The interface controller circuitry **1040** resides within the receiver analog circuitry **910** and produces a receiver analog circuitry SDO signal **1044** and an enable signal **1046**. By controlling tri-state driver circuitry **1042**, the enable signal **1046** controls the provision of the receiver analog circuitry SDO signal **1044** to the receiver digital circuitry **905** via the configurable interface signal line **965**.

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Interface controller circuitry **1010** within the receiver digital circuitry **905** accepts the SCLK signal **925**, the SENB signal **930**, and the SDI signal **935** from the baseband processor circuitry **120**. By decoding those signals, the interface controller circuitry **1010** determines whether the baseband processor circuitry **120** intends to communicate with the receiver digital circuitry **905** (e.g., the baseband processor circuitry **120** attempts to read a status or control register present on the receiver digital circuitry **905**). If so, the interface controller circuitry **1010** provides the SCLK signal **925**, the SENB signal **930**, and the SDI signal **935** to other circuitry (not shown explicitly) within the receiver digital circuitry **905** for further processing.

Interface controller circuitry **1010** provides as output signals a receiver digital circuitry SDO signal **1018**, a select signal **1020**, and an enable signal **1022**. The receiver digital circuitry SDO signal **1018** represents the serial data-out signal for the receiver digital circuitry **905**, i.e., the serial data-out signal that the receiver digital circuitry **905** seeks to provide to the baseband processor circuitry **120**. The interface controller circuitry **1010** supplies the select signal **1020** to multiplexer circuitry **1014**. The multiplexer circuitry **1014** uses that signal to selectively provide as the multiplexer circuitry output signal **1024** either the receiver digital circuitry SDO signal **1018** or the receiver analog circuitry SDO signal **1044**, which it receives through configurable interface signal line **965**. Tri-state driver circuitry **1016** provides the multiplexer circuitry output signal **1024** to the baseband processor circuitry **120** under the control of the enable signal **1022**.

Tri-state driver circuitry **1012A**, **1012B**, and **1012C** use an inverted version of the control signal **915** as their enable signals. Thus, a logic high value on the control signal **915** disables the driver circuitry **1012A**, **1012B**, and **1012C**, thus disabling the serial interface between the receiver digital circuitry **905** and the receiver analog circuitry **910**. Similarly, AND gates **1030A**, **1030B**, and **1030C** use an inverted version of the control signal **915** to gate interface signal lines **950**, **955**, and **960**. In other words, a logic high value on the control signal **915** inhibits logic switching at the outputs of AND gates **1030A**, **1030B**, and **1030C**, which reside on the receiver analog circuitry **910**.

FIG. **11A** shows a conceptual block diagram of an embodiment **1100A** of a configurable interface according to the invention, in an RF transceiver operating in the normal receive mode of operation (i.e., the control signal **915** is in a logic-high state). As noted above, in this mode, the receiver digital circuitry **905** provides a clock signal to the receiver analog circuitry **910** through the configurable interface signal lines **950** and **955**. Configurable interface signal line **950** provides the CKN signal, whereas configurable interface signal line **955** supplies the CKP signal. Also in this mode, the receiver analog circuitry **910** provides a data signal to the receiver digital circuitry **905** through the configurable interface signal lines **960** and **965**.

The receiver digital circuitry **905** provides the CKN and CKP signals to the receiver analog circuitry **910** by using clock driver circuitry **1114**. The clock driver circuitry **1114** receives a clock signal **1112A** and a complement clock signal **1112B** from signal processing circuitry **1110**. Signal processing circuitry **1110** receives the reference signal **220** and converts it to the clock signal **1112A** and complement clock signal **1112B**. Interface controller circuitry **1116** provides an enable signal **1118** that controls the provision of the CKN and CKP clock signals to the receiver analog circuitry **910** via the interface signal lines **950** and **955**, respectively.

Receiver analog circuitry **910** includes clock receiver circuitry **1130** that receives the CKN and CKP clock signals

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and provides a clock signal **1132A** and a complement clock signal **1132B**. Interface controller circuitry **1140** within the receiver analog circuitry **910** provides an enable signal **1142** that controls the operation of the clock receiver circuitry **1130**.

The clock signal **1132A** clocks the ADC circuitry **1144**, or other circuitry (for example, calibration circuitry), or both, as desired. Note that, rather than using the clock signal **1132A**, one may use the complement clock signal **1132B**, by making circuit modifications as persons skilled would understand. The ADC circuitry **1144** provides to multiplexer circuitry **1150** a one-bit differential in-phase digital signal **1146A** and a one-bit differential quadrature digital signal **1146B**. The multiplexer circuitry **1150** provides a one-bit differential digital output signal **1152** to data driver circuitry **1154**. The output signal **1152** therefore constitutes multiplexed I-channel data and Q-channel data. The data driver circuitry **1154** supplies the differential data signal comprising ION and IOP to the receiver digital circuitry **905**, using the configurable interface signal lines **960** and **965**, respectively.

The clock signal **1132A** also acts as the select signal of multiplexer circuitry **1150**. On alternating edges of the clock signal **1132A**, the multiplexer circuitry **1150** selects, and provides to, the data driver circuitry **1154** the one-bit differential in-phase digital signal **1146A** (i.e., I-channel data) and the one-bit differential quadrature digital signal **1146B** (i.e., Q-channel data). The interface controller circuitry **1140** supplies an enable signal **1156** to the data driver circuitry **1154** that controls the provision of the configurable interface signal **960** and the configurable interface signal **965** to the receiver digital circuitry **905** via the configurable interface signal lines **960** and **965**.

The receiver digital circuitry **905** includes data receiver circuitry **1120**. Data receiver circuitry **1120** accepts from the receiver analog circuitry **910** the signals provided via the configurable interface signal lines **960** and **965**. The data receiver circuitry **1120** provides a pair of outputs **1122A** and **1122B**. An enable signal **1124**, supplied by the interface controller circuitry **1116**, controls the operation of the data receiver circuitry **1120**.

The receiver digital circuitry **905** also includes a delay-cell circuitry **1119** that accepts as its inputs the clock signal **1112A** and the complement clock signal **1112B**. The delay-cell circuitry **1119** constitutes a delay-compensation circuit. In other words, ideally, the signal-propagation delay of the delay-cell circuitry **1119** compensates for the delays the signals experience as they propagate from the receiver digital circuitry **905** to the receiver analog circuitry **910**, and back to the receiver digital circuitry **905**.

The delay-cell circuitry **1119** provides as its outputs a clock signal **1121A** and a complement clock signal **1121B**. The clock signal **1121A** and the complement clock signal **1121B** clock a pair of D flip-flop circuitries **1123A** and **1123B**, respectively. The D flip-flop circuitries **1123A** and **1123B** latch the output **1122A** of the data receiver circuitry **1120** alternately. In other words, the clock signal **1121A** causes the latching of the I-channel data by the D flip-flop circuitry **1123A**, whereas the complement clock signal **1121B** causes the D flip-flop circuitry **1123B** to latch the Q-channel data.

The output signals of the delay-cell circuitry **1119** help the receiver digital circuitry **905** to sample the I-channel data and the Q-channel data that it receives from the receiver analog circuitry **910**. The receiver digital circuitry **905** receives multiplexed I-channel data and the Q-channel data

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through the ION signal **960** and the IOP signal **965**. Thus, the D flip-flop circuitries **1123A** and **1123B** perform a de-multiplexing function on the multiplexed I-channel data and Q-channel data.

In the normal receive or transmit modes, (i.e., the control signal **915** is in the logic-high state), interface signal line **950** provides the negative clock signal (CKN) and interface signal line **955** supplies the positive clock signal (CKP). In preferred embodiments of the invention, the CKN and CKP signals together form a differential clock signal that the receiver digital circuitry **905** provides to the receiver analog circuitry **910**.

During the receive mode, interface signal line **960** provides the negative data signal (ION), whereas interface signal line **965** supplies the positive data signal (IOP). The ION and IOP signals preferably form a differential data signal.

In the transmit mode, the data signal may function as an input/output signal to communicate data, status, information, flag, and/or configuration signals between the receiver digital circuitry **905** and the receiver analog circuitry **910**. Preferably, the interface signal lines **960** and **965** function as two logic signal lines in the transmit mode. As noted above, the transceiver disables the receiver circuitry during the transmit mode of operation. In RF transceivers partitioned according to the invention (see, e.g., FIGS. 2A-2D, 4, and 8), the clock receiver circuitry **1130** may provide the clock signal **1132A**, the complement clock signal **1132B**, or both, to transmitter circuitry (partitioned together with the receiver analog circuitry **910**) for circuit calibration, circuit adjustment, and the like, as described above.

In the transmit mode, once circuit calibration and adjustment has concluded, however, the clock driver circuitry **1114** uses the enable signal **1118** to inhibit the propagation of the CKN and CKP clock signals to the receiver analog circuitry **910**. In this manner, the clock driver circuitry **1114** performs the function of the switch **492** in FIGS. 4 and 8. Note that, during the normal transmit mode of operation, the ADC circuitry **1144** does not provide any data to the receiver digital circuitry **905** via the ION and IOP signals because, according to the TDD protocol, the receiver path circuitry is inactive during the normal transmit mode of operation. Instead, the receiver digital circuitry **905** provides control signals to the receiver analog circuitry **910** via interface signal lines **960** and **965**.

During the transmit mode, the interface controller circuitry **1116** provides control signals via signal lines **1160** to the interface signal lines **960** and **965**. The interface controller circuitry **1140** receives the control signals via signal lines **1165** and provides them to various blocks within the receiver analog circuitry, as desired. During the receive mode, the interface controller circuitry **1116** inhibits (e.g., high-impedance state) the signal lines **1160**. Similarly, the interface controller circuitry **1140** inhibits the signal lines **1165** during the receive mode.

For the purpose of conceptual illustration, FIG. 11A shows the interface controller circuitry **1116** and the interface controller circuitry **1140** as two blocks of circuitry distinct from the interface controller circuitry **1010** and the interface controller circuitry **1040** in FIG. 10, respectively. One may combine the functionality of the interface controller circuitry **1116** with the functionality of the interface controller circuitry **1010**, as desired. Likewise, one may combine the functionality of interface controller circuitry **1140** with the functionality of the interface controller cir-

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cuitry 1040, as desired. Moreover, one may combine the functionality of the signal processing circuitries 1110 with the functionality of the interface controller circuitry 1116 and the interface controller circuitry 1140, respectively. Combining the functionality of those circuits depends on various design and implementation choices, as persons skilled in the art would understand.

FIG. 11B illustrates a block diagram of a preferred embodiment 1100B of a delay-cell circuitry 1119 according to the invention. The delay-cell circuitry 1119 includes a replica of the clock driver circuitry 1114A in tandem with a replica of the data receiver circuitry 1120A. (Note that the delay-cell circuitry 1119 may alternatively include a replica of the data driver circuitry 1154 in tandem with a replica of the clock receiver circuitry 1130.) The replica of the clock driver circuitry 1114A accepts the clock signal 1112A and the complement clock signal 1112B. The replica of the clock driver circuitry 1114A provides its outputs to the replica of the data receiver circuitry 1120A. The replica of the data receiver circuitry 1120A supplies the clock signal 1121A and the complement clock signal 1121B. The clock signal 1121A and the complement clock signal 1121B constitute the output signals of the delay-cell circuitry 1119. The delay-cell circuitry 1119 also receives as inputs enable signals 1118 and 1124 (note that FIG. 11A does not show those input signals for the sake of clarity). The enable signal 1118 couples to the replica of the clock driver circuitry 1114A, whereas the enable signal 1124 couples to the replica of the data receiver circuitry 1120A.

Note that FIG. 11B constitutes a conceptual block diagram of the delay-cell circuitry 1119. Rather than using distinct blocks 1114A and 1120A, one may alternatively use a single block that combines the functionality of those two blocks, as desired. Moreover, one may use a circuit that provides an adjustable, rather than fixed, delay, as desired. Note also that the embodiment 1100B of the delay-cell circuitry 1119 preferably compensates for the delay in the clock driver circuitry 1114 in FIG. 11A. In other words, the delay-cell circuitry 1119 preferably compensates sufficiently for the round-trip delay in the signals that travel from the receiver digital circuitry 905 to the receiver analog circuitry 910 and back to the receiver digital circuitry 905 to allow for accurate sampling in the receiver digital circuitry of the I-channel data and the Q-channel data.

The receiver digital circuitry 905 and the receiver analog circuitry 910 preferably reside within separate integrated-circuit devices. Because those integrated-circuit devices typically result from separate semiconductor fabrication processes and manufacturing lines, their process parameters may not match closely. As a result, the preferred embodiment 1100B of the delay-cell circuitry 1119 does not compensate for the delay in the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120 in FIG. 11A.

Note, however, that if desired, the delay-cell circuitry 1119 may also compensate for the signal delays of the clock receiver circuitry 1130, the data driver circuitry 1154, and the data receiver circuitry 1120. Thus, in situations where one may match the process parameters of the receiver digital circuitry 905 and the receiver analog circuitry 910 relatively closely (for example, by using thick-film modules, silicon-on-insulator, etc.), the delay-cell circuitry 1119 may also compensate for the delays of other circuit blocks. As another alternative, one may use a delay-cell circuitry 1119 that provides an adjustable delay and then program the delay based on the delays in the receiver digital circuitry 905 and the receiver analog circuitry 910 (e.g., provide a matched set

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of receiver digital circuitry 905 and receiver analog circuitry 910), as persons skilled in the art would understand. Furthermore, rather than an open-loop arrangement, one may use a closed-loop feedback circuit implementation (e.g., by using a phase-locked loop circuitry) to control and compensate for the delay between the receiver analog circuitry 910 and the receiver digital circuitry 905, as desired.

Note that the digital circuit blocks shown in FIGS. 11A and 11B depict mainly the conceptual functions and signal flow. The actual circuit implementation may or may not contain separately identifiable hardware for the various functional blocks. For example, one may combine the functionality of various circuit blocks into one circuit block, as desired.

FIG. 12 shows a schematic diagram of a preferred embodiment 1200 of a signal-driver circuitry according to the invention. One may use the signal-driver circuitry as the clock driver circuitry 1114 and the data driver circuitry 1154 in FIG. 11A. In the latter case, the input signals to the signal-driver circuitry constitute the output signals 1152 and the enable signal 1156, whereas the output signals of the signal-receiver circuitry constitute the ION and IOP signals 960 and 965, respectively, in FIG. 11A.

The signal-driver circuitry in FIG. 12 constitutes two circuit legs. One circuit leg includes MOSFET devices 1218 and 1227 and resistor 1230. The second leg includes MOSFET devices 1242 and 1248 and resistor 1251. The input clock signal controls MOSFET devices 1218 and 1242. Current source 1206, MOSFET devices 1209 and 1215, and resistor 1212 provide biasing for the two circuit legs.

MOSFET devices 1227 and 1248 drive the CKN and CKP output terminals through resistors 1230 and 1251, respectively. Depending on the state of the clock signal, one leg of the signal-driver circuitry conducts more current than the other leg. Put another way, the signal-driver circuitry steers current from one leg to the other in response to the clock signal. As a result, the signal-driver circuitry provides a differential clock signal that includes current signals CKN and CKP.

If the enable signal is high, MOSFET device 1203 is off and therefore does not affect the operation of the rest of the circuit. In that case, a current  $I_O$  flows through the current source 1206 and diode-connected MOSFET device 1209. The flow of current generates a voltage at the gate of MOSFET device 1209. MOSFET devices 1227 and 1248 share the same gate connection with MOSFET device 1209. Thus, MOSFET devices 1227 and 1248 have the same gate-source voltage,  $V_{gs}$ , as MOSFET device 1209 when the appropriate MOSFET devices are in on state.

MOSFET devices 1218 and 1242 cause current steering between the first and second circuit legs. Only one of the MOSFET devices 1218 and 1242 is in the on state during the operation of the circuit. Depending on which MOSFET device is in the on state, the mirroring current  $I_O$  flows through the circuit leg that includes the device in the on state.

Resistors 1221 and 1239 provide a small trickle current to the circuit leg that includes the MOSFET device (i.e., MOSFET device 1218 or MOSFET device 1242) that is in the off state. The small trickle current prevents the diode-connected MOSFET devices in the signal receiver circuitry (see FIG. 13) from turning off completely. The trickle current helps to reduce the delay in changing the state of the circuit in response to transitions in the input clock signal. The trickle currents also help to reduce transient signals at the CKP and CKN terminals and, thus, reduce interference effects.

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Capacitors **1224** and **1245** provide filtering so that when MOSFET device **1218** and MOSFET device **1242** switch states, the currents through the first and second circuit legs (CKN and CKP circuit legs) do not change rapidly. Thus, capacitors **1224** and **1245** reduce the high-frequency content in the currents flowing through the circuit legs into the CKN and CKP terminals. The reduced high-frequency (i.e., band-limited) content of the currents flowing through the CKN and CKP terminals helps reduce interference effects to other parts of the circuit, for example, the LNA circuitries, as described above. Capacitors **1233** and **1236** and resistors **1230** and **1251** help to further reduce the high-frequency content of the currents flowing through the CKN and CKP terminals. Thus, the circuit in FIG. **12** provides smooth steering of current between the two circuit legs and therefore reduces interference effects with other circuitry.

When the enable signal goes to the low state, MOSFET device **1203** turns on and causes MOSFET device **1209** to turn off. MOSFET devices **1227** and **1248** also turn off, and the circuit becomes disabled. Note that the enable signal may be derived from the power-down PDNB signal.

FIG. **13** shows a schematic diagram of a preferred embodiment **1300** of a signal-receiver circuitry according to the invention. One may use the signal-receiver circuitry as the clock receiver circuitry **1130** and the data receiver circuitry **1120** in FIG. **11A**. In the latter case, the input signals to the signal-receiver circuitry constitute the ION and IOP signals **960** and **965** and the enable signal **1124**, whereas the output signals constitute the signals at the outputs **1122A** and **1122B**, respectively, in FIG. **11A**.

The signal receiver circuitry in FIG. **13** helps to convert differential input currents into CMOS logic signals. The signal-receiver circuitry in FIG. **13** constitutes two circuit legs. The first circuit leg includes MOSFET devices **1303**, **1342**, and **1345**. The second leg includes MOSFET devices **1309**, **1324**, and **1327**. Note that, preferably, the scaling of MOSFET devices **1303** and **1309** provides a current gain of 1:2 between them. Likewise, the scaling of MOSFET devices **1330** and **1327** preferably provides a current gain of 1:2 between them. The current gains help to reduce phase noise in the signal-receiver circuitry.

MOSFET devices **1339**, **1342**, **1333**, and **1324** provide enable capability for the circuit. When the enable input is in the high state, MOSFET devices **1339**, **1342**, **1333**, and **1324** are in the on state. MOSFET devices **1345** and **1336** are current mirrors, as are MOSFET devices **1303** and **1309**. MOSFET devices **1330** and **1327** also constitute current mirrors.

The currents flowing through the CKN and CKP terminals mirror to the MOSFET devices **1327** and **1309**. The actual current flowing through the second circuit leg depends on the currents that MOSFET device **1327** and MOSFET device **1309** try to conduct; the lower of the two currents determines the actual current that flows through the second circuit leg.

The difference between the currents that MOSFET device **1327** and MOSFET device **1309** try to conduct flows through the parasitic capacitance at node **1360**. The current flow charges or discharges the capacitance at node **1360**, thus making smaller the drain-source voltage ( $V_{ds}$ ) of whichever of MOSFET devices **1327** and **1309** that seeks to carry the higher current. Ultimately, the lower of the currents that MOSFET devices **1327** and **1309** seek to conduct determines the current through the second leg of the circuit.

A pair of inverters **1312** and **1315** provide true and complement output signals **1351** and **1348**, respectively. The

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signal receiver circuitry therefore converts differential input currents into CMOS logic output signals.

FIG. **14** shows an embodiment **1400** of an alternative signal-driver circuitry according to the invention. The signal-driver circuitry in FIG. **14** includes two circuit legs. The first circuit leg includes MOSFET device **1406** and resistor **1415A**. The second circuit leg includes MOSFET device **1409** and resistor **1415B**. A current source **1403** supplies current to the two circuit legs.

The input clock signal controls MOSFET devices **1406** and **1409**. MOSFET devices **1406** and **1409** drive the CKP and CKN output terminals, respectively. Depending on the state of the clock signal, one leg of the signal-driver circuitry conducts current. Put another way, the signal-driver circuitry steers current from one leg to the other in response to the clock signal. As a result, the signal-driver circuitry provides a differential clock signal that includes signals CKN and CKP. Capacitor **1412** filters the output signals CKN and CKP. Put another way, capacitor **1412** provides band-limiting of the output signals CKN and CKP. Note that the current source **1403** supplies limited-amplitude signals by providing current through resistors **1415A** and **1415B**.

Note that the signal-driver circuitries (clock driver and data driver circuitries) according to the invention preferably provide current signals CKN and CKP. Similarly, signal-receiver circuitries (clock receiver and data receiver circuitries) according to the invention preferably receive current signals. As an alternative, one may use signal-driver circuitries that provide as their outputs voltage signals, as desired. One may also implement signal-receiver circuitries that receive voltage signals, rather than current signals. As noted above, depending on the application, one may limit the frequency contents of those voltage signals, for example, by filtering, as desired.

Generally, several techniques exist for limiting noise, for example, digital switching-noise, in the interface between the receiver analog circuitry and the receiver digital circuitry according to the invention. Those techniques include using differential signals, using band-limited signals, and using amplitude-limited signals. RF apparatus according to the invention may use any or all of those techniques, as desired. Furthermore, one may apply any or all of those techniques to interface circuitry that employs voltage or current signals, as persons of ordinary skill in the art who have read this description of the invention will understand.

Note also that the RF transceiver embodiments according to the invention lend themselves to various choices of circuit implementation, as a person skilled in the art would understand. For example, as noted above, each of the circuit partitions, or circuit blocks, of RF transceivers partitioned according to the invention, resides preferably within an integrated circuit device. Persons skilled in the art, however, will appreciate that the circuit partitions, or circuit blocks, may alternatively reside within other substrates, carriers, or packaging arrangements. By way of illustration, other partitioning arrangements may use modules, thin-film modules, thick-film modules, isolated partitions on a single substrate, circuit-board partitions, and the like, as desired, consistent with the embodiments of the invention described here.

One aspect of the invention contemplates partitioning RF transceivers designed to operate within several communication channels (e.g., GSM, PCS, and DCS). Persons skilled in the art, however, will recognize that one may partition according to the invention RF transceivers designed to operate within one or more other channels, frequencies, or frequency bands, as desired.

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Moreover, the partitioning of RF transceivers according to the invention preferably applies to RF apparatus (e.g., receivers or transceivers) with a low-IF, digital-IF architecture. Note, however, that one may apply the partitioning and interfacing concepts according to the invention to other RF receiver or transceiver architectures and configurations, as persons of ordinary skill in the art will understand. By way of illustration, one may use the partitioning and interface concepts according to the invention in RF apparatus that includes:

- low-IF receiver circuitry;
- low-IF receiver circuitry and offset-PLL transmitter circuitry;
- low-IF receiver circuitry and direct up-conversion transmitter circuitry;
- direct-conversion receiver circuitry;
- direct-conversion receiver circuitry and offset-PLL transmitter circuitry; or
- direct-conversion receiver circuitry and direct up-conversion transmitter circuitry.

As an example of the flexibility of the partitioning concepts according to the invention, one may include the LO circuitry in one partition, the receiver digital circuitry in a second partition, and the transmitter up-converter circuitry and the receiver analog circuitry in a third partition. As another illustrative alternative, one may include the LO circuitry and the transmitter up-converter circuitry within one circuit partition, depending on the noise and interference characteristics and specifications for a particular implementation.

Note that, in a typical direct-conversion RF receiver or transceiver implementation, the receiver digital circuitry would not include the digital down-converter circuitry (the receiver analog circuitry, however, would be similar to the embodiments described above). Furthermore, in a typical direct up-conversion transmitter circuitry, one would remove the offset PLL circuitry and the transmit VCO circuitry from the transmitter circuitry. The LO circuitry would supply the RF LO signal to the up-conversion circuitry of the transmitter circuitry, rather than the offset-PLL circuitry. Also, in a direct up-conversion implementation, the LO circuitry typically does not provide an IF LO signal.

Furthermore, as noted above, one may use the partitioning and interface concepts according to the invention not only in RF transceivers, but also in RF receivers for high-performance applications. In such RF receivers, one may partition the receiver as shown in FIGS. 2A–2D and 4–8, and as described above. In other words, the RF receiver may have a first circuit partition that includes the receiver analog circuitry, and a second circuit partition that includes the receiver digital circuitry.

The RF receiver may also use the digital interface between the receiver analog circuitry and the receiver digital circuitry, as desired. By virtue of using the receiver analog circuitry and the receiver digital circuitry described above, the RF receiver features a low-IF, digital-IF architecture. In addition, as noted above with respect to RF transceivers according to the invention, depending on performance specifications and design goals, one may include all or part of the local oscillator circuitry within the circuit partition that includes the receiver analog circuitry, as desired. Partitioning RF receivers according to the invention tends to reduce the interference effects between the circuit partitions.

As noted above, although RF apparatus according to the invention use a serial interface between the receiver analog circuitry and the receiver digital circuitry, one may use other

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types of interface, for example, parallel interfaces, that incorporate different numbers of signal lines, different types and sizes of signals, or both, as desired. Moreover, the clock driver circuitries and the data driver circuitries may generally constitute signal-driver circuitries that one may use in a variety of digital interfaces between the receiver analog circuitry and the receiver digital circuitry according to the invention.

Likewise, the clock receiver circuitries and data receiver circuitries may generally constitute signal-receiver circuitries that one may use in a variety of digital interfaces between the receiver analog circuitry and the receiver digital circuitry according to the invention. In other words, one may use signal-driver circuitries and signal-receiver circuitries to implement a wide variety of digital interfaces, as persons of ordinary skill who have read the description of the invention will understand.

Further modifications and alternative embodiments of this invention will be apparent to persons skilled in the art in view of this description of the invention. Accordingly, this description teaches those skilled in the art the manner of carrying out the invention and are to be construed as illustrative only.

The forms of the invention shown and described should be taken as the presently preferred embodiments. Persons skilled in the art may make various changes in the shape, size and arrangement of parts without departing from the scope of the invention described in this document. For example, persons skilled in the art may substitute equivalent elements for the elements illustrated and described here. Moreover, persons skilled in the art who have the benefit of this description of the invention may use certain features of the invention independently of the use of other features, without departing from the scope of the invention.

We claim:

1. A radio-frequency (RF) transceiver, comprising:

a first circuit partition, comprising:

receiver analog circuitry configured to accept a received RF signal and to provide at least one digital output signal; and

transmitter circuitry configured to receive at least one transmit input signal and to provide a transmit RF signal;

a second circuit partition, comprising local-oscillator circuitry configured to accept a reference signal, the local oscillator circuitry further configured to provide a radio-frequency (RF) signal to the receiver analog circuitry and to the transmitter circuitry, wherein the first circuit partition and the second circuit partition are partitioned so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

2. The transceiver of claim 1, in which the transmitter circuitry within the first circuit partition comprises transmit voltage-controlled oscillator (VCO) circuitry.

3. The transceiver of claim 2, in which the receiver analog circuitry provides the at least one digital output signal to baseband processor circuitry external to both the first and second circuit partitions.

4. The transceiver of claim 3, in which the receiver analog circuitry comprises:

analog down-converter circuitry configured to accept the received RE signal, the down-converter circuitry further configured to provide an analog down-converted signal; and

analog-to-digital converter (ADC) circuitry coupled to the baseband processor circuitry, the analog-to-digital con-

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verter circuitry configured to receive the analog down-converted signal, the analog-to-digital circuitry further configured to provide the at least one digital output signal of the receiver analog circuitry.

5. The transceiver of claim 4, which the transmitter circuitry comprises baseband up-converter circuitry configured to accept the at least one transmit input signal, the baseband up-converter circuitry further configured to provide an intermediate frequency (IF) signal to offset phase-lock loop (PLL) circuitry coupled to the transmit voltage-controlled oscillator circuitry.

6. The transceiver of claim 5, comprising reference generator circuitry external to both the first and second circuit partitions, the reference generator circuitry configured to provide the reference signal to the second circuit partition.

7. The transceiver of claim 6, in which the reference generator circuitry resides within the baseband processor circuitry.

8. The transceiver of claim 6, in which the baseband processor circuitry receives the at least one digital output signal of the receiver analog circuitry, and in which the baseband processor circuitry provides the at least one transmit input signal to the baseband up-converter circuitry.

9. The transceiver of claim 8, in which the first circuit partition resides within a first integrated circuit device and the second circuit partition resides within a second integrated circuit device.

10. The transceiver of claim 2, comprising a third circuit partition that includes receiver digital circuitry configured to receive the at least one digital output signal of the receiver analog circuitry, wherein the first, second, and third circuit partitions are partitioned so that interference effects among the first, second, and third circuit partitions tend to be reduced.

11. The transceiver of claim 10, in which in which the receiver analog circuitry comprises:

analog down-converter circuitry configured to accept the received RF signal, the down-converter circuitry further configured to provide an analog down-converted signal; and

analog-to-digital converter (ADC) circuitry configured to receive the analog down-converted signal, the analog-to-digital circuitry further configured to provide the at least one digital output signal of the receiver analog circuitry.

12. The transceiver of claim 11, in which the receiver digital circuitry comprises:

digital down-converter circuitry configured to accept the at least one digital output signal of the receiver analog circuitry, the digital down-converter circuitry further configured to provide at least one digital down-converted signal; and

digital filter circuitry configured to receive the at least one digital down-converted digital signal, the digital filter circuitry further configured to provide at least one digital filtered signal.

13. The transceiver of claim 12, which the transmitter circuitry comprises baseband up-converter circuitry configured to accept the at least one transmit input signal, the baseband up-converter circuitry further configured to provide an intermediate frequency (IF) signal to offset phase-lock loop (PLL) circuitry coupled to the transmit voltage-controlled oscillator circuitry.

14. The transceiver of claim 13, comprising reference generator circuitry external to the first, second, and third circuit partitions, the reference generator circuitry configured to provide the reference signal to the second and third circuit partitions.

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15. The transceiver of claim 14, in which external baseband processor circuitry receives the at least one filtered digital signal of the digital filter circuitry, and in which the baseband processor circuitry provides to the baseband up-converter circuitry the at least one transmit input signal.

16. The transceiver of claim 15, in which the reference generator circuitry resides within the baseband processor circuitry.

17. The transceiver of claim 16, in which the first circuit partition resides within a first integrated circuit device, the second circuit partition resides within a second integrated circuit device, and the third circuit partition resides within a third integrated circuit device.

18. The transceiver of claim 14, in which the receiver digital circuitry comprises digital-to-analog converter (DAC) circuitry configured to accept from the digital filter circuitry the at least one filtered digital signal, the digital-to-analog-converter circuitry configured to provide at least one analog receive signal.

19. The transceiver of claim 18, which the first circuit partition resides within a first integrated circuit device, the second circuit partition resides within a second integrated circuit device, and the third circuit partition resides within a third integrated circuit device.

20. A method of partitioning radio-frequency (RF) transceiver circuitry, comprising:

providing a first circuit partition that includes a receiver analog circuitry and a transmitter circuitry;

utilizing the receiver analog circuitry to accept a received RF signal and to provide at least one digital output signal;

utilizing the transmitter circuitry to receive at least one transmit input signal and to provide a transmit RF signal;

providing a second circuit partition that includes local-oscillator circuitry;

utilizing the local-oscillator circuitry to accept a reference signal, and to provide a radio-frequency (RF) signal to the receiver analog circuitry and to the transmitter circuitry; and

partitioning the first circuit partition and the second circuit partition so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.

21. The method of claim 20, which further comprises including within the transmitter circuitry a transmit voltage-controlled oscillator (VCO) circuitry.

22. The method of claim 21, which further includes utilizing the receiver analog circuitry to provide the at least one digital output signal to baseband processor circuitry external to both the first and second circuit partitions.

23. The method of claim 22, which further includes:

including analog down-converter circuitry within the receiver analog circuitry;

utilizing the analog down-converter circuitry to accept the received RF signal and to supply an analog down-converted signal;

providing analog-to-digital converter (ADC) circuitry within the receiver analog circuitry;

coupling the analog-to-digital converter circuitry to the baseband processor circuitry; and

utilizing the analog-to-digital converter circuitry to receive the analog down-converted signal and to supply the at least one digital output signal of the receiver analog circuitry.

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**24.** The method of claim **23**, which further includes:  
 providing offset phase-lock loop (PLL) circuitry;  
 coupling the offset phase-lock loop circuitry to the transmit voltage-controlled oscillator circuitry;  
 including within the transmitter circuitry a baseband up-converter circuitry; and  
 utilizing the baseband up-converter circuitry to accept the at least one transmit input signal and to supply an intermediate frequency (IF) signal to the offset phase-lock loop circuitry. 5

**25.** The method of claim **24**, which further comprises:  
 providing reference generator circuitry external to both the first and second circuit partitions; and  
 utilizing the reference generator circuitry to provide the reference signal to the second circuit partition. 15

**26.** The method of claim **25**, which further comprises including the reference generator circuitry within the baseband processor circuitry.

**27.** The method of claim **25**, which further includes utilizing the baseband processor circuitry to receive the at least one digital output signal of the receiver analog circuitry and to supply the at least one transmit input signal to the baseband up-converter circuitry. 20

**28.** The method of claim **27**, which further includes:  
 integrating the first circuit partition within a first integrated circuit device; and  
 integrating the second circuit partition within a second integrated circuit device. 25

**29.** The method of claim **21**, which further comprises:  
 providing a third circuit partition that includes receiver digital circuitry;  
 utilizing the receiver digital circuitry to receive the at least one digital output signal of the receiver analog circuitry; and  
 partitioning the first, second, and third circuit partitions so that interference effects among the first, second, and third circuit partitions tend to be reduced. 30

**30.** The method of claim **29**, which further comprises:  
 providing analog down-converter circuitry within the receiver analog circuitry;  
 utilizing the analog down-converter circuitry to accept the received RF signal and to supply an analog down-converted signal; 35

providing analog-to-digital converter (ADC) circuitry within the receiver analog circuitry; and  
 converting the analog down-converted signal into the at least one digital output signal of the receiver analog circuitry by using the analog-to-digital converter circuitry. 40

**31.** The method of claim **30**, which further comprises:  
 providing digital down-converter circuitry within the receiver digital circuitry; 45

utilizing the digital down-converter circuitry to accept the at least one digital output signal of the receiver analog circuitry and to supply at least one digital down-converted signal; 50

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providing digital filter circuitry within the receiver digital circuitry; and  
 filtering the at least one digital down-converted digital signal by using the digital filter circuitry to produce at least one digital filtered signal.

**32.** The method of claim **31**, which further comprises:  
 providing offset phase-lock loop (PLL) circuitry;  
 coupling the offset phase-lock loop circuitry to the transmit voltage-controlled oscillator circuitry;  
 including baseband up-converter circuitry within the transmitter circuitry; and  
 utilizing the baseband up-converter circuitry to accept the at least one transmit input signal and to supply an intermediate frequency (IF) signal to the offset phase-lock loop circuitry.

**33.** The method of claim **32**, which further includes:  
 providing reference generator circuitry external to the first, second, and third circuit partitions; and  
 utilizing the reference generator circuitry to provide the reference signal to the second and third circuit partitions.

**34.** The method of claim **35**, which further includes:  
 providing external baseband processor circuitry; and  
 utilizing the external baseband processor circuitry to receive the at least one filtered digital signal of the digital filter circuitry and to supply to the baseband up-converter circuitry the at least one transmit input signal.

**35.** The method of claim **34**, which further comprises providing the reference generator circuitry within the baseband processor circuitry.

**36.** The method of claim **35**, which further comprises:  
 integrating the first circuit partition within a first integrated circuit device;  
 integrating the second circuit partition within a second integrated circuit device; and  
 integrating the third circuit partition within a third integrated circuit device.

**37.** The method of claim **33**, which further comprises:  
 providing digital-to-analog converter (DAC) circuitry within the receiver digital circuitry; and  
 utilizing the digital-to-analog converter circuitry to accept from the digital filter circuitry the at least one filtered digital signal and to provide at least one analog receive signal.

**38.** The method of claim **37**, which further comprises:  
 integrating the first circuit partition within a first integrated circuit device;  
 integrating the second circuit partition within a second integrated circuit device; and  
 integrating the third circuit partition within a third integrated circuit device.

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