

SILICON LABORATORIES, INC.
Petitioner

v.

CRESTA TECHNOLOGY CORPORATION
Patent Owner

IPR2015-00615
Patent No. 7,075,585

Trial Hearing: June 1, 2016
Petitioner's Demonstrative Exhibits



Ground 2: Claims 13, 15 and 20 are Obvious

Thomson (Ex. 1004) + Harris (Ex. 1005) + Zenith (Ex. 1011)

Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 696 854 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication: 14.02.1996 Bulletin 1996/07

(51) Int. Cl.: H04B 1/26, H04B 1/16

(21) Application number: 95111940.3

(22) Date of filing: 29.07.1995

(84) Designated Contracting States: DE FR GB IT

(30) Priority: 06.08.1994 EP 94401828

(71) Applicant: THOMSON multimedia S.A. F-92400 Courbevoie (FR)

(72) Inventor: Bole, Werner F-67100 Strasbourg (FR)

(74) Representative: Hartmann, Wolfgang, Dipl.-Ing. D-30453 Hannover (DE)

(54) Broadcast receiver adapted for analog and digital signals

(57) Background:
Digital satellite TV broadcasting systems use an analog IF input followed by an analog QPSK-demodulator and analog baseband filters prior to A/D conversion. Normally, two A/D converters would be required for digital demodulation of the in phase and the quadrature component.

Advantages
Allows multi-standard front-end architecture, architecture is suited for digital and analogue input signals, the possible net data rate around 40Mbits/s is even higher than required for DircatV.

Cost of the invention
A first IF frequency of about 2 GHz and a second IF of about 140 MHz allows to demodulate FM signals of 27 MHz bandwidth. A subsequent local 70 MHz local oscillator is followed by a lowered resolution A/D converter operating at about 100 MHz sampling frequency in a subsampling mode. A single A/D converter (7) is required only and allows high quality FM demodulation.

EP 0 696 854 A1

Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1004

A Digital Tuner for Wideband Receivers

Figure 1: High level block diagram of a single channel receiver

By Guy Olmstead and Mike Petrowski

Advances in both analog to digital conversion (ADC) and VLSI technologies have opened the door for the use of DSP techniques over an expanding range of high sample rate applications. Foremost among these is the use of standard off the shelf DSP IC's as digital replacements for the analog intermediate frequency (IF) processing stage in wideband receivers. Using this approach, the designer can take advantage of operational stability over time and temperature offered by digital technology, while realizing performance and flexibility unobtainable by older analog implementations.

In recent years there has been increasing interest in the topic of wideband receivers. These are receivers that can tune on a narrow band radio signal that exists in a broad spectrum of interest. The typical system in this application may be capable of extracting a signal as narrow as a few kHz out of a spectrum that spans tens, hundreds, or even thousands of MHz.

Because of the prohibitive cost of these receivers in the past, they were confined to use by the military, government agencies, and high end commercial users. Today, however, more widespread commercial communications systems are dependent on cost effective implementations of receivers. Cellular telephones, mobile radio, and wireless LANs are but a few examples of potential applications for DSP.

To better understand alternative wideband receiver designs using DSP, first consider the structure of the single channel wideband receiver as shown in Figure 1. As implied by the name, the single channel receiver is designed to receive and decode information within a single frequency band at a time. For the purposes of this discussion it will be assumed that one frequency band corresponds to one channel with no distinction between a frequency band and logical channels. When information is to be recovered from a different channel, the receiver must be tuned to the new

Today, more widespread commercial communications systems depend on cost effective implementations of these receivers.

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Silabs IPR Exhibit 1005

US06037731B1

(12) United States Patent Mycynek et al.

(10) Patent No.: US 6,377,316 B1

(45) Date of Patent: Apr. 23, 2002

(54) TUNER WITH SWITCHED ANALOG AND DIGITAL MODULATORS

(57) Abstract
A television receiver includes a tuner for receiving either analog or digital signals. Separate analog and digital demodulators are selectively coupled to the tuner through an RF switch that is controlled by the signal from a sync detector in the output of the analog demodulator. The selected one of the demodulators develops an AGC signal that is coupled to the tuner through a current mirror. Operating potential for the demodulators is coupled through the RF switch so that the oscillator in the non-selected demodulator is disabled and precluded from interfering with the oscillator in the enabled demodulator.

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/152,399

(22) Filed: Sep. 14, 1998

Related U.S. Application Data
(63) Continuation-in-part of application No. 09/027,608, filed on Feb. 23, 1998.

(51) Int. Cl.⁷ H04N 5/44, H04N 5/26, H04N 5/52

(52) U.S. Cl. 348/731, 348/725, 348/678, 348/705, 348/733, 348/636, 348/639, 348/725, 726, 348/731, 735, 678, 636, 639, 705, 706, 732, 733, 10, 740, 455/553, 245.1, 246.1, 247.1, 337, 214; H04N 5/44, 5/50, 5/26, 5/56, 5/52

(58) Field of Search 348/731, 348/725, 348/678, 348/705, 348/733, 348/636, 348/639, 348/725, 726, 348/731, 735, 678, 636, 639, 705, 706, 732, 733, 10, 740, 455/553, 245.1, 246.1, 247.1, 337, 214; H04N 5/44, 5/50, 5/26, 5/56, 5/52

9 Claims, 2 Drawing Sheets

Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1011

Exs. 1004, 1005, and 1011

Silicon Laboratories, Inc.
Exhibit 1065 - 2

Claim Construction: “Select Signal”

Petitioner’s Construction	Patent Owner’s Construction
Plain and ordinary meaning, i.e., “a select signal that serves as a sign or indication of or is suggestive of a format of said input RF signal.”	“A signal that performs a selection and that comprises information about the format of said input RF signal.”

Compare Petition at 22 (“plain and ordinary”), Paper No. 20 at 2-4 *with* Paper No. 16 at 6-10

Select Signal: Signal that is Indicative of the Format

13. The receiver of claim **10**, wherein said channel filter further comprises a standard selection circuit coupled to said signal processor, said standard selection circuit generating a **select signal** indicative of a format of said input RF signal and said signal processor selecting a finite impulse response filter in response to said select signal.

19. The method of claim **17**, wherein said processing said digital signals is performed in response to a **select signal** indicative of said format of said input RF signal.

Select Signal: Signal that is Indicative of the Format

14. The receiver of claim 13, wherein said standard selection circuit generates said **select signal** in response to an input signal from a user.

15. The receiver of claim 13, wherein said standard selection circuit generates said **select signal** by detecting carrier signals identifying one of said formats of said input RF signals.

20. The method of claim 19, further comprising:
generating said **select signal** by detecting carrier signals in said input RF signal identifying said format of said input RF signal.

Select Signal: Signal that is Indicative of the Format

The CASSELL DICTIONARY

indicative (-dik'ə-) *a.* **1** serving as a sign or indication (of); suggestive (of). **2** (*Gram.*) (of a mood of verbs) expressing fact. ~*n.* **1** the indicative mood. **2** a verb in this mood. **indicatively** *adv.*

indication (-ā'shən) *n.* **1** the act of indicating. **2** something which indicates or suggests. **3** something that is indicated as advisable or suitable. **4** a reading shown by a gauge etc.

■ *n.* **2** clue, evidence, explanation, forewarning, hint, index, inkling, intimation, manifestation, mark, note, omen, portent, sign, signal, suggestion, symbol, symptom, token, warning. **4** degree, measure, reading.

CASSELL

IPR2015-00615

Select Signal: Signal that is Indicative of the Format

- 3 the digital output signals according to one of the formats of the input RF signal and generates the corresponding video and audio baseband signals;
- 4 integrated tuner is a matter of design choice. In one embodiment, the IF is selected to be 20 MHz or higher.

FIG. 5 is a block diagram of a television signal processing system implemented in accordance with the present invention.

In accordance with the new standards, a television (TV) receiver must be equipped with a preselector filter that is able to receive televisions signals and filter out the signals and pass the signals in the digital domain. This filter eliminates the need for analog filters. Thus, digital filters can be readily integrated with the rest of the TV receiver circuitry, thereby eliminating the need for

FIG. 2 is a block diagram of a receiver according to one embodiment of the present invention. FIG. 2, taken in conjunction with FIG. 1, illustrates a receiver as those received in a mobile telephone input terminal. The receiver includes a tuner 54 which receives a radio signal from an intermediate frequency section 52. The receiver also includes a super-heterodyne converter 56, a discrete component section 58, and an intermediate frequency section 60. The receiver is also provided with a geographic region database 62 which is based on a geographic region.

In another embodiment, the IF is an integrated component of receiver 50. In that case, tuner 54 can be designed to generate intermediate signals having an intermediate frequency of any values. The IF used by tuner can be the same or different than the IF specified by the worldwide standards. More importantly, because TV receiver 50 includes a multi-standard channel filter 58, tuner 54 can use the same IF for receiving analog or digital television signals in any standards. The value of the IF is an

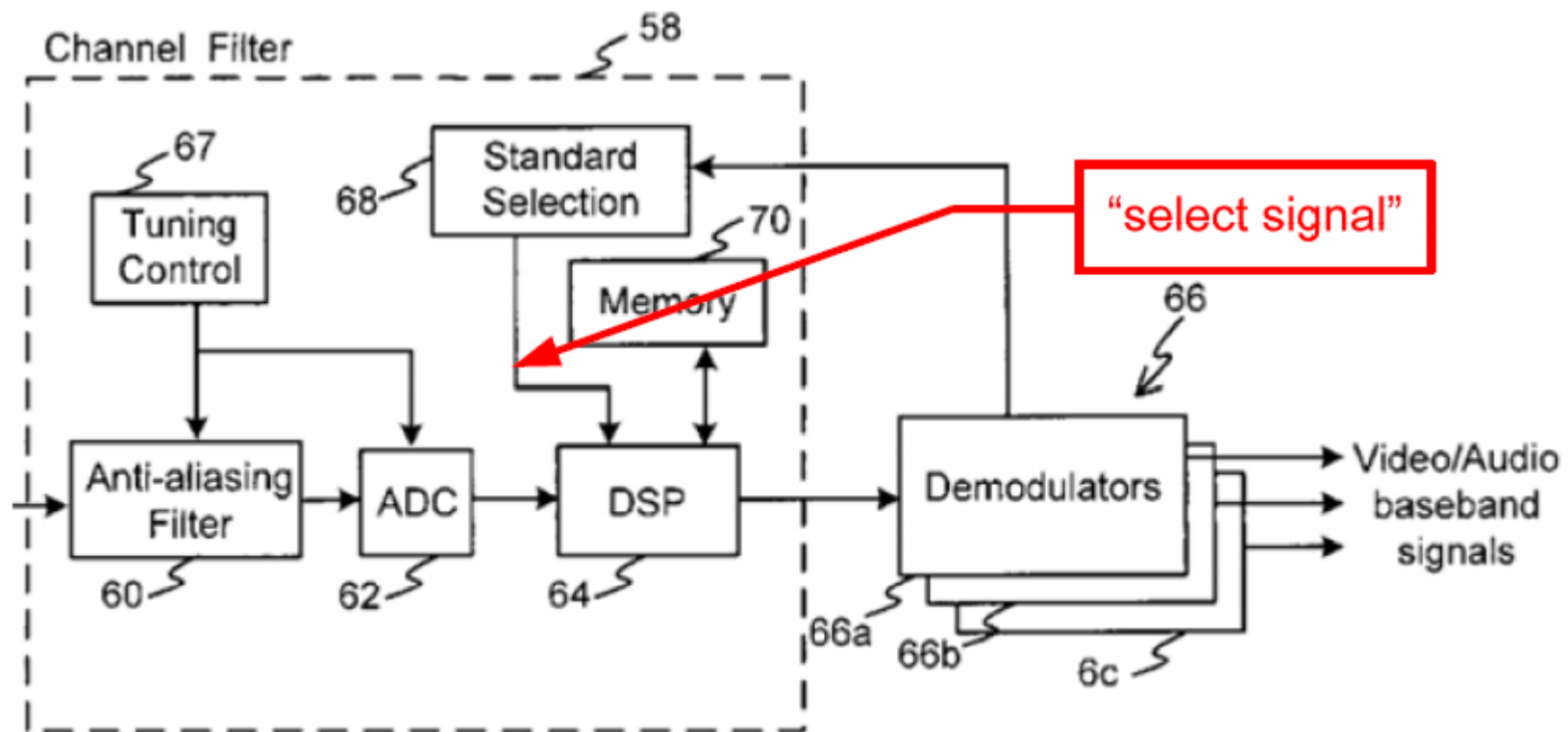
⁶⁵ depending on the state of standard selection circuit 68. In one embodiment, the coefficients of the filter functions are stored in a look-up table in a memory 70. DSP 64 retrieves the coefficients from memory 70 to be applied to the incoming digital signals.

⁶⁶ DSP 64 is a programmable and reconfigurable processor. In the present embodiment, DSP 64 implements a finite impulse response (FIR) filter which is reconfigurable based on

In the present embodiment, channel filter 58 includes a standard selection circuit 68 for selecting between the several analog television standards and the several digital television standards. DSP 64 applies the appropriate filter function, such as an impulse response, to the digital signals depending on the state of standard selection circuit 68. In one embodiment, the coefficients of the filter functions are stored in a look-up table in a memory 70. DSP 64 retrieves the coefficients from memory 70 to be applied to the incoming digital signals.

8

Select Signal: Generated by Selection Circuit



Select Signal: Signal that is Indicative of the Format

ION E. OPRIS, PH.D. - 01/13/2016	
1	UNITED STATES PATENT AND TRADEMARK OFFICE
2	BEFORE THE PATENT TRIAL AND APPEALS BOARD
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4	SILICON LABORATORIES, INC.,)
5)
6	
7	
8	4 Q. And it's also true that the signal processor
9	
10	5 selects a finite impulse response filter in response to
11	
12	6 said select signal, according to claim 13?
13	
14	
15	
16	
17	7 MR. HABER: Objection. Form.
18	
19	
20	8 THE WITNESS: That is correct.
21	
22	
23	
24	Reported by: PHILIP D. NORRIS
25	CSR NO. 4980
DTI Court Reporting Solutions - Woodland Hills 1-800-826-0277 www.deposition.com	
Silicon Labs Exhibit No. 1060 Silicon Laboratories v. Cresta Technology IPR2015-00615	

Select Signal: Signal that is Indicative of the Format

US 7,075,585 B2

the TV standard selected. Furthermore, in the present embodiment, DSP 64 includes two computing units to speed up the computation time. Specifically, the filtering operations of the real and imaginary parts in the frequency domain are carried out in parallel. In other embodiments, DSP 64 may include only one computing unit.

Standard selection circuit 68 can be implemented in one of many ways. The selection of the correct standard can be made manually by the user of the television system, such as by activating a switch, or the selection can be made automatically by providing an auto-detection capability in TV receiver 50. In the present embodiment, auto-detection is implemented by detecting in the baseband signals the presence or absence of carrier signals which uniquely identify the television standards. For example, analog television

such as a video and sound decoder, thereby providing compatibility with existing television components. An additional digital-to-analog converter may be coupled to the output terminal of demodulator 66a if analog output signals are desired. Digital demodulator 66b operates to decode the incoming digital television signal. Typically, digital television signals are modulated in a VSB, QAM or COFDM scheme. Digital

When the input RF signal is received by antenna 10, it is converted to a baseband signal by a tuner 20. The baseband signal is then processed by a DSP 64. DSP 64 applies a filter function to the digitized signals. The filter function is implemented as a FIR filter. The filter function is shown in FIG. 10. Other filter functions such as the interference of the signals then derived from the input signal.

The output signals from bank of demodulators 66 are video and audio baseband signals which are then decoded by decoders before being sent to the screen.

In the present embodiment, demodulator 66a provides three output signals: a Composite Video Baseband Signal (CVBS) containing the video information, and audio 1 and audio 2 containing the audio information. Audio 1 and audio 2 signals can be AM modulated, FM modulated or intercarrier signals. The intercarrier signal is a signal that can contain any format of modulated sound. It is usually connected to an external audio decoder. By using standard output signals, TV receiver 50 can readily interface with other standard components,

where analog demodulator 66b receives analog input signals and only a digital-to-analog converter (DAC) (not shown) can be included between the output terminal of DSP 64 and the input terminal of analog demodulator 66a.

Analog demodulator 66a provides three output signals: a Composite Video Baseband Signal (CVBS) containing the video information, and audio 1 and audio 2 containing the audio information. Audio 1 and audio 2 signals can be AM modulated, FM modulated or intercarrier signals. The intercarrier signal is a signal that can contain any format of modulated sound. It is usually connected to an external audio decoder. By using standard output signals, TV receiver 50 can readily interface with other standard components,

intermediate frequency (IF), said input RF signals encoding information in one of a plurality of formats; and a channel filter for receiving the intermediate signals, said channel filter comprising: an anti-aliasing filter for filtering said intermediate signals; an analog-to-digital converter for sampling said filtered intermediate signals and generating a digital representation thereof; a signal processor for processing said digital representation of said intermediate signals in accordance with said format of said input RF signal, said signal

Ex. 1001 at 5:7-15 (emphasis added); 1061 at 12-13

Silicon Laboratories, Inc.
Exhibit 1065 - 10

Zenith Generates a “Select Signal”

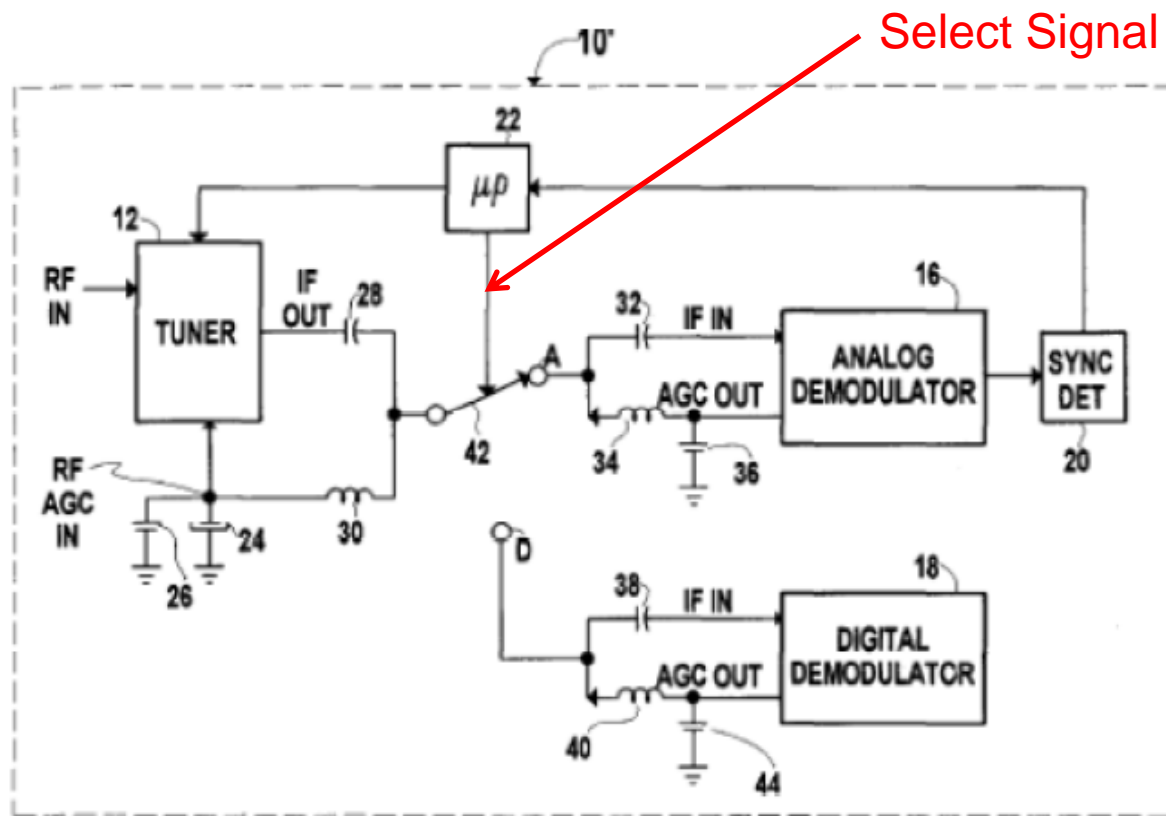
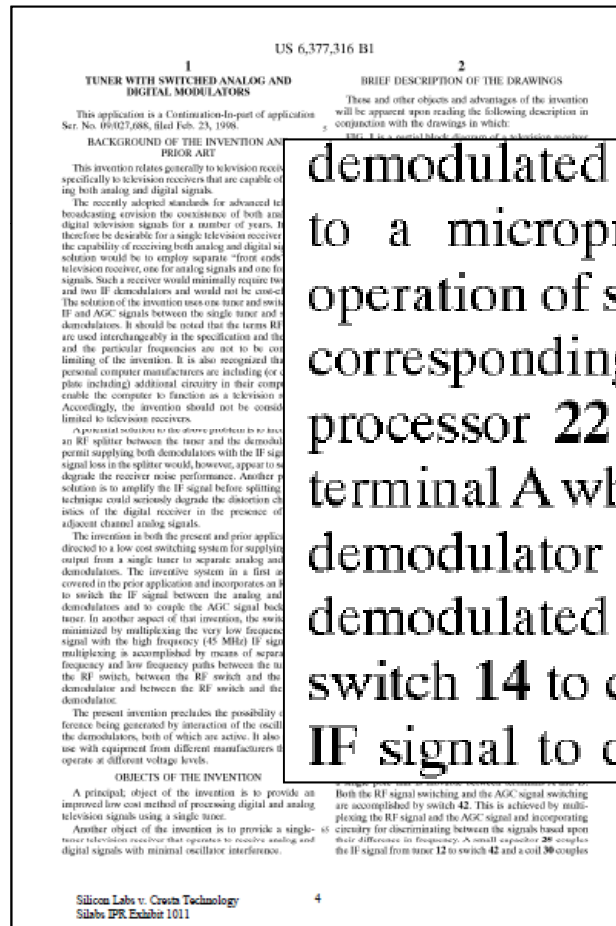


FIG. 2

Zenith Generates a "Select Signal"



demodulated analog signal. Sync separator **20** is connected to a microprocessor **22** that controls tuner **12** and the operation of switch **14**. Specifically, in the presence of syncs corresponding to a demodulated analog type signal, microprocessor **22** causes switch **14** to connect its pole **14a** to terminal A which routes the IF signal from tuner **12** to analog demodulator **16**. In the absence of syncs corresponding to a demodulated analog type signal, microprocessor causes switch **14** to connect its pole **14a** to terminal D to couple the IF signal to digital demodulator **18**.

Zenith Generates a “Select Signal”

85. The fact that Zenith infers the presence of the digital format in the absence of a valid sync signal, rather than affirmatively detects the digital signal, is irrelevant. The preferred embodiment of the standard selection circuit itself works “by detecting in the baseband signals the presence *or absence* of carrier signals which uniquely identify the television standards [sic: formats].” Ex. 1001 at 5:12-15 (emphasis added). The sync signal, like the examples given in the ’585 patent, “uniquely” identifies the analog television format from the digital television format. Thus, Dr. Opris cannot distinguish Zenith’s selection circuit on this basis without also excluding the ’585 patent’s own preferred embodiment.

Dr. Opris Agreed that a Single Bit would Suffice

ION E. OPRIS, PH.D. - 01/13/2016	
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19	WEDNESDAY
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24	Reported by: PHILIP D.
25	CSR NO. 4

17 Q. Okay. So in your opinion, how many bits does

18 this select signal need to be?

19 MR. HABER: Objection. Form.

20 THE WITNESS: Depends on the quantity of

21 information needed for the DSP.

23 Q. Okay. And in the '585 how many bits would that

24 be?

1 THE WITNESS: That information is not disclosed

2 in the '585 patent.

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1-800-826-0277

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Silicon Labs Exhibit No. 1060
Silicon Laboratories v. Cresta Technology
IPR2015-00615

Dr. Opris Agreed that a Single Bit would Suffice

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24	Reported by: PHILIP D. DEWITT
25	CSR NO. 4980
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Silicon Labs Exhibit No. 1060 Silicon Laboratories v. Cresta Technology IPR2015-00615	

4 Q. And you would agree with me that a single bit
5 can represent two states; correct?
6 A. Yes.

10 Q. A zero could represent one state; correct?
11 A. Yes.
12 Q. And a one could represent another state?
13 A. Yes.

Claim Construction: “Carrier Signals”

Petitioner’s Construction	Patent Owner’s Construction
Plain and ordinary meaning, i.e., “a wave having at least one characteristic that may be varied from a known reference value by modulation.”	“transmission carrier” (implicit)

Compare Petition at 22 (“plain and ordinary”), Paper No. 20 at 4-6 with Paper No. 16 at 40-44

Claim Construction: “Carrier Signals”

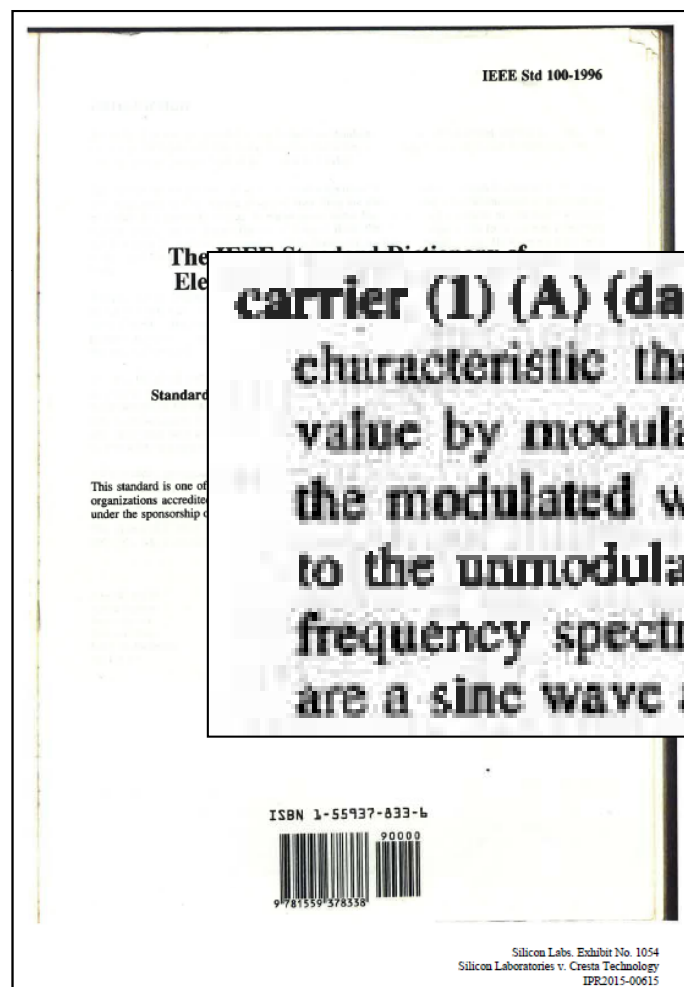
Case IPR2015-00615 Patent 7,075,585	
UNITED STATES BEFORE THE SILICON LABS CREST	what the particular carrier signal is. Nor does it explain how or why a “sync” could be a carrier signal. Silicon Labs cites no evidence for how or why a “sync” could be a carrier signal. Nor does it provide any rationale for why Zenith would use the terminology “sync” when it purportedly actually means a carrier signal.
Case IPR2015-00615 Patent 7,075,585	
PATENT	Silicon Labs has not proposed a construction for “carrier signal.” If Silicon Labs were correct that 5:12-15 of the ’585 patent provided a custom definition or lexicography of “carrier signal” that was the antithesis of the plain meaning of the term in the art, it should have proposed the term for construction, and by not doing so in the Petition it has waived its argument.
Mail Stop “PATENT BOARD” Patent Trial and Appeal Board U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

Claim Construction: “Carrier Signals”

15. The receiver of claim **13**, wherein said standard selection circuit generates said select signal by detecting **carrier signals** identifying one of said formats of said input RF signals.

20. The method of claim **19**, further comprising:
generating said select signal by detecting **carrier signals** in said input RF signal identifying said format of said input RF signal.

Claim Construction: “Carrier Signal”



Ex. 1054 at 134

Claim Construction: “Carrier Signal”

(12) **United States Patent**
Balaban et al.


(10) Patent No.: **US 6,369,857 B1**
(45) Date of Patent: **Apr. 9, 2002**

(54) **RECEIVER FOR TELEVISION SIGNALS**
(75) Inventors: **Alvin M. Balaban, Jr., et al.**
(73) Assignee: **Silicon Laboratories, Inc.**
(*) Notice: **See patent for details.**
(21) Appl. No.: **09/000,000**
(22) Filed: **Mar. 1, 2000**
(51) Int. Cl.: **H04N 01/00**
(52) U.S. Cl.: **348/731**
(58) Field of Search: **348/731**
(56) References:
U.S. Pat.
5,200,000 A
5,557,000 A
5,572,000 A
5,902,000 A
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GB 23380
WO 98/145
OTHER
Booth, Stephen A., "Digital Television Receivers," Mar. 1999, pp. 1-10, in: "Digital Television Receivers," T. Nelson, Ed., IEEE Press, 1999, pp. 1-10.
Date Handbook R2.2

receiver 50. In the present embodiment, auto-detection is implemented by detecting in the baseband signals the presence or absence of carrier signals which uniquely identify the television standards. For example, analog television signals can be identified by the analog visual carrier signal while digital television signals can be identified by the pilot carrier. Each demodulator in bank 66 generates a signal which is fed back to standard selection circuit 68 indicating which television standard the input signal is encoded. In other embodiments, other means for selecting between the different standards can be used.

Silicon Labs. Exhibit No. 1053
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Claim Construction: “Carrier Signal”


US907265792B2

(12) United States Patent
Favrat et al.

(54) TELEVISION RECEIVER
ANALOG TELEVISION

(75) Inventors: Pierre Favrat,
Alain-Serge P.
(US); Dominig
CA (US); Eric
Joue, CA (US);
San Jose, CA (US);
Santa Clara, CA;
Margulies, SA

(75) Assignee: Xerox Corp.
(US)

(*) Notice: Subject to any
patent is exten
U.S.C. 154(b)

(21) Appl. No.: 10884,347

(22) Filed: Jul. 1, 2004

(65) Prior Public
US 2006/0001779 A1

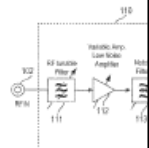
(51) Int. Cl.
H04N 5/27 (2006)
H04N 5/46 (2006)

(52) U.S. Cl.
348/558, 725, 726
455/180.1, 245.2

(58) Field of Classification See
See application file for con

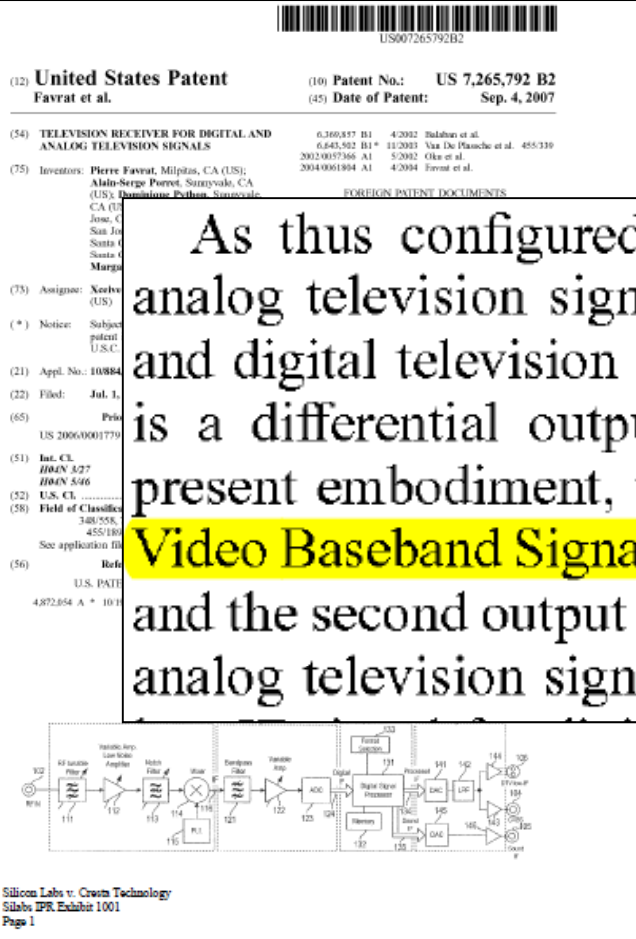
(56) References
U.S. PATENT DO
4,872,854 A * 10/1989 Gra

detection capability in receiver 100. In the present embodiment, auto-detection is implemented by detecting in the first and second output signals the presence or absence of carrier signals which uniquely identify the television formats and standards. For example, analog television signals can be identified by the analog visual carrier signal while digital television signals can be identified by the pilot carrier. A detection circuit can be included in receiver 100 for generating a signal which is fed back to format/standard selection circuit 133 indicating which television format and standard the input signal is encoded. In other embodiments, other means for selecting between the different formats and standards can be used.

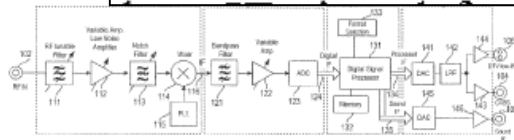


Silicon Labs v. Crown Technology
Silabs IPR Exhibit 1001
Page 1

Claim Construction: “Carrier Signal”



As thus configured, signal output circuit 140 provides analog television signals on output terminals 104 and 105 and digital television signals on output terminal 106 which is a differential output terminals (2 signal ports). In the present embodiment, the first output signal is a Composite Video Baseband Signal (CVBS) for analog television signals and the second output signal is the audio baseband signal for analog television signals. The third output signal is a DTV



Zenith Detects “Carrier Signals”

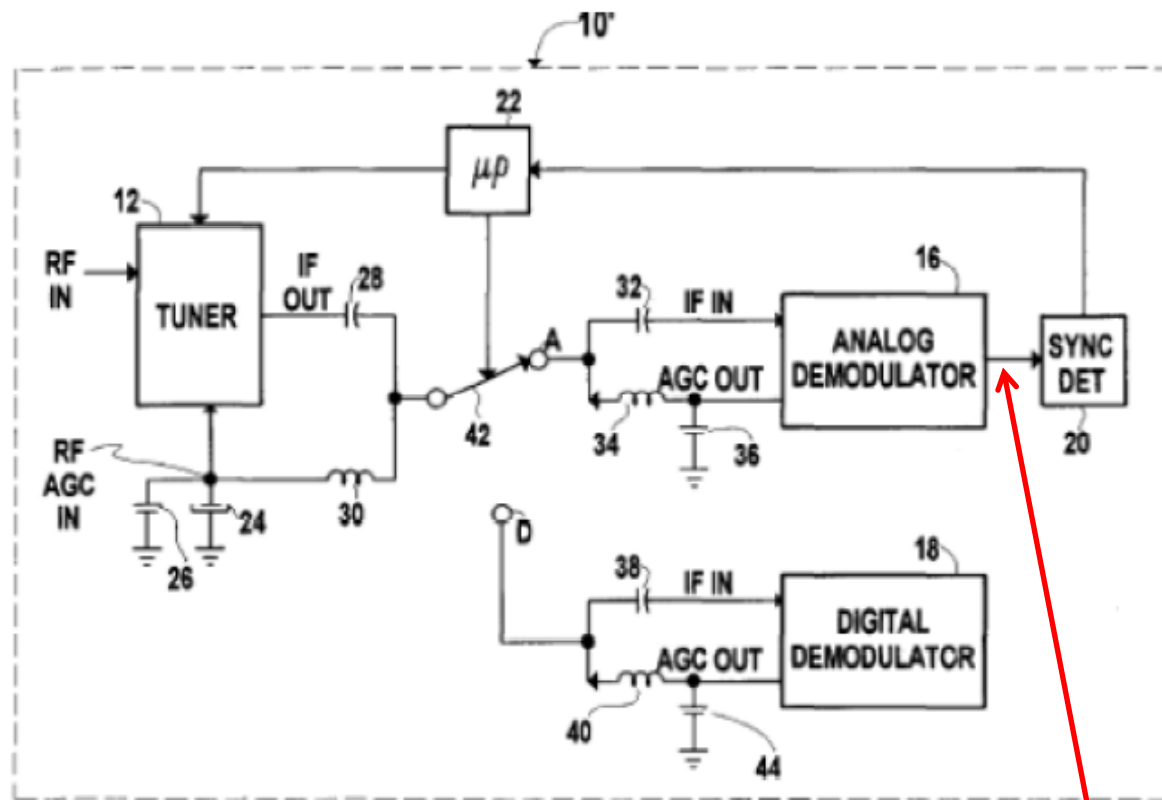


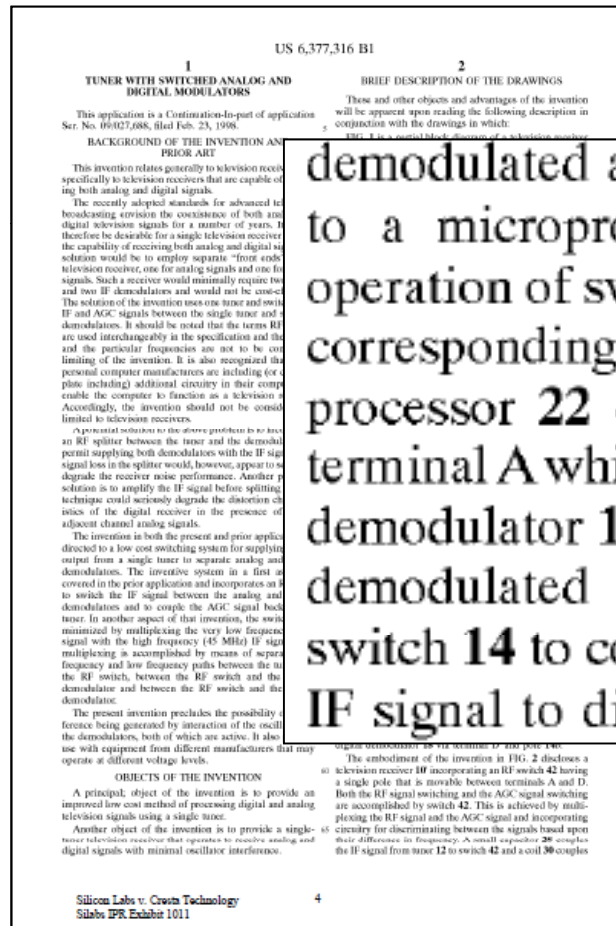
FIG. 2

baseband signals

Ex. 1011 at FIG. 2 (emphasis added)

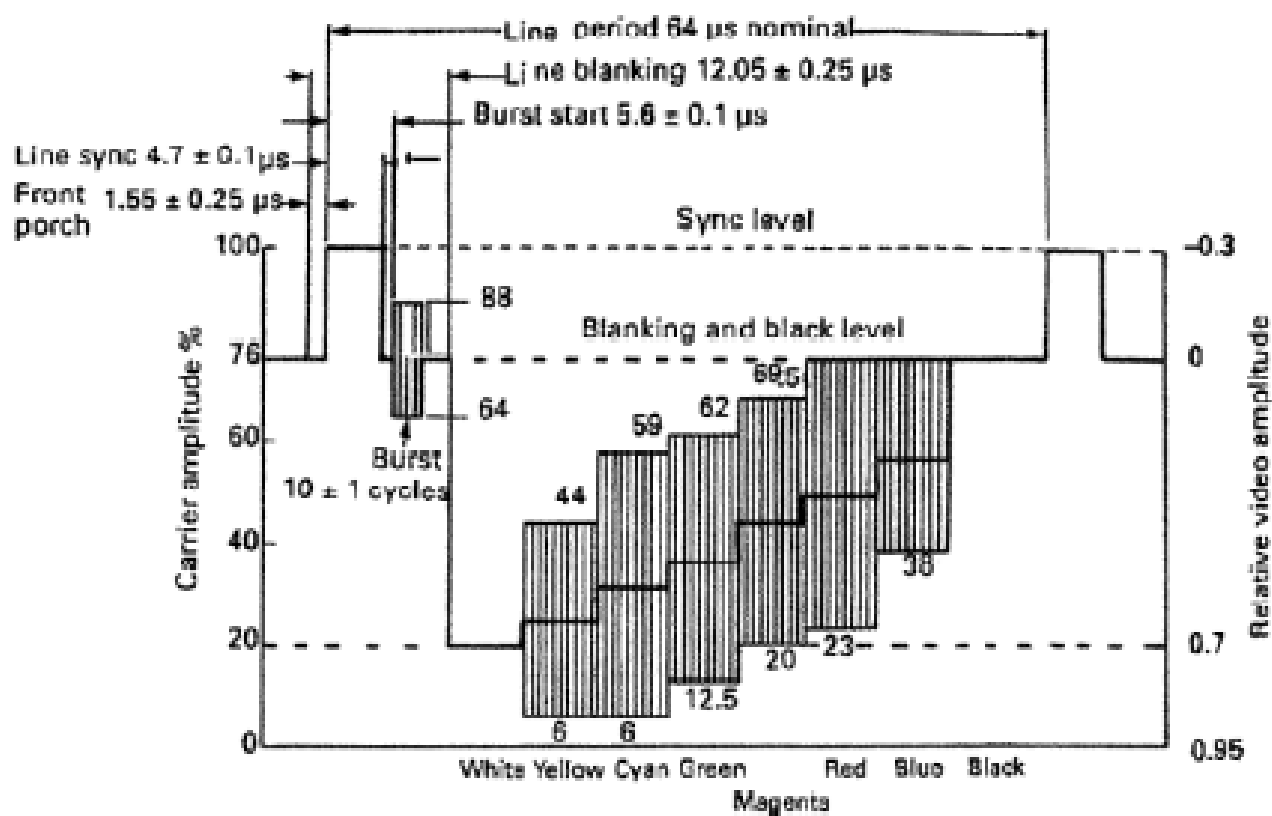
Silicon Laboratories, Inc.
Exhibit 1065 - 23

Zenith Detects "Carrier Signals"



demodulated analog signal. Sync separator **20** is connected to a microprocessor **22** that controls tuner **12** and the operation of switch **14**. Specifically, in the presence of syncs corresponding to a demodulated analog type signal, microprocessor **22** causes switch **14** to connect its pole **14a** to terminal A which routes the IF signal from tuner **12** to analog demodulator **16**. In the absence of syncs corresponding to a demodulated analog type signal, microprocessor causes switch **14** to connect its pole **14a** to terminal D to couple the IF signal to digital demodulator **18**.

Zenith Detects “Carrier Signals”



Zenith Detects "Carrier Signals"

US06369857B1

(12) **United States Patent**
Balaban et al.

(10) Patent No.: **US 6,369,857 B1**
(45) Date of Patent: **Apr. 9, 2002**

(54) **RECEIVER FOR ANALOG AND DIGITAL TELEVISION SIGNALS**

(75) Inventors: **Abba Reuben Balaban, Lehaan; Michael Leslie Low, Kenneth Paul; Edward Coley Fox, Conbury, all of NJ (US)**

(73) Assignee: **Sarnoff Corporation, Princeton, NJ (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.:
(22) Filed:
(51) Int. Cl.
(52) U.S. Cl.
(58) Field of Search:
(59) U.S.
5,203,053 A
5,557,337 A
5,572,264 A
5,902,857 A
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GB 23
WO 98
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Fox, Barry, "Digital
Report, IEEE Spec.
T. Nelson, Lyle L.
Date Handbook R-22, Partion: mar 1986, pp. 44-50.

34 Claims, 7 Drawing Sheets

Silicon Labs, Exhibit No. 1053
Silicon Laboratories v. Cresta Technology
IPR2015-00615

31. The method of claim **30** wherein the signal is a television signal and wherein the detecting a **carrier signal** includes detecting at least one of a picture carrier, a sound carrier signal, and a **synchronization signal**.

Zenith Detects “Carrier Signals”

(12) **United States Patent**
Favrat et al.

(10) **Patent No.:** US 7,075,585 B2
(45) **Date of Patent:** Jul. 11, 2006

(54) **BROADBAND RECEIVER HAVING A MULTISTANDARD CHANNEL FILTER**
(75) **Inventors:** Pierre Favrat, Sunnyvale, CA (US); Didier Margairaz, Santiago, CA (US); Alain-Serge Poret, Sunnyvale, CA (US); Dominique Pyhton, Sunnyvale, CA (US)
(73) **Assignee:** Xeive Corporation, Santa Clara, CA (US)
(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 392 days.

(21) **Appl. No.:** 10/236,645
(22) **Filed:** Sep. 6, 2002
(85) **Prior Publication Data**
US 2004/0061004 A1 Apr. 1, 2004

Related U.S. Application Data
(60) Provisional application No. 60/322,548, filed on Sep. 17, 2001.
(51) **Int. Cl.** H04N 3/27 (2006.01)
H04N 5/455 (2006.01)
(52) **U.S. CL.** 348/554; 348/726; 348/725; 375/340; 455/180.1
(58) **Field of Classification Search** 348/554; 348/555; 558; 725; 726; 375/316; 340; 343; 455/180.1; 245.2; 179.1; 188.1; 192.1; 334
See application file for complete search history.

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Primary Examiner
(74) Attorney, Agent
Carmen C. Cook
(57)

(56)

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2002/00510

Select Signal: Signal that is Indicative of the Format

ION E. OPRIS, PH.D. - 01/13/2016	
1	UNITED STATES PATENT AND TRADEMARK OFFICE
2	BEFORE THE PATENT TRIAL AND APPEALS BOARD
3	
4	SILICON LABORATORIES, INC.,)
5)
6	Petitioner,)
7) Case No.
8	VS.)
9	
10	CRESTA TECHNOLOGIES, INC.)
11)
12	
13	
14	
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17	DE
18	Q. And did you consider this patent in forming
19	your opinions that are reflected in Exhibit 2032?
20	MR. HABER: Objection. Form.
21	THE WITNESS: No.
22	
23	
24	Reported by: PHILIP D. NORRIS
25	CSR NO. 4980
DTI Court Reporting Solutions - Woodland Hills 1-800-826-0277 www.deposition.com	
Silicon Labs Exhibit No. 1060 Silicon Laboratories v. Cresta Technology IPR2015-00615	

Ex. 1060 at 60:18-21 (referring to "Patent No. 6,369,857").

Silicon Laboratories, Inc.
Exhibit 1065 - 28

Ground 1: Claims 11 and 12 are Obvious

Thomson (Ex. 1004)

+

Harris (Ex. 1005)

+

Grumman (Ex. 1008)

Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 696 854 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication: 14.02.1996 Bulletin 1996/07

(21) Application number: 95111940.3

(22) Date of filing: 29.07.1995

(84) Designated Contracting States: DE FR GB IT

(30) Priority: 08.08.1994 EP 94401828

(71) Applicant: THOMSON multimedia S.A. F-92400 Courbevoie (FR)

(72) Inventor: Bole, Werner F-67100 Strasbourg (FR)

(74) Representative: Hartnack, Wolfgang, Dipl.-Ing. D-30453 Hannover (DE)

(54) Broadcast receiver adapted for analog and digital signals

(57) Background:
Digital satellite TV broadcasting systems use an analog IF input followed by an analog QPSK-demodulator and analog baseband filters prior to A/D conversion. Normally, two A/D converters would be required for digital demodulation of the in phase and the quadrature component.

Advantages
Allows multi-standard front-end architecture, architecture is suited for digital and analogue input signals, the possible net data rate around 40Mbits/s is even higher than required for DVB-T.

Cost of the invention
A first IF frequency of about 2 GHz and a second IF of about 140 MHz allows to demodulate FM signals of 27 MHz bandwidth. A subsequent local 70 MHz local oscillator is followed by a lower resolution A/D converter operating at about 100 MHz sampling frequency in a subsampling mode. A single A/D converter (7) is required only and allows high quality FM demodulation.

Fig. 1: High level block diagram of a single channel receiver

Today, there widespread commercial systems depend on cost effective implementations of these receivers.

Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1004

A Digital Tuner for Wideband Receivers

Figure 1: High level block diagram of a single channel receiver

By Guy Olmstead and Mike Petrowski

Advances in both analog to digital conversion (ADC) and VLSI technologies have opened the door for the use of DSP techniques over an expanding range of high sample rate applications. Foremost among these is the use of standard off the shelf DSP IC's as digital replacements for the analog intermediate frequency (IF) processing stage in wideband receivers. Using this approach, the designer can take advantage of operational stability over time and temperature offered by digital technology, while realizing performance and flexibility unobtainable by older analog implementations.

In recent years there has been increasing interest in the topic of wideband receivers. These are receivers that can tune on a narrow band radio signal that exists in a broad spectrum of interest. The typical system in this application may be capable of extracting a signal as narrow as a few kHz out of a spectrum that spans tens, hundreds, or even thousands of MHz.

Because of the prohibitive cost of these receivers in the past, they were confined to use by the military, government agencies, and high end commercial users. Today, however, more widespread commercial communications systems are dependent on cost effective implementations of receivers. Cellular telephones, mobile radio, and wireless LANs are but a few examples of potential applications for DSP.

To better understand alternative wideband receiver designs using DSP, first consider the structure of the single channel wideband receiver as shown in Figure 1. As implied by the name, the single channel receiver is designed to receive and decode information within a single frequency band at a time. For the purposes of this discussion it will be assumed that one frequency band corresponds to one channel with no distinction between a frequency band and logical channels. When information is to be recovered from a different channel, the receiver must be tuned to the new

Silicon Labs v. Cresta Technology/Reprinted by permission of DSP Applications Magazine, Copyright 1992
Silabs IPR Exhibit 1005

United States Patent

US00531357A

(11) Patent Number: 5,381,357

(45) Date of Patent: Jan. 10, 1995

Wedge et al.

(54) COMPLEX ADAPTIVE FIR FILTER

(57) Inventors: Janet E. Wedge, Redwood, John F. Petrusic, New Hyde Park, both of N.Y.

(73) Assignee: Grumman Corporation, Redwood, N.Y.

(21) Appl. No.: 08,932

(22) Filed: May 28, 1993

(51) Int. Cl.⁷: G06F 15/31

(52) U.S. Cl.: 364/724.16; 364/724.19

(53) Field of Search: 364/724.16, 724.19, 364/724.13

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5,282,151 1/1994 Joon 364/724.19

Primary Examiner—David H. Malachuk
Attorney, Agent, or Firm—Scully, Scott, Murphy & Penseur

ABSTRACT

A complex adaptive Finite-Impulse-Response filter for processing complex digital data having real and imaginary data portions that includes a first data path for receiving and processing the real data portion of the complex input and a second data path for receiving and processing the imaginary data portion. Each first and second data path includes a corresponding plurality of adaptive weight circuits and accumulator circuits to perform respectively, multiplications of input data with a set of updatable coefficient data and accumulations of the multiplication results obtained. Two of multiplication results are obtained for each data path and a subset from each are accumulated to form a real output portion and imaginary output portion for the filter. A time delay circuit is provided to allow for proper time multiplexing of the imaginary output portion. The plurality of adaptive weight circuits have associated therewith first and second memory storage banks for storing the current coefficient data values. Alternate first and second memory storage banks are provided to receive updated coefficient data for use by the adaptive weight circuits at the request of the host processor. While the coefficient data stored in the first and second memory storage circuits are being used by the adaptive weight circuits for processing thereof, the coefficient data values may be updated in the first alternate and second alternate memory storage banks and vice versa.

13 Claims, 17 Drawing Sheets

Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1008

Ground 1: Claims 11 and 12 are Obvious

Trials@uspto.gov
571-272-7822

Paper 53
Entered: October 21, 2015

UNITED STATES PATENT AND
BEFORE THE PATENT TRIAL
SILICON LABORATORIES, INC.
Petitioner
v.
CRESTA TECHNOLOGIES, INC.
Patent Owner.

Case IPR2015-00728
Patent 7,075,585 B2

Before PHILLIP J. KAUFFMAN, GREY
PATRICK M. BOUCHER, Administrative Patent Judge
BOUCHER, Administrative Patent Judge

FINAL WRITING
35 U.S.C. § 318(a) and 37 C.F.R. § 42.103

10. The receiver of claim 1, wherein said signal processor applies one of a plurality of finite impulse response filters to said digital representation of said intermediate signal, each of said plurality of finite impulse response corresponding to a format of said input RF signal.

We conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, 5, 10, and 16 are unpatentable under 35 U.S.C. § 103(a) over Thomson and Harris.

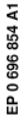
Silicon Labs Exhibit No. 1062
Silicon Laboratories v. Cresta Technology
IPR2015-00615

Ground 1: Claims 11 and 12 are Obvious

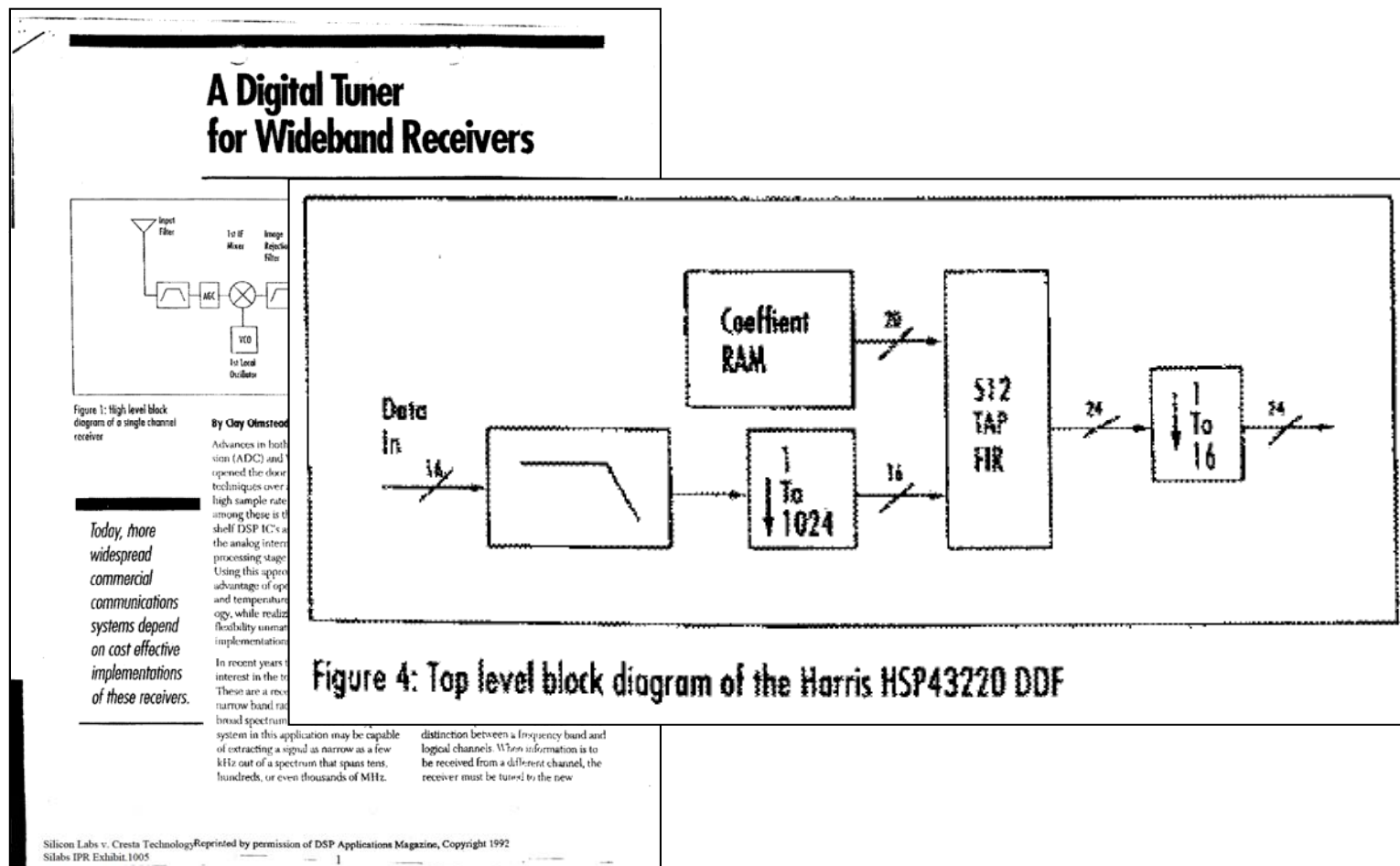
11. The receiver of claim 10, wherein said plurality of finite impulse response filters are stored in a memory, and said signal processor indexes said memory to retrieve one of said plurality of finite impulse response filters.

12. The receiver of claim 10, wherein said signal processor comprises a first computing unit and a second computing unit, said first computing unit processing a real part of said finite impulse response filter operation while said second computing unit processing an imaginary part of said finite impulse response filter operation.

Ground 1: Thomson's Digital Filter



Ground 1: Harris's Digital Filter



Ground 1: Harris's Digital Filter

A Digital Tuner for Wideband Receivers

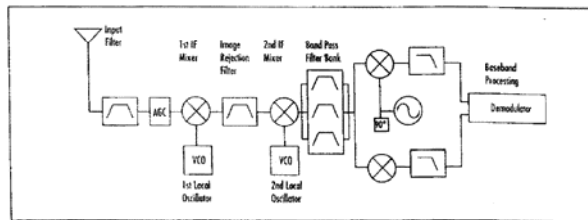


Figure 1: High level block diagram of a single channel receiver

By Clay Olmstead and Mike Petrowski

Today, more widespread commercial communications systems depend on cost effective implementations of these receivers.

Advances in both analog to digital conversion (ADC) and VLSI technologies have opened the door for the use of DSP techniques over an expanding range of high sample rate applications. Foremost among these is the use of standard off the shelf DSP IC's as digital replacements for the analog intermediate frequency (IF) processing stage in wideband receivers. Using this approach, the designer can take advantage of operational stability over time and temperature offered by digital technology, while realizing performance and flexibility unmatched by older analog implementations.

In recent years there has been increasing interest in the topic of wideband receivers. These are receivers that can tune on a narrow band radio signal that exists in a broad spectrum of interest. The typical system in this application may be capable of extracting a signal as narrow as a few kHz out of a spectrum that spans tens, hundreds, or even thousands of MHz.

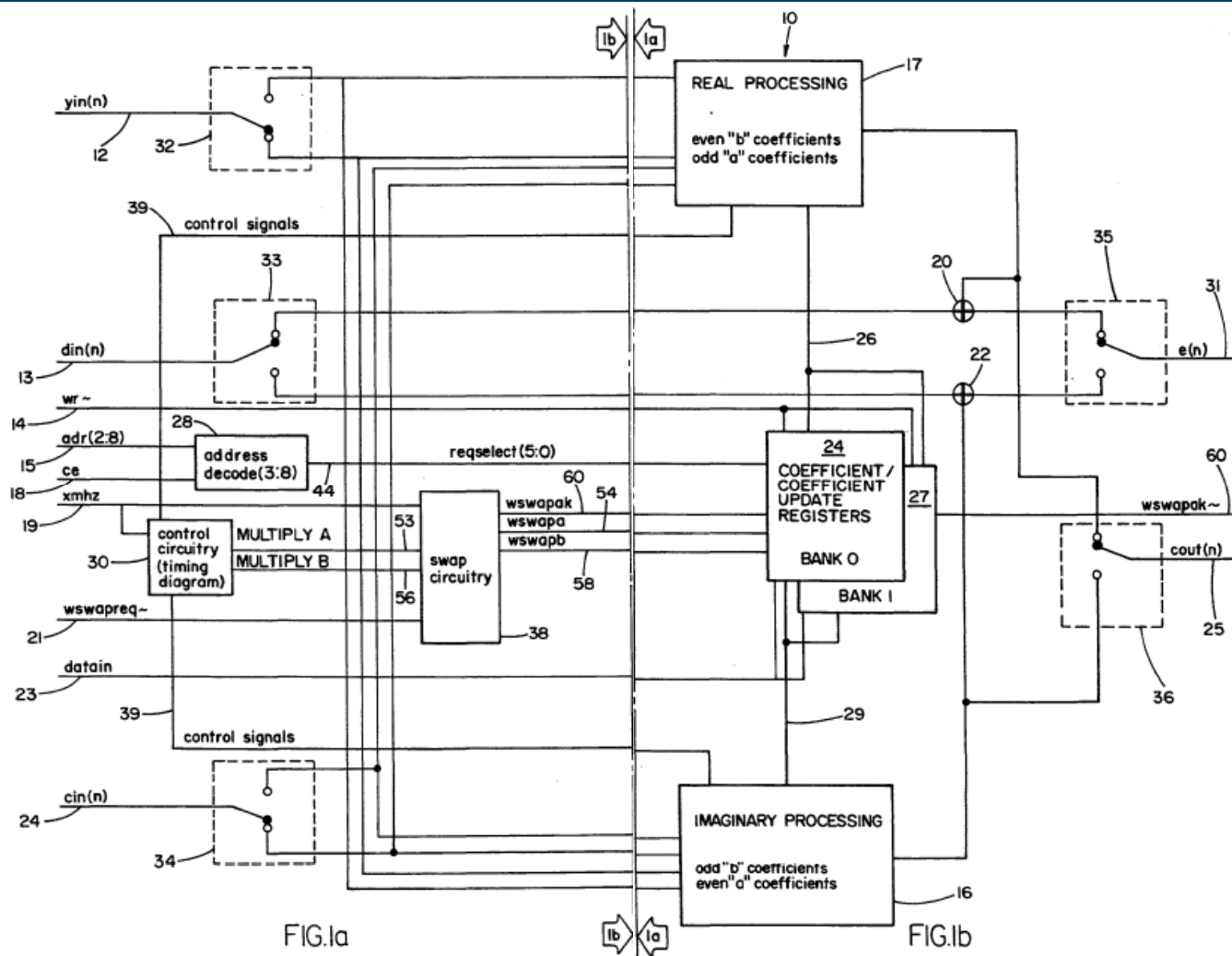
Because of the prohibitive cost of these receivers in the past, they were confined to use by the military, government agencies, and high end commercial users. Today, however, more widespread commercial communications systems are dependent on cost effective implementations of receivers. Cellular telephones, mobile radio, and wireless LANs are but a few examples of potential applications for DSP.

To better understand alternative wideband receiver designs using DSP, first consider the structure of the single channel wideband receiver as shown in Figure 1. As implied by the name, the single channel receiver is designed to receive and decode information within a single frequency band at a time. For the purposes of this discussion it will be assumed that one frequency band corresponds to one channel with no distinction between a frequency band and logical channels. When information is to be received from a different channel, the receiver must be tuned to the new

stopband attenuation of up to 120dB. As with the NCOM, the DDF can be rapidly reconfigured via a standard microprocessor interface.

PSK, etc. In addition to providing a platform which is capable of implementing any number of software based demodulation types, the digital receiver structure also offers flexibilities like programmable filtering, tuning, gain control, and activity detection to.

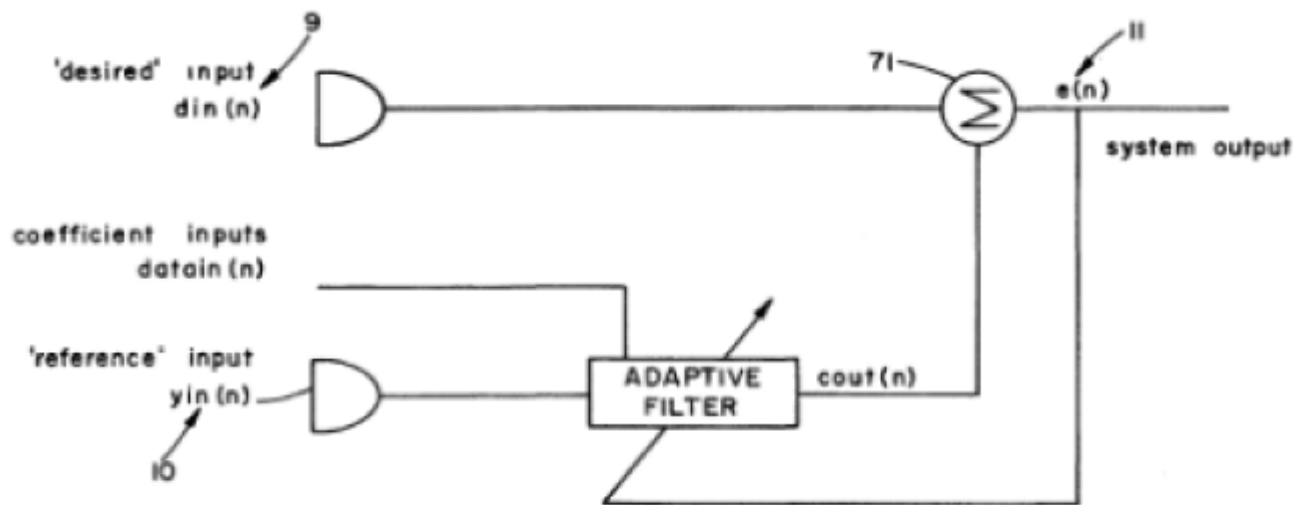
Ground 1: Grumman's Two Filters



Ex. 1008 at Fig. 1

Ground 1: Grumman's Two Filters

57. A “typical application” for Grumman’s adaptive filter is shown in Fig. 3, reproduced below:



Ground 1: Grumman's Two Filters

ION E. OPRIS, PH.D. - 01/13/2016

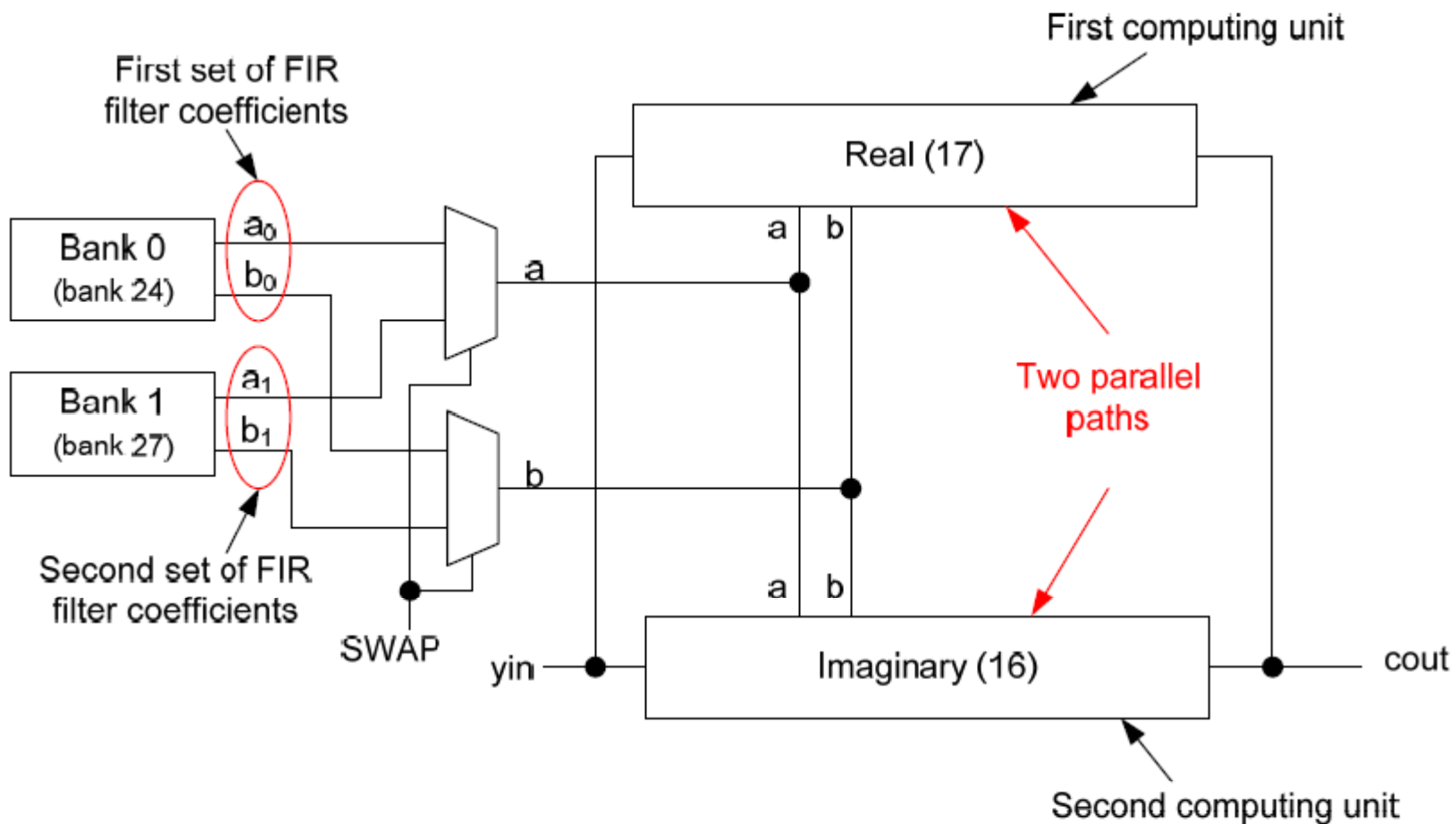
1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEALS BOARD
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4 SILICON LABORATORIES, INC. v. CRESTA TECHNOLOGIES, INC.
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8 VS.
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10 CRESTA TECHNOLOGIES, INC.
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24 Reported by: PHILIP D. NORRIS
25 CSR NO. 4980

2 Q. At some point in time potentially the filter --
3 the error signal's going to go to 0; correct?
4 A. Yes.
5 Q. At which point the filter coefficients would
6 remain constant; true?
7 A. Yes.

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Silicon Labs Exhibit No. 1060
Silicon Laboratories v. Cresta Technology
IPR2015-00615

Ground 1: Grumman's Two Filters



Ground 1: Grumman's Two Filters

11 5,381,357 12

all, maximum filter processing time is made available because, for e.g., while the accumulation of the results obtained from the multiplications of the input data with 'a' side coefficients presently loaded into Bank Φ are taking place, a new set of updated 'a' side coefficients in Bank 1 memory can be made accessible to the multipliers. This ensures that valid 'a' side coefficients are always made available so there is no interruption of the filtering process. Likewise, for the 'b' side coefficients although there is a one clock cycle delay.

With conventional prior art filters, it takes more than one clock cycle to write data into a memory bank of registers after that bank has supplied the coefficients for multiplication with the input during a previous clock cycle. Thus, in a filter having one coefficient memory bank, the new set of coefficient data could not be loaded into that memory bank during the accumulation cycle which normally lasts for one clock cycle (see FIGS. 4a and 4b). Hence, after the accumulate cycle is complete, there would be a filter processing time delay existing for the amount of time it takes to finish loading new coefficient data into the memory bank. During this time delay, no multiplication could take place and filter performance is degraded.

With applicant's two Bank architecture, while the filter is operating with data present in the first coefficient memory bank, the alternative memory bank, i.e., the one not being used by the filter, is being updated with the new set of coefficients. This ensures that under the control of the weight swap circuitry, after the accumulation has taken place, multiplication with new coefficients loaded into the alternative bank can immediately take place with no time lapse. Hence, with no filter processing time delay, the complex data output rate of the filter is equal to the complex data input rate. As noted above, it should be appreciated that coefficient data will be initially loaded into the first coefficient memory bank (e.g., Bank Φ). Subsequent updated coefficient data is successively loaded into the alternative memory bank, i.e., the one not being used by the multipliers, after each weight swap request under the automatic control of the weight swap circuitry.

The writing of coefficient data to the memory banks during the weight swapping process will now be explained with respect to FIG. 8. FIG. 8 shows how the 'a' side coefficients are swapped between coefficient registers in Bank Φ and Bank 1. It is understood that when the coefficient registers containing 'a' side coefficients in Bank Φ are being accessed by the filter 10, the coefficient registers containing 'a' side coefficients in Bank 1 may be accessed by the host computer for writing updated 'a' coefficient data thereto and vice versa. 'b' side coefficients are swapped similarly, i.e., the 'b' side coefficients registers in Bank Φ are either being accessed by the filter 10 or host computer at any one time.

In operation, the individual 'a' side coefficient registers are accessed to receive data that is present on the DATAIN bus 23. As shown in FIG. 8, WSWAPA signal 54, together with W_r- signal 14, determine which coefficient/coefficient update memory bank is being accessed by the filter 10 (e.g., Bank Φ), and which memory bank is to receive the updated coefficients (e.g., Bank 1). The REGSELECT(5- Φ), signal 44, selects which individual coefficient register in the selected memory bank, i.e., registers C₀ through C₅, is to receive the data present on DATAIN. As mentioned previously, DATAIN contains floating point coefficients, up to 32 bits, for enhanced mathematical precision. An identical operation is performed when coefficients are being updated to the alternate coefficient/coefficient update memory Bank Φ while the coefficients present in Bank 1 are being accessed by the filter 10. Again, WSWAPA, signal 54, together with W_r- signal 14, determine that the coefficient registers in Bank Φ are to receive updated coefficient data. The REG-

With applicant's two Bank architecture, while the filter is operating with data present in the first coefficient memory bank, the alternative memory bank, i.e., the one not being used by the filter, is being updated with the new set of coefficients. This ensures that under the control of the weight swap circuitry, after the accumulation has taken place, multiplication with new coefficients loaded into the alternative bank can immediately take place with no time lapse. Hence, with no filter processing time delay, the complex data output rate of the filter is equal to the complex data input rate. As

where w vector is processed in parallel with the input vector x, the output y is given by:

$$y(n) = \sum_{k=0}^{N-1} x(n-k)w(k)$$

The weight vector, w(k), is given by:

$$w(k) = w_r(k) + jw_i(k)$$

Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1008

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Ground 1: Grumman's Two Filters

Trials@uspto.gov
571-272-7822

Paper 9
Entered: October 24, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CRE

“Accordingly, we construe ‘signal processor’ as a digital module that processes signals in the digital domain.”

Before PHILLIP J. KAUFFMAN, GREGG I. ANDERSON, and
PATRICK M. BOUCHER, *Administrative Patent Judges*.

BOUCHER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

On May 5, 2014, Silicon Laboratories, Inc. (“Petitioner”) filed a
Petition (Paper 1, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an
inter partes review of claims 1–3, 5, 10, 13, 14, and 16–19 of US Patent No.

Ground 3: Claim 14 is Obvious over Birleson

13. The receiver of claim **10**, wherein said channel filter further comprises a standard selection circuit coupled to said signal processor, said standard selection circuit generating a select signal indicative of a format of said input RF signal and said signal processor selecting a finite impulse response filter in response to said select signal.

14. The receiver of claim **13**, wherein said standard selection circuit generates said select signal in response to an input signal from a user.

Ground 3: Claim 14 is Obvious over Birleson

US 6,725,463 B1

(12) **United States Patent**
Birleson

(10) Patent No.: **US 6,725,463 B1**
(45) Date of Patent: **Apr. 20, 2004**

(54) **DUAL MODE TUNER FOR CO-EXISTING DIGITAL AND ANALOG TELEVISION SIGNALS**

(75) Inventor: **Vince Birleson**, West Tawakoni, TX (US)

(73) Assignee: **Microtune (Texas), L.P.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No. **08/984,693**
(22) Filed: **Aug. 1, 1997**

(51) Int. Cl. **H04N 7/173**
(52) U.S. Cl. **725/151; 348/731; 348/555; 348/558; 455/143; 455/259; 455/260; 455/265; 351/22; 351/52**

(58) Field of Search: **348/731, 554; 348/726, 10, 441, 558, 555, 553, 584; 455/2, 6, 2, 137, 180, 1, 74, 143, 22, 550, 553, 307, 313, 314; 375/270, 321, 216, 351/22-32; 725/37, 151-153, 131-142, 345/731, 732; H04N 5/30, 7/10**

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(List continued on next page.)

Primary Examiner—Andrew Felle
Assistant Examiner—Rashen Brown
(74) Attorney, Agent, or Firm—Fulbright & Jaworski L.L.P.

ABSTRACT
(57) A dual mode tuner/receiver is disclosed in which both analog and digital signals can be received and processed. A low pass filter allows all channels below a selected frequency enter the circuit. A precisely controlled dual conversion circuit creates an intermediate frequency (IF) signal. An automatic carrier detection circuit monitors the IF signal and determines whether the signal is of analog or digital format and intermediate frequency filters are adjusted based upon the type of signal detected. A coherent oscillator circuit generates in-phase and quadrature reference signals that are used by video and audio detectors for further processing of the IF signal. In-phase and quadrature outputs are provided for digital signals and composite video and audio outputs are provided for analog signals.

89 Claims, 7 Drawing Sheets

Silicon Labs v. Crown Technology
Silicon EPR Exhibit 1015

1

Ex. 1015 at FIG. 1

Ground 3: Claim 14 is Obvious over Birleson

(12) **United States Patent**
Birleson

(10) Patent No.: **US 6,725,463 B1**
(45) Date of Patent: **Apr. 20, 2004**

(54) **DUAL MODE TUNER FOR CO-E
DIGITAL AND ANALOG TELEVI
SIGNALS**

(75) Inventor: **Vince Birleson, West Tex
(US)**

(73) Assignee: **Microtune (Texas), L.P.,
(US)**

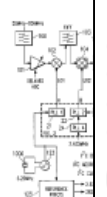
(*) Notice: Subject to any disclaimer,
patent is extended or adj
U.S.C. 154(b) by 0 days.

(21) Appl. No: **08/904,093**
(22) Filed: **Aug. 1, 1997**

(51) Int. Cl.:
(52) U.S. Cl.: **725/151; 348
348/558; 455/143; 455/259; 455**

(58) **Field of Search**
348/726, 10, 441, 558, 555, 553
6.2, 137, 180.1, 74, 143
307, 313, 314; 375/270, 321, 2
725/37, 151-153, 131-142,
10

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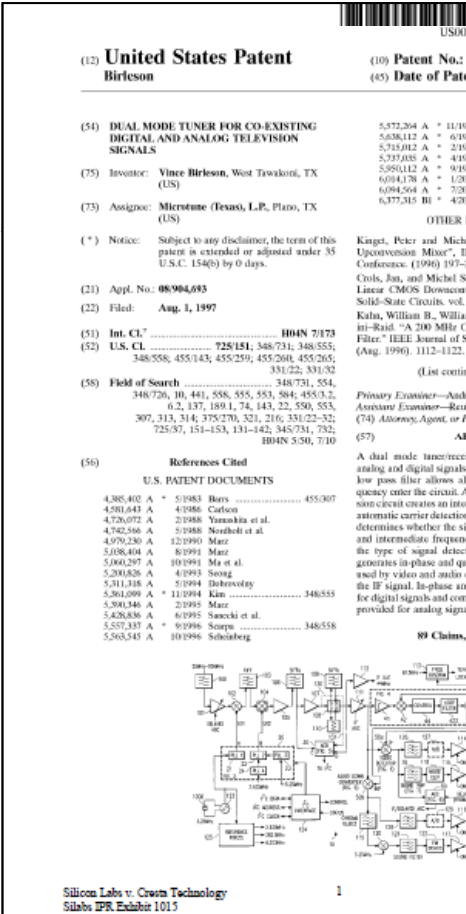


SIFFb 109 is designed to work in conjunction with **SIFFa 106** to provide the band pass characteristics that are necessary for analog television signal processing. A typical analog signal pass band is illustrated in FIG. 8. In the preferred method of operation, switch **108** selects **SIFFb 109** into the signal path when an analog television signal is detected. As a result, the combined pass band through **SIFFa 106** and **SIFFb 109** will be similar to that shown in FIG. 8 and will be optimized for processing the analog signal. If a digital television signal is detected, switch **108** selects attenuator **110** into the signal path. The resulting band pass of **SIFFa 106** and attenuator **110** will be similar to FIG. 9 and will be optimized for digital television signal processing.

Silicon Labs v. Crown Technology
Silabs EPR Exhibit 1015

1

Ground 3: Claim 14 is Obvious over Birleson



Signal testing may be initiated by a channel change. In that case, every time a new channel is selected, both SIFFa **106** and SIFFb **109** are switched into the circuit and ACD **30** compares signal levels on lines C and D. Following the test, I²C **124** either switches SIFFb **109** out or leaves it in the signal path depending on whether an analog or digital signal is detected.

I²C 124 can initiate signal testing in ACD 30 depending on any number of other factors. Signal testing could be initiated by a channel change, as discussed above, or by a change in the input source. For instance, if an operator switched the input from an antenna or cable line to a videotape recorder or laser disk player, then the test could be initiated even though the operator did not change the channel. ACD testing may be automatic or user-initiated. For example, a television system may provide a function on a remote control which allows the user to select the "test mode."

SILICON LABORATORIES, INC.
Petitioner

v.

CRESTA TECHNOLOGY CORPORATION
Patent Owner

IPR2015-00626
Patent No. 7,265,792

Trial Hearing: June 1, 2016
Petitioner's Demonstrative Exhibits



Silicon Laboratories, Inc.
Exhibit 1065-45

U.S. Pat. No. 7,265,792: Digital Receiver for Digital and Analog Television Signals

US007265792B2

(12) United States Patent
Fayrat et al.

(10) Patent No.: US 7,265,792 B2
(45) Date of Patent: Sep. 4, 2007

(54) TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS

(75) Inventors: **Pierre Fayrat**, Milpitas, CA (US);
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(73) Assignor: **Xcelve Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 483 days.

(21) Appl. No.: 10/884,347

(22) Filed: Jul. 1, 2004

(65) Prior Publication Data

US 2006/0001779 A1 Jan. 5, 2006

(51) Int. Cl. H04N 3/27 (2006.01)

H04N 5/46 (2006.01)

(52) U.S. Cl. 348/554; 348/558

(58) Field of Classification Search: 348/554, 348/558, 725, 726, 705, 706, 375/316, 340, 455/109.1, 245.2, 170.1, 188.1, 192.1, 534
See application file for complete search history.

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Primary Examiner—Victor R. Kostak

(74) Attorney, Agent, or Firm—Patent Law Group LLP, Carmen C Cook

(57)

ABSTRACT

A television receiver includes a frequency conversion circuit, an analog-to-digital converter, a signal processor, and a signal output circuit. The frequency conversion circuit receives an input RF signal in one of several television signal formats and converts the input RF signal to an intermediate frequency signal. The analog-to-digital converter samples the intermediate frequency signal and generates a digital representation thereof. The signal processor processes the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal and generates digital output signals indicative of information encoded in the input RF signal. Finally, the signal output circuit receives the digital output signals from the signal processor and provides one or more output signals corresponding to the digital output signals. The signal output circuit can be configured to provide output signals corresponding to an analog television format or a digital television format or both.

29 Claims, 3 Drawing Sheets

TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS

Inventors: **Pierre Favrat**, Milpitas, CA (US); **Alain-Serge Porret**, Sunnyvale, CA (US); **Dominique Python**, Sunnyvale, CA (US); **Friederich Mombers**, San Jose, CA (US); **Richard P. Perring**, San Jose, CA (US); **Philippe Duc**, Santa Clara, CA (US); **Benito Carnero**, Santa Clara, CA (US); **Didier Margairaz**, San Jose, CA (US)

Assignee: **Xceive Corporation**, Santa Clara, CA
(US)

Appl. No.: 10/884,347

Filed: **Jul. 1, 2004**

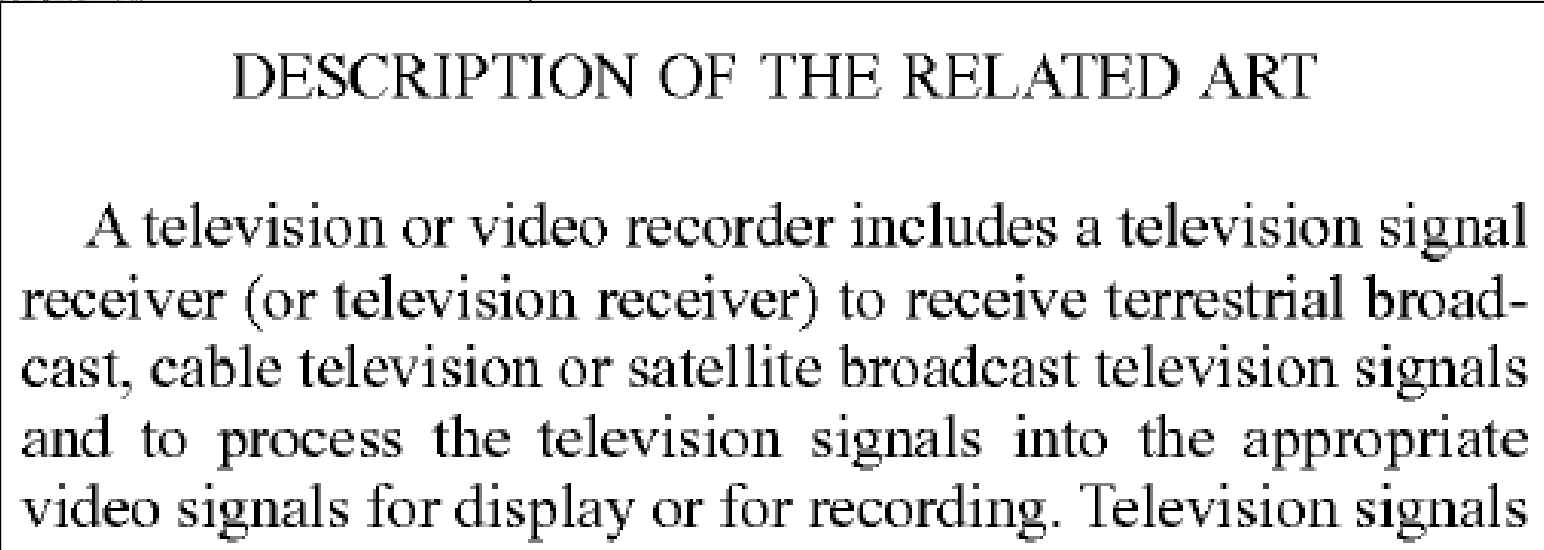
IPR2015-00626: Common Grounds with -00615

Trials@uspto.gov Tel: 571-272-7822	Paper 9 Entered: August 14, 2015
UNITED STATES PATENT BEFORE THE PATENT TRIAL SILICON LABORATORIES, INC. Petitioner	ORDERED that <i>inter partes</i> review is <i>instituted</i> with respect to the following grounds of unpatentability:
v. CRESTA TECHNOLOGY CORPORATION Patent	(2) claims 24 and 25 as unpatentable under 35 U.S.C. § 103(a) over Thomson, Harris, and Grumman;
Case IPR2 Patent 7,2	(3) claims 26 and 28 as unpatentable under 35 U.S.C. § 103(a) over Thomson, Harris, and Zenith;
Before PHILLIP J. KAUFFMAN, GR PATRICK M. BOUCHER, Administrative Patent Judges	(4) claim 27 as unpatentable under 35 U.S.C. § 103(a) over Thomson, Harris, Zenith, and Birleson; and
KAUFFMAN, Administrative Patent Judge DEC Instituting Inter Partes Review 37 C.F.R. § 42.101	


Ground 1: Claim 29 is Obvious

29. The television receiver of claim **1**, wherein the input RF signal comprises an RF signal received from terrestrial broadcast, an RF signal received from satellite broadcast, and an RF signal received from cable transmission.

Ground 1: Claim 29 is Obvious



Ground 1: Claim 29 is Obvious



US007265792B2

(12) **United States Patent**
Favrat et al.

(10) **Patent No.:** US 7,265,792 B2
(45) **Date of Patent:** Sep. 4, 2007

(54) **TELEVISION RECEIVER FOR DIGITAL AND ANALOG TELEVISION SIGNALS**

(75) **Inventors:** Pierre Favrat, Milpitas, CA (US); Alain-Serge Porret, Sunnyvale, CA (US); Dominique Pythen, Sunnyvale, CA (US); Friederich Muehlers, San Jose, CA (US); Richard B. Sazdovitch, Santa Clara, CA (US); Margarita, San Jose, CA (US)

(73) **Assignee:** Nexio Corporation (US)

(*) **Notice:** Subject to any disclaimer, this patent is extended under 35 U.S.C. 154(b) by 0 months.

(21) **Appl. No.:** 10/884,347

(22) **Filed:** Jul. 1, 2004

(65) **Prior Publication:** US 2006/0001779 A1

(51) **Int. Cl.:** H04N 5/27 (2006.01); H04N 5/06 (2006.01)

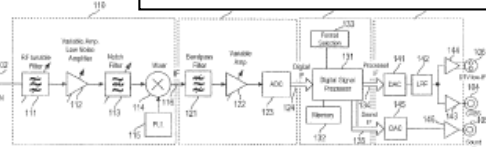
(52) **U.S. Cl.:** 348/558, 725, 726, 709, 455/180.1, 245.2, 17

(58) **Field of Classification Search:** See application file for complete list of references.

(56) **References Cited:** U.S. PATENT DOCUMENTS 4,872,854 A * 10/1989 Gray et al.

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Silicon Labs v. Crown Technology
Silabs IPR Exhibit 1001
Page 1

Referring to FIG. 1, receiver 100 includes a frequency conversion circuit 110 (or tuner circuit 110), a digitizing IF circuit 120, a digital signal processor (DSP) circuit 130 and a signal output circuit 140. Frequency conversion circuit 110 receives input RF signals on signal input terminal 102. The input RF signals can be received from terrestrial broadcast or cable transmissions. Frequency conversion circuit 110

Ground 1: Claim 29 is Obvious

ION E. OPRIS, PH.D. - 01/13/2016	
1	UNITED STATES PATENT AND TRADEMARK
2	BEFORE THE PATENT TRIAL AND APPEAL
3	
4	SILICON LABORATORIES, INC.,)
5)
6	Petitioner,)
7) Case No.
8	vs.) IPR2015-00
9) IPR2015-00
10	CRESTA TECHNOLOGY CORPORATION,) Pages 1 to
11)
12	Patent Owner.)
13)
14	
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17	DEPOSITION OF ION E. OPRIS, PH.D.
18	TAKEN ON
19	WEDNESDAY, JANUARY 13, 2016
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24	Reported by: PHILIP D. NORRIS
25	CSR NO. 4980

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Silicon Labs Exhibit No. 1060
Silicon Laboratories v. Cresta Technology
IPR2015-00615

7 Q. Okay. And where is that described in the '792
8 patent?
9 A. What is "that"?
10 Q. The differences in that frequency conversion
11 circuit to accommodate these three different frequency
12 bands.
13 MR. HABER: Objection. Form.
14 THE WITNESS: I think that was known in the art
15 at that time of the invention.
16 BY MR. AYERS:
17 Q. And that's why it's not specifically described
18 in the '792 patent?
19 A. Yes.

Ground 1: Claim 29 is Obvious

UNITED STATES PATENT AND TRADEMARK OFFICE	
BEFORE	<i>Thomson's Receiver Can Process the IF_{SAT} Signal Transmitted from All Three Sources</i>
Title: Tele	
SUPPLEMENT IN SUPPORT	<p>13. All that claim 29 requires is that the receiver be able to process “the input signal” of claim 1 where that signal includes “an RF signal” that originates from three different sources—satellite, cable, and terrestrial. Patent Owner admits that Thomson’s receiver is capable of receiving “an RF signal” from a satellite source. Thomson is also capable of receiving that same signal (“IFSAT”) if it had been transmitted via cable or over an antenna. Thomson’s receiver does not care</p>
Silicon Labs, Exhibit No. 1063 Silicon Laboratories v. Cresta Technology IPR2015-00626	

Ground 1: Claim 29 is Obvious

ION E. OPRIS, PH.D. - 01/13/2016

UNITED STATES PATENT AND TRADEMARK OFFICE

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24 Rep

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4 Q. So you'd agree with me that it was well known

5 in the art at the time of the '792 patent for a

6 television receiver to receive an RF signal from

7 terrestrial, cable or satellite broadcast television?

8 MR. HABER: Objection. Form.

9 THE WITNESS: That was known in the art.

10 MR. AYERS: Okay.

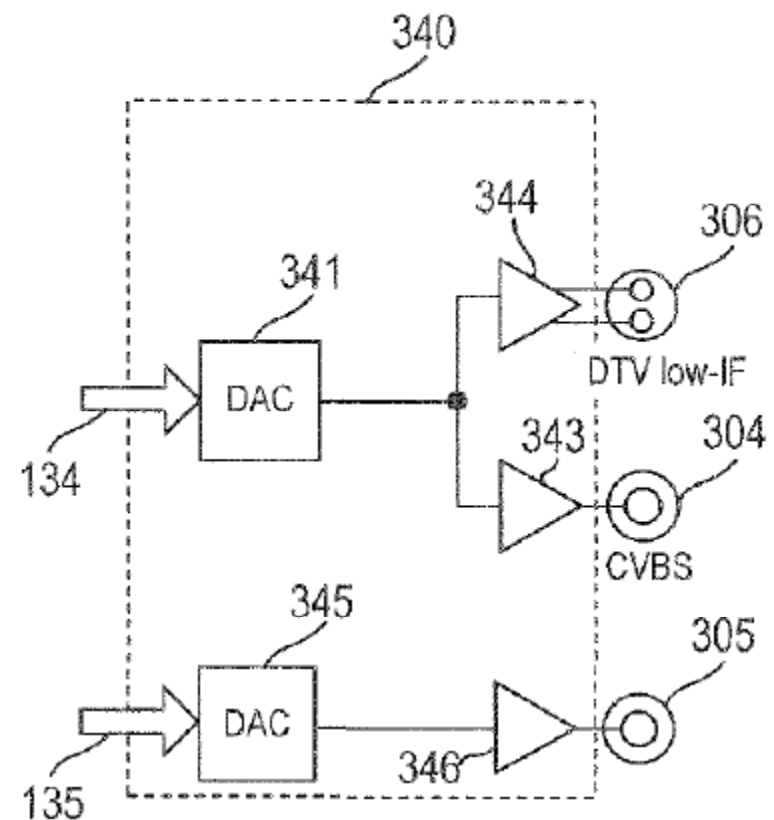
DTI Court Reporting Solutions - Woodland Hills
1-800-826-0277 www.deposition.com

Silicon Labs Exhibit No. 1060
Silicon Laboratories v. Cresta Technology
IPR2015-00615

Ground 5: Claim 18 is Obvious

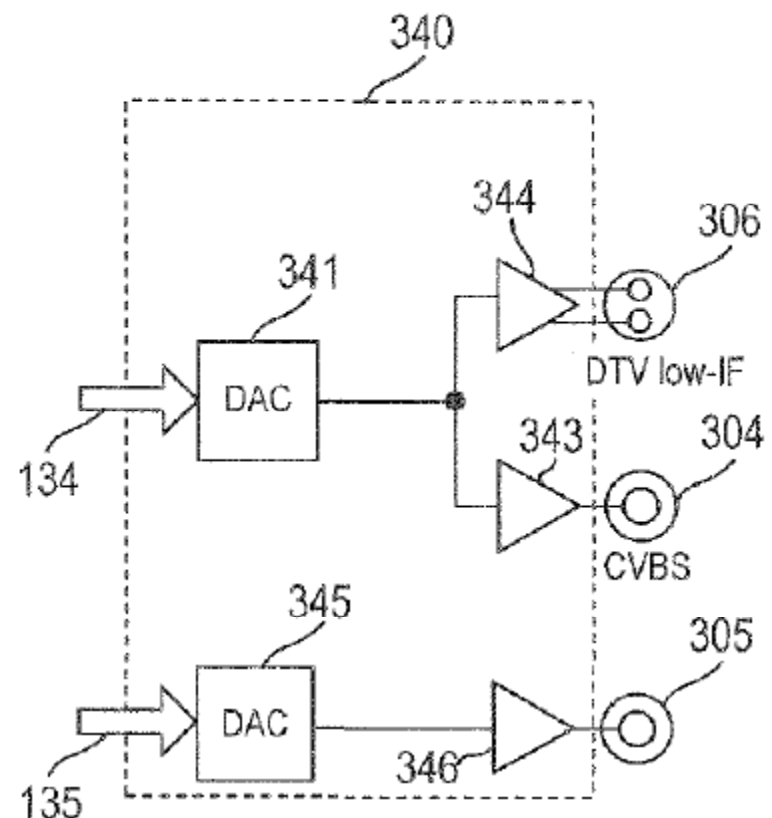
18. The television receiver of claim 1, wherein the signal output circuit comprises:

- a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals;
- a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal;
- a second driver circuit for driving the analog output signals from the first digital-to-analog converter, the second driver circuit comprising a differential output driver circuit having a first differential output terminal and a second differential output terminal, the first differential output terminal being coupled to the first output terminal and the second differential output terminal being coupled to a second output terminal;
- a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and
- a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto the second output terminal,

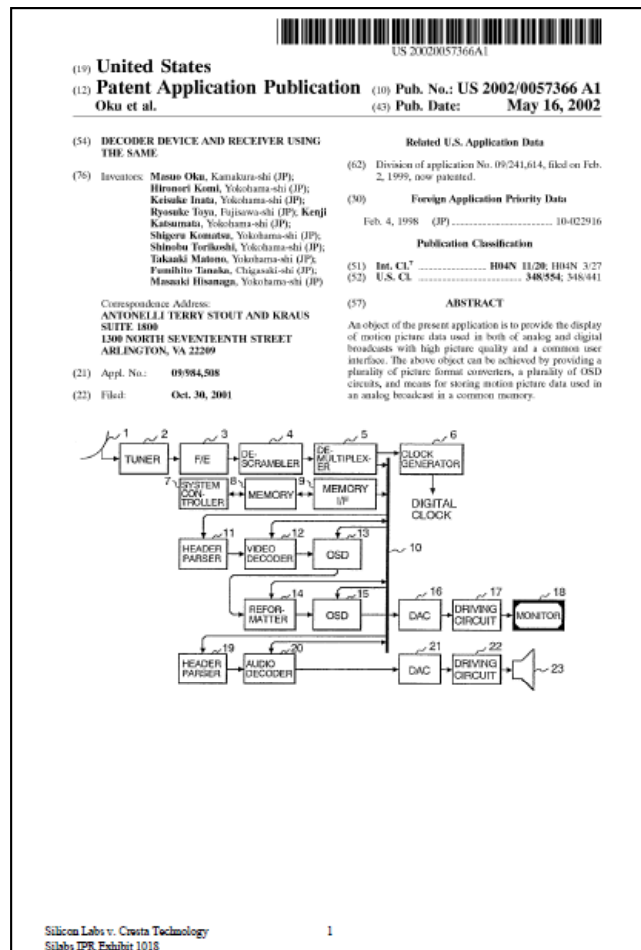


Ground 5: Claim 18 is Obvious

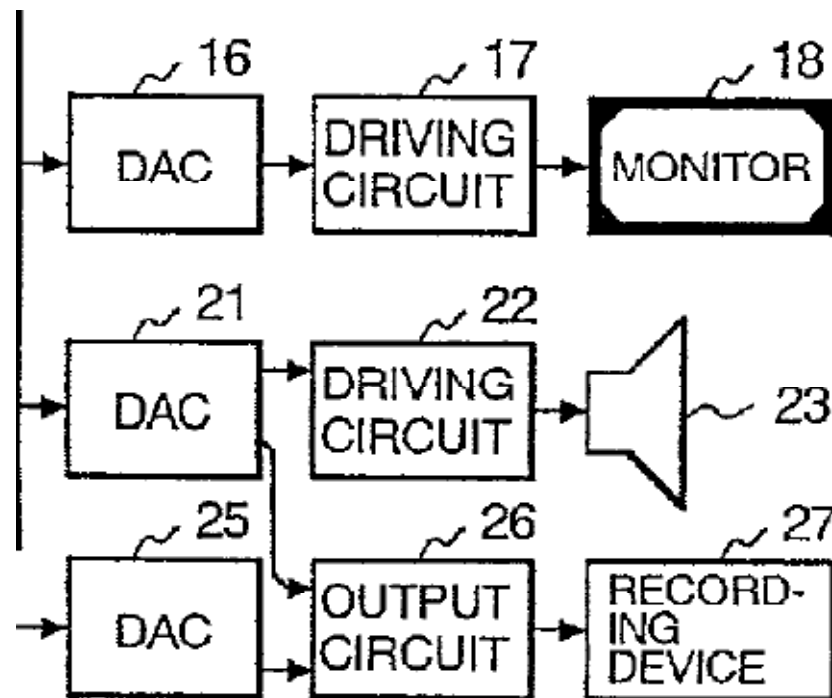
wherein the first and second output terminals provide differential output signals indicative of video and audio information encoded in the input RF signal when the input RF signal has a digital television signal format; and the first output terminal provides video information encoded in the input RF signal and the second output terminal provides signals indicative of audio information encoded in the input RF signal when the input RF signal has an analog television signal format.



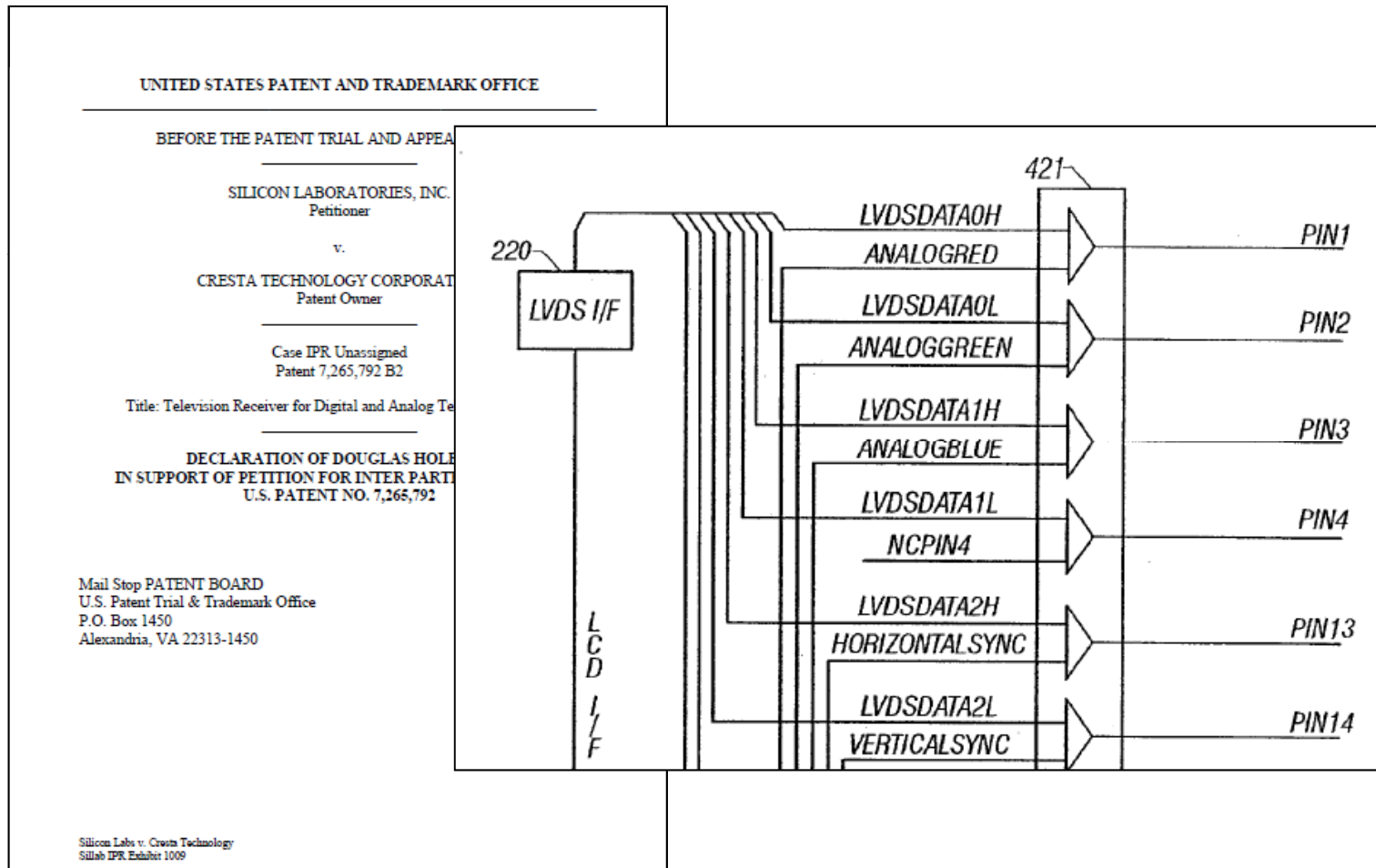
Claim 18: Multiplexing and Differential Signaling is Obvious



Ex 1018 at FIG. 4




Claim 18: Multiplexing and Differential Signaling is Obvious



Ex. 1009 at 11 (citing Ex 1020 (Fig. 4))

Silicon Laboratories, Inc.
Exhibit 1065 - 57

Claim 18: Multiplexing and Differential Signaling is Obvious



US006411136B1

(12) **United States Patent**
Nianxiang et al.

(10) **Patent No.:** **US 6,411,136 B1**
(45) **Date of Patent:** **Jun. 25, 2002**

(54) **DIFFERENTIAL LINE DRIVER**

(75) **Inventors:** **Tan Nianxiang, Sollenbom, Johan Erlund, Linköping, Jacob Wikner, Linköping, all of (SE)**

(73) **Assignee:** **Telefonaktiebolaget LM Ericsson (publ), Stockholm (SE)**

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/259,342**
(22) **Filed:** **Mar. 1, 1999**

(30) **Foreign Application Priority Data**
Mar. 2, 1998 (SE) 9800035

(51) **Int. Cl.:** **H03B 1/00; H05K 3/00**
(52) **U.S. Cl.:** **327/108; 327/110; 326/50; 326/83**

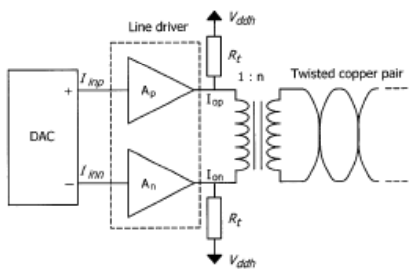
(58) **Field of Search** 327/108-112, 560, 327/563, 52, 65, 74, 75; 326/30, 82, 83, 330/253

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ABSTRACT
(57)
A fully differential line driver, especially for twisted copper pairs. It includes two current amplifiers made in standard CMOS technique, each having an input and an output, the latter being connected via terminal resistors to a voltage source, which may be set to a larger voltage than that used for driving the CMOS amplifiers. Accordingly, a low output impedance can be combined with a large swing. Further, feedback is not necessary, avoiding problems like potential instability. A very low-impedance input makes it appropriate for connecting to a DAC, thus reducing distortion of its output signal. The driver is suitable for very-high-speed-digital-subscriber-line modems.

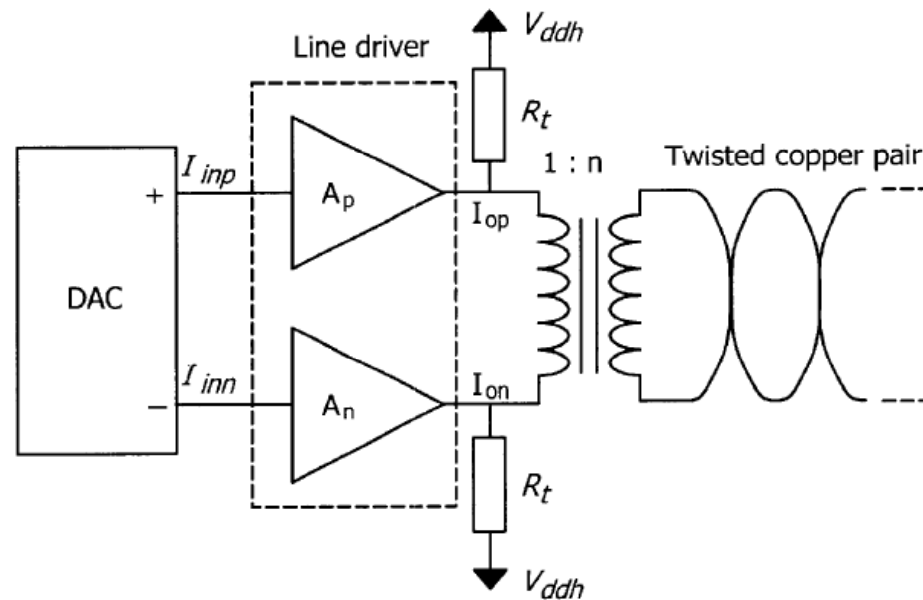
7 Claims, 2 Drawing Sheets



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Silicon Labs v. Cresta Technology
Silabs IPR Exhibit 1024

Ex. 1024 (Ericsson) at FIG. 2



Claim 18: Multiplexing and Differential Signaling is Obvious

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON LABORATORIES, INC.
Petitioner

v.

CRESTA TECHNOLOGY CORPORATION
Patent Owner

Case IPR Unassigned
Patent 7,265,792 B2

Title: Television Receiver for Digital and Analog TV

DECLARATION OF DOUGLAS HOLMES
IN SUPPORT OF PETITION FOR INTER PART
U.S. PATENT NO. 7,265,792

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U.S. Patent Trial & Trademark Office
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Silicon Labs v. Cresta Technology
Silicon Labs IPR Exhibit 1009

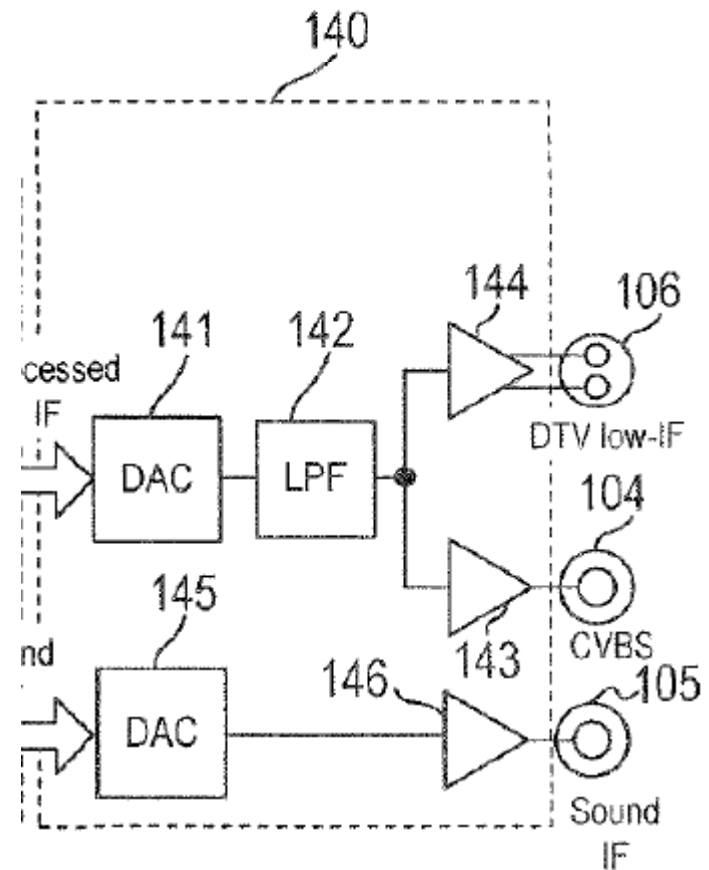
The diagram illustrates a television receiver circuit (400). It consists of three main functional blocks: a Digital Down-Converter Circuitry (427), a Digital Filter Circuitry (426), and a DAC Circuitry (445). The Digital Down-Converter Circuitry (427) receives differential inputs labeled 421 (diff.) and 422. It outputs two signals, I (430) and Q (433), to the Digital Filter Circuitry (426). The Digital Filter Circuitry (426) outputs two signals, I (439) and Q (442), to the DAC Circuitry (445). The DAC Circuitry (445) produces two differential output signals, RX-I (diff.) (448) and RX-Q (diff.) (451). A reference signal 120 is also shown entering the DAC Circuitry (445). A switch (436) is connected to the Q outputs (433 and 442) of the Digital Filter Circuitry (426) and the DAC Circuitry (445).

Ex. 1009 at 11-12 (citing Ex 1021)

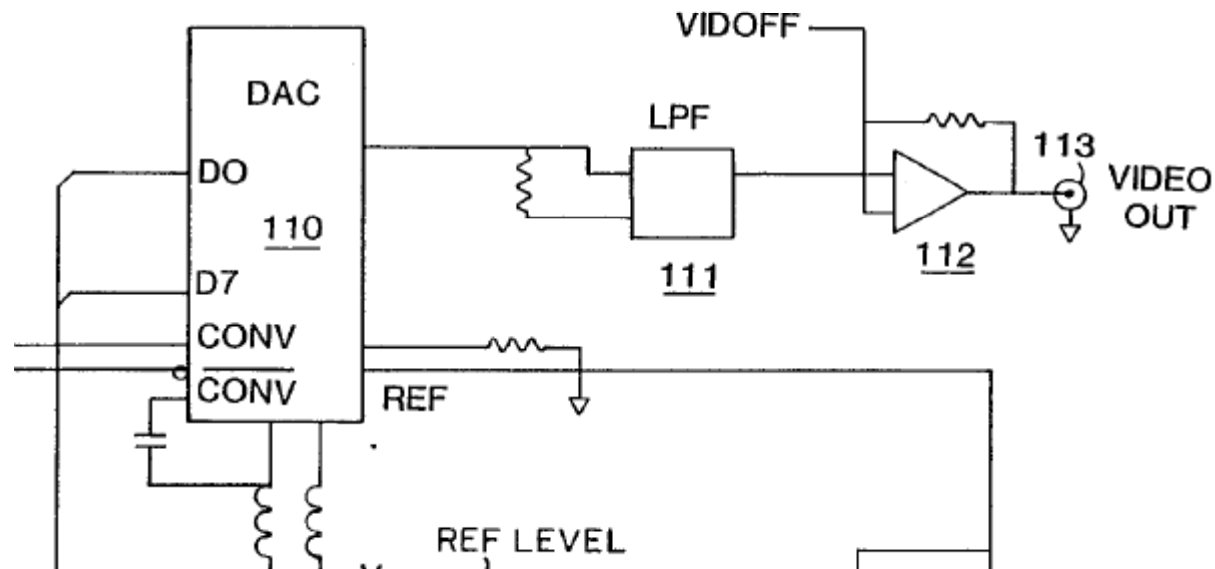
Silicon Laboratories, Inc.
Exhibit 1065 - 59

Claim 19: Low Pass Filtering DAC Output is Obvious

19. The television receiver of claim 18, wherein the signal output circuit further comprises:
a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.



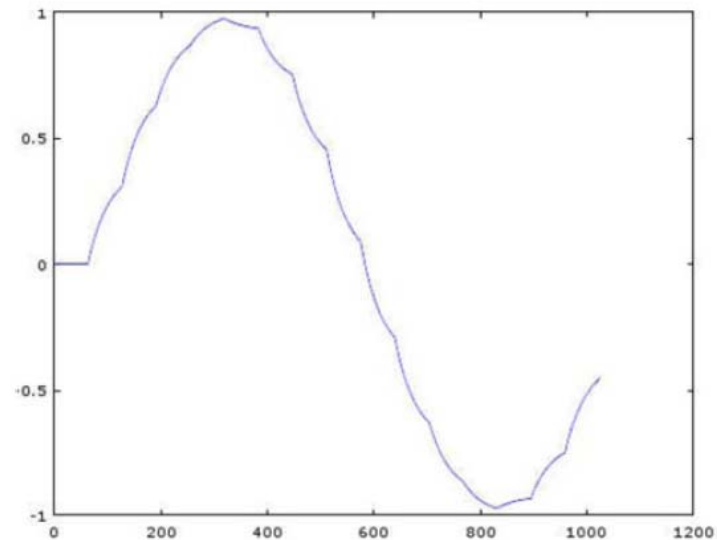
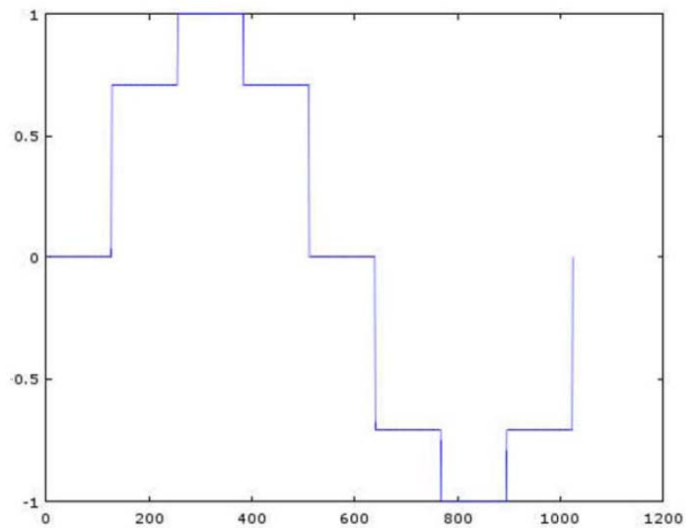
Claim 19: Low Pass Filtering DAC Output is Obvious



Gray notes that the inclusion of a lowpass filter following a D/A convertor is typically done to make sure that conversion artifacts are removed (element 111 in Fig 9: col. 15 lines 21-25).

Claim 19: Low Pass Filtering DAC Output is Obvious

of its sampling rate. A low-pass filter would be used to remove the high frequency components, producing a smoother waveform, as shown below:



Claim 19: Low Pass Filtering DAC Output is Obvious

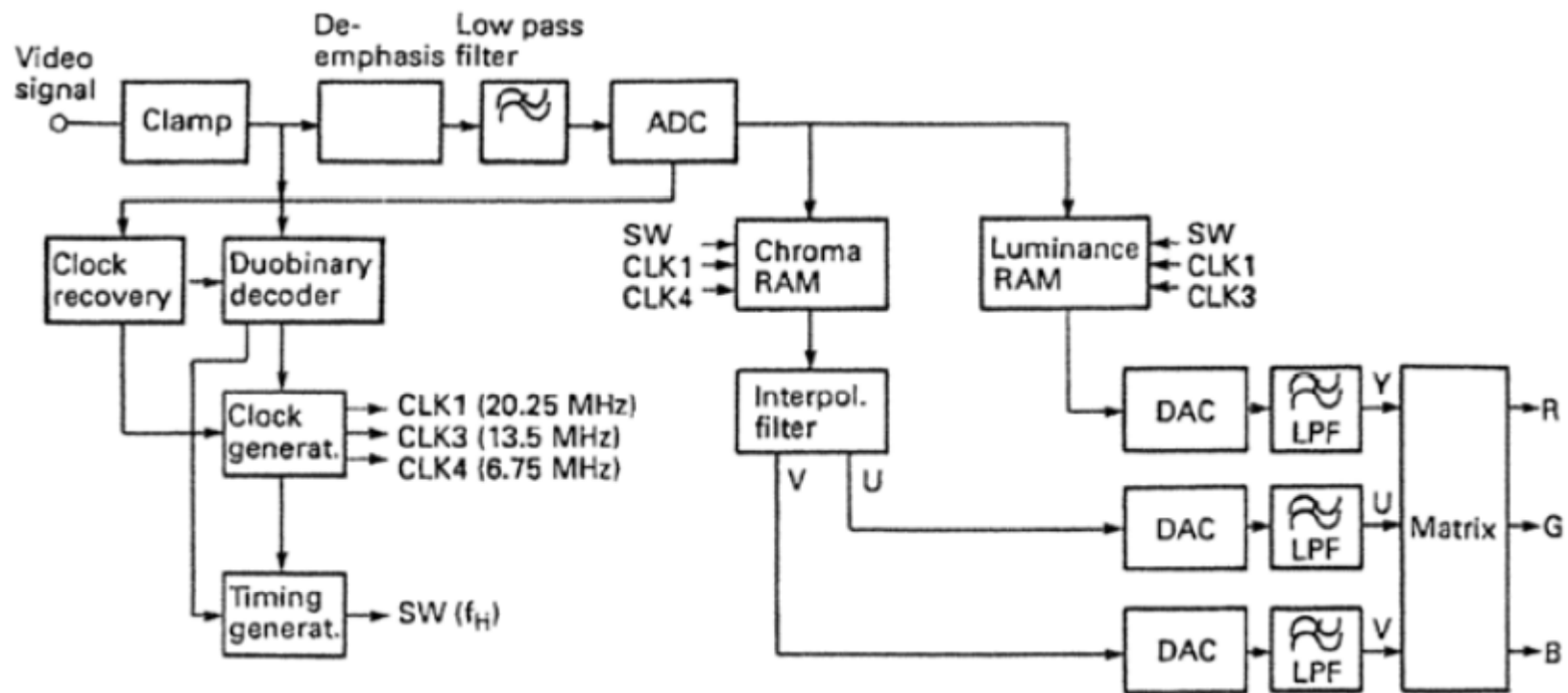


Figure 31.23 Notional diagram of a typical MAC vision decoder

Conclusion

- All instituted claims are unpatentable
- Questions?
- Thank you

