

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SILICON LABORATORIES, INC.  
Petitioner

v.

CRESTA TECHNOLOGY CORPORATION  
Patent Owner

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Case IPR Unassigned  
Patent 7,265,792

Title: Television Receiver for Digital and Analog Television Signals

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**PETITION FOR INTER PARTES REVIEW OF  
U.S. PATENT NO. 7,265,792  
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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## EXHIBIT LIST

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| Exhibit 1001 | U.S. Patent No. 7,265,792, titled “Television Receiver for Digital and Analog Signals,” to Favrat et al. (“the ‘792 patent”).                                                                                   |
| Exhibit 1002 | Complaint in <i>Cresta Technology Corporation v. Maxlinear, Inc. et al.</i> , Case No. 1:14-cv-00079-RGA before the United States District Court for the District of Delaware (January 21, 2014) (“Complaint”). |
| Exhibit 1003 | Complaint in ITC Investigation No. 377-TA-910 (January 28, 2014) (“ITC Complaint”).                                                                                                                             |
| Exhibit 1004 | European Patent Application No. EP 0696854, titled “Broadcast Receiver Adapted for Analog and Digital Signals,” assigned to Thomson Multimedia S.A. (“ <i>Thomson</i> ”).                                       |
| Exhibit 1005 | Clay Olmstead & Mike Petrowski of Harris Semiconductor, <i>A Digital Tuner for Wideband Receivers</i> , DSP Applications Magazine, Sep. 1992 (“Harris”).                                                        |
| Exhibit 1006 | Al Lovrich & Ray Simar, Jr., “Implementation of FIR/IIR Filters with the TMS32010/TMS32020,” Application Report: SPRA003A (Texas Instruments 1989) (“TI App Note”).                                             |
| Exhibit 1007 | U.S. Patent Application No. 2004/0061804, titled “Broadband Receiver Having a Multistandard Channel Filter,” to Favrat et al. (“the ‘585 application”).                                                         |
| Exhibit 1008 | U.S. Patent No. 6,369,857, titled “Receiver for Analog and Digital Television Signals,” to Balaban et al. (“Balaban”).                                                                                          |
| Exhibit 1009 | Declaration of Douglas Holberg (“Holberg Dec.”).                                                                                                                                                                |
| Exhibit 1010 | Excerpts of the prosecution file history of the ‘792 patent.                                                                                                                                                    |

- Exhibit 1011 U.S. Patent No. 6,804,497, titled “Partitioned Radio-Frequency Apparatus and Associated Methods,” to Kerth et al. (“Kerth”).
- Exhibit 1012 U.S. Patent 5,999,567, titled “Method for Recovering a Source Signal from a Composite Signal and Apparatus Therefor,” to Torkkola. (“Torkkola”).
- Exhibit 1013 U.S. Patent 6,263,222, titled “Signal Processing Apparatus,” to Diab et al. (“Diab”).
- Exhibit 1014 Rufus P. Turner & Stan Gibilisco, “The Illustrated Dictionary of Electronics,” p. 543 (5th ed. 1991).
- Exhibit 1015 Product Bulletin, Cirrus Logic CS92288 (single-chip, real-time MPEG audio/video CODEC with system mux/demux and OSD), published 2002 by Cirrus Logic, Inc. (collectively with Exs. 1016 and 1017, “Cirrus Logic”).
- Exhibit 1016 Data Sheet, Cirrus Logic CS4223/CS4224 (24-bit 105 dB audio codec with volume control), published April 2000 by Cirrus Logic, Inc. (collectively with Exs. 1015 and 1017, “Cirrus Logic”).
- Exhibit 1017 Data Sheet, Cirrus Logic CS4954/CS4955 (NTSC/PAL digital video encoder), published April 1999 by Cirrus Logic, Inc. (collectively with Exs. 1015 and 1016, “Cirrus Logic”).
- Exhibit 1018 U.S. Patent Application No. 2002/0057366, titled “Decoder Device and Receiver Using the Same,” to Oku et al. (“Oku”).
- Exhibit 1019 U.S. Patent No. 4,872,054, titled “Video Interface for Capturing an Incoming Video Signal and Reformatting the Video Signal,” to Gray et al. (“Gray”).
- Exhibit 1020 U.S. Patent No. 7,962,949, titled “Electronic Component Allowing the Decoding of Digital Terrestrial or Cable Television Signals,” to Busson et al. (“Busson”).

- Exhibit 1021 U.S. Patent No. 7,280,616, titled “Optimizing a Filter Bandwidth in a Digital Receiver,” to Arambepola et al. (“Arambepola”).
- Exhibit 1022 U.S. Patent No. 4,782,385, titled “Frequency Conversion of an RF Signal Transmitted for Color-Television Receivers,” to Gunter et al. (“Gunter”).
- Exhibit 1023 U.S. Patent No. 6,124,898, titled “Digital Television Receiver with Equalization Performed on Digital Intermediate-Frequency Signals,” to Patel et al. (“Patel”).
- Exhibit 1024 Kanwar Jit Singh and Alberto Sangiovanni-Vincentelli, *A Heuristic Algorithm for the Fanout Problem*, Proceedings of the 27th ACM/IEEE Design Automation Conference (1990). (“Singh”).
- Exhibit 1025 David Redmond et al., *A GSM/GPRS Mixed-Signal Baseband IC*, 2002 IEEE International Solid-State Circuits Conference (pub. 2002) (“Redmond”).
- Exhibit 1026 U.S. Patent No. 4,595,910, titled “Digital-to-analog Converter Useful in a Television Receiver,” to Wine (“Wine”).
- Exhibit 1027 U.S. Patent No. 4,292,597, titled “Circuit for Converting Single-Ended Input Signals to a Pair of Differential Output Signals,” to Niimura et al. (“Niimura”).
- Exhibit 1028 U.S. Patent No. 5,583,574, titled “Video-Data Transmitter, Video-Data Receiver, and Video-Data Transceiver for Connecting Parallel Video-data into Serial Video-data and Vice Versa,” to Tanaka et al. (“Tanaka”).
- Exhibit 1029 U.S. Patent No. 6,332,028, titled “Dual-Processing Interference Cancelling System and Method,” to Marash (“Marash”).
- Exhibit 1030 U.S. Patent No. 6,142,942, titled “Ultrasound Imaging System and Method Employing an Adaptive Filter,” to Clark (“Clark”).

- Exhibit 1031 U.S. Patent No. 6,324,290, titled “Method and Apparatus for Diagnosing Sound Source and Sound Vibration Source,” to Murakami et al. (“Murakami”).
- Exhibit 1032 U.S. Patent No. 6,282,176, titled “Full-Duplex Speakerphone Circuit Including a Supplementary Echo Suppressor,” to Hemkumar (“Hemkumar”).
- Exhibit 1033 U.S. Patent No. 6,275,592, titled “Method and an Arrangement for Attenuating Noise in a Space by Generating Antinoise,” to Vartiainen (“Vartiainen”).
- Exhibit 1034 U.S. Patent No. 6,147,713, titled “Digital Signal Processor for Multistandard Television Reception,” to Robbins et al. (“Robbins”).
- Exhibit 1035 U.S. Patent No. 7,272,375, titled “Integrated Low-IF Terrestrial Audio Broadcast Receiver and Associated Method,” to Tuttle et al. (“Tuttle”).
- Exhibit 1036 U.S. Patent No. 5,673,293, titled “Method and Apparatus for Demodulating QAM and VSB Signals,” to Scarpa et al. (“Scarpa”).



Petitioner hereby requests that the United States Patent and Trademark Office proceed with an *inter partes* review of claims 1–17, 26, and 27 of U.S. Patent No. 7,265,792 (“the ‘792 patent”) (Ex. 1001).

## **I. COMPLIANCE WITH FORMAL REQUIREMENTS**

### **A. Grounds for Standing (37 C.F.R. § 42.104(a))**

In accordance with 37 C.F.R. § 42.104(a), Petitioner certifies that the ‘792 patent is available for *inter partes* review. Petitioner further certifies that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the ‘792 patent on the grounds identified in this Petition.

### **B. Real Parties-In-Interest (37 C.F.R. § 42.8(b)(1))**

To the best of Petitioner’s knowledge, Silicon Laboratories, Inc. (“Petitioner”) and Cresta Technology Corporation (“Patent Owner”) are the real parties-in-interest in this matter.

### **C. Related Matters (37 C.F.R. § 42.8(b)(2))**

Petitioner is a defendant in two actions filed by Patent Owner involving the ‘792 patent: *Cresta Technology Corporation v. Maxlinear, Inc. et al.*, Case No. 1:14-cv-00079-RGA, filed on January 21, 2014 in the United States District Court for the District of Delaware (Complaint, Ex. 1002); and Investigation No. 337-TA-910, filed on January 28, 2014, in the International Trade Commission (“ITC”) (ITC Complaint, Ex. 1003). In both cases, Patent Owner sued several of Petitioner’s customers along with Petitioner. On May 5, 2014, Petitioner filed a

Petition for *inter partes* review on one of the other patents asserted in those cases. See IPR2014-00728. The patents at issue in both this Petition and the IPR2014-00728 petition share common inventors and common subject matter. Petitioner therefore requests that the two matters be consolidated before the Board.

**D. Counsel and Service Information (37 C.F.R. § 42.8(b)(3)–(4))**

| Lead Counsel                                                                                                                                                                     | Backup Counsel                                                                                                                                                                  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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**E. Fee**

Petitioner authorizes the Director to charge the fee specified by 37 C.F.R. § 42.15(a) and any additional fees associated with this Petition to Deposit Account No. 12-0769.

**F. Statement of Precise Relief Requested**

In accordance with 37 C.F.R. § 42.22, Petitioner respectfully requests cancellation of claims 1–17, 26, and 27 of the ‘792 patent.

**II. REASONABLE LIKELIHOOD TO PREVAIL**

This Petition, in accordance with 35 U.S.C. § 314(a), establishes a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in this petition because the Petition provides evidence and

supporting reasoning showing that all of the elements of each of claims 1–17, 26, and 27 of the ‘792 patent are unpatentable over the prior art.

### **III. IDENTIFICATION OF CHALLENGE**

#### **A. Prior Art Publications**

Petitioner relies on the following prior art publications:

1. Thomson, Exhibit 1004, was published on February 14, 1996, making it prior art at least under 35 U.S.C. § 102(b) (pre-AIA).
2. Harris, Exhibit 1005, was published on September 1992, making it prior art at least under 35 U.S.C. §102(b) (pre-AIA).
3. TI App Note, Ex. 1006, was published on or before 1997 making it prior art under §102(b) (pre-AIA).
4. The ‘585 application, Exhibit 1007, was filed in the United States on September 6, 2002, making it prior art at least under 35 U.S.C. §§ 102(a) and (e) (pre-AIA).
5. Balaban, Exhibit 1008, was filed May 13, 1999, making it prior art at least under 35 U.S.C. § 102(e) (pre-AIA).
6. Kerth, Exhibit 1011, claims priority to U.S. Provisional Patent Applications 60/273,119 filed March 2, 2001 and 60/261,506 filed January 12, 2001, making it prior art at least under 35 U.S.C. § 102(e) (pre-AIA).

7. Product Bulletin, Cirrus Logic CS92288 , Exhibit 1015, was published in 2002, making it prior art under 35 U.S.C. §§ 102(a) and (b) (pre-AIA).
8. Data Sheet, Cirrus Logic CS4223/CS4224 , Exhibit 1016, was published in April 2000, making it prior art under 35 U.S.C. §§ 102(a) and (b) (pre-AIA).
9. Data Sheet, Cirrus Logic CS4954/CS4955 , Exhibit 1017, was published in April 1999, making it prior art under 35 U.S.C. §§ 102(a) and (b) (pre-AIA).
10. Oku, Exhibit 1018, claims priority to No. 09/241,614 filed February 2, 1999, making it prior art under 35 U.S.C. §§ 102(a), (b), and (e) (pre-AIA).
11. Gunter Exhibit 1022 issued on November 1, 1988, making it prior art under 35 U.S.C. §§ 102(a), (b), and (e) (pre-AIA).
12. Patel, Exhibit 1023, issued on September 26, 2000, making it prior art under 35 U.S.C. §§ 102(a), (b), and (e) (pre-AIA).

**B. Brief Statement of Grounds for Challenge**

Petitioner challenges claims 1–17, 26, and 27 (“the challenged claims”) of the ‘792 patent on the following grounds:

**Ground 1:** Claims 1, 2, 4, 10, 11, and 26 are invalid under 35 U.S.C. § 103 as obvious over Thomson (Ex. 1004) in view of Harris (Ex. 1005).

**Ground 2:** Claims 1, 2, 4, 10, 11, and 26 are invalid under 35 U.S.C. § 103 as obvious over Thomson (Ex. 1004) in view of TI App Note (Ex. 1006).

**Ground 3:** Claim 3 is invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Gunter (Ex. 1022) or, in the alternative, Thomson and TI App Note in further view of Gunter (Ex. 1022).

**Ground 4:** Claims 5 and 6 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Cirrus Logic (Exs. 1015–1017) or, in the alternative, Thomson and TI App Note in further view of Cirrus Logic.

**Ground 5:** Claims 7 and 12 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Kerth (Ex. 1011) or, in the alternative, Thomson and TI App Note in further view of Kerth.

**Ground 6:** Claims 13–17 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.

**Ground 7:** Claims 8 and 9 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Kerth and Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Kerth and Cirrus Logic.

**Ground 8:** Claims 26 and 27 are invalid under 35 U.S.C. § 103 as obvious over Thomson and Harris in further view of Balaban (Ex. 1008) or, in the alternative Thomson and TI App Note in further view of Balaban.

**Ground 9:** Claims 1 is invalid under 35 U.S.C. § 102 as anticipated by Patel (Ex. 1023).

None of these grounds are redundant. While grounds 1 and 2 each present an obvious combination with Thomson as the primary reference, Harris teaches a FIR filter in combination with a microprocessor whereas TI App Note describes a reprogrammable DSP implementing a FIR filter. Grounds 3 through 8 address claims that are not addressed by any other ground. Ground 9 addresses challenged claim 1 under §102, while grounds 1 and 2 address challenged claim 1 under §103.

This Petition, supported by the Declaration of Douglas Holberg (“Holberg Dec.”) (Ex. 1009) filed with this Petition, demonstrates that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the challenged claims and that each of the challenged claims is unpatentable for the reasons cited in this petition. (*See* 35 U.S.C. § 314(a)).

#### **IV. INVALIDITY OF THE ‘792 PATENT**

##### **A. Introduction**

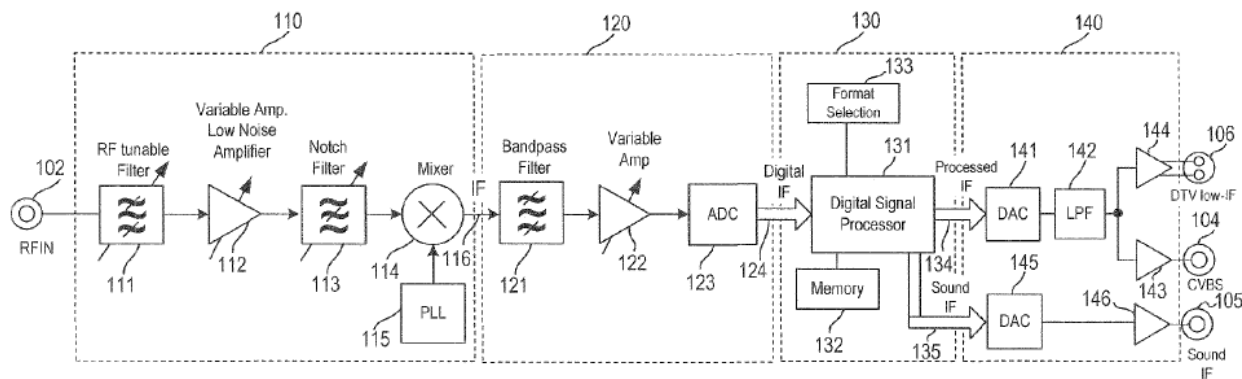
The ‘792 patent, titled “Television Receiver for Digital and Analog Television Signals,” was filed July 1, 2014 and originally assigned to Xceive Corp. (Ex. 1001). After Xceive’s business faltered, Cresta Technology Corp. (“CrestaTech”) purchased certain of Xceive’s assets including the ‘792 patent on October 10, 2011. (ITC Complaint, Ex. 1003, p.4). In January of this year,

CrestaTech sued Petitioner and several of its customers for infringing three of the patents it acquired from Xceive. (*Id.*).

The ‘792 patent builds on the earlier ‘585 patent (application publication Exhibit 1007). Both are directed towards a television signal receiver and, in particular, “a broadband television signal receiver for receiving multi-standard analog television and digital television signals.” (*Compare* Ex. 1001 at 1:6–10 with Ex. 1007 at [0002]). In fact, as described further below, the Examiner rejected many of the original ‘792 patent claims as “being anticipated” by the published ‘585 patent application. (Ex. 1010 at 75 (citing “Favrat et al.,” US2004/0061804 A1, published April 1, 2004)).

As described in IPR2014-00728, Thomson Multimedia anticipated the move to DSP-based, multi-format television signal receivers long before Xceive filed the application that resulted in its ‘585 patent. (*See* Ex. 1004). By the time Xceive filed its ‘792 application, it conceded that the industry had already addressed this perceived need. (Ex. 1001 at 2:4–5 (“Television receivers for receiving both analog and digital television signals are being developed.”)). In particular, Xceive acknowledged that U.S. Pat. No. 6,369,857 to Balaban described “digitizing the intermediate frequency signal and processing the digitized signal using two separate processing circuitry—one for the analog television signal and one for digital television signal.” (*Id.* at 2:15–20).

As a result, the ‘792 application pivoted to focus on the output circuitry. Specifically, the ‘792 application describes several iterations of a “signal output circuit,” labeled “140” in Fig. 1 (below). (*Id.* at 6:49–51).



This output circuit converts the “processed IF signals” into “the desired output signals.” (*Id.*) Figure 2 goes on to illustrate several other “desired output signals” including analog v. digital, single-ended v. differential, or serial v. parallel. (*Id.* at Fig. 2; 7:34–35 (“Turning now to FIG. 2 where alternate embodiments of the signal output circuit are shown.”). Many of the challenged claims recite the different permutations of these “desired output signals.” (*See, e.g., id.* at claim 13). Converting an output signal from one desired output form to another is not patentable. A person of ordinary skill in the art (“POSITA”) would know that a digital-to-analog converter (“DAC”) would be necessary if the desired output format was analog instead of digital. (Ex. 1009, ¶ 9 (citing Ex. 1026 (“Digital-to-Analog Converter useful in a television receiver”))). Likewise, a POSITA would know that a single to differential-ended converter was necessary to convert a signal



ended output to a differential-ended output, if a differential-ended output was desired. (Ex. 1009, ¶ 9 (citing Ex. 1027, Abstract (“A circuit that is particularly adapted to convert a single-ended input signal to a pair of differential output signals,” which finds ready application in “a color saturation control circuit in a color television receiver.”))). Similarly, a POSITA would know that a parallel-to-serial converter (i.e., “serializer”) was necessary if the desired output format was serial rather than parallel. (Ex. 1009, ¶ 9 (citing Ex. 1028 (“a transceiver for video data . . . comprises . . . a parallel-to-serial converter that converts the word-multiplexed parallel data into serial data”))). As the Federal Circuit explained in *Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006), such use of known elements in such predictable ways is obvious. (*See also KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)).

In this case, the choice of the desired output signal format is driven by the desire for a “cheaper,” “faster,” “smaller,” “or more efficient” television receiver, as the ‘792 patent concedes. (*Id.* at 2:22–24 (“It is further desired that such a dual-format television receiver be cost effective to manufacture and provides high quality video and audio performance.”); 6:51–56 (“A configuration for signal output circuit 140 can be selected based on factors such as the desired pin count for receiver 100 and the desired format for the output signals.”))). As the Supreme Court further explained in *KSR*, when, as here, “there is a design need or market

pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp.” 550 U.S. at 421. All of the claimed options are well within the grasp of a POSITA, as evidenced by the legions of prior art references using these options. (Ex. 1009, ¶ 5). For the reasons described in detail below, the challenged claims should be cancelled.

### **B. Prosecution History of the ‘792 Patent**

The ‘792 patent application was filed on July 1, 2004. In the first office action, claims 1–4, 11, 12, and 30–34 were rejected under 35 U.S.C. § 102(b) as anticipated by the published ‘585 patent application (Ex. 1007). Claims 5, 10, 13, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the ‘585 application in view of Oku (Ex. 1018). Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the ‘585 application in view of Oku, in further view of Gray (Ex. 1019). Claims 6–9, 15, and 18–29 were indicated to contain allegedly allowable subject matter. (Ex. 1010, pp. 75–77).

In response to the first office action, the applicant amended claim 1 to recite the limitations formerly of claim 24. (Ex. 1010, p. 84). The applicant also amended all of the other claims to depend from claim 1. Because the subject matter of claim 24 had been indicated as allowable, the applicant argued that independent claim 1 and all depending claims were therefore allowable. The

applicant cancelled claim 24 as well as claims 31–34 and requested allowance of all remaining claims.

The Examiner then allowed all remaining claims in the application (Ex. 1010 at 99), despite the fact that the limitation added to claim 1 by amendment was clearly taught in the ‘585 application. For example, claim 11 of the ‘585 application is virtually identical to the allegedly allowable subject matter. (See Ex. 1007 at claim 11 “wherein said signal processor applies one of a plurality of finite impulse response filters”). Clearly the Examiner should have maintained his rejection even in light of the amendment.<sup>1</sup>

### **C. Person of Ordinary Skill in the Art**

A person of ordinary skill in the art at the time of the alleged invention of the ‘792 patent (“POSITA”) would have held at least a Masters of Science or higher degree in electrical engineering, have at least four years of experience with mixed signal system design, including analog front ends and subsequent digital signal processing of various analog and digital signal formats of video and audio content. (Ex. 1009, ¶ 11).

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<sup>1</sup> As a result, while the patent is clearly invalid on double patenting grounds, Petitioner is unable to raise those grounds in this proceeding.

#### **D. Claim Construction**

The claims in an *inter partes* review should be accorded the broadest reasonable construction, as commonly understood by those of ordinary skill in the art in view of the descriptions of the specification. (See 37 C.F.R. § 42.100(b)). Petitioner contends that all of the terms in the challenged claims should be given their plain and ordinary meaning.

One term that may require additional consideration is the “signal processor” element of independent claim 1. (Ex. 1001 at claim 1). Petitioner contends that the broadest reasonable construction of “signal processor” in light of the specification is: any device that processes an input or output signal. (Ex. 1009, ¶ 14; “The Illustrated Dictionary of Electronics,” Ex. 1014, p. 543). This definition is supported by the intrinsic evidence as well as the extrinsic evidence.

The ‘792 patent describes a “DSP 131 [that] processes the digital IF signal according to the television format and standard to which the input RF signal is encoded.” (Ex. 1001 at 5:50–52). A DSP, as the name implies, is a form of a “signal processor,” but not the only one. (Ex. 1009, ¶ 14). A “signal processor” can take many different forms including “a preamplifier, expander, amplifier limiter, delay network, and the like.” (*Id.* (quoting “The Illustrated Dictionary of Electronics,” Ex. 1014, p. 543)). Accordingly, one skilled in the art would

interpret “signal processor” to be any device that processes an input or output signal. (*Id.*).

Petitioner contends that this element is not governed by 35 U.S.C. § 112, ¶ 6. Even if the term “processor” is considered a “nonce term,” the element goes on to recite specific structure in the form of “a plurality of finite impulse response filters” that takes the element out of §112, ¶6. *See Sage Prods., Inc. v. Devon Indus., Inc.*, 126 F.3d 1420, 1427–28 (Fed.Cir.1997).

## **V. DETAILED EXPLANATIONS OF THE CHALLENGES**

Independent claim 1 recites a television receiver. All of the remaining challenged claims (2–17, 26, and 27) depend from independent claim 1. A detailed explanation is provided below for each ground for each of the challenged claims.

### **A. Ground 1: Claim 1 is obvious over Thomson in view of Harris.**

#### **1. Preamble**

Under the broadest reasonable interpretation, Petitioner does not believe that the preamble of claim 1 is limiting. Even assuming it is, however, Thomson clearly describes the claimed “television receiver.” (Ex. 1004 at 1:3–4 (“invention relates to a broadcast receiver”)). Thomson describes a “multi-standard tuner” capable of receiving television signals transmitted in the form of a satellite broadcast, terrestrial, and cable transmissions in the range of “950-1750 MHz.” (*See id.* at 1:55–2:19). Thomson teaches this element. (Ex. 1009, ¶ 16).

#### **2. “a frequency conversion circuit”**

The first element of claim 1 recites “a frequency conversion circuit.” Thomson likewise describes a circuit that receives an incoming satellite signal “of about 2 GHZ” and, via a multi-stage frequency down conversion process, converts that signal to a signal having a lower frequency. (Ex. 1004 at 1 “Gist of the Invention”; 2:30–33). For at least these reasons, Thomson teaches this element. (Ex. 1009, ¶ 17).

- a. “for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF)”

The Thomson “multi-standard tuner” receives the RF signal from an “outdoor” satellite unit, which “supplies the satellite channels already down-converted in a frequency band covering 950-1750 MHz.” (Ex. 1004 at 1:55–60). As mentioned above, this RF signal is converted to a “140 MHz Sat-IF signal” that forms the “IF<sub>SAT</sub>” input to the circuit as shown above in Fig. 1. (Ex. 1004 at 2:17–19, Fig. 1). This signal then gets further “down-converted” by “mixer stage 2” into “an IF signal of around 75 MHz (see Figs. 2d and 2e).” (*Id.* at 2:53–57). Therefore, Thomson teaches this element. (Ex. 1009, ¶ 18).

- b. “the input RF signal encoding information in one of a plurality of television signal formats”

Thomson teaches that the “multi-standard tuner” can receive RF signals in a plurality of formats, including “analog or digital ones.” (*See, e.g.*, Ex. 1004 at

1:42–43). The ‘792 patent likewise identifies “analog or digital” as two different television signal “format[s].” (*Id.* at 1:30). For at least these reasons, Thomson teaches this element. (Ex. 1009, ¶ 19).

3. “an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof”

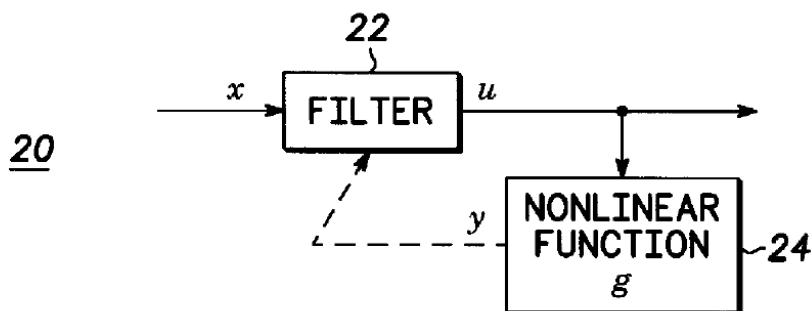
The filtered output of the AGC amplifier 5 in Thomson is coupled to an analog-to-digital converter (“A/D”) 7. (Ex. 1004 at Fig. 1). The “A/D-converter [is] necessary for the digiti[z]ing” of the bandpass-filtered intermediate frequency signal output of AGC 5. (Ex. 1004 at 1:47; *see also* Fig. 1). As the name implies, A/D 7 converts the filtered IF signal to, in the words of claim 1, “a digital representation thereof.” Fig. 1 shows that “A/D 7” has a sampling frequency of “ $f_s$ .” Thomson further teaches that in one embodiment the “A/D converter (7) operates with a sampling frequency of about 100MHz.” (*Id.* at 4:14–16). For at least these reasons, Thomson teaches this element. (Ex. 1009, ¶ 20).

4. “a signal processor for”

Thomson describes a “bandpass filter 8” that has “an adaptively controlled bandwidth” that passes the analog TV encoded information in the case of analog formatted signal or the digital TV encoded information in the case of digital formatted signal. (Ex. 1004 at 3:16–25). The adaptive filter 8 makes this selection based on the “TV standard” input to the filter. (*Id.* at Fig. 1; Ex. 1009, ¶ 21). By

disclosing an adaptive bandpass filter that processes an input or output signal (e.g., it filters an analog or digital TV signal), Thomson teaches a signal processor. (Ex. 1009, ¶ 21).

Additionally, those skilled in the art would consider the adaptive filter in Thomson to be a “signal processor,” as recited in claim 1. (Ex. 1009, ¶ 22 (citing U.S. Pat. Nos. 5,999,567 and 6,263,222)). United States Patent Number 5,999,567, for example, “shows a *signal processor 20* for processing a composite [television] signal.” (Ex. 1012 at 4:59–62). Indeed, the signal processor 20 includes adaptive filter 22:



(*Id.* at Fig. 2). U.S. Pat. No. 6,263,222, likewise teaches “wherein the signal processor comprises an adaptive filter.” (Ex. 1013 at 76:3–4). Unquestionably, an adaptive filter is a “signal processor” under the ordinary meaning of that term. (Ex. 1009, ¶ 22).

Even if the adaptive bandpass filter of Thomson is not considered a “signal processor” *per se*, as described in the next section, it would have been obvious to a POSITA to implement the Thomson adaptive filter using a digital signal processor



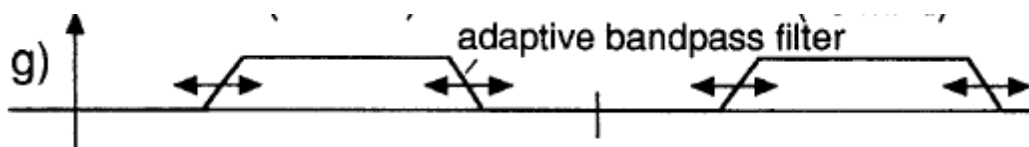
as taught by Harris. (See Ex. 1009, ¶ 23; see also Harris, Ex. 1005 at 1). Harris describes a digital signal processor to convert and filter IF signals. (Ex. 1005 p. 3 (“With the advancement of ADC technology and the evolution of high performance DSP circuitry, the analog second IF processor functions can be replaced with [a] digital processing chain . . . .”)). Thomson and Harris individually or in combination disclose a signal processor. (Ex. 1009, ¶ 23).

5. “processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate frequency signal, each of the plurality of finite impulse response filters corresponding to a format of the input RF signal”

Thomson discloses a signal processor that implements an adaptive filter having varying bandpass frequencies. Harris discloses a signal processor that implements a FIR filter. This element is rendered obvious by incorporating the FIR filter of Harris into the adaptive filter of Thomson.

The adaptive filter in Thomson processes intermediate frequencies according to the format of an input RF signal. An “adaptive filter is a filter which can change its characteristics by changing its filter coefficients.” (Ex. 1009, ¶ 25 (quoting Ex.

1029 and Ex. 1030 (“Generally, an adaptive filter is a filter having a transfer function that can be adjusted, or changed, based on the sampled signal statistics, or signal features, associated with an input or output signal.”)). The transfer function of the Thomson adaptive filter is illustrated in the frequency map of Fig. 2(g) (reproduced below):

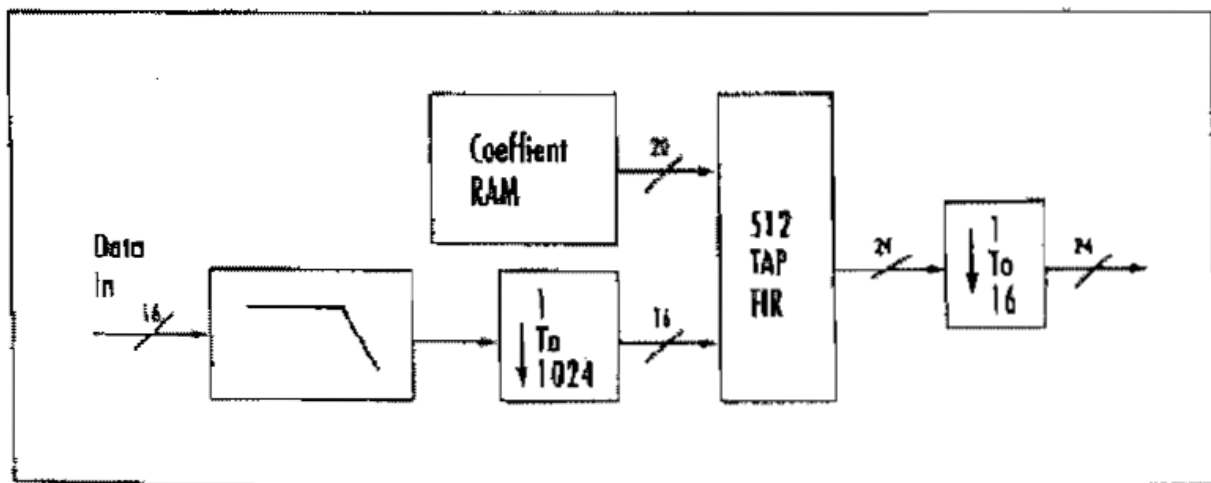


(Ex. 1004 at Fig. 2). The upper and lower bounds of the Thomson filter vary or “adapt” according to the format of the input RF signal, as indicated by the “TV Standard” input to the filter. (Ex. 1009, ¶ 25; *see also* Ex. 1004 at 3:16–19 (“bandpass filter 8 (see Fig. 2g) with an adaptively controlled bandwidth selects the desired signal”), Fig. 1).

The status of the “TV standard” input determines the function of the bandpass filter: the filter executes one filter function if the RF input signal is an analog TV format, or another filter function if it is in a digital TV format. (Ex. 1009, ¶ 26; *see also* Ex. 1004 at Fig. 1 (“TV Standard” input to “filter 8”); *see also* (Ex. 1004 at 3:16–18 (“bandpass filter 8 (Fig. 2g) with an adaptively controlled bandwidth selects the desired signal with a minimal remainder of adjacent channel signals.”)). Accordingly, the Thomson filter 8 is adapted to the particular TV format (e.g., analog or digital), receives the “digital representations of said

intermediate signals” output by the A/D 7, processes those digital representations according to its transfer function “in accordance with said format of said input RF signal,” as indicated by the TV standard input, and “generat[es] digital output signals indicative of information encoded in said input RF signal.” (Ex. 1009, ¶ 26). While Thomson does not explicitly disclose the use of FIR filters, Harris does.

Harris describes a processor-based FIR filter that can function as an adaptive filter. For example, Harris discloses the following digital decimation filter (“DDF”) including a finite impulse response filter:



(Ex. 1005 at 4). The Harris digital decimation filter (“DDF”) includes a “512 TAP FIR” filter coupled to a “coefficient RAM” that stores the FIR filter coefficients. (*Id.*). The DDF “can be rapidly reconfigured via a standard microprocessor interface.” (*Id.* at 5). In other words, this filter, combined with a microprocessor, can retrieve the FIR filter coefficients from memory and store those in the

“coefficient RAM.” (Ex. 1009, ¶ 27) just like the ’792 Patent ((’792 Pat. at 5:59–63 (“In one embodiment, the coefficients of the filter functions are stored in a look-up table in memory 132 in DSP circuit 130. DSP 131 retrieves the coefficients from memory 132 to be applied to the incoming digital signals.”). Harris further teaches that if this filter is used in “systems where the second IF filter state consists of a bank of filters to support various operational modes, cost and board space can be saved be [sic:by] *reconfiguring a single DDF to implement the filter required by each operational mode.*” (Ex. 1005 at 5 (emphasis added)).

It would have been obvious for one of ordinary skill in the art to incorporate the FIR filters of Harris into the Thomson adaptive filter and render this claim limitation obvious. (Ex. 1009, ¶ 28). Although both FIR and infinite impulse response (IIR) filters were well known in the art, (*See, e.g.*, Ex. 1006; Ex. 1009, ¶ 28), a POSITA would have been motivated to choose a FIR filter over an IIR filter for several reasons. A FIR filter produces “a linear phase, and only FIR filters can be designed to have linear phase,” which is a critical parameter in audio and video applications such as Thomson. (*Id.* (quoting TI App Note, Ex. 1006 at 21). FIR filters are also more stable and have less sensitivity to coefficient quantization than IIR filters. (Ex. 1009, ¶ 28). The FIR implementation of Harris would be an obvious design choice in the Thomson application because both Harris and Thomson solve similar problems, namely tuning an adaptive filter to the input

format or operational mode of the system. (Ex. 1009, ¶ 28). Harris also explicitly teaches that the “declining cost of technology is making DSP a desirable alternative for an expanding spectrum of communication problems.” (Ex. 1005 at 7). A POSITA would have interpreted that suggestion to include digital television such as in Thomson. (Ex. 1009, ¶ 28). For these reasons, a POSITA would have been motivated to use the FIR filters of Harris to implement the plurality of filter functions for the adaptive filter of Thomson, thereby rendering this limitation obvious. (*Id.*). Because such a well known combination would have had a reasonable expectation of success (*See* Ex. 1023, 6:1–5, 15:51–54 (implementing adaptive FIR filters using a “filter coefficient computation apparatus”)), a POSITA would be motivated to make such a combination. (*Id.*).

6. “a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals.”

Thomson discloses an output circuit including a plurality of demodulators, each coupled to receive output signals from said signal processor. (Ex. 1004 at Fig. 1 showing FM-demodulator 9 and QPSK-demodulator (12, 13) connected in parallel to receive the output signals from the adaptive bandpass filter 8 (i.e. “said signal processor”)). Thomson discloses that the “FM-demodulator (9)” demodulates the digital signals encoding information in the analog TV format and the “QPSK-demodulator (12, 13)” demodulates the digital signals encoding

information in the digital TV format. (Ex. 1004 at 4:10–11). Therefore Thomson discloses demodulators receiving processed I/Q output signals from the processor and outputting signals corresponding to received digital television signals. (Ex. 1009, ¶ 29).

Thomson discloses a TV receiver that receives TV signals having both audio and video components. “The FM demodulator 9 converts the IF signal into the CVBS signal and the subcarrier modulated sound signals.” (Thomson, Ex. 1004 at 3:19–21). Thomson further discloses “synchronous demodulators 12, 13 for QPSK quadrature demodulation and low pass filters 14, 15 providing signal Q, I at outputs of circuit 4.” (*Id.* at 2:41–44). One of ordinary skill in the art would understand that the video and audio information of digital TV signals (e.g. as MPEG) may be digitally encoded in a single signal (Ex. 1009, ¶ 30), and also that the I and Q baseband signal components must carry both the video and audio information for the TV signals of Thomson to serve the expressly disclosed purpose of a digital TV receiver (Ex. 1009, ¶ 30). For at least these reasons, Thomson teaches this element. (*Id.*).

**B. Ground 1: Claim 2 is obvious over Thomson in view of Harris.**

“2. The television receiver of claim 1, wherein the plurality of television signal formats comprises an analog television format and a digital television format.”

Thomson discloses an “architecture allow[ing] a digitising of the Sat-IF signals no matter that they are analog or digital ones.” (Thomson, Ex. 1004 at 1:42–43). Further, Thomson discloses that “a digital solution for video IF signals should no longer be excluded in the satellite TV receiver design,” and the receiver “should also include the classical analog satellite reception . . . .” (*Id.* at 1:24–28). Thomson teaches this element. (Ex. 1009, ¶ 31).

**C. Ground 1: Claim 4 is obvious over Thomson in view of Harris.**

1. “4. The television receiver of claim 1, wherein the signal output circuit provides a first output signal being a video baseband signal corresponding to an analog television format and a second output signal being an audio baseband signal corresponding to the analog television format.”

The FM-demodulator 9 of Thomson demodulates the digital signals corresponding to signals broadcast in analog TV format (Ex. 1004 at 3:19–22) to generate baseband video signals (i.e., Composite Video Baseband Signal (“CVBS”), and audio signals “ $S_{\text{mod1}}$ ,” “ $S_{\text{mod2}}$ ,”. (*Id.* at Fig. 1; Ex. 1009, ¶ 32). Thomson teaches this element. (Ex. 1009, ¶ 32).

**D. Ground 1: Claim 10 is obvious over Thomson in view of Harris.**

- “10. The television receiver of claim 1, further comprising: a bandpass filter coupled to receive the intermediate frequency signal from the frequency conversion circuit and generate a filtered intermediate frequency signal; and a variable gain amplifier coupled to receive the filtered intermediate frequency signal and

provide the amplified, filtered intermediate frequency signal to the analog-to-digital converter.”

The receiver of Thomson teaches that the incoming RF satellite signal is filtered by SAW Filter 1 and then down-converted by mixer 2 to an intermediate frequency (“IF”) signal. (Ex. 1001 at 2:47–57). The IF signal is then passed through automatic gain amplifier “AGC 5,” with “an internal bandpass limitation before the IF signal enters the input of the A/D-converter 7.” (*Id.* at 2:57–3:3). The automatic gain amplifier adjusts or varies its gain based upon an input generated by AGC control circuit 6. (*Id.*). Because “AGC amplifier 5 has to make sure that the full dynamic range of the A/D-converter 7 is exploited to keep the quantizing noise to a minimum,” (Ex. 1004, 3:1–3), a POSITA would understand (or at least it would have been a simple design choice) that the intermediate signal frequency is filtered before amplification. (Ex. 1009, ¶ 33). The AGC 5 with internal bandpass of Thomson therefore satisfies this element. (Ex. 1009, ¶ 33).

**E. Ground 1: Claim 11 is obvious over Thomson in view of Harris.**

“11. The television receiver of claim 1, wherein the signal output circuit provides output signals in an analog or a digital signal format.”

As discussed at Section V(A)(6) above, Thomson discloses an output circuit including a plurality of demodulators, each coupled to receive output signals from the signal processor. Thomson further discloses two different demodulators, each dedicated to processing digitized signals in a particular TV format (i.e., analog or



digital). As shown in Fig. 1, the digitized output signals of the adaptive filter 8 are input to “an FM demodulator (9) [which provides output in an analog TV signal format] and a QPSK demodulator (12, 13) [which provides output in a digital TV signal format].” (Ex. 1004 at 4:10–11; Ex. 1009, ¶ 34). Moreover, a POSITA would have been motivated to use a digital-to-analog converter to convert a digital signal format to an analog signal format. (Ex. 1009, ¶ 34; *see* Oku, Fig. 4 (showing DACs 16, 21, and 25)). Thomson teaches this element. (Ex. 1009, ¶ 34).

**F. Ground 1: Claim 26 is obvious over Thomson in view of Harris.**

1. “26. The television receiver of claim 1, further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the input RF signal”

Thomson discloses a bandpass filter 8 that receives a “TV standard” signal that indicates whether, for example, the incoming RF signal is in an analog or digital format. (Ex. 1004, Fig. 1; Ex. 1009, ¶ 35). A POSITA would understand that the TV standard signal is a signal generated by a circuit within the Thomson receiver, rather than a signal that is directly received by Thomson receiver. For example, Scarpa discloses a selection circuit, namely “[a]n MTS output of the AQM/VSB signal detection circuit 301 is coupled to corresponding inputs of the filter circuit 320.” Ex. 1036, 13:37–45; *see also id.* at 14:37–65 (“The configuration of the first and second complex FIR filters 324, 322 are controlled by

the MTS signal.”); Ex. 1008, 7:66–8:5 (describing a user-selectable “simple switch” or “programming feature.”)). This TV standard signal is a “TV standard” selection signal of Thomson generated by a “circuit,” which is a “standard selection circuit.” (*Id.*). Additionally, because the select signal in Thomson must be processed by at least one circuit element, Thomson inherently discloses this element. (Ex. 1009, ¶ 35). Therefore the “TV standard” selection signal that is input to bandpass filter 8 in Fig. 1 of Thomson anticipates or renders obvious (in combination with Scarpa or Balaban) the “standard selection circuit” . (*Id.*, ¶ 35; Ex. 1004, Fig. 1).

2. “the signal processor selecting a finite impulse response filter in response to the select signal.”

As previously described in Section V(A)(4) above, Thomson describes a bandpass filter that selects a particular filter in response to the “TV standard” input signal. (Ex. 1009, ¶ 36). Harris teaches a plurality of finite impulse response filters, each dedicated to a particular mode of operation. (See Section V(A)(4), *supra*). Harris further teaches that the FIR filters can be implemented in a single reprogrammable FIR filter to save board space. (Ex. 1005 at 4). Moreover, the bandpass filter in Thomson would select the particular FIR filter function that corresponds to the incoming RF signal format, as indicated by the “TV Standard” input. (Ex. 1009, ¶ 36). As discussed previously, a POSITA would have found it obvious to implement the bandpass filter of Thomson by using the reprogrammable

FIR filters taught by Harris in order to save board space and create a more robust filter. (*Id.*). For at least these reasons, claim 26 is obvious over Thomson in view of Harris. (*Id.*).

**G. Ground 2: Claim 1 is obvious over Thomson in view of TI App Note**

As described above in Section V(A), Thomson expressly describes all of the elements of claim 1 “signal processor” under its plain and ordinary meaning. (*See* Sec. V(A), *supra*). The TI App Note expressly teaches the use of a programmable digital signal processor to implement FIR filters. As described further below, using the programmable DSP-based FIR filter of the TI App Note to implement the adaptive filter of Harris would have been an obvious design choice to a POSITA. (Ex. 1009, ¶ 37).

“a signal processor for processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal,”

As described above, Thomson describes an adaptive filter that performs this function. The 1989 TI App Note (reprinted in 1997), titled “Implementation of FIR/IIR Filters with the TMS30101/TM32020,” describes “a variety of methods for implementing Finite Impulse Response (FIR) . . . digital filters with the TMS320 family of digital signal processors.” (Ex. 1006 at 7). The note is intended to encourage use of TI’s digital signal processors to implement filters in a variety of different applications including “such as removing noise from a signal,

removing signal distortion due to the transmission channel, separating two or more distinct signals that are mixed in order to maximize communication channel utilization.” (Ex. 1006 at p.7). One of the “important advantages” of using “a programmable processor such as the TMS320 is the ease of changing the filter parameters to modify the filter characteristics.” (*Id.*; Ex. 1009, ¶ 38).

It would have been obvious to use “a programmable processor such as the TMS320” to implement the adaptive filter in Thompson in light of the teaching in TI App Note. (Ex. 1009, ¶ 39). When the ‘792 patent was filed, programmable DSPs were commonly used to implement adaptive filters, in no small part because of publications like the TI App Note that simplified the implementation of such filters. (*See id.* (citing U.S. Pat. No. 6,324,290 at 5:27–29; 6,282,176 at 3:54–55; 6,142,942 at Fig. 2A–2B; 6,275,592 at 6:16–19)). One common application for DSPs was the optimal implementation of digital filters. (Ex. 1009, ¶ 39). “[B]y taking advantage of the TMS32010 features, a designer can implement a direct form FIR filter, optimized for execution time, data memory, or program memory.” (Ex. 1006 at 11). As a result, a POSITA would have been motivated to use a programmable DSP of TI App Note to implement the adaptive filter of Thomson more efficiently, for example reduce execution time, memory requirements, and other resource demands. (Ex. 1009, ¶ 39). Such a combination was within the skill of the art at the time and would have yielded predictable results, and therefore

would have been obvious to a POSITA. (*Id.*). For at least these reasons, the combination of Thomson and TI App Note renders claim 1 obvious. (*Id.*).

**H. Ground 2: Claims 2, 4, 10, 11, and 26 are obvious over Thomson in view of TI App Note.**

As described above in Section V(G), independent claim 1 is obvious over Thomson in view of TI App Note. (*See* Sec. V(G), *supra.*) As also described above in Sections V(B)–V(F), the additional limitations recited in dependent claims 2, 4, 10, 11, and 26 are also taught by Thomson. Accordingly, combining Thomson and TI App Note renders these claims obvious for the same reasons. (Ex. 1009, ¶ 40).

**I. Ground 3: Claim 3 is obvious over Thomson and Harris in further view of Gunter or, in the alternative, Thomson and TI App Note in further view of Gunter.**

“3. The television receiver of claim 1, wherein the television receiver is formed as a monolithic integrated circuit.”

Gunter (Ex. 1022) discloses frequency conversions of television signals from RF to baseband that can be implemented on a monolithic IC. (Ex. 1022, Abstract, 2:10–17, claim 1; Ex. 1009, ¶ 41). The desirability of integrating television receiver functions was well known in the art at the time of the invention, and indeed before the filing of the ‘792 patent application, digital television receivers embodied on a monolithic IC already existed. (Ex. 1009, ¶ 41 (citing Ex. 1021, 4:2–5, 3:50–55 (digital TV receiver embodied as a monolithic IC) and Ex.

1020, 2:38–41, Fig. 1 (electronic tuner for receiving and decoding digital terrestrial or cable television signals, wherein devices for receiving television signals, converting intermediate signals, filtering baseband signals, and converting baseband signals from analog-to-digital are all implemented on a single monolithic substrate.)). Moreover, monolithic tuners were well known in the art and had a reasonable expectation of success in the television tuner art. (Ex. 1009, ¶ 41).

A POSITA at the time of the patent would have been motivated to reduce the tuner of Thomson and Harris or Thomson and TI App onto a single monolithic IC in order to save printed circuit board space and reduce parasitic effects, as was well known at the time. (Ex. 1009, ¶ 42). A person of ordinary skill in the art would have considered many engineering and design factors, including time, space, and monetary considerations. (Ex. 1009, ¶ 42). For example, a POSITA would have been motivated to reduce the size of the receiver as much as possible to allow more functionality to be implemented by a particular element. Moreover, a reduced size element provides cost and manufacturing advantages. (Ex. 1009, ¶ 42). In addition, integrated multiple functional units onto a single integrated circuit reduces parasitic effects, thereby allowing the circuit to operate at a higher frequency with less delay. (Ex. 1009, ¶ 42). Accordingly, in a system wherein television signals are processed according to the combination of Thomson and Harris or Thomson and TI App Note, a POSITA would have been motivated to

implement the receiver as a single monolithic circuit to save physical space on a device and reduce manufacturing or sourcing costs by reducing the number of devices in an apparatus incorporating the receiver. (Ex. 1009, ¶ 42). Indeed the motivation here echoes the motivations that have driven designers and even the well-known Moore’s Law since the invention of the integrated circuit. (*Id.*). For at least these reasons, the combination of Thomson and Harris with Gunter or, in the alternative Thomson and TI App Note with Gunter renders claim 3 obvious.

**J. Ground 4: Claim 5 is obvious over Thomson and Harris in further view of Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Cirrus Logic.**

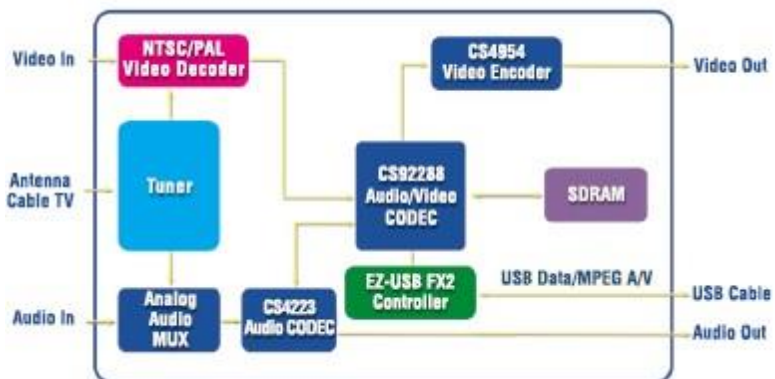
“5. The television receiver of claim 4, further comprising: a first decoder circuit coupled to decode the video baseband signal for providing video display signals corresponding to the analog television format; and a second decoder circuit coupled to decode the audio baseband signal for providing audio signals corresponding to the analog television format.”

A television receiver functions to receive television signals, process those signals according to the format and/or standard of the received signal, and output those signals to the input format required by the display device. (Ex. 1009, ¶ 43). Merely designing a decoder circuit to process video and audio signals according to a known analog television format was well known in the prior art so processing (or decoding) the data into known analog audio and video television formats (such as

PAL/NTSC/SECAM) was within the skill of a POSITA. (Ex. 1001, 1:52–2:3 (NTSC, PAL, and SECAM formats known in the prior art); Ex. 1009, ¶ 43).

Cirrus Logic (Ex. 1015) describes the Cirrus Logic product CS92288 as a real-time “audio/video encoder/decoder (CODEC)”. The CS92288 CODEC is further described in a USB-DVR 2.0 reference design.

(Ex. 1015, p. 4 (right)). The CS92288 MPEG-2 CODEC is a “single chip, real-time



MPEG audio/video encoder/decoder featuring a programmable system mux/demux that encodes/decodes VCD, SVCD, and DVD bitstreams with frame accurate lip

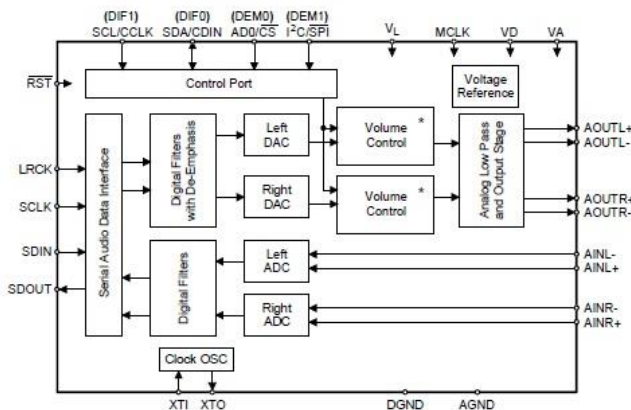
sync.” (*Id.*). The USB-DVR 2.0

design further includes an Audio CODEC CS4223 (Datasheet Ex.

1016 (left)). The CS4223 circuitry outputs audio at baseband at

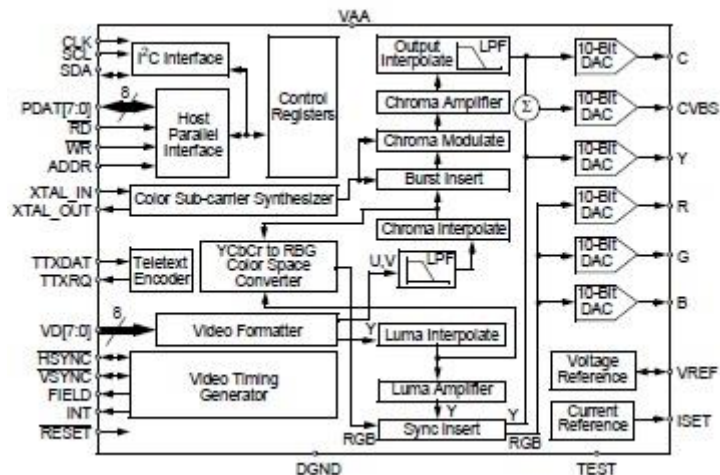
differential outputs AOUTL+/- and

AOUTR+/- representing differential outputs of the left and right audio channels, respectively, and thus correspond to audio signals corresponding to the analog television format. (*Id.*, Ex. 1009, ¶ 44).





The USB-DVR 2.0 design further includes CS4954 (Datasheet Ex. 1017), an overview of which appears in the figure at right: (Ex. 1017, p. 1). The CS4954



outputs baseband video signals CVBS and RGB or component YUV video outputs. (*Id.* at 1, 12; Ex. 1009, ¶ 45). The CVBS, RGB, and YUV outputs correspond to video signals in the analog television format. (*Id.*). Moreover, both the CS4954 and CS92288 are compliant with NTSC and PAL analog video standards. (Ex. 1017 at 1; Ex. 1009, ¶ 45). For at least these reasons, Thomson and Harris in further view of Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Cirrus Logic teach the elements of claim 5. (Ex. 1009, ¶ 45).

A person of ordinary skill in the art at the time of the patent would have been motivated to combine the teachings of Thomson and Harris or Thomson and TI App Note with the circuits of Cirrus Logic. (Ex. 1009, ¶ 46). In any system wherein television signals are processed according to the combination of Thomson and Harris or Thomson and TI App Note, a POSITA would have used decoder circuits to process the audio and video components of a received TV signal into baseband signals so that the baseband signals can be used by any standard display

device to output moving pictures for a human audience and by any standard audio playback device to produce corresponding sounds that can be heard by a human audience. (Ex. 1009, ¶ 46). Moreover, Cirrus Logic can be used in conjunction with digital and analog television signals. (Ex. 1009, ¶ 46; Ex. 1017 at 1 (“The CS4954/5 provides full conversion from digital video formats . . . or . . . analog video.”); Ex. 1016 at p. 1 (“audio codec providing stereo analog-to-digital and stereo digital-to-analog converters”)). The circuits in Cirrus Logic output audio channels (AOUTL+/- and AOUTR+/-) and video channels (CVBS and RGB or component YUV video outputs). Cirrus Logic is compatible with received analog (NTSC/PAL-encoded) TV format and digital (MPEG-encoded) TV format. (Ex. 1009, ¶ 46). Therefore it would have been a simple design choice, driven by the particular components selected or required to meet audio and video requirements for the system design, to include the Cirrus Logic circuitry in a receiver system requiring baseband outputs corresponding to video and audio analog signals. (*Id.*). For at least these reasons, the combination of Thomson and Harris with Cirrus Logic or, in the alternative, Thomson and TI App Note with Cirrus Logic renders claim 5 obvious. (Ex. 1009, ¶ 46).

**K. Ground 4: Claim 6 is obvious over Thomson and Harris in further view of Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Cirrus Logic.**

“6. The television receiver of claim 5, wherein the first decoder circuit comprises a PAL/SECAM/NTSC decoder circuit.”

As described above, CS4954 (Ex. 1017) describes an NTSC/PAL video encoder/decoder that outputs video signals at baseband. Further, as discussed above in Section IV(A), the ‘792 patent admits that television receivers capable of receiving multiple different television standards such as NTSC, PAL, and SECAM were “widely adopted” in the art, and therefore was admitted prior art (*E.g.*, Ex. 1001, 1:20–24; *see also* Ex. 1034 at 1:56–59 (describing the well-known NTSC, PAL, and SECAM standards)). Because television receivers supporting NTSC, PAL, and SECAM were not novel, Thomson and Harris in further view of Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Cirrus Logic renders claim 6 obvious. (Ex. 1009, ¶ 47).

**L. Ground 5: Claim 7 is obvious over Thomson and Harris in further view of Kerth or, in the alternative, Thomson and TI App Note in further view of Kerth.**

“7. The television receiver of claim 1, wherein the signal output circuit provides a first output signal and a second output signal corresponding to the digital output signals, the first output signal and the second output signal being differential output signals corresponding to a digital television format.”

As explained in Section V(C) above, Thomson teaches first and second output signals corresponding to digital television signals. (*See also* Ex. 1004 at 1:5; Ex. 1009, ¶ 48).

Digital signals 448 and 451 of Fig. 4 (and 859 and 872, Fig. 8) of Kerth provide differential I and Q components capable of carrying video and audio using a well-known quadrature demodulation technique. (Ex. 1011, 14:58–15:7; Ex. 1009, ¶ 49). Accordingly, Kerth discloses a signal output circuit (e.g., the DAC circuitry 445 in Fig. 4 or 875A and 875B of Fig. 8) that outputs first and second differential output signals (RX-I 448 and RX-Q 451 in Figs. 4 and 8) after processing in an RF receiver. (Ex. 1009, ¶ 49; *see, e.g.*, Ex. 1011, Fig. 8 and 16:16–18 (“The notation “(diff.)” adjacent to signal lines or reference numerals in Fig. 8 denotes the use of differential lines to propagate the annotated signals.”)). For example, digital signals 869 and 872 in Fig. 8 of Kerth provide differential I and Q components capable of carrying video and audio components of a digital TV format using a well-known quadrature demodulation technique. (Ex. 1011, 14:58–15:7; Ex. 1009, ¶ 49). A person of ordinary skill in the art would know that the DAC circuitry in Kerth includes differential output drivers for outputting differential signals. (Ex. 1009, ¶ 49).

A person of ordinary skill in the art at the time of the patent would have been motivated to combine the teaching of Thomson and Harris or Thomson and

TI App Note with the differential outputs disclosed by Kerth. (Ex. 1009, ¶ 50). In the analog realm, there are only two options for output circuits—single ended or differential ended. As explained in Kerth, circuits with differential outputs have improved common mode rejection over single-ended outputs. (*See also* Ex. 1025, p. 1). In addition, as further explained in Kerth, differential outputs help “reduce interference effects among the various circuit partitions or circuit blocks even further.” (Ex. 1011 at 8:19–23). Accordingly, a differential output solution would have been a simple and obvious design choice. (Ex. 1009, ¶ 50). The design of a differential output driver was well known and predictable. The actual design would have been driven by the particular components selected for the differential output circuit. (*Id.* at 50; *see also* Ex. 1001, 6:51–56 (output circuit design may be based on design factors such as desired output format or pin count)). For these reasons, the combination of Thomson and Harris (or, alternatively, Thomson and TI App Note) with Kerth renders this claim obvious. (Ex. 1009, ¶ 50).

**M. Ground 5: Claim 12 is obvious over Thomson and Harris in further view of Kerth or, in the alternative, Thomson and TI App Note in further view of Kerth.**

“12. The television receiver of claim 1, wherein the signal output circuit comprises one or more output terminals, each of the one or more output terminals of the signal output circuit comprises a single-ended output terminal or a differential output terminal”

As discussed in Section V(A)(6) above, Thomson discloses a single-ended signal output circuit. (Section V(A)(6), *supra*; Ex. 1009, ¶ 51). As further discussed in Section V(L) above, Kerth discloses a differential output terminal. For at least these reasons, claim 12 is obvious over the combination of Thomson and Harris (or, alternatively, Thomson and TI App Note) with Kerth.

**N. Ground 6: Claim 13 is obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.**

1. “13. The television receiver of claim 1, wherein the signal output circuit comprises: a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals; a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal”

Oku (Ex. 1018) discloses a television receiver including a first digital-to-analog converter (e.g., ref. 21 in Fig. 4) for receiving processed digital signals and converting to analog output signals. (Ex. 1018, ¶ [0046], Fig. 4; Ex. 1009, ¶ 52). Oku further discloses a first driving circuit (e.g., ref. 22 in Fig. 4) for driving analog output signals from DAC 21 to an output terminal. (Ex. 1018 at ¶¶ [0046] and [0066]; Ex. 1009, ¶ 52).

2. “a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a second output

terminal; a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals”

Oku discloses a second driver circuit (e.g. ref. 26 of Fig. 4) for driving the analog output signals from DAC 21. Oku also discloses a second DAC 16 driving circuit 17. Oku discloses many different embodiments of output circuitry including multiple driver circuits, e.g. in Figs. 1, 4, 6, 7, 9–11. As discussed in Section V(L) above, Kerth discloses first and second outputs (refs. 448 and 451) from a DAC (ref. 445), where the first and second outputs represent I and Q signal components using a well-known quadrature demodulation technique. (Ex. 1011, 14:58–15:7; Ex. 1009, ¶ 54). It would have been obvious to one of ordinary skill in the art to combine the teachings of Kerth and Oku for any receiver where multiple outputs from a DAC was desired or required. For example, Kerth and Oku could have been combined to yield a receiver that can output two different types of analog signals. Moreover, it was well known in the art for a single signal (e.g., a DAC output) to drive multiple drivers. (Ex. 1009, ¶ 54 (citing Ex. 1024 at Abstract, Fig. 3)). This would have been a simple design choice, well within the skill of the art, driven by the particular components selected. (*Id.* at 54; Ex. 1001, 6:51–56 (output circuit design may be based on design factors such as desired output format or pin count)). (Ex. 1009, ¶ 54).

3. “a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a third output terminal,”

Oku further discloses a third driving circuit (e.g., ref. 17 in Fig. 4) for driving analog output signals to a third output terminal. (Ex. 1018 at ¶¶ [0048] and [0049]; Ex. 1009, ¶ 55).

4. “wherein the first and second output terminals provide signals indicative of video and audio information encoded in the input RF signal and the third output terminal provides signals indicative of audio information encoded in the input RF signal”

As discussed in Section V(N)(3), Oku discloses the third output terminal (e.g., ref. 17 at Fig. 4). Oku further discloses wherein “the analog audio signal is outputted from the speaker 23 through the speaker driving circuit 22.” The analog audio signal of Oku reflects the audio information encoded in the input analog television signal. (Ex. 1018 at ¶¶ [0048] and [0067]).

As discussed in Section V(N)(2) above, Oku discloses wherein the first and second output terminals provide audio and video information. For example, DAC 16 and driving circuit 17 of Oku Fig. 4 output video signals, while DAC 21 and driving circuit 22 of Oku output audio signals. Therefore, Oku discloses first and second output terminals reflecting video and audio information encoded according the input digital signal format. Oku, Thomson, Harris, and TI App Note all address a similar problem, namely a digital receiver for receiving and processing



both analog and digital television signals for display. Accordingly a POSITA would have been motivated to combine these references, and for at least these reasons, the combination of Thomson and Harris (or, alternatively, Thomson and TI App Note) with Oku and Kerth renders this claim obvious. (Ex. 1009, ¶ 57).

**O. Ground 6: Claim 14 is obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.**

1. “14. The television receiver of claim 13, wherein the first driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to an analog television format, the analog output signals being video baseband signals”

Oku discloses wherein the first driver circuit comprises a single-ended driver for driving video baseband signals. (Ex. 1018, Fig. 1 and ¶¶ [0046]–[0048] (graphics data is displayed on monitor 18 after passing through DAC 16 and driving circuit 17)). One of ordinary skill in the art would know that the output signals are at baseband for purposes of displaying in a human-viewable form at monitor 18. (Ex. 1009, ¶ 58). Additionally, Kerth discloses the use of a single-ended driver. (Ex. 1011 at 8:57–58 (“Moreover the signals may constitute single-ended or differential signals, as desired.”)).

2. “the third driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to the analog television format, the analog output signals being audio baseband signals.”

As discussed in Sections V(N)(3)–(4), Oku discloses the third output terminal wherein “the analog audio signal is outputted from the speaker 23 through the speaker driving circuit 22.” (Sections V(N)(3)–(4), *supra*; Ex. 1009, ¶ 49). One of ordinary skill in the art would know that the output signals are at baseband for purposes of playing through speaker 23. (Ex. 1009, ¶ 49). Moreover, Oku discloses, among others, the use of analog television format. (*See, e.g.*, Ex. 1018 at [0016]). Additionally, Kerth discloses the use of a single-ended driver. *Kerth* at 8:57–58 (“[S]ignals may constitute single-ended or differential signals, as desired.”)

**P. Ground 6: Claim 15 is obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.**

1. “15. The television receiver of claim 13, wherein the second driver circuit comprises a differential output driver circuit for driving analog output signals corresponding to a digital television format, the analog output signals being DTV low-IF signals,”

As discussed above in Section V(N)(2), Kerth discloses wherein the second driver circuit comprises a differential output driver circuit. (Ex. 1009, ¶ 60). Oku further discloses that the output signals are digital format corresponding to analog input format. (*See, e.g.*, Ex. 1018 at [0002]; Ex. 1009, ¶ 60). One of ordinary skill in the art would understand that the IF frequency is a matter of design choice, and a

low IF was within the skill of the art at the time of invention. (Ex. 1009, ¶ 60; *see also* Ex. 1004 at 2:53–57 (disclosing the down-conversion of a signal by “mixer stage 2” into “an IF signal of around 75 MHz (see Figs. 2d and 2e)).

2. “wherein the second output terminal comprises a first differential output terminal and a second differential output terminal.”

As discussed in Section V(L) above, Kerth discloses first and second differential output terminals (e.g. refs. 448 and 451). (Section V(L), *supra*; Ex. 1009, ¶ 61; *see, e.g.*, Ex. 1011, Fig. 8 and 16:16–18 (“The notation “(diff.)” adjacent to signal lines or reference numerals in Fig. 8 denotes the use of differential lines to propagate the annotated signals.”)).

**Q. Ground 6: Claim 16 is obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.**

“16. The television receiver of claim 13, wherein the signal output circuit further comprises: a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function.”

Thomson discloses low-pass filtering of output signals using low-pass filters (refs. 14 and 15 for Q/I and ref. 10 for CVBS). (Ex. 1004 at Fig. 1, 2:37–44; Ex. 1009, ¶ 62). Additionally, it would be obvious to one of ordinary skill in the art to provide low-pass filtering of a baseband signal for attenuation of unwanted frequencies being output by baseband audio and video signal outputs. (Ex. 1009, ¶

62). A low-pass filter smoothes out waveforms and reduces or eliminates high-frequency noise which may be introduced by the electronic circuitry including the DAC. Moreover, a low-pass filter reduces additional error introduced by coupling a DAC simultaneously to two driver circuits. (Ex. 1009, ¶ 62).

**R. Ground 6: Claim 17 is obvious over Thomson and Harris in further view of Oku and Kerth or, in the alternative, Thomson and TI App Note in further view of Oku and Kerth.**

“17. The television receiver of claim 13, wherein the signal output circuit further comprises: a low pass filter coupled between the second digital-to-analog converter and the third driver circuit, the low pass filter providing low pass filtering function.”

As discussed above in Section V(Q), Thomson discloses low-pass filtering of output signals using low-pass filters (refs. 14 and 15 for Q/I and ref. 10 for CVBS). (Ex. 1004 at Fig. 1, 2:37–44; Ex. 1009, ¶ 63). Additionally, it would be obvious to one of ordinary skill in the art to provide low-pass filtering of a baseband signal for attenuation of unwanted frequencies being output by baseband audio and video signal outputs. (Ex. 1009, ¶ 63). A low-pass filter smoothes out waveforms and reduces or eliminates high-frequency noise which may be introduced by the electronic circuitry including the DAC.

**S. Ground 7: Claim 8 is obvious over Thomson and Harris in further view of Kerth and Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Kerth and Cirrus Logic.**

1. “8. The television receiver of claim 7, further comprising: a demodulator circuit for demodulating the first output signal and the second output signal according to the television signal format of the input RF signal, the demodulator circuit generating video and audio baseband signals corresponding to the format of the input RF signal;”

As described above in Section V(A)(6), Thomson discloses an output circuit including a demodulator generating audio and video baseband signals corresponding to the format of the input RF signal. For at least these reasons, Thomson teaches this element. (Ex. 1009, ¶ 64).

2. “a decoder circuit coupled to decode the video and audio baseband signals for providing video and audio display signals corresponding to the digital television format.”

As discussed above in Section V(J), Cirrus Logic describes circuits to decode for video and audio baseband signals corresponding to a digital format input signal. (See Section V(J), *supra*; Ex. 1009, ¶ 65). The CS4954 video chip provides the video output signals and the CS4223 chip provides analog audio signals. One of ordinary skill in the art would have been motivated to use the CS4954 and CS4223 circuits of Cirrus Logic to process various formats of

television to baseband. A POSITA would know that digital satellite TV signals as (discussed in Thomson) would be encoded using MPEG, and therefore would be motivated to combine Thomson (or other references disclosing digital TV) with MPEG circuitry such as Cirrus Logic. (Ex. 1009, ¶ 65). Moreover, Cirrus Logic is compatible with a receiver for digital television signal format. (Ex. 1009, ¶ 65). Accordingly, one of ordinary skill in the art would have been motivated to combine the teachings of Thomson, Harris, and Kerth (or Thomson, TI App Note, and Kerth) with the disclosures of Cirrus Logic to decode and provide video and audio signals corresponding to a digital format input signal. (Ex. 1009, ¶ 65)

It would have been a simple design choice, well within the skill of the art, driven by the particular components selected or required for the system design, to include the Cirrus Logic circuitry in a receiver system requiring baseband outputs corresponding to video and audio analog signals. (Ex. 1009, ¶ 66). In designing systems wherein television signals are processed according to the combination of Thomson and Harris or Thomson and TI App Note, a POSITA would have naturally thought to use decoder circuits to process the audio and video signals into baseband signals so that the signals can be used by any standard display device to output moving pictures for a human audience and by any standard audio playback device to produce corresponding sounds that can be heard by a human audience. (Ex. 1009, ¶ 66). Cirrus Logic was compatible with digital format input signals,

and was therefore available for use by a POSITA. Moreover, it is well known that encoding data can reduce the amount of data to be transmitted with little to no loss at the receiving end upon decoding. For at least these reasons, the combination of Thomson and Harris with Kerth and Cirrus Logic or, in the alternative, Thomson and TI App Note with Kerth and Cirrus Logic renders claim 8 obvious. (Ex. 1009, ¶ 66).

**T. Ground 7: Claim 9 is obvious over Thomson and Harris in further view of Kerth and Cirrus Logic or, in the alternative, Thomson and TI App Note in further view of Kerth and Cirrus Logic.**

“9. The television receiver of claim 8, wherein the video and audio baseband signals comprise a MPEG data stream and the decoder circuit comprises a MPEG decoder circuit”

As discussed above in Section V(J), Cirrus Logic describes a single-chip MPEG processor circuit to decode video and audio baseband signals corresponding to a digital format input signal. (See Section V(J), *supra*; Ex. 1009, ¶ 67). Further, the ‘792 patent disclosure admits as prior art a television receiver incorporating a digital demodulator “output[ting] data in a MPEG data stream.” (Ex. 1001, 2:2–3; Ex. 1009, ¶ 67).

One of ordinary skill in the art would have been motivated at the time of patent to combine the teachings of Thomson, Harris, and Kerth (or Thomson, TI App Note, and Kerth) with the disclosures of Cirrus Logic to implement a receiver

compatible with data encoded in a MPEG streaming format. (Ex. 1009, ¶ 68; *see* Sections V(J) and V(S)). The result of such a combination would have been well within the skill of one of ordinary skill in the art and would have produced predictable results. (*Id.* at 68). Not only did the digital demodulator of the admitted prior art output MPEG data streams, ('792 pat. at 2:2–3), but also the details of MPEG decoders were well known to one of ordinary skill in the art, for example, as discussed in Cirrus Logic. Therefore the combination of Thomson and Harris with Kerth and Cirrus Logic or, in the alternative, Thomson and TI App Note with Kerth and Cirrus Logic renders claim 9 obvious. (Ex. 1009, ¶ 68).

**U. Ground 8: Claims 26 and 27 are obvious over Thomson and Harris in further view of Balaban or, in the alternative Thomson and TI App Note in further view of Balaban.**

“27. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user.”

Thomson discloses a “bandpass filter 8 . . . with an adaptively controlled bandwidth [that] selects the desired signal” based on a “Television Standard” input signal. (Ex. 1004 at 3:16–25; Fig. 1). This “Television Standard” signal, as the name implies, indicates the format of the incoming television signal (i.e., analog or digital TV). (*Id.*). A POSITA would understand Thomson as disclosing a standard or format selection circuit that generates this “Television Standard” based on the standard or format of the received television signal. (Ex. 1009, ¶ 69). However,



Thomson is silent as to the implementation details of that signal selection circuit. One skilled in the art would understand that a circuit would need to be constructed to indicate the format of the incoming signal. (*Id.*). Balaban describes such an implementation, wherein the circuit would decode and detect the incoming format responsive to a user selection or use a look-up table for the channel. (Ex. 1008, 7:66–8:5, 12:16–28), or a combination of the two. (*Id.*).

Balaban is directed to the same problem as the ‘792 patent, namely providing a generic receiver for different television standards. As such, one skilled in the art would have naturally looked to Balaban concerning the implementation of the particular “Television Standard” selection circuit disclosed in Thomson. (Ex. 1009, ¶ 70). It would have been obvious to one of ordinary skill in the art to allow a user to manually select one of these standards using either the remote control or a physical button on the television itself, as taught by Balaban. (Ex. 1009, ¶ 70). Balaban discloses a television receiver capable of “provid[ing] a user-selectable default condition such as by a simple switch or through a programming feature” corresponding, e.g. to a selection of NTSC or ATSC signal formats. (Ex. 1008, 7:66–8:5). It would have been obvious to a POSITA to use the Balaban manual selection circuit in the standard selection circuit of Thomson to generate the “Television Standard.” (Ex. 1009, ¶ 70; *see also* Ex. 1036, 13:37–45). For at least these reasons, this claim is obvious. (*Id.*).

**V. Ground 9: Claim 1 is anticipated by Patel.**

1. Preamble

Under the broadest reasonable interpretation, Petitioner does not believe that the preamble of claim 1 is limiting. Even assuming it is, however, Patel clearly describes the claimed “television receiver.” (Ex. 1023 at 1:11–12 (“The present invention relates to receivers for digital television (DTV) signals”); *Id* at 4:23–24 (“digital television signal receiver embodying the invention”); Fig. 9). Patel teaches this limitation (Ex. 1009, ¶ 71).

2. “a frequency conversion circuit”

Patel discloses a “front-end” electronics circuit 11 that converts “radio-frequency television signals to intermediate-frequency television signals, supplied as input signal to an intermediate-frequency (IF) amplifier chain 12 for vestigial-sideband DTV signals,” (Ex. 1023 at 5:7–12). Patel teaches this limitation. (Ex. 1009, ¶ 72).

- a. “for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF)”

As discussed previously, the front-end electronics circuit 11 converts “radio-frequency television signals to intermediate-frequency television signals as an input signal to an intermediate-frequency (IF) amplifier chain 12 for vestigial-sideband DTV signals,” and therefore meets this limitation. (Ex. 1023 at 5:7–12; Ex. 1009, ¶ 73).

- b. “the input RF signal encoding information in one of a plurality of television signal formats”

The digital television receiver in Patel receives digital television signals according to the ATSC standard (Ex. 1023 at 1:11–17; 6:32–41) and also analog television signals (*Id.* at 3:34–36). Thus, Patel discloses receiving both digital and analog television signal formats. (Ex. 1009, ¶ 74).

3. “an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof”

“The final IF output signals from the IF amplifier chain 12 are digitized by the ADC 13” to generate digital signals for further processing. Therefore, Patel meets this limitation. (Ex. 1023 at 5:44–45; Ex. 1009, ¶ 75).

4. “a signal processor for”

Patel discloses an equalizer circuit which as a signal processor. “The equalizer circuitry 14 shown in Figs. 1–9 can be constructed in integrated circuit form as a multiple-tap finite-impulse-response digital filter used for amplitude-and-group-delay equalization, the tap weights of which FIR filter are programmable.” (Ex. 1023 at 6:1–5; Fig. 9) The equalizer includes a processing element. (*Id.* at 15:51–54 (“The equalizer 14 includes filter coefficient computation apparatus 140 for computing updated weighting coefficients for the adaptive filtering in the equalizer 14.”)). Accordingly, the analog-to-digital converter of Patel meets this element. (Ex. 1009, ¶ 76).

5. “processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate frequency signal, each of the plurality of finite impulse response filters corresponding to a format of the input RF signal”

As discussed above, the equalizer is a “multiple-tap finite-impulse-response digital filter” that performs “ghost-cancellation and equalization to reduce the number of taps in the kernel of the filter used for final amplitude-and-group-delay equalization after ghost-cancellation is carried out by cascaded sparse-kernel filters of finite-and infinite-impulse response types.” (Ex. 1023 at 6:6–25.) The FIR filter 141 suppresses “near ghosts and also helps suppress pre-ghosts, multipath responses that are received earlier than the principal DTV signal is received.” (*Id.* at 15:56–60). Moreover, the FIR filter response is “processed to reduce the effects of artifacts of co-channel NTSC interference in the I-channel baseband signal.” (*Id.* at 6:15–20). The FIR filters in the equalizer are tuned both received analog and digital television signals. (*Id.* at 2:59–61; Ex. 1009, ¶ 77). Accordingly, this element is disclosed by the equalizer of Patel. (Ex. 1009, ¶ 77).

6. “a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals.”

The complex demodulator for NTSC Video 46 and the complex demodulator for DTV signal 15 receive the output from the equalizer. (*E.g.*, Ex. 1023 at Fig. 9). The output of the equalizer is passed to a complex demodulator 15 to recover the I-channel baseband signal for the DTV signal. (*Id.* at 5:46–51 (the complex demodulator 15 “demodulates the equalized vestigial-sideband amplitude-modulation DTV signal in the final intermediate-frequency band to recover an I-channel baseband signal by digital in-phase synchronous detection and a Q-channel baseband signal by digital quadrature-phase synchronous detection.”)). The output of the equalizer is also passed to a complex demodulator 46 to recover the I-channel baseband signal for any NTSC co-channel reception. (*Id.* at 12:1–11) (the output of the equalizer is “supplied to a complex demodulator 46 that demodulates the equalized vestigial-sideband amplitude-modulation NTSC signal in the final intermediate-frequency band to recovery an I-channel baseband video signal by digital in-phase synchronous detection and a Q-channel baseband video signal by digital quadrature-phase synchronous detection.”) Therefore complex demodulator for NTSC Video 46 and complex demodulator for DTV signal 15 meet this limitation. (Ex. 1009, ¶ 78).

## W. Summary Claim Charts for Challenged Claims

A summary listing of further disclosures of Thomson, Harris, TI App Note, Kerth, Balaban, and the Declaration of Douglas Holberg relevant to the claim elements at issue in this Petition appears in the claim charts below. A detailed listing is also provided in the Holberg Declaration, Ex 1009.

| <b>Claim Chart of United States Patent No. 7,265,792</b>                                                                                           |                                                                                                                                             |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| <b>United States Patent No. 7,265,792</b>                                                                                                          | <b>Television Receiver for Digital and Analog Television Signals</b>                                                                        |
| 1. A Television receiver comprising:                                                                                                               | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 1:3–4, 1:55–2:19; Ex. 1009, ¶ 16.<br><b>Ground 9:</b> Ex. 1023, 1:11–12; Ex. 1009, ¶ 71.                |
| a frequency conversion circuit                                                                                                                     | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 2:30–33; Ex. 1009, ¶ 17.<br><b>Ground 9:</b> Ex. 1023, 5:7–12; Ex. 1009, ¶ 72.                          |
| for receiving an input RF signal and for converting the input RF signal to an intermediate frequency signal having an intermediate frequency (IF), | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 1:55–60, 2:17–19, 2:53–57; Ex. 1009, ¶ 18.<br><b>Ground 9:</b> Ex. 1023, 5:7–12; Ex. 1009, ¶ 73.        |
| the input RF signal encoding information in one of a plurality of television signal formats;                                                       | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 1:30, 1:42–43; Ex. 1009, ¶ 19.<br><b>Ground 9:</b> Ex. 1023, 1:11–17, 6:32–41, 6:17–19; Ex. 1009, ¶ 74. |
| an analog-to-digital converter for sampling the intermediate frequency signal and generating a digital representation thereof;                     | <b>Grounds 1 &amp; 2:</b> Ex. 1004, Fig. 1, 1:47, 4:14–16; Ex. 1009, ¶ 20.<br><b>Ground 9:</b> Ex. 1023, 5:44–                              |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 45; Ex. 1009, ¶ 75.                                                                                                                                                                                                                                               |
| a signal processor for                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | <p><b>Ground 1:</b> Ex. 1004, Fig. 1, 3:16–25; Ex. 1005, pp. 3, 5; Ex. 1009, ¶¶ 21–23.</p> <p><b>Ground 2:</b> Ex. 1004, Fig. 1, 3:16–25; Ex. 1006, pp. 7, 11; Ex. 1009, ¶¶ 37–39.</p> <p><b>Ground 9:</b> Ex. 1023, 6:1–5, Fig. 9, 15:51–54; Ex. 1009, ¶ 76.</p> |
| processing the digital representation of the intermediate frequency signal in accordance with the television signal format of the input RF signal, the signal processor generating digital output signals indicative of information encoded in the input RF signal, wherein the signal processor applies one of a plurality of finite impulse response filters to the digital representation of the intermediate frequency signal, each of the plurality of finite impulse response [filters] corresponding to a format of the input RF signal; and | <p><b>Ground 1:</b> Ex. 1004, Figs. 1 and 2, 3:16–19; Ex. 1005, p. 4; Ex. 1009, ¶¶ 24–28.</p> <p><b>Ground 2:</b> Ex. 1004, Figs. 1 and 2, 3:16–19; Ex. 1009, ¶¶ 37–39.</p> <p><b>Ground 9:</b> 6:6–25; 15:56–60; 6:15–20; Ex. 1009, ¶ 77.</p>                    |
| a signal output circuit for receiving the digital output signals from the signal processor and for providing one or more output signals corresponding to the digital output signals.                                                                                                                                                                                                                                                                                                                                                                | <p><b>Grounds 1 &amp; 2:</b> Ex. 1004, 4:10–11, 3:19–21, 2:41–44; Ex. 1009, ¶¶ 29–30.</p> <p><b>Ground 9:</b> Ex. 1023, Fig. 9, 5:46–51, 12:1–11; Ex. 1009, ¶ 78.</p>                                                                                             |
| 2. The television receiver of claim 1, wherein the plurality of television signal formats comprises an analog television format and a digital television format.                                                                                                                                                                                                                                                                                                                                                                                    | <b>Grounds 1 &amp; 2:</b> Ex. 1004, Figs. 1 and 2, 3:16–19; Ex. 1004, 1:42–43, 1:24–28; Ex. 1009, ¶¶ 31, 40.                                                                                                                                                      |
| 3. The television receiver of claim 1, wherein the television receiver is formed as a monolithic integrated circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                | <b>Ground 3:</b> Ex. 1020, 2:38–41; Ex. 1009, ¶¶ 41–42.                                                                                                                                                                                                           |
| 4. The television receiver of claim 1, wherein the signal output circuit provides a first output signal being a video baseband signal corresponding to an analog television format and a second output signal being an audio baseband signal corresponding to                                                                                                                                                                                                                                                                                       | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 3:19–22; Ex. 1009, ¶¶ 32, 40.                                                                                                                                                                                                 |

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| the analog television format.                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                 |
| 5. The television receiver of claim 4, further comprising: a first decoder circuit coupled to decode the video baseband signal for providing video display signals corresponding to the analog television format; and a second decoder circuit coupled to decode the audio baseband signal for providing audio signals corresponding to the analog television format. | <b>Ground 4:</b> Ex. 1015, p. 4; Ex. 1016, p. 1; Ex. 1017, pp. 1, 12; Ex. 1009, ¶¶ 43–46.                                       |
| 6. The television receiver of claim 5, wherein the first decoder circuit comprises a PAL/SECAM/NTSC decoder circuit.                                                                                                                                                                                                                                                  | <b>Ground 4:</b> Ex. 1017, p. 1; Ex. 1001, 1:20–24 (admitted prior art); Ex. 1009, ¶ 47.                                        |
| 7. The television receiver of claim 1, wherein the signal output circuit provides a first output signal and a second output signal corresponding to the digital output signals, the first output signal and the second output signal being differential output signals corresponding to a digital television format.                                                  | <b>Ground 5:</b> Ex. 1004, 3:19–22, 1:5; Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1009, ¶¶ 48–50.                |
| 8. The television receiver of claim 7, further comprising: a demodulator circuit for demodulating the first output signal and the second output signal according to the television signal format of the input RF signal, the demodulator circuit generating video and audio baseband signals corresponding to the format of the input RF signal; and                  | <b>Ground 7:</b> Ex. 1004, 4:10–11, 3:19–21, 2:41–44; Ex. 1009, ¶ 64.                                                           |
| a decoder circuit coupled to decode the video and audio baseband signals for providing video and audio display signals corresponding to the digital television format.                                                                                                                                                                                                | <b>Ground 7:</b> Ex. 1015, p. 4; Ex. 1016, p. 1; Ex. 1017, pp. 1, 12; Ex. 1009, ¶¶ 65–66.                                       |
| 9. The television receiver of claim 8, wherein the video and audio baseband signals comprise a MPEG data stream and the decoder circuit comprises a MPEG decoder circuit.                                                                                                                                                                                             | <b>Ground 7:</b> Ex. 1015, p. 4; Ex. 1016, p. 1; Ex. 1017, pp. 1, 12; Ex. 1001, 2:2–3 (admitted prior art); Ex. 1009, ¶¶ 67–68. |
| 10. The television receiver of claim 1, further comprising: a bandpass filter coupled to receive the intermediate frequency signal from the frequency                                                                                                                                                                                                                 | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 2:47–57, 2:57–3:3; Ex. 1009, ¶¶ 33, 40.                                                     |



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| conversion circuit and generate a filtered intermediate frequency signal; and a variable gain amplifier coupled to receive the filtered intermediate frequency signal and provide the amplified, filtered intermediate frequency signal to the analog-to-digital converter.                                                                                                                         |                                                                                                                                       |
| 11. The television receiver of claim 1, wherein the signal output circuit provides output signals in an analog or a digital signal format.                                                                                                                                                                                                                                                          | <b>Grounds 1 &amp; 2:</b> Ex. 1004, 4:10–11; Ex. 1009, ¶¶ 34, 40.                                                                     |
| 12. The television receiver of claim 1, wherein the signal output circuit comprises one or more output terminals, each of the one or more output terminals of the signal output circuit comprises a single-ended output terminal or a differential output terminal.                                                                                                                                 | <b>Ground 5:</b> Ex. 1004, 4:10–11, 3:19–21, 2:41–44; Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1009, ¶ 51.             |
| 13. The television receiver of claim 1, wherein the signal output circuit comprises: a first digital-to-analog converter coupled to receive digital output signals from the signal processor and convert the digital output signals to analog output signals; a first driver circuit for driving the analog output signals from the first digital-to-analog converter onto a first output terminal; | <b>Ground 6:</b> Ex. 1018, Fig. 1, ¶¶ [0046], [0066]; Ex. 1009, ¶ 52.                                                                 |
| a second driver circuit for driving the analog output signals from the first digital-to-analog converter onto a second output terminal; a second digital-to-analog converter coupled to receive digital output signals from the signal processor encoding audio information and convert the digital output signals to analog output signals; and                                                    | <b>Ground 6:</b> Ex. 1018, Figs. 1, 4, 6, 7, 9–11; Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1009, ¶¶ 53–54.            |
| a third driver circuit for driving the analog output signals from the second digital-to-analog converter onto a third output terminal,                                                                                                                                                                                                                                                              | <b>Ground 6:</b> Ex. 1018, Fig. 1 (ref 22), ¶¶ [0048]–[0049]; Ex. 1009, ¶ 55.                                                         |
| wherein the first and second output terminals provide signals indicative of video and audio information encoded in the input RF signal and the third output terminal provides signals indicative of audio information encoded in the input RF signal.                                                                                                                                               | <b>Ground 6:</b> Ex. 1018, Fig. 1 (ref 22), ¶¶ [0048]–[0049]; Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1009, ¶¶ 56–57. |
| 14. The television receiver of claim 13, wherein the                                                                                                                                                                                                                                                                                                                                                | <b>Ground 6:</b> Ex. 1018, Fig. 1,                                                                                                    |

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| first driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to an analog television format, the analog output signals being video baseband signals; and                                                                   | ¶¶ [0046]–[0049]; Ex. 1011, 8:57–58; Ex. 1009, ¶ 58.                                                     |
| the third driver circuit comprises a single-ended driver circuit for driving analog output signals corresponding to the analog television format, the analog output signals being audio baseband signals.                                                                  | <b>Ground 6:</b> Ex. 1018, Fig. 1, ¶¶ [0046]–[0049], [0016]; Ex. 1011, 8:57–58; Ex. 1009, ¶ 59.          |
| 15. The television receiver of claim 13, wherein the second driver circuit comprises a differential output driver circuit for driving analog output signals corresponding to a digital television format, the analog output signals being DTV low-IF signals, and          | <b>Ground 6:</b> Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1018, ¶ [0002]; Ex. 1009, ¶ 60. |
| wherein the second output terminal comprises a first differential output terminal and a second differential output terminal.                                                                                                                                               | <b>Ground 6:</b> Ex. 1011, Figs 4, 8, 14:58–15:7, 16:16–18, 8:19–23; Ex. 1009, ¶ 61.                     |
| 16. The television receiver of claim 13, wherein the signal output circuit further comprises: a low pass filter coupled between the first digital-to-analog converter and the first and second driver circuits, the low pass filter providing low pass filtering function. | <b>Ground 6:</b> Ex. 1004, Fig. 1 (refs. 14, 15), 2:37–44; Ex. 1009, ¶ 62.                               |
| 17. The television receiver of claim 13, wherein the signal output circuit further comprises: a low pass filter coupled between the second digital-to-analog converter and the third driver circuit, the low pass filter providing low pass filtering function.            | <b>Ground 6:</b> Ex. 1004, Fig. 1 (refs. 14, 15), 2:37–44; Ex. 1009, ¶ 63.                               |
| 26. The television receiver of claim 1, further comprising a format/standard selection circuit coupled to the signal processor, the format/standard selection circuit generating a select signal indicative of a format of the input RF signal and                         | <b>Grounds 1 &amp; 2:</b> Ex. 1004, Fig. 1 (“TV Standard” signal); Ex. 1009, ¶¶ 35, 40, 69–70.           |
| the signal processor selecting a finite impulse response filter in response to the select signal.                                                                                                                                                                          | <b>Grounds 1 &amp; 2:</b> Ex. 1004, Fig. 1, 3:16–25; Ex. 1005, pp. 3, 5; Ex. 1009, ¶¶ 36, 40, 69–70.     |

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| 27. The television receiver of claim 26, wherein the format/standard selection circuit generates the select signal in response to an input signal from a user. | <b>Ground 8:</b> Ex. 1004, 3:16–25, Fig. 1; Ex. 1008, 7:66–8:5, 12:16–28; Ex. 1009, ¶¶ 69–70. |
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## VI. CONCLUSION

The combination of Thomson and either Harris or TI App Note render claims 1, 2, 4, 10, 11, and 26 obvious. The addition of Gunter to either the combination of Thomson and Harris or Thomson and TI App note obviates dependent claim 3. The addition of Cirrus Logic to either the combination of Thomson and Harris or Thomson and TI App note obviates dependent claims 5 and 6. The addition of Kerth to either the combination of Thomson and Harris or Thomson and TI App note obviates dependent claims 7 and 12. The addition of Balaban to either the combination of Thomson and Harris or Thomson and TI App Note obviates dependent claim 26. The combination of either Thomson and Harris or Thomson and TI App Note with Oku and Kerth renders dependent claims 13–17 obvious. The combination of either Thomson and Harris or Thomson and TI App Note with Kerth and Cirrus Logic renders dependent claims 8 and 9 obvious. Finally, Patel anticipates claim 1. Petitioner therefore requests institution of an *inter partes* review to cancel claims 1–17, 26, and 27 of the ‘792 patent.

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Respectfully submitted,

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## CERTIFICATE OF SERVICE

The undersigned certifies that on May 23, 2014, I caused a true and correct copy of the following materials:

- PETITION FOR INTER PARTES REVIEW OF 7,075,585 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104
- Exhibits 1001–1036
- Table of Exhibits
- Fee Authorization
- Power of Attorney

to be served via Federal Express on the following attorney of record as listed on PAIR:

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