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18 **SILICON LABORATORIES INC.**

19 UNITED STATES DISTRICT COURT
20 NORTHERN DISTRICT OF CALIFORNIA

21 **SILICON LABORATORIES INC., a**
22 **Delaware Corporation,**

23 Plaintiff,

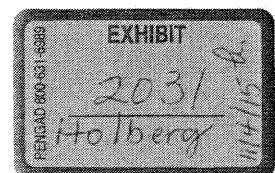
24 v.

25 **CRESTA TECHNOLOGY**
26 **CORPORATION, a Delaware**
27 **Corporation,**

28 Defendant.

Civil Action No. 14-cv-03227-PSG

**REBUTTAL EXPERT REPORT
OF DOUGLAS HOLBERG, PH. D.
REGARDING VALIDITY**



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1. INTRODUCTION

1.1 Qualifications

1. A complete listing of my qualifications including a list of my patents is attached to this report as Appendix A.

2. I am qualified to render opinions on electronics, wireless communications including radio, cellular, and television, televisions tuners, frequency synthesizers, the patents-at-issue, the cited invalidity references, and Cresta's products. As a result of my extensive experience as discussed in more detail below and on my resume, I am well aware of the skill level that a person of ordinary skill in the art of tuning control for high frequency communications signals would have possessed at the time the patents-in-suit were filed. I also am aware of how such a person would have understood the terms used in the patent claims and specifications at the time the patents were filed. The views and opinions I express in this declaration are specifically directed to the understanding such a person would have had in that time period. Except where stated otherwise, I have personal knowledge of the facts and opinions in this declaration and attached exhibits, and if called as a witness, could and would competently testify about these facts and opinions.

3. I have over 35 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when it acquired Cygnal, which I co-founded in 1999. I am a named inventor on 39 U.S. patents. I have held a variety of engineering positions over that time from circuit designer to Director of Engineering and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I earned my M.S.E. and Ph.D. degrees. I am also the co-author of CMOS Analog

1 Circuit Design (now in 3rd edition).

2 **1.3 Person of Ordinary Skill in the Art (POSITA)**

3 4. Through my education, experience, and training in academia and
4 industry, and my analysis of the patents-at-issue, I have considered certain issues
5 from the perspective of a person of ordinary skill in the art. It is my opinion, based
6 upon a review of the file history of the patents-at-issue, that a person of ordinary
7 skill in the art to the patents-at-issue, as of May 29, 1998, the time of the alleged
8 invention of the patents-at-issue ("POSITA") would have held at least a Masters of
9 Science or higher degree in electrical engineering, have at least four years of
10 experience with mixed signal system design, including analog front ends and
11 subsequent digital signal processing of various analog and digital signal formats of
12 video and audio content.

13 5. In determining what would be the level of ordinary skill in the field as
14 of May 29, 1998, considered are the following: (1) The educational level of the
15 inventors. My understanding is that the inventors' education is as follows: David
16 Welland received a Bachelors Degree in Electrical Engineering from the
17 Massachusetts Institute of Technology. Welland deposition 6:21-7:10. Caiyi
18 Wang received a Bachelors Degree in Physics from the East China Normal
19 University in Shanghai, a Masters Degree in Physics from the City University of
20 New York, and a Masters Degree and a Ph.D in Applied Physics from Columbia
21 University. Wang deposition 13:22-16:21.

22 6. (2) The type of problems encountered in the art. Electrical engineering
23 and RF frequency tuning problems generally involve choices in design. There are
24 often numerous ways to address RF frequency tuning problems that achieve the
25 same result. The design choices can include everything from physical structure, to
26 algorithmic choices, to implementation details.

27 7. (3) The prior art solutions to those problems. The principal prior art
28 asserted in the Murgulescu report involves RF frequency tuning solutions.

1 8. (4) The sophistication of the technology. Developing RF frequency
2 tuning solutions is a moderately sophisticated technology.

3 9. (5) The educational level of workers in the field. Workers in the field
4 generally have a Bachelor's degree or higher in electrical engineering. Most would
5 have acquired a significant portion of their knowledge through hands on
6 experience.

7 **1.4 Assignment**

8 10. I have been retained by Silicon Labs as an expert in this action. I have
9 reviewed the patents-at-issue. I am thoroughly familiar with the purported
10 inventions disclosed and claimed in those patents and the terms used in the claims.
11 I am being compensated at my normal rate of \$400 per hour for my trial preparation
12 work in connection with this matter. My compensation is not dependent in any way
13 on the contents of this report, the substance of any further opinions or testimony
14 that I may provide, or the ultimate outcome of this matter.

15 11. I have been informed and understand that the Defendant's expert
16 witness in this action, Dr. Murgulescu, has alleged that the asserted claims of U.S.
17 Patent Nos. 6,137,372, 6,233,441, 6,304,146, 6,308,055, 6,965,761, and 7,353,011
18 ("the '372, '441, '146, '055, '761, and '011 Patents," respectively, or collectively,
19 "the patents-at-issue"), are invalid. I have been retained to analyze the alleged prior
20 art references to determine whether any of them, singly or in combination,
21 anticipate or make obvious the asserted claims of the patents-at-issue. I have also
22 been asked to offer my opinion on issues relevant to allegations that certain asserted
23 claims are invalid under Section 112 of Title 35 of the United States Code.

24 12. Dr. Murgulescu asserted the invalidity arguments referenced above in
25 Murgulescu's Expert Report on Invalidity ("the Murgulescu Report") dated
26 September 29, 2015. I have reviewed and analyzed the Murgulescu Report and the
27 evidence cited therein as relating to the alleged obviousness, anticipation, and
28 invalidity under Section 112. This report contains my opinions in response to the

1 Murgulescu Report.

2 13. The opinions set forth in this report are based upon my extensive
3 education and experience in the field, my conversations with others in the field, and
4 my review of the materials listed in this report . This includes, but is not limited to,
5 the prior art and other materials referenced by Murgulescu in his report.

6 14. If called to testify at trial, I reserve the right to comment or rely upon
7 the above mentioned information and evidence, the testimony and reports of the
8 Parties' experts and any materials relied upon by such experts, and any other
9 information of record in this matter.

10 15. In addition, demonstrative exhibits may be prepared for my trial
11 testimony based on the documents and information cited in this report, including
12 without limitation the information mentioned above, and my ongoing analysis of
13 the same. The documents and other information cited in this report are examples of
14 the materials that support my opinions but are not intended to be an exhaustive
15 statement of all information relevant to opinions which I may present at trial.

16 16. I may be asked to study new materials as they become available,
17 further review material already available to me, or otherwise continue my efforts.
18 If I am asked to testify at trial, I may study additional materials, documentation,
19 software, and testimony as it becomes available. If I am asked to testify, I may
20 provide demonstrative computer systems, graphic materials, schematics, models,
21 animations, and other expository material. If warranted, I may issue a supplement
22 to this report, including, for example, to address information made available to me
23 after the date of this report or to address any orders the Court may issue concerning
24 the construction of the asserted claims. This report may also be supplemented by
25 deposition and trial testimony.

26 **2. OVERVIEW OF APPLICABLE LEGAL PRINCIPLES**

27 17. I am not an attorney. I have been informed and understand that the
28 following legal principles apply to my analysis of issues relating to validity. This

1 report addresses a number of different validity theories and, in addition to what is
2 set forth in this section, I set forth my understanding of the law relevant to some of
3 those theories in the context of my analysis of those theories.

4 **2.1 Claim Construction**

5 18. Claim construction is a matter of law for the Court. *Markman v.*
6 *Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). “It is a ‘bedrock principle’
7 of patent law that ‘the claims of a patent define the invention to which the patentee
8 is entitled the right to exclude.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed.
9 Cir. 2005).

10 19. I understand that the parties have reached agreed constructions on
11 certain claim terms, and that others are disputed. *See* Patent L.R. 4-3 Joint Claim
12 Construction and Prehearing Statement. The parties’ respective positions on certain
13 claim terms has been briefed, a claim construction hearing has been held, and a
14 claim construction ruling has been issued. In my analysis, I have applied the agreed
15 and ordered constructions. For all other terms, I have used the ordinary meaning of
16 the terms to one skilled in the art. I reserve the right to serve a supplement to this
17 report in the event additional claim construction rulings are issued by the Court.

18 **2.2 Validity**

19 20. I understand that a patent is presumed valid, each claim of a patent is
20 presumed valid independently of the validity of other claims, and to overcome the
21 presumption that patents are valid, clear and convincing evidence is required. 35
22 U.S.C. § 282; *Microsoft Corp. v. i4i Ltd. P’ship*, 131 S. Ct. 2238, 2242 (U.S. 2011);
23 *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1370-71 (Fed. Cir.
24 2003); *Oakley, Inc. v. Sunglass Hut Int’l*, 316 F.3d 1331, 1339 (Fed. Cir. 2003).

25 **2.3 Anticipation**

26 21. I understand that “[a] claim is anticipated only if each and every
27 element as set forth in the claim is found, either expressly or inherently described,
28 in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814

1 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

2 **2.4 Obviousness**

3 22. I understand that obviousness is a question of law, which depends on
4 several underlying factual inquiries. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398,
5 406 (2007). Under § 103, the scope and content of the prior art are to be
6 determined; differences between the prior art and the claims at issue are to be
7 ascertained; and the level of ordinary skill in the pertinent art resolved. Against this
8 background the obviousness or nonobviousness of the subject matter is determined.
9 Such secondary considerations as commercial success, long felt but unsolved needs,
10 failure of others, etc., might be utilized to give light to the circumstances
11 surrounding the origin of the subject matter sought to be patented. *KSR*, 550 U.S.
12 406, quoting *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

13 23. The Supreme Court explained in *KSR*, “[A] patent composed of
14 several elements is not proved obvious merely by demonstrating that each of its
15 elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418.
16 Likewise, a defendant asserting obviousness in view of a combination of references
17 has the burden to show “a reason that would have prompted a person of ordinary
18 skill in the relevant field to combine the elements in the way the claimed new
19 invention does.” *Id.*

20 24. I understand that the Defendant must further show that “such a person
21 would have had a reasonable expectation of success in doing so.” *PharmaStem*
22 *Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

23 25. I understand that these three conclusions (that each of the elements of
24 the claims was in the prior art, that a POSITA had reason to combine the elements
25 as claimed, and that such a POSITA would have had a reasonable expectation of
26 success in doing so) must be established using facts supported by clear and
27 convincing evidence. See *Kao Corp. v. Unilever U.S., Inc.*, 441 F.3d 963, 968
28 (Fed. Cir. 2006). Only then is a *prima facie* case of obviousness established. See

1 *Asahi Glass Co., Ltd. v. Guardian Indus. Corp.*, 813 F. Supp. 2d 602 (D. Del.
2 2011).

3 26. The Supreme Court has emphasized the need to value “common
4 sense” over “rigid preventative rules” in determining whether a motivation to
5 combine existed. *KSR* at 419-20. “[A]ny need or problem known in the field of
6 endeavor at the time of invention and addressed by the patent can provide a reason
7 for combining the elements in the manner claimed.” *Id.* at 420. However, the prior
8 art “must be considered in its entirety, i.e., as a whole, including portions that
9 would lead away from the invention in suit[.]” *Panduit Corp. v. Dennison Mfg.*
10 *Co.*, 810 F.2d 1561, 1568 (Fed. Cir. 1987).

11 27. “[W]hen a patent ‘simply arranges old elements with each performing
12 the same function it had been known to perform’ and yields no more than one
13 would expect from such an arrangement, the combination is obvious.” *KSR*, at
14 1740, quoting *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976). “The opposite
15 conclusion would follow, however, if the prior art indicated that the invention
16 would not have worked for its intended purpose or otherwise taught away from the
17 invention.” *Depuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314,
18 1326 (Fed. Cir. 2009).

19 28. I understand that predictability as discussed in *KSR* encompasses the
20 expectation that prior art elements are capable of being combined, as well as the
21 expectation that the combination would have worked for its intended purpose. An
22 inference that a claimed combination would not have been obvious is especially
23 strong where the prior art’s teachings undermine the very reason being proffered as
24 to why a POSITA would have combined the known elements. *DePuy Spine*, 567
25 F.3d at 1314.

26 **2.5 Prior Art**

27 29. I understand that the eligibility and qualification of prior art is
28 governed by 35 U.S.C. § 102, the relevant version of which states, in full:

- 1 30. "A person shall be entitled to a patent unless –
- 2 31. (a) the invention was known or used by others in this country, or
- 3 patented or described in a printed publication in this or a foreign country, before the
- 4 invention thereof by the applicant for patent, or
- 5 32. (b) the invention was patented or described in a printed publication in
- 6 this or a foreign country or in public use or on sale in this country, more than one
- 7 year prior to the date of the application for patent in the United States, or
- 8 33. (c) he has abandoned the invention, or
- 9 34. (d) the invention was first patented or caused to be patented, or was the
- 10 subject of an inventor's certificate, by the applicant or his legal representatives or
- 11 assigns in a foreign country prior to the date of the application for patent in this
- 12 country on an application for patent or inventor's certificate filed more than twelve
- 13 months before the filing of the application in the United States, or
- 14 35. (e) the invention was described in – (1) an application for patent,
- 15 published under section 122(b), by another filed in the United States before the
- 16 invention by the applicant for patent or (2) a patent granted on an application for
- 17 patent by another filed in the United States before the invention by the applicant for
- 18 patent, except that an international application filed under the treaty defined in
- 19 section 351(a) shall have the effects for the purposes of this subsection of an
- 20 application filed in the United States only if the international application designated
- 21 the United States and was published under Article 21(2) of such treaty in the
- 22 English language; or
- 23 36. (f) he did not himself invent the subject matter sought to be patented,
- 24 or
- 25 37. (g)(1) during the course of an interference conducted under section
- 26 135 or section 291, another inventor involved therein establishes, to the extent
- 27 permitted in section 104, that before such person's invention thereof the invention
- 28 was made by such other inventor and not abandoned, suppressed, or concealed, or

1 (2) before such person's invention thereof, the invention was made in this country
2 by another inventor who had not abandoned, suppressed, or concealed it. In
3 determining priority of invention under this subsection, there shall be considered
4 not only the respective dates of conception and reduction to practice of the
5 invention, but also the reasonable diligence of one who was first to conceive and
6 last to reduce to practice, from a time prior to conception by the other.”

7 38. I understand that part (b) of Section 102 sets out the on-sale bar.
8 “[T]he on-sale bar applies when two conditions are satisfied before the critical date.
9 First, the product must be the subject of a commercial offer for sale.” *Pfaff v. Wells*
10 *Electronics*, 525 U.S. 55, 67 (1998). “Second, the invention must be ready for
11 patenting. That condition may be satisfied in at least two ways: by proof of
12 reduction to practice before the critical date; or by proof that prior to the critical
13 date the inventor had prepared drawings or other descriptions of the invention that
14 were sufficiently specific to enable a person skilled in the art to practice the
15 invention.” *Id.* at 68.

16 39. “It is well settled that prior art under 35 U.S.C. § 102 (b) must
17 sufficiently describe the claimed invention to have placed the public in possession
18 of it. Such possession is effected if one of ordinary skill in the art could have
19 combined the publication’s description of the invention with his own knowledge to
20 make the claimed invention. Accordingly, even if the claimed invention is
21 disclosed in a printed publication, that disclosure will not suffice as prior art if it
22 was not enabling.” *In re Donohue*, 766 F.2d 531, 534 (Fed. Cir. 1985) (internal
23 citations omitted). To establish an on-sale bar, it must be shown that the device
24 sold “fully anticipated the claimed invention or would have rendered the claimed
25 invention obvious by its addition to the prior art.” *Allen Engineering Corp. v.*
26 *Bartell Industries*, 299 F. 3d 1336 (Fed. Cir. 2002). As the text of Section 102(b)
27 makes clear, the relevant sale or public use must have been in the United States.

28 **2.6 Non-analogous art, field of endeavor, and pertinence to the inventor’s**

1 **problem**

2 40. "A reference qualifies as prior art for an obviousness determination
3 under § 103 only when it is analogous to the claimed invention. Two separate tests
4 define the scope of analogous prior art: (1) whether the art is from the same field of
5 endeavor, regardless of the problem addressed and, (2) if the reference is not within
6 the field of the inventor's endeavor, whether the reference still is reasonably
7 pertinent to the particular problem with which the inventor is involved." *In re*
8 *Klein*, 647 F.3d 1343, 1347 (Fed. Cir. 2011).

9 41. "A reference is reasonably pertinent if, even though it may be in a
10 different field from that of the inventor's endeavor, it is one which, because of the
11 matter with which it deals, logically would have commended itself to an inventor's
12 attention in considering his problem." *In re Klein*, 647 F.3d at 1347. A reference
13 relates to the same problem as that addressed by the inventor if the reference
14 disclosure "has the same purpose as the claimed invention." *Id.*

15 42. When determining whether art is analogous, the Federal Circuit has
16 considered the field of endeavor narrowly. *In re Clay*, 966 F.2d 656, 659 (Fed. Cir.
17 1992) (holding that an invention relating to the extraction of crude petroleum was
18 not in the same field of endeavor as an invention relating to the storage of refined
19 petroleum). For example, the Federal Circuit agreed that "an inventor considering
20 the problem of making a nectar feeder with a movable divider to prepare different
21 ratios of sugar and water for different animals would not have been motivated" to
22 consider references with a purpose of separating solid objects, which were outside
23 the field of endeavor because they were devoted, in part, to separating, not mixing.
24 *In re Klein* at 1349-51.

25 43. Another useful example of art recently found to be non-analogous is
26 also in *Klein*. The Federal Circuit agreed that references "directed to containers
27 that facilitate the mixing of two separated substances together" would not have
28 been considered by "an inventor considering the problem of making a nectar feeder

1 with a movable divider to prepare different ratios of sugar and water for different
2 animals.” *In re Klein* at 1352.

3 44. I understand that an expert report on obviousness that attempts to rely
4 upon art outside the field of endeavor but which fails to state why a person of
5 ordinary skill would have found such art reasonably pertinent is inadmissibly
6 conclusory. *See K-Tec, Inc. V. Vita-Mix Corp.*, 729 F. Supp. 2d 1312, 1324 (D.
7 Utah 2010). Basing such a claim on “common knowledge” or the frequency with
8 which an approach was adopted outside the field of endeavor is insufficient. *See Id.*
9 at 1323. An expert report must provide some rational basis to explain why a person
10 of ordinary skill would look to a reference outside the field of endeavor. *See Id.* at
11 1324.

12 **2.7 “Vague prior art” and “Obvious to try”**

13 45. Consistent with *KSR*’s requirement that identified solutions be
14 predictable, “an invention is not obvious to try where vague prior art does not guide
15 an inventor toward a particular solution,” such as “where what was ‘obvious to try’
16 was to explore a new technology or general approach that seemed to be a promising
17 field of experimentation, where the prior art gave only general guidance as to the
18 particular form of the claimed invention or how to achieve it.” *Bayer Schering*
19 *Pharma AG v. Barr Laboratories*, 575 F.3d 1341, 1347 (Fed. Cir. 2009) (citations
20 omitted).

21 **2.8 Conclusory expert reports**

22 46. I understand that “vague and conclusory obviousness testimony,” such
23 as testimony that alleges claims are obvious but which does not offer any
24 motivation for one skilled in the art to combine the cited references in order to
25 practice the claimed method, may be precluded, even after *KSR*. *See Innogenetics*
26 *v. Abbot*, 512 F.3d 1363, 1373-74 (Fed. Cir. 2008).

27 **2.9 Impropriety of isolating claim elements and excerpting prior art**

28 47. I understand that the proper question in an obvious analysis is not

1 whether the difference between the prior art and the claims would be obvious, but
2 whether the claims, as a whole, would be obvious. *MySpace, Inc. v. Graphon*
3 *Corp.*, 2012 U.S. App. LEXIS 4375, 14–15, 101 U.S.P.Q.2D (BNA) 1873 (Fed.
4 Cir. Mar. 2, 2012) “Trial courts analyzing claim limitations should strive to connect
5 those limitations to the context of the claim as a whole Such a step may seem
6 a bit pro forma to some, but as the statute and our cases make clear, patent claims
7 are not judged solely by their individual limitations.” *Id.* at 15. This is one reason
8 it is improper to consider the “gist” or “thrust” of an invention. MPEP 2141.02,
9 citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540 (Fed. Cir.
10 1983), cert. denied, 469 U.S. 851 (1984).

11 48. Also, I understand that prior art references cannot be excerpted such
12 that portions that teach away from the claimed invention are not considered.
13 References must be considered in their entirety, including portions that would lead
14 away from the claimed invention. MPEP 2141.02, citing *W.L. Gore*, 721 F.2d at
15 1540.

16 **3. CLAIM TERM DEFINITIONS USED IN THIS REPORT**

17 49. I have applied the claim constructions listed on pp. 11-13 of the
18 Murgulescu Report.

19 50. I understand that Silicon Labs has proposed that the term “relatively
20 linear circuit behavior” be given its plain and ordinary meaning. Adopting the
21 construction proposed by Defendant, as set forth on p. 13 of the Murgulescu
22 Report, would not change my conclusions.

23 51. I understand that Silicon Labs has proposed that the term “non-
24 varactor diode variable capacitance circuit” be construed as “a variable capacitance
25 circuit that does not contain a varactor diode.” Adopting the construction proposed
26 by Defendant, as set forth on pp. 13-14 the Murgulescu Report, would not change
27 my conclusions.

28 52. For the remaining terms cited on pp. 14-15 of the Murgulescu Report,

1 I understand that Silicon Labs has proposed that these terms be construed under
2 their plain and ordinary meaning. Adopting the constructions proposed by
3 Defendant that are set forth in the Murgulescu Report would not change my
4 conclusions.

5 **4. ANALYTICAL AND TECHNICAL BACKGROUND**

6 **4.1 Overview of the Patents-at-Issue**

7 53. The '372 Patent is generally directed to a method and apparatus for
8 generating a mixing signal, coarsely tuning the mixing signal with a discretely
9 variable capacitance, finely tuning the mixing signal with a continuously variable
10 capacitance, and combining the mixing signal with an input signal to produce an
11 output signal at a desired frequency.

12 54. The '441 Patent is generally directed to a method and apparatus for
13 providing frequency synthesis using a discretely variable capacitance circuit, a
14 continuously variable capacitance circuit, one or more switches, and a multi-bit
15 digital control signal to control the one or more switches. The capacitances may be
16 different and weighted with respect to each other, and the switches may be scaled
17 proportionally to capacitors to which they are coupled.

18 55. The '146 Patent is generally directed to a method and apparatus for
19 providing frequency synthesis using a phase-locked loop (PLL), a first oscillator
20 controlled by a discretely controllable capacitance, and a second oscillator
21 controlled by a continuously controllable capacitance, with the oscillators providing
22 an output frequency to the PLL.

23 56. The '055 Patent is generally directed to a method and apparatus for
24 providing frequency synthesis using a phase-locked loop (PLL), a controllable LC
25 tank resonant oscillator, parallel-connected continuously variable capacitance
26 circuits, a reference clock, and control signals generated from a phase difference
27 between an output frequency and a reference frequency.

28 57. The '761 Patent is generally directed to a method and apparatus for

1 providing frequency synthesis using a controllable LC tank resonant oscillator and
2 non-varactor diode variable capacitance circuits controlled by analog control
3 signals adjusted based on a phase difference between an output frequency and a
4 reference frequency.

5 58. The '011 Patent is generally directed to a method and apparatus for
6 generating a first set of control signals for coarse tuning and generating a second set
7 of control signals for fine-tuning a controllable LC tank oscillator.

8 **4.2 Applicable Frequency Synthesizer Design Principles**

9 59. The specifications for a synthesizer applicable to a wireless application
10 would address at least the following parameters: 1) integration, 2) cost, 3) power, 4)
11 phase noise/jitter, 5) accuracy, 6) lock time, and 7) tuning range.

12 **5. ANTICIPATION UNDER 35 U.S.C. § 102 – DETAILED REBUTTAL** 13 **OPINION**

14 **5.1 Craninckx and Craninckx & Steyaert References - Overview**

15 60. The Craninckx and Craninckx & Steyaert references (collectively
16 referred to herein as “Craninckx” using when necessary Craninckx for absolute
17 references) address the design of modern frequency synthesizers for application in
18 integrated RF transceivers.

19 **5.1.1 The Craninckx references do not invalidate the '011 Patent**

20 61. In order to read Claim 1 of the '011 Patent on Craninckx, the
21 following claim element must be met: “a second set of variable capacitor circuits
22 that together provide at least part of the capacitance amount, each variable capacitor
23 circuit having at least one control node configured to receive a control signal that
24 determines at least in part an amount of capacitance contributed by that capacitor
25 circuit.” Murgulescu has identified C1 and C2 in Craninckx as the second set of
26 variable capacitor circuits. In order to assert that each of C1 and C2 receives its
27 own unique control signal, Murgulescu resorted to the physical layout of C1 and C2
28 shown in Craninckx Fig. 5.10 to define the contact points of these layouts as

1 separate and unique control signals. This argument is problematic for a number of
2 reasons. Fig. 5.10 illustrates the layout of C1 and C2 as would be viewed from a
3 CAD (Computer Aided Design) tool. Craninckx identifies the layers shown as
4 “active area” and “contact.” “Active area” defines a region of the final integrated
5 circuit that is occupied by either a diffusion or a polysilicon gate (during
6 processing, the area defined by the active area layout is covered by silicon nitride
7 which is removed during a later processing). “Contact” is a region where, during
8 processing, silicon dioxide is etched so that there is a hole in the silicon dioxide in
9 the areas defined by the contact geometry. In a subsequent processing step, metal is
10 deposited and the contact holes allow for the ohmic connection of the metal to the
11 underlying diffusion. Metal interconnect is not illustrated in Fig. 5.10--only “active
12 area” and “contact” are shown. Prior to metal interconnect, Fig. 5.10 shows six
13 unique nodes. Murgulescu combines certain nodes together as one and keeps others
14 separate as is convenient to his fallacious argument. Fig. 5.10 was not offered by
15 Craninckx to illustrate connectivity but instead to illustrate an optimal layout to
16 reduce series resistance and improve matching. (See Craninckx, p. 121). It is the
17 schematic (Fig. 5.9) that tells the true story of connectivity. Rather than each of C1
18 and C2 having a separate and unique control signal, the junction of C1 and C2 is a
19 single node driven by a single voltage control signal V_C . In fact, Murgulescu
20 himself admitted that the same control voltage will be applied to the cathodes of C1
21 and C2. (See Murgulescu Deposition Transcript at 139:1-7). Thus, Craninckx fails
22 to meet this claim element.

23 62. In order to read Claim 1 of the '011 Patent on Craninckx, the
24 following claim element must be met: “a plurality of second control signals coupled
25 to the second set of variable capacitor circuits.” Murgulescu has identified C1 and
26 C2 of Craninckx as the second set of variable capacitor circuits. In order to assert
27 that each of C1 and C2 receives a plurality of control signals, Murgulescu resorted
28 to the physical layout of C1 and C2 as shown in Craninckx Fig. 5.10 and defined

1 contact points of these layouts as separate and unique control signals. As discussed
2 above, Craninckx only teaches a single control node and a single control signal that
3 is common to both C1 and C2, as identified in Fig. 5.9 (*see above*, Paragraph 61).
4 Thus, Craninckx fails to meet this claim element.

5 63. In order to read Claim 17 of the '011 Patent on Craninckx, the
6 following claim element must be met: "providing a second set of variable capacitor
7 circuits that together provide at least part of the capacitance amount, each variable
8 capacitor circuit having at least one control node configured to receive a control
9 signal." Murgulescu has identified C1 and C2 of Craninckx as the second set of
10 variable capacitor circuits. In order to assert that each of C1 and C2 receives its
11 respective control signal, Murgulescu resorted to the physical layout of C1 and C2
12 as shown in Craninckx Fig. 5.10 and defined contact points of these layouts as
13 separate and unique control signals. As discussed above, Craninckx only teaches a
14 single control node and a single control signal that is common to both C1 and C2,
15 as identified in Fig. 5.9 (*see above*, Paragraph 61) Thus, Craninckx fails to meet
16 this claim element.

17 64. In order to read Claim 1 of the '011 Patent on Craninckx, the
18 following claim element must be met: "a first set of variable capacitor circuits that
19 together provide at least part of the capacitance amount." Murgulescu has
20 identified Craninckx Fig. 7.1 as the first set of variable capacitor circuits. While
21 Craninckx offers Fig. 7.1 as "some implementation examples of switched tuning
22 capacitors," Craninckx gives no implementation details as to how this circuit would
23 be merged or inserted into the Fig. 5.9 VCO. Craninckx spends several paragraphs
24 discussing the performance impact of the various (a, b, and c) configurations,
25 explaining that great care must be taking when applying these circuits to an
26 oscillator. Finally, Craninckx states that, due to these possibly detrimental
27 performance impacts, he did not include switched capacitor banks in the VCO
28 configuration of his final phase-locked loop design. (*See* Craninckx at p. 163).

1 Thus, Craninckx teaches away from using the capacitors of Fig. 7.1 in the VCO of
2 Fig. 5.9. Moreover, all three configurations shown in Fig. 7.1 are switched
3 capacitors shunting a single inductor. The VCO of Fig. 5.9 uses two inductors.
4 Would Fig. 7.1c be shunted across each inductor of Fig. 5.9, or across the C1, C2
5 combination? The reference does not say. Thus, Murgulescu fails to make a 102
6 argument for this claim element.

7 **5.1.2 The Craninckx references do not invalidate the '761 Patent**

8 65. In order to read Claim 1 of the '761 Patent on Craninckx, the
9 following claim element must be met: "a plurality of non-varactor diode variable
10 capacitance circuits that together provide at least part of the capacitance amount,
11 each variable capacitance circuit having at least one control node configured to
12 receive an analog control signal." Murgulescu has identified C1 and C2 of
13 Craninckx as the plurality of non-varactor diode variable capacitance circuits. The
14 claim requires that each variable capacitance circuit have at least one control node.
15 Murgulescu resorted to the physical layout of C1 and C2 as shown in Craninckx
16 Fig. 5.10 and defined contact points of these layouts as separate and unique control
17 signals. However, C1 and C2 have a single node (*see above*, Paragraph 61) and a
18 single control signal as identified in Fig. 5.9 of Craninckx. Thus, C1 and C2 are not
19 a plurality of capacitor circuits but together form a single "variable capacitance
20 circuit" having "one control node." Therefore, Craninckx fails to meet this claim
21 element.

22 66. In order to read Claim 1 of the '761 Patent on Craninckx, the
23 following claim element must be met: "a plurality of different analog signals
24 coupled to provide the analog control signals for the variable capacitance circuits."
25 The claim requires that each "different analog signal" provides "the analog control
26 signal" for the "variable capacitance circuit" respectively. Murgulescu relies on
27 what he identifies as nodes N1 and N2 (in his report), which are the inputs to the
28 summing element in Craninckx Fig. 7.16. Murgulescu does not apply the plain and

1 ordinary meaning of “different analog signals,” “analog control signals,” and
2 “variable capacitance circuits.” The voltages on nodes N1 and N2 cannot each, by
3 themselves, be separate control signals because either N1 or N2 alone would result
4 in poor loop dynamics (such as stability and bandwidth). The voltages on nodes N1
5 and N2 can only control a variable capacitor circuit after they are summed together
6 to form a single control signal. Therefore, nodes N1 and N2 combine to form ONE
7 “analog control signal” (not signals) for a single “variable capacitance circuit” and
8 thus fails to meet the claim element: “analog control signals for the variable
9 capacitance circuits.” Thus Craninckx fails to meet this claim element.

10 67. In order to read Claim 23 of the '761 Patent on Craninckx, the
11 following claim element must be met: “Providing a plurality of non-varactor diode
12 variable capacitance circuits that together provide at least part of the capacitance
13 amount, each variable capacitance circuit having at least one control node
14 configured to receive an analog control signal.” Murgulescu has identified C1 and
15 C2 of Craninckx as the plurality of non-varactor diode variable capacitance circuits.
16 The claim requires that each variable capacitance circuit have at least one control
17 node. Murgulescu resorted to the physical layout of C1 and C2 as shown in
18 Craninckx and defined contact points of these layouts as separate and unique
19 control signals (*see also*, paragraph 61). However, C1 and C2 have a single node
20 and a single control signal. The single node is the node located between C1 and C2
21 and the single control signal is V_c , as identified in Fig. 5.9 of Craninckx. Thus,
22 Craninckx fails to meet this claim element.

23 68. In order to read Claim 23 of the '761 Patent on Craninckx, the
24 following claim element must be met: “generating a plurality of different analog
25 signals coupled to provide the control signals for the variable capacitance circuits.”
26 Murgulescu relies on what he identifies as nodes N1 and N2 (in his report), which
27 are the inputs to the summing element in Fig. 7.16. Murgulescu does not apply the
28 plain and ordinary meaning of “different analog signals,” “control signals,” and

1 “variable capacitance circuits.” The voltages on nodes N1 and N2 cannot each, by
2 themselves, be separate control signals because either N1 or N2 alone would result
3 in poor loop dynamics (such as stability and bandwidth). The voltages on nodes N1
4 and N2 can only control a variable capacitor circuit after they are summed together
5 to form a single control signal. Therefore, nodes N1 and N2 combine to form ONE
6 “analog control signal” (not signals) for a single “variable capacitance circuit” and
7 thus fails to meet the claim element: “control signals for the variable capacitance
8 circuits.” Thus Craninckx fails to meet this claim element.

9 **5.1.3 The Craninckx references do not invalidate the '055 Patent**

10 69. In order to read Claim 12 of the '055 Patent on Craninckx, the
11 following claim element must be met: “a plurality of parallel-connected
12 continuously variable capacitor circuits that together provide at least part of the
13 capacitance amount .” Murgulescu has identified C1 and C2 of Craninckx as the
14 plurality of parallel-connected continuously variable capacitor circuits. The plain
15 and ordinary meaning of “parallel-connected” for a two-terminal devices would be
16 that each device would share a single node in common. This meaning is supported
17 by the IEEE Dictionary (IEEE Std 100-1996), which defines “parallel” as “Two-
18 terminal elements are connected in parallel when they are connected between the
19 same pair of nodes.” Murgulescu resorts to the physical layout of C1 and C2 to
20 argue that tracks of active area suffice to meet the claim language of parallel.
21 However, capacitor circuits C1 and C2 are connected in series, not parallel, as
22 shown in the schematic of Fig. 5.9. Murgulescu invented a circuit configured
23 similarly to the Craninckx oscillator (*see* US5937340). During his deposition,
24 Murgulescu stated that the two varactors (Cs) in Fig. 1 of US5937340 were
25 connected in series (*see* Murgulescu Deposition Transcript at 52: 24-25, 53: 1-4).
26 Murgulescu’s explanation as to the connectivity of the two Cs devices in his
27 invention can also be applied to the two similarly connected capacitor devices in
28 Craninckx—in both cases, they are connected in series, not parallel. Thus,

1 Craninckx fails to meet this claim element.

2 70. In order to read Claim 12 of the '055 Patent on Craninckx, the
3 following claim element must be met: "a plurality of different control signals
4 coupled to inputs of the controllable oscillator to provide said control signals to the
5 plurality of variable capacitor circuits." The claim requires that each "different
6 control signal" provides "said control signal" for the "variable capacitance circuit"
7 respectively. Murgulescu relies on what he identifies as nodes N1 and N2 (in his
8 report), which are the inputs to the summing element in Fig. 7.16. Murgulescu does
9 not apply the plain and ordinary meaning of "different control signals," "control
10 signals," and "variable capacitance circuits." The voltages on nodes N1 and N2
11 cannot each, by themselves, be separate control signals because either N1 or N2
12 alone would result in poor loop dynamics (such as stability and bandwidth). The
13 voltages on nodes N1 and N2 can only control a variable capacitor circuit after they
14 are summed together to form a single control signal. Therefore, nodes N1 and N2
15 combine to form ONE "analog control signal" (not signals) for a single "variable
16 capacitance circuit" and thus fails to meet the claim element: "analog control
17 signals for the variable capacitance circuits." Thus Craninckx fails to meet this
18 claim element.

19 71. In order to read Claim 15 of the '055 Patent on Craninckx, the
20 following claim element must be met: "providing a plurality of parallel-connected
21 continuously variable capacitor circuits within an LC tank." Murgulescu has
22 identified C1 and C2 of Craninckx as the plurality of parallel-connected
23 continuously variable capacitor circuits. The plain and ordinary meaning of
24 "parallel-connected" for a two-terminal devices would be that each device would
25 share a single node in common. Murgulescu resorts to the physical layout of C1
26 and C2 to argue that tracks of active area suffice to meet the claim language of
27 parallel. Capacitor circuits C1 and C2 are connected in series, not parallel (*see*
28 *above*, Paragraph 69). Thus, Craninckx fails to meet this claim element.

1 72. In order to read Claim 15 of the '055 Patent on Craninckx, the
2 following claim element must be met: "applying each of the plurality of control
3 signals to at least different variable capacitor circuit." Murgulescu relies on what
4 he identifies as nodes N1 and N2 (in his report), which are the inputs to the
5 summing element in Fig. 7.16. Murgulescu does not apply the plain and ordinary
6 meaning of "plurality of control signals to at least different." Nodes N1 and N2
7 combine to form ONE control signal (not signals) to the SAME (not DIFFERENT)
8 control node (V_C of Fig. 5.9). The voltages on nodes N1 and N2 cannot each, by
9 themselves, be separate control signals because either N1 or N2 alone would result
10 in poor loop dynamics (such as stability and bandwidth). The voltages on nodes N1
11 and N2 can only control a variable capacitor circuit after they are summed together
12 to form a single control signal. Therefore, nodes N1 and N2 combine to form ONE
13 "analog control signal" (not signals) for a single "variable capacitor circuit" and
14 thus fails to meet the claim element: "each of the plurality of control signals to at
15 least different variable capacitor circuit." Thus Craninckx fails to meet this claim
16 element.

17 **5.1.4 The Craninckx references do not invalidate the '372 Patent**

18 73. In order to read Claim 1 of the '372 Patent on Craninckx, the
19 following claim element must be met: "adjusting a capacitance amount for the first
20 capacitance circuit." Murgulescu has identified Craninckx Fig. 7.1 as the first
21 capacitance circuit. While Craninckx offers Fig. 7.1 as "some implementation
22 examples of switched tuning capacitors," Craninckx gives no implementation
23 details as to how this circuit would be merged or inserted into the Fig. 5.9 VCO.
24 Craninckx spends several paragraphs discussing performance impact of the various
25 (a, b, and c) configurations, implying that great care must be taking when applying
26 these circuits to an oscillator. Finally, Craninckx states that, due to these possibly
27 detrimental performance impacts, he did not include switched capacitor banks in
28 the VCO configuration of his final phase-locked loop design. (See Craninckx at p.

1 163). Thus, Craninckx teaches away from using the capacitors of Fig. 7.1.
2 Moreover, all three configurations are switched capacitors shunting a single
3 inductor. The VCO of Fig. 5.9 uses two inductors. Would Fig. 7.1c be shunted
4 across each inductor of Fig. 5.9, or across the C1, C2 combination? The reference
5 does not say. Thus Murgulescu fails to establish that this claim element is met by
6 Craninckx.

7 74. In order to read Claim 1 of the '372 Patent on Craninckx, the following
8 claim element must be met: "the second capacitance circuit comprises a plurality of
9 continuous capacitance values and wherein the control signal comprises a plurality
10 of variable control signals." Murgulescu identifies two control voltages in Fig.
11 7.16, 1) the inverting input to the summer element, and 2) the inverting input to the
12 integrator, as meeting the claim language. Murgulescu states that these two control
13 signals combine to form one control signal to control the frequency of the
14 oscillator. However, the claim requires that "the control signal comprises a
15 plurality of variable control signals." In his argument, Murgulescu has turned the
16 meaning of the claim around to say that instead of a one comprising a plurality, he
17 uses a plurality to comprise one. Murgulescu has misinterpreted the claim.
18 Craninckx describes one control signal (V_{CTRL} or V_C) and not a plurality of control
19 signals (*see also* Paragraph 66). Thus, Craninckx does not satisfy this claim
20 element.

21 75. In order to read Claim 11 of the '372 Patent on Craninckx, the
22 following claim element must be met: "a first variable capacitance circuit."
23 Murgulescu has identified Craninckx Fig. 7.1 as the first capacitance circuit. While
24 Craninckx offers Fig. 7.1 as "some implementation examples of switched tuning
25 capacitors," Craninckx gives no implementation details as to how this circuit would
26 be merged or inserted into the Fig. 5.9 VCO. Craninckx spends several paragraphs
27 discussing performance impact of the various (a, b, and c) configurations implying
28 that great care must be taking when applying these circuits to an oscillator. Finally,

1 Craninckx states that, due to these possibly detrimental performance impacts, he did
2 not include switched capacitor banks in the VCO configuration of his final phase-
3 locked loop design. (See Craninckx at p. 163). Thus, Craninckx teaches away from
4 using the capacitors of Fig. 7.1. Moreover, all three configurations are switched
5 capacitors shunting a single inductor. The VCO of Fig. 5.9 uses two inductors.
6 Would Fig. 7.1c be shunted across each inductor of Fig. 5.9, or across the C1, C2
7 combination? The reference does not say. Thus Murgulescu fails to establish that
8 this claim element is met.

9 76. In order to read Claim 11 of the '372 Patent on Craninckx, the
10 following claim element must be met: "wherein the second control signal comprises
11 a plurality of variable control signals." Murgulescu identifies two control voltages
12 in Fig. 7.16, 1) the inverting input to the summer element, and 2) the inverting input
13 to the integrator, as meeting the claim language. Murgulescu states that these two
14 control signals combine to form one control signal to control the frequency of the
15 oscillator. However, the claim requires that "the control signal comprises a
16 plurality of variable control signals." In his argument, Murgulescu has turned the
17 meaning of the claim around to say that instead of a one comprising a plurality, he
18 uses a plurality to comprise one. Murgulescu has misinterpreted the claim.
19 Craninckx describes one control signal (V_{CTRL} or V_C) and not a plurality of control
20 signals (*see also* Paragraph 66). Thus, Craninckx does not satisfy this claim
21 element.

22 **5.1.5 The Craninckx references do not invalidate the '441 Patent**

23 77. In order to read Claim 1 of the '441 Patent on Craninckx, the
24 following claim element must be met: "a discretely variable capacitance circuit
25 integrated within the frequency synthesizer including a plurality of capacitor
26 circuits, each capacitor circuit comprising: a capacitor coupled between a first node
27 and a second node; and a switch coupled between the second node and a third node
28 to selectively couple the capacitor between the first node and the third node

1 depending upon a control signal applied to a control node for the switch.”
2 Murgulescu has identified Craninckx Fig. 7.1 as the discretely variable capacitance
3 circuit. While Craninckx offers Fig. 7.1 as “some implementation examples of
4 switched tuning capacitors,” Craninckx gives no implementation details as to how
5 this circuit would be merged or inserted into the Fig. 5.9 VCO. Craninckx spends
6 several paragraphs discussing performance impact of the various (a, b, and c)
7 configurations implying that great care must be taking when applying these circuits
8 to an oscillator. Finally, Craninckx states that, due to these possibly detrimental
9 performance impacts, he did not include switched capacitor banks in the VCO
10 configuration of his final phase-locked loop design. (See Craninckx at p. 163).
11 Thus, Craninckx teaches away from using the capacitors of Fig. 7.1. Moreover, all
12 three configurations are switched capacitors shunting a single inductor. The VCO
13 of Fig. 5.9 uses two inductors. Would Fig. 7.1c be shunted across each inductor of
14 Fig. 5.9, or across the C1, C2 combination? The reference does not say. Thus,
15 Murgulescu fails to establish that this claim element is met.

16 78. In order to read Claim 1 of the '441 Patent on Craninckx, the
17 following claim element must be met: “a plurality of analog signals as inputs, the
18 analog signals controlling a plurality of capacitor circuits within the continuously
19 variable capacitance circuit.” POSITA would interpret this claim to mean that each
20 “analog signal” controls its respective “capacitor circuit.” Murgulescu relies on
21 what he identifies as nodes N1 and N2 (in his report), which are the inputs to the
22 summing element in Fig. 7.16. Murgulescu does not apply the plain and ordinary
23 meaning of “a plurality of analog signals as inputs, the analog signals controlling a
24 plurality of capacitor circuits.” Nodes N1 and N2 combine to form ONE input, V_C
25 of Fig. 5.9, (not inputs) to control the capacitance circuit. The voltages on nodes
26 N1 and N2 cannot each, by themselves, be separate control signals because either
27 N1 or N2 alone would result in poor loop dynamics (such as stability and
28 bandwidth). The voltages on nodes N1 and N2 can only control a variable

1 capacitor circuit after they are summed together to form a single control signal.
2 Therefore, nodes N1 and N2 combine to form ONE “analog control signal” (not
3 signals) for a single “variable capacitor circuit” and thus fails to meet the claim
4 element: “plurality of ...analog signals controlling a plurality of capacitor circuits”
5 Thus Craninckx fails to meet this claim element.

6 79. In order to read Claim 1 of the '441 Patent on Craninckx, the
7 following claim element must be met: “wherein at least two of the capacitor circuits
8 within the discretely variable capacitance circuit have different capacitances with
9 respect to each other.” Murgulescu does not assert that Craninckx anticipates this
10 claim element and instead relies on Craninckx in view of Prakash (U.S. Patent No.
11 5,648,744) to meet this claim element. Thus, Murgulescu fails to establish that this
12 claim element is met by Craninckx alone.

13 80. In order to read Claim 5 of the '441 Patent on Craninckx, the
14 following claim element must be met: “a discretely variable capacitance circuit
15 integrated within the frequency synthesizer including a plurality of capacitor
16 circuits, each capacitor circuit comprising: a capacitor coupled between a first node
17 and a second node; and a switch coupled between the second node and a third node
18 to selectively couple the capacitor between the first node and the third node
19 depending upon a control signal applied to a control node for the switch.”
20 Murgulescu has identified Craninckx Fig. 7.1 as the discretely variable capacitance
21 circuit. While Craninckx offers Fig. 7.1 as “some implementation examples of
22 switched tuning capacitors,” Craninckx gives no implementation details as to how
23 this circuit would be merged or inserted into the Fig. 5.9 VCO. Craninckx spends
24 several paragraphs discussing performance impact of the various (a, b, and c)
25 configurations implying that great care must be taking when applying these circuits
26 to an oscillator. Finally, Craninckx states that, due to these possibly detrimental
27 performance impacts, he did not include switched capacitor banks in the VCO
28 configuration of his final phase-locked loop design. (See Craninckx at p. 163).

1 Thus, Craninckx teaches away from using the capacitors of Fig. 7.1. Moreover, all
2 three configurations are switched capacitors shunting a single inductor. The VCO
3 of Fig. 5.9 uses two inductors. Would Fig. 7.1c be shunted across each inductor of
4 Fig. 5.9, or across the C1, C2 combination? The reference does not say. Thus,
5 Murgulescu fails to establish that this claim element is met.

6 81. In order to read Claim 5 of the '441 Patent on Craninckx, the
7 following claim element must be met: "the capacitor circuits have different
8 capacitances so that they are weighted with respect to each other." Murgulescu
9 conclusorily relies on the alleged view of a POSITA without offering any reference
10 or support for that conclusion. Thus, Murgulescu fails to establish that this claim
11 element is met.

12 82. In order to read Claim 5 of the '441 Patent on Craninckx, the
13 following claim element must be met: "the switches are MOS transistors and
14 wherein a size for each MOS transistor is scaled proportionally with a size of the
15 respective capacitor to which each MOS transistor is coupled." Murgulescu
16 conclusorily relies on the alleged knowledge of a POSITA for this element and
17 points to a Section 103 argument in Appendix F. Thus, Murgulescu fails to
18 establish that this claim element is met.

19 **5.2 Kral and Kral, Behbahani & Abidi References - Overview**

20 83. The Kral and Kral, Behbahani & Abidi references (collectively
21 referred to herein as "Kral" using when necessary Kral for absolute references)
22 address the design of fully integrated oscillators for single-chip wireless
23 transceivers. In particular, Kral addresses the design of an RF CMOS oscillator
24 with a wide tuning range without compromising power or phase noise. Kral
25 teaches two methods to achieve wide tuning range: 1) switched tuning capacitors,
26 and 2) switched tuning inductors. The latter method (as described by Kral) is
27 switching complete VCOs with their respective inductors.

28 **5.2.1 The Kral references do not invalidate the '146 Patent**

1 84. In order to read Claim 1 of the '146 Patent on Kral, the following
2 claim elements must be met: "a first controlled oscillator within the phase locked
3 loop having an output frequency determined by a discretely controllable
4 capacitance amount," and "a second controlled oscillator within the phase locked
5 loop having an output frequency determined by a discretely controllable
6 capacitance amount." Murgulescu combines the circuit in Fig. 4 of Kral with the
7 circuit of Fig. 6 of Kral. Kral does not combine these two tuning methods but
8 rather proposes one or the other: "With this method, either an array of weighted
9 capacitors may be switched in parallel with a *single* oscillator core, or one of an
10 array of multiple oscillator cores may be selected, each tuned by inductors of
11 various sizes." Therefore, Kral teaches away from using both tuning methods in a
12 single implementation. Thus Murgulescu fails to establish that these claim
13 elements are met.

14 85. In order to read Claim 4 of the '146 Patent on Kral, the following
15 claim elements must be met: "a first controlled oscillator within the phase locked
16 loop having an output frequency determined by a discretely controllable
17 capacitance amount," and "a second controlled oscillator within the phase locked
18 loop having an output frequency determined by a discretely controllable
19 capacitance amount." Murgulescu combines the circuit in Fig. 4 of Kral with the
20 circuit of Fig. 6 of Kral. Kral does not combine these two tuning methods but
21 rather proposes one or the other: "With this method, either an array of weighted
22 capacitors may be switched in parallel with a *single* oscillator core, or one of an
23 array of multiple oscillator cores may be selected, each tuned by inductors of
24 various sizes." Therefore, Kral teaches away from using both tuning methods in a
25 single implementation. Thus Murgulescu fails to establish that these claim
26 elements are met.

27 86. In order to read Claim 11 of the '146 Patent on Kral, the following
28 claim elements must be met: "the first controllable oscillator having an output

1 frequency determined by a discretely controllable capacitance amount,” and “the
2 second controlled oscillator within the phase locked loop having an output
3 frequency determined by a discretely controllable capacitance amount.”
4 Murgulescu combines the circuit in Fig. 4 of Kral with the circuit of Fig. 6 of Kral.
5 Kral does not combine these two tuning methods but rather proposes one or the
6 other: “With this method, either an array of weighted capacitors may be switched in
7 parallel with a *single* oscillator core, or one of an array of multiple oscillator cores
8 may be selected, each tuned by inductors of various sizes.” Therefore, Kral teaches
9 away from using both tuning methods in a single implementation. Thus
10 Murgulescu fails to establish that these claim elements are met.

11 **5.3 Connell Reference - Overview**

12 87. Connell describes a tunable crystal oscillator. Tuning is achieved
13 using switched varactor diodes. Switches used to switch in the varactor diodes are
14 controlled via a level shifter that shifts a low control voltage to a higher control
15 voltage produced by a DC-DC converter (block 210) clocked by a prescaler (206)
16 whose input comes from the crystal oscillator. Connell does not describe a
17 frequency synthesizer or a PLL, nor does Connell mention either term.

18 **5.3.1 The Connell reference does not invalidate the '441 Patent**

19 88. In order to read Claim 1 of the '441 Patent on Connell, the following
20 claim element must be met: “A frequency synthesizer having at least one variable
21 frequency output.” This claim element is part of the preamble which carries with it
22 the antecedent of “the frequency synthesizer” in the body of the claim, and thus the
23 preamble is limiting as it recites necessary structure for the claim in its entirety.
24 Connell does not teach “a frequency synthesizer” as construed by the court (“a
25 circuit producing one or more signals at frequencies that are different from a single
26 input frequency, based on a reference frequency”). Connell teaches a “crystal
27 oscillator” which is “arranged to utilize a tuning network” (*see* ABSTRACT). At
28 any given time, there is only one frequency present in the Connell oscillator. Thus,

1 there cannot be two frequencies that are different as required by the court-ordered
2 claim construction cited above. Murgulescu argues for the presence of a frequency
3 synthesizer by pointing to certain terms used in the figures. According to
4 Murgulescu, the presence of “charge pump” 210 and “prescaler” 206 establishes
5 that Connell discloses a “frequency synthesizer.” This is incorrect. The “charge
6 pump” on Connell is a “voltage multiplying charge pump” (Col 3, Ln 45-46). The
7 “prescaler” is used to provide the clock frequency to the “charge pump” (Col 5, Ln
8 35-38). In order to meet the court-ordered claim construction of “frequency
9 synthesizer,” at least one signal must be produced at a frequency different from a
10 single input frequency. The Connell crystal oscillator fails to meet this definition.
11 Thus, Murgulescu fails to establish that this claim element is met.

12 89. In order to read Claim 1 of the '441 Patent on Connell, the following
13 claim element must be met: “wherein at least two of the capacitor circuits within
14 the discretely variable capacitance circuit have different capacitances with respect
15 to each other.” Murgulescu combines capacitors 112A and 216A to make a
16 capacitor circuit and argues that this combination is different from capacitor 216B.
17 This is an incorrect reading of the reference. Claim 1 makes very clear the meaning
18 of “capacitor circuit.” Capacitor 112A does not meet the claim limitation of a
19 “capacitor circuit” being “each capacitor circuit comprising: a capacitor coupled
20 between a first node and a second node; and a switch coupled between the second
21 node and a third node to selectively couple the capacitor between the first node and
22 the third node depending upon a control signal applied to a control node for the
23 switch.” Further, the claim requires “a multiple-bit digital control signal coupled to
24 the control nodes of the plurality of switches to include or exclude the capacitors
25 within the plurality of capacitor circuits.” Capacitor 112A can never be “excluded”
26 as the claim requires because it is connected between node “B” and “VREG”
27 without an intervening switch. Therefore, capacitor 112A cannot be part of the
28 “capacitance circuit” and thus should not be included as such. Connell therefore

1 fails to meet this claim element.

2 90. In order to read Claim 5 of the '441 Patent on Connell, the following
3 claim element must be met: "A frequency synthesizer having at least one variable
4 frequency output." This claim element is part of the preamble which carries with it
5 the antecedent of "the frequency synthesizer" in the body of the claim, and thus the
6 preamble is limiting as it recites necessary structure for the claim in its entirety.
7 Connell does not teach "a frequency synthesizer" as construed by the court ("a
8 circuit producing one or more signals at frequencies that are different from a single
9 input frequency, based on a reference frequency"). Murgulescu argues for the
10 presence of a frequency synthesizer by pointing to certain terms in the figures.
11 According to Murgulescu, the presence of "charge pump" 210 and "prescaler" 206
12 establishes that Connell discloses a "frequency synthesizer." This is incorrect. The
13 "charge pump" in Connell is a "voltage multiplying charge pump" (Col 3, Ln 45-
14 46). The "prescaler" is used to provide the clock frequency to the "charge pump"
15 (Col 5, Ln 35-38). In order to meet the court-ordered claim construction of
16 "frequency synthesizer," at least one signal must be produced at a frequency
17 different from a single input frequency. The Connell crystal oscillator fails to meet
18 this definition. Thus, Murgulescu fails to establish that this claim element is met.

19 91. In order to read Claim 5 of the '441 Patent on Connell, the following
20 claim element must be met: "wherein at the capacitor circuits have different
21 capacitances so that they are weighted with respect to each other." Murgulescu
22 combines capacitors 112A and 216A to make a capacitor circuit and argues that this
23 combination is different that capacitor 216B. This is an incorrect reading of the
24 reference. Claim 5 makes very clear the meaning of "capacitor circuit." Capacitor
25 112A does not meet the claim limitation of a "capacitor circuit" being "each
26 capacitor circuit comprising: a capacitor coupled between a first node and a second
27 node; and a switch coupled between the second node and a third node to selectively
28 couple the capacitor between the first node and the third node depending upon a

1 control signal applied to a control node for the switch.” In addition, the claim
2 states: “a multiple-bit digital control signal coupled to the control nodes of the
3 plurality of switches to include or exclude each of the capacitors within the
4 capacitor circuits.” Therefore, for capacitor 112A to be included as part of the
5 “capacitor circuit” there must be a way to “exclude” it and no such way exists
6 because it is connected between node “B” and “VREG” without an intervening
7 switch. Capacitor 112A cannot be included as part of the “capacitor circuit” and
8 without it, there is no way to meet the “different capacitances” requirement of the
9 claim. Connell therefore fails to meet this claim element.

10 92. In order to read Claim 5 of the '441 Patent on Connell, the following
11 claim elements must be met: “wherein the switches are MOS transistors and
12 wherein a size for each MOS transistor is scaled proportionally with a size of the
13 respective capacitor to which each MOS transistor is coupled.” Connell does not
14 contain these claim elements. There is no indication in Connell whatsoever that the
15 transistors are sized proportionally with anything. Connell only states that the
16 switches should be relatively small. Ultimately, Murgulescu relies on his Section
17 103 argument in Appendix F in attempt to make his Section 102 argument here.
18 Connell does not meet these claim elements.

19 **5.4 Rotzoll Reference - Overview**

20 93. Rotzoll describes a band switchable resonant circuit for a voltage
21 controlled oscillator using an inductor and switched varactor diodes.

22 **5.4.1 The Rotzoll reference does not invalidate the '441 Patent**

23 94. In order to read Claim 1 of the '441 Patent on Rotzoll, the following
24 claim element must be met: “a continuously variable capacitance circuit integrated
25 within the frequency synthesizer and having a plurality of analog signals as inputs,
26 the analog signals controlling a plurality of capacitor circuits within the
27 continuously variable capacitance circuit.” Murgulescu incorrectly argues that VIN
28 and VBIAS are the plurality of analog signals performing the controlling. Only

1 VIN controls the capacitor circuits. VBIAS provides the voltage on the gates of
2 transistors 3T1 and 3T2 which “enables the oscillator circuit” (Col 8 , Ln 32-33).
3 This is different from controlling the capacitor circuits because a change in VBIAS
4 does not result in a change in the capacitance of the varactor diodes. Therefore,
5 VBIAS cannot comprise one of the claimed “analog signals.” Rotzoll does not
6 meet this claim element.

7 95. In order to read Claim 5 of the '441 Patent on Rotzoll, the following
8 claim elements must be met: “wherein at the capacitor circuits have different
9 capacitances so that they are weighted with respect to each other “ and “wherein the
10 switches are MOS transistors and wherein a size for each MOS transistor is scaled
11 proportionally with a size of the respective capacitor to which each MOS transistor
12 is coupled.” Fig. 3 is the Rotzoll preferred embodiment (Col 8, Ln 6-43) which
13 gives no indication of the size of the capacitors (varactors) but does indicate that the
14 transistor switches are equal in size (Col 8, Ln 12-14). To meet the claim language,
15 the capacitors must be of different size. If one assumes that the preferred
16 embodiment comprises capacitors of different size (and thus meets the claim
17 language), then the preferred embodiment fails to meet a different required claim
18 element that the transistors are scaled proportionally to the capacitors. If, on the
19 other hand, one assumes that the capacitors in the preferred embodiment are scaled
20 according the transistor sizes, then the capacitors would have a scale factor of unity
21 and thus fail to meet the requirement of the claim (that the capacitors have different
22 weighting with respect to each other). Rotzoll never teaches that the transistor
23 switches are scaled according to the capacitor sizes. Therefore, Murgulescu
24 mischaracterizes the teachings of Rotzoll to suit his own position. Rotzoll does not
25 meet this claim element.

26 96. In order to read Claim 7 of the '441 Patent on Rotzoll, the following
27 claim elements must be met: “a continuously variable capacitance circuit integrated
28 within the frequency synthesizer and having a plurality of analog signals as inputs,

1 the analog signals controlling a plurality of capacitor circuits within the
2 continuously variable capacitance circuit.” Murgulescu incorrectly argues that VIN
3 and VBIAS are the plurality of analog signals performing the controlling. Only
4 VIN controls the capacitor circuits. VBIAS provides the voltage on the gates of
5 transistors 3T1 and 3T2 which “enables the oscillator circuit” (Col 8 , Ln 32-33).
6 This is different from controlling the capacitor circuits because a change in VBIAS
7 does not result in a change in the capacitance of the varactor diodes. Therefore,
8 VBIAS cannot comprise one of the claimed “analog signals.” Rotzoll does not
9 meet this claim element.

10 97. In order to read Claim 17 of the '441 Patent on Rotzoll, the following
11 claim elements must be met: “wherein at the capacitor circuits have different
12 capacitances so that they are weighted with respect to each other “ and “wherein the
13 switches are MOS transistors and wherein a size for each MOS transistor is scaled
14 proportionally with a size of the respective capacitor to which each MOS transistor
15 is coupled.” Fig. 3 is the Rotzoll preferred embodiment (Col 8, Ln 6-43) which
16 gives no indication of the size of the capacitors (varactors) but does indicate that the
17 transistor switches are equal in size (Col 8, Ln 12-14). To meet the claim language,
18 the capacitors must be of different size. If one assumes that the preferred
19 embodiment comprises capacitors of different size (and thus meets the claim
20 language), then the preferred embodiment fails to meet a different required claim
21 element that the transistors are scaled proportionally to the capacitors. If on the
22 other hand, if one assumes that the capacitors in the preferred embodiment are
23 scaled according the transistor sizes, then the capacitors would have a scale factor
24 of unity and thus fail to meet the requirement of the claim (that the capacitors have
25 different weighting with respect to each other). Rotzoll never teaches that the
26 transistor switches are scaled according to the capacitor sizes. Therefore,
27 Murgulescu mischaracterizes the teachings of Rotzoll to suit his own position.
28 Rotzoll does not meet this claim element.

1 98. In order to read Claim 21 of the '441 Patent on Rotzoll, the following
2 claim elements must be met: "providing a continuously variable capacitance circuit
3 integrated within the frequency synthesizer and having a plurality of analog signals
4 as inputs; and utilizing the analog signals to control a plurality of capacitor circuits
5 within the continuously variable capacitance circuit." Murgulescu incorrectly
6 argues that VIN and VBIAS are the plurality of analog signals performing the
7 controlling. Only VIN controls the capacitor circuits. VBIAS provides the voltage
8 on the gates of transistors 3T1 and 3T2 which "enables the oscillator circuit" (Col 8
9 , Ln 32-33). This is different from controlling the capacitor circuits because a
10 change in VBIAS does not result in a change in the capacitance of the varactor
11 diodes. Therefore, VBIAS cannot comprise one of the claimed "analog signals."
12 Rotzoll does not meet this claim element.

13 99. In order to read Claim 25 of the '441 Patent on Rotzoll, the following
14 claim elements must be met: "providing a continuously variable capacitance circuit
15 integrated within the frequency synthesizer and having a plurality of analog signals
16 as inputs; and utilizing the analog signals to control a plurality of capacitor circuits
17 within the continuously variable capacitance circuit." Murgulescu incorrectly
18 argues that VIN and VBIAS are the plurality of analog signals performing the
19 controlling. Only VIN controls the capacitor circuits. VBIAS provides the voltage
20 on the gates of transistors 3T1 and 3T2 which "enables the oscillator circuit" (Col 8
21 , Ln 32-33). This is different from controlling the capacitor circuits because a
22 change in VBIAS does not result in a change in the capacitance of the varactor
23 diodes. Therefore, VBIAS cannot comprise one of the claimed "analog signals."
24 Rotzoll does not meet this claim element.

25 **5.4.2 The Rotzoll reference does not invalidate the '761 Patent**

26 100. In order to read Claim 1 of the '761 Patent on Rotzoll, the following
27 claim element must be met: "a plurality of non-varactor diode variable capacitance
28 circuits." Rotzoll teaches varactor diodes in its architecture as noted in the

1 ABSTRACT (see below). The term “varactor” is used 48 additional times

2 [57]

ABSTRACT

3 A band switchable resonant circuit for a voltage controlled
4 oscillator has an inductive component in parallel with a
5 plurality of varactor diodes. Some of the varactor diodes are
6 selectively switchable to control the frequency range of
7 circuit operation.

8 throughout the specification and claims to describe capacitor circuits. Rotzoll does
9 not meet this “non-varactor” claim element.

10 101. In order to read Claim 1 of the '761 Patent on Rotzoll, the following
11 claim element must be met: “a plurality of different analog signals coupled to
12 provide the analog control signals for the variable capacitance circuits.”

13 Murgulescu incorrectly argues that VIN and VBIAS are the plurality of analog
14 signals performing the controlling. Only VIN controls the capacitor circuits.

15 VBIAS provides the voltage on the gates of transistors 3T1 and 3T2 which “enables
16 the oscillator circuit” (Col 8 , Ln 32-33). This is different from controlling the
17 capacitor circuits because a change in VBIAS does not result in a change in the
18 capacitance of the varactor diodes. Therefore, VBIAS cannot comprise one of the
19 claimed “analog signals.” Rotzoll does not meet this claim element.

20 102. In order to read Claim 1 of the '761 Patent on Rotzoll, the following
21 claim element must be met: “being adjusted based upon a phase difference between
22 a first signal that is related to the output frequency and a second signal.” Rotzoll
23 does not teach the structure of a PLL nor the structure of a synthesizer. Murgulescu
24 conclusorily relies on the alleged knowledge of a POSITA to make this argument.
25 Murgulescu testified that “not all PLLs use a PFD.” (See Murgulescu Deposition
26 Transcript at p.151: 11-21.) Therefore, an adjustment based on phase difference is
27 not necessarily implied by the mere presence of a PLL. Thus, Murgulescu fails to
28 establish that this claim element is met.

103. In order to read Claim 23 of the '761 Patent on Rotzoll, the following

1 claim element must be met: "Providing a plurality of non-varactor diode variable
2 capacitance circuits." Rotzoll teaches varactor diodes in its architecture as noted in
3 the ABSTRACT (see below). The term "varactor" is used 48 additional times

4 [57]

ABSTRACT

5 A band switchable resonant circuit for a voltage controlled
6 oscillator has an inductive component in parallel with a
7 plurality of varactor diodes. Some of the varactor diodes are
8 selectively switchable to control the frequency range of
circuit operation.

9 throughout the specification and claims to describe capacitor circuits. Rotzoll does
10 not meet this "non-varactor" claim element.

11 104. In order to read Claim 23 of the '761 Patent on Rotzoll, the following
12 claim element must be met: "a plurality of different analog signals coupled to
13 provide the control signals for the variable capacitance circuits." Murgulescu
14 incorrectly argues that VIN and VBIAS are the plurality of analog signals
15 performing the controlling. Only VIN controls the capacitor circuits. VBIAS
16 provides the voltage on the gates of transistors 3T1 and 3T2 which "enables the
17 oscillator circuit" (Col 8 , Ln 32-33). This is different from controlling the
18 capacitor circuits because a change in VBIAS does not result in a change in the
19 capacitance of the varactor diodes. Therefore, VBIAS cannot comprise one of the
20 claimed "analog signals." Rotzoll does not meet this claim element.

21 105. In order to read Claim 23 of the '761 Patent on Rotzoll, the following
22 claim element must be met: "by adjusting the different analog signals based upon a
23 phase difference between a first signal that is related to the output frequency and a
24 second signal." Rotzoll does not teach the structure of a PLL nor of a synthesizer.
25 Murgulescu conclusorily relies on the alleged knowledge of a POSITA to make this
26 argument. Murgulescu fails to establish that this claim element is met.

27 5.5 Humphreys Reference - Overview

28 106. Humphreys describes a voltage controllable resonant oscillator.

1 Humphreys combines multiple Voltage Variable Capacitances (VVCs) essentially
2 functioning as switched capacitors performing coarse adjustment, in parallel with a
3 single variable reactance element providing fine adjustment.

4 **5.5.1 The Humphreys reference does not invalidate the '011 Patent**

5 107. In order to read Claim 1 of the '011 Patent on Humphreys, the
6 following claim element must be met: "a second set of variable capacitor circuits."
7 Murgulescu combines elements 130, 160, 150, and 165 of Humphreys to meet the
8 "second set" requirement. The claim also requires: "the second control signals are
9 configured to determine fine tuning." In Humphreys the singular element 130 (in
10 series with capacitor 160) performs the fine tuning. The "VVC" elements are
11 switches and perform coarse tuning (*see* Fig. 7 of Humphreys). Because there is
12 only one element 130 involved with fine tuning, elements 130, 160, 150, and 165
13 cannot comprise the claimed "second set." Therefore, the claim language is not met
14 by Humphreys.

15 108. In order to read Claim 17 of the '011 Patent on Humphreys, the
16 following claim element must be met: "providing a second set of variable capacitor
17 circuits." Murgulescu combines elements 130, 160, 150, and 165 to meet the
18 "second set" requirement. The claim also requires: "fine tuning the controllable
19 oscillator by utilizing a plurality of second control signals to adjust an amount of
20 capacitance." In Humphreys the singular element 130 (in series with capacitor 160)
21 performs the fine tuning. The "VVC" elements are switches and perform coarse
22 tuning (*see* Fig. 7 of Humphreys). Because there is only one element involved with
23 fine tuning, the claim language is not met by Humphreys.

24 **5.5.2 The Humphreys reference does not invalidate the '372 Patent**

25 109. In order to read Claim 1 of the '372 Patent on Humphreys, the
26 following claim element must be met: "wherein the control signal comprises a
27 plurality of variable control signals." Murgulescu combines elements 130 and 150
28 to meet the "second capacitance circuit" requirement. The claim also requires:

1 “further tuning the mixing signal frequency to the desired mixing signal frequency
2 for the mixing signal by adjusting the capacitance amount for the second
3 capacitance circuit.” The “further tuning” follows “tuning” of the “first capacitance
4 circuit” and is, according to the specification, fine tuning. In Humphreys the
5 singular control signal, 180, controlling element 130 performs the fine tuning. The
6 “VVC” elements are switches and perform coarse tuning (*see* Fig. 7 of
7 Humphreys). Because there is only one control signal involved with fine tuning,
8 the claim language is not met by Humphreys.

9 110. In order to read Claim 11 of the '372 Patent on Humphreys, the
10 following claim element must be met: “wherein the second control signal comprises
11 a plurality of variable control signals.” The claim also requires: “the second control
12 signal to finely tune the frequency.” Murgulescu combines control signals 180 and
13 190 and controlling elements 130 and 150, respectively, to meet this claim element.
14 The singular control signal, 180, controlling element 130 performs the fine tuning.
15 The “VVC” elements are switches and perform coarse tuning (*see* Fig. 7 of
16 Humphreys). Because there is only one control signal involved with fine tuning,
17 the claim language is not met by Humphreys.

18 **5.6 Parker & Ray Reference - Overview**

19 111. Parker & Ray (“Parker”) describe a tuned oscillator suitable for
20 application to a PLL in wireless communications applications. The oscillator uses
21 switched capacitors for coarse tuning and varactors for fine tuning.

22 **5.6.1 The Parker & Ray reference does not invalidate the '372 Patent**

23 112. In order to read Claim 1 of the '372 Patent on Parker, the following
24 claim element must be met: “wherein the control signal comprises a plurality of
25 variable control signals.” In addition, the claim requires “adjusting a control signal
26 to adjust the capacitance” so it is clear that capacitance is adjusted by the control
27 signal. Murgulescu cites “From the loop filter” and “Bias” as making up the
28 plurality of variable control signals. “From the loop filter” signal controls CVAR

1 varactors, whereas “Bias” does not. “Bias” cannot be one of the variable control
2 signals because “Bias” controls M3, which provides the bias current to the cross-
3 coupled transistors M1 and M2. Therefore, “Bias” does not “adjust the
4 capacitance” as the claim requires. Thus, Parker does not meet this claim element.

5 **5.7 Yamashita Reference - Overview**

6 113. Yamashita teaches a PLL using a VCO with band switching. Band
7 switching and voltage control (from the loop filter) are achieved using varactor
8 diodes.

9 **5.7.1 The Yamashita reference does not invalidate the '011 Patent**

10 114. In order to read Claim 1 of the '011 Patent on Yamashita, the
11 following claim element must be met: “a first set of variable capacitor circuits” and
12 “a second set of variable capacitor circuits.” Yamashita embodiments show at most
13 two capacitor circuits, one for the coarse (V_{band}) adjustment and the other for the
14 fine (V_{cont}) adjustment. As support for the presence of multiple capacitor circuits,
15 Murgulescu cites the second to last paragraph of the Yamashita specification where
16 Yamashita states that it is possible “to compose a voltage controlled oscillator
17 circuit according to the present invention which includes three or more variable
18 capacitance diodes”(Col 8, Ln 65-67). However, there is no teaching in Yamashita
19 how a configuration having a “first set” and a “second set” can be designed and
20 implemented. Since there is no teaching in Yamashita for this claim element,
21 Murgulescu fails to establish that this claim element is met.

22 **5.7.2 The Yamashita reference does not invalidate the '055 Patent**

23 115. In order to read Claim 1 of the '055 Patent on Yamashita, the
24 following claim element must be met: “the control signals being generated from, at
25 least in part, a phase difference between a first clock signal on the first clock node
26 that is related to the output frequency and a second clock signal on the second clock
27 node that is related to the reference frequency.” Yamashita teaches that V_{cont} comes
28 from LPF, which is the loop filter driven from the Phase Detector. This voltage is a

1 control signal and depends on the phase difference between the first clock signal
2 and the second clock signal. However, V_{band} does not depend on the relationship of
3 the clocks. According to Yamashita, "A DC voltage V_{band} is applied to the variable
4 capacitance diode D1 via a choking coil L1 by a voltage source such as a constant-
5 voltage regulated power supply" Col 4, Ln 28-34. Yamashita further states,
6 "Another control voltage V_{cont} is applied to the variable capacitance diode D2 by a
7 voltage source which is independent of the voltage source of the DC voltage V_{band} ."
8 Thus Yamashita clearly states that V_{cont} and V_{band} are independent of one another,
9 and therefore they cannot both be controlled by the phase difference of the
10 reference clock and the output clock. Yamashita does not meet this claim element.

11 116. In order to read Claim 15 of the '055 Patent on Yamashita, the
12 following claim element must be met: "generating a plurality of different control
13 signals utilizing first and second clock signals." Yamashita teaches that V_{cont} comes
14 from LPF which is the loop filter driven from the Phase Detector. This voltage is a
15 control signal and depends on the phase difference between the first clock signal
16 and the second clock signal. However, V_{band} does not depend on the relationship of
17 the clocks. According to Yamashita, "A DC voltage V_{band} is applied to the variable
18 capacitance diode D1 via a choking coil L1 by a voltage source such as a constant-
19 voltage regulated power supply" Col 4, Ln 28-34. Yamashita further states,
20 "Another control voltage V_{cont} is applied to the variable capacitance diode D2 by a
21 voltage source which is independent of the voltage source of the DC voltage V_{band} ."
22 Thus Yamashita clearly states that V_{cont} and V_{band} are independent of one another,
23 and therefore they cannot both be controlled by the phase difference of the
24 reference clock and the output clock. Yamashita does not meet this claim element.

25 **5.8 Mori Reference - Overview**

26 117. Mori describes a VCO to be used in a PLL application where the VCO
27 incorporates variable capacitance diode tuning for both fine and coarse tuning.

28 **5.8.1 The Mori reference does not invalidate the '055 Patent**

118. In order to read Claim 1 of the '055 Patent on Mori, the following claim element must be met: "a plurality of parallel connected continuously variable capacitor circuits." In order to allege Mori discloses this claim element, Murgulescu argues that C_{VD2} , C_C , L_B , C_5 , C_3 , R_A , R_B , C_1 , C_2 , R_C , C_A , C_B , R_D , and T_r are in parallel with C_4 , C_{VD1} , and L_A . This is an incorrect interpretation of the reference. Murgulescu conveniently draws boxes in such a way as to allege a parallel connection. However, C_{VD1} and C_{VD2} are the continuously variable capacitor elements and these are not connected in parallel. The plain and ordinary meaning of "parallel connected" for two-terminal devices would be that each device would share a single node in common. The IEEE Dictionary (IEEE Std 100-1996) defines "parallel" as "Two-terminal elements are connected in parallel when they are connected between the same pair of nodes." This meaning of parallel is consistent with what is taught in the specification of the '055 Patent. Mori does not meet this claim element.

119. In order to read Claim 1 of the '055 Patent on Mori, the following claim element must be met: "the control signals being generated from, at least in part, a phase difference between a first clock signal on the first clock node that is related to the output frequency and a second clock signal on the second clock node that is related to the reference frequency." Mori teaches that V_{D2} is adjusted when V_{D1} goes outside of a range of voltages. Because V_{D1} correlates to the frequency output from the VCO, a range of voltages for V_{D1} correspond to a range of frequencies. Therefore, V_{D2} depends on frequency and not phase. Murgulescu incorrectly argues otherwise. Mori does not satisfy this claim element.

6. OBVIOUSNESS UNDER 35 U.S.C. § 103 – DETAILED REBUTTAL OPINION

6.1.1 The '011 Patent is not obvious over the various combinations of Mori, Hester, Todsén, Prakash, Peckham, Zuta, Oba, Craninckx, and Rasmussen.

120. Mori generally teaches a voltage controlled oscillator operating within

1 a PLL with two analog control inputs. One of the inputs is derived from the charge
2 pump based on the phase difference between the reference frequency and the VCO
3 output frequency and functions as the fine control of the oscillator. The other
4 analog control input is derived from the difference in the reference frequency and
5 the VCO frequency as measured by the response at the output of the charge pump
6 and functions as coarse control of the oscillator. Mori is not specific as to the
7 technology used in his implementation, but it is clear that MOS technology was not
8 used. Mori is either bipolar technology or discrete.

9 121. Hester teaches a single-ended switched capacitor array implemented in
10 MOS technology.

11 122. Oba generally teaches a voltage controlled oscillator that is controlled
12 by three analog inputs where one is held constant while the other two are variable
13 inputs. This effectively yields two analog input voltages (e.g., $V_a - V_c$, and $V_b -$
14 V_c) where the sensitivity of frequency to voltage change is different for the two
15 analog inputs, effectively making one of the inputs a fine control and the other a
16 coarse control.

17 123. Todsen describes a trimmable switched capacitor array implemented in
18 MOS technology.

19 124. Prakash generally teaches a PLL using a VCO operable in multiple
20 narrowly defined frequency bands. The VCO comprises a differential switched
21 varactor array that has a single analog control. Coarse tuning is achieved via the
22 switched-varactor array, and fine tuning is achieved via the single common
23 connection to the switched-varactor array.

24 125. Peckham generally teaches an oscillator specifically designed to be a
25 radio transmitter. The Peckham oscillator has control inputs to select the desired
26 frequency band as well as a single control input to fine tune the output frequency.
27 Peckham makes no mention of integration and appears to be a discrete
28 implementation.

1 126. Zuta generally teaches a frequency synthesizer architecture that uses a
2 frequency measuring unit to compare the synthesized frequency (from the
3 oscillator) to a reference frequency and make appropriate adjustments to the
4 oscillator. In the Zuta architecture, a computer calculates the required control
5 signals. As part of the calculation process, Zuta makes use of tables stored in RAM
6 or ROM defining the required control signals. Zuta teaches away from classical
7 PLL synthesizers because of the undesired PLL lock time. Zuta uses a single-ended
8 structure of its oscillator combining switched inductors and switched capacitors
9 along with a varactor for fine tuning driven by a single analog control signal
10 derived from a D/A converter whose input comes from the computer. Switched
11 inductors are generally a bad idea because switches are resistive and, as a result,
12 lower the Q (the quality factor) of the inductor. The Zuta oscillator would never be
13 implemented in integrated form for this very reason.

14 127. Rasmussen teaches a ring oscillator comprising differential delay cells
15 implemented using an LC tank. The delay cell also incorporates varactor diodes for
16 the capacitance portion of the LC tank and the varactors are tuned with a voltage
17 signal common to all of the delay cells.

18 128. Craninckx generally teaches a PLL-based frequency synthesizer for
19 integrated wireless communications applications. The oscillator described by
20 Craninckx is a differential LC tank structure using a tapped inductor where the
21 capacitance portion of the LC tank comprises two varactor diodes sharing a
22 common cathode where the single control signal is applied.

23 129. Mori in view of Hester: Murgulescu states that it would have been
24 obvious to replace CVD1 of Mori with the apparatus shown by Hester. CVD1 is
25 the "fine" control in the Mori oscillator. However, Hester's switched-capacitor
26 would implement coarse control requiring digital inputs where only voltage, V_{D1} , is
27 available to control CVD1. In addition, Murgulescu relies on the Craninckx
28 reference throughout his report. While Craninckx offers useful insight as to the

1 application of switched capacitors, he actually teaches away from the use of
2 switched capacitors in continuously tuning VCOs. (See Craninckx at p. 163).

3 130. Oba in view of Hester: Murgulescu states that it would have been
4 obvious to replace X1 of Oba with the apparatus shown by Hester. Oba's, X1 is the
5 "fine" control in the Oba oscillator. Hester's switched-capacitor would implement
6 coarse control requiring digital inputs where only voltages, V_a and V_c are available
7 to control X1. In addition, Murgulescu relies on the Craninckx reference elsewhere
8 in the report. While Craninckx offers useful insight as to the application of
9 switched capacitors, he actually teaches away from the use of switched capacitors
10 in continuously tuning VCOs. (See Craninckx at p. 163).

11 131. Rasmussen in view of Hester: Murgulescu states that it would have
12 been obvious to place the Hester variable capacitor at node 46 of the Rasmussen
13 delay cell. Firstly, Rasmussen implements a ring oscillator. A POSITA would not
14 have chosen the Rasmussen oscillator to address the problem solved by the '011
15 patent because ring oscillators have low Q and poor noise performance compared to
16 classical LC oscillators. Secondly, Rasmussen discloses using a fully-differential
17 delay cell so that the delay through the cell is balanced for rising and falling inputs.
18 By placing the Hester capacitor at node 46 of Rasmussen, the delay cell would
19 become imbalanced adversely affecting the performance of the oscillator. In
20 addition, Murgulescu relies on the Craninckx reference elsewhere in the report.
21 While Craninckx offers useful insight as to the application of switched capacitors,
22 he actually teaches away from the use of switched capacitors in continuously tuning
23 VCOs. (See Craninckx at p. 163).

24 132. Mori in view of Todsen: Murgulescu states that it would have been
25 obvious to replace CVD1 of Mori with the apparatus disclosed by Todsen. Todsen
26 is implemented in MOS technology and Mori is not, and thus a POSITA would not
27 be motivated to substitute Todsen's capacitors and control signals into Mori.
28 Moreover, CVD1 is the "fine" control in the Mori oscillator. Todsen's switched-

1 capacitor would implement coarse control requiring digital inputs where only
2 voltage, V_{D1} , is available to control CVD1. In addition, Murgulescu relies on the
3 Craninckx reference elsewhere in the report. While Craninckx offers useful insight
4 as to the application of switched capacitors, he actually teaches away from the use
5 of switched capacitors in continuously tuning VCOs. (*See Craninckx at p. 163*).

6 133. Oba in view of Todsens: Murgulescu states that it would have been
7 obvious to replace X1 of Oba with the apparatus disclosed by Todsens. Todsens is
8 implemented in MOS technology and Oba is not, thus a POSITA would not be
9 motivated to substitute Todsens's capacitor and control signals into Oba. Moreover,
10 X1 is the "fine" control in the Oba oscillator. Hester's switched-capacitor would
11 implement coarse control requiring digital inputs where only voltages, V_a , V_b and
12 V_c are available to control X1. In addition, Murgulescu relies on the Craninckx
13 reference elsewhere in the report. While Craninckx offers useful insight as to the
14 application of switched capacitors, he actually teaches away from the use of
15 switched capacitors in continuously tuning VCOs. (*See Craninckx at p. 163*).

16 134. Rasmussen in view of Todsens: Murgulescu states that it would have
17 been obvious to place the Todsens variable capacitor at node 46 of the Rasmussen
18 delay cell. Firstly, Rasmussen implements a ring oscillator. A POSITA would not
19 have chosen the Rasmussen oscillator to address the problem solved by the '011
20 patent. Secondly, Rasmussen has used a fully-differential delay cell so that the
21 delay through the cell is balanced for rising and falling inputs. By placing the
22 Todsens capacitor at node 46 of Rasmussen, the delay cell would become
23 imbalanced adversely affecting the performance of the oscillator. In addition,
24 Murgulescu relies on the Craninckx reference elsewhere in the report. While
25 Craninckx offers useful insight as to the application of switched capacitors, he
26 actually teaches away from the use of switched capacitors in continuously tuning
27 VCOs. (*See Craninckx at p. 163*).

28 135. Prakash in view of Oba: While Oba teaches a VCO with a plurality of

1 analog control signals, neither Oba nor Prakash teach the origin of the source of an
2 additional control signal required by Oba as an input and by the claim language.
3 Without a source for a plurality of control signals, the combination would not work.
4 In fact, Murgulescu admitted this fact in his deposition testimony. (*See* Murgulescu
5 Deposition Transcript at 166:5-9). Oba requires the inductor chokes at the control
6 nodes of the varactor diodes in order to isolate the low-impedance control voltage
7 from the signal node at the diode at frequencies of interest. Assuming multiple
8 control signals were derived from the charge pump (which is not taught by either
9 reference), a solution resulting from replacing the capacitor circuits of Prakash with
10 the capacitor circuits of Oba would be very costly in terms of the added inductor
11 chokes. For these reasons, the combination of Prakash and Oba will not work.

12 136. Zuta in view of Oba: Murgulescu states that it would have been
13 obvious for a POSITA to add element block 2 from Oba to the Zuta apparatus, but
14 he does not say where it would be added or how. Zuta teaches a Power Amplifier
15 in the oscillator circuit. Oba does not. Zuta derives analog control from a D/A
16 converter whose input comes from a computer. Zuta teaches a very complex
17 architecture (Central Processing Unit, RAM/ROM, software arithmetic unit, Digital
18 to Analog converter). With such complexity and capability, a POSITA would have
19 no motivation to combine Oba with Zuta because Oba does not offer any new
20 feature or capability that Zuta does not already have. If multiple analog signals
21 were required to tune a circuit such as Oba's, multiple D/A converters would be
22 required. This adds cost, power, and complexity to the Zuta architecture which
23 already addresses coarse and fine tuning effectively without modification.

24 137. Peckham in view of Oba: Murgulescu argues that it would have been
25 obvious for a POSITA to add element block 2 from Oba to the Peckham apparatus.
26 This makes no sense. A POSITA would know that to achieve multiple input analog
27 control, he could simply take Peckham and control varactors 327 and 328 with
28 separate analog inputs. There would be no motivation to include the circuit from

1 Block 2 of Oba.

2 138. Prakash in view of Mori: Murgulescu argues it would have been
3 obvious to substitute Block 2 of Mori into Prakash. Block 2 of Mori is a D/A
4 converter. Adding a D/A converter to Prakash fails to address any claim language
5 from the '011 Patent. I can only assume that this is an error and Murgulescu
6 intended to make some other argument. Any other conclusion would be difficult
7 because the difference between the two architectures would make for a non-obvious
8 inclusion of Mori into Prakash. The structure of the Mori oscillator is entirely
9 different than the Prakash oscillator. For example, the Mori oscillator is single
10 ended whereas the Prakash oscillator is differential. While Mori teaches a VCO
11 with a plurality of analog control signals, Prakash does not teach the origin of the
12 source of an additional control signal required by Mori as an input and by the claim
13 language. Without a source for a plurality of control signals, the combination
14 would not work. The Mori oscillator isolates the variable capacitors (varactors) at
15 high frequency with inductor chokes and at low frequency with capacitors. No
16 similar structure exists in Prakash, so a POSITA would have no hint whatsoever as
17 to how to combine Mori with Prakash. Even if it were possible, it would be costly
18 due to the added inductor chokes. As noted previously (*see above*, Paragraph 135)
19 Murgulescu stated in his deposition that the chokes of Oba could not be replaced
20 with a wire. For these reasons the combination of Prakash and Mori will not work.

21 139. Zuta in view of Mori: Murgulescu argues that it would be obvious to
22 substitute Block 2 of Mori into Zuta. Block 2 of Mori is a D/A converter. Adding
23 a D/A converter to Zuta fails to address any claim language from the '011 Patent. I
24 can only assume that this is an error and Murgulescu intended to make some other
25 argument. Any other conclusion would be difficult because the difference between
26 the two architectures would make for a non-obvious inclusion of Mori into Zuta.
27 Zuta derives analog control from a D/A converter whose input comes from a
28 computer. If multiple analog signals were required to tune a circuit such as Zuta's,

1 multiple D/A converters would be required. This adds cost, power, and complexity
2 to the Zuta architecture which already addresses coarse and fine tuning effectively
3 without modification.

4 140. Peckham in view of Mori: Murgulescu argues that it would be
5 obvious to substitute Block 2 of Mori into Peckham. Block 2 of Mori is a D/A
6 converter. Adding a D/A converter to Peckham fails to address any claim language
7 from the '011 Patent. I can only assume that this is an error and Murgulescu
8 intended to make some other argument. Any other conclusion would be difficult
9 because the difference between the two architectures would make for a non-obvious
10 inclusion of Mori into Peckham. Murgulescu argues that a POSITA would use
11 Mori to accomplish frequency control using multiple analog inputs. This makes no
12 sense. A POSITA would know that to achieve multiple input analog control, he
13 could simply take Peckham and control varactors 327 and 328 with separate analog
14 inputs. There would be no motivation to include the circuit from Mori.

15 141. Prakash in view of Craninckx: Craninckx teaches a VCO with a
16 single analog control signal. Neither Craninckx nor Prakash teach "a second set of
17 variable capacitor circuits...each variable capacitor circuit having at least one
18 control node configured to receive a control signal" (US7353011, Col 32, Ln 3-6),
19 thus neither alone or in combination meet the required claim language.

20 142. Prakash in view of Rasmussen: Murgulescu argues that it would have
21 been obvious for a POSITA to add the control signals of Rasmussen to Prakash to
22 control the capacitances because the Rasmussen capacitances were added (and they
23 would need their respective control signals). Murgulescu never argues for the
24 inclusion of the capacitors from Rasmussen into the oscillator of Prakash so it is
25 impossible to comprehend where the control signals of Rasmussen would be
26 applied. Accepting, on its face, that Rasmussen I_{BIAS} "determines an amount of
27 capacitance" (it does not), there is no indication where it would be applied to the
28 phantom capacitors included from Rasmussen. Murgulescu fails to explain how a

1 POSITA would include the Rasmussen capacitors and thus fails to explain how a
2 POSITA would derive controls for these phantom devices. Murgulescu's argument
3 fails on every level.

4 143. Zuta in view of Rasmussen: Murgulescu argues that it would have
5 been obvious for a POSITA to add the control signals of Rasmussen to Zuta to
6 control the capacitances because the Rasmussen capacitances were added (and they
7 would need their respective control signals). Murgulescu never argues for the
8 inclusion of the capacitors from Rasmussen into the oscillator of Zuta so it is
9 impossible to comprehend where the control signals of Rasmussen would be
10 applied. Accepting, on its face, that Rasmussen I_{BIAS} is a frequency control signal
11 (it is not), there is no indication where it would be applied to the phantom
12 capacitors included from Rasmussen. Murgulescu fails to explain how a POSITA
13 would include the Rasmussen capacitors and thus fails to explain how a POSITA
14 would derive controls for these phantom devices. Murgulescu's argument fails on
15 every level.

16 144. Peckham in view of Rasmussen: Murgulescu argues that it would
17 have been obvious for a POSITA to add the control signals of Rasmussen to
18 Peckham to control the capacitances because the Rasmussen capacitances were
19 added (and they would need their respective control signals). Murgulescu never
20 argues for the inclusion of the capacitors from Rasmussen into the oscillator of
21 Peckham so it is impossible to comprehend where the control signals of Rasmussen
22 would be applied. Accepting, on its face, that Rasmussen I_{BIAS} "determines an
23 amount of capacitance" (it does not), there is no indication where it would be
24 applied to the phantom capacitors included from Rasmussen. Murgulescu fails to
25 explain how a POSITA would include Rasmussen capacitors and thus fails to
26 explain how a POSITA would derive controls for these phantom devices.
27 Murgulescu's argument fails on every level.

28 **6.2.1 The '761 Patent is not obvious over various combinations of**

1 **Mori, Rasmussen, Rajkanan, and Oba.**

2 145. Mori generally teaches a voltage controlled oscillator operating within
3 a PLL with two analog control inputs. One of the inputs is derived from the charge
4 pump based on the phase difference between the reference frequency and the VCO
5 output frequency and functions as the fine control of the oscillator. The other
6 analog control input is derived from the difference in the reference frequency and
7 the VCO frequency as measured by the response at the output of the charge pump
8 and functions as coarse control of the oscillator. Mori is not specific as to the
9 technology used in his implementation, but it is clear that MOS technology was not
10 used. Mori is either bipolar technology or discrete.

11 146. Oba generally teaches a voltage controlled oscillator with two analog
12 inputs where each of the inputs affects the resulting frequency at different,
13 effectively making one of the inputs a fine control and the other coarse control.

14 147. Rasmussen teaches a ring oscillator comprising differential delay cells
15 implemented using an LC tank. The delay cell also incorporates varactor diodes for
16 the capacitance portion of the LC tank and the varactors are tuned with a voltage
17 signal common to all of the delay cells.

18 148. The claim language of the '761 Patent requires that the plurality of
19 analog signals be derived from the phase difference between a first signal derived
20 from the output signal and a second signal. Mori fails to meet this claim element
21 alone because only one of the analog control signals meets this claim element while
22 the other does not as it is derived from a difference in frequency between the first
23 and second signals. Therefore Mori fails to be suitable for any combination with
24 other references but will be analyzed nonetheless.

25 149. The claim language of the '761 Patent requires that the plurality of
26 analog signals be derived from the phase difference between a first signal derived
27 from the output signal and a second signal. Oba fails to meet this claim element
28 alone because Oba does not teach a phase locked loop architecture or any other

1 mechanism for controlling the analog voltages used in Oba. While Oba does
2 mention that a voltage controlled oscillator might be incorporated in a phase locked
3 loop synthesizer, Murgulescu admitted that some phase locked loops do not require
4 phase detectors. (*See Murgulescu Deposition Testimony at 151: 11-21*). If
5 Murgulescu is correct in this regard, then a phase detector is not implied by the
6 mere presence of a phase locked loop and thus does not teach signals "derived from
7 the phase difference." Therefore Oba fails to be suitable for any combination with
8 other references but will be analyzed nonetheless.

9 150. Rajkanan generally teaches how to implement a MOS capacitor to
10 achieve a low voltage coefficient. Rajkanan recites various capacitor
11 implementations from prior art and then describes his invention of a capacitor with
12 a low voltage coefficient. Nowhere in Rajkanan is there any indication that the
13 prior art capacitor or the invented capacitor is useful as a voltage-variable capacitor.
14 In fact, Rajkanan teaches away from such a device. Murgulescu specifically recites
15 Fig. 1 from Rajkanan as a useful non-varactor diode voltage-variable capacitor.
16 Murgulescu offers no argument for its usefulness in this regard (no indication of
17 capacitance vs. voltage performance). Moreover, if Rajkanan achieved a useful
18 voltage variable capacitor, it would suffer from a low quality factor due to the
19 substrate resistance. Moreover, in the structure offered from Rajkanan, the p-
20 substrate would be necessarily connected to ground so that its only use would be as
21 a ground-referenced voltage variable capacitor. The Rajkanan capacitor in Fig. 1
22 has one terminal connected to ground, has a significant undesirable series
23 resistance, and has no known dependence of capacitance to voltage. It is known
24 that when the series resistance in a capacitor decreases, Q increases. Murgulescu
25 confirmed this well-known relationship between series resistance and Q for a
26 capacitor. (*See Murgulescu Deposition Testimony at 83:11-13*). Thus a POSITA
27 would not look to Rajkanan to find a useful voltage variable capacitor exhibiting
28 high Q for synthesizer applications.

1 151. Mori in view of Rasmussen: Claim 1 of the '761 Patent recites a
2 variable frequency LC oscillator using non-varactor diodes as the variable-capacitor
3 component. Murgulescu cites Mori's oscillator in view of Rasmussen to meet this
4 claim limitation. Mori uses varactors and in fact, so does Rasmussen (Col 1, Ln 54-
5 56). Thus Mori in view of Rasmussen does not address the claim language
6 required.

7 152. Mori in view of Rajkanan: Murgulescu argues that a POSITA would
8 use the Mori oscillator and replace the varactors with Fig. 1 from Rajkanan. As
9 noted earlier, (*see above*, Paragraph 150) in the description of the Rajkanan
10 invention, Fig. 1 is a capacitor with a poor quality factor, is ground referenced (one
11 terminal must be connected to ground), and has an undisclosed performance in
12 terms of capacitance versus voltage. Murgulescu suggests that it would be obvious
13 for a POSITA to replace CVD2 of Mori with element 10 in Fig. 1 from Rajkanan.
14 If a POSITA did this, Mori would not work because L1 (the L of the LC tank)
15 would be short circuited to ground. A POSITA would never try this (and thus
16 break Mori) because a POSITA would have no expectation of success since
17 Rajkanan teaches away from the very thing the POSITA would try to achieve (that
18 is, a voltage variable capacitor).

19 153. Oba in view of Rasmussen: Claim 1 of the '761 Patent recites a
20 variable frequency LC oscillator using non-varactor diodes as the variable-capacitor
21 component. Murgulescu cites Oba's oscillator in view of Rasmussen to meet this
22 claim limitation. Oba uses varactors and, in fact, so does Rasmussen (Col 1, Ln 54-
23 56). Thus Oba in view of Rasmussen does not address the claim language required.

24 154. Oba in view of Rajkanan: Murgulescu argues that a POSITA would
25 use the Oba oscillator and replace the varactors with Fig. 1 from Rajkanan. As
26 noted earlier (*see above*, Paragraph 150) in the description of the Rajkanan
27 invention, Fig. 1 is a capacitor with a poor quality factor, is ground referenced (one
28 terminal must be connected to ground), and has an undisclosed performance in

1 terms of capacitance versus voltage. Murgulescu suggests that it would be obvious
2 for a POSITA to replace X and X1 of Oba with element 10 in Fig. 1 from
3 Rajkanan. If a POSITA did this, Oba would not work (shorting the X and X1
4 anodes to ground eliminates the plurality of control voltages, the capacitance vs.
5 voltage is unknown and likely not useful, and the substitution would result in low
6 quality factor). A POSITA would never try this (and thus break Oba) because a
7 POSITA would have no expectation of success since Rajkanan teaches away from
8 the very thing the POSITA would try to achieve (that is a voltage variable
9 capacitor).

10 155. Mori in view of Oba: Murgulescu states that a POSITA would find it
11 obvious to replace Mori's VCO 13 of Fig. 10 with Oba Fig. 1. A POSITA would
12 have no motivation nor see any benefit from such a substitution. Mori already has a
13 VCO with multiple analog control signals and both VCOs fail to meet the "non-
14 varactor diode" claim language.

15 **6.3.1 The '055 Patent is not obvious over various combinations of**
16 **Prakash, Mori, Yamashita, Cranineckx , and Oba.**

17 156. Mori generally teaches a voltage controlled oscillator operating within
18 a PLL with two analog control inputs. One of the inputs is derived from the charge
19 pump based on the phase difference between the reference frequency and the VCO
20 output frequency and functions as the fine control of the oscillator. The other
21 analog control input is derived from the difference in the reference frequency and
22 the VCO frequency as measured by the response at the output of the charge pump
23 and functions as coarse control of the oscillator. Mori is not specific as to the
24 technology used in his implementation, but it is clear that MOS technology was not
25 used. Mori is either bipolar technology or discrete.

26 157. Oba generally teaches a voltage controlled oscillator with two analog
27 inputs where each of the inputs affects the resulting frequency at different,
28 effectively making one of the inputs a fine control and the other coarse control.

1 158. Prakash generally teaches a PLL using a VCO operable in multiple
2 narrowly defined frequency bands. The VCO comprises a differential switched
3 varactor array that has a single analog control. Coarse tuning is achieved via the
4 switched-varactor array, and fine tuning is achieved via the single common
5 connection to the switched-varactor array.

6 159. Craninckx generally teaches a PLL-based frequency synthesizer for
7 integrated wireless communications applications. The oscillator described by
8 Craninckx is a differential LC tank structure using a tapped inductor where the
9 capacitance portion of the LC tank comprises two varactor diodes sharing a
10 common cathode where the single control signal is applied.

11 160. Yamashita generally teaches a voltage-controlled oscillator (VCO)
12 with band switching capability. Yamashita's oscillator uses varactor diodes
13 configured to allow for a band-switching input voltage and a fine-tuning input
14 voltage derived from the output of the phase-locked loop (PLL) loop filter.
15 Yamashita demonstrates use of the VCO in a PLL architecture.

16 161. Prakash in view of Craninckx: Craninckx teaches an LC oscillator
17 tuned by two varactor diodes connected in series between the differential output
18 nodes of the oscillator. Murgulescu invented a circuit configured similarly to the
19 Craninckx oscillator (US5937340). During his deposition, Murgulescu stated that
20 the two varactors (Cs) in Fig. 1 of US5937340 were connected in series. (See
21 Murgulescu Deposition Transcript at 52: 24-25, 53: 1-4). Murgulescu's
22 explanation as to the connectivity the two Cs devices in his invention informs as to
23 a correct understanding of two similarly connected devices in Craninckx—in both
24 cases, they are connected in series, not in parallel. Therefore Craninckx does not
25 meet the claim language: "a plurality of parallel connected continuously variable
26 capacitor circuits" because the Craninckx capacitors are connected in series. The
27 two varactors are controlled by a single control signal, V_C . Thus Craninckx fails to
28 meet the claim language, which requires "a plurality of different control signals."

1 Craninckx does not disclose anything more than what Prakash discloses, so a
2 POSITA would not look to Craninckx to add extra features to Prakash.

3 162. Prakash in view of Mori: Searching for additional control signals in
4 Prakash, Murgulescu proposes Mori as a source for those signals. In order to read
5 Claim 12 of the '055 Patent on Mori, the following claim element must be met: "a
6 plurality of parallel connected continuously variable capacitor circuits." In order to
7 force Mori into this claim language, Murgulescu argues that C_{VD2} , C_C , L_B , C_5 , C_3 ,
8 R_A , R_B , C_1 , C_2 , R_C , C_A , C_B , R_D , and T_r are in parallel with C_4 , C_{VD1} , and L_A . The
9 plain and ordinary meaning of "parallel connected" for a two-terminal devices
10 would be that each device would share a single node in common. The IEEE
11 Dictionary (IEEE Std 100-1996) defines "parallel" as "Two-terminal elements are
12 connected in parallel when they are connected between the same pair of nodes."
13 This meaning of parallel is consistent with what is taught in the specification of the
14 '055 Patent. Mori fails to address the deficiencies of Prakash in their
15 combination.

16 163. Prakash in view of Oba: Murgulescu suggests that a POSITA would
17 be motivated to combine Oba and Prakash. Oba is a single-ended design whereas
18 Prakash is differential. The configuration of the capacitor circuits (varactors) in
19 Oba are suited for a single-ended design. No teaching is given as to how these
20 would be adapted to the differential design of Prakash. There are benefits to
21 differential circuits (e.g., reduced common-mode noise, wider signal swing, etc.)
22 that are not available in single-ended designs, and thus a POSITA would not have
23 considered Oba while looking to enhance Prakash. Moreover, using Oba in
24 Prakash would require a plurality of inductor chokes as taught by Oba and these
25 would add to the complexity, size, and cost of the combination.

26 164. Prakash in view of Yamashita: Murgulescu suggests that a POSITA
27 would be motivated to combine Yamashita and Prakash. Yamashita is a single-
28 ended design whereas Prakash is differential. The configuration of the capacitor

1 circuits (varactors) in Yamashita are suited for a single-ended design. No teaching
2 is given as to how these would be adapted to the differential design of Prakash.
3 There are benefits to differential circuits that are not available in single-ended
4 designs, and thus a POSITA would not have considered Yamashita while looking to
5 enhance Prakash. Moreover, using Yamashita in Prakash would require a plurality
6 of inductor chokes as taught by Yamashita and these would add to the complexity,
7 size, and cost of the combination.

8 165. Mori in view of Oba: Murgulescu states that a POSITA would find it
9 obvious to replace Mori's VCO 13 of Fig. 10 with Oba Fig. 1. A POSITA would
10 have no motivation nor see any benefit from such a substitution. Mori already has a
11 VCO with multiple analog control signals.

12 **6.4.1 The '372 Patent is not obvious over various combinations of**
13 **Razavi, Rasmussen, Dickes, Hester, and Todsen**

14 166. Hester teaches a single-ended switched capacitor array implemented
15 in MOS technology.

16 167. Todsen describes a trimmable switched capacitor array implemented
17 in MOS technology.

18 168. Rasmussen teaches a ring oscillator comprising differential delay cells
19 implemented using an LC tank. The delay cell also incorporates varactor diodes for
20 the capacitance portion of the LC tank and the varactors are tuned with a voltage
21 signal common to all of the delay cells.

22 169. Razavi generally discusses the challenges of designing synthesizers
23 for wireless applications.

24 170. Dickes generally teaches a synthesizer architecture using multiple
25 VCOs in order to provide a broader input frequency lock range. Dickes is a
26 discrete implementation of a synthesizer incorporating, among other components,
27 electromagnetic relays. Dickes uses a relaxation oscillator that is tuned by
28 adjusting the tail current of a differential switch. Dickes incorporates a

1 microprocessor, random-access memory, and read-only memory to complete the
2 synthesizer function.

3 171. Razavi in view of Rasmussen: Murgulescu argues that a POSITA
4 would use Razavi for an integrated synthesizer for wireless communication systems
5 and combine it with Rasmussen for “adjusting the capacitance amount for the
6 second capacitance circuit.” On the contrary, Razavi teaches away from the
7 Rasmussen ring oscillator, by stating “Rules number 1 and 2 have made topologies
8 such as ring oscillators and relaxation oscillators less attractive for RF applications.
9 Despite their wide tuning range, these circuits exhibit an open-loop Q in the vicinity
10 of unity while containing many noisy devices in the oscillation path.” (See Razavi,
11 p. 300, Col 1). For this reason, Rasmussen would never be considered alone or in
12 combination for a synthesizer applied to wireless applications.

13 172. Razavi/Dickes in view of Rasmussen/Hester/Todsen: Murgulescu
14 argues that a POSITA would combine the Dickes synthesizer with coarse control to
15 Rasmussen in view of Hester or Todsen for selectable capacitors. Further,
16 Murgulescu argues that a POSITA would make this combination in light of Razavi
17 for application to integrable wireless applications. This is incorrect. A POSITA
18 would flee from any combination with Rasmussen because (as noted before)
19 Rasmussen teaches a ring oscillator which is anathema to an RF synthesizer
20 designer. In addition, Murgulescu relies on the Craninckx reference elsewhere in
21 the report. While Craninckx offers useful insight as to the application of switched
22 capacitors, he actually teaches away from the use of switched capacitors in
23 continuously tuning VCOs. (See Craninckx at p. 163). Therefore, Craninckx
24 teaches away from combining Razavi/Dickes/Rasmussen with Hester or Todsen.

25 **6.5.1 The '146 Patent is not obvious over various combinations of**
26 **Kral, Craninckx, Dickes, Taketoshi, Peckham, and Parker, and Bath.**

27 173. Craninckx generally teaches a PLL-based frequency synthesizer for
28 integrated wireless communications applications. The oscillator described by

1 Craninckx is a differential LC tank structure using a tapped inductor where the
2 capacitance portion of the LC tank comprises two varactor diodes sharing a
3 common cathode where the single control signal is applied.

4 174. Dickes generally teaches a synthesizer architecture using multiple
5 VCOs in order to provide a broader input frequency lock range. Dickes is a
6 discrete implementation of a synthesizer incorporating, among other components,
7 electromagnetic relays. Dickes uses a relaxation oscillator that is tuned by
8 adjusting the tail current of a differential switch. Dickes incorporates a
9 microprocessor, random-access memory and read-only memory to complete the
10 synthesizer function.

11 175. Peckham generally teaches an oscillator specifically designed to be a
12 radio transmitter. The Peckham oscillator has control inputs to select the desired
13 frequency band as well as a single control input to fine tune the output frequency.
14 Peckham makes no mention of integration and appears to be a discrete
15 implementation.

16 176. Kral generally teaches the design of fully integrated oscillators for
17 single-chip wireless transceivers. In particular, Kral addresses the design of an RF
18 CMOS oscillator with a wide tuning range without compromising power or phase
19 noise. Kral teaches two methods to achieve wide tuning range: 1) switched tuning
20 capacitors, and 2) switched tuning inductors. The latter method (as described by
21 Kral) is switching complete VCOs with their respective inductors.

22 177. Taketoshi generally teaches a synthesizer having a plurality of VCOs
23 for expanding the range of output frequencies.

24 178. Bath teaches a multiband PLL, implemented using two VCOs. Bath
25 teaches an integrated solution.

26 179. Kral in view of Craninckx: Murgulescu argues that it would have been
27 obvious for a POSITA to use the Craninckx oscillator of Fig. 5.9 in combination
28 with the Craninckx capacitor bank of Fig. 7.1 to meet the claim elements for the

1 first controlled oscillator. A POSITA would not have been motivated to make this
2 combination because Kral already has the necessary elements in Kral Fig. 4.
3 Furthermore, while Craninckx offers useful insight as to the application of switched
4 capacitors, he actually teaches away from the use of switched capacitors in
5 continuously tuning VCOs. (*See Craninckx at p. 163*).

6 180. Dickes in view of Craninckx: Murgulescu argues that a POSITA
7 would be motivated to combine the Craninckx oscillator with the Dickes discrete
8 design of a synthesizer. Craninckx teaches a monolithic solution for a complete
9 synthesizer. A POSITA would not be motivated to extract the oscillator from
10 within Craninckx and apply it to the discrete design of Dickes for at least the
11 following reasons: 1) Dickes uses current to control the frequency of the oscillator
12 while Craninckx uses voltage, and 2) the Dickes oscillator outputs a triangle
13 waveform and Craninckx does not.

14 181. Taketoshi in view of Peckham: Murgulescu indicates that a POSITA
15 would use the Peckham oscillator for the oscillators in Taketoshi's synthesizer.
16 Taketoshi teaches an architecture with multiple VCOs where each VCO has a
17 different mean frequency (Col 2, Ln 10-11). There is no discretely controllable
18 capacitance amount (as required by the claim) in the Taketoshi VCOs and there is
19 no mechanism to generate the control signals even if Peckham were substituted into
20 Taketoshi. Moreover, the claim requires that each VCO comprise a plurality of
21 control input nodes. Taketoshi teaches a control mechanism to provide only one
22 control input node. For these reasons, a POSITA would not consider combining
23 Taketoshi with Peckham.

24 182. Taketoshi in view of Parker: Taketoshi teaches an architecture with
25 multiple VCOs where each VCO has a different mean frequency (Col 2, Ln 10-11).
26 There is no discretely controllable capacitance amount (as required by the claim) in
27 the Taketoshi VCOs and there is no mechanism to generate the control signals even
28 if Parker were substituted into Taketoshi. Moreover, the claim requires that each

1 VCO comprise a plurality of control input nodes. Taketoshi teaches a control
2 mechanism to provide only one control input node. For these reasons, a POSITA
3 would not consider combining Taketoshi with Parker.

4 183. Bath in view of Peckham: Murgulescu indicates that a POSITA would
5 use the Peckham oscillator for the oscillators in Bath's synthesizer. The Peckham
6 oscillator is implemented discretely while Bath teaches an integrated solution. A
7 POSITA would not see a readily apparent way to integrate the oscillator taught by
8 Peckham. Bath teaches an architecture with multiple VCOs where each VCO has a
9 different mean frequency (Col 2, Ln 10-11). The VCOs in Bath are fixed
10 frequency. There is no discretely controllable capacitance amount (as required by
11 the claim) in the Bath VCOs and there is no mechanism to generate the control
12 signals even if Peckham were substituted into Bath. Moreover, the claim requires
13 that each VCO comprise a plurality of control input nodes. Bath teaches a control
14 mechanism to provide only one control input node. For these reasons, a POSITA
15 would not consider combining Bath with Peckham.

16 184. Bath in view of Parker: Bath teaches an architecture with multiple
17 VCOs where each VCO has a different mean frequency (Col 2, Ln 10-11). The
18 VCOs in Bath are fixed frequency. There is no discretely controllable capacitance
19 amount (as required by the claim) in the Bath VCOs and there is no mechanism to
20 generate the control signals even if Parker were substituted into Bath. Moreover,
21 the claim requires that each VCO comprise a plurality of control input nodes. Bath
22 teaches a control mechanism to provide only one control input node. For these
23 reasons, a POSITA would not consider combining Bath with Parker.

24 **6.6.1 The '441 Patent is not obvious over various combinations of**
25 **Rasmussen, Hester, Prakash, Craninckx, Todsén, Garrity, Razavi, Brilka, and**
26 **Rotzoll.**

27 185. Craninckx generally teaches a PLL-based frequency synthesizer for
28 integrated wireless communications applications. The oscillator described by

1 Craninckx is a differential LC tank structure using a tapped inductor where the
2 capacitance portion of the LC tank comprises two varactor diodes sharing a
3 common cathode where the single control signal is applied.

4 186. Hester teaches a single-ended switched capacitor array implemented
5 in MOS technology.

6 187. Todsén describes a trimmable switched capacitor array implemented
7 in MOS technology.

8 188. Rasmussen teaches a ring oscillator comprising differential delay cells
9 implemented using an LC tank. The delay cell also incorporates varactor diodes for
10 the capacitance portion of the LC tank and the varactors are tuned with a voltage
11 signal common to all of the delay cells.

12 189. Razavi generally discusses the challenges of designing synthesizers
13 for wireless applications.

14 190. Prakash generally teaches a PLL using a VCO operable in multiple
15 narrowly defined frequency bands. The VCO comprises a differential switched
16 varactor array that has a single analog control. Coarse tuning is achieved via the
17 switched-varactor array, and fine tuning is achieved via the single common
18 connection to the switched-varactor array.

19 191. Garrity generally teaches a switched capacitor array with scaled
20 capacitor sizes and respective switches scaled in a corresponding way.

21 192. Brilka generally describes an oscillator for application to video signal
22 demodulation. The Brilka oscillator uses a differential LC tank and a two varactor
23 diodes driven by a single analog control signal.

24 193. Rotzoll generally describes a voltage-controlled oscillator with both
25 analog and digital control inputs. Frequency is tuned by switching in (or out)
26 varactor diodes driven by a single analog control signal.

27 194. The Rasmussen delay cell fails to meet the following limitation from
28 Claims 1, 7, 18, 21, 25, and 30: “a plurality of analog signals as inputs.” A POSITA

1 would not interpret I_{BIAS} of Rasmussen as an analog signal input
2 “controlling...capacitor circuits” of the Rasmussen oscillator. Therefore,
3 Rasmussen in any combination fails to meet the claim limitations of the ’441
4 Patent. Even in light of this, combinations with Rasmussen will be analyzed.

5 195. The Rotzoll oscillator fails to meet the following limitations from
6 Claims 1,7, 18, 21, 25, and 30: “a plurality of analog signals as inputs.” A POSITA
7 would not interpret V_{BIAS} of Rotzoll as an analog signal input
8 “controlling...capacitor circuits” of the Rotzoll oscillator. Therefore, Rotzoll in
9 any combination fails to meet the claim limitations of the ’441 Patent. Even in light
10 of this, combinations with Rotzoll will be analyzed.

11 196. Rasmussen in view of Hester in view of Garrity: Murgulescu argues
12 that a POSITA would be motivated to use the Hester switched capacitor array in the
13 Rasmussen oscillator and size the switches based on the teaching of Garrity. The
14 Rasmussen delay cell is a fully differential design whereas the Hester capacitor
15 array is ground referenced. According to Rasmussen, the differential capacitance is
16 adjusted to achieve the desired effects. Given that a differential capacitance would
17 be required, a POSITA would not look to Hester’s single-ended (ground-
18 referenced) capacitor for substitution or inclusion into the Rasmussen delay cell.
19 Moreover, Craninckx teaches away from using the capacitors similar to Hester and
20 Todsén. While Craninckx offers useful insight as to the application of switched
21 capacitors, he actually teaches away from the use of switched capacitors in
22 continuously tuning VCOs. (See Craninckx at p. 163). Moreover, as ordered by
23 the court “weighted with respect to each other” is to be construed as “the
24 capacitances associated with the plurality of capacitors circuits are different from
25 each other and weighted based on a mixed-radix weighting scheme.” The Hester
26 binary-weighted switched capacitors exhibit a ratio that are in powers of 2. In order
27 to exhibit a mixed radix, the ratio of at least some of the switched capacitors would
28 have to be of a power other than 2.

1 197. Rasmussen in view of Todsen in view of Garrity: Murgulescu argues
2 states that a POSITA would be motivated use the Todsen switched capacitor array
3 in the Rasmussen oscillator and size the switches based on the teaching of Garrity.
4 The Rasmussen delay cell is a fully differential design whereas the Todsen
5 capacitor array asymmetrical. Because the Todsen array places switches on only
6 one side of the capacitor, the fully differential design of Rasmussen would be
7 imbalanced. A POSITA would know not to do this and would not be motivated to
8 include Todsen in the Rasmussen delay cell. Moreover, as ordered by the court
9 “weighted with respect to each other” is to be construed as “the capacitances
10 associated with the plurality of capacitors circuits are different from each other and
11 weighted based on a mixed-radix weighting scheme.” The Todsen binary-weighted
12 switched capacitors exhibit a ratio that are in powers of 2. In order to exhibit a
13 mixed radix, the ratio of at least some of the switched capacitors would have to be
14 of a power other than 2.

15 198. Rasmussen in view of Craninckx in view of Prakash: Murgulescu
16 argues that a POSITA would use the Rasmussen oscillator and the switched
17 capacitor of Craninckx using capacitors sized with guidance from Prakash. While
18 Craninckx offers Fig. 7.1 as “some implementation examples of switched tuning
19 capacitors,” Craninckx teaches away from using these switched tuning capacitors.
20 Craninckx spends several paragraphs discussing performance impact of the various
21 (a, b, and c) configurations implying that great care must be taking when applying
22 these circuits to an oscillator. Finally, Craninckx that, due to these possibly
23 detrimental performance impacts, he did not include switched capacitor banks in
24 the VCO configuration of his final phase-locked loop design. (See Craninckx at p.
25 163).

26 199. Razavi in view of Rasmussen: Murgulescu argues that a POSITA
27 would use the synthesizer in Rasmussen in the wireless communication system
28 proposed by Razavi. On the contrary, Razavi teaches away from the Rasmussen

1 ring oscillator: “Rules number 1 and 2 have made topologies such as ring
2 oscillators and relaxation oscillators less attractive for RF applications. Despite
3 their wide tuning range, these circuits exhibit an open-loop Q in the vicinity of
4 unity while containing many noisy devices in the oscillation path.” (See Razavi, p.
5 300, Col 1). For this reason, Rasmussen would never be considered alone or in
6 combination for a synthesizer applied to wireless applications.

7 200. Craninckx in view of Prakash: Murgulescu argues that a POSITA
8 would use the discretely variable circuit having binary –weighted capacitances of
9 Prakash in Craninckx. As ordered by the court, the claim element “weighted with
10 respect to each other” is to be construed as “the capacitances associated with the
11 plurality of capacitors circuits are different from each other and weighted based on
12 a mixed-radix weighting scheme.” The Prakash binary-weighted switched
13 capacitors exhibit a ratio that are in powers of 2. In order to exhibit a mixed radix,
14 the ratio of at least some of the switched capacitors would have to be of a power
15 other than 2. Therefore, this combination fails to meet this claim element.

16 201. Rotzoll in view of Brilka: Murgulescu argues that a POSITA would
17 use the Brilka oscillator in Rotzoll. The Brilka oscillator offers nothing that Rotzoll
18 does not already have. The Brilka oscillator uses a diode switch scheme controlled
19 with current sources. A POSITA would consider the Brilka switching technique
20 inferior to the simple MOS switch solution offered by Rotzoll because the Brilka
21 technique requires extra power. Therefore, this combination cannot be used to meet
22 the claimed “wireless communication system.”

23 202. Razavi in view of Rotzoll: A POSITA would not be motivated to
24 combine the Rotzoll oscillator into the Razavi wireless communication system
25 because Rotzoll does not teach the application of his oscillator to the problem
26 Razavi was solving.

27 **7 ENABLEMENT AND DEFINITENESS UNDER 35 U.S.C. § 112**
28 **– DETAILED REBUTTAL OPINION**

1 **7.1 Claim 5 of the '441 Patent is enabled**

2 203. The term “wherein at the capacitor circuits have different
3 capacitances” is enabled because a POSITA would know how to practice the
4 invention. Claim 5 recites “a plurality of capacitor circuits” and these “capacitor
5 circuits” provide the antecedent basis for “the capacitor circuits have different
6 capacitances.” A POSITA would simply understand “the capacitor circuits” to
7 have different values (“capacitances”).

8 **7.2 Claims 1 and 11 of '372 Patent are not indefinite**

9 204. Murgulescu opines that the term “circuit behavior” would leave a
10 POSITA confused because it could relate to aging, temperature, et al. On the
11 contrary, as the specification makes this clear on Col 29, Ln 21-24, “Each
12 individual capacitance circuit has a nonlinear relationship between the phase of
13 fOUT and the resulting capacitance of the one capacitance circuit. However,
14 utilizing a plurality of capacitance circuits controlled with voltages generated
15 according to the techniques described above yields a relatively linear relationship
16 between the phase and the total capacitance C_A .” The context for the term
17 “nonlinear” and “linear” as used in the specification is the relationship between
18 phase and capacitance or phase and frequency. A POSITA would understand these
19 to be “circuit behavior.”

20 205. Murgulescu further argues that “relatively linear” is indefinite.
21 Because the term appears in the context of Figs. 26-31 where the abscissa of each
22 graph is in units of time (nsec), Murgulescu argues that a POSITA would not be
23 able to understand the meaning of the term. Murgulescu argues that phase and time
24 are different and a POSITA would in no way be able to reconcile these. A POSITA
25 would have no problem understanding the relationship between phase and time. A
26 POSITA would rely on the IEEE Standard Dictionary (IEEE Std 100-1996, P765),
27 which defines phase as follows:
28

phase (1) (of a periodic phenomenon $f(t)$, for a particular value of t) The fractional part t/P of the period P through which t has advanced relative to an arbitrary origin. *Note:* The origin is usually taken at the last previous passage through zero from the negative to the positive direction. *See also:* control system, feedback; simple sine-wave quantity. (IM) [120]
 (2) (A) A distinct part of a process in which related operations are performed, as in the shift phase of a shift-and-carry operation. (B) A relative measurement that describes the temporal relationship between two signals that have the same frequency. (C) 610.10-1994
 (3) A major stage within the generating-plant life cycle. *See also:* plant life cycle. (PE) 1150-1991
 phase advancer A phase modifier that supplies leading reactive

In addition, the specification draws a relationship between time and phase in Col 27, Ln 31-32, where it offers the phrase, “a time period indicative of the phase difference.”

206. Murgulescu further posits that because the specification offers no criterion for “relatively linear” it would have no meaning to a POSITA. The term does have meaning because the word “relatively” is a modifier of the word “linear” and each of these words, alone, would be well understood by POSITA. The term “linear” has a mathematical basis in that, for example, three points in two-dimensional Cartesian space are linear if they satisfy the equation: $Y = mX + b$, where m and b are constants. The modifier of “linear” is “relatively.” It is not uncommon for a POSITA to use such a term. In fact, Murgulescu uses the term in one of his US Patent Applications (Paragraph [0022]): US 20020145481 A1. In that application, he states “as the resonant frequency of a tank circuit is *relatively* independent of the Q of the circuit.” In another patent of his, US Patent US8442476, Murgulescu uses the term in the following context (Col 3, Ln 20): “In the full-power mode, a number of analog processing stages of circuits 46, 48 are provided with performance-optimized, *relatively*-high power levels.” In another place in the same patent he states (Col 4, Ln 14): “the emitter degeneration provided by the *relatively*-high equivalent resistance.” Yet again in another place

1 in the same patent, he states (Col 4, Ln 51): “and filter circuit 68 has a *relatively*
2 steep roll-off.” Murgulescu used the term “relatively” in the context of the Q of a
3 circuit, power levels, and resistance and since he provided no objective criteria for
4 these, he expected that a POSITA would generally understand the scope of that
5 term. That is the same position I take with regards to the term “relatively linear” in
6 the ‘372 Patent.

7 207. In the broadest interpretation of the claim language, “relatively linear”
8 is understood with reference to the claim itself as Claim 1 recites “adjusting a
9 capacitance amount for a first capacitance circuit,” “further tuning...adjusting the
10 capacitance amount for the second capacitance circuit,” and finally “relatively
11 linear circuit behavior for the second capacitance circuit is achieved.” The
12 language “further tuning” relates to the tuning of the second capacitance circuit
13 after the tuning of the first capacitance circuit. The first capacitance adjustment is a
14 coarse tuning step while the second capacitance adjustment is a fine tuning step.
15 “Relatively linear circuit behavior” is achieved by virtue of the fine tuning step
16 providing more linear behavior than the coarse step alone. A POSITA would
17 understand this.

18 7.3 Claims 1 and 17 of the '011 Patent are not indefinite

19 208. Murgulescu argues that “fine tuning” is indefinite. He opines that
20 there is only one place in the specification providing a numerical hint of the
21 meaning of “fine tuning.” Murgulescu cites that place and argues that it offers no
22 guidance for interpreting the meaning.

23 209. In the paragraph at issue, Col 9, Ln 3-34, the specification offers “An
24 example will now be provided for the coarse and fine tuning that may be provided
25 by a VCO 400 according to the present invention.” The specification further
26 states: “The discretely variable capacitance (C_D) 402 may be designed to coarsely
27 tune the RF output frequency of the frequency synthesizer to about 0.1% of the
28 desired frequency of 1120.03 MHz or to within about 1 MHz.” Here the

1 specification gives indication of the meaning of “coarsely tune.” The specification
2 further states: “The continuously variable capacitance (C_A) 406 may be designed to
3 provide a frequency range of about 1% of the desired frequency of 1120.03 MHz or
4 a range of about 11 MHz, which is about 10 times the coarse tuning accuracy of the
5 discretely variable capacitance (C_D) 402.” Here the specification teaches that the
6 continuously variable capacitance, C_A , is designed to finely tune to within 1% of
7 the desired frequency. The specification subsequently states: “This frequency range
8 allows the continuously variable capacitance (C_A) 406 to finely tune the RF output
9 frequency of the frequency synthesizer.” By way of this numerical example, the
10 specification could not be more clear as to the meaning of “fine tuning,” and
11 therefore a POSITA would understand the meaning of the term in light of the
12 specification.

13 **7.4 Claims 1, 5, 7, 17, 21, and 25 of the '441 Patent are not**
14 **indefinite**

15 210. Murgulescu asserts that it is ambiguous as to what “capacitances” are
16 owned by the “capacitor circuits” in these claims. He opines that “capacitance” of a
17 “capacitance circuit” is ambiguous and that the specification offers no help in
18 understanding this.

19 211. Murgulescu is incorrect. Claim 5, for example, is very clear about the
20 apparatus. It states: “...each capacitor circuit comprising:...a capacitor...a
21 switch...a multiple-bit digital control signal...” Claim 5 teaches that a capacitor
22 circuit contains a “capacitor” and a “switch.” When Claim 5 states: “wherein at the
23 capacitor circuits have different capacitances” it would be absolutely clear to a
24 POSITA that the “capacitance” is that of the “capacitor” attached to the “switch.”

25 212. Murgulescu confounds understanding by re-defining “capacitor
26 circuit” when the claim clearly informs a POSITA as to its meaning.

27 213. Murgulescu goes on to argue (somewhat redundantly) that “wherein at
28 the capacitor circuits have different capacitances” is indefinite because there is no

1 way to assign “capacitance” to a “capacitor circuit,” and thus there is no way to
2 determine how to ascertain differences.

3 214. Finally, for the sake of argument, if I adopt Murgulescu’s complex
4 capacitor circuit that offers various different values based on switch position, all
5 that the claim requires is that the “capacitor circuit” (whatever it is) have “different
6 capacitances” regardless of how measured and at what time.

7 **7.5 Claim 18 of the ’441 Patent is not indefinite**

8 215. Murgulescu argues that a POSITA has no way to interpret the meaning
9 of “the capacitors” in Claim 18 of the ’441 Patent because the term “the capacitors”
10 does not have antecedent basis in the body of the claim. Other portions of Claim 18
11 are helpful in guiding a POSITA as to the meaning of “the capacitors” in Claim 18.

12 216. The claim states: “each capacitor circuit including a control node to
13 include or exclude capacitance associated with the capacitor circuit.” A POSITA
14 would understand from the claim that “capacitor circuit” includes a “control node”
15 that would “include or exclude capacitance associated with the capacitance circuit.”
16 Later in the claim, the phrase “to include or exclude the capacitors” contains the
17 element at issue. A POSITA, observing the parallel language from the earlier
18 element of the claim, would associate “capacitance” that was included or excluded
19 to “the capacitor” that was included or excluded. For that reason, a POSITA would
20 understand the meaning of “the capacitors.”

21 **7.6 Claims 18 and 30 of the ’441 Patent are not indefinite**

22 217. Murgulescu claims that a POSITA would not understand the meaning
23 of “capacitance associated” in Claims 18 and 30 of the ’441 Patent. He professes to
24 be confounded as to how a POSITA would understand where the capacitance might
25 be applied in a capacitor circuit. As noted before, Claim 5 gives a very clear
26 construction of the “capacitor circuit” within which is a “capacitor.” Naturally, the
27 capacitance associated with a capacitance circuit would be the capacitance of the
28 capacitor. Based on that, a POSITA would understand the meaning of “capacitance

1 associated.”

2 **11 SUMMARY OF OPINIONS**

3 218. As set forth above, I disagree with Murgulescu’s analysis and
4 conclusions regarding the validity of the patents-at-issue.

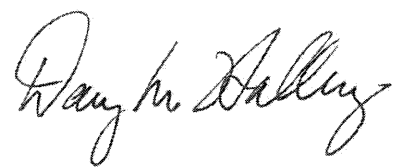
5 219. In particular, it is my opinion that the asserted claims of the patents-at-
6 issue are not anticipated by the references cited by Murgulescu and are not obvious
7 over the combinations of references cited by Murgulescu.

8 220. It is also my opinion that claim none of the asserted claims are invalid
9 for lack of enablement or indefiniteness under 35 U.S.C. § 112.

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I declare under penalty of perjury that the foregoing is true and correct.
Executed on November 2, 2015 in Austin, Texas.



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Douglas Holberg, Ph. D.

APPENDIX A
TO REBUTTAL EXPERT REPORT
OF DOUGLAS HOLBERG, PH.D.
REGARDING VALIDITY

APPENDIX A

Douglas R. Holberg, Ph.D.

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Education

B.S.E.E. - 1977, Texas A&M University, College Station, TX.

M.S.E. - 1989, The University of Texas, Austin, TX.

Ph.D. - 1992, The University of Texas, Austin, TX.

Experience

Intellectual Property Technical Consultant –

Jan 2008 – Present: Principal

Patent analysis for licensing (offensive and defensive)

Technical support for patent prosecution

Patent review for valuation

Silicon Laboratories –

Jun 2005 – Jan 2008: V. P. of Technology

Dec 2003 – Jun 2005: Director of Engineering, MCU Products

Cygnal Integrated Products - Feb. 1999 to Dec 2003 (acquired by Silicon Labs Dec 2003)

Vice President of Engineering, Chief Technical Officer, Co-founder

Concurrent to the position at Cygnal, I served as Adjunct Assistant Professor at the University of Texas at Austin, and Technical Advisory Boards for Silicon Metrics and Celite Systems.

Adjunct Assistant Professor, University of Texas at Austin – 1995-2001

Taught “CMOS Analog Circuit Design” Graduate class: EE397K and Undergraduate class: EE338L

Crystal Semiconductor Corp. - Sep. 1996 to Feb. 1999

Director of Imaging and Video Products (CCD interface, CMOS imagers, TV encoders, etc.)

Crystal Semiconductor Corp. - Oct. 1992 to Sep. 1996

Design Manager for VLSI mixed-signal products including telecommunications and disk drive read channel devices.

Independent Consultant - Aug. 1987 to Oct. 1992

Taught a short-course entitled “CMOS Analog Integrated Circuit Design” in Berlin, Germany twice per year as a part of the “Berlin Continuing Engineering Education Program.” In addition, this course was taught at Analog Devices BV, Ireland, Aug. 1990.

Lectured at Baylor University's Department of Engineering (Spring '89, Spring '91).

Consultant for Advanced Micro Devices, Crystal Semiconductor, and other companies on projects relating to switched-capacitor filters, operational amplifiers, latchup, and the ISDN analog interface.

Crystal Semiconductor Corp. - Oct. 1984 to Aug. 1987

Project leader on the CS7008 Universal Filter--a universal programmable filter using novel switched-capacitor techniques. This design was completed in a 3 μ m silicon-gate double-polysilicon CMOS process.

Texas Micro Engineering, Inc. - June 1980 to Oct. 1984

Project leader on TME3030 Sense Amplifier/Filter--a dual-channel switched-capacitor filter circuit to be used in a medical electronic application. Performed extensive device characterization of MOS transistors. This work included characterization of noise performance and characterization of transistors operating in weak inversion.

Mostek, Inc., Carrollton, TX. - Jan. 1978 to June 1980

Circuit designer. Served as project leader on MK5387 DTMF generator.

Inventions

1. 8,010,819 Microcontroller unit (MCU) with power saving mode
2. 7,719,595 Preview mode low resolution output system and method
3. 7,660,968 Reconfigurable interface for coupling functional input/output blocks to limited number of I/O pins
4. 7,613,901 Comparators in IC with programmably controlled positive / negative hysteresis level and open-drain/push-pull output coupled to crossbar switch or rising/falling edge interrupt generation
5. 7,511,465 Digital pulse width modulated power supply with variable LSB
6. 7,504,902 Precision oscillator having linbus capabilities
7. 7,504,900 Integrated circuit package including programmable oscillators
8. 7,502,883 USB integrated module
9. 7,498,962 Analog-to-digital converter with low power track-and-hold mode
10. 7,441,131 MCU with power saving mode
11. 7,421,251 Precise frequency generation for low duty cycle transceivers using a single crystal oscillator
12. 7,382,181 Method and apparatus for tuning GMC filter
13. 7,323,855 Digital pulse width modulated power supply with variable LSB
14. 7,315,200 Gain control for delta sigma analog-to-digital converter
15. 7,304,679 Preview mode low resolution output system and method
16. 7,289,145 Correlated double sampling variable gain amplifier circuit for use in a digital camera
17. 7,286,176 CCD imager analog processor systems and methods
18. 7,256,611 Cross-bar matrix with LCD functionality
19. 7,171,542 Reconfigurable interface for coupling functional input/output blocks to limited number of i/o pins
20. 7,164,311 Method and apparatus for tuning GMC filter
21. 7,061,421 Flash ADC with variable LSB
22. 6,950,047 Method and apparatus for combining outputs of multiple DACs for increased bit resolution
23. 6,922,164 SAR analog-to-digital converter with abort function
24. 6,891,487 Capacitor calibration in SAR converter
25. 6,879,004 High voltage difference amplifier with spark gap ESD protection
26. 6,724,336 Segmented D/A converter with enhanced dynamic range
27. 6,720,999 CCD imager analog processor systems and methods
28. 6,686,957 Preview mode low resolution output system and method
29. 6,617,934 Phase locked loop circuits, systems, and methods
30. 6,448,917 DAC using current source driving main resistor string
31. 6,400,300 D/A converter street effect compensation
32. 6,384,763 Segmented D/A converter with enhanced dynamic range
33. 6,288,661 A/D converter with voltage/charge scaling
34. 6,285,536 High voltage input pad system
35. 6,172,361 Methods for mounting an imager to a support structure and circuitry and systems embodying the same
36. 6,038,116 High voltage input pad system
37. 4,849,662 Switched-capacitor filter having digitally-programmable capacitive element
38. 4,492,927 Offset voltage compensation circuit
39. 4,390,754 Tone generator circuit

Currently have 26 pending applications in the PTO.

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Welland, D.; Phillip, S.; Tuttle, T.; Ka Leung; Dupuie, S.; Holberg, D, et al., "Implementation of a digital read/write channel with EEPR4 detection," *IEEE Transactions on Magnetics*, Volume: 31, Issue: 2, 1995.

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Douglas R. Holberg, Santanu Dutta, Lawrence Pillage, "DC Parameterized Piecewise-Function Transistor Models for Bipolar and MOS Logic Stage Delay Evaluation," *Proc. IEEE International Conference on Computer-Aided Design*, Nov. 1990.

Douglas R. Holberg, "Digitally Programmable Filter Based on Standard Cell Design," IEEE Analog/Digital VLSI Workshop, Sept. 1986.

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Books

Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, New York: Holt Rinehart, and Winston, ©1987.

Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd Ed, Oxford University Press, ©2002.

Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 3rd Ed, Oxford University Press, ©2011.

Other Professional Activities

Served on the "Industrial Electronics Advisory Committee" for the University of Texas Instruction and Materials Center, University of Texas, Austin, 1988-1989.

Baylor University Board of Advocates, 2001 to 2003.

Member of IEEE