



MICROELECTRONICS DIVISION

SCSI ENGINEERING NOTEBOOK

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I. NCR SCSI PRODUCT FAMILIES

NCR 5385/86 PRODUCT FAMILY

The NCR 5385, which was the first general purpose SCSI protocol controller available in the market, has been replaced by the upgraded NCR 5385E ("enhanced"). The NCR 5386 is primarily a cost reduced version of the 5385E, with a few additional features such as pass parity and the ability to suppress spurious phase changes. Shortly following the introduction of the 5386, a synchronous version (the NCR 5386S) will be available. This device is capable of supporting 3.3 Mbyte operation using a synchronous (offset of one) handshake.

In spite of continuing enhancements, these devices have maintained pin and software compatibility. Future upgrades such as higher offsets, faster transfer rates, lower power CMOS, and on-chip bus transceivers are being planned. In addition to the standard 48-pin DIP, these devices are available in 52 or 68-pin J-leaded PLCC (surface mounted) packages.

To provide a single-chip open-collector interface to the SCSI bus, the NCR 8310 General Purpose 48 mA Bus Transceiver may be used as a companion chip with any members of the NCR 5385/86 family.

A summary of the product family is listed below.

NCR 5385

- First family member
- Replaced by the NCR 5385E

NCR 5385E

- Currently in production
- Supports latest ANSC timings (Post Revision 10)
- Manufactured until the NCR 5386 is in production

NCR 5386

- Samples currently available
- Superset of the NCR 5385/85E
- Production availability 2/86

NCR 5386S

- Samples available 1/86
- Identical to NCR 5386 with synchronous operation to 3.3 Mbytes/sec

NCR 8310

- Samples available
- Production 12/85
- Single-chip open-collector bus interface

NCR 5380 PRODUCT FAMILY

The NCR 5380 was the first SCSI interface device to provide on-chip open-collector 48 mA bus transceivers. This provides for low parts count and direct SCSI bus interfacing. Since the 5380 is an NMOS device, and not susceptible to latch-up like CMOS, the single ground pin is adequate to handle 14 signals sinking 48 mA simultaneously. (When operating as a Target device, a maximum of 14 signals may be simultaneously active.) Inductance problems are avoided by purposely slowing each signals turn-on time. This provides the added benefit of reducing the RF generated due to switching signals. However, to maintain ground integrity, it is recommended that inexpensive sockets not be used.

To accommodate differential-pair operation, the 48-pin NCR 5381 can be used. This device allows use of the internal open-collector bus transceivers and provides the additional signals necessary to control external differential-pair bus transceivers.

SCSI is finding its way into lap-top computing. To provide the lowest power possible, the 53C80/81 will be introduced in the 4th quarter of 1985. Since CMOS is susceptible to latch-up, four additional ground lines have been provided. Due to this consideration, the part has maintained functional compatibility but not pin compatibility. Additionally, the REQ/ACK response time has been considerably improved over its NMOS counterpart.

All of these devices are available in standard DIP or surface mountable PLCC packaging. A summary of the devices is listed below.

NCR 5380

- On-chip open-collector bus transceivers
- Currently in production

NCR 5381

- Supports external differential-pair bus transceivers
- Samples available
- Production 12/85

NCR 53C80

- Functionally equivalent to the NCR 5380
- Samples available 11/85

NCR 53C81

- Functionally equivalent to the NCR 5381
- Samples available 12/85

CHOOSING THE RIGHT PRODUCT FAMILY FOR YOUR DESIGN

The NCR 5385/86 family and the NCR 5380 family are all fully featured SCSI protocol controller devices. Both product lines support nearly every option available in the proposed SCSI standard and can be used in a variety of configurations. However, differences between the families will make one device more appropriate than another for your application.

REASONS TO CHOOSE THE NCR 5385/86 PRODUCT FAMILY

You probably would need an NCR 5385E or NCR 5386 if the most important factors influencing your choice are:

- * Performance
- * System Integrity
- * Guaranteed Compatibility

PERFORMANCE

All members of the NCR 5385/86 product family are capable of 2.0 Mbyte/sec operation using the asynchronous SCSI handshake. The NCR 5386 provides 3.3 Mbyte/sec operation using the synchronous (offset of one) handshake. Future products in this family will support faster transfer rates and greater offsets. The NCR 5380 product family is rated at 1.5 Mbyte/sec operation and is currently not planned to support synchronous operation.

Even if your transfer requirements are less than 1.5 Mbyte/sec operation, the NCR 5380 has longer REQ/ACK response times than the combination of the NCR 5385/86 and the associated bus transceiver delay. Because of this delay, your overall transfer rate could be reduced depending on the cable length being used and the response of the other SCSI bus devices.

Additionally, the NCR 5385/86 family supports a slightly faster MPU interface. This could prevent the insertion of wait states if the device is being addressed by high-end processors.

SYSTEM INTEGRITY

Many designs have the requirement to maintain parity throughout the system. The NCR 5386 and 5386S will optionally pass, or check and pass, parity through the chip. The NCR 5380 family does not support this feature.

GUARANTEED COMPATIBILITY

The NCR 5380 product is firmware oriented thus adherence to the SCSI protocol is the responsibility of the programmer. It is impossible to violate any of the SCSI specifications using the NCR 5385/86 device.

REASONS TO CHOOSE THE NCR 5380 PRODUCT FAMILY

You probably would need an NCR 5380 or NCR 5381 if the most important factors influencing your choice are:

- * Board Space
- * Cost
- * Flexibility
- * Low-power

BOARD SPACE

The NCR 5380 family was the first SCSI interface device to include on-chip open-collector bus transceivers. By providing the high-current transceivers on-chip, fewer parts are required to implement the interface and the device pin-out requirements are reduced. Even though the 5385/86 family does not have on-chip bus transceivers, the NCR 8310 provides a convenient single-chip bus interface. Future members of the 5385/86 product line will include the bus transceivers on chip.

Another board savings feature is the absence of a clock pin. No clock circuitry, resistors, or capacitors are required to make the device operate. The exclusive process-independant, free-running internal oscillator is unique to the NCR 5380 (patent pending).

COST

The NCR 5380 and the NCR 5386 products are comparably priced, however the NCR 5386 requires an external bus transceiver. Since the NCR 5380 requires fewer parts and uses less board space, it is a less expensive solution.

FLEXIBILITY

Since the NCR 5380 is a register-oriented device and most bus signals may be freely asserted or sampled, it is capable of supporting variations of the SCSI interface such as XSASI and SCSI/PLUS. XSASI is the interface used by XEBEC on many of its products and varies slightly from the proposed SCSI standard. SCSI/Plus is a proposed superset for the SCSI interface that allows up to 64 bus devices compared to the 8 devices specified by the X3T9.2 subcommittee. This flexibility also makes it a perfect tool for use in SCSI testing, analyzing, and bus emulating equipment.

Additionally, the versatility of the NCR 5380 allows it to be used in non-SCSI applications such as industrial control busses, local I/O communication links, and other interfaces requiring 48 ma sink capability.

LOW POWER CONSUMPTION

The NCR 5380 typically draws 110 ma of current, while the NCR 53C80 draws only a few microamps. This makes them ideal products for low-power applications.

DIFFERENCES BETWEEN THE NCR 5385E AND THE NCR 5386

The NCR 5386 is primarily a cost reduced version of the NCR 5385E. Eventually, the NCR 5386 will replace the NCR 5385E since it's intended to be superset of this device. The NCR 5386, however, does have a few improvements that are significant in some implementations. The following list will help you decide if you can design with the NCR 5385E or if you need an NCR 5386 for your development. Detailed information concerning these changes may be found in the NCR 5386 SCSI Protocol Controller Data Sheet.

ITEM #1 - PASS PARITY

The NCR 5386 provides an option so that the integrity of the parity bit is maintained through the chip. In this mode, parity may be passed or checked and passed between the SCSI bus and the DMA data path.

Using this mode sacrifices pin compatibility with the NCR 5385E device. To support this operation, the ID register must be written with the appropriate device ID. Pin 14, previously ID0, may now be used for data bus parity (DP). Pins 12 and 13 in this mode are not used.

ITEM #2 - SUPPRESS SPURIOUS PHASE CHANGE INTERRUPTS

When operating as an initiator, interrupts are generated by the NCR 5385E when phase changes occur on the SCSI bus. This chip determines a phase change by sampling the phase signals (C/D, MSG, I/O) for a period of twelve clock cycles. If the phase lines have indeed changed, BSY/ is sampled for an additional twelve clocks to insure that the target is still connected.

Since the phase change interrupt can be generated before a bus request (REQ) occurs, a system could realize performance advantages if the target changed the phase lines before the actual transfer were to take place. If a disk controller received a command to read a sector of information, it may change the phase lines to a Data In phase before the data was ready to be transferred. By doing this, the host can be servicing the phase change interrupt while the disk is seeking to read the proper sector.

However, most controllers do not operate in this fashion and the scheme used by the NCR 5385E could create multiple phase change interrupts with certain products. To reduce the number of interrupts generated, the NCR 5386 provides a Valid Phase Enable bit (bit 3) in the Control Register. This bit, when set (1), causes the NCR 5386 to generate a phase change interrupt only when REQ becomes active. When this bit is reset, operation will be identical to the NCR 5385E.

ITEM #3 - EXTRA DREQ SUPPRESSED

When the NCR 5385E is transferring data in the DMA mode, DREQ will go active one additional time after the Transfer Counter reaches zero. No data is transferred for this additional DREQ and no DMA response is expected.

The NCR 5386 has been modified to suppress this additional DREQ. For most this change will be transparent in your system. However, some designs have hardware and/or software that expect this additional DREQ.

Please be aware of this change when upgrading to the NCR 5386.

ITEM #4 - TRANSFER COUNTER IN TARGET RECEIVE MODE

When operating the NCR 5385E in a Target receive mode and an exit condition occurs (Pause command issued or parity error occurred), the Transfer Counter is decremented one additional time before exiting the state machine.

The NCR 5386 has been modified so that the Transfer Counter accurately reflects the number of bytes that have been transferred. Systems that make use of this value need to be aware of this change. For most users this change is transparent.

ITEM #5 - ACCESS TO DATA REGISTER II

The NCR 5385E has a doubly-buffered data register but provides only status of and access to only one of these registers. In some applications it is important to know whether one or two bytes of data remain in the chip.

The NCR 5386 will use bit 0 of the Auxiliary Status Register as a flag for indicating that Data Register II is full. Data Register II may now be accessed by performing a CPU read to device register eight (A3-A0=1000).

ITEM #6 - PAUSE COMMAND MODIFICATION

If a Target designed with the NCR 5385E wishes to halt a Target send operation in order to change to a new bus phase, he must issue the Pause command. With the NCR 5385E, the Pause command requires that one or two bytes of data be sent to the chip before a new command can be issued.

The Target send state machine has been modified in the NCR 5386 so that a new command may be issued immediately after the Pause command.

ITEM #7 - CHANGES MADE TO ACCOMMODATE SASI AND XSASI CONTROLLERS

Several low-end controllers do not monitor BSY during the selection process. Additionally, they do not check to see if more than two ID's are active on the bus during this phase. Both conditions are requirements of the proposed ANSI specification. The NCR 5385E while moving from Arbitration into Selection, asserts SBEN/ while the data bus is tri-stated. This causes all the data signals on the SCSI bus to go active for approximately three clock cycles. During this time both BSYOUT and SELOUT are active. Since low-end controllers, such as the Xebec S1410 do not monitor BSY, but detect SEL and their ID active, they become falsely selected.

The NCR 5386 has been modified so that Xebec S1410 type controllers may be properly selected without using additional control circuitry.

Some controllers in this class also allow the phase lines to change while ACK is still active on the SCSI bus. If this phase change occurs while the Target is changing from the Status to the Message In phase, the NCR 5385E will leave ACK asserted on the SCSI bus. The chip is tricked into thinking that the Status byte just transferred was a Message In byte and leaves ACK active so that the message may be rejected. At this point an out-of-sequence Message Accepted command may be issued to de-assert ACK. The Message In byte may now be transferred.

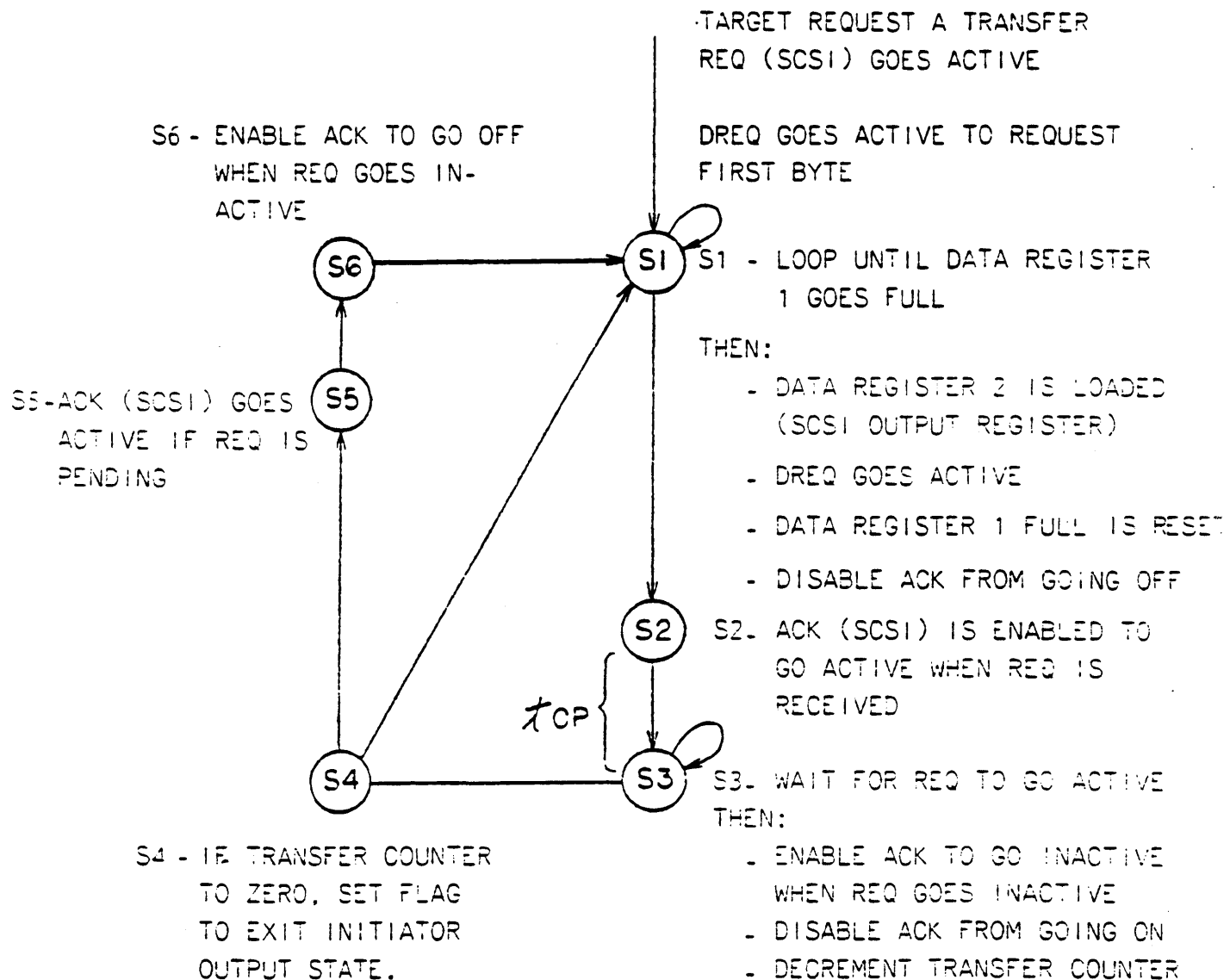
The NCR 5386 will not require this out-of-sequence Message Accepted command and ACK signal will return to its inactive state.

II. NCR 5385/86 STATE MACHINE OPERATION

- A. Initiator Output State Machine
- B. Target Receive State Machine
- C. Initiator Input State Machine
- D. Target Send State Machine

NCR 5385 STATE MACHINE OPERATION

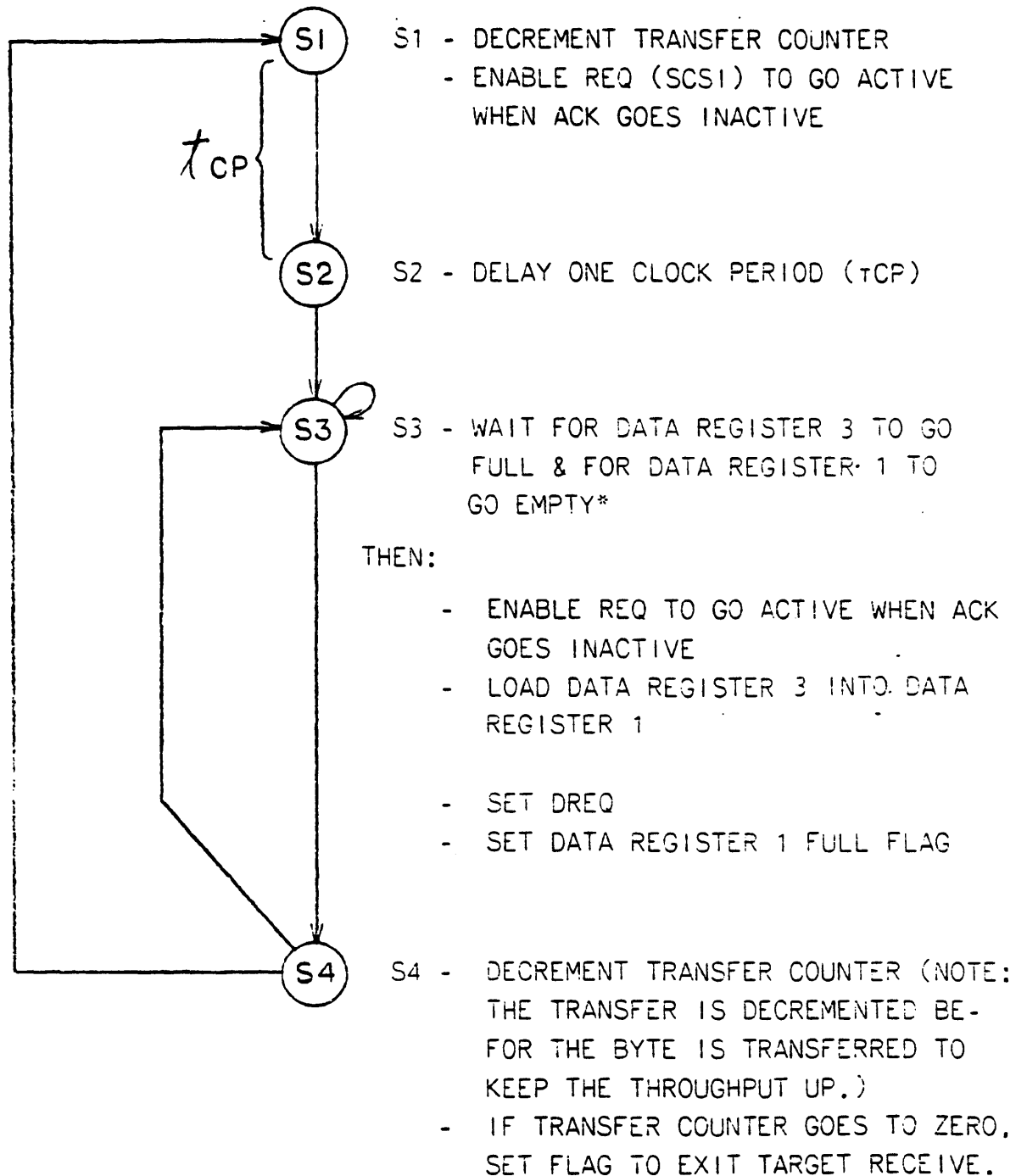
INITIATOR OUTPUT STATE MACHINE



t_{CP} = CLOCK PERIOD

$100 \text{ NS} \leq t_{CP} \leq 200 \text{ NS}$

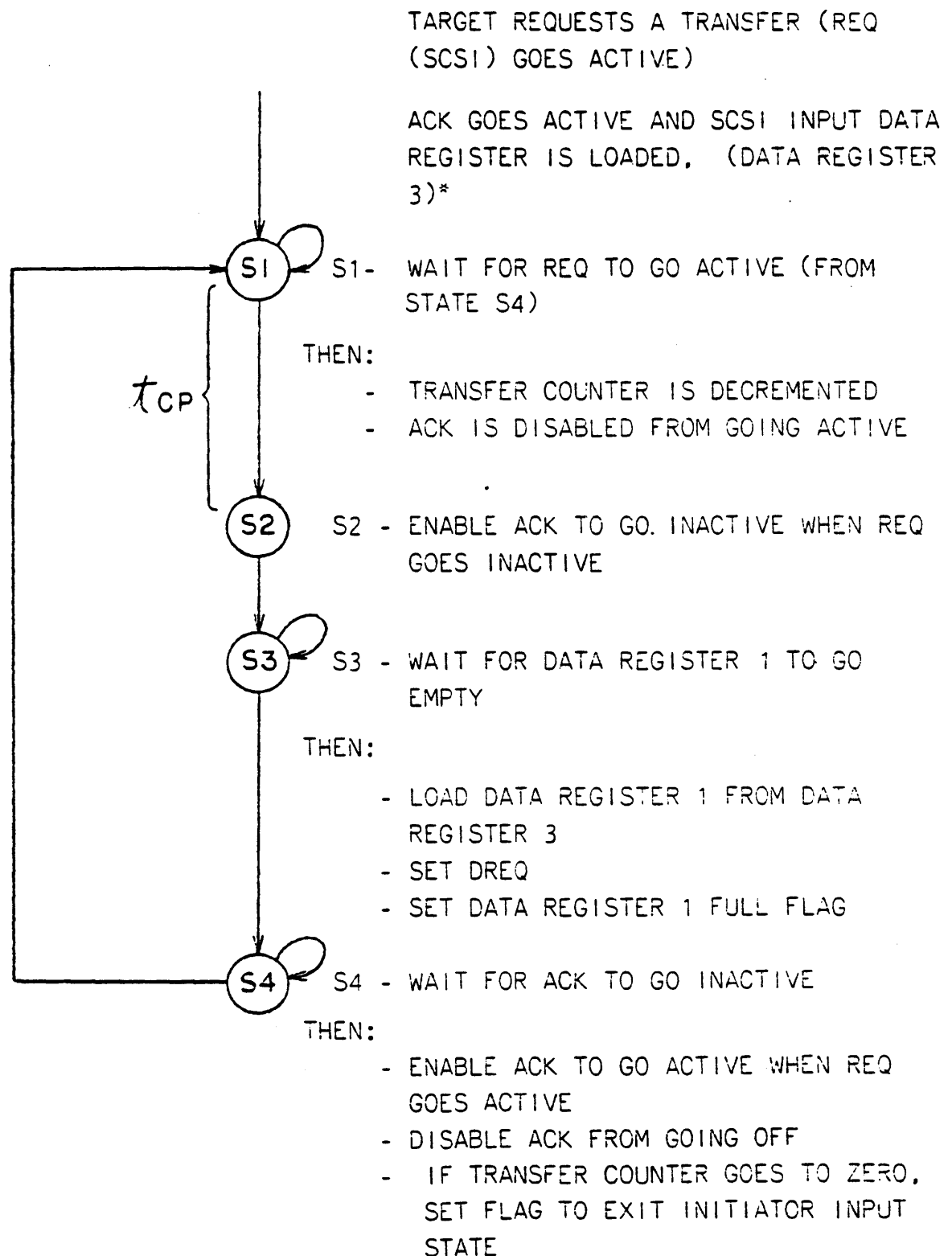
TARGET RECEIVE STATE MACHINE



t_{CP} = CLOCK PERIOD
 $100 \text{ NS} \leq t_{CP} \leq 200 \text{ NS}$

* DATA REGISTER 3 IS LOADED WHEN ACK GOES ACTIVE.

INITIATOR INPUT STATE MACHINE



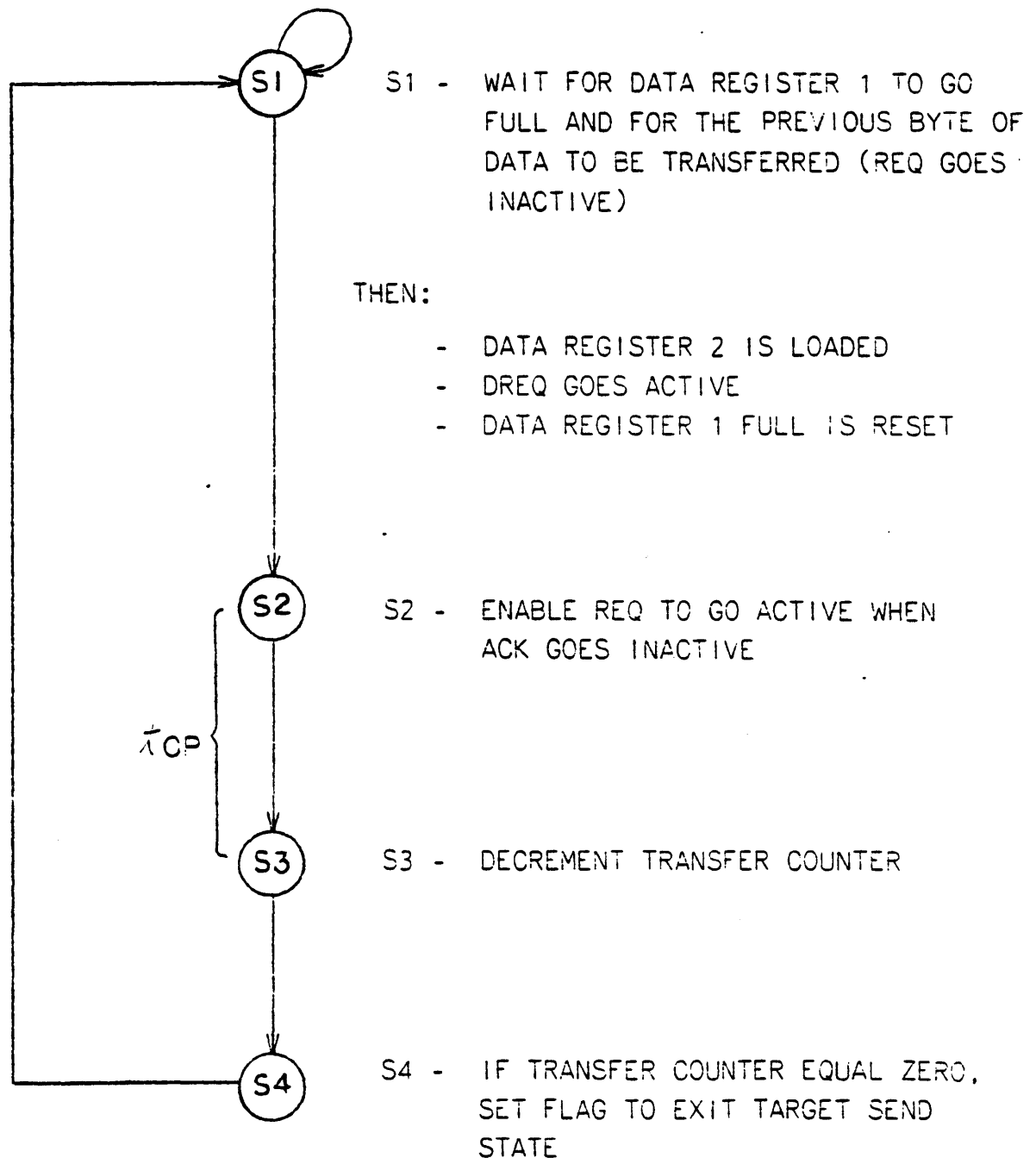
t_{CP} = CLOCK PERIOD

$100 \text{ NS} \leq t_{CP} \leq 200 \text{ NS}$

* DATA REGISTER 3 IS LOADED WHEN ACK GOES ACTIVE

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TARGET SEND STATE MACHINE



t_{CP} = CLOCK PERIOD

100 NS \leq t_{CP} \leq 200 NS

III. NCR 5385S SYNCHRONOUS OPERATION

NCR 5386S Synchronous Operation

The NCR 5386S SCSI Protocol Controller is pin and software compatible with the NCR 5385E and 5386 but may additionally be used to transfer data in a synchronous fashion. Using a 10 Mhz clock the NCR 5386S is capable of transferring data up to 3.3 MBytes/sec. The following information describes how to invoke the synchronous operation and what is required to achieve to maximum data rate.

CONTROL REGISTER

The control register is used to notify the NCR 5386S whether data phases are to be transferred synchronously or asynchronously. (NOTE: All SCSI devices must first establish that they are transferring synchronously through the SCSI message system. Also, only data phases may be transferred synchronously. This allows both synchronous and asynchronous devices to share the same bus.) Bits 4-7 of this register have been defined to support synchronous operation. The use of these bits are described below:

CONTROL REGISTER

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
1 PDM	1 TP6	1 TP5	1 SYN	1 VPE	1 PE	1 RE	1 SE
1	1	1	1	1	1	1	1
1				1	1		1
1	-----86S-----			1-86-	1	-----85E-----	
1				1	1		1

- BIT 0 Select Enable** When this bit is a "1" the chip will respond to any attempt to select it as a Target. When it is a "0", the chip will ignore all selection attempts.
- BIT 1 Reselect Enable** When this bit is a "1" the chip will respond to any reselection attempts. When set to a "0" the chip will ignore all reselection attempts.
- BIT 2 Parity Enable** When the parity enable bit is set to a "1", the chip generates and checks parity on all transfers on the SCSI bus. When this bit is not set, parity is generated but not checked.
- BIT 3 Valid Phase Enable** When this bit is set to a "1", the chip generates an interrupt for phase changes only when REQ becomes active. When bit 3 is a "0", bus service interrupts are generated if the phase lines are stable for twelve clocks and BSY is active for twelve clocks after the phase lines have stablized.

IT 4 Synchronous SCSI When this bit is set to a "1", the chip is configured to transfer all data phases across the SCSI bus using the synchronous offset of one handshake. When this bit is a zero, the chip will handshake data as the NCR 5385E and the 5386 in an asynchronous fashion.

BIT 5,6 Transfer Period The Transfer Period bits are provided so you may program the NCR 5386S to match the transfer rate of your application. These bits determine the minimum REQ cycle time and are only used when operating as a Target device. These transfer period bits are only used in synchronous data transfers.

TP6	TP5	MINIMUM REQ CYCLE TIME
0	0	3 Clock Periods
0	1	3.5 Clock Periods
1	0	4 Clock Periods
1	1	4.5 Clock Periods

BIT 7 Pulsed DMA Mode In order to achieve the maximum synchronous transfer rate the optional Pulsed DMA handshake may be used. This handshake is compatible with the flyby mode used with the AMD 9516 DMA device. The primary difference with this handshake is that the DACK/ input signal must be pulsed in response to the DREQ output. Restrictions on the DACK/ pulse are described in the synchronous timing diagrams. This mode is optional and not required for synchronous operation or evaluation but may be necessary to achieve the desired transfer rate.

IDENTIFICATION

In the ID Register Bit 6 is used to identify the device as an NCR 5386S. This read only bit notifies the controlling software that synchronous data transfers are supported. If this bit is not set then the device is either an NCR 5385E or NCR 5386.

SYNCHRONOUS TIMING DIAGRAMS

Pulsed DMA Operation

#	Name	Description	MIN	MAX	UNITS
1	tcd	CLK low to DREQ active	70	130	nsec
2	tdl	DACK/ active to DREQ low		40	nsec
3	tdd	CLK high after DREQ to DACK/ low to meet minimum cycle time (300 ns)		80	nsec
4	trd	RD/ and DACK/ concurrently active	90		nsec (75?)
5	trdl	Minimum tdd + trd to meet minimum cycle time (300 nsec)		220	nsec
	twr	WR/ and DACK/ concurrently active	60		nsec
7	twrl	Minimum tdd + twr to meet minimum cycle time (300 ns)		170	nsec

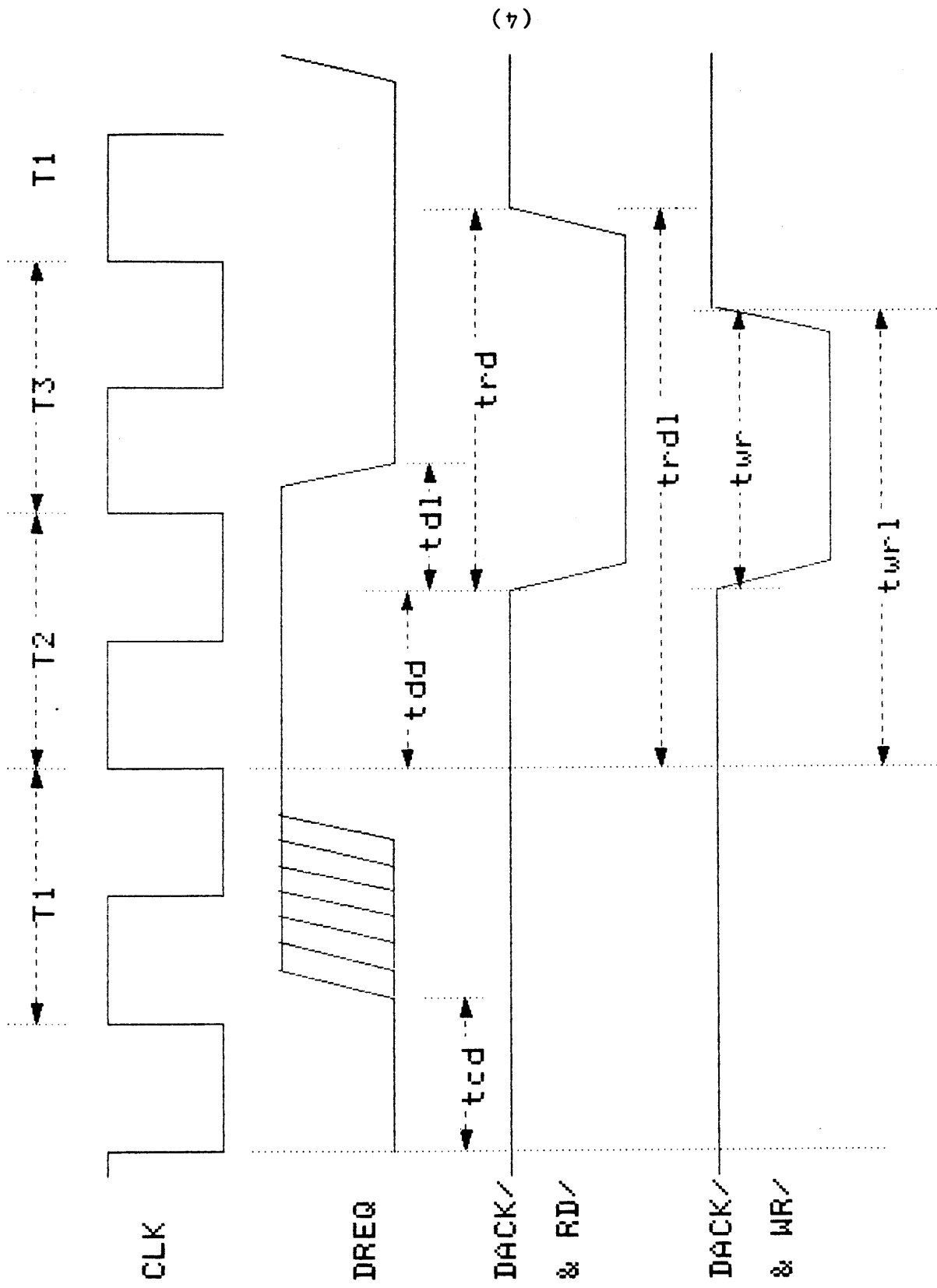


FIGURE 1 PULSED DMA OPERATION (10 MHz)

Target Role Handshake

#	Name	Description	MIN	MAX	UNITS
8	tmr	Minimum REQ assertion time	100		nsec
9	tmx	Maximum REQ assertion time		200	nsec
10	tc0	Minimum REQ cycle time (TP6,5=00)	3		Clock Periods
11	tc1	Minimum REQ cycle time (TP6,5=01)	3.5		Clock Periods
12	tc2	Minimum REQ cycle time (TP6,5=10)	4		Clock Periods
13	tc3	Minimum REQ cycle time (TP6,5=11)	4.5		Clock Periods
14	tal	ACK/ active prior to next REQ/ to meet specified transfer period	80		nsec

NOTE: A minimum deassertion period of 90 nsec on ACK/ must be meet for correct operation.

Initiator Role Handshake

#	Name	Description	MIN	MAX	UNITS
15	tra	REQ/ active to ACK/ active		70	nsec
16	tar	Minimum ACK/ assertion period	100		nsec
17	tax	Maximum ACK/ assertion period		200	nsec

NOTE: A minimum deassertion period of 90 nsec on REQ/ must be meet for correct operation.

FIGURE 2 - NCR 5386S TARGET ROLE OPERATION

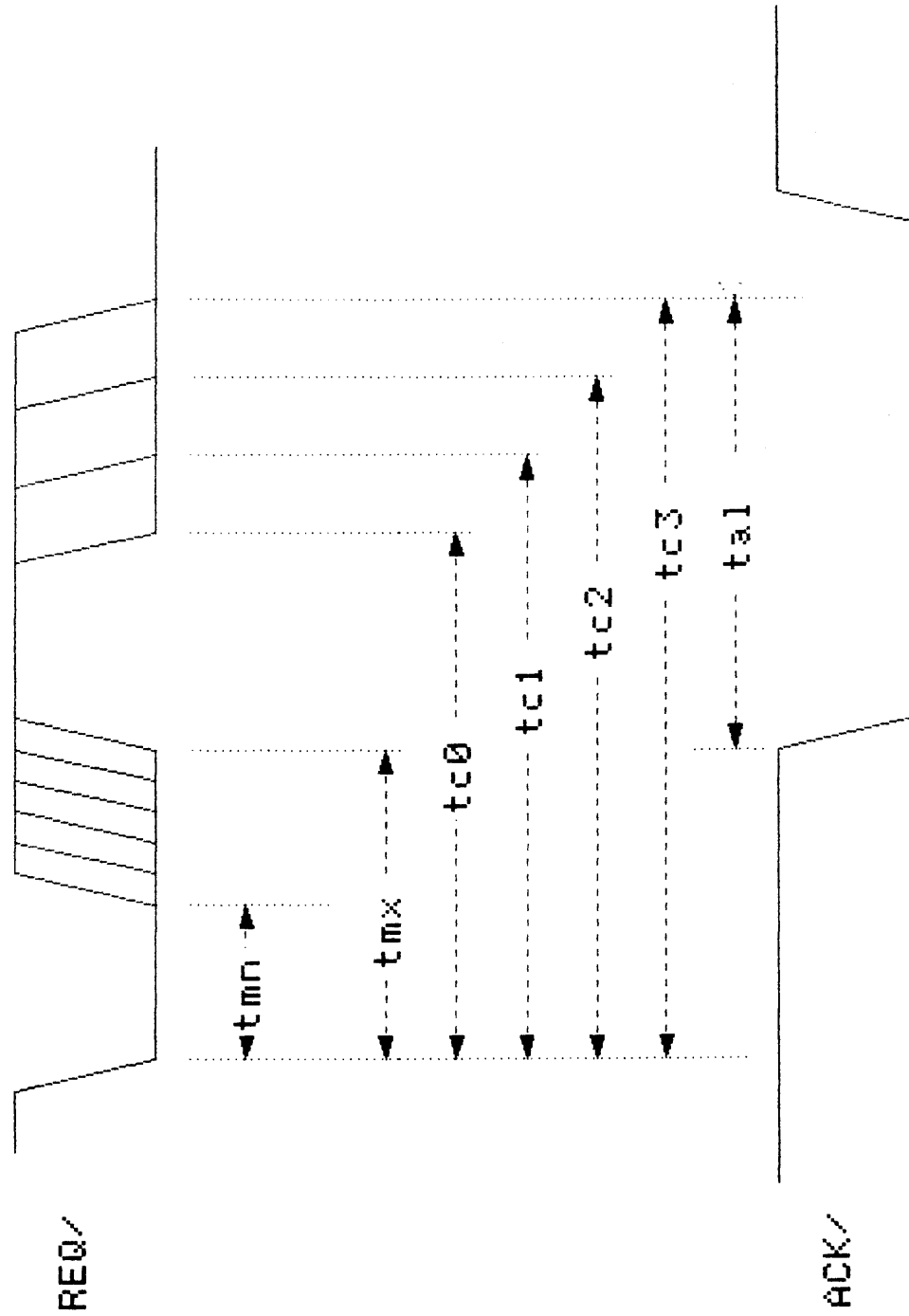
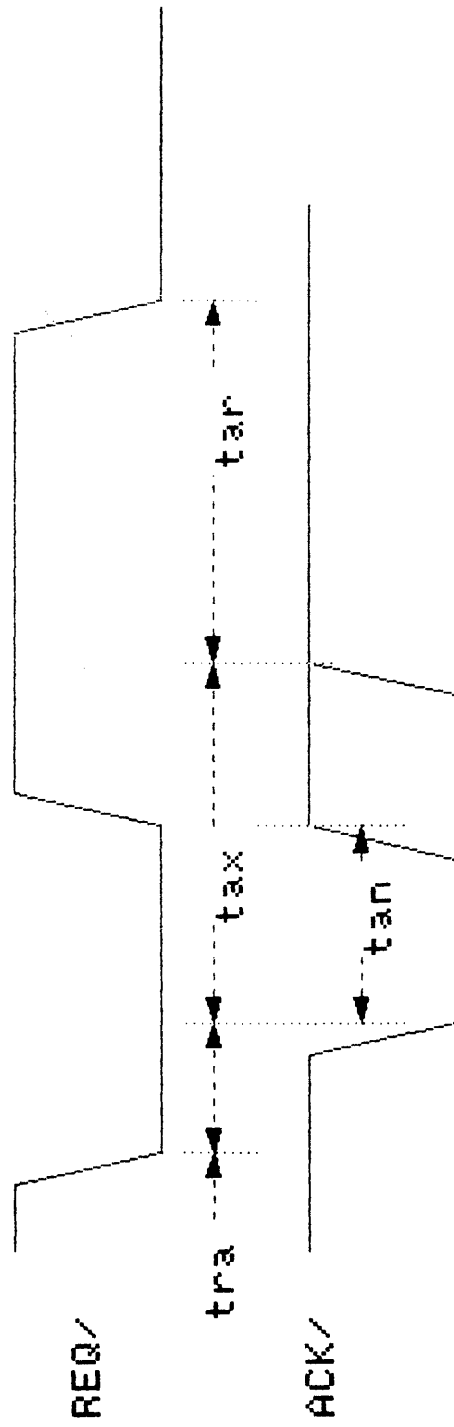


FIGURE 3 - NCR 5386S INITIATOR OPERATION



(7)

IV. SCSI ACCOMMODATES FLEXIBLE SYSTEM ARCHITECTURES

SCSI ACCOMMODATES FLEXIBLE SYSTEM ARCHITECTURES

The SCSI interface is rapidly gaining acceptance as a standard for interconnecting intelligent peripheral devices. Much of the standard's success may be directly attributed to the flexibility that the interface offers. In order to demonstrate the versatility of the SCSI standard, four unique system architectures will be described: single-user/single tasking, multi-tasking, multi-user, and multi-processing systems. These examples represent actual product offerings that span a range of computing requirements. The SCSI interface provides a readily available, cost-effective solution for the differing needs of each configuration.

SINGLE-USER/SINGLE-TASKING SYSTEMS

The personal computer products, which make up a majority of the computers sold, may be generally characterized as a single-user/single-tasking system. In these systems I/O is performed in a sequential manner. For example, if you wish to store a file to disk and then read another file from disk, you would wait for the first task to complete before the second task can be performed. Figure 1 shows a block diagram of products which represent this category.

Because the SCSI interface operates with generic device types, the system may be designed to operate with a variety of intelligent mass storage devices. This allows the user a choice

of configurations that meet his performance and storage capacity requirements.

Flexibility is important, but product cost is the primary concern for this class of computer. A hard disk drive and a controller board may account for as much as 50% of the system cost. Disk drive manufacturers have traditionally provided drive-level interfaces that interface to the host bus through a disk controller. However, with the increasing integration of controller electronics, several manufacturers are finding it less costly to provide an integrated SCSI controller directly on the disk drive.

Obviously, a single board is less expensive than two boards, plus the hardware required to interconnect the boards. Less obvious is the savings realized by achieving higher manufacturing yields on the drive's head/disk assembly. Since the disk is addressed as a logical storage device and the controller manages the surface defect mapping, the manufacturer's assembly yields are increased, thereby reducing the overall product cost.

MULTI-TASKING SYSTEMS

In single-tasking or single-threaded environments, system performance suffers due to the sequential nature of all I/O operations. Seek and rotational latencies, associated with the

disk drive, may occupy up to 70% of the time required to access a sector of information.

In single-user/multi-tasking systems, to take advantage of this "dead" time, the SCSI standard allows devices not actively transferring data to remove themselves from the bus, so that other I/O operations may be initiated. Therefore, multiple disk drives may be seeking data simultaneously, providing for higher bus utilization. The drive which locates its data first will reselect the host and complete the transfer. Figure 2 shows a block diagram of a single-user/multi-tasking system. Many workstations are being designed around this architecture.

Since these systems are more sophisticated, additional devices such as optical disks and tape back-up units may optionally be added. The SCSI bus is easily expanded to include additional devices, without occupying valuable backplane slots. Again, since the SCSI interface supports generic device types, all peripherals may be upgraded to the user's performance and storage requirements.

MULTI-USER SYSTEMS

In today's office environment, personal computers are stand-alone devices that support individual productivity requirements. However, if data needs to be shared between users, then the

system components need to be networked. Local area networks, such as Omnet, Ethernet, Arcnet and Appletalk, may be used to accomplish this interfacing task. Since data is shared between these various components, file servers are used as common storage elements. File servers, in many cases, are personal computers modified to support multi-user file management. Figure 3 shows a common file server implementation.

In some cases, the mere fact of having multiple users dramatically reduces system responsiveness, which is so important in multi-user environments. However, since the SCSI bus supports data rates at 1.5 Mbytes/sec in an asynchronous mode and up to 4 Mbytes/sec using a synchronous handshake, system performance need not suffer. This fast transfer rate coupled with the disconnect capability allows for high data throughput and efficient bus utilization. Additionally, these transfer rates match or exceed the performance of the commonly used local area networks (LANs).

The SCSI interface supports several commands to accommodate multi-user systems by providing increased system performance and shared file protection. Search commands, implemented in the file server or the disk controller, allow key words to be searched locally rather than occupying the LAN or the SCSI bus with large data transfers. These commands increase the system performance while reducing the bus bandwidth requirements. To keep shared

files from being accessed simultaneously, the Reserve and Release commands may be used to manage file activity. Reserved files are not available to other users until the files have been Released by the current users.

Aside from sharing data, file servers may be used to share expensive system resources. Laser printers, large storage devices, color plotters, and even copiers may act as shared resources in the multi-user environment. The SCSI interface allows the file server to be easily reconfigured for specific system requirements.

MULTI-PROCESSOR SYSTEMS

Systems supporting multiple operating systems, real time data acquisition, communication processors, or other dedicated processors have traditionally used backplane architectures to support their multi-processing requirements. These systems require a local communications bus as well as an intelligent peripheral interface. The SCSI interface, with its multi-host capability, provides the needed functionality at a fraction of the backplane cost. In addition to file transfers between individual processors and mass storage devices, inter-processor communications can be accomplished across the SCSI interface. Furthermore, freedom from backplane form factors provides increased design flexibility. Figure 4 shows a block diagram of a multi-processor system.

Since the SCSI interface is limited to directly supporting up to eight bus devices, this may preclude the use of the standard SCSI interface in complex multi-processing configurations. SCSI/Plus (tm) addresses this limitation by taking advantage of unused bus phases to provide a binary selection phase. Using the binary selection phase, up to 64 bus devices may be supported. SCSI/Plus is a superset of the SCSI standard and the different bus devices may co-exist on the same bus.

SUMMARY

The systems described in this article are a few of the many configurations that use SCSI as the backbone of their architectures. The standard offers the flexibility needed to incorporate a range of system requirements, spanning several-hundred-dollar personal computers to several-hundred-thousand-dollar multi-user systems. Additionally, integrated circuits, board level products, and fully integrated bus devices are readily available from a variety of manufacturers. In each product category, SCSI offers a cost-effective solution that provides the necessary performance, features and vendor uniqueness to make it a truly usable standard.

SCSI/Plus is a trademark of Ampro Computers, Inc.

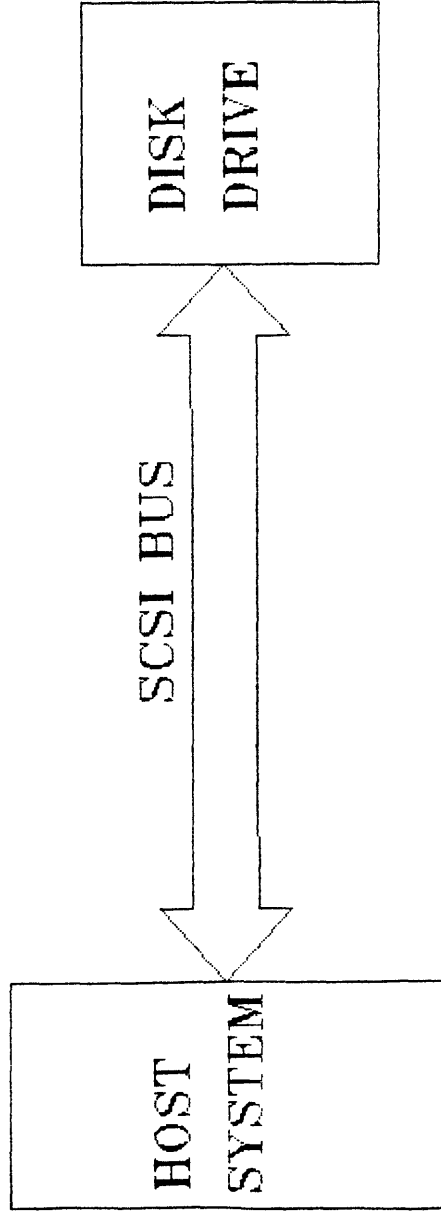


FIGURE 1 – SIMPLE SCSI CONFIGURATION

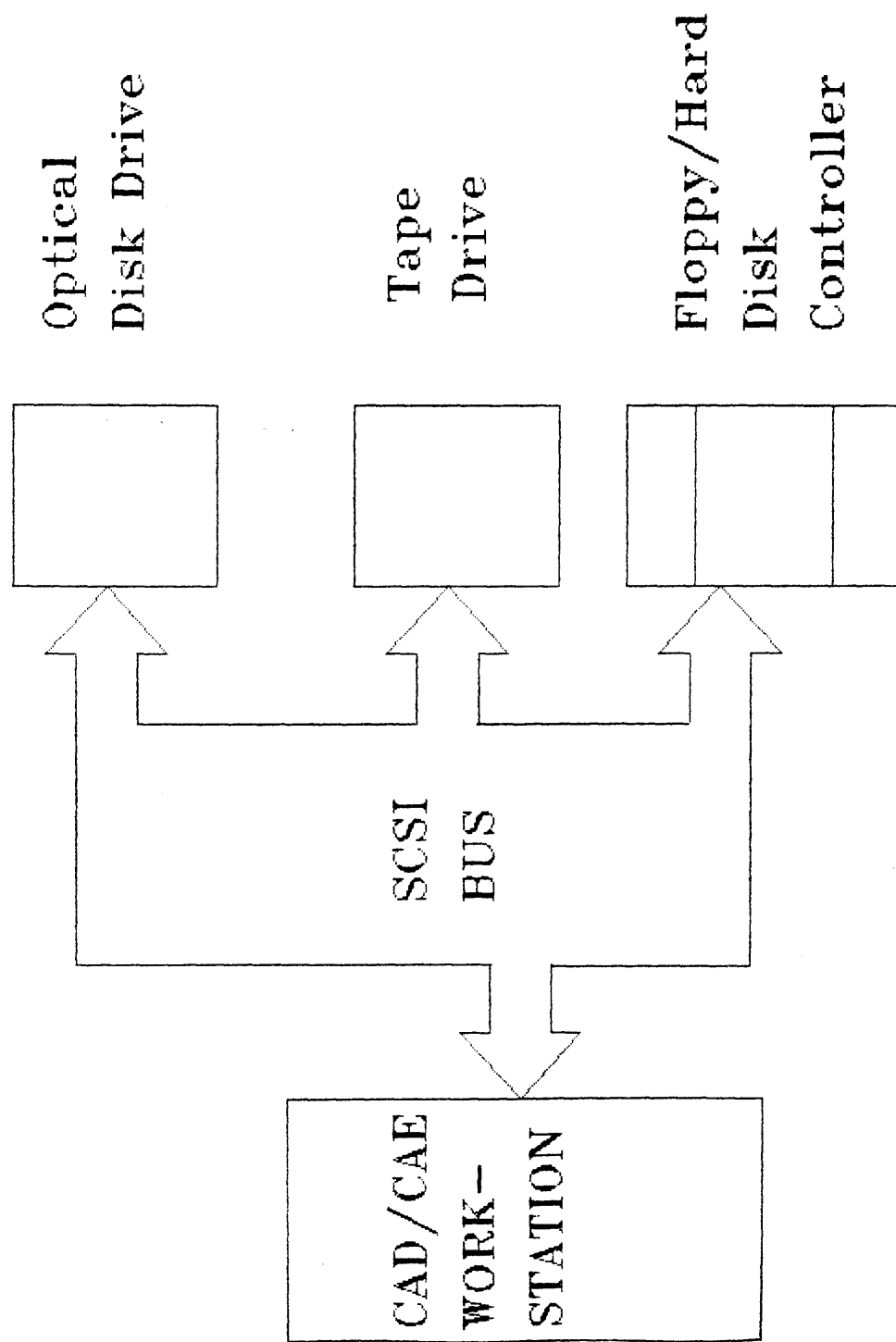


FIGURE 2 - MULTI-TASKING SCSI SYSTEM

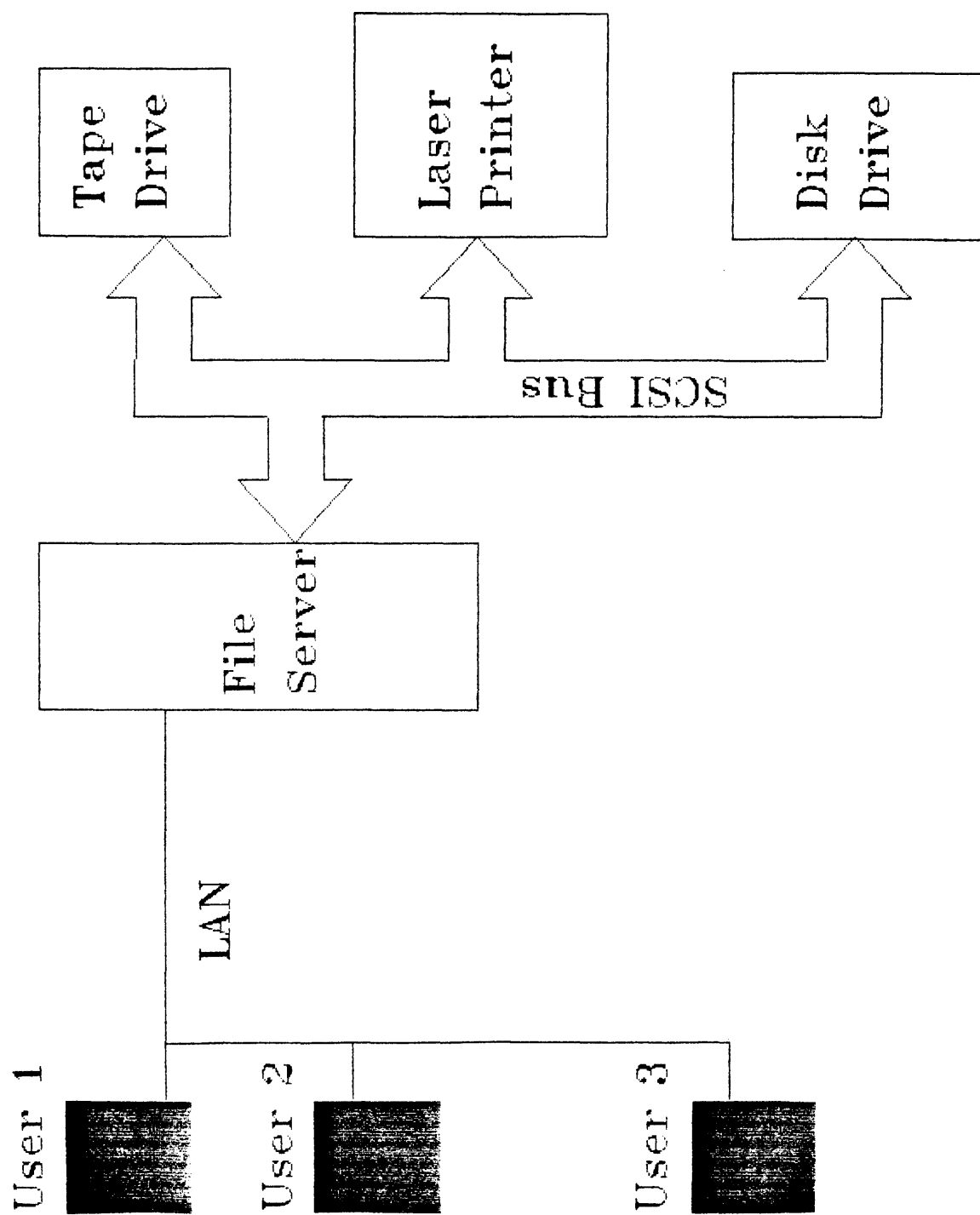


FIGURE 3 - SCSI IN A MULTI-USER SYSTEM

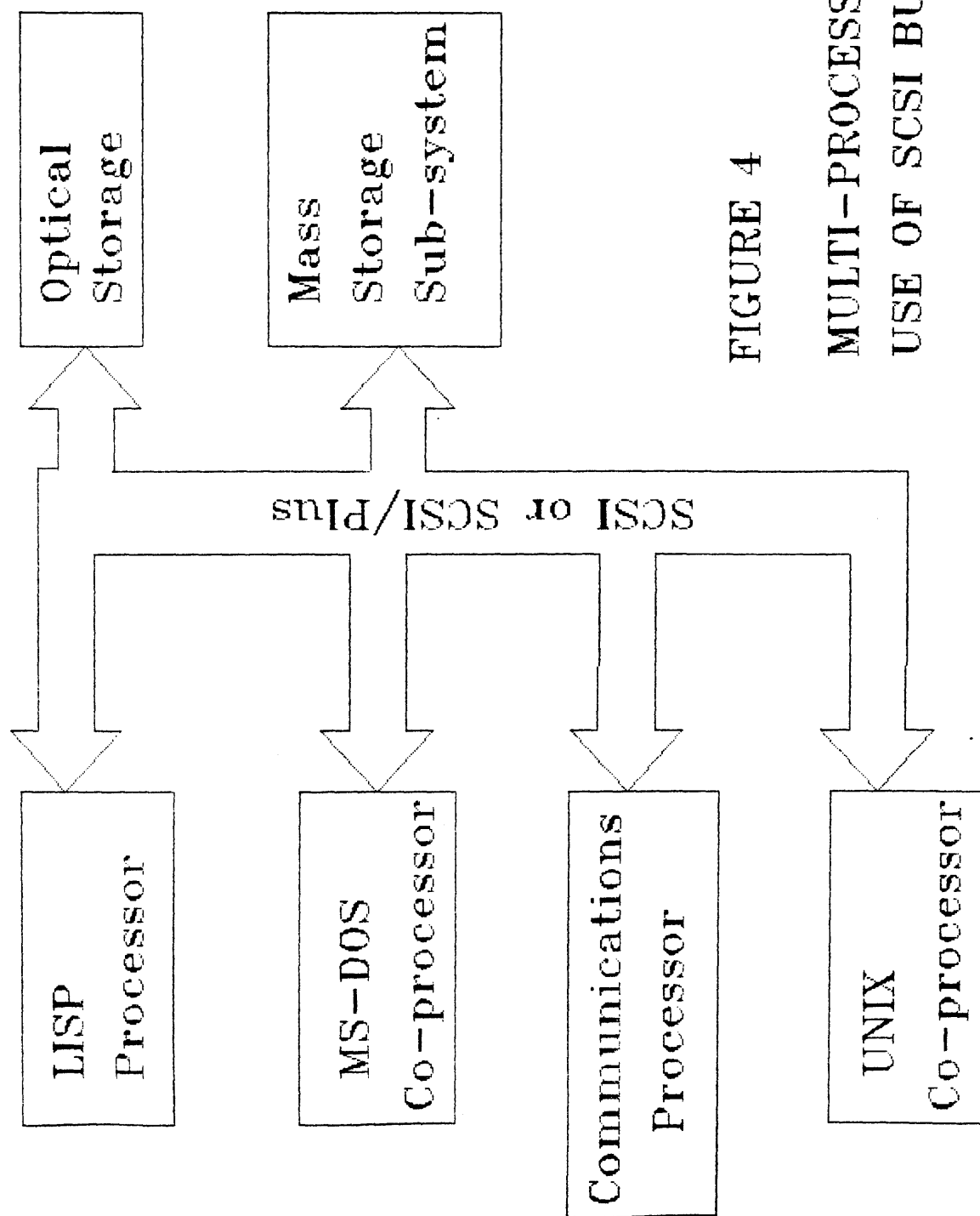


FIGURE 4
MULTI-PROCESSOR
USE OF SCSI BUS

V. SCSI PACKAGING OPTIONS

NCR MICROELECTRONICS

SCSI PRODUCTS

Listed and shown below are the packages that the NCR 5380, 5381 5385E, 5386, 5386S and 8310 SCSI products are either currently available in or will be available in. Product availability and lead-time is also shown. Please note that if a package is not listed that would be of interest to you, please contact NCR Microelectronics in Colorado Springs on (800)-525-2252 or (303)-596-5612.

NCR 5380
40 pin DIP

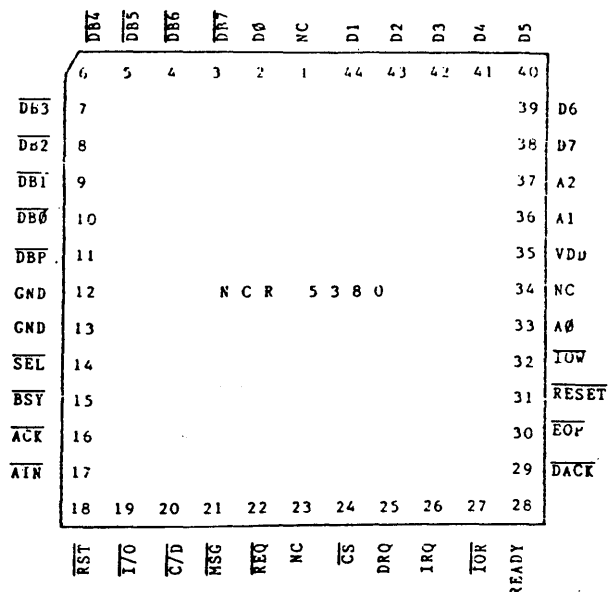
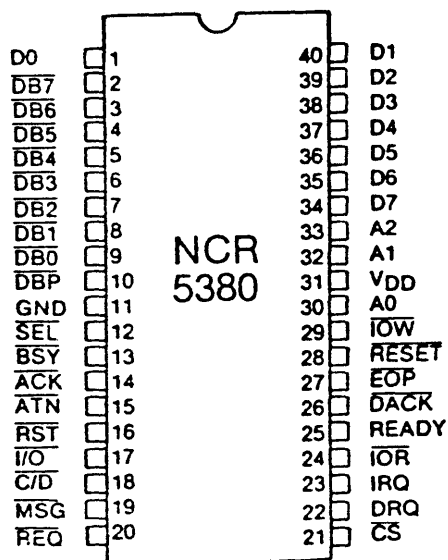
Samples: Now
Production: Now

Lead-time: 8 weeks

NCR 5380
44 pin J lead PLCC

Samples: Now
Production: January, 1986

Lead-time: 8 weeks



NCR 5381
48 pin DIP

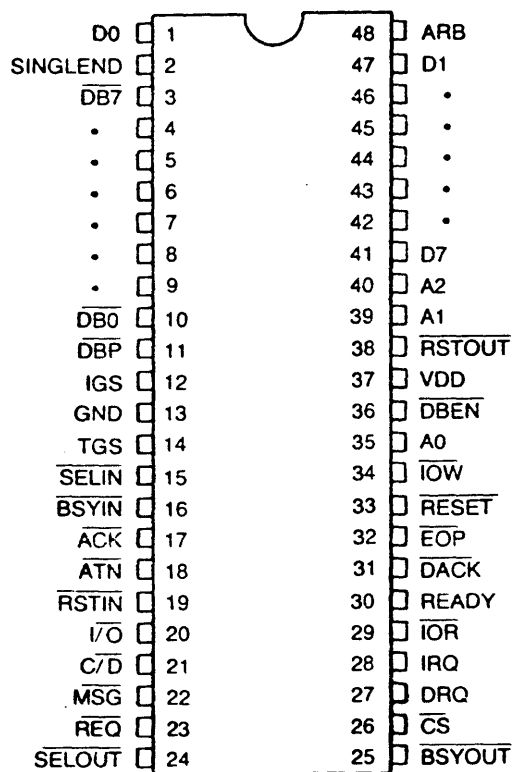
Samples: Now
Production: Now

Lead-time: 8 weeks

NCR 5381
68 pin J Lead PLCC

Samples: November, 1985
Production: January, 1986

Lead-time: 8 weeks



NCR 5385E
48 pin DIP

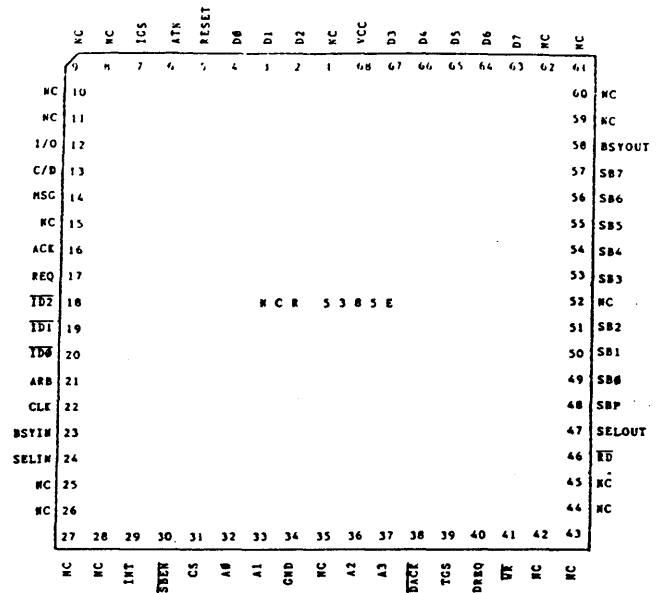
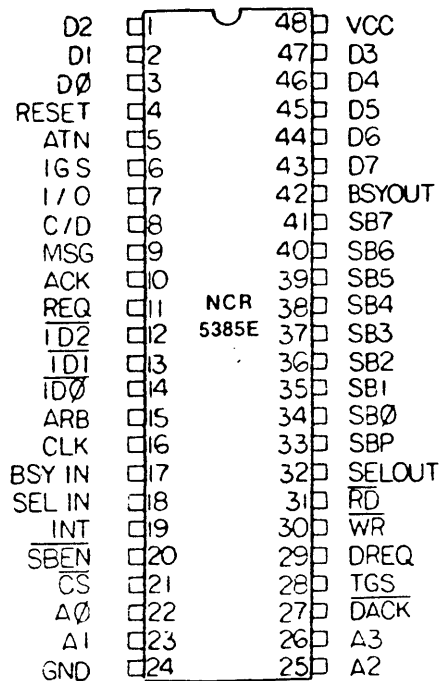
Samples: Now
Production: Now

Lead-time: 8 weeks

NCR 5385E
68 pin J-lead PLCC

Samples: November, 1985
Production: January, 1986

Lead-time: 8 weeks



NCR 5385E
52 pin J Lead PLCC

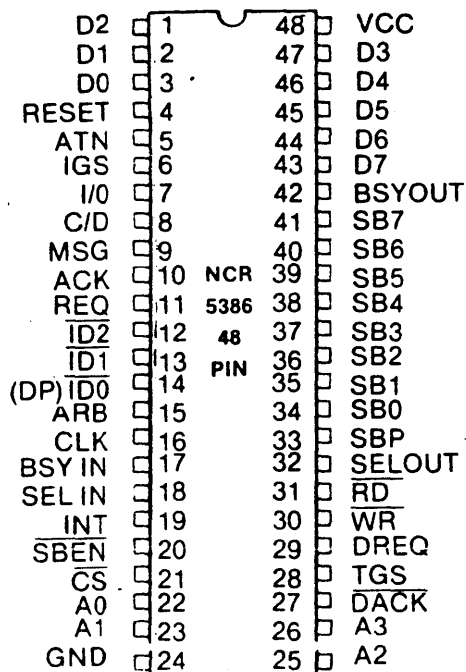
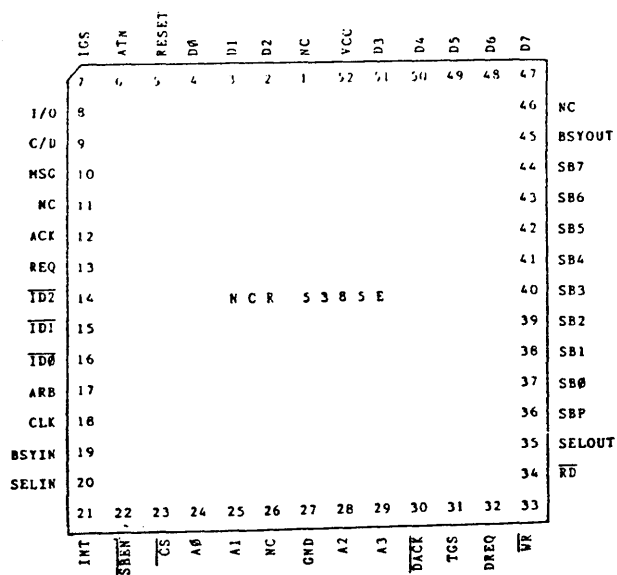
Samples: January, 1986
Production: February, 1986

Lead-time: 8 weeks

NCR 5386
48 pin DIP

Samples: December, 1985
Production: February, 1986

Lead-time: 8 weeks



NCR 5386
68 pin J Lead PLCC

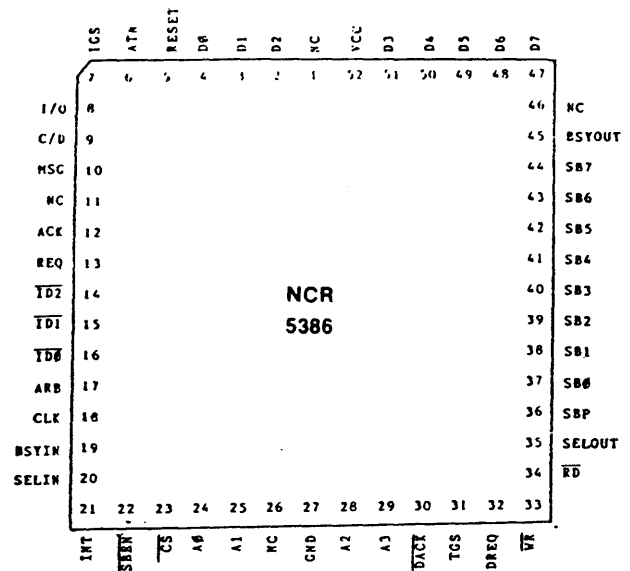
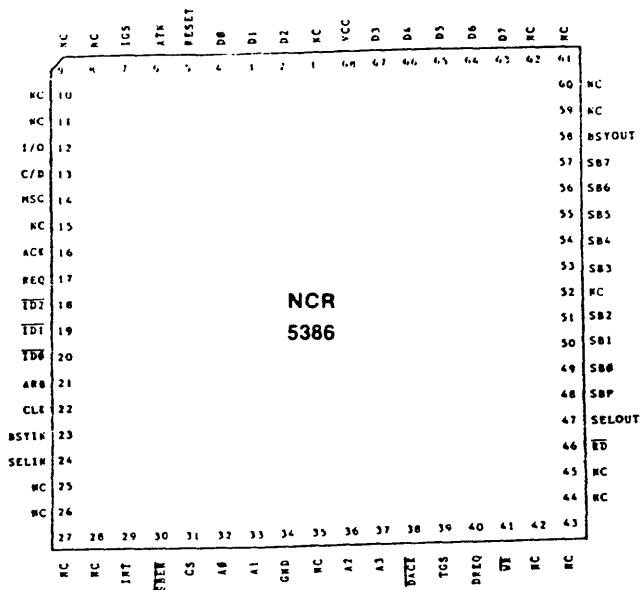
Samples: February, 1986
Production: March, 1986

Lead-time: 8 weeks

NCR 5386
52 pin J Lead PLCC

Samples: February, 1986
Production: March, 1986

Lead-time: 8 weeks



NCR 5386S
48 pin DIP

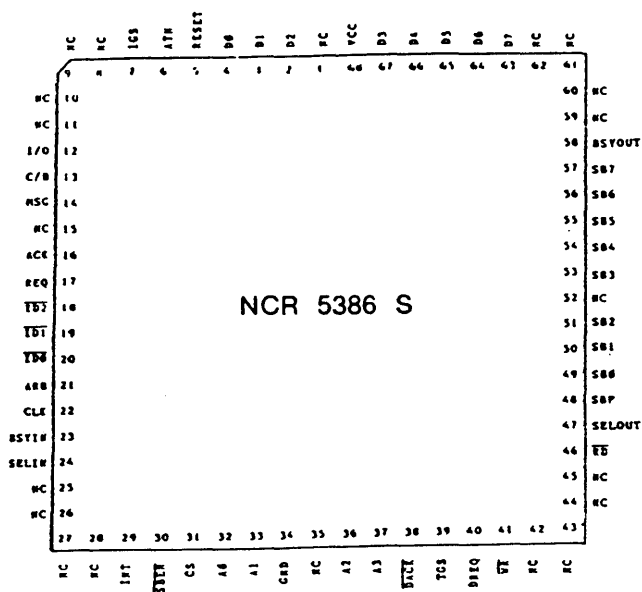
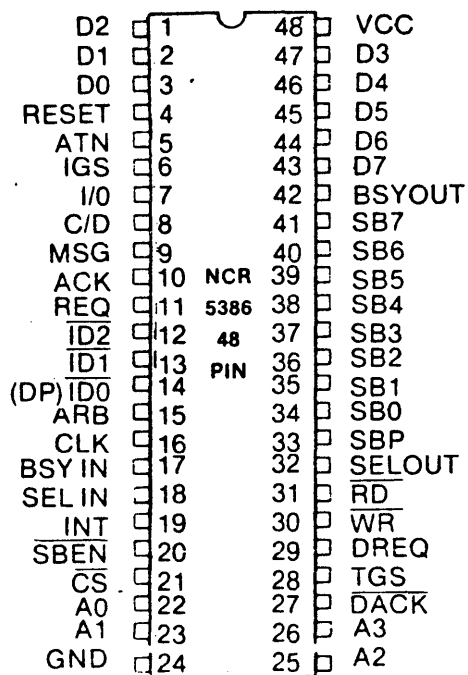
Samples: February, 1986
Production: March, 1986

Lead-time: 8 weeks

NCR 5386S
68 pin J Lead PLCC

Samples: March, 1986
Production: May, 1986

Lead-time: 8 weeks



NCR 8310
48 pin DIP

Samples: December, 1985
Production: January, 1986

Lead-time: 8 weeks

NCR 8310
68 pin J-Lead PLCC

Samples: January, 1986
Production: February, 1986

Lead-time: 8 weeks

DO	1	48	(ARBI) ENCODE (1 of 8)
DP	2	47	D1
MD7/ (DB7)	3	46	D2
MD6/ (DB6)	4	45	D3
MD5/ (DB5)	5	44	D4
MD4/ (DB4)	6	43	D5
MD3/ (DB3)	7	42	D6
MD2/ (DB2)	8	41	D7
MD1/ (DB1)	9	40	ID2/
MD0/ (DB0)	10	39	ID1/
MDP/ (DBP)	11	38	(RSTIN) EN
PAEN (PGS)	12	37	Vdd
QND	13	36	(VO) B0
PBEN (TGS)	14	35	ID0/
HF/ (SEL)	15	34	DBEN/
HG/ (BSY)	16	33	(RSTOUT) EOUT/
HA0/ (ACK)	17	32	(SELOUT) FOUT
HA1/ (ATN)	18	31	(BSYOUT) GOUT
HE/ (RST)	19	30	(ATN) A1
HB0/ (C/D)	20	29	(C/D) B1
HB1/ (C/D)	21	28	(REQ) B3
HB2/ (MSG)	22	27	(MSG) B2
HB3/ (REQ)	23	26	(ACK) A0
FIN (SELIN)	24	25	(BSYIN) GIN

NCR 8310
52 pin J Lead PLCC

Samples: January, 1986
Production: March, 1986

Lead-time: 8 weeks

NCR 53C80
48 pin DIP

Samples: December, 1985
Production: February, 1986

Lead-time: 8 weeks

NCR 53C80
44 pin J-Lead PLCC

Samples: January, 1986
Production: February, 1986

Lead-time: 8 weeks

DR7/	1	48	DM7/
RST/	2	47	DB5/
GND	3	46	GND
BSY/	4	45	DB4/
SEL/	5	44	DB3/
ATN/	6	43	DB2/
NC	7	42	NC
RESET/	8	41	DB1/
IRQ	9	40	DB0/
DRQ	10	39	GND
EOP/	11	38	DBP/
DACK/	12	37	REQ/
GND	13	36	ACK/
READY	14	35	I/O/
A0	15	34	GND
A1	16	33	C/D/
A2	17	32	MSG/
NC	18	31	NC
CS/	19	30	D0
IOW/	20	29	D1
IOR/	21	28	D2
D7	22	27	D3
D6	23	26	D4
D5	24	25	VDD

ATN	SEL	BSY	VSS	RST	DB7	DB6	DB5	VSS	DB4	DB3
6	5	4	3	2	1	44	43	42	41	40
RESET	7								39	DB2
IRQ	8								38	DB1
DRQ	9								37	DB0
EOP	10								36	VSS
DACK	11								35	DBP
VSS	12								34	REQ
READY	13								33	ACK
A0	14								32	I/O
A1	15								31	VSS
A2	16								30	C/D
CS	17								29	MSG
18	19	20	21	22	23	24	25	26	27	28
IOW	IOR	D7	D6	D5	VDD	D4	D3	D2	D1	D0