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APPLICANT

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VERIFIED THIS APPLN IS A DIV OF 08/748,148 11/12/96 , *abandoned*
yes, PC

371 (NAT'L STAGE) DATA***
VERIFIED
NONE, PC

FOREIGN APPLICATIONS***
VERIFIED REPUBLIC OF KOREA 96-25227 06/28/96
yes, PC

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Foreign Priority claimed 35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OF COUNTRY KRX	SHEETS DRAWING 2	TOTAL CLAIMS 16	INDEPENDENT CLAIMS 2
Verified and Acknowledged <i>PC</i> Examiner's Initials _____ Initials _____					
SEE CUSTOMER NUMBER: 020792					
METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS					
FILING FEE RECEIVED \$760	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

PATENT APPLICATION



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jc511 U.S. PTO

09/318188



05/25/99

INITIALS

CONTENTS

	Date received (Incl. C. of M.) or Date Mailed	Date received (Incl. C. of M.) or Date Mailed
1. Application _____ papers.		42. _____
2. <u>I D S</u>	5-25-99	43. _____
3. <u>Associate Pa</u>	5-25-99	44. _____
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7. <u>Amdt B</u>	5/4/00	48. _____
8. <u>FINAL REJECTION (3 MONTHS)</u>	7-13-00	49. _____
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10. <u>ADVISORY ACTION</u>	10-23-00	51. _____
11. <u>EX. OF TIME</u>	11-10-00	52. _____
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13. <u>NON-FINAL REJECTION (3 MONTHS)</u>	12-5-00	54. _____
14. <u>Amdt E</u>	3/7/01	55. _____
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40. _____		81. _____
41. _____		82. _____

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(10) **Patent No.:** **US 6,287,902 B1**
(45) **Date of Patent:** **Sep. 11, 2001**

FIG. 1
(PRIOR ART)

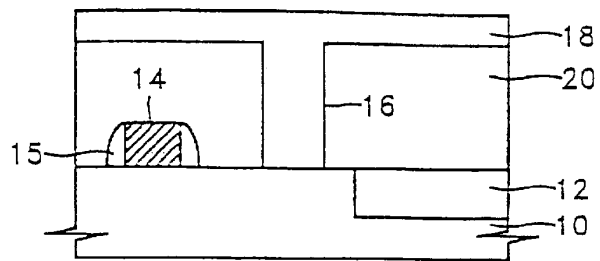


FIG. 2
(PRIOR ART)

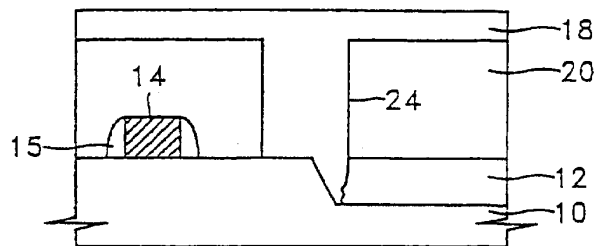


FIG. 3
(PRIOR ART)

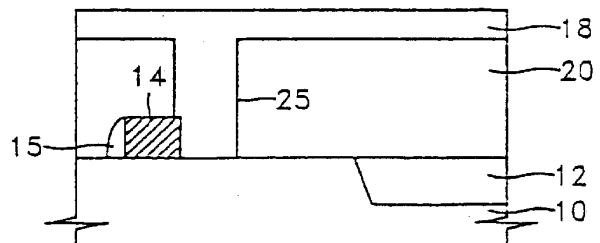


FIG. 4

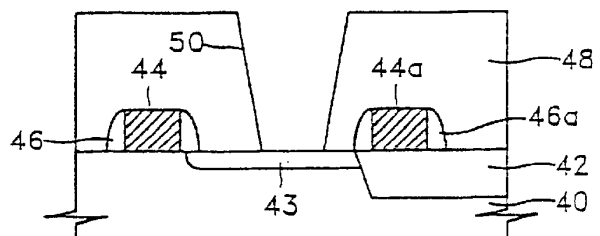


FIG. 5



FIG. 6

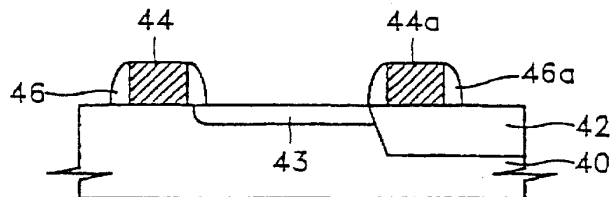


FIG. 7

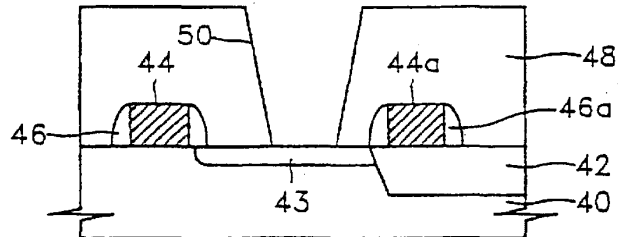
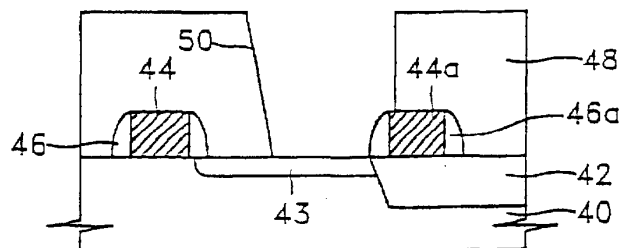


FIG. 8



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METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS

This application is a divisional application of U.S. patent application Ser. No. 08/748,148 filed Nov. 12, 1996, abandoned, and entitled ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS AND RELATED METHODS.

FIELD OF THE INVENTION

The present invention relates to microelectronic structures and methods and more particularly to microelectronic structures and methods including isolation regions.

BACKGROUND OF THE INVENTION

As integrated circuit devices become more highly integrated, the space available for individual devices formed thereon is reduced. Accordingly, the sizes of patterns such as gates, bit lines, and metal lines formed on integrated circuits are generally reduced. Furthermore, space between these patterns is also generally reduced.

In particular, integrated circuit memory devices include a plurality of memory cells, and each memory cell is connected to other cells by conductive (metal) lines. The cells and conductive (metal) lines are connected to the substrate or other conductive layers by contact holes or via holes. The contact holes expose active regions of the substrate and the via holes expose the surface of other conductive layers. Patterned layers such as the gate electrodes should be isolated from the holes, and these patterned layers are generally arranged around the holes. Accordingly, the holes must be accurately placed in order to maintain electrical isolation with respect to the patterned layers such as the gate electrodes.

As the space between these patterned layers is reduced, however, the space available for forming the holes may also be reduced. Furthermore, there may be physical limits to the reductions which can be made to the size of the holes. Accordingly, the increased integration reduces the margin available in the placement of the holes. The margin available for the placement of the holes is also influenced by the process limitations of the steps for forming other adjacent patterns. For example, when a LOCOS field oxide layer is formed, the bird's beak phenomenon may reduce the active region. When a trench field oxide layer is formed, the inner wall of the trench may encroach into the active region also reducing the area available to the hole and further decreasing the margin for the formation of the hole.

FIG. 1 is a cross-sectional view of an integrated circuit device having a contact hole 16. The field oxide layer 12 is formed on the semiconductor substrate 10, and the gate electrode 14 is formed on an active region defined by the field oxide layer 12. Spacers 15 are formed along the sidewalls of the gate electrode 14. An insulating layer 20 is then formed on the surface of the substrate including the gate electrode 14 and the field oxide layer 12, and the contact hole 16 is formed therein to expose a portion of the active region of the substrate. The conductive layer 18 is formed on the insulating layer 20 thus filling the contact hole 16. The contact hole 16 is preferably formed over the active region between the gate electrode 14 and the field oxide film 12 so that neither the gate electrode 14 nor the field oxide film 12 is exposed.

While the contact hole 16 is shown centered between the gate electrode 14 and the field oxide layer 12 in FIG. 1, it

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may become more difficult to form the contact hole between these structures as the device integration increases. As the spaces become smaller, formation of the contact hole 16 may be limited by the physical characteristics of light and the ability to properly align the mask. Accordingly, the margin for error during the formation of the contact hole is reduced. As shown in FIGS. 2 and 3, misalignment of the contact hole photomask may cause the contact hole to expose either the gate electrode 14 or the field oxide layer 12.

As shown in FIG. 2, the misaligned contact hole 24 exposes a portion of the active region as well as a portion of the field region. This misalignment may also result in the formation of a well through the field oxide layer 12 thus exposing a portion of a field region of the substrate when etching the insulating film 20. In other words, a contact hole 24 may partially expose an active region of the substrate and a well in the field region of the substrate. Accordingly, when the contact hole 24 is filled with the conductive layer 18, the conductive layer 18 is brought into contact with the well. Leakage current may thus flow through the conductive layer 18 into the well area. The integrated circuit device may thus overload leading to a delay in the operation of the device or even a malfunction. If a capacitor is formed, the life of the capacitor may also be reduced.

In FIG. 3, a misaligned contact hole exposes a portion of the gate electrode 14. Accordingly, the conductive layer 18 filling the contact hole 25 may contact the gate electrode 14 thus short circuiting the device. The reliability of the integrated circuit device may thus be reduced.

As discussed above, margins for forming contact holes are reduced as device integration increases. For example, the extension of a gate or a field region may reduce the area available for a contact hole, thus reducing the process margins. The reduction of process margins in turn causes a reduction in the alignment margin for the photomask used to form the contact hole. Accordingly, alignment of the photomask may become more difficult. The contact holes for integrated circuit devices may thus be more difficult to form and the alignment thereof may also be more difficult.

Accordingly, there continues to exist a need in the art for improved contact hole structures and related methods.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide improved contact hole structures and methods.

It is still another object of the present invention to provide increased alignment tolerances for the formation of contact holes.

These and other objects are provided according to the present invention by structures and methods wherein an etch inhibiting layer is provided on a field isolation layer adjacent the active region of the substrate. This etch inhibiting layer allows the misalignment of the contact hole without damaging the field isolation layer. Accordingly, the yield and reliability of integrated circuit devices formed according to the present invention can be increased at a given level of integration.

In particular, a microelectronic structure includes a substrate having active and field regions and a field isolation layer which covers the field region, and first and second patterned conductive layers. The first patterned conductive layer is on the active region of the substrate spaced apart from the field region, and the second patterned conductive layer is on the field isolation layer adjacent the active region of the substrate. The second patterned conductive layer thus acts as the etch inhibiting layer protecting the field isolation layer.

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The structure can also include an insulating layer covering the substrate, the field isolation layer, and the first and second patterned conductive layers, and the insulating layer includes a contact hole therein exposing a portion of the active region between the first and second patterned conductive layers. The contact hole can thus extend over the field region without damaging the field isolation layer because the first patterned conductive layer protects the field isolation layer.

In addition, the first and second patterned conductive layers may include insulating spacers along sidewalls thereof, and the insulating layer can preferably be selectively etched with respect to the insulating spacers. In particular, the insulating layer can be formed from nitride.

The second patterned conductive layer is preferably electrically isolated so that it serves no electrical function in the completed device. This layer can thus act only as an etch inhibiting layer to protect the field isolation layer. Furthermore, the field isolation layer can be formed from oxide, and the field region can be a trench in the substrate with the field isolation layer filling the trench.

According to another aspect of the invention, a method includes the steps of defining adjacent active and field regions on a substrate, and forming a field isolation layer on the field region. An etch inhibiting layer is formed on the field isolation layer adjacent the active region of the substrate. An insulating layer is then formed on the substrate, the field isolation layer, and the etch inhibiting layer, and a contact hole is formed in the insulating layer. This contact hole exposes a portion of the active region of the substrate adjacent the etch inhibiting layer and the field isolation layer. The etch inhibiting layer thus protects the field isolation layer during the step of forming the contact hole.

The insulating layer can be nitride, and the step of forming the insulating layer can be preceded by the step of forming a patterned conductive layer on the active region of the substrate. More particularly, the etch inhibiting layer and the patterned conductive layer can each include a conductive portion and insulating spacers along sidewalls thereof. Preferably, the steps of forming the etch inhibiting layer and forming the patterned conductive layer are performed simultaneously. In addition, the etch inhibiting layer is preferably electrically isolated, and the field isolation layer can be oxide.

The methods and structures of the present invention thus provide protection for the field isolation layer during the formation of a contact hole. Accordingly, a greater degree of misalignment during the step of forming the contact hole can be tolerated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross sectional view illustrating a contact hole formed according to the prior art.

FIG. 2 is a cross sectional view illustrating a first misaligned contact hole formed according to the prior art.

FIG. 3 is a cross sectional view illustrating a second misaligned contact hole formed according to the prior art.

FIG. 4 is a cross sectional view illustrating a contact hole formed according to the present invention.

FIGS. 5-7 are cross sectional views illustrating steps of a method for forming a contact hole according to the present invention.

FIG. 8 is a cross sectional view illustrating a misaligned contact hole formed according to the present invention.

DETAILED DESCRIPTION

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in

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which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout.

A contact hole formed according to the present invention is illustrated in FIG. 4. As shown, a field isolation layer 42 is formed on a field region of the substrate 40, and the field isolation layer 42 can be an oxide layer. Portions of the substrate 40 not covered by the field isolation layer 42 define the active region where microelectronic devices will be formed. As also shown, the field isolation layer 42 may be formed in a trench. Alternately, the field oxide layer may be formed by a LOCOS-type method.

First and second patterned conductive layers 44 and 44a are formed respectively on the active region of the substrate and on a field isolation layer 42. Insulating spacers 46 and 46a are formed along the sidewalls of the first and second patterned conductive layers 44 and 44a. In particular, the first patterned conductive layer 44 can be a gate electrode of a transistor. The second patterned conductive layer 44a preferably has the same structure as the first patterned conductive layer 44 with the exception that the second patterned conductive layer is electrically isolated. In other words, the second patterned conductive layer 44a serves as a dummy pattern.

An insulating layer 48 is then formed over the surface of the semiconductor substrate including the first and second patterned conductive layers 44 and 44a. A contact hole 50 is then formed in the insulating layer 48 thereby exposing a portion of the active region of the substrate. More particularly, the contact hole 50 may expose a doped layer 43 in the active region of the substrate. The insulating layer 48 is preferably formed from a material such as nitride which is more susceptible to etching than the material used to form the insulating spacers 46 and 46a.

Using the structure discussed above, some misalignment of the contact hole 50 can be tolerated. In particular, if the contact hole extends beyond the active region of the substrate encroaching into the field region, a second patterned conductive layer 44a reduces the likelihood that a well will be formed in the field isolation layer 42. In particular, the second patterned conductive layer 44a can act as an etch stop if needed when etching the insulating layer 48. In other words, contact hole 50 can now extend over the field region without damaging the field isolation layer 42.

When comparing the prior art structure of FIG. 1 with that of FIG. 4, the area over which the contact hole 50 can be formed using the structure of the present invention is larger than the area available using the structure of the prior art. In particular, the contact hole of FIG. 1 must be formed between the gate electrode 14 and the field oxide layer 12. When using the structure of the present invention, however, the area over which the contact hole 50 can be formed extends over a portion of the field region covered by the second patterned conductive layer 44a.

A method for forming an integrated circuit device according to the present invention will be discussed with reference to FIGS. 5-7. Active and isolation regions of the substrate 40 are defined as shown in FIG. 5. In particular, field isolation layer 42 is formed on the isolation region of the substrate, and the active region of the substrate is left exposed. This

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field isolation layer can be formed from a layer of oxide. Electronic devices are typically not formed in the isolation region of the substrate. As shown, a trench can be formed on the isolation region of the substrate and this trench can be filled with the field isolation layer. Alternately, a field isolation layer can be formed by other methods such as the LOCOS method. Electronic devices can be formed in the active region of the substrate which is left exposed.

First and second patterned conductive layers 44 and 44a can then be formed as shown in FIG. 6. As shown, a first patterned conductive layer 44 is formed on an active region of the substrate 40, and a second patterned conductive layer 44a is formed on the field isolation layer 42. In particular, an oxide layer and a conductive layer can be sequentially formed on the surface of the substrate 40 including the field isolation layer 42. A photoresist pattern can then be formed on the conductive layer to define the patterned conductive layers. The exposed portions of the conductive layer and the oxide layer can then be isotropically etched to expose portions of the surface of the substrate 40 and the field isolation layer 42. Accordingly, the first and second patterned conductive layers 44 and 44a are respectively formed on the active and field regions of the substrate. The patterned conductive layers can be defined to include an oxide layer adjacent the substrate.

A nitride layer can then be formed over the surface of the patterned conductive layers, the substrate 40, and the field isolation layer 42. This nitride film can be isotropically etched to form the nitride spacers 46 and 46a along the sidewalls of the first and second patterned conductive layers 44 and 44a. As will be discussed below, a contact hole 50 can thus be self-aligned using the spacers 46 and 46a.

Unlike methods of the prior art, the structure formed according to the present invention includes the second patterned conductive layer 44a on the field isolation layer 42. The first patterned conductive layer 44 may be used as a gate electrode, while the second patterned conductive layer 44a can be a dummy pattern serving no electrical function. Instead, the second patterned conductive layer 44a is used to increase a process margin for the formation of a contact hole by allowing the formation of a self-aligned contact hole as discussed below. Accordingly, the second patterned conductive layer 44a is preferably electrically isolated over the field region.

The second patterned conductive layer 44a is formed on a portion of the field isolation layer 42 where a misaligned contact hole would most likely encroach. Accordingly, the second patterned conductive layer 44a can be used to reduce design rule constraints related to the formation of the contact hole. The size of the second patterned conductive layer 44a is determined in part by the size of the contact hole to be formed and the likely position of the contact hole in the event of misalignment.

A contact hole 50 is formed as shown in FIG. 7. A conductive layer 43 can be formed in the active region of the substrate by implanting a dopant into the substrate 40. This implant can be masked in part by the patterned conductive layer 44, and the implanting step may be an ion implanting step. The insulating layer 48 can then be formed with a thickness sufficient to cover the first and second patterned conductive layers 44 and 44a. The contact hole 50 is then formed in the insulating layer 48 to expose a portion of the active region between the first and second patterned conductive layers 44 and 44a. The contact hole 50 preferably exposes the doped layer 43 without exposing either of the patterned conductive layers.

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The contact hole 50, however, may extend into the field region or into the first patterned conductive layer 44 according to the alignment of the mask used to form the contact hole. As shown in FIG. 8, a self-aligned contact hole 50 may extend over the field region. Because the second patterned conductive layer 44a serves as an etch inhibiting film, the contact hole 50 is self-aligned allowing it to extend over the field region. Stated in other words, the second patterned conductive layer 44a and associated spacers 46a protect the field isolation layer 42 from the etch used to form the contact hole 50. Accordingly, even with a misalignment of the contact hole mask over the field region and over etching to insure exposure of the active region, the field isolation layer 42 is not damaged. The masking and etching margins can thus be increased with respect to the prior art. In the event the contact hole mask is aligned to the first patterned conductive layer 44, a self-aligned contact hole can be formed using the spacers 46.

In the integrated circuit devices of the present invention, patterned conductive layers are simultaneously formed on both the active and field regions. The patterned conductive layer on the field region, however, can be electrically isolated thus serving no electrical function in the completed integrated circuit device. A self-aligned contact hole can thus be formed over the active region of the substrate using the patterned conductive layer formed in the field region to protect the field isolation layer during the etch used to form the contact hole. Because the patterned conductive layer over the field region protects the field isolation layer, the area over which the contact hole can be formed is increased with respect to the prior art. Accordingly, a greater contact margin is allowed when forming the contact hole. Furthermore, the etching margins can be increased without increasing the risk of damaging the field isolation layer. Reliability of the integrated circuit device can thus be increased because leakage current generated by damage to the field isolation layer can be reduced. Furthermore, no extra processing steps are required because the second patterned conductive layer and the first patterned conductive layer (which can be a transistor gate) can be formed simultaneously.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:
 - defining adjacent active and field regions on a substrate, and circuits thereon;
 - forming a field isolation layer on said field region;
 - forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;
 - forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, wherein the second patterned conductive layer does not extend over the active region of the substrate, and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

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forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer; and

forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer.

2. A method according to claim 1 wherein said insulating layer comprises nitride.

3. A method according to claim 1 wherein said first patterned conductive layer comprises a conductive portion and insulating spacers along sidewalls thereof.

4. A method according to claim 3 wherein said steps of forming said etch inhibiting layer and forming said patterned conductive layer are performed simultaneously.

5. A method according to claim 1 wherein said field isolation layer comprises oxide.

6. A method according to claim 1 wherein said step of defining said field and active regions comprises the step of forming a trench in said substrate, and wherein said field isolation layer fills said trench.

7. A method according to claim 1 wherein the insulating spacer of the etch inhibiting layer extends to the active region of the substrate.

8. A method according to claim 1 wherein the insulating spacer and the insulating layer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.

9. A method according to claim 1 wherein contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer.

10. A method according to claim 1 wherein at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer.

11. A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

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12. A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

13. A method according to claim 12 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.

14. A method according to claim 12 wherein the insulating layer and the insulating spacer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.

15. A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers; wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

16. A method according to claim 15 wherein said insulating layer can be selectively etched with respect to said insulating spacers.

17. A method according to claim 16 wherein said insulating layer comprises nitride.

18. A method for forming a microelectronic structure, said method comprising the steps of:

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defining adjacent active and field regions on a substrate,
and circuits thereon;
forming a field isolation layer which covers said field
region;
forming a first patterned layer on said active region of said
substrate spaced apart from said field region;
forming a second patterned layer on said field isolation
layer adjacent said active region of said substrate, the
active region including the first patterned layer wherein
said second patterned layer comprises a patterned con-
ductive layer and an insulating spacer along a sidewall
of the patterned conductive layer, wherein the patterned
conductive layer does not extend over the active region
of the substrate, and wherein the patterned conductive

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layer is a dummy pattern electrically isolated from the
substrate and circuits thereon;
forming an insulating layer covering said substrate, said
field isolation layer, and said first and second patterned
layers; and
forming a contact hole in said insulating layer wherein
said contact hole exposes a portion of said active region
between said first and second patterned layers;
wherein the first patterned layer comprises a patterned
gate layer and an insulating gate spacer along a
sidewall thereof.

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JCS34 U.S. PTO
05/25/99

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY DOCKET NO.: 5649-129DV
DATE: May 25, 1999

UTILITY PATENT APPLICATION TRANSMITTAL LETTER
AND FEE TRANSMITTAL FORM (37 CFR 1.53(b))

JCS11 U.S. PTO
09/318188
05/25/99

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is:

- ☐ a patent application
☐ a Continuation ☒ a Divisional ☐ a Continuation-in-Part (CIP)
of prior application no.: 08/748,148; filed November 12, 1996
☐ A Small Entity Statement(s) was filed in the prior application; Status still proper and desired.

Inventor(s) or Application Identifier:
Do-hyung Kim

Entitled: **ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS AND
RELATED METHODS**

Enclosed are:

1. ☒ Application Transmittal Letter and Fee Transmittal Form (*A duplicate is enclosed for fee processing*)
2. ☒ 19 pages of Specification (including 31 claims)
3. ☒ 2 sheets of formal Drawings (35 USC 113)
4. ☒ Oath or Declaration
 - a. ☐ newly executed (*original or copy*)
 - b. ☒ copy from prior application (37 CFR 1.63(d) (*for continuation/divisional*) [**Note Box 5 Below**]
 - c. ☐ DELETION OF INVENTOR(S) (*Signed statement deleting inventor(s) named in the prior application*)
5. ☒ Incorporation By Reference (*useable if box 4b is checked*)

The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (*Appendix*)
7. ☐ Assignment papers (*cover sheet(s) and document(s)*)
8. ☐ Small Entity Statement(s)
9. ☒ Information Disclosure Statement, PTO-1449
10. ☒ Preliminary Amendment (***Please enter all claim amendments prior to calculating the filing fee.***)
11. ☐ English Translation Document
12. ☒ Certified Copy of Korean App. No. 96-25227; Filed June 28, 1996, filed in parent app.

In re: Do-hyung Kim
Filed: May 25, 1999
Page 2

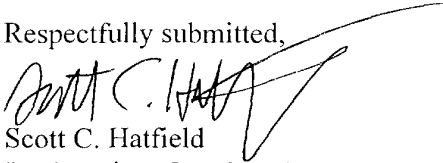
13. ☐ Sequence Listing/ Sequence Listing Diskette
a. ☐ computer readable copy
b. ☐ paper copy
c. ☐ statement in support
14. ☒ Copy of an Associate Power of Attorney
15. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
16. ☒ Other: Change of Correspondence Address filed in parent application

The fee has been calculated as shown below:

	Column 1 No. Filed	Column 2 No. Extra	Small Entity Rate Fee	Large Entity Rate Fee
BASIC FEE			\$380.00	\$760.00
TOTAL CLAIMS	16 - 20 =	0	x 9 = \$	x 18 =
INDEP CLAIMS	2 - 3 =	0	x 39 = \$	x 78 =
<input type="checkbox"/> MULTIPLE Dependent Claims Presented			+ 130 = \$	+ 260 =
If the difference in Col. 1 is less than zero, Enter "0" in Col. 2			Total \$	Total \$760.00

- ☒ A check in the amount of \$760.00 to cover the filing fee is enclosed.
☐ A check in the amount of \$ is enclosed to cover the filing fee, PLUS the Assignment Recordation fee (\$40.00).
☐ Please charge my Deposit Account No. 50-0220 in the amount of \$.
☐ The Commissioner is hereby authorized to credit overpayments or charge the following fees associated with this communication to Deposit Account No. 50-0220:
a. ☐ Additional filing fees under 37 CFR 1.16 for presentation of extra claims.
b. ☐ Additional patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

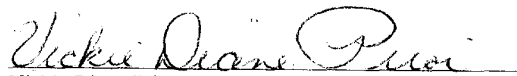

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CERTIFICATE OF EXPRESS MAILING

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I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Assistant Commissioner For Patents, Washington, DC 20231.


Vickie Diane Prior
Date of Signature: May 25, 1999

**ETCH INHIBITING STRUCTURES ON FIELD
ISOLATION REGIONS AND RELATED METHODS**

Insul Field of the Invention

5 The present invention relates to
microelectronic structures and methods and more
particularly to microelectronic structures and methods
including isolation regions.

Background of the Invention

10 As integrated circuit devices become more
highly integrated, the space available for individual
devices formed thereon is reduced. Accordingly, the
sizes of patterns such as gates, bit lines, and metal
lines formed on integrated circuits are generally
reduced. Furthermore, space between these patterns is
also generally reduced.

15 In particular, integrated circuit memory
devices include a plurality of memory cells, and each
memory cell is connected to other cells by conductive
(metal) lines. The cells and conductive (metal) lines
are connected to the substrate or other conductive
20 layers by contact holes or via holes. The contact
holes expose active regions of the substrate and the
via holes expose the surface of other conductive
layers. Patterned layers such as the gate electrodes
should be isolated from the holes, and these patterned
25 layers are generally arranged around the holes.
Accordingly, the holes must be accurately placed in
order to maintain electrical isolation with respect to
the patterned layers such as the gate electrodes.

As the space between these patterned layers is reduced, however, the space available for forming the holes may also be reduced. Furthermore, there may be physical limits to the reductions which can be made to the size of the holes. Accordingly, the increased integration reduces the margin available in the placement of the holes. The margin available for the placement of the holes is also influenced by the process limitations of the steps for forming other adjacent patterns. For example, when a LOCOS field oxide layer is formed, the bird's beak phenomenon may reduce the active region. When a trench field oxide layer is formed, the inner wall of the trench may encroach into the active region also reducing the area available to the hole and further decreasing the margin for the formation of the hole.

Figure 1 is a cross-sectional view of an integrated circuit device having a contact hole 16. The field oxide layer 12 is formed on the semiconductor substrate 10, and the gate electrode 14 is formed on an active region defined by the field oxide layer 12. Spacers 15 are formed along the sidewalls of the gate electrode 14. An insulating layer 20 is then formed on the surface of the substrate including the gate electrode 14 and the field oxide layer 12, and the contact hole 16 is formed therein to expose a portion of the active region of the substrate. The conductive layer 18 is formed on the insulating layer 20 thus filling the contact hole 16. The contact hole 16 is preferably formed over the active region between the gate electrode 14 and the field oxide film 12 so that neither the gate electrode 14 nor the field oxide film 12 is exposed.

While the contact hole 16 is shown centered between the gate electrode 14 and the field oxide layer 12 in Figure 1, it may become more difficult to form the contact hole between these structures as the device

integration increases. As the spaces become smaller, formation of the contact hole 16 may be limited by the physical characteristics of light and the ability to properly align the mask. Accordingly, the margin for error during the formation of the contact hole is reduced. As shown in Figures 2 and 3, misalignment of the contact hole photomask may cause the contact hole to expose either the gate electrode 14 or the field oxide layer 12.

As shown in Figure 2, the misaligned contact hole 24 exposes a portion of the active region as well as a portion of the field region. This misalignment may also result in the formation of a well through the field oxide layer 12 thus exposing a portion of a field region of the substrate when etching the insulating film 20. In other words, a contact hole 24 may partially expose an active region of the substrate and a well in the field region of the substrate. Accordingly, when the contact hole 24 is filled with the conductive layer 18, the conductive layer 18 is brought into contact with the well. Leakage current may thus flow through the conductive layer 18 into the well area. The integrated circuit device may thus overload leading to a delay in the operation of the device or even a malfunction. If a capacitor is formed, the life of the capacitor may also be reduced.

In Figure 3, a misaligned contact hole exposes a portion of the gate electrode 14. Accordingly, the conductive layer 18 filling the contact hole 25 may contact the gate electrode 14 thus short circuiting the device. The reliability of the integrated circuit device may thus be reduced.

As discussed above, margins for forming contact holes are reduced as device integration increases. For example, the extension of a gate or a field region may reduce the area available for a contact hole, thus reducing the process margins. The

reduction of process margins in turn causes a reduction in the alignment margin for the photomask used to form the contact hole. Accordingly, alignment of the photomask may become more difficult. The contact holes
5 for integrated circuit devices may thus be more difficult to form and the alignment thereof may also be more difficult.

Accordingly, there continues to exist a need in the art for improved contact hole structures and
10 related methods.

Summary of the Invention

It is therefore an object of the present invention to provide improved contact hole structures and methods.
15

It is still another object of the present invention to provide increased alignment tolerances for the formation of contact holes.

These and other objects are provided
20 according to the present invention by structures and methods wherein an etch inhibiting layer is provided on a field isolation layer adjacent the active region of the substrate. This etch inhibiting layer allows the misalignment of the contact hole without damaging the
25 field isolation layer. Accordingly, the yield and reliability of integrated circuit devices formed according to the present invention can be increased at a given level of integration.

In particular, a microelectronic structure
30 includes a substrate having active and field regions and a field isolation layer which covers the field region, and first and second patterned conductive layers. The first patterned conductive layer is on the active region of the substrate spaced apart from the
35 field region, and the second patterned conductive layer is on the field isolation layer adjacent the active region of the substrate. The second patterned

conductive layer thus acts as the etch inhibiting layer protecting the field isolation layer.

5 The structure can also include an insulating layer covering the substrate, the field isolation layer, and the first and second patterned conductive layers, and the insulating layer includes a contact hole therein exposing a portion of the active region between the first and second patterned conductive layers. The contact hole can thus extend over the
10 field region without damaging the field isolation layer because the first patterned conductive layer protects the field isolation layer.

15 In addition, the first and second patterned conductive layers may include insulating spacers along sidewalls thereof, and the insulating layer can preferably be selectively etched with respect to the insulating spacers. In particular, the insulating layer can be formed from nitride.

20 The second patterned conductive layer is preferably electrically isolated so that it serves no electrical function in the completed device. This layer can thus act only as an etch inhibiting layer to protect the field isolation layer. Furthermore, the field isolation layer can be formed from oxide, and the
25 field region can be a trench in the substrate with the field isolation layer filling the trench.

30 According to another aspect of the invention, a method includes the steps of defining adjacent active and field regions on a substrate, and forming a field isolation layer on the field region. An etch inhibiting layer is formed on the field isolation layer adjacent the active region of the substrate. An insulating layer is then formed on the substrate, the field isolation layer, and the etch inhibiting layer,
35 and a contact hole is formed in the insulating layer. This contact hole exposes a portion of the active region of the substrate adjacent the etch inhibiting

layer and the field isolation layer. The etch inhibiting layer thus protects the field isolation layer during the step of forming the contact hole.

5 The insulating layer can be nitride, and the step of forming the insulating layer can be preceded by the step of forming a patterned conductive layer on the active region of the substrate. More particularly, the etch inhibiting layer and the patterned conductive layer can each include a conductive portion and
10 insulating spacers along sidewalls thereof. Preferably, the steps of forming the etch inhibiting layer and forming the patterned conductive layer are performed simultaneously. In addition, the etch inhibiting layer is preferably electrically isolated,
15 and the field isolation layer can be oxide.

The methods and structures of the present invention thus provide protection for the field isolation layer during the formation of a contact hole. Accordingly, a greater degree of misalignment during
20 the step of forming the contact hole can be tolerated.

Brief Description of the Drawings

Figure 1 is a cross sectional view illustrating a contact hole formed according to the prior art.
25

Figure 2 is a cross sectional view illustrating a first misaligned contact hole formed according to the prior art.

Figure 3 is a cross sectional view illustrating a second misaligned contact hole formed according to the prior art.
30

Figure 4 is a cross sectional view illustrating a contact hole formed according to the present invention.

35 Figures 5-7 are cross sectional views illustrating steps of a method for forming a contact hole according to the present invention.

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patterned conductive layer 44 with the exception that the second patterned conductive layer is electrically isolated. In other words, the second patterned conductive layer 44a serves as a dummy pattern.

5 An insulating layer 48 is then formed over the surface of the semiconductor substrate including the first and second patterned conductive layers 44 and 44a. A contact hole 50 is then formed in the
10 insulating layer 48 thereby exposing a portion of the active region of the substrate. More particularly, the contact hole 50 may expose a doped layer 43 in the active region of the substrate. The insulating layer 48 is preferably formed from a material such as nitride
15 which is more susceptible to etching than the material used to form the insulating spacers 46 and 46a.

 Using the structure discussed above, some misalignment of the contact hole 50 can be tolerated. In particular, if the contact hole extends beyond the active region of the substrate encroaching into the
20 field region, a second patterned conductive layer 44a reduces the likelihood that a well will be formed in the field isolation layer 42. In particular, the second patterned conductive layer 44a can act as an etch stop if needed when etching the insulating layer
25 48. In other words, contact hole 50 can now extend over the field region without damaging the field isolation layer 42.

 When comparing the prior art structure of Figure 1 with that of Figure 4, the area over which the
30 contact hole 50 can be formed using the structure of the present invention is larger than the area available using the structure of the prior art. In particular, the contact hole of Figure 1 must be formed between the gate electrode 14 and the field oxide layer 12. When
35 using the structure of the present invention, however, the area over which the contact hole 50 can be formed

extends over a portion of the field region covered by the second patterned conductive layer 44a.

5 A method for forming an integrated circuit device according to the present invention will be discussed with reference to Figures 5-7. Active and isolation regions of the substrate 40 are defined as shown in Figure 5. In particular, field isolation layer 42 is formed on the isolation region of the substrate, and the active region of the substrate is left exposed. This field isolation layer can be formed from a layer of oxide. Electronic devices are typically not formed in the isolation region of the substrate. As shown, a trench can be formed on the isolation region of the substrate and this trench can be filled with the field isolation layer. Alternately, a field isolation layer can be formed by other methods such as the LOCOS method. Electronic devices can be formed in the active region of the substrate which is left exposed.

10 20 First and second patterned conductive layers 44 and 44a can then be formed as shown in Figure 6. As shown, a first patterned conductive layer 44 is formed on an active region of the substrate 40, and a second patterned conductive layer 44a is formed on the field isolation layer 42. In particular, an oxide layer and a conductive layer can be sequentially formed on the surface of the substrate 40 including the field isolation layer 42. A photoresist pattern can then be formed on the conductive layer to define the patterned conductive layers. The exposed portions of the conductive layer and the oxide layer can then be isotropically etched to expose portions of the surface of the substrate 40 and the field isolation layer 42. Accordingly, the first and second patterned conductive layers 44 and 44a are respectively formed on the active and field regions of the substrate. The patterned

conductive layers can be defined to include an oxide layer adjacent the substrate.

5 A nitride layer can then be formed over the surface of the patterned conductive layers, the substrate 40, and the field isolation layer 42. This nitride film can be isotropically etched to form the nitride spacers 46 and 46a along the sidewalls of the first and second patterned conductive layers 44 and 44a. As will be discussed below, a contact hole 50 can
10 thus be self-aligned using the spacers 46 and 46a.

Unlike methods of the prior art, the structure formed according to the present invention includes the second patterned conductive layer 44a on the field isolation layer 42. The first patterned
15 conductive layer 44 may be used as a gate electrode, while the second patterned conductive layer 44a can be a dummy pattern serving no electrical function. Instead, the second patterned conductive layer 44a is used to increase a process margin for the formation of a contact hole by allowing the formation of a self-aligned contact hole as discussed below. Accordingly,
20 the second patterned conductive layer 44a is preferably electrically isolated over the field region.

The second patterned conductive layer 44a is
25 formed on a portion of the field isolation layer 42 where a misaligned contact hole would most likely encroach. Accordingly, the second patterned conductive layer 44a can be used to reduce design rule constraints related to the formation of the contact hole. The size
30 of the second patterned conductive layer 44a is determined in part by the size of the contact hole to be formed and the likely position of the contact hole in the event of misalignment.

A contact hole 50 is formed as shown in
35 Figure 7. A conductive layer 43 can be formed in the active region of the substrate by implanting a dopant into the substrate 40. This implant can be masked in

part by the patterned conductive layer 44, and the implanting step may be an ion implanting step. The insulating layer 48 can then be formed with a thickness sufficient to cover the first and second patterned conductive layers 44 and 44a. The contact hole 50 is then formed in the insulating layer 48 to expose a portion of the active region between the first and second patterned conductive layers 44 and 44a. The contact hole 50 preferably exposes the doped layer 43 without exposing either of the patterned conductive layers.

The contact hole 50, however, may extend into the field region or into the first patterned conductive layer 44 according to the alignment of the mask used to form the contact hole. As shown in Figure 8, a self-aligned contact hole 50 may extend over the field region. Because the second patterned conductive layer 44a serves as an etch inhibiting film, the contact hole 50 is self-aligned allowing it to extend over the field region. Stated in other words, the second patterned conductive layer 44a and associated spacers 46a protect the field isolation layer 42 from the etch used to form the contact hole 50. Accordingly, even with a misalignment of the contact hole mask over the field region and over etching to insure exposure of the active region, the field isolation layer 42 is not damaged. The masking and etching margins can thus be increased with respect to the prior art. In the event the contact hole mask is aligned to the first patterned conductive layer 44, a self-aligned contact hole can be formed using the spacers 46.

In the integrated circuit devices of the present invention, patterned conductive layers are simultaneously formed on both the active and field regions. The patterned conductive layer on the field region, however, can be electrically isolated thus serving no electrical function in the completed

integrated circuit device. A self-aligned contact hole
can thus be formed over the active region of the
substrate using the patterned conductive layer formed
in the field region to protect the field isolation
layer during the etch used to form the contact hole.
5 Because the patterned conductive layer over the field
region protects the field isolation layer, the area
over which the contact hole can be formed is increased
with respect to the prior art. Accordingly, a greater
10 contact margin is allowed when forming the contact
hole. Furthermore, the etching margins can be
increased without increasing the risk of damaging the
field isolation layer. Reliability of the integrated
circuit device can thus be increased because leakage
15 current generated by damage to the field isolation
layer can be reduced. Furthermore, no extra processing
steps are required because the second patterned
conductive layer and the first patterned conductive
layer (which can be a transistor gate) can be formed
20 simultaneously.

In the drawings and specification, there have
been disclosed typical preferred embodiments of the
invention and, although specific terms are employed,
they are used in a generic and descriptive sense only
25 and not for purposes of limitation, the scope of the
invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A microelectronic structure comprising:
a substrate having active and field regions;
a field isolation layer which covers said field region;
a first patterned conductive layer on said active region of said substrate spaced apart from said field region; and
a second patterned conductive layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned conductive layer is electrically isolated.
2. A microelectronic structure according to Claim 1 further comprising an insulating layer covering said substrate, said field isolation layer, and said first and second patterned conductive layers, wherein said insulating layer defines a contact hole therein exposing a portion of said active region between said first and second patterned conductive layers.
3. A microelectronic structure according to Claim 2 wherein each of said first and second patterned conductive layers comprises insulating spacers along sidewalls thereof.
4. A microelectronic structure according to Claim 3 wherein said insulating layer can be selectively etched with respect to said insulating spacers.
5. A microelectronic structure according to Claim 4 wherein said insulating layer comprises nitride.

6. A microelectronic structure according to Claim 1 wherein said field isolation layer comprises oxide.

7. A microelectronic structure according to Claim 1 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.

8. A microelectronic structure according to Claim 1 wherein said first and second patterned conductive layers are identical in size and shape.

9. A microelectronic structure comprising:
a substrate having adjacent active and field regions;

5 a field isolation layer which covers said field region; and
an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate wherein said etch inhibiting layer is electrically isolated.

10. A microelectronic structure according to Claim 9 further comprising:

5 an insulating layer covering said substrate, said field isolation layer, and said etch inhibiting layer, wherein said insulating layer defines a contact hole therein exposing a portion of said active region adjacent said etch inhibiting layer and said field isolation layer.

11. A microelectronic structure according to Claim 10 wherein said insulating layer comprises nitride.

12. A microelectronic structure according to Claim 9 further comprising:

5 a patterned conductive layer on said active region of said substrate spaced apart from said field isolation region.

13. A microelectronic structure according to Claim 12 wherein each of said etch inhibiting layer and said patterned conductive layer comprise a conductive portion and insulating spacers along sidewalls thereof.

14. A microelectronic structure according to Claim 9 wherein said field isolation layer comprises oxide.

15. A microelectronic structure according to Claim 9 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.

Sub B1's
16. A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:

5 defining adjacent active and field regions on a substrate;
forming a field isolation layer on said field region;
forming an etch inhibiting layer on said field isolation layer adjacent said active region of
10 said substrate wherein said etch inhibiting layer is electrically isolated;
forming an insulating layer on said substrate, said field isolation layer, and said etch inhibiting layer; and

15 forming a contact hole in said insulating layer exposing a portion of said active region adjacent said etch inhibiting layer and said field isolation layer.

²
~~17~~. A method according to Claim ~~16~~¹ wherein said insulating layer comprises nitride.

18. A method according to Claim 16 wherein said step of forming said insulating layer is preceded by the step of:

5 forming a patterned conductive layer on said active region of said substrate spaced apart from said field isolation region.

Sub 1/2
19. A method according to Claim 18 wherein each of said etch inhibiting layer and said patterned conductive layer comprise a conductive portion and insulating spacers along sidewalls thereof.

⁴
~~20~~. A method according to Claim ~~19~~³ wherein said steps of forming said etch inhibiting layer and forming said patterned conductive layer are performed simultaneously.

⁵
~~21~~. A method according to Claim ~~19~~¹ wherein said field isolation layer comprises oxide.

⁴
~~22~~. A method according to Claim ~~16~~¹ wherein said step of defining said field and active regions comprises the step of forming a trench in said substrate, and wherein said field isolation layer fills said trench.

Sub B2 >

23. A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate;

5 forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

10 forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer is electrically isolated.

24. A method according to Claim 23 wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

Sub D >

25. A method according to Claim 23 further comprising the steps of:

5 forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

13

26. A method according to Claim 25 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.

12

Sub D >

27. A method according to Claim 23 wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

¹⁶
~~28.~~ A method according to Claim ~~27~~¹⁵ wherein
said insulating layer can be selectively etched with
respect to said insulating spacers.

¹⁷
~~29.~~ A method according to Claim ~~28~~¹⁶ wherein
said insulating layer comprises nitride.

30. A method according to Claim 23 wherein
said field isolation layer comprises oxide.

~~31.~~ A method according to Claim 23 wherein
each of said first and second patterned layers
comprises a patterned conductive layer.

Add B3 >

**ETCH INHIBITING STRUCTURES ON FIELD
ISOLATION REGIONS AND RELATED METHODS**

Abstract of the Disclosure

A microelectronic structure includes a substrate having adjacent active and field regions. A field isolation layer covers the field region, and an etch inhibiting layer is provided on the field isolation layer adjacent the active region of the substrate. An insulating layer covers the substrate, the field isolation layer, and the etch inhibiting layer, and the insulating layer defines a contact hole therein exposing a portion of the active region adjacent the etch inhibiting layer. Related methods are also discussed.

34048

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No. 5649-129

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS AND RELATED METHODS.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT International application having a filing date before that of the application on which priority is claimed.

96-25227	Korea	June 28, 1996	[X] Yes [] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed
			[] Yes [] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed
			[] Yes [] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed

ENGLISH LANGUAGE DECLARATION CONTINUED

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

None	
Application Number(s)	Filing Date (MM/DD/YYYY)
Application Number(s)	Filing Date (MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application (37 C.F.R. § 1.63(d)).

None		
Appln. Serial No.	Filing Date	Status Patented/Pending/Abandoned
Appln. Serial No.	Filing Date	Status Patented/Pending/Abandoned
Appln. Serial No.	Filing Date	Status Patented/Pending/Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

ENGLISH LANGUAGE DECLARATION CONTINUED

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Charles R. Donohoe
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Neil A. Steinberg
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William L. Geary, Jr.
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I hereby authorize the above-named attorneys to accept and follow instructions from my Korean or United States representatives, Samsung Electronics, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the above-named attorneys and myself. In the event of a change in the persons from whom instructions may be taken, I will notify the above-named attorneys.

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Citizenship: Republic of Korea

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FIG. 1
(PRIOR ART)

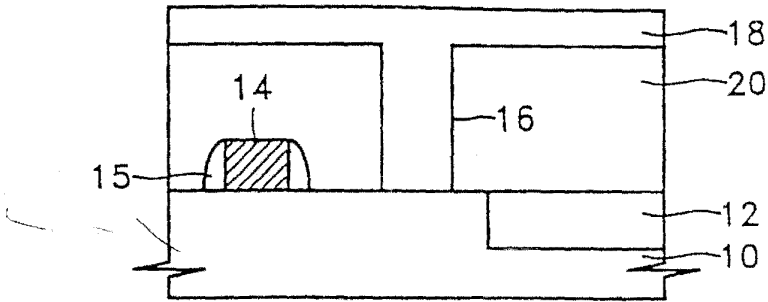


FIG. 2
(PRIOR ART)

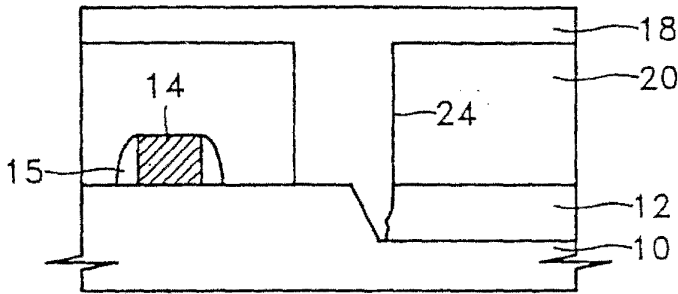


FIG. 3
(PRIOR ART)

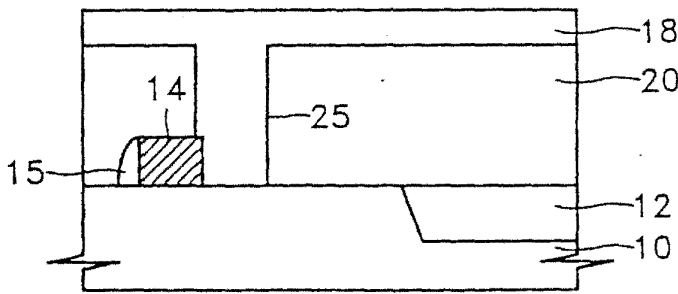


FIG. 4

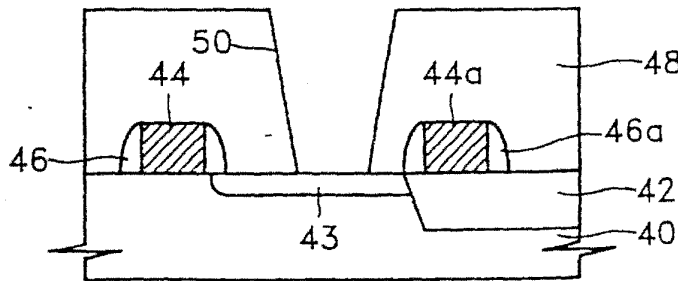


FIG. 5

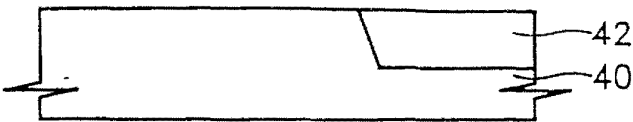


FIG. 6

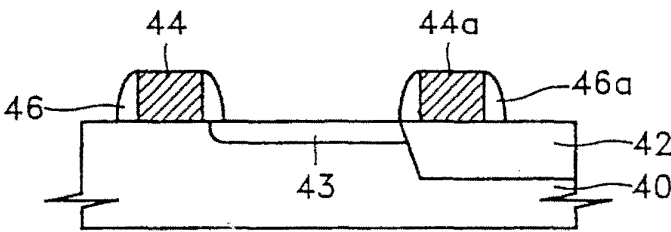


FIG. 7

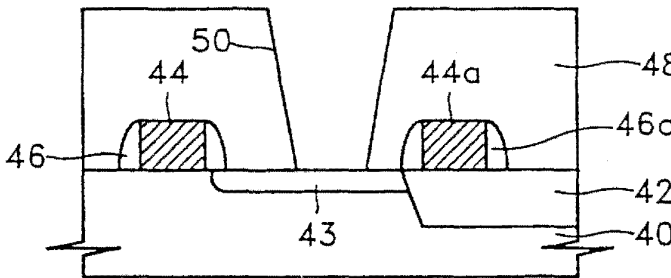
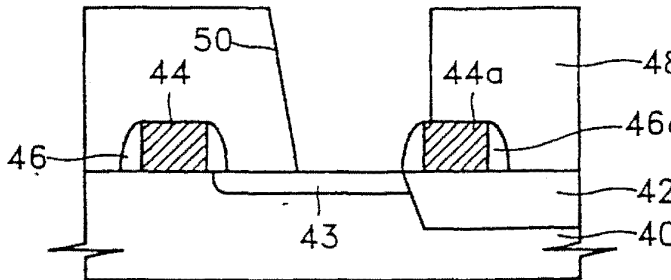


FIG. 8



Attorney's Docket No. 5649-129DV

#2/I DS
8-27-99
DM PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: To Be Assigned
Filed: Concurrently Herewith
For: ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS AND
RELATED METHODS

jc511 U.S. PTO
09/318188
05/25/99

May 25, 1999

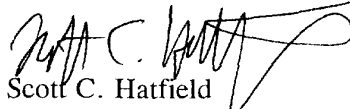
Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT
CITATION UNDER 37 C.F.R. § 1.97

Sir:

Attached is a list of documents on form PTO-1449. All items listed on the PTO-1449 were cited during the prosecution of parent application 08/748,148, filed November 12, 1996. Since the benefit of this application was claimed under 35 U.S.C. 120, no copies need to be furnished in accordance with 37 C.F.R. 1.98(d); however, copies will be furnished on request. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. §1.97 and Section 609 of the MPEP.

Respectfully submitted,


Scott C. Hatfield
Registration No. 38,176

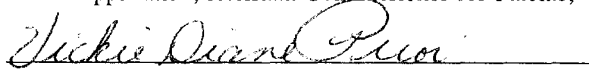
USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone (919) 854-1400
Facsimile (919) 854-1401

CERTIFICATE OF MAILING

"Express Mail" mailing label number EL299857199US

Date of Deposit: May 25, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, DC 20231.



Vickie Diane Prior

Date of Signature: May 25, 1999

3/associate Pa
8-27-95
Dm PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No. 08/748,148
Filed: November 12, 1996
For: ETCH INHIBITING STRUCTURES ON FIELD ISOLATION
REGIONS AND RELATED METHODS

January 31, 1997

BOX MISSING PART
Assistant Commissioner for Patents
Washington, DC 20231

ASSOCIATE POWER OF ATTORNEY

Sir:

The undersigned attorney of record in this case hereby appoints the below named persons, individually and collectively, as associate attorneys to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith and with the resulting patent:

Raymond O. Linker, Jr. Registration No. 26,419	Charles B. Elderkin Registration No. 24,357
Mitchell S. Bigel Registration No. 29,614	Timothy J. O'Sullivan Registration No. 35,632
Robert W. Glatz Registration No. 36,811	Grant J. Scott Registration No. 36,925
Scott C. Hatfield Registration No. 38,176	

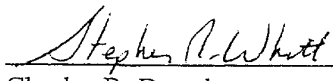
Unless and until otherwise directed, please send all correspondence about this application and the resulting patent to:

Mitchell S. Bigel
Bell, Seltzer, Park & Gibson, P.A.
P. O. Drawer 34009
Charlotte, NC 28234

Please direct all telephone calls about this application and the resulting patent to:

Mitchell S. Bigel
Telephone: 919/420-2200
Facsimile: 919/881-3175

The above-appointed associate attorneys are hereby authorized to act and rely on instructions from and communication directly with the assignee of record and with such patent agent/attorney liaison individual or firm, selected by the assignee, as may represent themselves to the associate attorneys as having been so appointed, unless and until I instruct the associate attorneys in writing to the contrary.


Charles R. Donohoe 24,546
Stephen R. Whitt 34,753
Allen LeRoy Limberg 27,211
Neil A. Steinberg 34,735
William L. Geary, Jr. 35,879
Brian C. Altmiller 37,271
Eric Oliver 35,307
SAMSUNG ELECTRONICS CO, LTD.

4/Change of
address
8-27-99
Dm PATENT

Attorney's Docket No. 5649-129

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 08/748,148
Filed: November 12, 1996
For: ETCH INHIBITING STRUCTURES ON FIELD ISOLATION
REGIONS AND RELATED METHODS

Group Art Unit: 2508
Examiner: P. Cao

Date : October 30, 1997

Box Non-Fee Amendment
Assistant Commissioner for Patents
Washington, DC 20231

CHANGE OF CORRESPONDENCE ADDRESS

Sir:


The address of the correspondence attorney in the above-referenced case
has changed to:

Mitchell S. Bigel
MYERS BIGEL SIBLEY & SAJOVEC, L.L.P.
P.O. Box 37428
Raleigh, NC 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

Please direct all telephone calls in connection with the above
identified application to:

Mitchell S. Bigel
Telephone: 919/854-1400


Respectfully submitted,


Scott C. Hatfield
Registration No. 38,176

Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, NC 27627
Telephone (919) 854-1400
Facsimile (919) 854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as
first class mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for
Patents, Washington, DC 20231, on October 30, 1997.


Denise O. Funderburke
Date of Signature: October 30, 1997

Attorney's Docket No. 5649-129DV

5/Pre Amnd
a
9/2/99
Dm PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: To Be Assigned
Filed: Concurrently Herewith
For: ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS
AND RELATED METHODS

May 25, 1999

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:
Please amend the present application as is described below.

In the Title:

Please amend the title:

--METHODS OF FORMING ETCH INHIBITING STRUCTURES ON
FIELD ISOLATION REGIONS [AND RELATED METHODS]--

In the Specification:

Prior to the section entitled "Field of the Invention" please insert the
following:

Related Applications

This application is a divisional application of United States Patent Application
Serial No. 08/748,148 filed November 12, 1996, and entitled *ETCH INHIBITING*
STRUCTURES ON FIELD ISOLATION REGIONS AND RELATED METHODS.

In re: Do-hyung
Serial No.: To Be Assigned
Filed: Concurrently Herewith
Page 2

In the Claims:

Please cancel Claims 1-15.

REMARKS

The present divisional application is being filed to claim non-elected Claims 16-31 from the parent application. The title has been changed to reflect the method claims. Examination and allowance of the present application is respectfully requested.

Respectfully submitted,



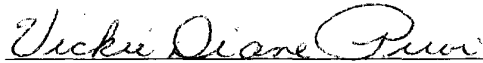
Scott C. Hatfield
Registration No. 38,176

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone (919) 854-1400
Facsimile (919) 854-1401

CERTIFICATE OF MAILING

"Express Mail" mailing label number EL299857199US
Date of Deposit: May 25, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, DC 20231.



Vickie Diane Prior
Date of Signature: May 25, 1999



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/318,188	05/25/99	KIM	D 5649-129DV

020792 MM42/0208
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH NC 27627

EXAMINER

CAD.P	
ART UNIT	PAPER NUMBER

2814
DATE MAILED: 02/08/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action SummaryApplication No.
09/318,188Applicant(s)
KimExaminer
Phat X. CaoGroup Art Unit
2814☒ Responsive to communication(s) filed on May 25, 1999☐ This action is **FINAL**.☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims☒ Claim(s) 16-31 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.☒ Claim(s) 16-31 is/are rejected.☐ Claim(s) _____ is/are objected to.☐ Claims _____ are subject to restriction or election requirement.**Application Papers**☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.☐ The drawing(s) filed on _____ is/are objected to by the Examiner.☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.☐ The specification is objected to by the Examiner.☐ The oath or declaration is objected to by the Examiner.**Priority under 35 U.S.C. § 119**☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.☒ received in Application No. (Series Code/Serial Number) 08/748,148.☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).**Attachment(s)**☒ Notice of References Cited, PTO-892☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2☐ Interview Summary, PTO-413☒ Notice of Draftsperson's Patent Drawing Review, PTO-948☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2814

DETAILED ACTION

1. The cancellation of claims 1-15 in paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 16-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uehara et al (US. 5,698,902) in view of Rodder (US. 5,475,266).

Regarding claims 16, 18-27, and 30-31, Uehara et al disclose in Figs. 1(a) - 1(e) a method of forming a contact hole for a microelectronic structure, the method comprising the steps of: defining adjacent active and field regions on a substrate 10; forming a field oxide isolation layer 17 on the field region by forming a trench in the substrate and filling the trench with the field isolation layer (see Fig. 7(f) and column 14, lines 29-31); simultaneously forming a dummy pattern 50b (column 10, lines 6-7) on the field isolation layer 17 adjacent the active region of the substrate and forming the patterned conductive layer 50a on the active region of the substrate spaced apart from the field isolation region 17, wherein each of the dummy pattern 50b and the patterned conductive layer 50a comprise a conductive portion and insulating spacer (20a, 20b) along sidewalls thereof; forming an insulating layer 32 on the substrate 10, the field isolation layer

Art Unit: 2814

17 and the dummy pattern 50b; and forming a contact hole penetrating the insulating layer 32 and contacting to the active region (21a,21b) of the substrate through the electrode 31. It is noted that the dummy patterned conductive layer 50b and the insulating spacers 20b shown in Fig. 1(e) are used for protecting the field isolation layer 17 during the etching of the metal layer 31. Therefore, the second patterned conductive layer 50b and the insulating spacers 20b are formed an etch inhibiting layer.

Uehara et al do not disclose that the contact hole in the insulating layer 32 is formed to expose a portion of the active region.

However, Rodder teaches in Fig. 4C that it would have been obvious to form the contact hole of Uehara extending through the insulating layer and exposing the active region of the substrate because this process step is well known for providing the electrical contacts to the active region of the substrate.

Regarding claims 17, 28 and 29, Uehara does not disclose the insulating layer comprises nitride. However, Rodder teaches in Fig. 4F that insulating layer 22 has high etch selectivity relative to the underlayer (column 6, lines 50-53) and insulating layer 22 can be any of a number of combinations of insulating material well known in the art (column 5, lines 32-34). Therefore, selecting SiN for an insulating layer of Uehara would have been obvious.

4. Claims 16-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US. 5,550,076) in view of Uehara et al (US. 5,698,902).

Art Unit: 2814

Regarding claims 16, 18-27, and 30-31, Chen discloses in Figs. 1, 2A, and related text, column 4, lines 35-67 through column 5, lines 1-20, a method of forming a contact hole for a microelectronic structure, the method comprising the steps of: defining adjacent active and field regions on a substrate 12; forming a field oxide isolation layer 14 on the field region by forming a trench in the substrate and filling the trench with the field isolation layer 14; simultaneously forming pattern 22I on the field isolation layer 14 adjacent the active region of the substrate and forming the patterned conductive layer 22G on the active region of the substrate spaced apart from the field isolation region 14, wherein each of the conductive pattern 22I and the patterned conductive layer 22G comprise a conductive portion and insulating spacer 24 along sidewalls thereof; forming an insulating layer 28 on the substrate 12, the field isolation layer 14 and the conductive pattern 22I; and forming a contact hole 33" in the insulating layer 28 exposing a portion of the active region adjacent the conductive pattern 22I and the field isolation layer 14. It is noted that because the conductive pattern 22I and the isolating spacers 24 are used for protecting the field isolation layer 14 during the etching of the contact hole 33", the conductive pattern 22I and the insulating spacers 24 are formed an etch inhibiting layer.

Chen does not disclose that the conductive pattern 22I is electrically isolated from circuitry.

However, Uehara et al teach in Fig. 1(e) the obviousness of forming a conductive pattern 50b on the field isolation layer 17 as an electrically isolated dummy electrode.

Art Unit: 2814

Accordingly, in view of the teaching of Uehara et al, it would have been obvious to electrically isolate the conductive pattern 22I of Chen from the circuitry because the same effects of reducing in the area occupied by the source/drain regions would result, such as taught by Uehara (column 4, lines 27-29).

Regarding claims 17, 28 and 29, Chen further discloses in Fig. 2A and column 8, lines 7-15 the obviousness of forming a selectively etching process between the insulating layers and the insulating spacers for preventing an etching over the underlying field oxide. And because the BPSG insulating layer 28 (column 5, line 7) includes phosphorus, the BPSG insulating layer 28 would have a higher etch rate than the silicon dioxide spacers 24 (column 7, lines 29-33). In addition, in view of the above teaching, selecting silicon nitride for a high etch selectively layer 28 relative to the underlayer would have been obvious because it is a design choice.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917.


Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

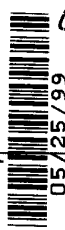
Application/Control Number: 09/318,188

Page 6

Art Unit: 2814

PHAT X. CAO
PC
January 28, 2000


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)		Attorney Entry Number 5649-129DV		Serial No. To Be Assigned <div style="text-align: center;">  09/318188 05/25/99 </div>	
		Applicant: Do-hyung Kim		Filing Date Concurrently Herewith	
		Group Art Unit To Be Determined 2816			

U. S. PATENT DOCUMENTS							
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
pc	1	5,365,111	11/94	Ramaswami et al.	257	768	
pc	2	5,306,945	4/94	Drummond	257	620	
pc	3	5,293,503	3/94	Nishigoori	174	250	
pc	4	5,164,806	11/92	Nagatomo et al.	257	395	
pc	5	5,475,266	12/95	Rodder	257	750	
pc	6	5,706,164	1/98	Jeng	438	239	
pc	7	5,550,076	8/96	Chen	438	253	
pc	8	5,436,188	7/95	Chen	438	397	
pc	9	5,273,936	12/93	Ikeda	438	453	
pc	10	5,174,858	12/92	Yamamoto et al.	156	643	
pc	11	5,698,902	12/97	Uehara	257	773	

FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation Yes No		
pc 12	59-76447	8/84	Japan	H01L 21/88	H01L 21/28		
pc 13	60-66444	4/85	Japan	H01L 21/76	H01L 21/88		
pc 14	53-108391	9/78	Japan	H01L 21/88	H01L 27/04		
pc 15	2724165	12/77	Germany				
pc 16	0523856A2	1/93	EPO	H01L 21/90			
pc 17	62-177945	8/87	Japan	257	758		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		

EXAMINER PHAT X. CAO	DATE CONSIDERED 1/28/00
--------------------------------	-----------------------------------

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conference and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited			Application No. 09/318,188		Applicant(s) Kim		
			Examiner Phat X. Cao		Group Art Unit 2814	Page 1 of 1	
U.S. PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	NAME		CLASS	SUBCLASS
	A	5,698,902	12/16/97	Uehara et al (filed 12/18/95)		257	773
	B	5,550,076	8/27/96	Chen (filed 9/11/95)		438	253
	C	5,475,266	12/12/95	Rodder		257	750
	D	5,357,133	12/18/97	Morita		257	316
	E						
	F						
	G						
	H						
	I						
	J						
	K						
	L						
	M						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N	59-76447	5/1/84	Japan	Kanamori		
	O						
	P						
	Q						
	R						
	S						
	T						
NON-PATENT DOCUMENTS							
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE
	U						
	V						
	W						
	X						

9/318188

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 5/25/99 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:

Black ink. Color.

☐ Color drawings are not acceptable until petition is granted.

Fig(s) _____

☐ Pencil and non black ink not permitted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84 (b)

☐ 1 full-tone set is required. Fig(s) _____☐ Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____☐ Poor quality (half-tone). Fig(s) _____

3. TYPE OF PAPER. 37 CFR 1.84(e)

☐ Paper not flexible, strong, white, and durable.

Fig(s) _____

☐ Erasures, alterations, overwritings, interlineations,☐ folds, copy machine marks not accepted. Fig(s) _____☐ Mylar, velum paper is not acceptable (too thin).

Fig(s) _____

4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:

☐ 21.0 cm by 29.7 cm (DIN size A4)☐ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)☐ All drawing sheets not the same size.

Sheet(s) _____

☐ Drawings sheets not an acceptable size. Fig(s) _____

5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm

SIZE: A4 Size

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm

SIZE: 8 1/2 x 11

Margins not acceptable. Fig(s) _____

☐ Top (T) _____ Left (L) _____☐ Right (R) _____ Bottom (B) _____

6. VIEWS. 37 CFR 1.84(h)

REMINDER: Specification may require revision to correspond to drawing changes.

Partial views. 37 CFR 1.84(h)(2)

☐ Brackets needed to show figure as one entity.

Fig(s) _____

☐ Views not labeled separately or properly.

Fig(s) _____

☐ Enlarged view not labeled separately or properly.

Fig(s) _____

7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)

☐ Hatching not indicated for sectional portions of an object.

Fig(s) _____

☐ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.

Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS.

37 CFR 1.84(i)

☐ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).

Fig(s) _____

11. SHADING. 37 CFR 1.84(m)

☐ Solid black areas pale. Fig(s) _____☐ Solid black shading not permitted. Fig(s) _____☐ Shade lines, pale, rough and blurred. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.

37 CFR 1.84(p)

☐ Numbers and reference characters not plain and legible.

Fig(s) _____

☐ Figure legends are poor. Fig(s) _____☐ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)

Fig(s) _____

☐ English alphabet not used. 37 CFR 1.84(p)(2)

Figs _____

☐ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)

Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)

☐ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____

15. NUMBERING OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from prior PTO-948 dated _____

17. DESIGN DRAWINGS. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____☐ Solid black shading not used for color contrast.

Fig(s) _____

COMMENTS

REVIEWER

WIS

DATE

6/22/99

TELEPHONE NO.

7033058484

ATTACHMENT TO PAPER NO.

6



Attorney's Docket No. 5649-129CXDV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
For:

Group Art Unit: 2814
Examiner: Phat Cao
ETCH INHIBITING STRUCTURES ON FIELD ISOLATION
REGIONS AND RELATED METHODS

#71B
5/11/00
Surles

May 2, 2000

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

MAY 11 2000
RECEIVED

Sir:

In response to the Office Action dated February 8, 2000, please amend the above-identified application as follows:

IN THE CLAIMS:

16.(Amended) A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer on said field region;

forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate wherein [said etch inhibiting layer is electrically isolated] said etch inhibiting layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer on said substrate, said field isolation layer, and said etch inhibiting layer; and

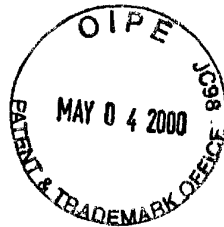
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01 FC:103

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In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 2



MAY 11 2000

Exhibit B1
forming a contact hole in said insulating layer exposing a portion of said active region adjacent said etch inhibiting layer and said field isolation layer.

23.(Amended) A method for forming a microelectronic structure, said method comprising the steps of:

B2
defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

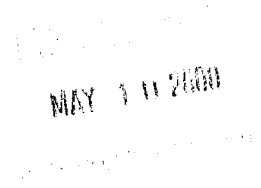
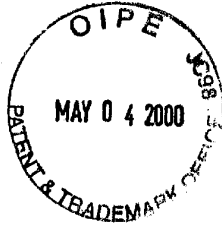
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate [wherein said second patterned layer is electrically isolated] wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.

Please add the following new claims.

32. A method according to Claim 23 wherein the insulating spacer of the second patterned layer extends to the active region of the substrate.

B3
¹⁴ 33. A method according to Claim ¹² 25 wherein the insulating layer and the insulating spacer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.

In re: Do-hyung Kim
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Attorney's Docket No. 5649.129CXDV
Page 3



34. A method according to Claim 23 wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a sidewall thereof.

35. A method according to Claim 16 wherein the insulating spacer of the etch inhibiting layer extends to the active region of the substrate.

36. A method according to Claim 16 wherein the insulating spacer and the insulating layer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.

REMARKS

The Applicant sincerely appreciates the Examiner's thorough review of the present application as evidenced by the Office Action of February 8, 2000. In response, the Applicant has amended the claims to more clearly define the claimed invention. The Applicant further submits that all claims are in condition for allowance for at least the reasons discussed below.

Claims 16-31 Are Patentable Over the Combination of Uehara et al. and Rodder

Claims 16-31 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 5,698,902 to Uehara et al. in view of U.S. Patent No. 5,475,266 to Rodder. The combination of these patents, however, fails to teach or suggest the methods of Claims 16-31.

Independent Claim 23, for example, recites a method for forming a microelectronic structure. This method includes:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

In re: Do-hyung Kim
Serial No.: 09/318,188
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Page 4



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MAY 11 2000

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.

The combination of the Uehara et al. and Rodder patents fails to teach or suggest this method.

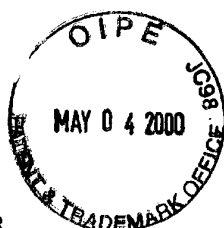
With reference to Figures 1(a)-1(e) relied on by the Office Action, the Uehara et al. patent states that:

dry etching is performed ... thereby forming a gate electrode 50a and a gate protective film 19a on the active region, while forming dummy electrodes 50b and dummy protective films 19b such that they extend over the active region and the isolation 17.

Uehara et al., col. 10, lines 1-8. (Underline added.) Accordingly, the Uehara et al. patent fails to teach or suggest an electrically isolated patterned conductive layer that does not extend beyond the field isolation layer over the active region of the substrate.

The Rodder patent fails to provide the missing teachings. In particular, the Rodder patent discusses a static random access memory (SRAM) cell structure as depicted in Figure 2. As shown in Figure 2, doped gate 14 extends over the doped moat 16 in substrate 12. Accordingly, the Rodder patent also fails to teach or suggest an electrically isolated patterned conductive layer that does not extend beyond the field isolation layer over the active region of the substrate. In other words, both the Uehara et al. patent and the Rodder patent fail to teach or suggest that an electrically isolated patterned conductive layer does not extend beyond a field isolation layer. As set forth in the MPEP, to establish a prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations. See MPEP § 2143.

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Filed: May 25, 1999
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The Applicant thus submits that the combination of the Uehara et al. and Rodder patents fails to teach or suggest the method of Claim 23. The Applicant further submits that Independent Claim 16 is patentable for at least the reasons discussed above with regard to Claim 23. In addition, the Dependent Claims are at least patentable as per the patentability of Independent Claims 16 and 23 from which they depend.

Claims 16-31 Are Patentable Over the Combination of Chen and Uehara et al.

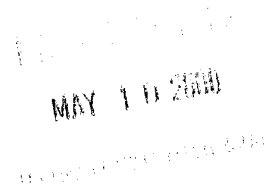
Claims 16-31 have also been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 5,550,076 to Chen in view of the Uehara et al. patent. The combination of these patents, however, fails to teach or suggest the methods of Claims 16-31.

As discussed above, Independent Claim 23 recites a method for forming a microelectronic structure. This method includes:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region; and
- forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.

The combination of the Chen and Uehara et al. patents fails to teach or suggest this method.

The Chen patent discusses a DRAM device formed over a device with field oxide regions and device areas with source/drain regions. As shown in Figure 1, the Chen patent discusses a DRAM device 10 including a field oxide region 14, a gate



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oxide layer 20, a gate electrode 22G, and a conductor structure 22I. More particularly, the:

conductor (or interconnector) structure 22I is provided on the surfaces of FOX 14 or elsewhere as seen in FIG. 2A to provide interconnections to other circuits.

Chen, col. 4, lines 55-57. Accordingly, this patent teaches away from a conductive layer on a field isolation layer wherein the conductive layer is electrically isolated from the substrate and from circuits thereon. A short circuit to the conductor (or interconnector) structure 22I may thus adversely affect the operation thereof. The Chen patent thus fails to teach or suggest the method of Claim 23.

The Uehara et al. patent fails to provide the missing teachings. In reference to Figures 1(a)-1(e), the Uehara et al. patent states that:

dry etching is performed ... thereby forming a gate electrode 50a and a gate protective film 19a on the active region, while forming dummy electrodes 50b and dummy protective films 19b such that they extend over the active region and the isolation 17.

Uehara et al., col. 10, lines 1-8. (Underline added.) It would not be obvious, however, to substitute the dummy electrodes 50b of the Uehara et al. patent for the interconnector 22I of the Chen patent because the Applicant believes that such a combination would not work. As discussed in the Chen patent:

Structure 22I is provided on the surfaces of FOX 14 or elsewhere as seen in FIG. 2A to provide interconnections to other circuits.

Chen, col. 4, lines 55-57. The Chen patent thus teaches away from the substitution of the dummy electrode 50b of the Uehara et al. patent for the interconnector structure 22I of the Chen patent because such a substitute would likely result in a non-functioning memory device. In other words, the Office Action fails to provide a reasonable expectation of success of the combination suggested therein. The Applicant points out that to establish a prima facie case of obviousness, there must be a reasonable expectation of success of the combination. See MPEP § 2143.



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MAY 10 2000

The combination of the cited patents thus fails to teach or suggest the method of Claim 23. Accordingly, the Applicant respectfully submits that Claim 23 is patentable. In addition, the Applicant submits that Claim 16 is patentable for the reasons discussed above with regard to Claim 23. In addition, the dependent claims are at least patentable as per the patentability of Independent Claims 16 and 23 from which they depend.

CONCLUSION

The Applicant sincerely appreciates the Examiner's through examination of this application. In response, the Applicant has shown that the cited art fails to teach or suggest the claimed methods. Accordingly, the Applicant submits that all pending claims in the present application clearly define over the cited art and are in condition for allowance. A Notice of Allowance is thus respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any further issues need to be addressed.

Respectfully submitted,

Scott C. Hatfield
Registration No. 38,176

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone (919) 854-1400
Facsimile (919) 854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on May 2, 2000.

Joyce Paoli
Date of Signature: May 2, 2000



Attorney's Docket No. 5649-129CXDV

GAU 2814 #
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
For: ETCH INHIBITING STRUCTURES ON FIELD ISOLATION
REGIONS AND RELATED METHODS
Date: May 2, 2000

Examiner: Phat Cao
Group Art Unit: 2814

Assistant Commissioner for Patents
Washington, DC 20231

RECEIVED
MAY 11 2000

Sir:

Transmitted herewith is an AMENDMENT in the above-identified patent application.

- ☐ Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.
- ☐ No additional fee is required.
- ☐ Other: Petition for Extension of Time for _____ month; Supplemental Information Disclosure Statement

The fee has been calculated as shown below:

(COL. 1)		(COL. 2)	(COL. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	RATE	ADDIT. FEE	OR RATE	ADDIT. FEE
Total	21-	16	5=	x 09=	\$	x 18=	\$90.00
Indep	2-	3	=	x 39=	\$	x 78=	\$
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+130=	\$	+260=	\$
				Total Add. Fee	\$	OR Total	\$ 90.00

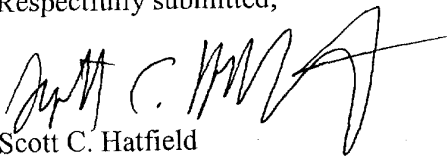
* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Page 2 of 2



- ☐ Please charge Deposit Account No. 50-0220 in the amount of \$
- ☒ A check in the amount \$90.00 to cover the additional claims.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0220.
- ☒ Any additional filing fees required under 37 C.F.R. § 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17.

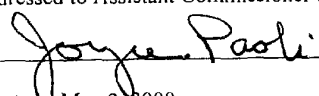
Respectfully submitted,


Scott C. Hatfield
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Attorney of Record

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Raleigh, North Carolina 27627
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Facsimile (919) 854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on May 2, 2000.


Joyce Paoli

Date of Signature: May 2, 2000

A circular stamp from the Patent & Trademark Office (PTO). The text "PTO" is at the top, "MAY 10 2000" is in the center, and "PATENT & TRADEMARK OFFICE" is around the bottom edge.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/318,188	05/25/99	KIM	D 5649-129DV

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH NC 27627

MMC1/0713

EXAMINER

CAO.P

ART UNIT

PAPER NUMBER

2814


DATE MAILED:

07/13/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/318,188	Applicant(s) Kim
	Examiner Phat X. Cao	Group Art Unit 2814



☒ Responsive to communication(s) filed on May 4, 2000.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 16-36 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 16-36 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been ☐ received.

☒ received in Application No. (Series Code/Serial Number) 08/748,148.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

U. S. Patent and Trademark Office
PTO-326 (Rev. 9-95)

Office Action Summary

Part of Paper No. 8

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23, 30-31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Ashida (US. 5,659,202).

Ashida discloses in Fig. 2 a method for forming a microelectronic structure, the method comprising the steps of: defining adjacent active region 3 and field region on a substrate 1, and circuits thereon; forming an oxide field isolation layer 2 which covers the field region; forming a first patterned layer 7 on the active region 3 of the substrate spaced apart from the oxide field isolation layer 2; and forming a second patterned layer 4 on the field isolation layer 2 adjacent the active region 3 of the substrate, wherein the second patterned layer 4 comprises a patterned conductive layer and an insulating spacer 5 along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon (column 5, lines 16-17).

Art Unit: 2814

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US. 5,550,076) in view of Uehara et al (US. 5,698,902).

Regarding claims 16, 18-27, 30-31 and 34, Chen discloses in Figs. 1, 2A, and related text, column 4, lines 35-67 through column 5, lines 1-20, a method of forming a contact hole for a microelectronic structure, the method comprising the steps of: defining adjacent active and field regions on a substrate 12; forming a field oxide isolation layer 14 on the field region by forming a trench in the substrate and filling the trench with the field isolation layer 14; simultaneously forming pattern 22I on the field isolation layer 14 adjacent the active region of the substrate and forming the patterned conductive layer 22G on the active region of the substrate spaced apart from the field isolation region 14, wherein each of the conductive pattern 22I and the patterned conductive layer 22G comprise a conductive portion and insulating spacer 24 along sidewalls thereof; forming an insulating layer 28 on the substrate 12, the field isolation layer 14 and the conductive pattern 22I; and forming a contact hole 33" in the insulating layer 28 exposing a portion of the active region adjacent the conductive pattern 22I and the field isolation layer 14. It is noted that because the conductive pattern 22I and the isolating spacers 24 are used for

Art Unit: 2814

protecting the field isolation layer 14 during the etching of the contact hole 33", the conductive pattern 22I and the insulating spacers 24 are formed an etch inhibiting layer.

Chen does not disclose that the conductive pattern 22I is a dummy pattern electrically isolated from the circuitry.

However, Uehara et al teach in Fig. 1(e) the obviousness of forming a conductive pattern 50b on the field isolation layer 17, wherein the conductive pattern 50b is a dummy pattern electrically isolated from circuitry and having a function as an etch inhibiting layer.

Accordingly, in view of the teaching of Uehara et al, it would have been obvious to either connect the conductive pattern 22I of Chen to the circuitry or disconnect the conductive pattern 22I from the circuitry because it is a desired choice and because in both cases, the conductive pattern 22I of Chen would perform the same function as an etch inhibiting layer.

Regarding claims 17, 28-29, 33, and 36, Chen further discloses in Fig. 2A and column 8, lines 7-15 the obviousness of forming a selectively etching process between the insulating layers and the insulating spacers for preventing an etching over the underlying field oxide. And because the BPSG insulating layer 28 (column 5, line 7) includes phosphorus, the BPSG insulating layer 28 would have a higher etch rate than the silicon dioxide spacers 24 (column 7, lines 29-33). In addition, in view of the above teaching, selecting silicon nitride for a high etch selectively layer 28 relative to the underlayer would have been obvious because it is a desired choice.

Art Unit: 2814

Regarding claims 32 and 35, Chen further discloses in Fig. 2A the insulating spacer 24 of the second patterned layer (or etch inhibiting layer) extending to the active region of the substrate 12.

Response to Arguments

5. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

In the remark, Applicant argues that the combination of Chen and Uehara will not provide a reasonable expectation of success because according to Applicant there is no motivation for electrically isolating the conductive pattern 22I of Chen from other circuits.

The Examiner respectfully disagrees because as discussed in ground of rejection, connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it is a desired choice depending upon the requirement by the layout of a wiring section in the integrated circuit. Therefore, it does not necessary connect the conductive pattern 22I to the circuitry if it does not require by the wiring section layout. In the other words, in view of teaching of Uehara, connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it involves only routine skill in the art and because in both cases, the conductive pattern 22I of Chen would perform the same function as an etch inhibiting layer as claimed.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917.

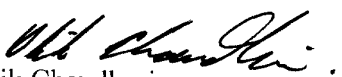
Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

Application/Control Number: 09/318,188

Page 7

Art Unit: 2814

PHAT X. CAO
PC
July 7, 2000


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

Notice of References Cited			Application No. 09/318,188		Applicant(s) Kim	
			Examiner Phat X. Cao		Group Art Unit 2814	Page 1 of 1
U.S. PATENT DOCUMENTS						
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,659,202	8/1997	Ashida (filed 4/10/96)	257	758
	B	5,932,920	8/1997	Kim et al (filed 4/17/96)	257	395
	C					
	D					
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FOREIGN PATENT DOCUMENTS						
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NON-PATENT DOCUMENTS						
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)				DATE
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**RESPONSE UNDER 37 C.F.R. § 1.116 – EXPEDITED
PROCEDURE – GROUP ART UNIT 2814**

Attorney's Docket No. 5649-129CXDV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188 ✓
Filed: May 25, 1999
For:

Group Art Unit: 2814
Examiner: Phat Cao

**METHODS OF FORMING ETCH INHIBITING
STRUCTURES ON FIELD ISOLATION REGIONS**

October 10, 2000

Box AF
Commissioner for Patents
Washington, DC 20231

#-9/c
HE
Aue
10/12/00

AMENDMENT AFTER FINAL

Sir:

In response to the Final Office Action dated July 13, 2000, please amend the above referenced application as indicated below. The Applicant respectfully requests entry of this Amendment After Final and allowance of the present application. Alternatively, the Applicant respectfully requests entry of this Amendment After Final as narrowing issues for further consideration as all amendments have been to either cancel a claim, rewrite dependent claims in independent form, or amend dependent claims to depend from currently pending claims. Accordingly, no new issues have been raised.

IN THE CLAIMS:

Please cancel Claim 23 without prejudice.

24.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 2

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

25.(Amended) [A method according to Claim 23 further comprising the steps of:] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 3

27.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

30.(Amended) A method according to Claim [23] 24 wherein said field isolation layer comprises oxide.

31.(Amended) A method according to Claim [23] 24 wherein [each of] said first [and second] patterned layer[s] comprises a patterned conductive layer.

32.(Amended) A method according to Claim [23] 25 wherein the insulating spacer of the second patterned layer extends to the active region of the substrate.

34.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 4

forming a first patterned layer on said active region of said substrate spaced apart from said field region; and

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a sidewall thereof.

REMARKS

The Applicant sincerely appreciates the Examiner's thorough review of the present application as evidenced by the Office Actions of February 8, 2000, and July 13, 2000. In response, the Applicant has canceled Claim 23; rewritten Claims 24, 25, 27, and 34 in independent form; amended Claims 30 and 31 to depend from Claim 24; and amended Claim 32 to depend from Claim 25. The Applicant will also show in the following remarks that all claims are patentable over the cited art. The Applicant thus requests allowance of the present application in due course. In addition, all remarks from Applicant's Amendment of May 2, 2000, are incorporated herein for the purposes of any subsequent appeal.

All Rejections Under 35 U.S.C. Sec. 102 Have Been Overcome

Independent Claim 23 and Dependent Claims 30-32 have been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by U.S. Patent No. 5,659,202 to Ashida. In this Amendment After Final, Independent Claim 23 has been canceled without prejudice to advance the prosecution of this application to allowance. In addition, Dependent Claims 30-32 have been amended to depend from Claims not

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 5

rejected under 35 U.S.C. Sec. 102. Accordingly, all rejections under 35 U.S.C. Sec. 102 have been overcome.

**Pending Claims 16-22 And 24-36 Are Patentable
Over the Combination of Chen and Uehara et al.**

Claims 16-22 and 24-36 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 5,550,076 to Chen ("Chen") in view of U.S. Patent No. 5,698,902 to Uehara et al. ("Uehara"). The combination of these patents, however, fails to teach or suggest the methods of Claims 16-22 and 24-36.

Claim 24, for example, recites a method for forming a microelectronic structure. This method includes:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region; and
- forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
- wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

The combination of the Chen and Uehara et al. patents fails to teach or suggest this method.

Chen discusses a DRAM device formed over a device with field oxide regions and device areas with source/drain regions. As shown in Figure 1, Chen discusses a DRAM device **10** including a field oxide region **14**, a gate oxide layer **20**, a gate electrode **22G**, and a conductor structure **22I**. More particularly, Chen states that the:

In re: Do-hyung Kim
Serial No.: 09/318,188
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Page 6

conductor (or interconnector) structure 22I is provided on the surfaces of FOX **14** or elsewhere as seen in FIG. 2A to provide interconnections to other circuits.

Chen, col. 4, lines 55-57. (Underline added.) Accordingly, Chen teaches away from the invention of Claim 24 wherein a conductive layer is on a field isolation layer wherein the conductive layer is electrically isolated from the substrate and circuits thereon. Chen thus fails to teach or suggest the method of Claim 24.

Uehara fails to provide the missing teachings. In reference to Figures 1(a)-1(e), Uehara states that:

dry etching is performed ... thereby forming a gate electrode **50a** and a gate protective film **19a** on the active region, while forming dummy electrodes 50b and dummy protective films **19b** such that they extend over the active region and the isolation **17**.

Uehara, col. 10, lines 1-8. (Underline added.) It would not be obvious to substitute the dummy electrodes **50b** of Uehara for the interconnector **22I** of Chen because Chen teaches away from such a combination, and such a combination would not work.

The Applicant points out that to establish a prima facie case of obviousness, three basic criteria must be met. The prior art references must teach or suggest all the claim limitations. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success of the combination. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. See MPEP § 2143. As recently affirmed by the Court of Appeals for the Federal Circuit, to support combining references in a § 103 rejection, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement is not met by broad, conclusory statements about teachings of references. *In re Dembiczak*, 50 USPQ2.d 1614, 1617 (Fed. Cir. 1999).

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Serial No.: 09/318,188
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Attorney's Docket No. 5649.129CXDV
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The Applicant thus submits that the combination of Chen and Uehara fails to teach or suggest the method of Claim 24 because Chen teaches away from such a combination, and because such a combination would not work. In particular, no motivation has been identified in the cited references or elsewhere in the art to substitute the dummy electrodes **50b** of Uehara for the structure **22I** of Chen, and, in fact, such motivation cannot exist because Chen states that the "structure **22I** is provided ... to provide interconnections to other circuits." (See Chen, col. 4, lines 55-57.) Moreover, if the dummy electrodes **50b** of Uehara were somehow substituted for the structure **22I** of Chen, the DRAM of Chen would not work because the resulting structure **22I** would not provide interconnections to other circuits.

In the Response to Arguments section of the Final Office Action, the Final Office Action states that:

Connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it is a desired choice depending upon the requirement by the layout of a wiring section in the integrated circuit. Therefore, it does not necessary connect the conductive pattern 22I to the circuitry if it does not require by the wiring section layout. In other words, in view of teaching of Uehara, connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it involves only routine skill in the art and because in both cases, the conductive pattern 22I of Chen would perform the same function as an etch inhibiting layer as claimed.

Final Office Action, page 5. The Applicant respectfully disagrees. As discussed above, Chen discusses a structure **22I** to provide interconnections to other circuits, and disconnecting the structure **22I** would appear to cause misoperation of the DRAM device. According to Chen, it appears that the structure **22I** would not be provided in situations where interconnection was not needed and that a resulting layout according to Chen would thus not include a structure **22I** where interconnection was not needed. Accordingly, there would be no motivation to substitute the electrodes **50b** of Uehara for the structure **22I** of Chen because in that

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
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case there would be no need for any such structure. Moreover, disconnecting the conductive pattern **22I** from the circuitry as suggested by the Final Office Action would appear to cause misoperation of the DRAM device of Chen, and motivation to disconnect the conductive pattern **22I** appears to come from improper hindsight based on the Applicant's disclosure.

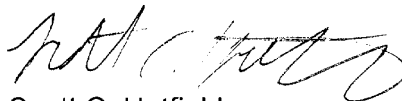
The combination of the cited patents thus fails to teach or suggest the method of Claim 24. Accordingly, the Applicant respectfully submits that Claim 24 is patentable. In addition, the Applicant submits that Claims 16, 25, 27, and 34 are patentable for the reasons discussed above with regard to Claim 24. In addition, Dependent Claims 17-22, 26, 28-33, and 35-36 are at least patentable as per the patentability of Independent Claims 16, 24, 25, 27, and 34 from which they depend.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 9

CONCLUSION

The Applicant sincerely appreciates the Examiner's through examination of this application. In response, the Applicant has shown that the cited art fails to teach or suggest the claimed methods. Accordingly, the Applicant submits that all pending claims in the present application clearly define over the cited art and are in condition for allowance. A Notice of Allowance is thus respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any further issues need to be addressed.

Respectfully submitted,

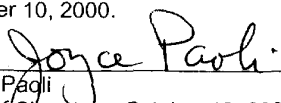


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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF, Commissioner for Patents, Washington, DC 20231, on October 10, 2000.



Joyce Paoli
Date of Signature October 10, 2000

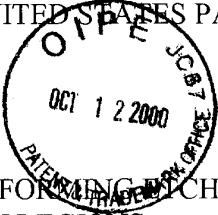
orney's Docket No. 56 129CXDV

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AF/2514
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
For: METHODS OF FORMING EACH INHIBITING STRUCTURES
ON FIELD ISOLATION REGIONS



Group Art Unit: 2814
Examiner: Phat Cao

Date: October 10, 2000

Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith is an AMENDMENT in the above-identified patent application.

- ☒ Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.
- ☐ No additional fee is required.
- ☐ Other:

The fee has been calculated as shown below:

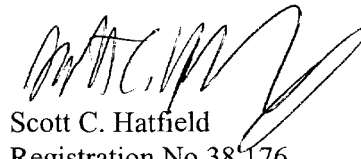
(COL. 1)		(COL. 2)	(COL. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	RATE	ADDIT. FEE	OR RATE	ADDIT. FEE
Total	* 20	** 21	= 0	x 09=	\$	x 18=	\$
Indep	* 5	*** 3	= 2	x 40=	\$	x 80=	\$160.00
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+135=	\$	+270=	\$
				Total Add. Fee	\$	OR Total	\$ 160.00

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

in re: Do-hyung Kim
Serial No.: 09/318,188
Page 2

- ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____.
- ☒ A check in the amount \$160.00 to cover the additional fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0220.
- ☒ Any additional filing fees required under 37 C.F.R. § 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17.

Respectfully submitted,

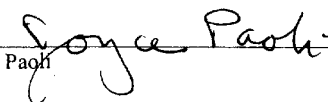


Scott C. Hatfield
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Attorney of Record

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on October 10, 2000.



Joyce Paoli



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/318,188	05/25/99	KIM	5649-129DV

020792 MM21/1023
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37429
RALEIGH NC 27627

EXAMINER
CAD.P


ART UNIT	PAPER NUMBER
2814	10

DATE MAILED: 10/23/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Advisory Action	Application No. 09/318,188	Applicant(s) Kim
	Examiner Phat X. Cao	Group Art Unit 2814



THE PERIOD FOR RESPONSE: [check only a) or b)]

a) ☒ expires 3 months from the mailing date of the final rejection.

b) ☐ expires either three months from the mailing date of the final rejection, or on the mailing date of this Advisory Action, whichever is later. In no event, however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition, and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

☐ Appellant's Brief is due two months from the date of the Notice of Appeal filed on _____ (or within any period for response set forth above, whichever is later). See 37 CFR 1.191(d) and 37 CFR 1.192(a).

Applicant's response to the final rejection, filed on Oct 12, 2000 has been considered with the following effect, but is NOT deemed to place the application in condition for allowance:

☒ The proposed amendment(s):

☐ will be entered upon filing of a Notice of Appeal and an Appeal Brief.

☒ will not be entered because:

☒ they raise new issues that would require further consideration and/or search. (See note below).

☐ they raise the issue of new matter. (See note below).

☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

☐ they present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE: the scopes of the amended dependent claims 30, 31 and 32 are changed because the dependency of each of the claims 30,31, and 32 are changed. However, the amendment will be entered if claims 16-22, 24-29, 33-36 are filed separately.

☐ Applicant's response has overcome the following rejection(s):

☐ Newly proposed or amended claims _____ would be allowable if submitted in a separate, timely filed amendment cancelling the non-allowable claims.

☐ The affidavit, exhibit or request for reconsideration has been considered but does NOT place the application in condition for allowance because:

☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

☒ For purposes of Appeal, the status of the claims is as follows (see attached written explanation, if any):

Claims allowed: _____


Claims objected to: _____

Claims rejected: 16-36

☐ The proposed drawing correction filed on _____ ☐ has ☐ has not been approved by the Examiner.

☐ Note the attached Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Other


OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

AF/GP 2814
PATENT

#11/Ext. of
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T. 4 w/br
11-15-00

Examiner: Phat Cao

Group Art Unit: 2814

Date: November 10, 2000

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TECHNOLOGY CENTER 2800

1. This is a petition for an extension of time for a total period of one (1) month to respond to the Official Action dated
2. A response in connection with the matter for which this extension is requested:
☒ is filed herewith.
☐ has been filed.
3. Applicant is
☐ a small entity--verified statement:
☐ attached.
☐ already filed.
☒ other than a small entity.
4. Calculation of extension fee (37 C.F.R. § 1.17(a)-(d)):


	Total Months <u>Requested</u>	Fee For Other <u>Than Small Entity</u>	Fee for <u>Small Entity</u>
<input checked="" type="checkbox"/>	one month	\$110.00	\$55.00
<input type="checkbox"/>	two months	\$390.00	\$195.00
<input type="checkbox"/>	three months	\$890.00	\$445.00
<input type="checkbox"/>	four months	\$1,390.00	\$695.00

110.00 00

In re: Application of Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Page 2

☐ Charge Deposit Account No. 50-0220 for any additional extension and/or fee required or credit for any excess fee paid.

Respectfully submitted,

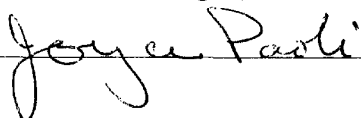

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"Express Mail" mailing label number EL682672863US
Date of Deposit: November 10, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box AF, Commissioner of Patents, Washington, DC 20231.

Joyce Paoli



RESPONSE UNDER 37 C.F.R. § 1.116 – EXPEDITED
PROCEDURE – GROUP ART UNIT 2814

Attorney's Docket No. 5649-129CXDV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
For:

Group Art Unit: 2814
Examiner: Phat Cao

METHODS OF FORMING ETCH INHIBITING
STRUCTURES ON FIELD ISOLATION REGIONS

#12/D
T.Y. WONG
11-15-00
NE

November 10, 2000

Box AF
Commissioner for Patent
Washington, DC 20231



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NOV 15 2000

TECHNOLOGY CENTER

SECOND AMENDMENT AFTER FINAL

Sir:

In response to the Final Office Action dated July 13, 2000, and the Advisory Action of October 23, 2000, please amend the above referenced application as indicated below. The Applicant respectfully requests entry of this Amendment After Final and allowance of the present application. Alternatively, the Applicant respectfully requests entry of this Amendment After Final as narrowing issues for further consideration as all amendments have been to either cancel claims, or rewrite dependent claims in independent form. Accordingly, no new issues have been raised.

IN THE CLAIMS:

Please cancel Claim 23 without prejudice.

24.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits

thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate

spaced apart from said field region; and

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 2

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

25.(Amended) [A method according to Claim 23 further comprising the steps of:] A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

Amended
E3
Cont.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 3

27.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:
defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced apart from said field region; and
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

Please cancel Claims 30-32.

34.(Amended) [A method according to Claim 23] A method for forming a microelectronic structure, said method comprising the steps of:
defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced apart from said field region; and
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 4

*sub
vs
cont.*
a dummy pattern electrically isolated from the substrate and circuits thereon;

wherein the first patterned layer comprises a patterned gate layer and
an insulating gate spacer along a sidewall thereof.

REMARKS

The Applicant sincerely appreciates the Examiner's thorough review of the present application as evidenced by the Office Actions of February 8, 2000, and July 13, 2000. In response, the Applicant has canceled Claims 23 and 30-32; and rewritten Claims 24, 25, 27, and 34 in independent form. The Applicant will also show in the following remarks that all claims are patentable over the cited art. The Applicant thus requests allowance of the present application in due course. In addition, all remarks from Applicant's Amendment of May 2, 2000, are incorporated herein for the purposes of any subsequent appeal.

All Rejections Under 35 U.S.C. Sec. 102 Have Been Overcome

Independent Claim 23 and Dependent Claims 30-32 have been rejected under 35 U.S.C. Sec. 102(b) as being anticipated by U.S. Patent No. 5,659,202 to Ashida. In this Amendment After Final, Claims 23 and 30-32 have been canceled without prejudice to advance the prosecution of this application to allowance. Accordingly, all rejections under 35 U.S.C. Sec. 102 have been overcome.

Pending Claims 16-22 And 24-36 Are Patentable Over the Combination of Chen and Uehara et al.

Claims 16-22 and 24-36 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 5,550,076 to Chen ("Chen") in view of U.S. Patent No. 5,698,902 to Uehara et al. ("Uehara"). The combination of these patents, however, fails to teach or suggest the methods of Claims 16-22 and 24-36.

Claim 24, for example, recites a method for forming a microelectronic structure. This method includes:

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 5

defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced apart from said field region; and
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

The combination of the Chen and Uehara et al. patents fails to teach or suggest this method.

Chen discusses a DRAM device formed over a device with field oxide regions and device areas with source/drain regions. As shown in Figure 1, Chen discusses a DRAM device **10** including a field oxide region **14**, a gate oxide layer **20**, a gate electrode **22G**, and a conductor structure **22I**. More particularly, Chen states that the:

conductor (or interconnector) structure **22I** is provided on the surfaces of FOX **14** or elsewhere as seen in FIG. 2A to provide interconnections to other circuits.

Chen, col. 4, lines 55-57. (Underline added.) Accordingly, Chen teaches away from the invention of Claim 24 wherein a conductive layer is on a field isolation layer wherein the conductive layer is electrically isolated from the substrate and circuits thereon. Chen thus fails to teach or suggest the method of Claim 24.

Uehara fails to provide the missing teachings. In reference to Figures 1(a)-1(e), Uehara states that:

dry etching is performed ... thereby forming a gate electrode **50a** and a gate protective film **19a** on the active region, while forming dummy electrodes **50b** and dummy protective films **19b** such that they extend over the active region and the isolation **17**.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 6

Uehara, col. 10, lines 1-8. (Underline added.) It would not be obvious to substitute the dummy electrodes **50b** of Uehara for the interconnector **22I** of Chen because Chen teaches away from such a combination, and such a combination would not work.

The Applicant points out that to establish a prima facie case of obviousness, three basic criteria must be met. The prior art references must teach or suggest all the claim limitations. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success of the combination. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. See MPEP § 2143. As recently affirmed by the Court of Appeals for the Federal Circuit, to support combining references in a § 103 rejection, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement is not met by broad, conclusory statements about teachings of references. *In re Dembiczak*, 50 USPQ2.d 1614, 1617 (Fed. Cir. 1999).

The Applicant thus submits that the combination of Chen and Uehara fails to teach or suggest the method of Claim 24 because Chen teaches away from such a combination, and because such a combination would not work. In particular, no motivation has been identified in the cited references or elsewhere in the art to substitute the dummy electrodes **50b** of Uehara for the structure **22I** of Chen, and, in fact, such motivation cannot exist because Chen states that the "structure **22I** is provided ... to provide interconnections to other circuits." (See Chen, col. 4, lines 55-57.) Moreover, if the dummy electrodes **50b** of Uehara were somehow substituted for the structure **22I** of Chen, the DRAM of Chen would not work because the resulting structure **22I** would not provide interconnections to other circuits.

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Serial No.: 09/318,188
Filed: May 25, 1999
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In the Response to Arguments section of the Final Office Action, the Final Office Action states that:

Connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it is a desired choice depending upon the requirement by the layout of a wiring section in the integrated circuit. Therefore, it does not necessary connect the conductive pattern 22I to the circuitry if it does not require by the wiring section layout. In other words, in view of teaching of Uehara, connecting the conductive pattern 22I to the circuitry or disconnecting the conductive pattern 22I from the circuitry would have been obvious because it involves only routine skill in the art and because in both cases, the conductive pattern 22I of Chen would perform the same function as an etch inhibiting layer as claimed.

Final Office Action, page 5. The Applicant respectfully disagrees. As discussed above, Chen discusses a structure **22I** to provide interconnections to other circuits, and disconnecting the structure **22I** would appear to cause misoperation of the DRAM device. According to Chen, it appears that the structure **22I** would not be provided in situations where interconnection was not needed and that a resulting layout according to Chen would thus not include a structure **22I** where interconnection was not needed. Accordingly, there would be no motivation to substitute the electrodes **50b** of Uehara for the structure **22I** of Chen because in that case there would be no need for any such structure. Moreover, disconnecting the conductive pattern **22I** from the circuitry as suggested by the Final Office Action would appear to cause misoperation of the DRAM device of Chen, and motivation to disconnect the conductive pattern **22I** appears to come from improper hindsight based on the Applicant's disclosure.

The combination of the cited patents thus fails to teach or suggest the method of Claim 24. Accordingly, the Applicant respectfully submits that Claim 24 is patentable. In addition, the Applicant submits that Claims 16, 25, 27, and 34 are patentable for the reasons discussed above with regard to Claim 24. In addition, Dependent Claims 17-22, 26, 28-29, 33, and 35-36 are at least patentable as per

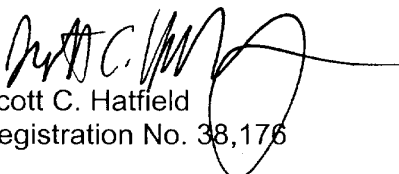
In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Attorney's Docket No. 5649.129CXDV
Page 8

the patentability of Independent Claims 16, 24, 25, 27, and 34 from which they depend.

CONCLUSION

The Applicant sincerely appreciates the Examiner's thorough examination of this application. In response, the Applicant has shown that the cited art fails to teach or suggest the claimed methods. Accordingly, the Applicant submits that all pending claims in the present application clearly define over the cited art and are in condition for allowance. A Notice of Allowance is thus respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any further issues need to be addressed.

Respectfully submitted,

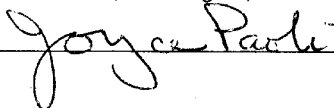

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"Express Mail" mailing label number EL682672863US
Date of Deposit: November 10, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box AF, Commissioner of Patents, Washington, DC 20231.

Joyce Paoli



Attorney's Docket No. 5649-129CXDV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim;
Serial No.: 09/318,188
Filed: May 25, 1999
For: METHODS OF FORMING ETCH INHIBITING STRUCTURES ON
FIELD ISOLATION REGIONS

Group Art Unit: 2814
Examiner: Phat Cao

BOX AF
Commissioner for Patents
Washington, DC 20231



Date: November 10, 2000

RECEIVED
NOV 15 2000

TECHNOLOGY CENTER 2800

Sir:

Transmitted herewith is an AMENDMENT in the above-identified patent application.

- ☐ Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.
- ☐ No additional fee is required.
- ☒ Other: 1 Month Extension of Time
- The fee has been calculated as shown below:

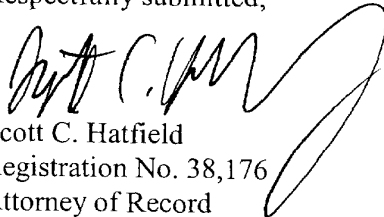
(COL. 1)		(COL. 2)	(COL. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	RATE	ADDIT. FEE	OR RATE	ADDIT. FEE
Total	* 17	** 21	= 0	x 09=	\$	x 18=	\$
Indep	* 5	*** 5	= 0	x 40=	\$	x 80=	\$
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+135=	\$	+270=	\$
				Total Add. Fee \$		OR Total	\$

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

In re: Do-hyung Kim;
Serial No.: 09/318,188
Page 2

- ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____.
- ☒ A check in the amount \$110.00 to cover the additional fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0220.
- ☒ Any additional filing fees required under 37 C.F.R. § 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17.

Respectfully submitted,

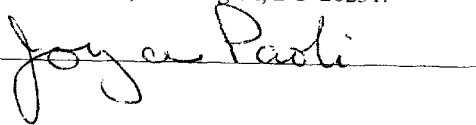

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Joyce Paoli





**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/318,188 05/25/99 KIM

D 5649-129DV

020792 MMC2/1205
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH NC 27627

EXAMINER

CAD, P

ART UNIT

PAPER NUMBER

2814


DATE MAILED:

12/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/318,188	Applicant(s) Kim
	Examiner Phat X. Cao	Group Art Unit 2814



☒ Responsive to communication(s) filed on Nov 10, 2000.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 16-22, 24-29, and 33-36 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 16-22, 24-29, and 33-36 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) 08/748,148.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

U. S. Patent and Trademark Office
PTO-326 (Rev. 9-95)

Office Action Summary

Part of Paper No. 13

NVIDIA Corp.
Exhibit 1102
Page 098

Art Unit: 2814

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. The cancellation of claims 23, and 30-32 in Paper No. 12 is acknowledged.

Claim Rejections - 35 USC § 112

3. Claim 28 recites the limitation "said insulating layer" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 24-27 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Motonami (US. 5,441,916).

With respect to claims 24 and 26, Motonami discloses in Figs. 3A-3B and 4A a method for forming a microelectronic structure, the method comprising the steps of: defining adjacent active and field regions on a substrate, and circuits thereon; forming a trench in the substrate 11 and filling the trench with a field isolation layer 12; forming a first patterned layer 18 on the active

Art Unit: 2814

region of the substrate spaced apart from the field region; and forming a second patterned layer 44 on the field isolation layer 12 adjacent the active region of the substrate wherein the second patterned layer 44 comprises a patterned conductive layer 24 and an insulating spacer 26 along a sidewall of the patterned conductive layer, wherein the patterned conductive layer 24 does not extend over the active region of the substrate, and wherein the patterned conductive layer 24 is a dummy pattern electrically isolated from the substrate and circuits thereon (column 4, lines 42-47); wherein the steps of forming the first patterned layer 18 and forming the second patterned layer 44 are performed simultaneously (see Fig. 3A).

With respect to claims 27 and 34, Fig. 4A of Motonami further discloses an insulating gate spacer 2 formed along the sidewall of the first patterned layer 18.

With respect to claim 25, Fig. 9A of Motonami also discloses the steps of forming an insulating layer 33 covering the substrate, the field isolation layer and the first and second patterned layers; and forming a contact hole exposes a portion of the active region 15 between the first and second patterned layers.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2814

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 16-22, 24-29, and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michihiro (JP. 4-63437) in view of Chen (US. 5,550,076).

Regarding claims 16, 18-22, 24-27 and 34, Michihiro discloses in Figs. 2(e) and 4(b) and abstract, a method of forming a contact hole for a microelectronic structure, the method comprising the steps of: defining adjacent active and field regions on a substrate 1; forming a field oxide isolation layer 2 on the field region by forming a trench in the substrate and filling the trench with the field isolation layer 2; simultaneously forming a second pattern layer 15 on the field isolation layer 2 adjacent the active region of the substrate and forming a first pattern layer 4a on the active region of the substrate spaced apart from the field isolation region, wherein the second pattern layer 15 comprises a patterned conductive layer which does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon (see abstract); forming an insulating layer 5 on the substrate 1, the field isolation layer 2 and the first and second pattern layers; and forming a contact hole 8 in the insulating layer 5 wherein the contact hole 8 exposes a portion of the active region between the first and second patterned layers. It is noted that because the first patterned layer 15 is formed on the field isolation layer 2, the field isolation layer 2 would be protected during the etching of the contact hole 8. Therefore, the first patterned layer 15 is inherently formed as an etch inhibiting layer.

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Michihiro does not disclose an insulating spacer formed along a sidewall of the first patterned layer 4a and a sidewall of the second pattern layer 15.

However, Chen teaches in Fig. 1 the obviousness of forming a second patterned layer 22I on a field oxide isolation layer 14 and a first patterned layer 22G on the active region of a substrate, wherein the sidewall of the second patterned layer 22I and the sidewall of the first patterned layer 22G, each has an insulating spacer 24 formed thereon. Accordingly, it would have been obvious to modify the device structure of Michihiro by forming the insulating spacers along a sidewall of the first and second patterned layers, because as is well known, the insulating sidewall spacers would protect and prevent the first patterned conductive layer (gate electrode) and the second patterned conductive layer from contacting with the other adjacent elements.

Regarding claims 17, 28-29, 33, and 36, Chen further discloses in Fig. 2A and column 8, lines 7-15 the obviousness of forming a selectively etching process between the insulating layers and the insulating spacers for preventing an etching over the underlying field oxide. And because the BPSG insulating layer 28 (column 5, line 7) includes phosphorus, the BPSG insulating layer 28 would have a higher etch rate than the silicon dioxide spacers 24 (column 7, lines 29-33). In addition, in view of the above teaching, selecting silicon nitride for a high etch selectively layer 28 relative to the underlayer would have been obvious because it is a desired choice.

Regarding claim 35, Chen further discloses in Fig. 2A the insulating spacer 24 of the second patterned layer (or etch inhibiting layer) extending to the active region of the substrate 12.

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8. Claims 16, 18-22, 24-27, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michihiro (JP. 4-63437) in view of Motonami (US. 5,441,916).

As discussed in detail above, Figs. 2(e) and 4(b) of Michihiro substantially read on the above claims, except that Figs. 2(e) and 4(b) do not disclose the step of forming an insulating spacer along a sidewall of the gate electrode patterned layer 4a and a sidewall of the dummy patterned layer 15.

However, Motonami teaches in Fig. 4A the obviousness of forming a gate electrode patterned layer 18 on the active region of a substrate and a dummy patterned layer 44 on a field oxide isolation layer 12, wherein the sidewall of the gate electrode patterned layer 18 and the sidewall of the dummy patterned layer 44, each has an insulating spacer formed thereon. Accordingly, it would have been obvious to modify the device structure of Michihiro by forming the insulating spacers along a sidewall of the first and second patterned layers, because as is well known, the insulating sidewall spacers would protect and prevent the first patterned conductive layer (gate electrode) and the second patterned conductive layer from contacting with the other adjacent elements.

Response to Arguments

9. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

Application/Control Number: 09/318,188

Page 7

Art Unit: 2814

Applicant's arguments are persuasive. However, the new references are applied in the new ground of rejection.


Conclusion

10. This action is made non-final

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PC
November 29, 2000


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

Notice of References Cited				Application No. 09/318,188		Applicant Kim	
				Examiner Phat X. Cao		Group Art Unit 2814	
						Page 1 of 1	
U.S. PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	NAME		CLASS	SUBCLASS
	A	5,441,916	8/1995	Motonami		437	195
	B	5,789,313	8/1995	Lee (filed 9/1/92)		438	599
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						
	L						
	M						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N	4-63437	2/1992	Japan	Michihiro	-----	-----
	O	9-64195	3/1997	Japan	Sony Corp.	-----	-----
	P	8-335701	2/1992	Japan	Sony Corp.	-----	-----
	Q						
	R						
	S						
	T						
NON-PATENT DOCUMENTS							
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE
	U						
	V						
	W						
	X						

Attorney's Docket No. 5649-129CXDV



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999

Group Art Unit: 2814
Examiner: Phat X. Cao

For: METHODS OF FORMING ETCH INHIBITING STRUCTURES ON
FIELD ISOLATION REGIONS

March 5, 2001

BOX NON-FEE AMENDMENT
Commissioner for Patents
Washington, DC 20231

**AMENDMENT RESPONSIVE TO THE
OFFICIAL ACTION MAILED DECEMBER 5, 2000**

Sir:

In response to the Official Action dated December 5, 2000, please amend the above-identified application as indicated below. Attached hereto at pages 13-16 is a marked up version of the changes made to the title and claims by the current amendment. The marked up version of the changes is captioned "Version With Markings To Show Changes Made".

In the Claims:

Please enter amended Claims 16, 19, 24-25, 27, and 34 as indicated below, and please also enter the cancellation of Claim 18.

16. (Twice Amended) A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer on said field region;

forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;

forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, wherein the

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Page 2 of 16

second patterned conductive layer does not extend over the active region of the substrate, and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer; and

forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer.

Please cancel claim 18.

~~319~~ (Amended) A method according to Claim ~~16~~ wherein said first patterned conductive layer comprises a conductive portion and insulating spacers along sidewalls thereof.

~~1124~~ (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
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¹²
~~25~~. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced apart from said field region;
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and
forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

¹³
~~27~~. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced apart from said field region;
forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

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Serial No.: 09/318,188
Filed: May 25, 1999
Page 4 of 16

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

¹⁸
34. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer which covers said field region;

forming a first patterned layer on said active region of said substrate spaced apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a sidewall thereof.

Please enter new Claims 37 and 38 as indicated below.

¹⁸
37. (New) A method according to Claim 16 wherein contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
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¹⁰
~~38~~. (New) A method according to Claim ~~16~~¹ wherein at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer.

Ex.
cont.

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
Page 6 of 16

REMARKS

Applicant appreciates the thorough examination of the present application that is reflected in the Official Action of December 5, 2000. Applicant also appreciates the Examiner's indication that the finality of the Final Official Action of July 13, 2000 is withdrawn. In particular, Applicant appreciates the Examiner's indication that all of the rejections under 35 U.S.C. § 102(b) as being anticipated by Ashida (U.S. 5,659,202) have been withdrawn, and that all of the rejections under 35 U.S.C. § 103(a) over Chen (U.S. 5,550,076) in view of Uehara et al. (U.S. 5,698,902) have also been withdrawn.

In response to the Official Action of December 5, 2000, Applicant has amended each of Independent Claims 16, 24, 25, 27, and 34. Claim 18 has been cancelled, and the dependency of Claim 19 has also been changed from Claim 18 to Claim 16. Applicant has also added new dependent Claims 37-41 to further distinguish over the cited references. Accordingly, Applicant respectfully requests withdrawal of the rejections and allowance of the present application.

The 35 U.S.C. 112, First Paragraph Rejection Has Been Overcome

Claim 28 was rejected under 35 U.S.C. § 112, with the Office Action stating that there was insufficient antecedent basis for the recitation "said insulating layer" in line 2 of Claim 28. Applicant respectfully submits that the above amendments to Claim 27 rectify this antecedent basis problem. Accordingly, the Applicant respectfully submits that the rejection under 35 U.S.C. § 112 has been overcome and should be withdrawn.

Independent Claims 24, 25, 27, and 34 Are Patentable Over the Motonami Reference

Independent Claims 24, 25, 27 and 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Motonami. For purposes of analysis, Applicant will discuss Claim 25, since the comments made with respect to Claim 25 are applicable to Independent Claims 24, 27, and 34.

Claim 25 recites a method for forming a microelectronic structure. As amended, the method of Claim 25 comprises the steps of:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region;

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forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.
[Underlining added.]

At page 3, lines 11-14, the Official Action states that:

With respect to Claim 25, Fig. 9A of Motonami also discloses the steps of forming an insulating layer 33 covering the substrate... and forming a contact hole exposes a portion of the active region 15 between the first and second patterned layers.

For the reasons discussed below, Applicant respectfully traverses the above grounds of rejection since Motonami fails to teach or suggest at least the underlined recitations of Claim 25 above.

For example, the dummy interconnection 44 of Montonami is **not** adjacent an active region of the substrate that includes a patterned layer on the active region of the substrate. Rather, as shown in FIG. 4A of Motonami, gate 18 is formed on the field oxide film 12 adjacent the active region 15 including the second gate 18. Stated in other words, the dummy interconnection 44 of Motonami appears to be on the field oxide film 12 opposite the active region having the gate 18 thereon. As such, Motonami fails to teach or suggest this recitation of each of the independent claims.

Assuming for the sake of argument that gates 18 of Motonami including gate oxide films 19, gate electrodes 20, overlapping insulation films 21, and sidewall insulation films 22 (as shown in FIG. 1A) are interpreted as first and second patterned layers of Claim 25, Motonami fails to teach or suggest forming an insulating layer covering the gates 18 and forming a contact hole in the insulating layer exposing an active region between the gates 18. Instead, Motonami shows that a storage node is formed directly on the gates 18 and diffusion layer 15 without forming an insulating layer on the gates and without forming a contact hole through the insulating layer to expose the diffusion layer.

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For at least the above reasons, Motonami fails to teach or suggest all of the recitations of Claim 25. Similarly, Motonami fails to teach or suggest the corresponding recitations in Independent Claims 24, 27 and 34. Accordingly, Applicant respectfully submits that Claims 24, 25, 27 and 34 are patentable over Motonami. In addition Dependent Claims 26, 28-33, and 35-36 are at least patentable over Motonami as per the patentability of Independent Claims 24, 25, 27, and 34 from which they depend.

Claims 16-22, 24-29, and 33-36 Are Patentable Over Michihiro In View of Chen

Claims 16-22, 24-29, and 33-36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Michihiro (JP. 4-63437) in view of Chen (US. 5,550,076). Again, for purposes of analysis, Claim 25 will be discussed since the comments made with regard to Claim 25 are applicable to the other independent claims.

In rejecting Claims 16-22, 24-29, and 33-36, the Official Action concedes that Michihiro does not disclose an insulating spacer formed along a sidewall of the first patterned layer 4a and sidewall of a second patterned layer 15. However, the Official Action takes the position that "Chen teaches ... forming a second patterned layer 22I ...and a first patterned layer 22G ..., each [having] an insulating 24 spacer formed thereon."

Applicant respectfully submits, however, that there is no clear and particular evidence of a motivation for modifying Michihiro in view of Chen. As noted in the previous response, Chen discusses a DRAM device formed over a device with field oxide regions and device areas with source/drain regions. As shown in FIG. 1, Chen discusses a DRAM device 10 including a field oxide region 14, a gate oxide layer 20, a gate electrode 22G, and a conductor structure 22I. More particularly, Chen states that the:

conductor (or interconnector) structure 22I is provided on the surfaces of FOX 14 or elsewhere as seen in FIG. 2A to provide interconnections to other circuits.

Chen, column 4, lines 55-57. (underlining added)

Accordingly, Chen teaches away from the recitations of Claim 25 wherein a conductive layer is on a field isolation layer wherein the conductive layer is electrically isolated from the substrate and circuits thereon. Thus, it would not be obvious to substitute the interconnector 22I of Chen for the dummy patterns 15 of Michihiro, because Chen teaches away from such a combination.

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Moreover, such a combination simply would not work. If the structure 22I of Chen were somehow substituted for dummy electrodes of Michihiro, the DRAM of Chen would not work because the resulting structure 22I would not provide interconnections to other circuits. On the other hand, the modified device of Michihiro would not work since there is no suggestion with respect to how the dangling interconnections of Chen would be interconnected, and because Michihiro explicitly discusses dummy patterns "to make the channels of mixed field effect transistors the same length and suppress fluctuation thereof" Michihiro, Abstract.

There is also nothing in Chen that would suggest the use of spacers on sidewalls of a dummy pattern. This is because Chen does not teach or suggest the use of a dummy pattern such as that taught in FIG. 4B of Michihiro. Instead, Chen states that the structure 22I is used to provide interconnections to other circuits. Accordingly, apart from hindsight based on the Applicant's disclosure, there would be no motivation to randomly substitute the insulating spacers 24 of Chen into the structure shown in FIG. 4B of Michihiro.

As discussed above with respect to Michihiro, there is simply no mention in Michihiro that it is desirable to prevent damage to the field oxide layer 2. There is nothing in Michihiro which suggests that there is need to include spacers that would prevent damage to the field oxide layer in the event the contact hole is misaligned. Thus, there would be no motivation based on Michihiro to include the spacers of Chen.

Applicant respectfully submits that neither reference appreciates that misalignment of the contact hole during formation thereof can be a problem that can damage the field oxide layer. The only motivation for including these spacers in the structure of Michihiro appears to come from improper hindsight that is based solely on the Applicant's disclosure.

Thus, the proposed combination of patents fails to suggest the method of Claim 25. Accordingly, Applicant respectfully submits that Claim 25 is patentable over the combination of Michihiro in view of Chen. In addition, Applicant submits that Claims 16, 24, 27, and 34 are patentable over the combination of Michihiro in view of Chen for at least the reasons discussed above, with regard to Claim 25. In addition, Dependent Claims 17, 19-22, 26, 28-29, 33, and 35-36 are at least patentable over the combination of Michihiro in view of Chen as per the patentability of Independent Claims 16, 24-25, 27, and 34, from which they depend.

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Independent Claims 16, 18-22, 24-27, and 34-35 Are Patentable Over Michihiro In View Of Motonami

Independent Claims 16, 18-22, 24-27, and 34-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michihiro (JP. 4-63437) in view of Motonami. Again, for purposes of analysis, Claim 25 will be discussed since the comments made with respect to Claim 25 are applicable to the other independent claims.

In rejecting Claim 25, page 5 of the Official Action concedes that Michihiro does "not disclose the step of forming an insulating spacer along a sidewall of the gate electrode patterned layer 4a and a sidewall of the dummy patterned layer 15." However, the Official Action then takes the position that "Motonami teaches in FIG. 4A the obviousness of forming a gate electrode patterned layer 18 ... and a dummy patterned layer 44... each [having] an insulating spacer formed thereon." In view of this alleged teaching, the Official Action asserts that:

Accordingly, it would have been obvious to modify the device structure of Michihiro by forming the insulating spacers along a sidewall of the first and second patterned layers, because as is well known, the insulating sidewall spacers would protect and prevent the first patterned conductive layer (gate electrode) and the second patterned conductive layer from contacting with the other adjacent elements. (underlining added.)

It is impermissible to use the claimed invention as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious. One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention (*In re Fine* 837 F.2D 1071,1075, 5 USPQ2D (BNA) 1596, 1600 (Fed. Cir. 1988).

Applicant respectfully submits that there is no motivation for combining the unrelated structures disclosed in Michihiro and Motonami. Applicants further respectfully submit that the Official Action has impermissibly used hindsight to pick and choose from among these isolated portions of the disclosures of the cited references, and in turn, using hindsight, has used those isolated portions of each reference to reconstruct the prior art to meet the recitations of the claimed invention.

Moreover, in order to include such a spacer on the sidewalls of the dummy pattern 15, the method of Michihiro would have to be substantially modified in ways that are not taught or suggested by the art of record. For example, formation of a gate spacer on the sidewall of

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the second dummy pattern 15 would require an additional insulating layer over the gate and dummy lines that layer is not taught or suggested by Michihiro. Moreover, there is absolutely nothing in Michihiro that suggests that damage to the insulating film 2 is a problem that needs to be remedied. In other words, Michihiro does not appear to recognize that misalignment of the contact hole 8 may cause over etching into the insulating films 2. As such, there would be no motivation in view of Michihiro to improve Michihiro by including spacers on the sidewalls of the dummy patterned 15 that cover the element separation insulating films 2.

Applicant further submits that there is no motivation in the references to make the substitution of elements suggested in the Official Action. In particular, Michihiro discusses arranging parallel dummy patterns "to make the channels of mixed field effect transistors the same length and suppress fluctuation thereof..." (Michihiro, Abstract.) In contrast, Motonami discusses providing a dummy interconnection in the vicinity of a step-like portion so that "the first and second conductive interconnection layers are precisely patterned within depth of focus." (Motonami, Abstract.) Applicant thus submits that there is no motivation in the references to somehow substitute elements of the dummy interconnection of Motonami that are used to provide patterning within depth of focus for elements of the parallel dummy patterns of Michihiro that are used to make channels of the same length.

Accordingly, Applicant respectfully submits that Claims 16, 18-22, 24-27, and 34-35 are patentable over the combination of Michihiro in view of Motonami.

New Dependent Claims 37-38 Are Also Patentable

New Claims 37 and 38 have been added to this Application in this Amendment. These new Claims also recite additional aspects of the present invention that are not disclosed or suggested by the cited references. For example, new Claim 37 recites:

A method according to Claim 16 wherein at least a portion of the contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer.

Support for this Claim can be found throughout the application and is illustrated in detail, for example, by FIG. 8, and also at page 8, line 16 through page 9, line 2. Applicants respectfully submit that the above-underlined recitations of Claim 37 are not disclosed or

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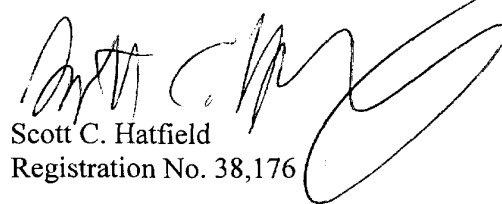
suggested by the cited references. Accordingly, Applicants respectfully request an indication of allowability of new Claim 37.

The new dependent Claim 38 is also separately patentable. For example, new dependent Claim 38 recites that " the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer". Support for this Claim can be found throughout the application and is illustrated in detail, for example, by FIGs. 7 and 8, and also at page 11, line 19. Applicants respectfully submit that the above-underlined recitations of Claim 38 are not disclosed or suggested by the cited references. Accordingly, Applicants respectfully request an indication of allowability of new Claim 38.

CONCLUSION

The Applicant sincerely appreciates the Examiner's thorough examination of this application. In response, the Applicant has shown that the cited art fails to teach or suggest the claimed methods. Accordingly, the Applicant submits that all the pending claims in the present application clearly define over the cited art and are in condition for allowance. A Notice of Allowance is thus respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any further issues need to be addressed.

Respectfully submitted,


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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, DC 20231, on March 5, 2001.


Traci A. Brown

Date of Signature: March 5, 2001

In re: Do-hyung Kim
Serial No.: 09/318,188
Filed: May 25, 1999
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

Please enter amended Claims 16, 19, 24-25, 27, and 34 as indicated below,
and please also enter the cancellation of Claim 18.

16. (Twice Amended) A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;

forming a field isolation layer on said field region;

forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;

forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, wherein the second patterned conductive layer does not extend over the active region of the substrate, and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer; and

forming a contact hole in said insulating layer exposing a portion of said active region [adjacent] between said etch inhibiting layer and said [field isolation layer] first patterned conductive layer.

Please cancel claim 18.

19. (Amended) A method according to Claim [18] 16 wherein [each of said etch inhibiting layer and] said first patterned conductive layer [comprise] comprises a conductive portion and insulating [spacer] spacers along sidewalls thereof.

24. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

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defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced
apart from said field region; [and]

forming a second patterned layer on said field isolation layer adjacent said
active region of said substrate, the active region including the first patterned layer wherein
said second patterned layer comprises a patterned conductive layer and an insulating spacer
along a sidewall of the patterned conductive layer, wherein the patterned conductive layer
does not extend over the active region of the substrate, and wherein the patterned conductive
layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer,
and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a
portion of said active region between said first and second patterned layers;

wherein said steps of forming said first patterned layer and forming said
second patterned layer are performed simultaneously.

25. (Twice Amended) A method for forming a microelectronic structure, said
method comprising the steps of:

defining adjacent active and field regions on a substrate, and circuits thereon;
forming a field isolation layer which covers said field region;
forming a first patterned layer on said active region of said substrate spaced
apart from said field region;

forming a second patterned layer on said field isolation layer adjacent said
active region of said substrate, the active region including the first patterned layer wherein
said second patterned layer comprises a patterned conductive layer and an insulating spacer
along a sidewall of the patterned conductive layer, wherein the patterned conductive layer
does not extend over the active region of the substrate, and wherein the patterned conductive
layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer,
and said first and second patterned layers; and

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forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers.

27. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region; [and]

- forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

- forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

- forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

- wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.

34. (Twice Amended) A method for forming a microelectronic structure, said method comprising the steps of:

- defining adjacent active and field regions on a substrate, and circuits thereon;
- forming a field isolation layer which covers said field region;
- forming a first patterned layer on said active region of said substrate spaced apart from said field region; [and]

- forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer

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does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

forming an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers; and

forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a sidewall thereof.

Please enter new Claims 37 and 38 as indicated below.

37. (New) A method according to Claim 16 wherein contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer.

38. (New) A method according to Claim 16 wherein at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/318.188 05/25/99 KIM

D 5649-129DV

020792 MM92/0502
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH NC 27627

EXAMINER

CAQ.P

ART UNIT

PAPER NUMBER


2814

DATE MAILED:

05/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of Allowability	Application No. 09/318,188	Applicant(s) Kim	
	Examiner Phat X. Cao	Art Unit 2814	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment E, filed 3/7/01.

2. ☒ The allowed claim(s) is/are 16-17,19-22,35-38, 24-26,33,27-29,34 (renumbered 1-2,3-6,7-10,11-13,14,15-17,18,
respectively)

3. ☐ The drawings filed on _____ are acceptable as formal drawings.

4. ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/748,148.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
*Certified copies not received: _____

5. ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION.** This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

6. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

7. ☒ Applicant MUST submit NEW FORMAL DRAWINGS
(a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☒ to Paper No. 6.
(b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the examiner.
(c) ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

8. ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

1 <input type="checkbox"/> Notice of References Cited (PTO-892)	2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____
5 <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449), Paper No(s). _____	6 <input type="checkbox"/> Examiner's Amendment/Comment
7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material	8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance
9 <input type="checkbox"/> Other	

Art Unit: 2814

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

the prior art of record fails to disclose all the process limitations recited in the base claims, including a combination of a step of forming a dummy pattern as an etch inhibiting layer on a field isolation layer and a step of forming along the sidewalls of a dummy pattern the spacers that will prevent damage to the field oxide layer in the event the contact hole is misaligned (also see Applicant's arguments on page 9, third paragraph).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.


Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

Application/Control Number: 09/318,188

Page 3

Art Unit: 2814

PHAT X. CAO
PC
April 30, 2001


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

020792 MM92/0502
MYERS BIGEL SIBLEY & SAJOWEC
PO BOX 37428
RALEIGH NC 27627

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/318,188	05/25/99	018	CAO, P 2814	05/02/01
First Named Applicant	KIM,	35 USC 154(b) term ext. = 0 Days.		

TITLE OF INVENTION METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 5649-129DV	438-183.000	F70	UTILITY	NO	\$1240.00	08/02/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.
- II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.



Attorney's Docket No. 5649-129CXDV

AF/2B4
#16 Dm SN
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Do-Hyun Kim
Serial No.: 09/318,188
Filed: May 25, 1999
For: METHODS OF FORMING ETCH INHIBITING STRUCTURES ON
FIELD ISOLATION REGIONS

Group Art Unit: 2814

Examiner: P. Cao

May 18, 2001

Box AF
Commissioner for Patents
Washington, DC 20231


COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

In response to the Reasons For Allowance provided with the Notice of Allowability of May 2, 2001, the Applicant appreciates the allowance of all claims. In response, the Applicant points out that the scope and patentability of each independent claim is defined with respect to the recitations thereof. The patentability and scope of Independent Claims 16, 24, 25, 27, and 34 are, thus, determined with respect to the recitations thereof.

Entry of these comments is respectfully requested. The Examiner is encouraged to contact the undersigned attorney if any further issues should need to be addressed.

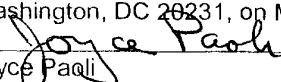
Respectfully submitted,


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Date of Signature: May 18, 2001

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Attorney's Docket No. 5649-129CXDV

PATENT

B

17a

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Do-Hyun Kim

Serial No.: 09/318,188

Allowed: May 2, 2001

Filed: May 25, 1999

Issue Batch No.: F70 ✓

For: METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS

May 18, 2001

Commissioner for Patents
Washington, DC 20231
Attn: Drawing Review Branch

SUBMITTAL OF FORMAL DRAWINGS

Sir:

In response to the requirement for new drawings as set forth in Paper No. 6 in the above application, there is enclosed herewith one set (2 sheets) of new formal drawings. It is requested that these new drawings be substituted for the originally filed informal drawings.

Respectfully submitted,

Scott C. Hatfield
Registration No. 38,176

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Joyce Paoli
Date of Signature: May 18, 2001

FIG. 1
(PRIOR ART)

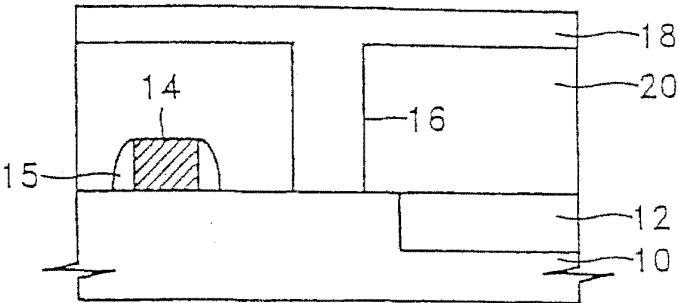


FIG. 2
(PRIOR ART)

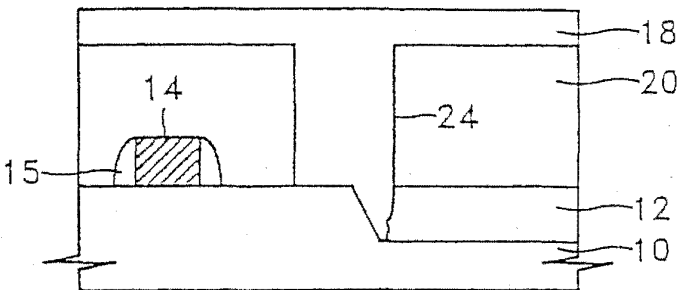


FIG. 3
(PRIOR ART)

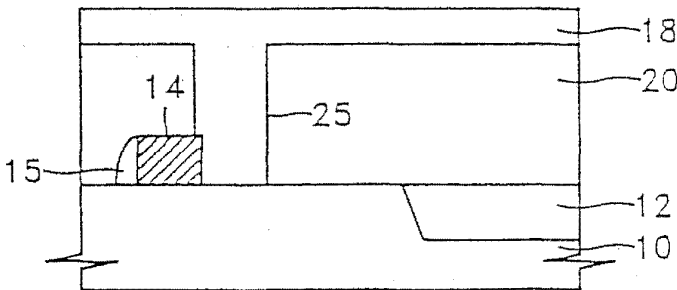


FIG. 4

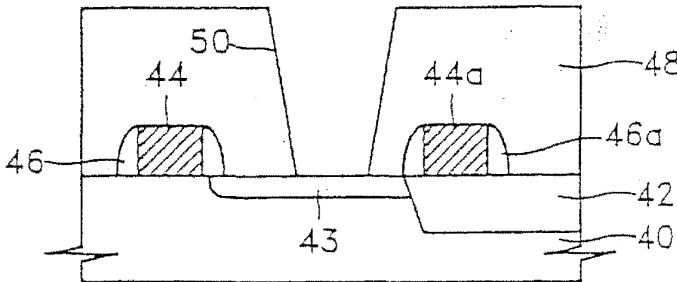


FIG. 5

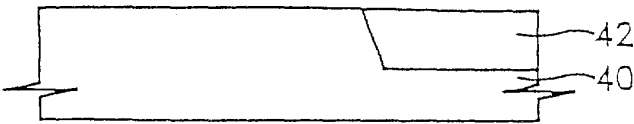


FIG. 6

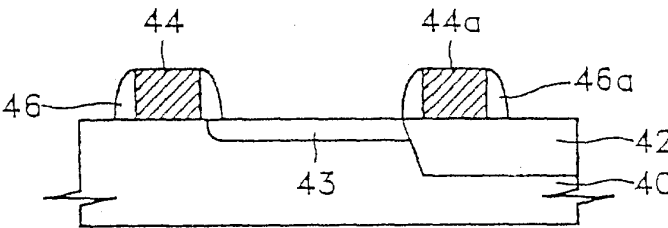


FIG. 7

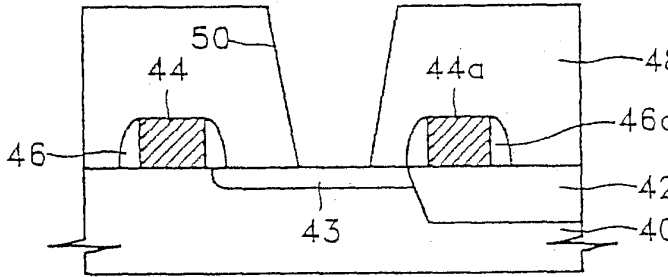
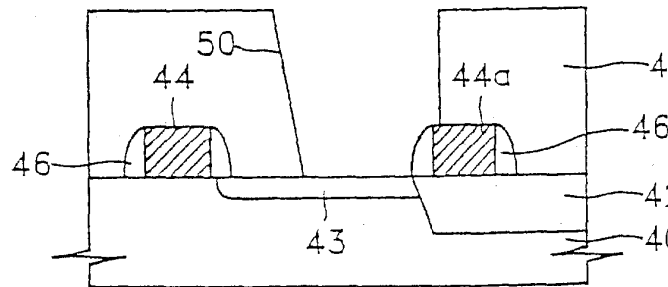


FIG. 8



PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

05-04-01 A10:11 01

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CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

020792
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH NC 27627

MM92/0502



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Joyce Paoli

(Depositor's name)

Joyce Paoli
7-27-01

(Signature)

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/318,188	05/25/99	018	CAO, P	2814 05/02/01
First Named Applicant	KIM,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION: METHODS OF FORMING ETCH INHIBITING STRUCTURES ON FIELD ISOLATION REGIONS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 5649-129DV	438-183.000	F70	UTILITY	NO	\$1240.00	08/02/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Myers Bigel Sibley
& Sajovec

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE **Samsung Electronics Co., Ltd.**

(B) RESIDENCE: (CITY & STATE OR COUNTRY)

Republic of Korea

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee **10**
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The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature)
Scott C. Hatfield, Reg. No. 38,176
NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

(Date) **07/27/01**

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08/01/2001 NGEINR2 00000058 09318188**01 FC:142**
02 FC:561**1240.00 DP**
30.00 DP

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PTOL-85B (REV.10-96) Approved for use through 08/30/99. OMB 0651-0033

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/08/1999 TDADE1 00000022 09318188

01 FC:101 760.00 0P

PTO-1556
(5/87)

*U.S. GPO: 1998-433-214/80404

PATENT APPLICATION FEE DETERMINATION RECORD
Effective November 10, 1998

Application or Docket Number

09/318188

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	16 minus 20= *	
INDEPENDENT CLAIMS	2 minus 3= *	
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 16	Minus	** 20	=
	Independent	* 2	Minus	*** 3	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 21	Minus	** 20	= 1
	Independent	* 2	Minus	*** 2	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	* 20	Minus	** 21	=
	Independent	* 5	Minus	*** 3	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

**SMALL ENTITY
TYPE** ☒

OR

**OTHER THAN
SMALL ENTITY**

RATE	FEE
	380.00
X\$ 9=	
X39=	
+130=	
TOTAL	

OR

RATE	FEE
	760.00
X\$18=	
X78=	
+260=	
TOTAL	760

SMALL ENTITY

OR

**OTHER THAN
SMALL ENTITY**

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	18.00
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	
X78=	16.00
+260=	
TOTAL ADDIT. FEE	

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number:

CLAIMS AS AMENDED - PART II

AMENDMENT	(Column 1)		(Column 2)		(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
Total	*	Minus	**		=	x 9 =		OR	x 18 =	
Independent	*	Minus	***		=	x 40 =		OR	x 80 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						+135 =		OR	+270 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1)		(Column 2)		(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
Total	* 16	Minus	** 21		=	x 9 =		OR	x 18 =	
Independent	* 5	Minus	*** 5		=	x 40 =		OR	x 80 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						+135 =		OR	+270 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1)		(Column 2)		(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
Total	*	Minus	**		=	x \$ 9 =		OR	x 18 =	
Independent	*	Minus	***		=	x 40 =		OR	x 80 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						+135 =		OR	+270 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1)		(Column 2)		(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
Total	*	Minus	**		=	x \$ 9 =		OR	x \$ 18 =	
Independent	*	Minus	***		=	x 40 =		OR	x 80 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						+135 =		OR	+270 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/97)

U.S. Government Printing Office: 1997 - 430-571/89194

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

3

CLAIMS ONLY							SERIAL NO.		FILING DATE		
							APPLICANT(S)				
CLAIMS											
	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT			*	*	*	
	IND.	DEP.	IND.	DEP.	IND.	DEP.		IND.	DEP.	IND.	DEP.
1							51				
2							52				
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45							95				
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48							98				
49							99				
50							100				
TOTAL IND.	32						TOTAL IND.				
TOTAL DEP.	14						TOTAL DEP.				
TOTAL CLAIMS	112						TOTAL CLAIMS				
* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS											
U.S.DEPARTMENT OF COMMERCE Patent and Trademark Office											

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	T.D.		6/7/99
O.I.P.E. CLASSIFIER	M		6/10/99
FORMALITY REVIEW		71476	6/17/99

INDEX OF CLAIMS

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Appeal
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Objected

Claim		Date					
Final	Original	1	2	3	4	5	6
1	16	✓	✓	✓	✓	✓	✓
2	17	✓	✓	✓	✓	✓	✓
3	18	✓	✓	✓	✓	✓	✓
4	19	✓	✓	✓	✓	✓	✓
5	20	✓	✓	✓	✓	✓	✓
6	21	✓	✓	✓	✓	✓	✓
7	22	✓	✓	✓	✓	✓	✓
8	23	✓	✓	✓	✓	✓	✓
9	24	✓	✓	✓	✓	✓	✓
10	25	✓	✓	✓	✓	✓	✓
11	26	✓	✓	✓	✓	✓	✓
12	27	✓	✓	✓	✓	✓	✓
13	28	✓	✓	✓	✓	✓	✓
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15	30	✓	✓	✓	✓	✓	✓
16	31	✓	✓	✓	✓	✓	✓
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19	34	✓	✓	✓	✓	✓	✓
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22	37	✓	✓	✓	✓	✓	✓
23	38	✓	✓	✓	✓	✓	✓
24	39	✓	✓	✓	✓	✓	✓
25	40	✓	✓	✓	✓	✓	✓
26	41	✓	✓	✓	✓	✓	✓
27	42	✓	✓	✓	✓	✓	✓
28	43	✓	✓	✓	✓	✓	✓
29	44	✓	✓	✓	✓	✓	✓
30	45	✓	✓	✓	✓	✓	✓
31	46	✓	✓	✓	✓	✓	✓
32	47	✓	✓	✓	✓	✓	✓
33	48	✓	✓	✓	✓	✓	✓
34	49	✓	✓	✓	✓	✓	✓
35	50	✓	✓	✓	✓	✓	✓

Claim		Date					
Final	Original	1	2	3	4	5	6
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