

Jack C. Lee is a Professor of the Electrical and Computer Engineering Department and holds the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor device (i.e. MOSFETs) fabrication processes, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, and alternative channel materials. Dr. Lee has over 30 years of experience in semiconductor technology and dielectric processing. He has published over 500 journal publications and conference proceedings and several patents; and co-authored one book and two book chapters on high-K gate dielectrics. He has also been recognized with many teaching and research awards including the prestigious SRC Inventor Recognition Award from Semiconductor Research Corporation for his work on dielectric technology and characterization. Dr. Lee is a Fellow of IEEE and a Distinguished Lecturer for the IEEE Electron Devices Society.

Professional Experience

Professor, Department of Electrical and Computer Engineering
Cullen Trust For Higher Education Endowed Professorship in Engineering #4
The University of Texas at Austin, September 1996 - present
Associate Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin, September 1992 - August 1996
Assistant Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin, September 1988 - August 1992
Lecturer, EECS Department
University of California at Berkeley, Spring 1988
Member of Technical Staff, Microelectronics Center
TRW, Redondo Beach, CA, June 1979 – August 1984

Education

Ph.D. in Electrical Engineering, University of California at Berkeley,
August 1988
M.S. in Electrical Engineering, University of California at Los Angeles, December 1981
B.S. in Electrical Engineering (with highest honors) UCLA,
June 1980

Selected Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - present.
Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 “For contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices”
Gordon Lepley IV Memorial Teaching Award, ECE Department, The University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-
 Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
 Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching,
 College of Engineering, The University of Texas at Austin, 1996
 Award of Excellence, Halliburton Foundation, 1993
 Departmental Teaching Award, College of Engineering, The University of Texas at Austin,
 1993
 SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
 Hughes Aircraft Company Endowed Faculty Fellowship in Engineering,
 The University of Texas at Austin, 1991- 2000
 Outstanding Engineering Teaching by an Assistant Professor, College of Engineering,
 The University of Texas at Austin, 1991
 Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
 Dow Outstanding Young Faculty Award, American Society for Engineering Education, 1990
 Engineering Research Initiation Award, Engineering Foundation of the United Engineering
 Trustees, 1989
 Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts:

My litigation experience includes writing expert reports on validity/ invalidity, infringement/non-infringement, claim construction, reverse engineering, advising clients during discovery, deposition and cross-examination of opposing experts, and testimony at hearings and at trial.

- Expert Reports – I have written about 20 expert reports
 - Depositions – I have been deposed about 7 times
 - Trials – 2 cases have gone to trials (Elpida Memory v. Nanya Technology Corporation, and Agere Systems v. Rohm)
 - Tutorial – I have given 1 tutorial to the judge in the Macronix v. Spansion case

- Macronix, Inc. v. Spansion, Inc.
 September 2014 –
 → Flash memory devices and fabrication methods, an ITC case
 [Ropes and Gray LLP]
 (Representing defendant, Spansion, Inc.)
- Keranos, LLC v. MicrochipTechnology, Inc.
 August 2012 – February 2014
 → Flash memory devices and fabrication methods
 [King and Spalding, LLP]
 (Representing defendant, MicrochipTechnology)
- University of Illinois v. Micron Technology, Inc.
 April 2012 – March 2013 → Semiconductor processes
 [Stadheim and Gear, Ltd.]
 (Representing plaintiff, University of Illinois)

- Xicor LLC v. Silicon Storage Technology, Inc.
January 2011 – December 2011
→ Semiconductor processes
[Covington and Burling LLP]
(Representing defendant, Silicon Storage Technology)
- Elpida Memory, Inc. v. Nanya Technology Corporation
April 2012 – December 2012
→ DRAM memory processes, an ITC case
[Freitas Tseng & Kaufman LLP]
(Representing defendant, Nanya Technology Corporation)
- Spansion LLC v. Samsung
May 2010 – June 2011
→ Semiconductor devices
[McDermott Will & Emery LLP]
(Representing plaintiff, Spansion LLC)
- Spansion LLC v. Samsung
July 2009 – March 2010
→ Semiconductor devices, an ITC case
[King and Spalding, LLP]
(Representing plaintiff, Spansion LLC)
- Advanced Micro Devices v. Samsung
March 2008 – September 2010
→ Semiconductor devices;
[Robins, Kaplan, Miller & Ciresi, LLP]
(Representing plaintiff, Advanced Micro Devices)
- Agere Systems Inc. v. Samsung
January 2007 – July 2010
→ Semiconductor devices
[Townsend and Townsend and Crew, LLP]
(Representing plaintiff, Agere Systems Inc.)
- Agere Systems Inc. v. Rohm Co. Ltd.
April 2006 – November 2007
→ Semiconductor devices and fabrication methods
[Townsend and Townsend and Crew, LLP]
(Representing plaintiff, Agere Systems Inc.)

Jack Lee is the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at The University of Texas at Austin. He received the B.S. and M.S. degrees in electrical engineering from University of California at Los Angeles in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California at Berkeley in 1988. From 1981 to 1984, he was a member of technical staff at the TRW Microelectronics Center, California, in the High-Speed Bipolar Device Program. He worked on bipolar circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor devices, fabrication processes, characterization and modeling, dielectric processes, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, and alternative channel materials.

He has published over 500 journal publications and conference proceedings; 1 book and 2 book chapters. He has been awarded two best paper awards, numerous teaching / research awards and several patents. He has supervised and graduated 40 Ph.D. students. Six of his PhD graduates are now professors in other universities and the rest are working in research and development programs in semiconductor industry. Dr. Lee is a fellow of the Institute of Electrical and Electronic Engineers (IEEE) and Distinguished Lecturer for IEEE Electron Devices Society.

At The University of Texas at Austin, Dr. Lee continues to teach undergraduate circuit analysis and design courses, as well as the graduate level course which he developed entitled "Nanoscale Device Physics and Technologies". This course focuses on the topics of current research on ultra-small high-speed semiconductor devices used in integrated circuits, and is designed for graduate students wishing to pursue research in the microelectronics area.

Professional Experience

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The University of Texas at Austin, September 1992 - August 1996
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The University of Texas at Austin, September 1988 - August 1992
Lecturer, EECS Department
University of California at Berkeley, Spring 1988
Member of Technical Staff, Microelectronics Center
TRW, Redondo Beach, CA, May - August 1984 and June 1979 - September 1983

Education

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Dean’s Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003

Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching,
College of Engineering, The University of Texas at Austin, 1996

Award of Excellence, Halliburton Foundation, 1993

Departmental Teaching Award, College of Engineering, The University of Texas at Austin,
1993

SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991

Hughes Aircraft Company Endowed Faculty Fellowship in Engineering,
The University of Texas at Austin, 1991- 2000

Outstanding Engineering Teaching by an Assistant Professor, College of Engineering,
The University of Texas at Austin, 1991

Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.

Dow Outstanding Young Faculty Award, American Society for Engineering Education, 1990

Engineering Research Initiation Award, Engineering Foundation of the United Engineering
Trustees, 1989

Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Publications

Jack C. Lee, The University of Texas at Austin

Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.
2. J. Lee, I-C Chen and C. Hu, "Comparison Between CVD and Thermal Oxide Dielectric Integrity," IEEE Electron Device Letters, vol. EDL-7, no. 9, p. 506 - 509, September 1986.
3. K. Mayaram, J. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," IEEE Transactions on Electron Devices, vol. ED-34, no.7, p. 1509 - 1518, July 1987.
4. J. Lee and C. Hu, "Polarity Asymmetry of Oxides Grown on Polycrystalline Silicon," IEEE Transactions on Electron Devices, vol. ED-35, no. 7, p. 1063 - 1070, July 1988.
5. J. Lee, C. Hegarty and C. Hu, "Electrical Characteristics of MOSFET's Using Low-Pressure Chemical Vapor Deposited Oxide," IEEE Electron Device Letters, vol. EDL-9, no. 7, p. 324 - 327, July 1988.
6. J. Lee, I-C Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," Special Issue of IEEE Transactions on Electron Devices on Reliability, Vol. ED-35, no. 12, p. 2268 - 2278, December 1988.
7. H. Hwang, W. Ting, D. L. Kwong, J. Lee, L. Buhrow and R. Bowling, "Electrical Characteristics of Reoxidized-nitrided CVD Oxide," Applied Physics Letters, 55(8), p. 755 - 756, 21 August, 1989.
8. R. Moazzami, J. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," Special issue of IEEE Transactions on Electron Devices on Vacuum Microelectronic Devices, vol. ED-36, no. 11, p. 2462 - 2465, November 1989.
9. H. Hwang, W. Ting, D.L. Kwong, J. Lee, L. Buhrow and R.A. Bowling, "Effects of Dynamic Stressing on Nitrided and Reoxidized-Nitrided Chemical Vapor Deposited Gate Oxides," IEEE Electron Device Letters, vol. EDL-10, no. 12, p. 568 - 570, December 1989.
10. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Soft Breakdown in Titanium-Silicided Shallow Source/Drain Junction," IEEE Electron Device Letters, vol. EDL-11, no. 5, p. 191 - 193, May 1990.
11. K. Park, S. Batra, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, and G. Lux, "Anomalous Capacitance-Voltage Behavior Due to Dopant Segregation and Carrier Trapping in Arsenic-Implanted Polysilicon and Polycide Gates," Applied Physics Letters, vol. 56, no. 23, p.2325 - 2327, June 4, 1990.
12. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Anomalous Current-Voltage Behavior in Titanium-Silicided Source/Drain Junctions," Journal of Applied Physics, vol. 68, no. 3, p. 1082 - 1087, August 1, 1990.

13. H. Hwang, W. Ting, B. Maiti, D.L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Gate Dielectrics Prepared by Rapid Thermal Oxidation of Si in N₂O," Applied Physics Letters, vol. 57, no. 10, p. 1010 - 1011, Sept. 3, 1990.
14. S. Batra, K. Park, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain and G. Lux "Effects of Dopant Redistribution, Segregation and Carrier Trapping in As-Implanted MOS Gates," IEEE Transactions on Electron Devices, vol. 37, no. 11, p. 2322 - 2330, October, 1990.
15. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "The Impact of Trench Isolation on Latch-up Immunity in Bulk, Non-epitaxial CMOS," IEEE Electron Device Letters, vol. EDL-12, no. 2, p. 77 - 79, February, 1991.
16. W. Ting, H. Hwang, J. Lee and D. L. Kwong, "Composition and Growth Kinetics of Ultrathin SiO₂ Films Formed by Oxidizing Si Substrate in N₂O," Applied Physics Letters, vol. 57, p. 2808 - 2810, 1990.
17. W. Ting, P.C. Li, G. Q. Lo, J. Lee and D.L. Kwong, "Metal-Oxide Semiconductor Characteristics of Rapid Thermal Processed Chemical Vapor Deposited SiO₂ Gate Dielectrics," Solid State Electronics, vol. 34, no. 4, p 385 - 388, 1991.
18. W. Ting, H. Hwang, J. Lee and D.L. Kwong, "Growth Kinetics of Ultrathin SiO₂ Films Prepared by Rapid Thermal Oxidation of Si Substrates in N₂O," Journal of Applied Physics, vol. 70, no. 2, p. 1072 - 1074, July 15, 1991.
19. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Enhancement of Boron Diffusion Through Gate Oxides in MOS Devices During Rapid Thermal Silicidation," Applied Physics Letters, vol. 58, no. 19, p. 2123 - 2125, May 1991.
20. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "A Physical Model for Boron Penetration Through Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N₂O," Applied Physics Letters, vol. 59, no. 13, p. 1581 - 1582, September 23, 1991.
21. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Improved Reliability Characteristics of Submicron nMOSFET's with Oxynitride Gate Dielectrics Prepared by Rapid Thermal Oxidation in N₂O," IEEE Electron Device Letters, vol. 12, no.9, p.495-497, September 1991.
22. J. Carrano, C. Sudhama, V. Chikarmane, J. Lee, A. Tasch, W. Shepherd and N. Abt, "Electrical and Reliability Properties of PZT Thin Films for ULSI DRAM Applications," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 38, no. 6, p. 690 - 703, November 1991.
23. V. Chikarmane, C. Sudhama, J. Kim, J. Lee, A. Tasch and S. Novak, "Comparative Study of The Perovskite Phase Microstructure Evolution and Electrial Properties of PZT Thin Film Capacitors Annealed in Oxygen and Nitrogen Ambients," Applied Physics Letters, vol. 59, no. 22, p. 2850 - 2852, Nov. 25, 1991.
24. M. Hao and J. Lee, "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon," Applied Physics Letters, vol. 60, no. 4, p. 445 - 447, January 27, 1992 .

25. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Parametric Study of Latchup-Immunity of Deep Trench-Isolated, Bulk, Non-epitaxial CMOS," IEEE Trans. Elec. Dev., vol. 39, no. 4, p. 921 - 931, April 1992.
26. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "Annealing of Lead Zirconate Titanate (65/35) Thin Films for Storage Dielectric Applications: Phase Transformations and Electrical Characteristics," Journal of Electronic Materials, vol. 21, no. 5, p. 503 - 512, May 1992.
27. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-Deposition Annealing Ambient on the Electrical Characteristics and Phase Transformation Kinetics of Sputtered Lead Zirconate titanate (65/35) Thin Film Capacitors," Journal of Vacuum Science and Technology, vol. 10, no. 4, p. 1562 - 1568, July 1992.
28. V.K. Mathews, R. L. Maddox, P.C. Fazan, J. Rosato, H. Hwang and J. Lee, "Degradation of Junction Leakage in Devices Subjected to Gate Oxidation in Nitrous Oxide," IEEE Electron Device Letters, vol. 13, no. 12, p. 648 - 650, Dec. 1992.
29. B. Maiti, M. Hao, I. Lee and J. Lee, "Improved Ultrathin Oxynitride Formed by Thermal Nitridation and Low Pressure Chemical Vapor Deposition Process," Applied Physics Letters, vol. 61, p. 1790 - 1792, 1992.
30. B. Maiti and J. Lee, "Low-Pressure Chemical Vapor Deposited Silicon-Rich Oxides for Non-volatile Memory Applications," IEEE Electron Device Letters, vol. 13, no. 12, p. 624 - 626, Dec. 1992.
31. H. Hwang, M. Y. Hao, J. Lee, V. Mathews, P. Fazan and C. Dennison, "Furnace N₂O Oxidation Process for Submicron MOSFET Device Applications," Solid-State Electronics, vol. 36, p. 749 - 751, 1993.
32. H. Hwang, J. Lee, P. Fazan and C. Dennison, "Hot-Carrier Reliability Characteristics of Narrow Width MOSFETs," Solid-State Electronics, Vol. 36, No. 4, p. 665 - 666, 1993.
33. B. Maiti and J. Lee, "A New Low-Thermal Budget Process for Ultrathin Oxynitride Dielectrics," Journal of Electronic Materials, 1992.
34. J. Lin, W. Chen, S. Banerjee and J. Lee, "Cobalt Disilicide as a Dopant Diffusion Source for Polysilicon Gates in MOS Devices," Journal of Electronic Materials, vol. 22, p. 667 - 673, 1993.
35. W. Chen, J. Lin, S. Banerjee and J. Lee, "Thermal Stability and Dopant Drive-Out Characteristics of CoSi₂ Polycide Gates," Journal of Applied Physics, vol. 73, p. 4712 - 4714, May 1993.
36. J. Lee, V. Chikarmane, C. Sudhama, and J. Kim, "Sputtered PZT Thin Films for Memory Applications," Journal of Integrated Ferroelectrics, vol. 3, 1993.
37. C. Sudhama, J. Kim, J. Lee, W. Shepherd and E. Meyer, "The Effects of Lanthanum Doping on the Electrical Properties of Sol-Gel Derived Ferroelectric Lead Zirconate Titanate (PZT) for ULSI DRAM Applications," Journal of Vacuum Science and Technology, p. 1302 - 1309, July / Aug 1993.

38. M. Y. Hao, H. Hwang and J. Lee, "Silicon-Implanted SiO₂ for Non-volatile Memory Applications," Solid-State Electronics, vol. 36, p. 1321 - 1324, 1993.
39. M. Y. Hao, H. Hwang and J. Lee, "Memory Effects of Silicon-Implanted Oxides for EEPROM Applications," Applied Physics Letters, vol. 62, No. 13, p. 1530 - 1532, March 1993.
40. S. Batra, K. Picone, K. Park, S. Bhattacharya, S. Banerjee, J. Lee, M. Manning and C. Dennison, "Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and Its Effects on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes," Solid-State Electronics vol. 36, no. 7, p. 955 - 960, 1993.
41. J. Lee, C. Sudhama, J. Kim and R. Khamankar, (Invited Paper) "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications", Extended Abstracts of International Conference on Solid State Devices and Materials, p. 850 - 852, 1993.
42. W. M. Chen, S. K. Banerjee, and J. C. Lee, "Degradation mechanism and improvement of thermal stability of CoSi₂/polycrystalline Si layers," Applied Physics Letters, vol. 64, no. 12, p. 1505 - 1507, 1994.
43. W. M. Chen, J. Lin, S. K. Banerjee, and J. C. Lee, " Simultaneous Shallow-Junction Formation and Gate Doping p-channel Metal-Semiconductor-Oxide Field-Effect Transistor Process Using Cobalt Silicide as a Diffusion/Doping Source," Applied Physics Letters, vol. 64, no. 3, p. 345 - 347, 1994.
44. M. Y. Hao, B. Maiti, and J. Lee, " Novel Process for Reliable Ultrathin Tunnel Dielectrics," Appl. Phys. Lett., vol. 64, p. 2102 - 2104, April 1994.
45. B. Jiang, C. Sudhama, R. Khamankar, J. Kim and J. Lee, "Effects of Nonlinear Storage Capacitor on DRAM READ/WRITE," IEEE Electron Device Letters, vol. 15, no. 4, p.126 - 128, April 1994.
46. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, p. 151 - 152, 1994.
47. M. Y. Hao, K. Lai, W. M. Chen, and J. Lee, " Surface Cleaning Effect on Dielectric Integrity for Ultrathin Oxynitrides Grown in N₂O," Applied Physics Letters, vol. 65, no. 9, p. 1133 - 1135, August 1994.
48. K. Lai, M. Y. Hao, C. Y. Hu, W. M. Chen, and J. Lee, " Effects of Surface Preparation on the Electrical and Reliability Properties of Ultrathin Thermal Oxide," IEEE Electron Device Letters, vol. ED-15, no. 11, p. 446 - 448, November, 1994.
49. M. Y. Hao, W. M. Chen, K. Lai, M. Gardner, J. Fulford, and J. Lee, "Correlation of Dielectric Breakdown with Hole Transport for Ultrathin Thermal Oxides and N₂O Oxynitrides," Applied Physics Letters, vol. 66, no. 9, p. 1126 - 1128, February 27, 1995.
50. R. Khamankar, J. Kim, C. Sudhama, B. Jiang, and J. Lee, "Effects of Electrical Stress Parameters on Polarization Loss in Ferroelectric PZT Thin Film Capacitors," Electron Device Letter, p. 130 - 132, April 1995.

51. J. Lee, B. Jiang, R. Khamankar, and J. Kim, "Nonlinearity of Ferroelectric Capacitors on DRAM R/W Operations," *Integrated Ferroelectrics*, p. 319 - 328, 1995.
52. W. M. Chen, M. Y. Hao, K. Lai, M. Gardner, J. Fulford, and J. Lee, " 'Turn-around' Effects of Stress-Induced Leakage Current of Ultrathin N₂O-Annealed Oxides," *Applied Physics Letters*, vol. 67, No. 5, p. 1 - 3, July 1995.
53. Kafai Lai, Wei-Ming Chen, Ming-Yin Hao, Mark Gardner, Jim Fulford, Jack C. Lee, "'Turn-around' effects of stress-induced leakage current of ultrathin N₂O-annealed oxides", *Applied Physics Letters*, vol. 67, no. 5, p. 673-5, Jul. 31, 1995.
54. Kafai Lai, Kiran Kumar, Anthony I. Chou, and Jack C. Lee, "Plasma damage and photo-annealing effects of thin gate oxides and oxynitrides during O₂ plasma exposure", *IEEE Elec. Dev. Lett.*, vol. 17, no. 3, p. 82, Mar. 1996.
55. Anthony I. Chou, Kafai Lai, Kiran Kumar, Mark Gardner, Jim Fulford, and Jack C. Lee, "Optimization of gate dopant concentration and microstructure for improved electrical and reliability characteristics of ultrathin oxides and N₂O-oxynitrides", *Applied Physics Letters*, vol. 69, no. 7, p. 934, Aug. 12, 1996.
56. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Effect of BF₂ implantation on ultra-thin gate oxide reliability" *Appl. Phys. Lett.*, vol. 69, no. 11, p1591, Sep. 1996.
57. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Reliability of gate oxide grown on nitrogen-implanted Si substrate" *Appl. Phys. Lett.* Vol. 69, No. 24, 9 Dec. 1996.
58. K. Kumar, A. Chou, C. Lin, P. Choudhury, and J. C. Lee, "Optimization of sub 3 nm gate dielectrics grown by rapid thermal oxidation in a nitric oxide ambient", *Appl. Phys. Lett.* 70 (3), 20 January 1997.
59. Prasenjit Chowdhury, Anthony I. Chou, Kiran Kumar, Chuan Lin and Jack C. Lee, "Improvement of Ultra-thin Gate Oxide and Oxynitride Integrity Using Fluorine Implantation Techniques," *Applied Physics Letters* 70 (1), January 6, 1997.
60. A. Chou, K. Lai, K. Kumar, P. Chowdhury and J. Lee, "Modeling of Stress-Induced Leakage Current in Ultra-Thin Oxide with the Trap Assisted Tunneling Mechanism," *Applied Physics Letters*, vol. 70, no. 25, Pg. 3407, June 23, 1997.
61. Byoung Hun Lee, Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi and Jack C. Lee, "Effect of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon", *Appl. Phys. Lett.* Vol. 74, p. 3143, 1999.
62. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee and Jack C. Lee, "Effects of Ir Electrodes on BST Thin Film Capacitors for High-Density Memory Application" *IEEE Transactions on Electron Devices* vol. 46, no. 12, p. 2304, Dec. 1999.
63. Jian-Hung Lee, Razak Mohammedali, Venkatasubramani Balu, Jeong Hee Han, Sundar Gopalan, Chun-Hui Wong and Jack C. Lee "The Niobium Doping Effects on Resistance Degradation of Strontium Titanate Thin Film Capacitors", *Applied Physics Letters*, vol. 75, no. 10, p. 1455, September 6, 1999.

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65. T. Ngai, W. Qi, R. Sharma, J. Fretwell, X. Chen, J. Lee and S. Banerjee, "Electrical Properties of ZrO_2 Gate Dielectric on SiGe," *Applied Physics Letters*, vol. 76, no. 4, p. 502, January 24, 2000.
66. Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee, "Electrical Characteristics of Highly Reliable Ultra-Thin Hafnium Oxide Gate Dielectric," *IEEE Electron Dev. Lett.*, vol. 21, 4, p.181, 2000.
67. Byoung Hun Lee, Laegu Kang, Renee Nieh, Wen-Jie Qi, and Jack C. Lee, "Thermal stability and electrical characteristics of Hafnium oxide gate dielectric reoxidized with rapid thermal annealing", *Appl. Phys. Lett.*, 76, p.1926, 2000.
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69. Wen-Jie Qi, Renee Nieh, Easwar Dharmarajan, Byoung Hun Lee, Yongjoo Jeon, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultrathin zirconium silicate film with good thermal stability for alternative gate dielectric applications", *Appl. Phys. Lett.*, vol. 77, no.11, p. 1704-1706, Sept. 2000.
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