IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Review of:	)
U.S. Patent No. 6,287,902	)
Issued: Sept. 11, 2001	)
Application No.: 09/318,188	)
Filing Date: May 25, 1999	)

For: **Methods of Forming Etch Inhibiting Structures on Field Isolation Regions**

FILED VIA PRPS

DECLARATION OF DR. JACK LEE IN SUPPORT OF PETITION NO. 2 FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,287,902

For ease of reference, Dr. Lee refers to this declaration as being in support of "the '902 Petition No. 2" challenging all claims of the '902 patent.

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I, Jack Lee, Professor in the Department of Electrical and Computer Engineering at The University of Texas at Austin, hereby declare as follows:

I. INTRODUCTION AND QUALIFICATIONS

1. I have been retained by NVIDIA Corporation ("NVIDIA") to provide my opinion concerning the validity of U.S. Patent No. 6,287,902 (Ex. 1101, "the '902 patent") in support of Petition For *Inter Partes* Review of U.S. Patent No. 6,287,902 ("the '902 Petition").

2. I am an expert in the field of semiconductor process technology and semiconductor design. I have over 30 years of first-hand experience as a researcher, educator, and consultant in this field.

3. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

4. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

5. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and

Electronics Engineers ("IEEE") International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

6. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised 40 students who received a doctoral degree under my guidance. I am currently the Cullen Trust for Higher Education Endowed Professor in Engineering #4 in the Department of Electrical and Computer Engineering at UT Austin.

7. My current research interests include: high-K gate dielectrics and metal gate electrodes in semiconductor devices (CMOS/MOSFETs); semiconductor device fabrication processes, characterization and modeling; dielectric processes, characterization and reliability; and alternative transistor channel materials. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others. Throughout my career, I have been developing improved processing technologies for insulating layers, including isolation regions and preventing defects such as etching-induced defects.

8. I have authored over 500 journal publications and conference proceeding papers, and have coauthored one book and two book chapters on semiconductor devices. I am a named inventor of several U.S. patents, including:

- U.S. Patent No. 6,013,546 ("Semiconductor Device Having a PMOS Device with a Source/Drain Region Formed Using a Heavy Atom p-Type Implant and Method of Manufacture Thereof")
- U.S. Patent No. 6,057,584 ("Semiconductor Device Having a Tri-Layer Gate Insulating Dielectric")
- U.S. Patent No. 6,146,934 ("Semiconductor Device with Asymmetric PMOS Source/Drain Implant and Method of Manufacture Thereof")
- U.S. Patent No. 6,306,742 ("Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit")
- U.S. Patent No. 5,891,798 ("Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit")

9. I have also earned many research awards including the prestigious SRC Inventor Recognition Award from Semiconductor Research Corporation for my work on dielectric technology and characterization.

10. In 2002, I became an IEEE fellow for my "contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices." I am also an IEEE Electron Devices Society Distinguished

Lecturer.

11. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

12. My *Curriculum Vitae* is provided as Ex. 1103.

13. My work in this matter is being billed at a rate of $475 per hour, with reimbursement for necessary and reasonable expenses. My compensation is not in any way contingent upon the outcome of this *Inter Partes* Review. I have no interest in the outcome of this proceeding or any related litigation.

II. UNDERSTANDING OF THE GOVERNING LAW

A. Invalidity By Anticipation Or Obviousness

14. I understand that a claim is invalid if it is anticipated or obvious. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in a single prior art reference, arranged as in the claim.

15. I further understand that obviousness of a claim requires that the claim be obvious from the perspective of a person of ordinary skill in the relevant art, at the time the invention was made. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any secondary considerations. I also understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. There may also be a specific teaching, suggestion or motivation to combine any first prior art reference with a second prior art reference. Such a teaching, suggestion, or motivation to combine the first prior art reference with the second prior art reference can be explicit or implicit in the first or second prior art references.

B. Interpreting Claims Before The Patent Office

16. I understand that "*Inter Partes* Review" is a proceeding before the United States Patent & Trademark Office ("Patent Office") for evaluating the validity of an issued patent claim. Claims in an *Inter Partes* Review are given their broadest reasonable interpretation that is consistent with the patent specification. I understand that a patent's "specification" includes all the figures, discussion, and claims within the patent document. I understand that the Patent

Office will look to the specification to see if there is a definition for a claim term, and if not, will apply the broadest reasonable interpretation from the perspective of a person of ordinary skill in the art.

C. Relevant Time Period For The Obviousness Analysis

17. I also understand that the earliest patent application filing leading to the ’902 patent was filed in November 12, 1996, with a foreign priority date of June 28, 1996. I have therefore analyzed obviousness as of approximately mid to late 1996 or slightly before, understanding that as time passes, the knowledge of a person of ordinary skill in the art will increase.

D. Basis For My Opinion

18. In forming my opinion, I have relied on the ’902 patent claims, disclosure and prosecution history, the prior art exhibits to the Petition for *Inter Partes* Review of the ’902 patent, and my own experience, expertise and knowledge of a person of ordinary skill in the relevant art in the relevant timeframe.

III. LEVEL OF ORDINARY SKILL IN THE ART IN THE RELEVANT TIMEFRAME

19. In 1996, I believe that a relevant person of ordinary skill in the art would have had an undergraduate degree in electrical engineering (or equivalent subject) together with three to four years of post-graduate experience designing semiconductor devices and fabrication processes, or a master’s degree in electrical

engineering (or equivalent subject) together with one to two years of post-graduate experience in designing semiconductor devices and fabrication processes. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa.

20. I believe that I would qualify as a person of at least ordinary skill in the art in 1996, and that I have a sufficient level of knowledge, experience and education, to provide an expert opinion in the field of the ’902 patent. Because of my work experience and the earlier date on which I received my bachelor’s, master’s, and Ph.D. degrees in electrical and computer engineering, and because of my work experience, by 1996 my own level of skill likely exceeded the ordinary level of skill in the art.

21. However, in my roles as professor of Electrical and Computer Engineering and as a member of technical staff at the TRW Microelectronics Center, I frequently worked with and taught individuals who were persons of ordinary skill in the art as defined above. Accordingly, I am well acquainted with the actual performance of a POSITA as defined above, and can approach technical issues from the perspective of such a person.

IV. PERSPECTIVE APPLIED IN THIS DECLARATION

22. My testimony in this declaration is given from the perspective of a person of ordinary skill in the art at the time of the filing of the ’902 patent, and for

some time before then, unless otherwise specifically indicated. This is true even if the testimony is given in the present tense. Each of the statements below is my opinion based on my review of the prior art, the '902 patent, and the claims, as well as the prior art cited in this declaration and the prosecution history of the '902 patent.

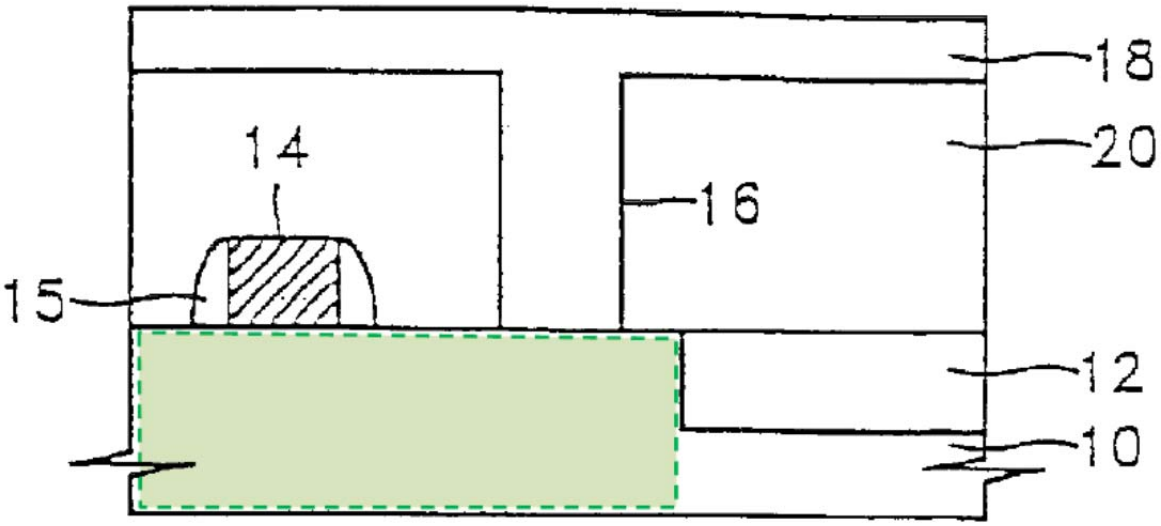
V. OVERVIEW OF THE '902 PATENT

A. Background

23. The purported invention of the '902 patent relates to methods for forming contact holes in microelectronic structures. For example, integrated circuit memory devices include a plurality of memory cells, and each memory cell is connected to other cells by conductive (metal) lines. '902 patent at 1:23-25. The cells and conductive (metal) lines are connected to the substrate by contact holes. *Id.* at 1:25-27. The contact holes expose active regions of the substrate. *Id.* at 1:28-29. Patterned gate electrode layers are generally arranged around the contact holes and are electrically isolated from the contact holes. *Id.* at 1:32-33.

24. Such structures are formed on a semiconductor substrate, as illustrated in Fig. 1. First, a field oxide layer **12** is formed on the substrate **10**. *Id.* at 1:52-53. The field oxide layer may be formed using a LOCOS field oxide layer or alternatively a trench field oxide layer. *Id.* at 1:45-50, 4:16-18. The field oxide layer defines the active region on the substrate **10**. *Id.* at 1:52-55. Annotated Fig.

1 of the ’902 patent shows a cross-sectional view of an integrated circuit device. *Id.* at Fig. 1.



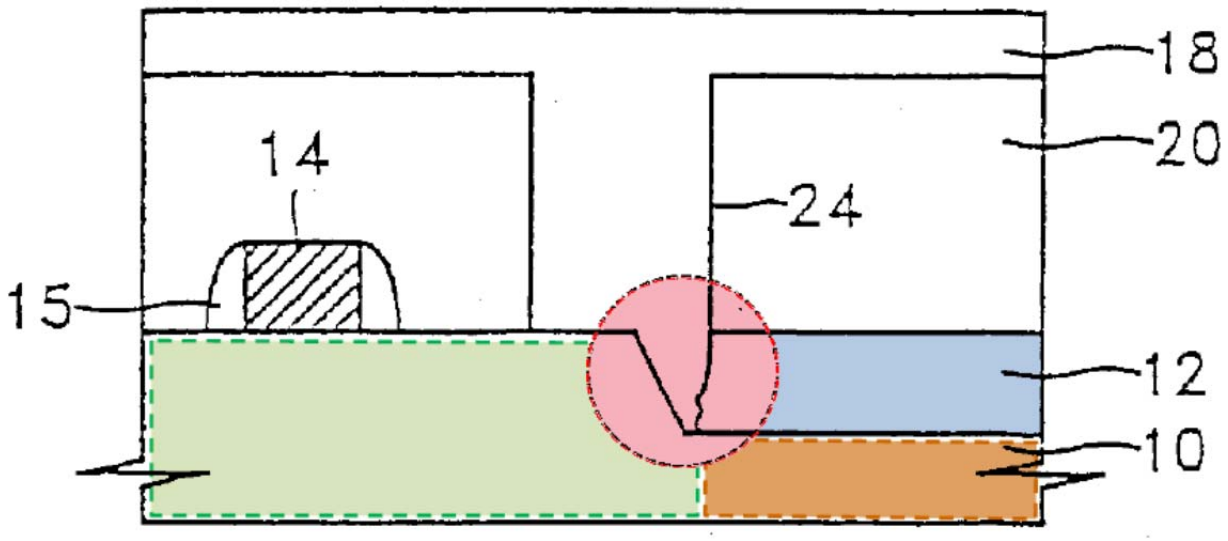
A gate electrode **14** is formed over the active region (highlighted green), and spacers **15** are formed along the sidewall. *Id.* at 1:52-56. An insulating layer **20** is formed on the surface of the substrate including the gate electrode **14** and the field oxide layer **12**. *Id.* at 1:56-58. A contact hole **16** is formed by etching the insulating layer **20** between the gate and field oxide layer to expose a portion of the active region. *Id.* at 1:58-60. A conductive layer **18** is formed on the insulating layer and fills the contact hole, creating a contact with the active region. *Id.* at 1:60-65.

B. Stated Problem

25. As integrated circuit devices become more highly integrated, the space available for forming devices is reduced. ’902 patent at 1:18-20. For

example, the space between the patterned layers is reduced, and accordingly the space available for forming the contact holes is also reduced. *Id.* at 1:36-38. Thus increased integration reduces the margin available in the placement of the holes, and leads to an increased risk in misaligned contact holes. *Id.* at 1:41-50.

26. Annotated Fig. 2 of the '902 patent shows a cross-sectional view of an integrated circuit device with a misaligned contact hole **24** exposing a portion of the active region (green) as well as a portion of the field oxide layer (blue) **12** on the field region (brown) in the substrate **10**. '902 patent at 2:10-12. This misalignment results in the formation of a well (red circle) through the field oxide layer **12** thus exposing a portion of a field region. *Id.* at 2:12-15.

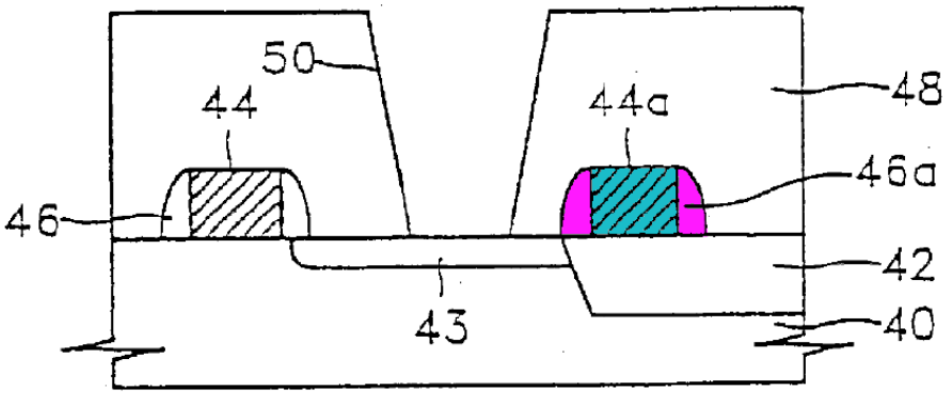


When the contact hole **24** is filled with the conductive layer **18**, the conductive layer **18** is brought into contact with the well. *Id.* at 2:17-19. Leakage current may thus flow through the conductive layer **18** into the well area and cause a delay or

malfunction in the device. *Id.* at 2:20-23.

C. Description of '902 Patent Alleged Invention

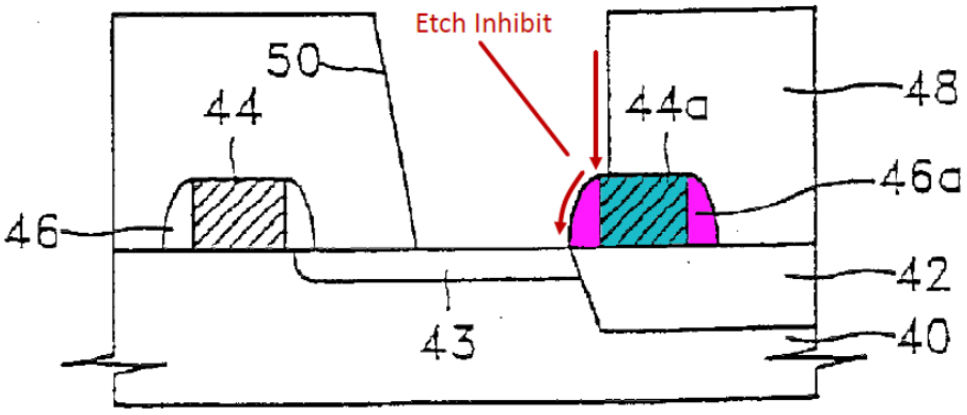
27. The '902 patent addresses the problem of contact hole misalignment by forming a second patterned conductive layer **44a** with insulating sidewall spacers **46a** on the field region:



'902 patent, Fig. 4. Compared to the first patterned conductive layer **44**, the second patterned conductive layer is electrically isolated and thus serves as a dummy pattern. *Id.* at 4:27-30.

28. An insulating layer is then formed over the surface of the substrate and the first and second patterned conductive layers. *Id.* at 3:31-33. A contact hole **50** is formed in the insulating layer **48** exposing a portion of the active region **43**. *Id.* at 3:33-35. Because the insulating layer is preferably formed of a material more susceptible to etching than the material used to form the sidewall spacers **46a**, some misalignment of the contact hole **50** can be tolerated. *Id.* at 4:37-42. In particular, if the contact hole extends beyond the active region of the substrate

encroaching into the field region, a second patterned conductive layer **44a** and its sidewall spacers **46a** act as an etch inhibitor when etching the insulating layer **48**:



'902 patent, Fig. 4; *Id.* at 4:42-48.

29. In the structure of the '902 patent invention, the area over which the contact hole can be formed is larger than the area available using the structure of the prior art cited in the '902 patent. *Id.* at 4:52-55. In the prior art Fig. 1, the contact hole must be formed between the gate electrode and the field oxide layer so as not to risk operational problems. *Id.* at 4:55-57. When using the structure of the '902 patent, the area over which the contact hole can be formed extends over a portion of the field region covered by the second patterned conductive layer. *Id.* at 4:58-61. Accordingly, a greater contact margin is allowed when forming the contact hole. *Id.* at 6:31-32. Etching margins can be increased without increasing the risk of damaging the field isolation layer. *Id.* at 6:33-34. Reliability of the integrated circuit device can thus be increased because leakage current generated by damage to the field isolation layer can be reduced. *Id.* at 6:35-37.

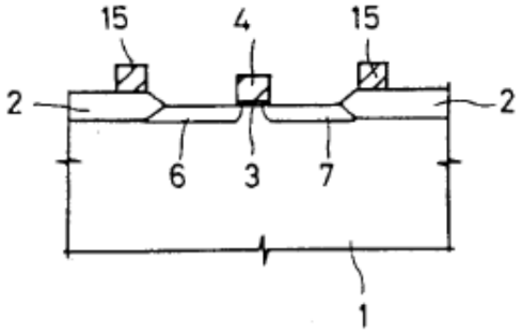
D. ’902 Patent Prosecution History

30. I have reviewed the prosecution history of the ’902 patent. While the Patent Office discussed several references during prosecution, it did not discuss the Lee, Yasushige, Nowak, or the ’524 Patent discussed below, nor were they cited. The Examiner thus likely did not consider any of these references.

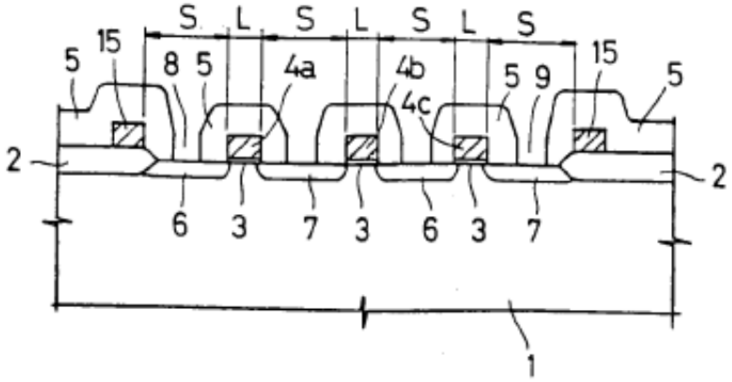
31. I also note that in applicant’s last Remarks before receiving the Notice of Allowance, applicant distinguished two combinations of references that the examiner had used to reject the claims under 35 U.S.C. § 103. Ex. 1102, FH, pp. 113-116. The examiner cited JP 4-63437 (“Michihiro”), US 5,550,076 (“Chen”), and US 5,441,916 (“Motonami”), with a combination of Michihiro in view of Chen and a combination of Michihiro in view of Motonami. Ex. 1104, Michihiro; Ex. 1105, Chen; Ex. 1106, Motonami.

Michihiro in view of Chen

32. In a non-final rejection, the examiner stated that Michihiro disclosed in Figs. 2(e), 4(b), and abstract, all elements of the independent claim except for “an insulating spacer” formed along a sidewall of the first patterned layer and a sidewall of the second pattern layer.” Ex. 1102, FH, Dec. 5, 2000, p. 4; *see also* Michihiro at Fig. 2e:



See also id. at Fig. 4(a):



33. The examiner noted that Chen teaches the obviousness of forming a second patterned layer on a field oxide isolation layer and a first patterned layer on the active region of a substrate, wherein the first and second patterned layers have insulating spacers formed thereon. Ex. 1102, FH, Dec. 5, 2000, p. 5; *see also id.*:

> Accordingly, it would have been ***obvious to modify the device structure of Michihiro*** by forming the insulating spacers along a sidewall of the first and second patterned layers, because as is well known, the insulating sidewall spacers would protect and prevent the first patterned conductive layer (gate electrode) and the second patterned conductive layer from contacting with the other adjacent

elements.[1]

34. In response, applicant did not dispute that all the elements were disclosed by Michihiro and Chen. Instead, applicant only argued, "there is no clear and particular evidence of a motivation for modifying Michihiro in view of Chen." Ex. 1102, FH, Mar. 7, 2001, p. 8. In particular, applicant argued that a POSITA could not combine Michihiro with Chen, because "Chen does not teach or suggest the use of a dummy pattern." *Id.* at 9 (emphasis in original). Further, "there is simply no mention in Michihiro that it is desirable to prevent damage to the field oxide layer." *Id.* "There is nothing in Michihiro which suggests that there is need to include spacers that would prevent damage to the field oxide layer in the event the contact hole is misaligned." *Id.* "Applicant respectfully submits that neither reference appreciates that misalignment of the contact hole during formation thereof can be a problem that can damage the field oxide layer." *Id.*

Michihiro in view of Motonami

35. Similarly, applicant submitted that there is no motivation to combine Michihiro with Motonami because, while they both discuss dummy patterns, 1) Michihiro discusses dummy patterns "to make the channels of mixed field effect transistors the same length and suppress fluctuation thereof"; and 2) Motonami only discusses providing dummy interconnections "in the vicinity of a step-like

[1] All emphasis added unless otherwise indicated.

portion so that 'the first and second conductive interconnection layers are precisely patterned within depth of focus.'" *Id.* at 11.

Notice of Allowance

36. In the Notice of Allowance, the Examiner stated: "the prior art of record fails to disclose all the process limitations recited in the base claims, including a combination of a step of forming a dummy pattern as an etch inhibiting layer on a field isolation layer and a step of forming along the sidewalls of a dummy pattern the spacers that will prevent damage to the field oxide layer in the event the contact hole is misaligned." As discussed below, prior art discloses this combination of limitations.

37. However, as explained below in the Overview of the Prior Art and Motivations to Combine the Prior Art References sections, both primary reference Lee and secondary reference Yasushige disclose the use of dummy patterns, the desirability to prevent damage to the field oxide layer, and using the dummy patterns or their spacers to prevent that damage. The Nowak reference discloses the use of dummy patterns with no electrical functions, and just mechanical functions.

VI. OVERVIEW OF THE PRIOR ART

A. KR App. No. 1994/021255 ("Lee")

38. The purported invention of the '902 patent relates to the forming of a

dummy pattern and spacers on a field oxide layer to serve as an etch inhibitor layer when forming contact holes. However, a Korean company Gold Star Electron Co., Ltd.[2] had already addressed the very same problems and designed and filed a patent application on the features described in the '902 patent more than two years prior to the filing date of the earliest parent application of the '902 patent. The patent application, KR App. No. 1994/021255 (Ex. 1107, "Lee"), is titled "Fabrication Method for Semiconductor Device" and lists Jeung Sang Lee of Korea as an inventor.

39. Lee is a Korean application filed on August 27, 1994. On March 22, 1996, in accordance with its patent laws,[3] the Korean Patent Office published in the Patent Gazette for "publication" KR Patent Pub. No. 1996-0009001 (Ex. 1112),

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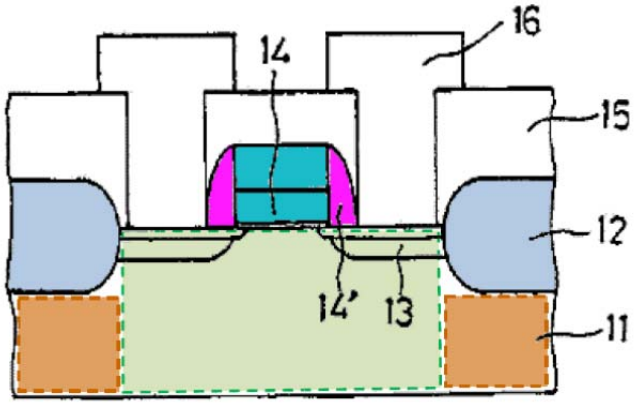
[2] Gold Star Electron Co., Ltd. changed named to LG Electronics in 1997. http://elliott.org/contacts/goldstar-lg-electronics-u-s-a/.

[3] Ex. 1108, Certified English translation of Korean Ministry of Government Legislation, Enforcement Decree of the Patent Act effective January 1, 1994, partially amended by Presidential Decree No. 14059 on Dec. 31, 1993, at p. 10, *available at* http://www.law.go.kr/lsInfoP.do?lsiSeq=30767&ancYd=19931231&ancNo=14059&efYd=19940101&nwJoYnInfo=N&efGubun=Y&chrClsCd=010202#0000

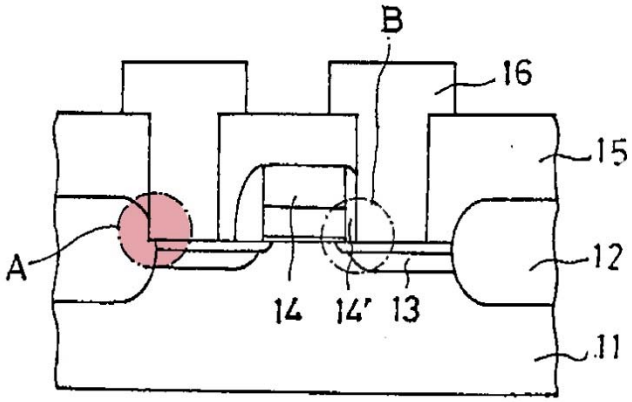
providing information on: 1) the applicant; 2) the application number, classification code and filing date; 3) the inventor; 4) application publication number and date of publication; ***5) title of invention; 6) scope of patent claims; 7) drawings;*** 8) priority claims; ***9) summary;*** and 7) other matters for the Lee application. By providing a publication of the title, claims, drawing, and summary of the invention of the Lee application, anyone can search and inspect the full Lee application. Based on my understanding of the law constituting a printed publication for purposes of prior art, the Korean Patent Office's laying open process is sufficient to make Lee a printed publication as of March 22, 1996. Lee is thus prior art to the '902 patent under 35 U.S.C. § 102(a).

40. Lee discloses a method for fabricating an improved semiconductor device with an etch stop layer for improving the alignment margin when forming a contact hole. Lee teaches in annotated Figure 1 below that in the prior art, a structure is formed by isolating an active region (green) with a field oxide layer **12** (blue) on a field region (brown) on a semiconductor substrate **11**, and patterning a gate **14** on the substrate. Lee at 17-2. A gate sidewall **14'** (purple) is formed on the gate using a deposition and etch-back process. *Id.* An interlayer insulation film **15** is deposited on top of the substrate and over the gate. Then, a contact hole that opens the source and drain region is formed through etching an interlayer insulation film **15**:



Lee at Fig. 1. The process is completed by depositing a conductive layer **16** into the contact hole to form the contact. *Id.* at 17-2.

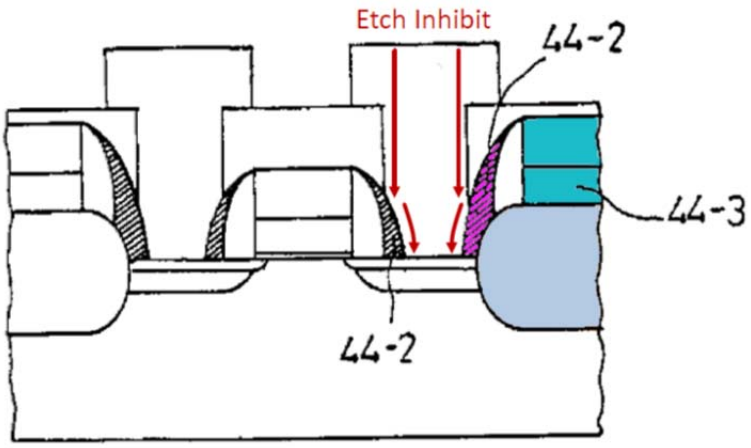
41. Lee recognized that the prior art method depended on the alignment accuracy of a photolithography process. *Id.* In the case of misalignment, the field oxide layer may be damaged, as shown in area A of annotated Fig. 1(b):



Such damage becomes the cause of junction leakage. *Id.* at 17-2.

42. To address this problem, Lee discloses a method of forming an etch stop layer around the source and drain region by depositing and etching back a spacer having a high etch selectivity **44-2** along the sidewalls of both an active gate

and a gate **44-3** on a field oxide layer, as shown in annotated Fig. 4:



Id. at Fig. 4. Lee discloses that the etch stop layers 44-2 are "in the form of a sidewall" and formed using the same process discussed by Lee to form a sidewall on the gate, by deposition and conducting etch-back. *Id.* at 17-5; *see* 17-2 ("forming a gate sidewall (14') using a deposition and etch-back process"). Lee discloses that the gate 44-3 serving as an etch inhibiting layer may be an adjacent internal connection line or a "dummy pattern."

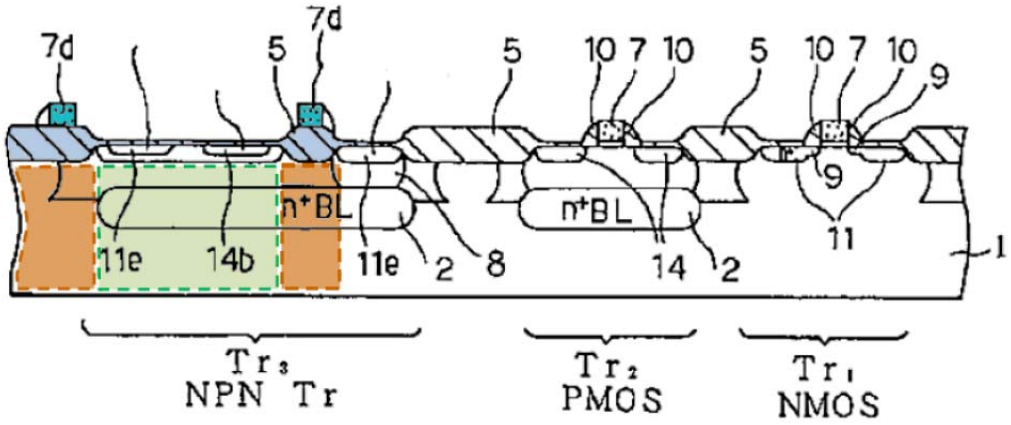
B. JP Pub. No. H7-86158 ("Yasushige")

43. Claim 1 of the '902 patent describes the use of a "dummy pattern" to serve as an etch inhibiting layer. While a POSITA would understand that Lee discloses that the dummy pattern is electrically isolated from the substrate and circuits thereon, Lee does not explicitly use the term "electrically isolated." However, the patent application publication, JP Pub. No. H7-86158 (Ex. 1109, "Yasushige") discloses a dummy pattern and explicitly states that it is "electrically

isolated" to solve the same problems of etching that Lee addressed. While Yasushige does not explicitly disclose a first patterned layer on an adjacent active region, the dummy pattern disclosed by Yasushige is formed on a field isolation layer, and serves as an etch stopper when etching an insulation layer formed over the substrate. The dummy pattern, made of a conductive film, serves in part to protect other insulation layers on the substrate, during an etch. Yasushige was filed by Sony Corporation almost three and a half years prior to the filing date of the earliest parent application of the '902 patent. It is titled "BICMOS Semiconductor Device and Manufacturing Method Thereof" and was filed on June 30, 1993, listing Hiroaki Yasushige and Norikazu Ouchi of Sony Corporation in Tokyo, Japan as inventors.

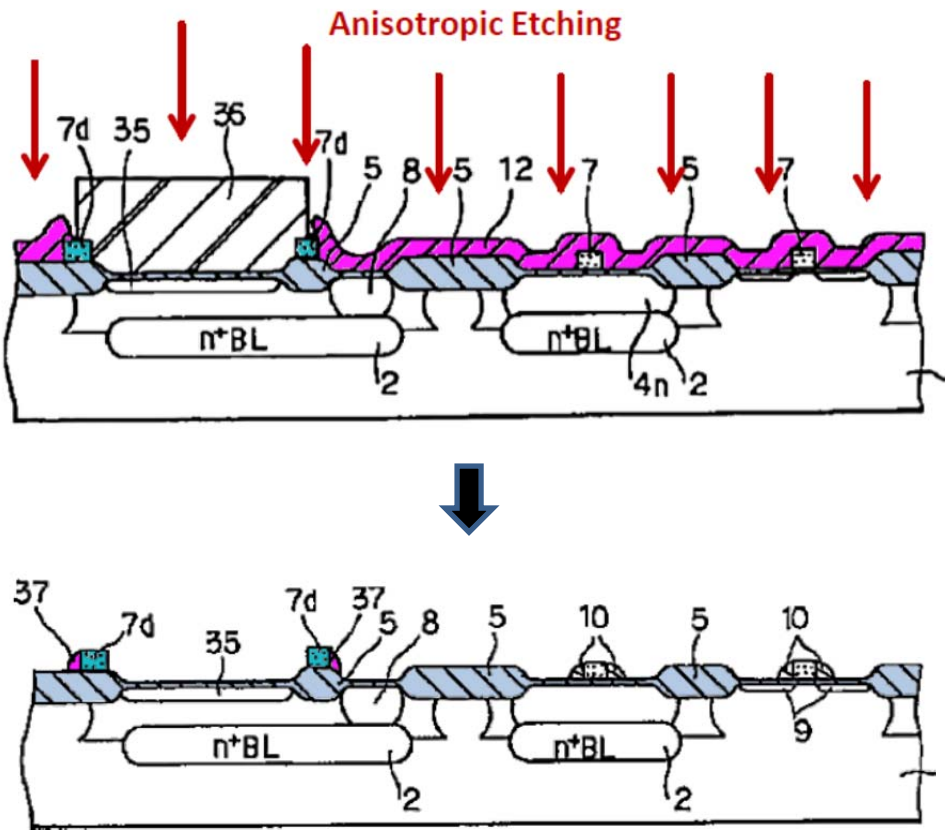
44. Yasushige was published on March 31, 1995 and is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

45. Yasushige discloses a technique for forming a dummy pattern **7d** around the base region of a semiconductor device, as shown in annotated Fig. 1:



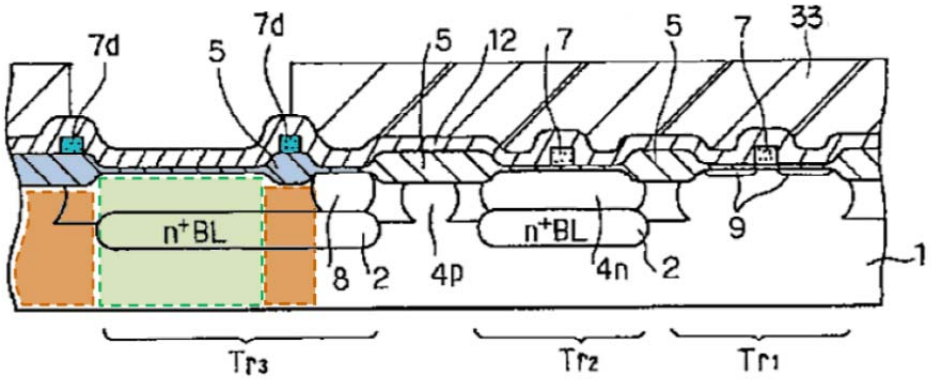
The dummy pattern **7d** is "identical" and formed "simultaneously" to the gate electrode **7** on the active region. Yasushige at ¶¶ 31, 41. Both dummy pattern and active gate electrode are made of a conductive material, poly Si film doped with phosphorus. *Id.* at ¶ 44. The dummy pattern is "formed around the base region **14b** of the bipolar transistor Tr3" on a field oxide layer made of an SiO2 film **5** and "***electrically isolated***." *Id.* at ¶ 29. As was known in the field, ion implantation is carried out on the base region to form diffused active regions. *Id.* at ¶ 42.

46. Yasushige recognized that during an etching process of an insulation film **12**, a mask alignment shift may cause damage to a field oxide region **5**, unless a dummy pattern protects the field oxide region. *Id.* at ¶ 50 (""Forming the dummy pattern **7d** can prevent said problem caused by mask alignment shift.""). As shown in annotated Fig. 6 to Fig. 7, the insulation film **12** is etched by performing an anisotropic etching process over the entire surface, where the dummy patterns protect the field oxide region **5**. *Id.* at ¶ 49.

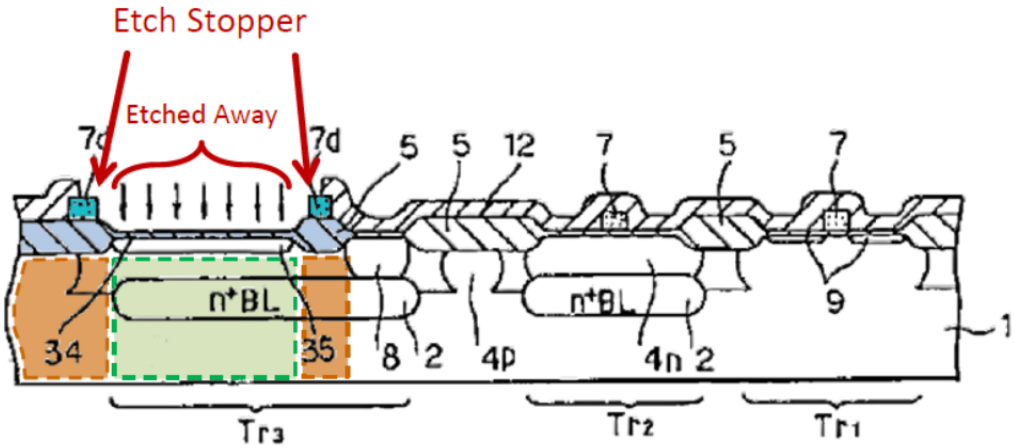


Without the dummy patterns, such over-etching would cause damage to the field oxide region 5, leading to an increase of the leakage current in the substrate. *Id.* at ¶ 50, 53.

47. Yasushige further discloses that the dummy pattern **7d** can serve as an etch stopper when an insulating film of the base region is removed by wet etching. Like Lee, Yasushige recognizes that a dummy pattern provides good etch selectivity against insulation layers formed on the substrate. As shown in annotated Fig. 4, a resist pattern 33 is set up first over the substrate with an opening to the base region:



Then, a wet etching process is used to remove the insulating film **12**, as shown in annotated Fig. 5:



As shown in Fig. 5, the edge of the opening is etched until it reaches the dummy pattern, which stops the etch. *Id.* at 46.

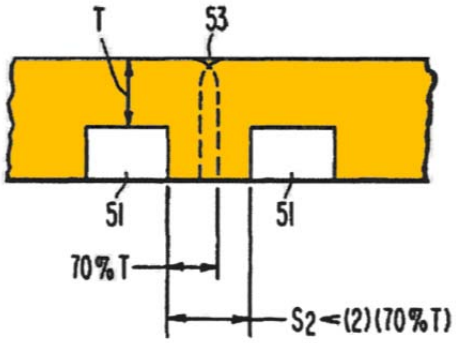
C. U.S. Patent 4,916,514 ("Nowak")

48. The '902 patent describes the use of an insulating layer comprising nitride. While Lee discloses an insulating layer, Lee does not explicitly disclose that the insulating layer comprises nitride, as recited in dependent claims 2 and 17. However, this is an obvious design choice, as there are limited options in

semiconductor fabrication for insulating materials (mainly oxides or nitrides). Further, the well-known use of silicon nitride or oxynitride as the material for the insulation layer is disclosed by Unisys Corporation in U.S. Patent No. 4,916,514 (Ex. 1110, "Nowak"), listing Matthew Nowak as an inventor and titled "Integrated Circuit Employing Dummy Conductors for Planarity." Nowak was filed on May 31, 1988 and issued on April 10, 1990, more than six years prior to the filing date of the earliest parent application of the '902 patent.

49. Nowak is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

50. While Nowak does not explicitly disclose the specific configuration of forming a contact hole between a dummy conductor and a gate on an active region like the '902 patent, Nowak discloses forming electrically isolated dummy conductors on an insulating layer on a substrate. Nowak at 3:18-22. The dummy conductors are made of the same material, patterned with the same mask, and are formed by the same fabrication steps as signal conductors on the substrate. *Id.* at 2:59-66. The dummy conductors have no electrical function, and thus are "open circuited" and carry no signals. *Id.* at 3:1-3, Abstract. Nowak further discloses that a layer of insulating material, such as silicon nitride or oxynitride, is "used to cover the dummy conductors" and form conformally over the substrate, as shown in annotated Fig. 5B:



Id. at 3:65-4:2.

D. U.S. Patent 4,952,524 ("the '524 Patent")

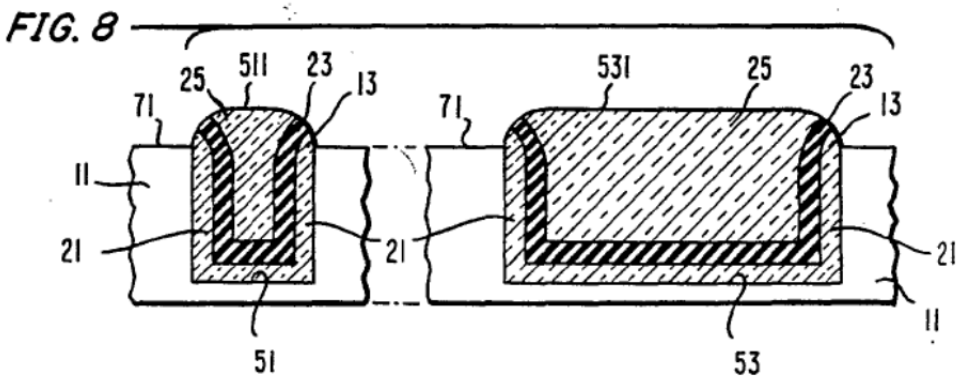
51. The '902 Patent describes the use of a field oxide layer formed in a trench of the substrate and recites this limitation in claims 6 and 13. While Lee does not explicitly use the word "trench," a POSITA would understand that the disclosure in Lee may include a trench field oxide layer. Further, this is an obvious design choice, and is explicitly disclosed by AT&T Bell Labs in U.S. Patent No. 4,952,524 (Ex. 1111, "the '524 Patent"), listing Kuo-Hua Lee and Chih-Yuan Lu as inventors and titled "Semiconductor Device Manufacture Including Trench Formation." The '524 Patent was filed on May 5, 1989 and issued on Aug. 28, 1990, six years prior to the filing date of the earliest parent application of the '902 patent.

52. The '524 Patent is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

53. While it does not discuss the use of a dummy gate as an etch inhibitor, the '524 Patent discloses a method for forming an improved trench isolation layer

in a semiconductor substrate. The '524 Patent discloses using "trenches for inter-device isolation." '524 Patent at 1:9. Traditionally, "trench isolation involves etching a narrow, deep trench or groove in a silicon substrate and then filling the trench with a filler material such as a silicon oxide or polysilicon." *Id.* at 1:24-25. The '524 Patent discloses both a "narrow trench" and a "wide trench." *Id.* at 2:60-61, Figs. 7-9. It further discloses at least one specific etching recipe for forming a trench. *Id.* at 3:30-38. Then, trenches may be filled with multiple layers, "an exemplary candidate for filler layer 25 is an oxide." *Id.* at 4:28-29.

54. These techniques result in oxide-filled trenches with upper surfaces that protrude somewhat beyond the upper surface of the substrate:



'524 Patent at Fig. 8, 6:6-8. Fig. 8 shows a narrow trench **51** and a wide trench **53**. The '524 Patent further discloses trenches with slanted sidewalls, as a technique known to a POSITA. *Id.* at 7:29-31.

VII. MOTIVATIONS TO COMBINE THE PRIOR ART REFERENCES

A. Motivation To Combine Lee with Yasushige

55. A POSITA would have been motivated to combine the teachings of the Lee and Yasushige in order to achieve the methods claimed in the ’902 patent.

1. Same Technology

56. A POSITA would have been motivated to combine Lee with Yasushige because both Lee and Yasushige are directed to forming etch stoppers on field oxide regions surrounding an active region on a semiconductor substrate. In particular, as shown above, both patents disclose forming dummy pattern structures on a field oxide layer. Both Lee and Yasushige recognize that dummy patterns provide good etch selectivity against the insulation layers formed on the substrate, and particularly as a barrier to protect other insulating layers on the substrate from the etch, such as underlying field oxide regions. Both patents teach that the dummy pattern structures are identical to adjacent MOS gate transistors. Both patents further discuss the other processes for forming structures for an electronic device, such as ion implantation on the active region, forming patterned conductive gates, forming gate sidewalls using an anisotropic etching process, and depositing an interlayer insulating film.

2. Same Problem

57. Both Lee and Yasushige use dummy patterns to solve the problem of a misalignment in an etching process resulting in over-etching of an insulating layer and causing damage to a field oxide layer. Lee at 17-2; Yasushige at 50

("The case where there is no dummy pattern 7d is considered . . . the SiO2 film 5 of the field is shaved at the time of anisotropic etching."). In both Lee and Yasushige, the dummy patterns are used as etch stoppers for etching an insulating layer formed on the substrate. Lee disclosed that damage to the field oxide layer from etching "becomes the cause of junction leakage." Lee at 17-2. Yasushige recognized that etching could shave the field oxide region (Yasushige at 50), leading to damage that could result in "problems such as an increase in the leakage current." *Id.* at 53.

58. While Lee discloses an etch stop layer on a dummy pattern, Yasushige also discloses using dummy patterns on field oxide layers to serve as an etch stopper around a base, or active, region, and protecting a field oxide layer:

> As shown in FIG. 4, a resist pattern 33 that opens the base region of NPN transistor part Tr3 is formed after forming the SiO2 film 12 over the entire surface. At this time, the ***edge of the opening is made until it reaches the dummy pattern 7d.*** Yasushige at [45].
>
> As shown in Fig. 5, the insulating film of the base region is removed by wet etching. At this time, the ***dummy pattern 7d serves as an etching stopper***. Yasushige at [46].
>
> As shown in Fig. 7, sidewalls 10 and 37 are formed . . . by performing an anisotropic etching process over the entire surface. . . . Forming the dummy pattern 7d can prevent said problem caused by mask alignment shift. *Id.* at [0049-50].

A POSITA would have recognized that Lee and Yasushige were solving a

common problem and been motivated to combine the teachings of forming a dummy pattern as an etch stopper. Based on the similar concern over damage from etching insulation layers, a POSITA would have looked to combine Lee with the teaching from Yasushige so as to ensure that the dummy pattern is electrically isolated on a field oxide region. Since the dummy pattern is intended to protect against an etch on insulation layers, a POSITA knew to position the dummy pattern completely over other insulation layers, such as a field oxide layer, for best coverage. Further, a POSITA understood that keeping the dummy pattern electrically isolated ensures that the dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern. A POSITA would have been motivated to keep the dummy pattern electrically isolated, given that its sole function is for a mechanical purpose as an etch stop, and avoid adding additional electrical connections to the subtrate that are unnecessary.

3. Nothing Incompatible

59. Nothing in these prior references teaches away from their combination. There is no essential feature in any of these references that conflicts with an essential feature of any other reference. To the contrary, these references are a natural fit, as evidenced by both Lee and Yasushige teaching the use of a dummy pattern on a field oxide layer to serve as an etch stop for an etching

process. Many aspects of forming gates and transistors on a semiconductor substrate were well-known to a POSITA, and Lee and Yasushige use many of the same techniques, e.g., ion implantation, patterning gates, anisotropic etching.

4. Additional Reasons to Combine

60. As discussed in the '902 Patent, devices were becoming more integrated, reducing the space available on a substrate. Thus, there is less room for error in the process steps of semiconductor manufacturing.

61. Members of the semiconductor field were constantly looking for ways to improve the manufacturing process, to make circuits smaller. Both Lee and Yasushige teach methods of manufacturing intended to both increase the margin for error while not introducing extra process steps. For example, both Lee and Yasushige use dummy patterns that are identical to and simultaneously created with the active gates, thus not requiring extra deposition or patterning steps. Lee discloses that because etch stop spacers are "formed through self-alignment without a separate mask, there is no additional process." Lee at 17-7. And as discussed above, both Lee and Yasushige focus on solving issues of misalignment, and improving room for error. Especially in this field, a POSITA would have been motivated to combine Lee and Yasushige to attempt to improve the manufacturing process.

B. Motivation To Combine Lee and Yasushige with Nowak

62. A POSITA would have been motivated to combine the teachings of Lee and Yasushige with Nowak in the manner described above for several reasons.

1. Same Technology

63. A person of ordinary skill in the art would have been motivated to look to Nowak for details regarding the semiconductor fabrication processes disclosed in Lee and Yasushige. All three of these references disclose a technology for forming well-known structures, such as gates, field isolation layers, and insulation layers on a semiconductor substrate. Lee, Yasushige, and Nowak all teach methods of forming electrically isolated dummy patterns on a substrate to perform mechanical functions.

2. Well Known Techniques

64. While all three references disclose a method for fabricating a semiconductor device, and describe similar structures and fabrication techniques, each reference provides different levels of details, which are well known to a POSITA. For example, Nowak discloses forming an insulation layer over dummy conductors, similar to Lee and Yasushige, but describes the well-known use of silicon nitride or oxynitride as the material for the insulation layer, which is claimed in dependent claims 2 and 17.

3. Nothing Incompatible

65. Nothing in these prior references teaches away from their

combination. There is no essential feature in any of these references that conflicts with an essential feature of any other reference. To the contrary, these references are a natural fit, as evidenced by all three of the references, Lee, Yasushige, and Nowak teaching the use of electrically isolated dummy patterns formed on insulation layers to perform mechanical functions.

C. Motivation To Combine Lee, Yasushige, and the '524 Patent

66. A POSITA would have been motivated to combine the teachings of Lee, Yasushige, and the '524 Patent in the manner described above for several reasons.

67. A person of ordinary skill in the art would have been motivated to look to the '524 Patent for details regarding the semiconductor fabrication processes disclosed in Lee and Yasushige. All three of these references disclose a technology for forming well-known structures, such as gates, field isolation layers, and insulation layers on a semiconductor substrate. Lee and Yasushige both teach methods of forming electrically isolated dummy patterns on a substrate to perform mechanical functions. The '524 patent describes in detail the insulation layers formed over the dummy patterns.

68. The '524 Patent discloses forming trench isolation layers, to provide electrical isolation for active regions on a substrate. It was well known to a POSITA to use either a LOCOS method or trench isolation method to form a field

oxide layer. Moreover, the benefits and drawbacks of LOCOS and trench isolation were well known to a POSITA. As discussed in the '524 Patent for the prior art, a LOCOS method for growing a field oxide layer would often result in encroachment of the oxide layer onto the active region. While Lee discloses the formation of a field oxide layer, Lee does not explicitly disclose the method. However, a POSITA would know that the issue described in Lee—increasing margin of error for forming a contact hole over a field oxide layer—would benefit from using a trench isolation technique that decreased the area used by the field oxide layer. Accordingly, a POSITA certainly would have been motivated to combine Lee with the teaching of a trench isolation layer in the '524 Patent.

69. Nothing in these prior references teaches away from their combination. There is no essential feature in any of these references that conflicts with an essential feature of any other reference. To the contrary, these references are a natural fit, as evidenced by the fact that Lee is compatible with the teaching of a trench isolation layer in the '524 Patent. For example, while Lee teaches the formation of an etch stop layer on the side of a field oxide layer, Lee appears to contemplate that the field oxide layer may be formed in a trench with a lower protrusion—thus having insufficient "step" to form the etch stop layer (Lee at 17-6)—and proposes an embodiment where a dummy pattern formed on the trench serves as the "step" for the etch stop layer to be formed.

VIII. CLAIM CONSTRUCTIONS

70. I understand that in deciding whether to institute *Inter Partes* review, "A claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). I understand that this claim construction standard is different from - and typically broader than that applied in district court. I further understand that "the broader standard serves to identify ambiguities in the claims that can then be clarified through claim amendments." Final Rules, 77 Fed. Reg. at 48699.

71. I applied this broadest reasonable construction standard to my review of the claims of the '902 patent discussed below. Further, I have reviewed the proposed constructions submitted by the parties in the district court action *Samsung Electronics Co. Ltd., et al. v. NVIDIA Corp. et al.*, 3:14-cv-00757-REP (E.D. Va.) (the "District Court Action"). (Ex. 1115.) The parties' differing constructions do not impact my analysis below, as under either parties' constructions, the claims are shown to be invalid.

72. I provide below a construction, under the broadest reasonable construction standard, of claim terms "insulating spacer along a sidewall of the [second] patterned conductive layer," "an insulating layer," and "forming a trench in said substrate, and wherein said field isolation layer fills said trench." I reserve the right to propose alternate or additional constructions in any other proceedings,

where the standard may differ.

A. "insulating spacer along a sidewall of the [second] patterned conductive layer"

73. The term "insulating spacer along a sidewall of the [second] patterned conductive layer" is used in challenged independent claims 1, 11, 12, 15, and 18.

74. A POSITA would have generally understood "insulating spacer along a sidewall of the [second] patterned conductive layer," in light of the specification, to mean "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." The specification describes the "present invention" to "allow[] the misalignment of the contact hole without damaging the field isolation layer." *Id.* at 2:49-54, *see also id.* at 3:44-48 ("The methods and structures of the present invention thus provide protection for the field isolation layer during the formation of a contact hole.") Further, in "the present invention" (*Id.* at 4:62-64) "a contact hole can thus be self-aligned using the spacers 46 and 46a," (*Id.* at 5:26-32) as illustrated in Fig. 8.

75. As discussed in Section V, the specification is confirmed by the prosecution history, where the Applicant distinguished prior art that did not "suggest[] that there is need to include spacers that would prevent damage to the field oxide layer in the event the contact hole is misaligned," and the Examiner agreed and re-stated this understanding in the Reasons for Allowance. (Ex. 1102,

'902 FH, 3/5/2001 Amendment, p. 9; 5/2/2001 Reasons for Allowance, p. 2.)

76. Accordingly, in my opinion, the broadest reasonable construction of the term "insulating spacer along a sidewall of the [second] patterned conductive layer" is, consistent with the specification, "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." My invalidity analysis below relies on this construction and does not depend on the exact articulation.

B. "an insulating layer"

77. In the District Court Action, patent owner Samsung has taken the position that the term "an insulating layer" should be construed to mean "a structure comprising one or more electrically insulating sublayers." (Ex. 1115 at 2.) My invalidity analysis below relies on the plain and ordinary meaning of the term "an insulating layer." However, as explained further below, the prior art discussed in this declaration meets Samsung's proposed construction of this term in the District Court Action.

C. "forming a trench in said substrate, and wherein said field isolation layer fills said trench"

78. In the District Court Action, patent owner Samsung has taken the position that the term "forming a trench in said substrate, and wherein said field isolation layer fills said trench" should be construed to mean "etching a recess into said substrate and subsequently filling said recess with a field isolation layer."

(Ex. 1115 at 2.)

79. My invalidity analysis below relies on the plain and ordinary meaning of the term "forming a trench in said substrate, and wherein said field isolation layer fills said trench." However, as explained further below, the prior art discussed in this declaration meets Samsung's proposed construction of this term in the District Court Action.

IX. SUMMARY OF OPINIONS

80. Claims 1, 3-5, 7-12, 14-16, and 18 are rendered obvious by Lee and Yasushige.

81. Claims 2 and 17 are rendered obvious by Lee in combination with Yasushige and Nowak.

82. Claims 6 and 13 are rendered obvious by Lee in combination with Yasushige and the '524 patent.

X. FIRST GROUND OF INVALIDITY – OBVIOUSNESS BY LEE IN COMBINATION WITH YASUSHIGE

A. Claim 1

[1pre] "A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:"

83. To the extent the preamble is a limitation, Lee discloses this limitation.

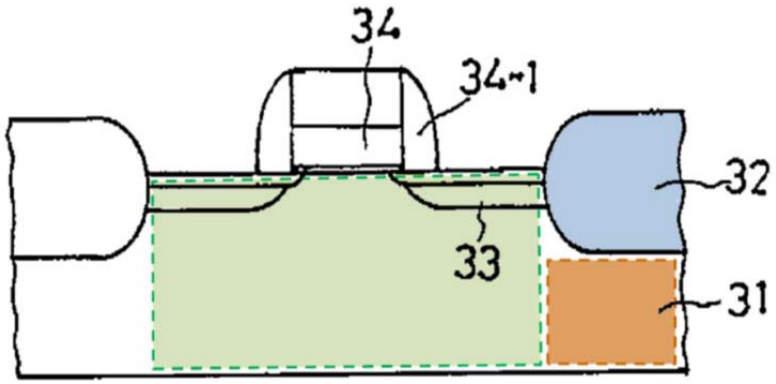
84. Lee discloses "[a] method for fabricating a semiconductor device, and

specifically pertains to a method for fabricating semiconductor device, in which the characteristics of the device are improved by securing an align margin upon formation of the contact hole." Lee at 17-1.

[1a] "defining adjacent active and field regions on a substrate, and circuits thereon;"

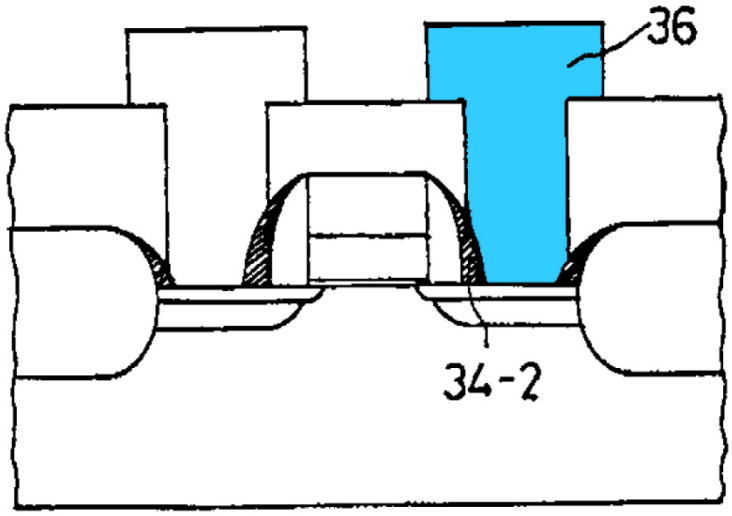
85. In the '902 patent, an active region is defined by forming a field isolation layer, such as an oxide layer, on a field region of the substrate. '902 patent at 4:11-16 ("Portions of the substrate not covered by the field isolation layer ***define the active region*** where microelectronic devices will be formed.").

86. Lee discloses "defining adjacent active and field regions on a substrate." Lee discloses "an active region is ***isolated electrically from the surrounding active regions by forming a field oxide layer*** (32) on a semiconductor substrate (31)" as shown in annotated Fig. 3(a):



Lee at 17-5, Fig. 3(a). The active region (highlighted green) is adjacent the field oxide layer 32. A POSITA understands that the field region is then defined by the area of the substrate where field oxide layer 32 is formed.

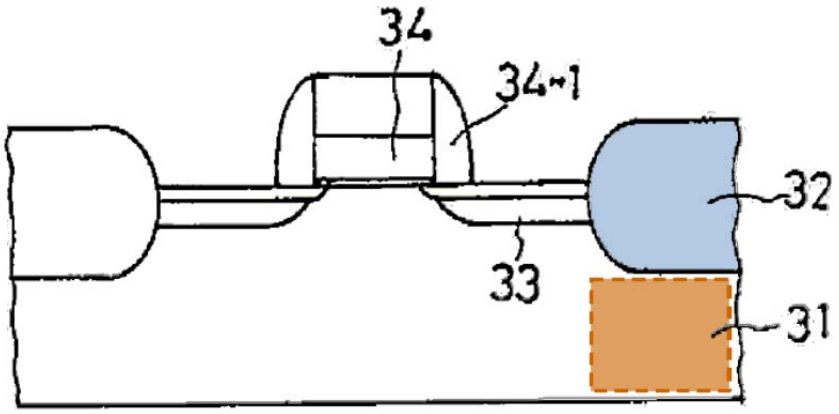
87. Lee further discloses defining "circuits thereon." Lee discloses forming a transistor on the substrate with a junction contact formed with a conductive layer (36) composed of conductive material:



Lee at 17-6, annotated Fig. 3(d). One of skill in the art understands that a circuit is defined by forming a transistor and junction contacts.

[1b] "forming a field isolation layer on said field region;"

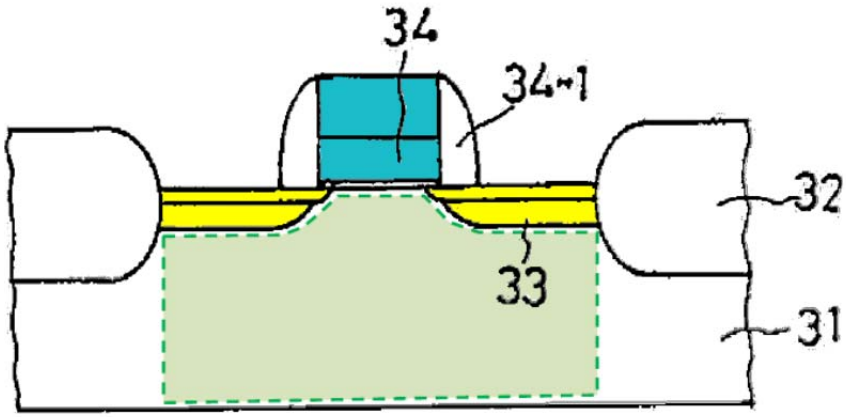
88. Lee discloses "an active region is ***isolated electrically from the surrounding active regions by forming a field oxide layer*** (32) on a semiconductor substrate (31)" as shown in annotated Fig. 3(a):



Lee at 17-5, Fig. 3(a). The field oxide layer 32 is on the field region (shaded brown) of the substrate **31** and is a field isolation layer.

[1c] "forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;"

89. Lee discloses "an ***active region*** is isolated electrically from the surrounding active regions by forming a field oxide layer (32) on a semiconductor substrate (31), and an ***MOS gate (34)*** is formed by ***depositing and etching*** gate oxide layer, ***poly*** and gate cap in order" as shown in annotated Fig. 3(a):



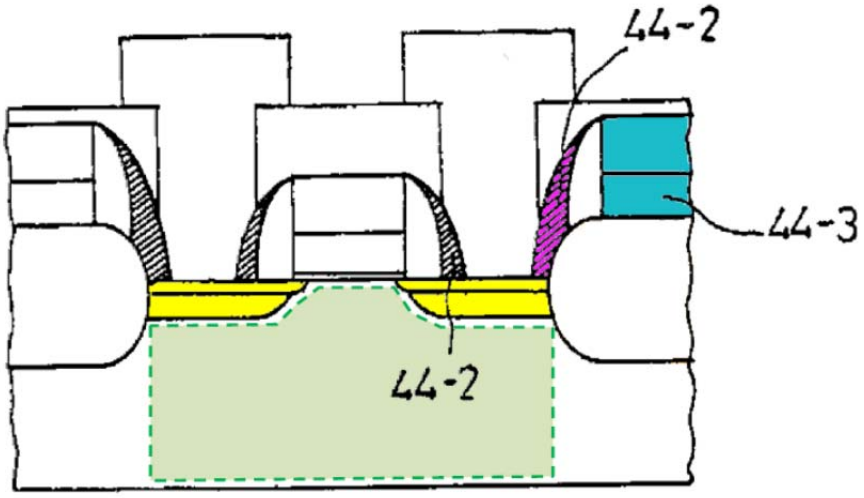
Lee at 17-5, Fig. 3(a). Lee's disclosure of depositing layers and etching the layers discloses forming a "patterned" layer. *Id.* at 17-5. Lee further discloses a "poly" layer, which a POSITA understands to be a conductive polysilicon layer. *Id.*

90. As further shown in Lee at Fig. 3(a), the MOS gate is formed on the active region (shaded green) separated from the field oxide layer **32**. It would have been a natural design choice for the MOS gate to be formed entirely on the active region, and spaced apart from the field region (shaded brown) defined by the field oxide layer **32**.

[1d] "forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate,"

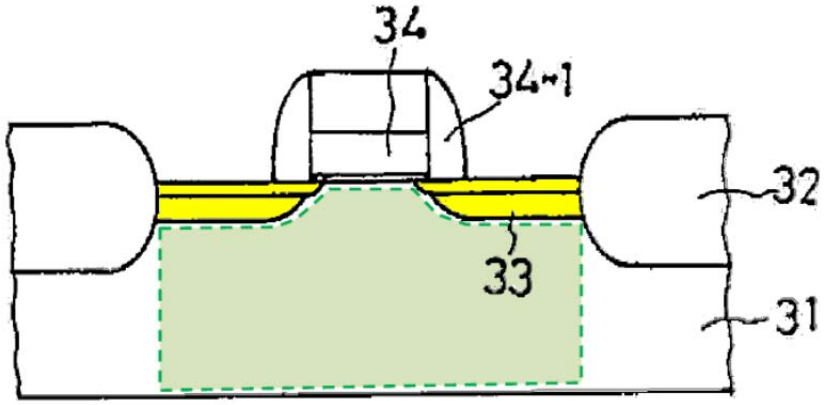
91. Lee discloses "forming an etch inhibiting layer." Lee discloses forming an etch stop layer by "depositing a material having a high etch selectivity with an interlayer insulation film." Lee at 17-5. "[T]he etch stop layer is formed with a conductive or non-conductive material." *Id.* at 17-6.

92. Lee further discloses that the etch inhibiting layer is formed "on said field isolation layer adjacent said active region of said substrate." For example, Fig. 4 shows that the etch-inhibiting layer is formed on the field isolation layer as a spacer (44-2) on the sidewall of a dummy pattern (44-3), and is adjacent to the active region:



Id. at annotated Fig. 4, 17-6.

93. Lee further confirms that the "etch stop layer" of the contact etching process is "***formed around the impurity region*** in the form of a sidewall." *Id.* at 17-5. Lee discloses that a high concentration impurity region is formed in the active region to make a source and drain region (33), shown in annotated Fig. 3(a):



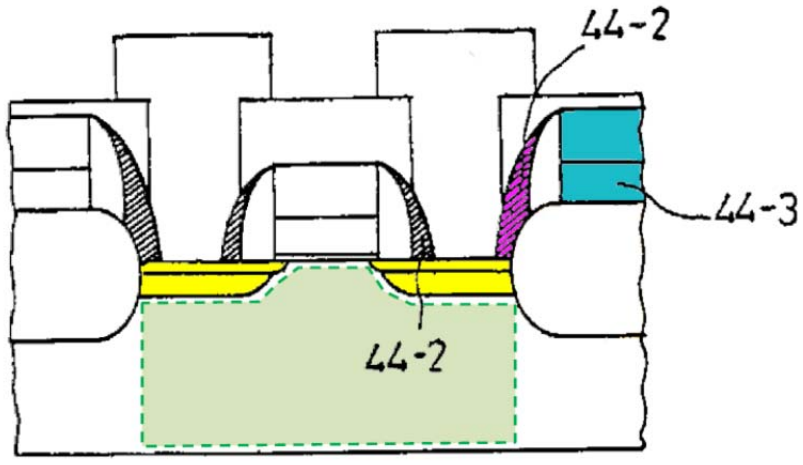
Lee at Fig. 3(a), 17-5; *see also* 17-4 ("making a source and drain region which is formed by doping impurity on the gate in the active region on a semiconductor

substrate and the substrate around the gate"). Thus the etch stop layer is formed ***around*** the active region, or the impurity region, and since it is formed along the side of the dummy pattern, accordingly the dummy pattern and the etch stop layer formed on it are adjacent to the active region.

[1e] "the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer,"

94. As discussed in element [1c], Lee discloses that "the active region includ[es] the first patterned conductive layer."

95. Lee further discloses "wherein said etch inhibiting layer comprises a second patterned conductive layer." Lee discloses an embodiment in Fig. 4 where the etch stop layer (44-2) is formed using "an internal connection line (44-3) passing adjacently or the step of a ***dummy pattern***":



Lee at Fig. 4 (annotated), 17-6. As shown in Fig. 4, the etch inhibiting layer

comprises a second patterned conductive layer (44-3), that may be a dummy pattern.

96. Lee discloses "an insulating spacer along a sidewall of the second patterned conductive layer." As discussed above, "an insulating spacer along a sidewall of the second patterned conductive layer" should be construed as "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." My opinion below does not change under Samsung's construction proffered in district court for this limitation.

97. As shown above in annotated Fig. 4, Lee discloses forming the etch stop layer **44-2** as a spacer along a sidewall of the second patterned conductive layer (**44-3**). Lee discloses that the etch stop layer is formed with a "non-conductive material," and is thus an insulating layer. *Id.* at 17-6. Lee discloses that the "a process alignment margin is secured when forming a contact hole by forming an etch stop layer on the contact hole area to protect the lower insulating layer," (*id.* at 17-4), and as further shown in Fig. 4, etch stop layer 44-2 prevents etch damage to the field isolation layer if the contact hole is misaligned.

98. The etch stop layer 44-2 in Lee is identical in structure to the insulating spacer formed along a sidewall of the patterned conductive layer 44-3, and is formed right next to a first insulating spacer. Lee discloses that the etch stop

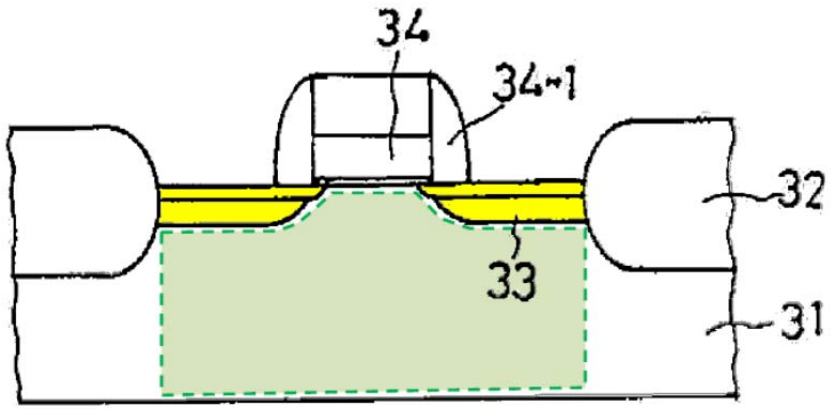
layer (44-2) is formed in the "form of a sidewall" and using the same process for making a sidewall:

> At this time, the etch stop layer is formed with conductive or non-conductive material, and it is formed ***in the form of a sidewall*** through a ***deposition and etch-back process*** using the step area formed on the lower layer without any additional mask.

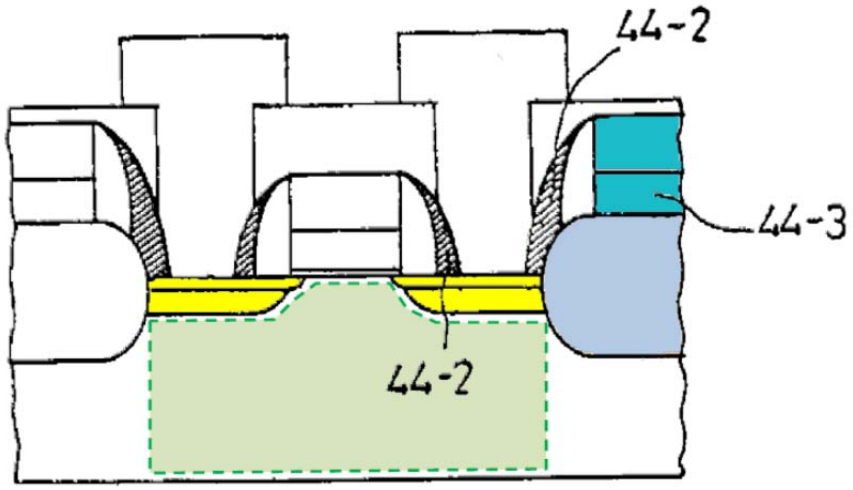
Lee at 17-6. The deposition and etch-back process is the same process for making an insulating sidewall spacer disclosed by Lee. *Id*. at 17-5 ("forming a gate sidewall (34-1) using a deposition and etch-back process"). Thus, Lee's disclosure of the etch stop layer 44-2 formed on the dummy pattern 44-3 meets the limitation "an insulating spacer along a sidewall of the second patterned conductive layer."

[1f] "wherein the second patterned conductive layer does not extend over the active region of the substrate,"

99. Lee discloses that the second patterned conductive layer does not extend over the active region of the substrate. For example, Lee discloses that a high concentration impurity region is formed in the active region to make a source and drain region (33), shown in annotated Fig. 3(a):



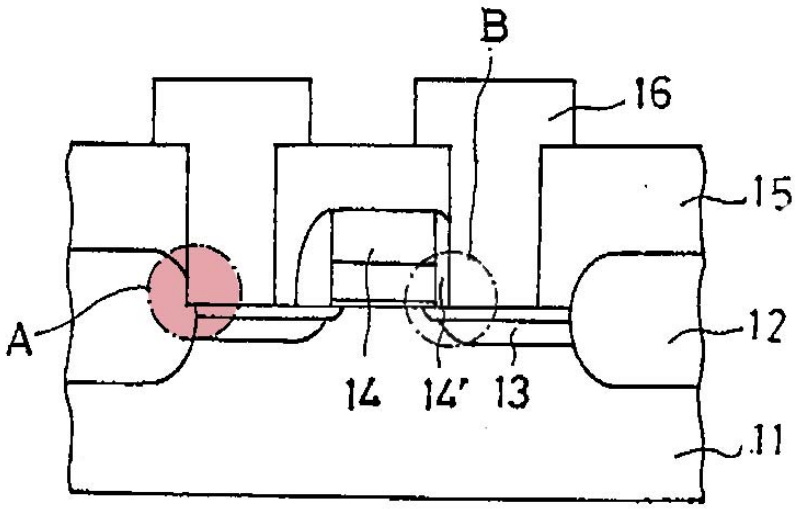
Lee at Fig. 3(a), 17-6. Annotated Fig. 4 shows that the conductive pattern (44-3) is formed on the field isolation layer, and is adjacent to the active region (highlighted green):



Id. at Fig. 4, 17-6. Lee further confirms that the etch stop layer **44-2** of the contact etching process is "formed ***around the impurity region*** in the form of a sidewall." *Id.* at 17-5. Because the etch stop layer is formed around the active, or impurity, region, and is thus sitting on the border of the active and field regions as shown in

Fig. 4, the second patterned conductive layer inside the etch stop layer is formed entirely on the field isolation layer and does not extend over the active region of the substrate.

100. As further discussed in Lee, the etch stop layer is intended to protect the field oxide layer when forming a contact hole:



Lee at Fig. 1(b) (annotated), 17-2. As shown in the region marked A in Fig. 1(b) above, a misalignment in the photolithography process to form a contact hole may cause damage to the field oxide layer and result in junction leakage. *Id.* Accordingly, based at least on Lee's disclosures that 1) the etch stop layer 44-2 is formed ***around*** the active region; 2) the etch stop layer protects the edge of the field oxide layer from damage in a contact hole formation process; and 3) the etch stop layer is formed along the sidewall of the second patterned conductive layer, as shown in Fig. 4 and further discussed in element 1[e], one of skill in the art would

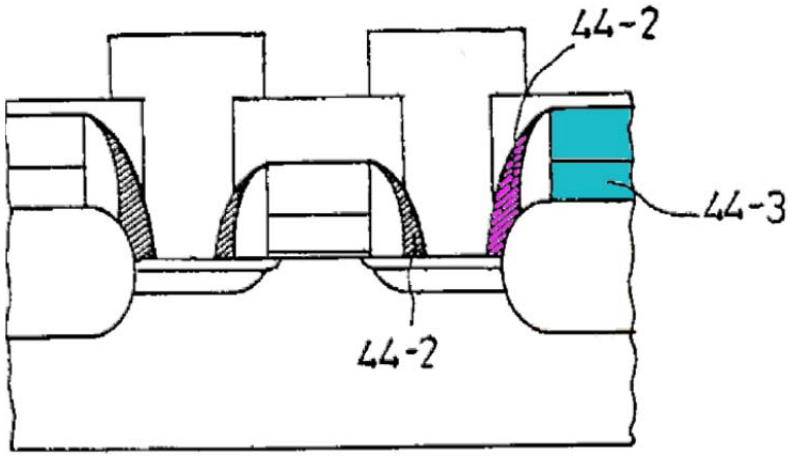
know that the second patterned conductive layer does not extend over the active region of the substrate.

101. To the extent that this limitation "the second patterned conductive layer does not extend over the active region of the substrate" is not explicitly disclosed in Lee, this limitation is obvious based on Lee in view of Yasushige. Yasushige explicitly discloses a dummy pattern that is "electrically isolated from the base region by an isolation region," and thus the dummy pattern does not extend to the active region. Yasushige at Fig. 1 (base region 14b corresponds to active region), 29, 41. A POSITA would have combined the teaching in Lee of a dummy pattern used as an etch inhibiting layer, with the explicit disclosure in Yasushige that such a dummy pattern does not extend to the active region, to meet the claim limitation. In addition to the reasons to combine Lee and Yasushige discussed above in Section VII.A, for a dummy pattern that serves as the "step" for forming an etch stop layer to protect the edge of the field oxide layer, as discussed in Lee, positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole formation process. A POSITA would have been motivated to combine Lee with Yasushige's teaching to ***not*** form the dummy pattern extending into the active region, so that there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes. The semiconductor

industry is constantly focused on developing smaller dimensions, and it would be beneficial to actively avoid forming nonfunctional dummy patterns onto an active region. Accordingly, Lee in view of Yasushige renders this limitation obvious.

[1g] "and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;"

102. Lee discloses and makes obvious that "the second patterned conductive layer is a dummy pattern." Lee contemplates in one embodiment illustrated in Fig. 4 that the etch stop layer may be formed as a spacer along an "internal connection line passing adjacently" ***or*** a "dummy pattern":



Lee at (annotated) Fig. 4, 17-6. As shown in Fig. 4 at 44-3, the dummy pattern has identical structure to the first patterned conductive layer on the active region. One of skill in the art would know as a matter of design choice that the dummy "pattern" is formed from depositing the same materials, gate oxide layer, poly, and gate cap layers in a sequence and patterning, as disclosed by Lee. *Id.* at 17-2. The

term "pattern" also conveys to one of skill in the art that the dummy pattern was formed in the same masking process as the first patterned conductive layer. Accordingly, the dummy pattern is also a "conductive layer," as it is made of the same conductive poly material as the first patterned conductive layer.

103. Lee discloses that the dummy pattern is "electrically isolated from the substrate and circuits thereon." First, as disclosed in element 1[f], the dummy pattern does not extend over the active region of the substrate. It is thus electrically isolated over the field oxide layer, similar to the disclosure of "electrically isolated" in the '902 patent. *See* '902 patent at 5:43-45 ("the second patterned conductive layer is preferably electrically isolated over the field region").

104. In addition, Lee explicitly contemplates two embodiments—one where the conductive pattern is an "internal connection line" and the other where the conductive pattern is a "dummy pattern." Lee's contemplation of alternative embodiments where one has connections is further confirmation to a POSITA that the dummy pattern embodiment does not have electrical connections. For example, Lee teaches that where an internal connection line is not conveniently located to form the etch stop layer on the field oxide layer, a dummy pattern may be created to serve this mechanical function. While other mechanical structures are possible, forming a gate pattern is most efficient given the already existing patterning process for gates throughout the chip. And where a dummy pattern was

created for the purpose of serving as a step for forming the etch stop layer, a POSITA would know that keeping the mechanical structure electrically isolated is the best and most efficient practice to prevent accidental electrical connections or shorting damage.

105. One of skill in the art would understand that a dummy pattern is a gate pattern that performs no electrical function, as confirmed by contemporary electrical engineering and microelectronics dictionaries for the term "dummy"[4]:

> "dummy": "Pertaining to a nonfunctioning item used to satisfy some format or logic requirement or to fulfill prescribed conditions."[5]
> "dummy connector plug": "A part included in the total design of a connector to mate with a connector but not to perform an electrical

[4] Nowak (Ex. 1110) also provides background on dummy conductors and their electrical isolation: "[T]he integrated circuit further includes dummy conductors on the insulating layers in the spaces between the signal conductors. ***These dummy conductors are open circuited, and thus they carry no signals.*** Their function is purely mechanical; and specifically, they function to partially fill the spaces between the signal conductors such that an overlying insulating layer can be formed without peaks and valleys. 2:13-22.

[5] Ex. 1114, IEEE Standard Dictionary of Electrical and Electronics Terms at 322, 6th ed.

function."[6]

As recognized in the '902 patent, an electrically isolated conductive pattern serves no electrical function. '902 patent at 6:20-23 ("the patterned conductive layer on the field region, however, can be electrically isolated thus serving no electrical function in the completed integrated circuit device"). Thus, Lee discloses forming a dummy pattern, on an isolation layer, which is electrically isolated from the substrate and circuits.

106. However, to the extent that this limitation "the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon" is not explicitly disclosed in Lee, this limitation is obvious based on Lee in view of Yasushige. Yasushige explicitly discloses a dummy pattern that is "electrically isolated." Yasushige at 29, 41. A POSITA would have combined the teaching in Lee of a dummy pattern used as an etch inhibiting layer, with the explicit disclosure in Yasushige that such a dummy pattern used as an etch inhibiting layer is electrically isolated, to meet the claim limitation "wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon."

107. A POSITA would have been motivated to combine the teaching of a

[6] Ex. 1113, The Electronic Packaging, Microelectronics, and Interconnection Dictionary, 1993.

dummy pattern in Lee with the teaching in Yasushige that the dummy pattern is electrically isolated from the substrate and circuits, for the reasons stated in Section VII.A. In addition, Lee and Yasuhige disclose similar structure and positioning of the dummy pattern, indicating a shared intent to electrically isolate the dummy pattern from the substrate and circuits. Both Lee and Yasushige disclose that the etch stopper was formed ***on*** a field oxide layer and ***around*** the active region. *See* Lee at 17-5 ("an etch stop layer . . . is formed around the impurity region"); Yasushige ("a conductive film 7d . . . is formed around the base region of the bipolar transistor").

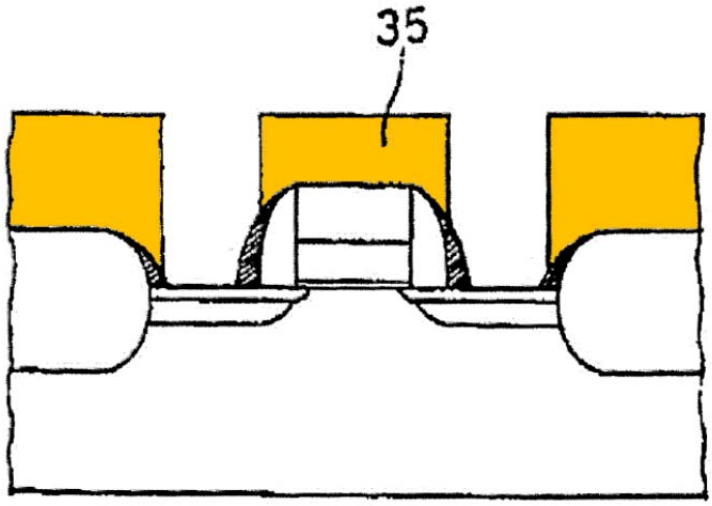
108. Further, A POSITA would have recognized that Yasushige's teaching of electrically isolating the dummy pattern on a field oxide layer would improve the functionality of Lee's disclosure of the dummy pattern and etch stop layer along its sidewall. First, positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole formation process. By not positioning the dummy pattern on the active region itself, there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes. Second, keeping the dummy pattern electrically isolated ensures that the dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern.

A POSITA would have recognized these benefits of Yasushige's teaching of electrical isolation of the dummy pattern on the field oxide layer, and applied those teachings to Lee.

109. Thus, given the identical disclosure of function, structure, and positioning on an isolation layer around an active region, of the dummy pattern, a POSITA would have either understood that the disclosure of a dummy pattern in Lee comprises a dummy pattern that is electrically isolated from the substrate and circuits, as explicitly disclosed in Yasushige, or would have been highly motivated to design the dummy pattern in Lee so that it was electrically isolated from the substrate and circuits, as disclosed in Yasushige.

[1h] "forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer;"

110. Lee discloses that "a contact hole is formed by depositing an interlayer insulation film (**35**) and etching the interlayer insulation film," as shown in annotated Fig. 3(c):

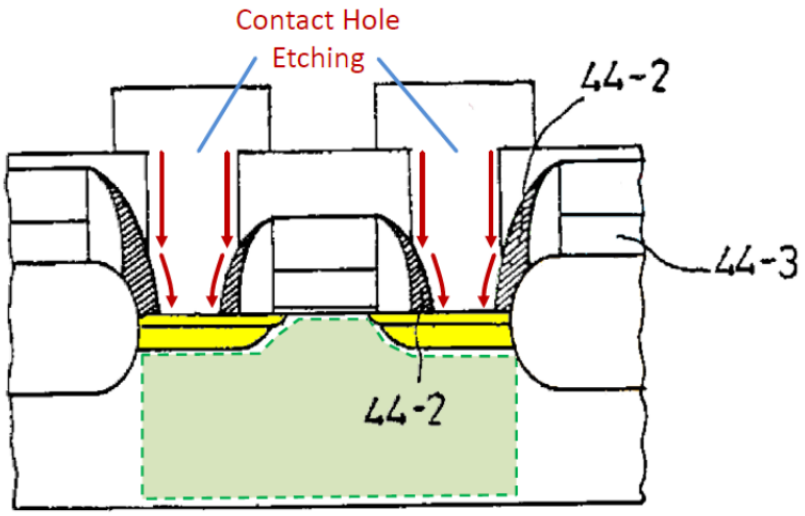


Lee at Fig. 3(c) (annotated), 17-6. Lee further discloses that the interlayer insulating film is deposited "on the following transistor." *Id.* at 17-2. As further shown in Fig. 4, the interlayer insulating film is also formed on the etch stop layer and dummy pattern, and the field isolation layer. My opinion does not change under Samsung's construction proffered in district court for this limitation.

[1i] "forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer."

111. Lee discloses that "a contact hole that ***opens the source and drain region*** is formed by depositing an interlayer insulation film (15) on the following transistor and etching the interlayer insulation film." Lee at 17-2. Lee thus discloses that the contact hole exposes a portion of said active region. As further shown in annotated Fig. 4, the contact hole is formed between the first patterned conductive layer on the active region (yellow source/drain region on green active

region) and the etch inhibiting layer, comprising the etch stop layer and dummy pattern:



Lee at Fig. 4.

112. Therefore, for the reasons set forth above, I find that all elements of claim 1 are rendered obvious by Lee in combination with Yasushige.

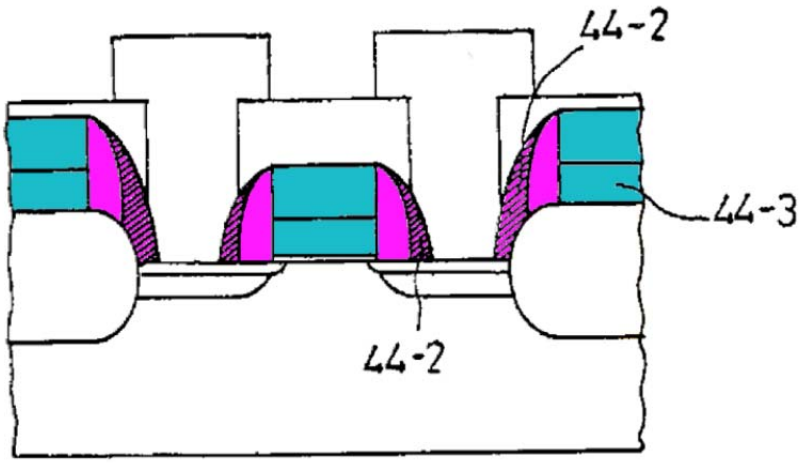
B. Claim 3

"A method according to claim 1 wherein said first patterned conductive layer comprises a conductive portion and insulating spacers along sidewalls thereof."

113. As discussed in Claim 1(c), Lee discloses a first patterned conductive layer formed on an active region and a conductive portion comprising a "poly" layer. Lee further discloses "forming a gate sidewall (34-1) using a deposition and etch-back process," which meets the limitation of a spacer, and as shown in Fig. 3(a) is formed along the sidewall of the first patterned conductive layer. Lee

further discloses that the gate sidewall is an "oxide layer." Lee at 17-6 (". . . oxide layers on the substrate (field oxide layer, ***gate sidewall***, cap oxide layer . . .)"). A POSITA understands that an oxide layer is an insulating material.

114. Lee further discloses forming an etch stop layer **44-2** on the first patterned conductive layer, as shown in annotated Fig. 4:



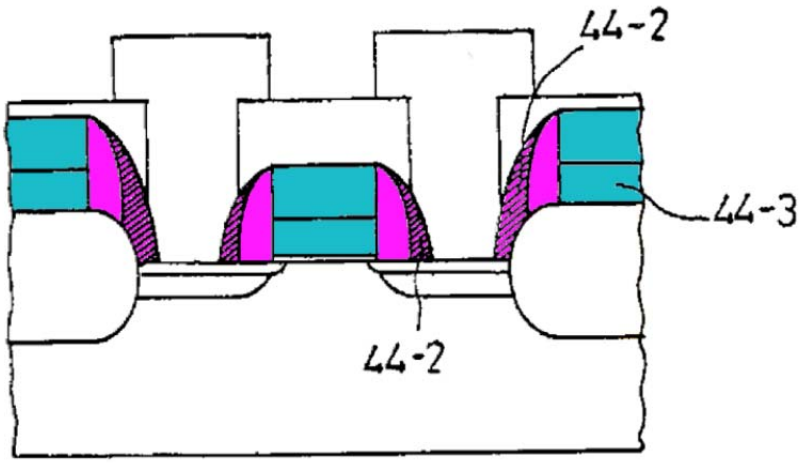
As discussed in Claim 1(e), etch stop layer 44-2 on the second patterned conductive layer is an insulating spacer along a sidewall, and for the same reasons the etch stop layer 44-2 on the first patterned conductive layer is an insulating spacer along a sidewall. As shown in annotated Fig. 4, the etch stop layers 44-2 are labeled identically, and appear identical.

C. Claim 4

"A method according to claim 3 wherein said steps of forming said etch inhibiting layer and forming said patterned conductive layer are performed simultaneously."

115. As discussed in Claim 1(c), Lee discloses forming a first patterned

conductive layer.[7] As discussed in Claim 1(e), Lee further discloses forming an etch inhibiting layer, comprising a second patterned conductive layer and an etch stop layer formed next to a gate sidewall of the second patterned conductive layer. Lee discloses that the second patterned conductive layer is a "dummy pattern," and as shown in annotated Fig. 4, is identical to the first patterned conductive layer:



Lee at 17-6, Fig. 4. Lee discloses that a MOS gate is "formed by depositing gate oxide layer, poly and gate caps in this sequence and then etching them." This is a

[7] The claim refers to "said patterned conductive layer" but does not specify "first" or "second" patterned conductive layer. I assume for my analysis that the claim refers to the "first" patterned conductive layer. Also, the "etch inhibiting layer" is defined to include both a patterned conductive layer and spacers, whereas the "said patterned conductive layer" does not include spacers. I assume for my analysis the claim includes the spacers.

well-known process for patterning a MOS gate, and a POSITA would know that the first conductive layer and the second conductive layer, called a "dummy pattern," are formed and patterned simultaneously. Patterning gates that are identical, as the two in Fig. 4 are, simultaneously is a well-known design choice and indeed is the only design choice that would be practical from a manufacturing standpoint. A semiconductor has thousands of gates formed on the substrate. Chip designers create masks that provide a pattern to deposit all gates at the same level simultaneously. Compared to forming gates in different processes, forming gates simultaneously saves substantially on cost, time, and complexity.

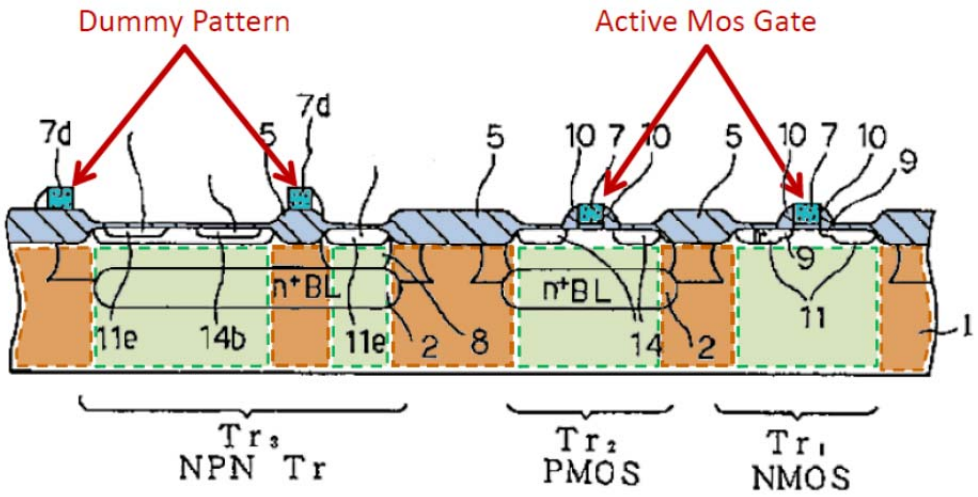
116. Lee also shows in Fig. 4 the formation of etch stop layers 44-2 and 44-3 on the first and second patterned conductive layers, through a "deposition and etch-back process." *See* Lee at 17-6. The gate sidewalls (*see* Fig. 3(a) at 34-1) are also formed through a "deposition and etch-back process." *Id.* at 17-5. A POSITA would understand that this deposition and etch-back process happens simultaneously to be efficient. As shown in Fig. 4, the first and second patterned conductive layers have the same number and appearance of spacers. Performing the deposition and etch-back process for all gates on the same level simultaneously is the only feasible design choice and known for semiconductor fabrication.

117. Thus, to the extent Lee does not explicitly disclose forming the etch inhibiting layer and first patterned conductive layer simultaneously, Lee strongly

suggests this obvious limitation to a POSITA.

118. In the alternative, to the extent Lee does not explicitly disclose or make obvious this limitation, this limitation is obvious based on Lee in view of Yasushige. Yasushige explicitly discloses that a dummy pattern is formed on a field oxide layer "simultaneously with the gate electrode of the MOS transistor." Yasushige at 31.

119. Like Lee, Yasushige uses dummy patterns to solve the problem of a mis-alignment in an etching process resulting in over-etching and causing damage to a base region surface. Yasushige at 50. Yasushige discloses that the dummy pattern **7d** is "identical to the gate electrode **7** of the MOS transistor." Yasushige at 41. The dummy pattern is "formed around the base region **14b** of the bipolar transistor Tr3":



Id. at Fig. 1 (annotated). Yasushige discloses that the dummy pattern is formed on a field oxide layer "***simultaneously*** with the gate electrode of the MOS transistor."

Yasushige at 31.

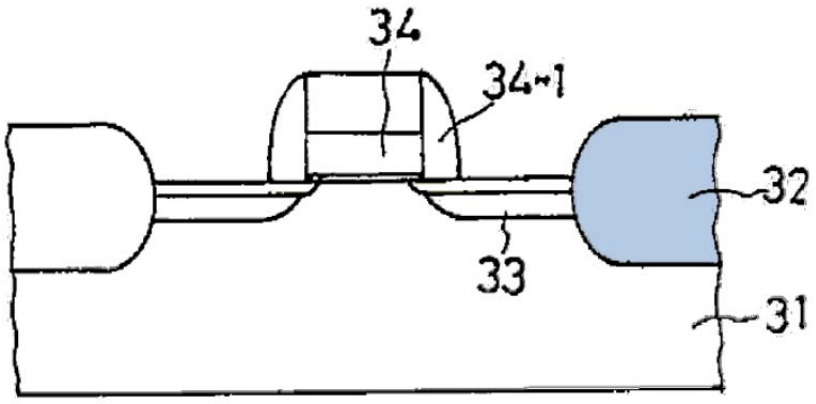
120. A POSITA would have been motivated to combine the teaching of a dummy pattern in Lee with the teaching in Yasushige that the dummy pattern is formed simultaneously with the MOS transistor. In addition to the reasons discussed in section VII.A., both Lee and Yasushige disclose the use of a dummy pattern as an etch stopper, in order to prevent the etch process from damaging the field oxide layer and resulting in leakage of current. Lee at 17-2, Fig. 1(b); Yasushige at 50, 53. Both Lee and Yasushige also disclose an additional active MOS gate that is identical to the dummy pattern. Lee at 17-5 ("MOS gate is formed"); *id.* at Fig. 4; Yasushige at 41 ("a conductive film 7d identical to the gate electrode 7 of the MOS transistor is formed . . . and this conductive film 7d is electrically separated from the base region"). Thus, given the similarity in use of a dummy pattern as an etch stop, to complement the function of a MOS transistor identical to the dummy pattern, a POSITA would have been strongly motivated to look to Yasushige's manufacturing process to simultaneously form a first patterned conductive layer and a dummy pattern.

D. Claim 5

"A method according to claim 1 wherein said field isolation layer comprises oxide."

121. Lee discloses "an active region is isolated electrically from the surrounding active regions by ***forming a field oxide layer*** (32) on a semiconductor

substrate (31)" as shown in Fig. 3(a):

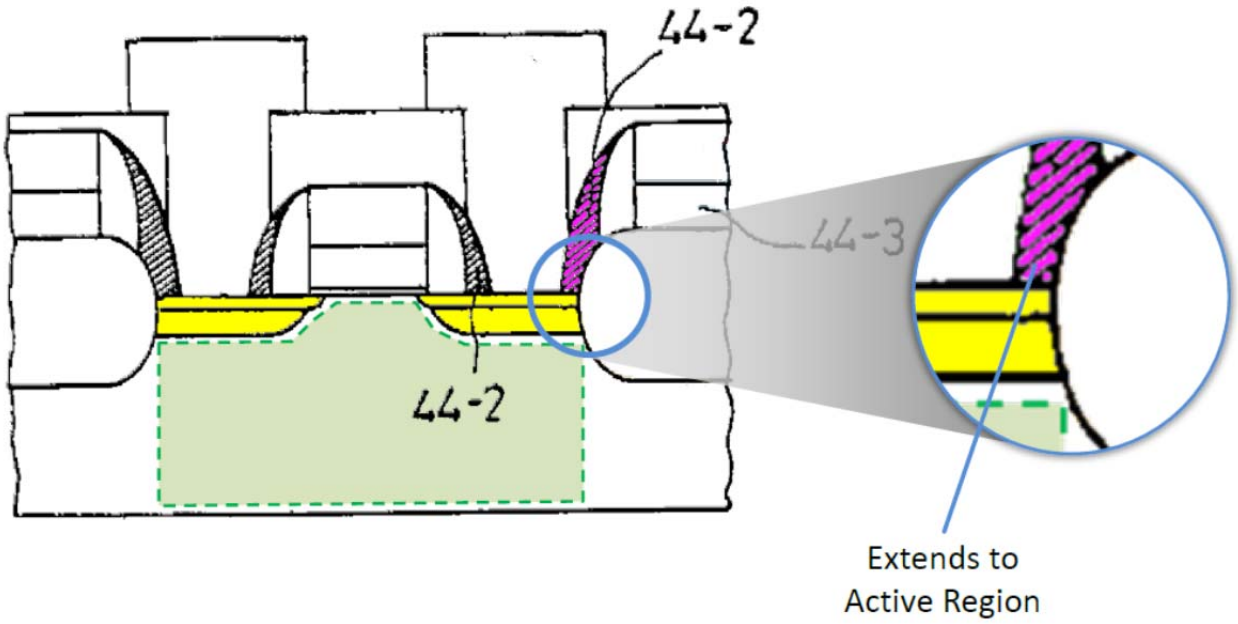


Lee at 17-5, Fig. 3(a) (annotated). Lee's disclosure of a "field oxide layer" that isolates the active region is a field isolation layer comprising oxide.

E. Claim 7

"A method according to claim 1 wherein the insulating spacer of the etch inhibiting layer extends to the active region of the substrate."

122. As discussed in Claim 1(e) Lee's disclosure of forming an etch stop layer **44-2** as an insulating spacer along the second patterned conductive layer (**44-3**) meets the limitation "insulating spacer of the etch inhibiting layer." As shown in annotated Fig. 4, Lee discloses forming the etch stop layer 44-2 extending to the active region (highlighted yellow) of the substrate:



The etch stop layer 44-2 is formed partially on the field oxide layer and partially on the active region, so that it can protect the field oxide layer from damage when etching a contact hole to expose the active region. Lee at 17-2, 17-5, 17-6.

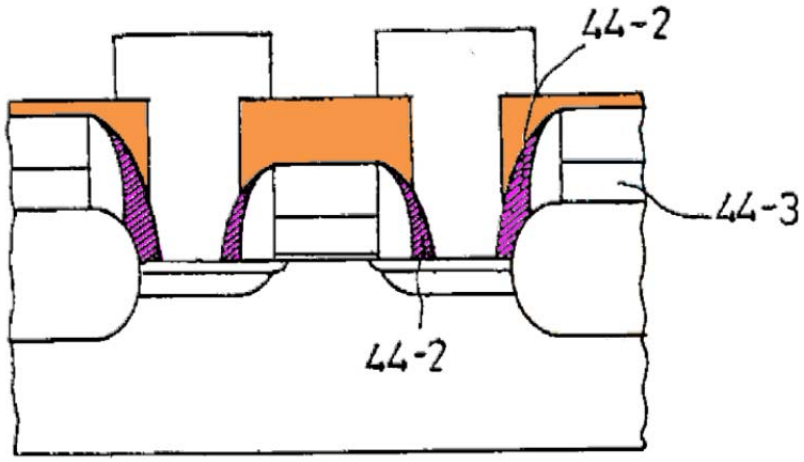
F. Claim 8

"A method according to claim 1 wherein the insulating spacer and the insulating layer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer."

123. Lee discloses that the insulating spacer, or the etch stop layer, comprises a different material than the insulating layer, or interlayer insulation film, so that the insulating layer can be etched selectively with respect to the insulating spacer.

124. Lee discloses "a step of forming an etch stop layer around said source

and drain region by depositing a ***material having a high etch selectivity with an interlayer insulation film***." Lee at 17-4. As discussed in Claim 1(e), Lee further discloses that the etch stop layer can be formed as an insulating spacer along the sidewall of a dummy pattern:



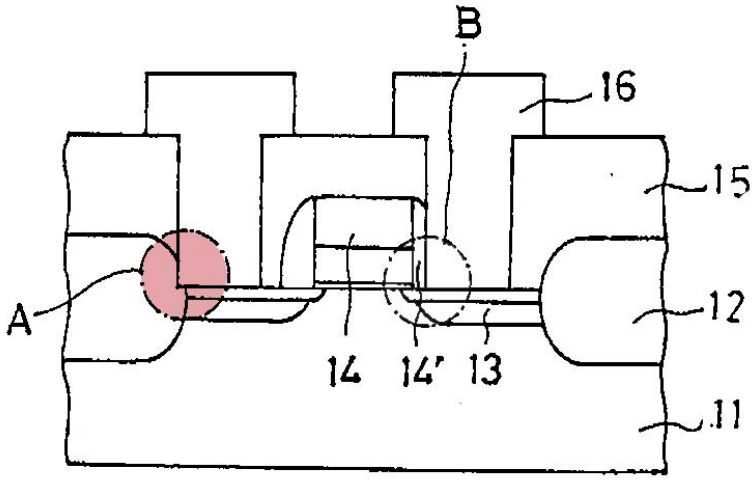
Id. at Fig. 4 (annotated), 17-6. Accordingly, Lee discloses that the insulating spacer comprises a different material than the insulating layer, so that the insulating layer can be etched selectively with respect to the insulating spacer.

G. Claim 9

> **"A method according to claim 1 wherein contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer."**

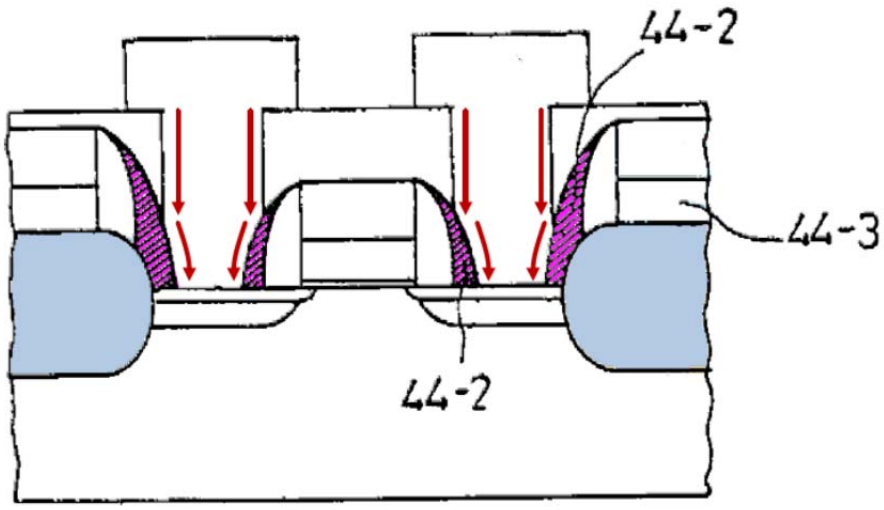
125. Lee discusses the problem of misalignment when forming a contact hole, where the contact hole is formed over the field isolation layer and damages

the field isolation layer (shown below in Fig. 1(b) circled and labeled "A") causing junction leakage:



Lee at Fig. 1(b), 17-2.

126. Lee discloses forming an etch stop layer to solve this problem, and discloses forming an etch stop layer on a dummy pattern formed over a field isolation layer:



Lee at Fig. 4 (annotated), 17-6. As discussed in Claim 8, the etch stop layer 44-2 is

formed with a "material having a high etch selectivity with an interlayer insulation film," so that an etching process can etch a contact hole through the interlayer insulation film without etching the etch stop layer. As shown in Fig. 4, the formation of the contact hole exposes a portion of the etch stop layer without exposing the field isolation layer. While Fig. 4 does not illustrate the contact hole formed directly over the field isolation layer, it is shown on the edge of the field isolation layer and Lee discloses that "since the heavily stressed site is protected by the etch stop layer, the area in which junction leakage can happen can be protected from the etching process." Lee at 17-7. Thus a POSITA would know that if the contact hole were formed slightly more misaligned, the end result would be the same—the contact hole would expose the etch stop layer without etching it, and the contact hole would not expose the field oxide layer.

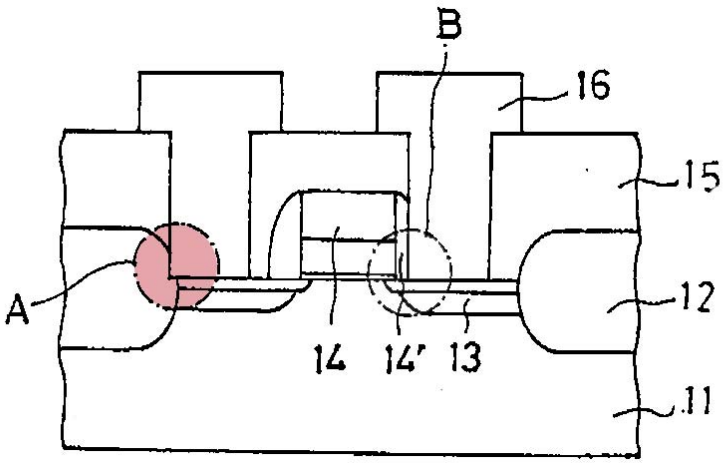
127. Lee further discloses that the invention "relates to the structure of a semiconductor device in which ***a process alignment margin is secured*** when forming a contact hole by forming an etch stop layer on the contact hole area to ***protect the lower insulation layer***." Lee at 17-4. Thus a POSITA would understand that a contact hole formed over the field isolation layer (referred to in 17-4 as a "lower insulation layer") would expose the etch stop layer without exposing the field isolation layer. Further, given Lee's disclosure that "a process alignment margin is secured," (Lee at 17-4) a POSITA would understand that Lee

discloses an invention to increase the area over which the contact hole can be formed without damaging the field isolation layer.

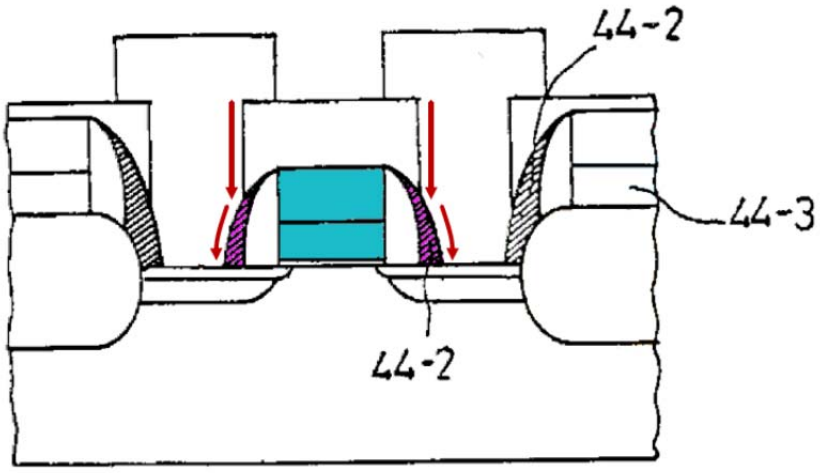
H. Claim 10

"A method according to claim 1 wherein at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer."

128. Lee discloses that a problem with forming contact holes is the possibility of damage to a field oxide layer, or a first patterned conductive layer on an active region:



Lee at Fig. 1(b) (annotated), 17-2. Lee discloses that "when a mis-alignment occurs, **the gate sidewall ('14) is damaged as shown in the area B** or the field oxide layer that separates an active region is also damaged **(area A of the drawing)** and thus, it becomes the cause of junction leakage." In order to protect these two areas, an etch stop layer **(44-2)** is formed along the sidewalls of both a first patterned conductive layer and a dummy pattern:



Lee at Fig. 4. As shown in Fig. 4, the bottom portion of the contact hole is self-aligned with respect to both the first patterned conductive layer and the etch inhibiting layer, or etch stop layer on the dummy pattern.

129. Lee further discloses that the present invention "relates to the structure of a semiconductor device in which a ***process alignment margin is secured*** when forming a contact hole." Lee at 17-4; *see also id.* at 17-7 ("an alignment margin can be secured easily at contact photographing"). A POSITA would understand that disclosure of securing a process alignment margin, coupled with the illustration in Fig. 4 of a contact hole aligning with the etch stop layers **(44-2)** on both the first conductive pattern and the dummy pattern, satisfies this limitation.

I. Claim 12

[12pre] A method for forming a microelectronic structure, said method comprising the steps of:

130. Lee discloses "[a] method for forming a microelectronic structure." *See* Lee at 17-1 ("The present invention relates to a method for fabricating a semiconductor device").

[12a] defining adjacent active and field regions on a substrate, and circuits thereon;

131. Lee discloses limitation [12a] of claim 12 for the reasons set forth above as to limitation [1a] of claim 1.[8]

12[b] forming a field isolation layer which covers said field region;

132. Lee discloses limitation [12b] of claim 12 for the reasons set forth above as to limitation [1b] of claim 1. The only distinction is the claiming of a field isolation layer "which covers" said field region, rather than "on" said field region. As discussed in limitation [1b], the disclosure in Lee also shows forming a field isolation layer which covers said field region.

12[c] forming a first patterned layer on said active region of said substrate spaced apart from said field region;

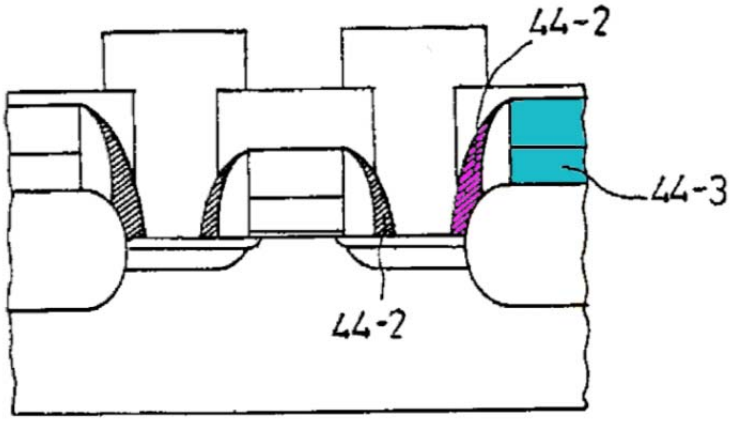
133. Lee discloses limitation [12c] of claim 12 for the reasons set forth above as to limitation [1c] of claim 1.

12[d] forming a second patterned layer on said field

[8] I cite back to a previous limitation where the language is identical or only different in a non-material way such that my analysis applies equally.

isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;

134. Lee in combination with Yasushige renders obvious the limitation [12d] of claim 12 for the reasons set forth above as to limitation [1d, 1e, 1f, and 1g] of claim 1. The only distinction is the claiming of a "second patterned layer" instead of an "etch inhibiting layer." But as discussed in limitation [1e], Lee in combination with Yasushige renders obvious the limitation of a second patterned layer by Lee's disclosure of the dummy pattern, (Fig. 4, 17-6) which comprises a patterned conductive layer and an etch stop layer formed along the spacer of the patterned conductive layer:



12[e] forming an insulating layer covering said substrate,

said field isolation layer, and said first and second patterned layers; and

135. Lee discloses limitation [12e] of claim 12 for the reasons set forth above as to limitation [1h] of claim 1. The only distinction is the claiming of an insulating layer "covering" said substrate, rather than "on" said substrate. As discussed in limitation [1h], the disclosure in Lee also shows an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers.

12[f] forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;

136. Lee discloses limitation [12f] of claim 12 for the reasons set forth above as to limitation [1i] of claim 1. The only distinction is the claiming of a portion of said active region between said "first and second patterned layers," rather than an "etch inhibiting layer and said first patterned conductive layer" as claimed in limitation [1i] of claim 1. As discussed in limitation [1i] of claim 1, the disclosure in Lee also shows forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers, because the etch inhibiting layer is also a second patterned layer.

J. Claim 11:

137. Claim 11 contains the limitations of claim 12, with one additional

limitation added. Lee in combination with Yasushige discloses the limitations of claim 11 that also appear in claim 12, for the reasons set forth as to claim 12.

> **11[g] wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.**

138. Lee discloses limitation [11g] of claim 11 for the reasons set forth above as to claim 4. The only distinction is the claiming of forming first and second patterned layers simultaneously, rather than a patterned layer and an etch inhibiting layer as claimed in claim 4. As discussed in claim 4, the disclosure in Lee also shows forming a first patterned layer and second patterned layer simultaneously, because the etch inhibiting layer is also a second patterned layer.

K. Claim 14

> **A method according to claim 12 wherein the insulating layer and the insulating spacer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.**

139. Lee in combination with Yasushige renders obvious claim 14 for the reasons set forth above as to claim 8.

L. Claim 15

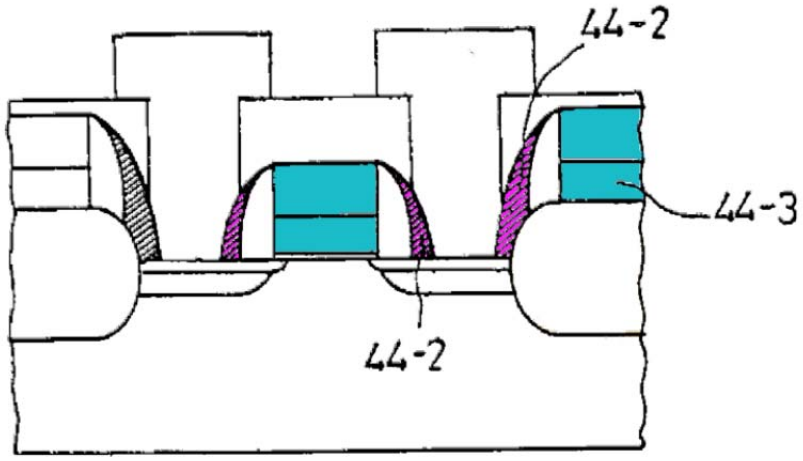
140. Claim 15 contains the limitations of claim 12, with one limitation added. Lee in combination with Yasushige discloses the limitations of claim 15 that also appear in claim 12, for the reasons set forth as to claim 12.

> **15[g] wherein each of said first and second patterned layers**

comprises insulating spacers along sidewalls thereof.

141. Lee discloses wherein the second patterned layer comprises insulating spacers along sidewalls for the reasons set forth above as to limitation [1e] of claim 1.

142. Lee further discloses said first patterned layer comprises insulating spacers along sidewalls thereof. The etch stop layer **44-2** is formed as a spacer along sidewalls of the first and second patterned conductive layers (colored blue), as shown in annotated Fig. 4:



The etch stop layer 44-2 is formed with a "non-conductive material," and is thus an insulating layer. *Id.* at 17-6.

143. The etch stop layer 44-2 is identical in structure to the insulating spacer formed along a sidewall of the patterned conductive layer 44-3, and is formed along side the insulating spacer. Lee discloses that the etch stop layer (44-2) is formed in the "form of a sidewall" and using the same process for making a

sidewall:

> At this time, the etch stop layer is formed with conductive or non-conductive material, and it is formed ***in the form of a sidewall*** through a ***deposition and etch-back process*** using the step area formed on the lower layer without any additional mask.

Lee at 17-6. The deposition and etch-back process is the same process for making an insulating sidewall spacer disclosed by Lee. *Id.* at 17-5 ("forming a gate sidewall (34-1) using a deposition and etch-back process"). In Fig. 4, Lee illustrates the etch stop layer 44-2, and it has similar structure to the insulating spacer formed onto the conductive patterned layer.

144. Thus Lee in combination with Yasushige renders obvious claim 15.

M. Claim 16

> **A method according to claim 15 wherein said insulating layer can be selectively etched with respect to said insulating spacers.**

145. Lee in combination with Yasushige renders obvious claim 16 for the reasons set forth above as to claim 8.

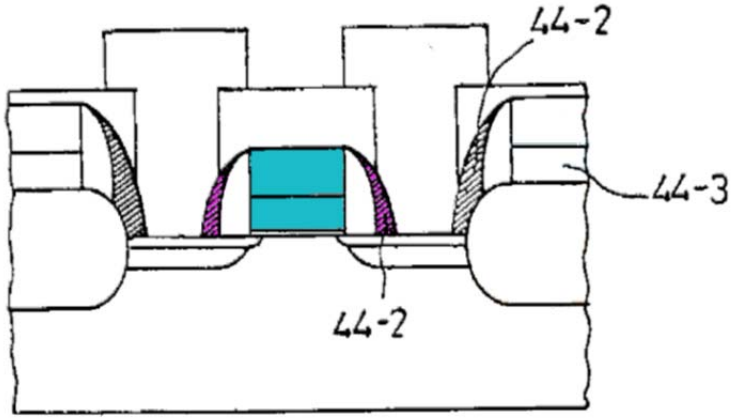
N. Claim 18

146. Claim 18 contains the limitations of claim 12, with one limitation added. Lee in combination with Yasushige discloses the limitations of claim 18 that also appear in claim 12, for the reasons set forth as to claim 12.

> **18[g] wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a**

sidewall thereof.

147. Lee discloses that a "MOS gate **(14)** is formed by depositing ***gate oxide layer***, poly and gate caps in this sequence and then ***etching them***." Lee at 17-2; *see also* annotated Fig. 4:



A POSITA would understand that depositing a sequence of layers and then etching the layers to form a MOS gate is a patterning process to create a patterned gate layer.

148. Lee discloses an insulating gate spacer along a sidewall for the reasons set forth above as to claim 3.

149. Thus Lee in combination with Yasushige renders obvious claim 18.

XI. SECOND GROUND OF INVALIDITY – OBVIOUSNESS BY LEE IN COMBINATION WITH YASUSHIGE AND NOWAK

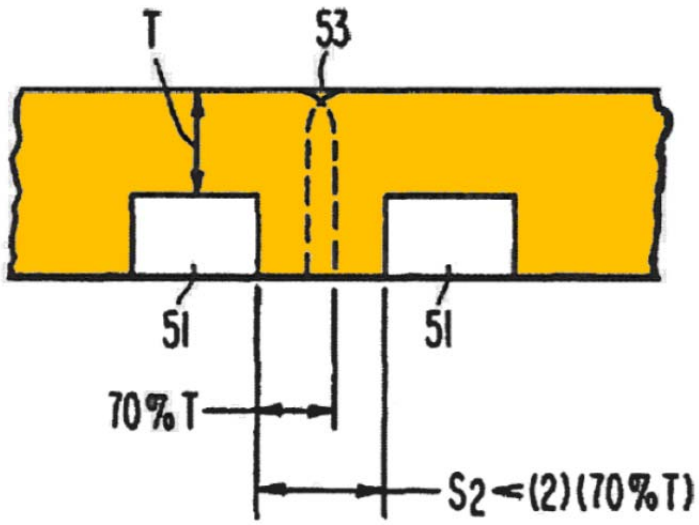
A. Claim 2

"A method according to claim 1 wherein said insulating layer comprises nitride."

150. As discussed in Claim 1[h], Lee discloses forming an insulating layer.

Lee discloses that "a contact hole is formed by depositing an interlayer insulation film and etching the interlayer insulation film." Lee at 17-6. While Lee does not explicitly disclose that the insulating layer comprises nitride, this limitation is obvious based on Lee in view of Nowak. As disclosed by Lee, the insulation film is an insulating material, of which one well-known group of materials is nitride, among just a few others including oxides and spin-on polymers. Lee discloses that the etch stop layer may comprise a material that has "high etch selectivity with an interlayer insulation film." Lee at 17-5. Lee further discloses "oxide layers on the substrate (field oxide layer, ***gate sidewall***, []) as mask," (*id.* at 17-6) and that the etch stop layer may be formed "in the form of a sidewall." *Id.* at 17-5. Where the etch stop layer is also an oxide layer, a POSITA would have been motivated to use another material with high etch selectivity as the interlayer insulation film, and looked to other references such as Nowak which provide details on the materials in insulating layers.

151. Nowak explicitly discloses forming a dummy conductor gate on a substrate and depositing "a conformal layer of insulating material, such as SiO2 or ***Si3N4 or oxynitride*** . . . to cover the dummy conductors." Nowak at 3:61-4:4; *see also id.* at annotated Fig. 5B:



Thus while Nowak confirms that several materials may be used for the insulating layer, Nowak explicitly discloses that the insulating layer comprises Si3N4, which is silicon nitride, or oxynitride. Both of these materials are well-known nitrides used to form insulating layers on a semiconductor substrate.

152. A POSITA would have been motivated to combine the disclosure of an interlayer insulation film in Lee with the disclosure in Nowak that the insulating layer can be silicon nitride or oxynitride. Like Lee, Nowak describes the formation of electrically isolated dummy conductors on a substrate. Lee at 17-6; Nowak at 2:17-18 ("dummy conductors are open circuited, and thus they carry no signals."). Like Lee, Nowak further describes forming contact holes next to the dummy conductors through insulating layers. Lee at 17-6; Nowak at 2:5-13 (". . . a plurality of insulating layers over the top surface which are interleaved with respective sets of signal conductors. These signal conductors are spaced apart on

the insulating layers and are routed through holes in the insulating layers."). Lee and Nowak both discuss forming contact holes through an insulating layer, and while Lee does not disclose the well-known technique of forming an insulating layer from a nitride, a POSITA would have been motivated to look to Nowak for details on the material composition of an insulating layer with similar function and structure as the insulating layer in Lee. Further, the disclosure in Lee motivates a POSITA to try different materials that will result in high etch selectivity between the insulating layer and spacers on a gate. Additional motivations to combine are discussed in section VII.B.

153. Accordingly Nowak discloses the limitations of this claim, and because claim 2 is dependent on claim 1, the combination of Lee, Yasushige, and Nowak renders this claim obvious.

B. Claim 17

A method according to claim 16 wherein said insulating layer comprises nitride.

154. Lee in combination with Yasushige and Nowak renders obvious claim 17 for the reasons set forth above as to claim 2.

XII. THIRD GROUND OF INVALIDITY - – OBVIOUSNESS BY LEE IN COMBINATION WITH YASUSHIGE AND THE '524 PATENT

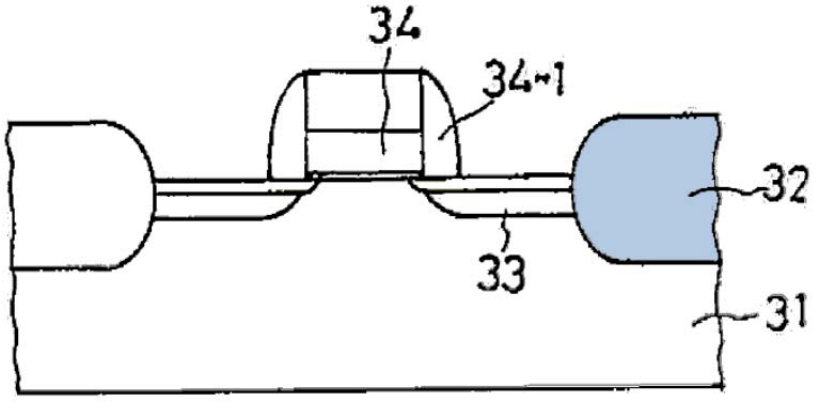
A. Claim 6

"A method according to claim 1 wherein said step of defining said field and active regions comprises the step of

forming a trench in said substrate, and wherein said field isolation layer fills said trench."

155. This limitation is obvious based on Lee in combination with the '524 Patent.

156. Lee discloses forming a field oxide layer:



Lee at Fig. 3(a) (annotated). Lee discloses "an active region is isolated electrically from the surrounding active regions by ***forming a field oxide layer*** (32) on a semiconductor substrate (31)." Lee at 17-5. While Lee does not explicitly use the word "trench," a POSITA would know that forming a trench in the substrate that is filled by a field isolation layer is common practice in the industry, and an obvious design choice.

157. The '524 Patent discloses using "trenches for inter-device isolation." '524 Patent at 1:9. Traditionally, "trench isolation involves etching a narrow, deep trench or groove in a silicon substrate and then filling the trench with a filler material such as a silicon oxide or polysilicon." *Id.* at 1:24-25. The '524 Patent

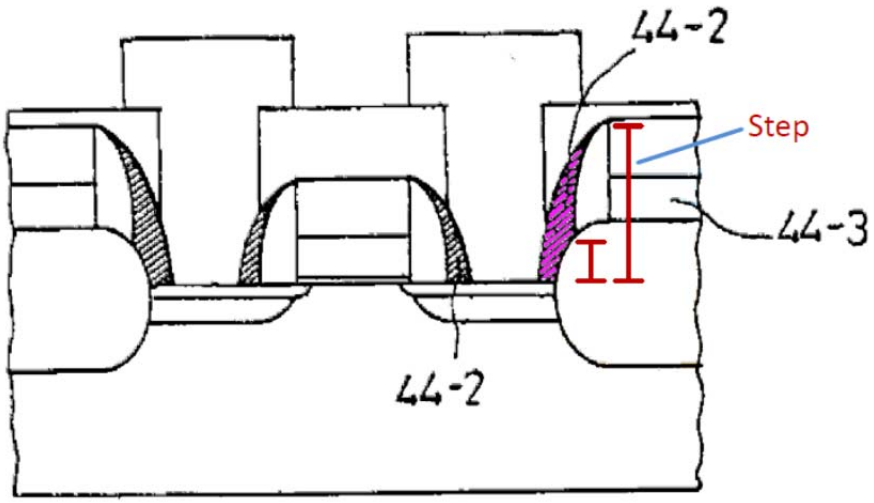
discloses both a "narrow trench" and a "wide trench." *Id.* at 2:60-61, Figs. 7-9. It further discloses at least one specific etching recipe for forming a trench. *Id.* at 3:30-38. Then, the '524 Patent discloses filling in the trench with multiple layers, "an exemplary candidate for filler layer 25 is an oxide." *Id.* at 4:28-29.

158. The '524 Patent issued six years prior to the filing of the parent application of the '902 Patent, and discusses an improvement on trench isolation technology. '524 Patent at 1:24-25. The '524 Patent shows that trench isolation was well known years before the filing date of the '902 Patent. The '524 Patent notes the limitations of conventional means of growing a field oxide layer, including the "birds beaks and other formations" which cause "undesirable encroachments" into device areas. '524 Patent at 1:20-23. In contrast, a trench isolation process has advantages of consuming less space than conventional methods of forming field oxide layers. *Id.* at 1:35-38.

159. A POSITA would have been motivated to combine Lee with the '524 Patent to form trench isolation layers. For example, the main purpose of Lee was to prevent damage to the field oxide layer during formation of a contact hole. Lee at 17-2. A POSITA would recognize that a method, such as the LOCOS method, would create a bird's beak which encroaches into the active regions and decrease the room for error in forming a contact hole. In contrast, the trench isolation process creates field oxide layers with a "narrow, deep trench" which generally

"consume less space" and accordingly helps solve the problem of contact hole misalignment into the field oxide layer, recognized by Lee. *Id.* at 1:27-28.

160. Lee also contemplates that the field oxide layer may be a trench, which are typically less protruded from the surface, in its teaching of forming the etch stop layer. While the '524 Patent teaches that a trench isolation layer "protrude somewhat beyond upper surface of the silicon wafer," Lee specifically contemplates that the "step" of the field oxide layer may not be "sufficient" and so the "step of a dummy pattern" is used to form the etch stop layer:



Lee at Fig. 4 (annotated), 17-6. Thus, where the protrusion of the trench isolation layer in the '524 Patent is not sufficient a "step," Lee addresses that issue by providing the dummy pattern **44-3** to form etch stop layer **44-2** along the sidewall.

161. Accordingly Lee and the '524 Patent disclose the limitations of this claim, and because claim 6 is dependent on claim 1, the combination of Lee,

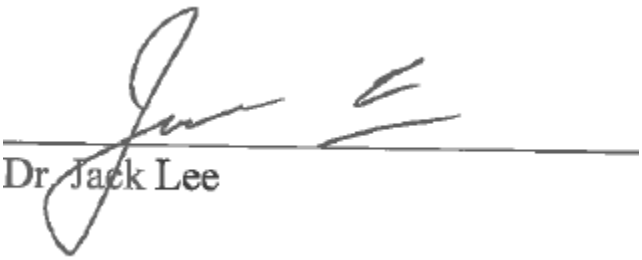
Yasushige, and the ’524 Patent renders this claim obvious. My opinion does not change under Samsung’s narrower construction proffered in district court for this limitation.

B. Claim 13

A method according to claim 12 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.

162. Lee in combination with Yasushige and the ‘524 Patent renders obvious claim 13 for the reasons set forth above as to claim 6.

Executed on June 2, 2015, in Austin, TX.



Dr. Jack Lee