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Filed on behalf of: Samsung Electronics Company, Ltd.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION
Petitioner

v.

SAMSUNG ELECTRONICS COMPANY, LTD.
Patent Owner

Case IPR2015-01327
Patent No. 6,287,902

Patent Owner's Response

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LIST OF EXHIBITS

Exhibit No.	Description	Previously Submitted
2001	Memorandum Opinion in *Samsung Electronics Co., Ltd. et al. v. NVIDIA Corp. et al*., 3:14-cv-00757-REP (E.D. Va. July 30, 2015)	X
2002	Order in *Samsung Electronics Co., Ltd. et al. v. NVIDIA Corp. et al*., 3:14-cv-00757-REP (E.D. Va. July 30, 2015)	X
2003	MOSIS Scalable CMOS Design Rules (revision 7)	
2004	Annotated Portions of *Lee* (Ex. 1107) from Deposition of Dr. Jack Lee (Feb. 25-26, 2016)	
2005	Transcript of Deposition of Dr. Jack Lee (February 25-26, 2016)	
2006	Declaration of Dr. Richard Fair (March 10, 2016)	
2007	M. Koyanagi et al., IEEE SSCS News, pp. 37–41, Winter 2008	
2008	U.S. Patent No. 5,142, 438	
2009	G. Fonstad, *Microelectronic Devices and Circuits*, McGraw Hill, 1994, pp. 241-242	
2010	Wolf and R.N. Tauber, *Silicon Processing*, Vol. 2, Lattice Press, 1990, pp. 17-28	

I. Introduction

Patent Owner Samsung Electronics Company, Ltd. ("Patent Owner" or "Samsung") respectfully submits this Response to the Board's decision to institute *inter partes* review (Paper No. 9, the "Decision") and to the petition for *inter partes* review (the "Petition" or "Pet.") filed by nVidia Corporation ("Petitioner" or "nVidia"). Based on the Petition, the Board instituted review of U.S. Patent No. 6,287,902 ("the '902 patent") on three grounds: (1) obviousness of claims 1, 3-5, 7-12, 14-16, and 18 over KR App. No. 1994/021255 to Lee ("*Lee*", Ex. 1107) in view of JP Pub. No. H7-86158 to Yasushige ("*Yasushige*", Ex. 1109); (2) obviousness of claims 2 and 17 over *Lee*, *Yasushige*, and U.S. Patent No. 4,916,514 to Nowak ("*Nowak*", Ex. 1110); and (3) obviousness of claims 6 and 13 over *Lee*, *Yasushige*, and U.S. Patent No. 4,952,524 to Lee et al. ("*Lee* II", Ex. 1111). Petitioner has, however, not carried its "burden of proving . . . unpatentability by a preponderance of the evidence" (35 U.S.C. § 316(e)) because as explained below and in the accompanying declaration of Patent Owner's expert, Dr. Richard Fair, the asserted references, alone or in combination, fail to disclose or suggest all of the limitations of the challenged claims. Moreover, one of ordinary skill in the art would not have combined the references in the manner proposed by Petitioner. Accordingly, the Board should confirm the challenged claims and enter judgment against Petitioner.

II. Overview of the ’902 Patent

The ’902 Patent, entitled “Methods of Forming Etch Inhibiting Structures On Field Isolation Regions,” was filed on May 25, 1999 and issued on September 11, 2001. The ’902 Patent claims priority as a division to U.S. Patent Application No. 08/748,148, filed on November 12, 1996 (now abandoned).

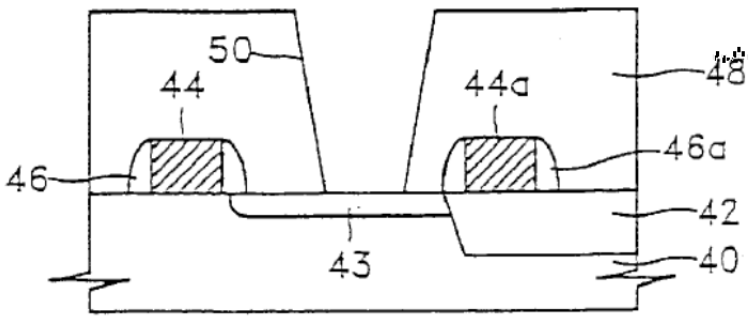
The ’902 patent is directed to a method of providing improved alignment tolerances for contact holes made to scaled microelectronic structures. (Ex. 1001 at 2:44-48; Ex. 2006 at ¶ 23.) A problem that the ’902 patent addresses is how to reliably make contact holes for MOSFETs in smaller and smaller spaces on a wafer when device integration density increases. (Ex. 1001 at 2:10-41; Ex. 2006 at ¶ 23.) For instance, the ’902 patent notes that a misaligned contact hole 24 may expose a portion of the active region of a MOSFET and an adjacent field region that may lead to the flow of leakage currents into the well area of the MOSFET. (Ex. 1001 at 2:10-20, Fig. 2; Ex. 2006 at ¶ 23.)

To remedy the above problem resulting from contact hole misalignment, the ’902 patent discloses an exemplary method of forming etch inhibiting layers on the field isolation region adjacent to the active region (where transistors are formed). (Ex. 2006 at ¶ 24.) The etch inhibiting layer improves alignment tolerance for a contact hole between a first patterned conductive layer on an active region of the substrate and an adjacent field region (which isolates an active region). (Ex. 2006

at ¶ 24; Ex. 1001 at 4:41-50.) The exemplary solution disclosed in the '902 patent may be better understood by referring to the description associated with figures 4-8.

Figure 4 of the '902 patent discloses an exemplary embodiment in which a contact hole 50 is placed between first and second patterned conductive layers 44, 44a to make contact to the doped area 43 (source or drain of a transistor) in the active region. (Ex. 1001 at 4:10-37; Ex. 2006 at ¶ 25.)

FIG. 4

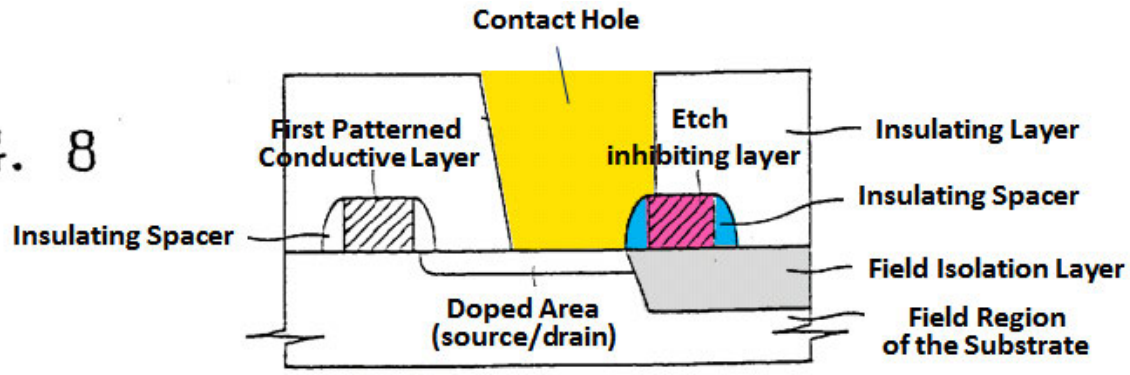


(Ex. 1001 at Fig. 4.) An insulating layer 48 covering the first and second patterned conductive layers 44, 44a, active region 43, and field isolation layer 42 is etched to form contact hole 50. (Ex. 1001 at 5:62-65, 6:8-11, Fig. 7; Ex. 2006 at ¶ 26.)

Conductive layer 44a (annotated in pink below), which is formed on the field isolation layer 42, in combination with sidewall spacers 46a (annotated in blue below) acts as an etch inhibiting layer protecting the field isolation layer from any undesired etching in case of a contact hole misalignment. (Ex. 1001 at 6:1-18, Fig. 8 (annotated below); Ex. 2006 at ¶ 27.) Conductive layer 44a, which is

electrically isolated, is a dummy pattern that protects against contact hole misalignment. (Ex. 1001 at 4:25-30, 5:33-44, 6:20-23; Ex. 2006 at ¶ 27.) According to the ’902 patent, forming an electrically isolated conductive layer 44a that serves no electrical function was “unlike methods of the prior art.” (Ex. 1001 at 5:33-44; Ex. 2006 at ¶ 27.)

FIG. 8



(Ex. 1001 at Fig. 8 (annotated).)

Claims 1-18 of the ’902 patent recite some of the features discussed above that protect the field region from contact-hole misalignment, resulting in improved margins for forming contact holes. (Ex. 2006 at ¶ 28.) For instance, claim 1 of the ’902 patent recites, *inter alia*, “forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, . . . wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, . . . wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.” (Ex. 1001, claim 1.)

III. Claim Construction

A. The Board Should Apply the *Phillips* Standard for Claim Construction

The claims of an unexpired patent are given their broadest reasonable interpretation (BRI) in an *inter partes* review. 37 C.F.R. § 42.100(b). *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 17 at 3 (June 26, 2014) ("*Cisco I*"); *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 20 at 2-3 (July 10, 2014) ("*Cisco II*"); *see also Clearwire Corp. v. Mobile Telecommunications Tech. LLC*, IPR2013-00306, Paper No. 12 at 11 (October 22, 2013); *Toyota Motor Corp. v. Hagenbuch*, IPR2013-00483, Paper No. 9 at 7 (February 4, 2014) ("*Toyota I*"); *Square Inc. v. Cooper*, IPR2014-00156, Paper No. 13 at 3-4 (June 4, 2014) ("*Square I*"). But if a patent subject to an IPR proceeding is due to expire during the pendency of a proceeding (e.g., before the Board rendering its final written decision), the Board applies the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *Cisco II* at 2-3 (citing *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)); *Cisco Systems, Inc., v. AIP Acquisition, LLC*, IPR2014-00247, Paper No. 39 at 6-7 (May 20, 2015) ("*Cisco III*"); *Toyota Motor Corp.*, Paper No. 37 at 5-6 (December 5, 2014) ("*Toyota II*"); *Square Inc.*, Paper No. 38 at 7 (May 14, 2015) ("*Square II*"). Specifically, under *Phillips*, claim terms are given their ordinary and customary meanings, as would be understood by a person of ordinary skill in the art, at the

time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Cisco III*, *Toyota II*, and *Square II* (all citing *Phillips*).

In its institution decision, the Board applied the BRI standard and correctly refused to construe the terms proposed by Petitioner finding that the construction of those terms is not relevant to the parties' dispute in this proceeding. (Decision at 6-7.) Patent Owner submits that this continues to be the case even under the *Phillips* standard. Thus, the Board need not construe any claim term for its final decision.

In the sections below, Patent Owner discusses terms that Petitioner offered for construction or that the Board construed in its institution decision. Patent Owner provides its comments for sake of completeness and to ensure that Patent Owner's positions with respect to these claim terms are in the record in the event Petitioner raises these terms in its reply or the Board construes any of these terms in its final decision. Again, Patent Owner does not believe the Board needs to construe any claim term explicitly for its final decision. Rather, the Board should apply the *Phillips* standard, as Patent Owner has done in this response, to render its final decision.

B. "an insulating spacer along a sidewall of the [second] patterned conductive layer" (Claims 1, 11, 12, 15, and 18)[1]

Claims 1, 11, 12, 15, and 18 recite an "insulating spacer along a sidewall of the [second] patterned conductive layer." (Ex. 1001 at 6:61-63, 7:53-54, 8:14-15, 8:46-47, 9:11-12.) As discussed in the preliminary response (Prelim. Resp. at 13-15), nothing in the phrase warrants any special meanings, and Petitioner has not demonstrated that is the case. Petitioner proposed that this phrase should be construed as "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." (Pet. at 25-26.) The Board correctly rejected Petitioner's proposed construction. (Decision at 6-7.) Patent Owner agrees with the Board's analysis with respect to this phrase. Furthermore, the Board need not construe this phrase at least because this phrase is not relevant to the parties' dispute with regards to whether the cited references disclose all of the claimed features. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy).

[1] Patent Owner identifies only the challenged claims that expressly recite the terms at issue.

C. "an insulating layer" (Claims 1, 2, 8, 11, 12, 14-18)

Claims 1, 2, 8, 11, 12, and 14-18 recite "an insulating layer." (Ex. 1001 at 7:1, 7:4, 7:7-8, 7:27-28, 7:59, 7:62, 8:19, 8:23, 8:29-31, 8:52, 8:55, 8:60-61, 8:64-65, 10:3, 10:6.) As an initial matter, the Board need not construe this term at least because this term is not relevant to the parties' dispute with regards to whether the cited references disclose all of the claimed features. *See Vivid Techs., Inc.*, 200 F.3d at 803. But to the extent the Board wishes to construe this term, it should adopt Patent Owner's construction because it is the correct construction under the *Phillips* standard. Specifically, Patent Owner proposes that this term should be construed as "a structure comprising one or more electrically insulating sublayers." Patent Owner's interpretation is consistent with how the term is used in the claims and specification of the '902 patent.

For example, claim 1 includes the use of "an insulating layer." (Ex. 1001 at 7:1-3.) Dependent claim 2 narrows the scope of the "insulating layer" and states that the insulating layer "comprises nitride." In using the term "comprises," claim 2 is open-ended and permits for additional elements (e.g., additional sublayers). Claim 1, which is necessarily broader than dependent claim 2, similarly is written so as to permit the insulating layer to include one or more electrically insulating sublayers. (*Id.* at 7:1-3.) The specification of the '902 patent also does not limit the scope of an "insulating layer" to a particular number of layers. (*See, e.g., id.*,

4:32-40, 5:60-65.) (*See also* Ex. 2001 at 20-22; Ex. 2002 at 1 (construing "an insulating layer" as "a structure comprising one or more electrically insulating layers").) Therefore, under *Phillips*, "an insulating layer" should be construed as "a structure comprising one or more electrically insulating sublayers." Indeed, the district court in the corresponding litigation adopted Patent Owner's construction. (Ex. 2001 at 20-22.)

D. "forming a trench in said substrate, and wherein said field isolation layer fills said trench" (Claim 6)

Claim 6 recites "forming a trench in said substrate, and wherein said field isolation layer fills said trench." (Ex. 1001 at 7:18-21.) For purposes of this proceeding, Patent Owner agrees with Petitioner that this limitation may be understood in accordance with its plain and ordinary meaning. Patent Owner notes that in co-pending litigation, it proposed a construction under the *Phillips* standard that this limitation means "etching a recess into said substrate and subsequently filling said recess with a field isolation layer." (*See* Ex. 2001 at 23.) However, as noted by the district court in that co-pending litigation, the construction was proposed to make clear that claim 6 does not claim the "LOCOS method" of forming a field isolation layer, but rather the "trench method." (*See id.*; *see also* Ex. 1001 at 4:10-18 (disclosing the LOCOS method and the trench method of forming a field isolation layer).) Since both Petitioner and Patent Owner agree that claim 6 does not claim the LOCOS method (*see* Ex. 2001 at 23), Patent Owner

submits that this clarification is not necessary for purposes of this proceeding.

E. "dummy pattern" (Claims 1, 11, 12, 15, and 18)

In the institution decision, the Board construed "dummy pattern" as "a patterned conductive layer that serves no electrical purpose and is electrically isolated from the substrate and circuits thereon." (Decision at 7.) Patent Owner does not acquiesce with the Board's interpretation. But for purposes of this proceeding, Patent Owner does not contest the Board's interpretation because it does not appear relevant to the parties' dispute with regards to whether the cited references disclose all of the claimed features.

IV. The Cited References Do Not Render Claims 1-18 Unpatentable

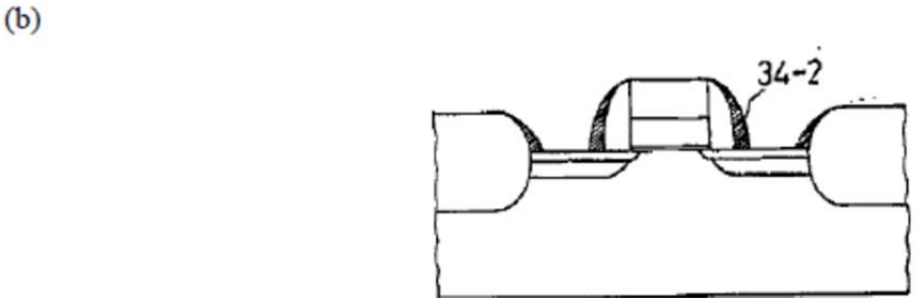
The Board instituted review of the '902 patent based on (1) obviousness of claims 1, 3-5, 7-12, 14-16, and 18 over *Lee* in view of *Yasushige*; (2) obviousness of claims 2 and 17 over *Lee*, *Yasushige*, and *Nowak*; and obviousness of claims 6 and 13 over *Lee*, *Yasushige*, and *Lee* II. (Decision at 19.) In instituting review, the Board relied on the Petition and the declaration of Petitioner's declarant, Dr. Jack Lee. (*Id*. at 8-18.) But for the reasons discussed below, the cited references do not render claims 1-18 unpatentable.

A. Overview of *Lee*

Lee discloses a prior art structure in Fig. 1(a), in which the active region is isolated by a field oxide layer 12 on a semiconductor substrate 11. (Ex. 1107 at 3.) A MOS gate 14 is also shown that is "formed by depositing gate oxide layer, poly

and gate caps in . . . sequence and then etching them." (*Id*.) *Lee* recognizes that in prior art devices, a contact hole misalignment may cause damage to the gate sidewall of the MOS gate or may damage the field oxide layer resulting in junction leakage. (*Id*.) *Lee* illustrates these issues with respect to figure 1(b). (*Id*.; Ex. 2006 at ¶ 29.)

Lee's first embodiment is described with reference to figure 3b, which is shown below:



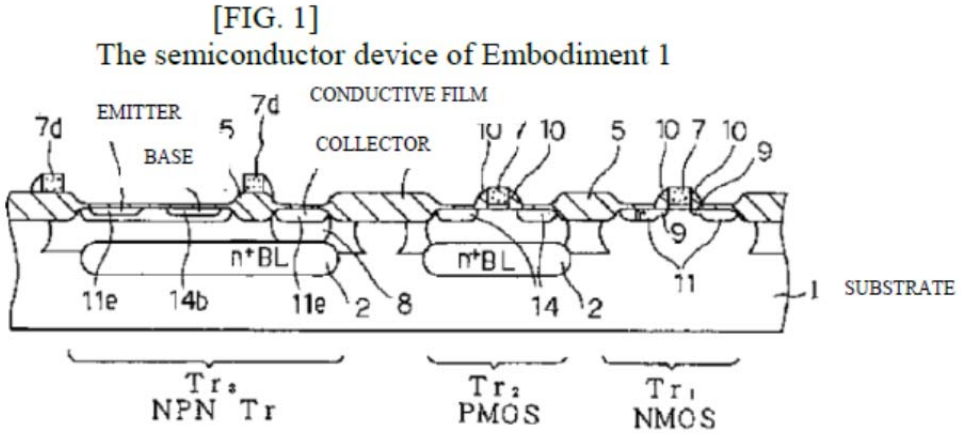
(Ex. 1107 at Fig. 3(b).) *Lee* describes the first embodiment as follows: "At this time, the etch stop layer is formed …in the form of a sidewall through a deposition and etch-back process using the step area formed on the lower layer without any additional mask." (*Id*. at 6.). In Fig. 3b above, it can be seen that the step area referred to by *Lee* is the field oxide layer on which the etch stop layer 34-2 is formed "on the lower layer." (*Id*.; Ex. 2006 at ¶¶ 30-31.)

In a second embodiment, *Lee* discloses "forming an etch stop layer (44-2) using an internal connection line (44-3) passing adjacently or the step of a dummy pattern when the step at the lower layer used to form the etch stop layer in the first

embodiment is not sufficient." (Ex. 1107 at 7.) *Lee* is completely silent on the structure or the constituent layers of the "dummy pattern." (Ex. 2006 at ¶ 32.) For instance, *Lee* does not explain whether the "dummy pattern" takes the shape of a gate (such as MOS gate 34 in Fig. 3(a)) or any other structure. (*Id*.) Nor does *Lee* disclose whether the "dummy pattern" includes a conductive portion. (*Id*.) Neither does *Lee* disclose that the "dummy pattern" is electrically isolated. (*Id*.) All *Lee* discloses is that the etch stop layer 44-2 may be formed using a "dummy pattern" as a step when the step area of the field oxide layer is insufficient. (*Id*.)

B. Overview of *Yasushige*

Yasushige relates to a method of forming a BiCMOS semiconductor device with a lightly doped drain (LDD) structure. (Ex. 2006 at ¶ 33; Ex. 1109 at abstract.) In certain embodiments of *Yasushige*, dummy patterns are formed around the base region of a bipolar transistor simultaneously with the gate electrode of a MOS transistor. (Ex. 2006 at ¶ 33.) For instance, figure 1 of *Yasushige* illustrates dummy patterns (7d) formed on a insulation film (5).



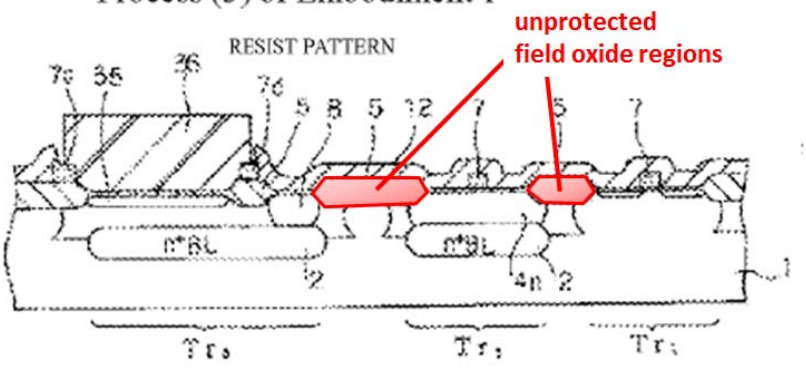
(Ex. 1109 at Fig. 1.)

The problem *Yasushige* was trying to solve was how to form lightly doped drain (LDD) sidewalls on MOS transistors without deterioration in the base regions of bipolar transistors formed in the BiCMOS device. (Ex. 1109 at ¶¶ [0027] – [0028].) As shown in figures 4 and 5, dummy patterns 7d are formed around the base region 14b of a bipolar transistor Tr3, and the dummy patterns 7d and are "electrically isolated from the base region by an isolation region 5." (Ex. 1109 at ¶ [0041].) When film 12 of the base region is removed by wet etching, the dummy patterns 7d act as an etch stopper. (Ex. 1109 at Figs. 4, 5, ¶¶ [0045]-[0046].) At this time, the MOSFET portion of the device is covered by a resist pattern 33. (Ex. 1109 at Fig. 4.) But during this wet etch of the base region isolation film, the sidewall spacers that would have formed on the side of the dummy patterns 7d are removed from one side of the dummy patterns 7d. (*See* Ex. 1109 at Fig. 7, illustrating that the dummy patterns only have spacers 37 on one side.) By doing

so, the area of isolation region 5 adjacent to the active area in the bipolar junction portion is left unprotected during any subsequent etching, such as contact hole formation. (Ex. 2006 at ¶ 34.)

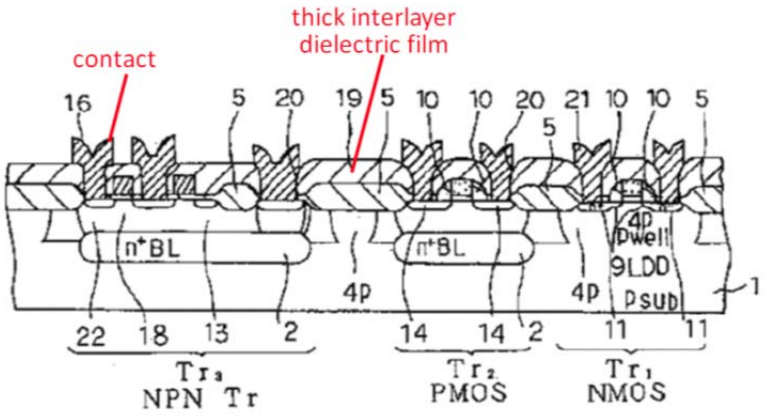
Yasushige is not concerned about avoiding damage to the isolation region 5. (*Id*.) This is evident from the fact that there is no dummy pattern 7d or any other mask present over the field oxide regions during the anisotropic etching of the SiO_2 film 12. (*Id*.; see Ex. 1109 at Fig. 6 (below with annotations added).) Rather, the dummy patterns 7d are added to provide larger tolerance during the formation of resist pattern 36. (Ex. 2006 at ¶ 35; Ex. 1109 at ¶ [0049].) It is the resist pattern 36, which carries out *Yasushige*'s purpose of protecting the active region of the transistor (35) during the anisotropic etching process. (Ex. 2006 at ¶ 35; Ex. 1109 at ¶ [0049].)

[FIG. 6]
Process (5) of Embodiment 1



Moreover, *Yasushige* is not concerned about avoiding damage to the field oxide region during the contact hole formation. (Ex. 2006 at ¶ 36.) For instance,

the only discussion of the contact hole, as shown in figure 8 of *Yasushige*, relates to an embodiment where dummy patterns are not used. (*Id.*) In the embodiment relating to figure 8, the contact holes are made through the thick interlayer dielectric film (19), without any protection from a dummy gate and the sidewall spacers of the dummy pattern for any field oxide region. (*Id.*; *see* Ex. 1109 at Fig. 8 (annotated).)



(Ex. 1109 at Fig. 8 (annotated).) As is shown in figure 8, the field isolation regions (5) are covered only by the dielectric film (19) and are not protected by a dummy pattern. (Ex. 2006 at ¶ 37.)

C. *Lee* and *Yasushige*, Alone or in Combination, Do Not Render Obvious Independent Claim 1

Lee and *Yasushige*, alone or in combination, do not disclose or suggest every feature of independent claim 1 and would not have been combined as alleged. Therefore, they do not render claim 1 obvious. For instance, independent claim 1 recites, *inter alia*, a "second patterned conductive layer [that] is a dummy pattern

electrically isolated from the substrate and circuits thereon." Independent claim 1 further recites "an insulating spacer along a sidewall of the second patterned conductive layer." Petitioner contends that *Lee* and *Yasushige* disclose these features. (Pet. at 44-55.) The institution decision adopted all of Petitioner's allegations and found that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to claim 1. (Decision at 11-15.) Petitioner's allegations are, however, not correct for at least the following reasons.

1. *Lee* Does Not Disclose or Suggest a "Second Patterned Conductive Layer [that] Is a Dummy Pattern"

Relying on figure 4 and a single sentence in *Lee*, Petitioner contends that *Lee* discloses a "second patterned conductive layer (44-3), that may be a dummy pattern." (Pet. at 32, 34, citing Ex. 1116 at ¶¶ 95, 102.) As discussed in detail below, element 44-3 in *Lee* refers to an "internal connection line" and not a "dummy pattern." Having presumed that element 44-3 also refers to a "dummy pattern," Petitioner arrives at the following conclusions: (1) the "dummy pattern" in *Lee* is a "conductive layer" that is patterned; and (2) the "dummy pattern" is "electrically isolated from the substrate and circuits thereon." (*Id*. at 36-38.) Petitioner's analysis is incorrect.

Lee discloses a "second embodiment" with respect to figure 4. *Lee* does not provide a detailed discussion of figure 4 and simply states that figure 4 discloses "a method of forming an etch stop layer (44-2) using an internal connection line (44-

3) passing adjacently *or* the step of *a dummy pattern* when the step at the lower layer used to form the etch stop layer in the first embodiment is not sufficient." (Ex. 1107 at 7, emphases added; Ex. 2006 at ¶¶ 38-39.) *Lee* is completely silent on the structure or the constituent layers of the "dummy pattern." (Ex. 2006 at ¶¶ 39-40.) For instance, *Lee* does not explain whether the "dummy pattern" takes the shape of a gate (such as MOS gate 34 in Fig. 3(a)) or any other structure. (Ex. 2006 at ¶¶ 39-40.) Nor does *Lee* disclose whether the "dummy pattern" includes a conductive portion. (Ex. 2006 at ¶¶ 39-40.) All *Lee* discloses is that the etch stop layer 44-2 may be formed using a "dummy pattern" as a step when the step area of the field oxide layer is insufficient. Relying on *Lee*'s silence regarding the "dummy pattern," Petitioner and its declarant take several leaps with respect to what a "dummy pattern" is in *Lee*.

For instance, Petitioner first assumes that element "44-3" in *Lee* refers to the "dummy pattern."[2] (Pet. at 36, "dummy pattern 44-3"; *see also* Ex. 2005 at 152:25-153:5, 153:18-19.) This is incorrect. *Lee* never annotates the "dummy pattern" by element 44-3. (*See* Ex. 1107 generally.) *Lee* only refers to an internal

[2] This leap is relevant because, as discussed below, Petitioner builds the remainder of its case (e.g., showing that the "dummy pattern" is a "patterned conductive layer") by assuming that element 44-3 and dummy pattern refer to the same thing.

connection line 44-3 and not a "dummy pattern 44-3." (Ex. 2006 at ¶ 40.) Moreover, Petitioner acknowledges that *Lee* distinguishes between an internal connection line and a "dummy pattern." (Pet. at 37, "*Lee* explicitly contemplates two embodiments-one where the conductive pattern is an "internal connection line" and the other where the conductive pattern is a "dummy pattern.") As such, it is improper for Petitioner to assume that 44-3 also refers to the "dummy pattern" in *Lee*.

Having improperly assumed that 44-3 denotes a dummy pattern, Petitioner tries to analogize "dummy pattern 44-3" with MOS gate 34 possibly because element 44-3 (*see* Ex. 1107 at Fig. 4) and MOS gate 34 (*see id*. at Fig. 3(a)) look similar. For instance, Petitioner contends that "dummy pattern 44-3" is formed in the same masking process as MOS gate 34 and "is formed from depositing the same materials, gate oxide layer, poly, and gate cap layers in sequence" as MOS gate 34. (Pet. at 36-37; *see also* Ex. 1116 at ¶ 102.) Because the layers of MOS gate 34 are patterned and include a poly layer, Petitioner presumes that "dummy pattern 44-3" is also "patterned" and is a "conductive layer," as required by claim 1. (Pet. at 36-37; *see also* Decision at 13, relying on Petitioner's representation.) But there is no disclosure in *Lee* whether the internal connection line 44-3, let alone the "dummy pattern," has the same structure and composition as MOS gate 34. (Ex. 2006 at ¶ 40.) Nor is there any disclosure in *Lee* that the layers of internal

connection line 44-3, let alone the "dummy pattern," would have been patterned in the same sequence as MOS gate 34. (Ex. 2006 at ¶ 40.) Indeed, Petitioner and its declarant concede that "other mechanical structures are possible" for forming the "dummy pattern" in *Lee*. (Pet. at 37; Ex. 1116 at ¶ 104.) Therefore, it is improper for Petitioner to conclude from *Lee*'s silence regarding the "dummy pattern" that the "dummy pattern" would have the same structure as MOS gate 34, and by extension of that logic the "dummy pattern" is a "patterned conductive layer." (Ex. 2006 at ¶ 40.)

Likely recognizing this lack of disclosure in *Lee*, Petitioner contends through Dr. Lee's testimony that the "dummy pattern" is most likely to be a gate structure like MOS gate 34 because "forming a gate pattern is most efficient given the already existing patterning process for gates throughout the chip." (Pet. at 37, citing Ex. 1116 at ¶ 104.) But Dr. Lee's testimony merely parrots the Petition and provides no factual basis for its conclusion. (*See* Ex. 1116 at ¶ 104.) Dr. Lee provides no explanation why forming a gate structure as the "dummy pattern" would be "most" efficient. (*Id*.) Neither does Dr. Lee explain what other structures are possible for the "dummy pattern" and why such structures would be less desirable compared to a gate structure. (*Id*.) As such, Dr. Lee's testimony should be accorded little to no weight because it "lack[s] sufficient rationale and factual support." *SAS Institute, Inc. v. Complementsoft, LLC*, IPR2013-00581,

Paper No. 17 at 3, 4 (Feb. 25, 2014); 37 C.F.R. § 42.65(a). It provides no "facts, data, or analysis to support the opinion stated," and should be given no weight. *Kinetic Technologies, Inc. v. Skyworks Solutions, Inc.*, IPR2014-00529, Paper No. 8 at 14-15 (Sep. 23, 2014). To the extent Petitioner is contending that *Lee* makes it obvious to form a "dummy pattern" as a "patterned conductive layer," Petitioner has not met the burden of showing obviousness because an obviousness analysis "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

In fact, Dr. Lee's own testimony in this proceeding casts doubt on his statement that "forming a gate pattern is most efficient." Specifically, Dr. Lee contends that a mechanical structure such as a "dummy pattern" should be "electrically isolated . . . to prevent accidental electrical connections or shorting damage." (Ex. 1116 at ¶ 104.) But a simple way to prevent accidental electrical connection or shorting is to make the "dummy pattern" from a non-conductive material so that there is no chance of any shorting, which implies that a gate structure is not used for the "dummy pattern." (Ex. 2006 at ¶ 41.) Accordingly, if, as Dr. Lee contends, the "dummy pattern" should necessarily be "electrically isolated," then the "most" efficient way to construct the "dummy pattern" would be to form the "dummy pattern" with a non-conductive material instead of using a

gate structure likes MOS gate 34. (*Id*.) After all, *Lee* only utilizes the "dummy pattern" as a step for the etch-stop layer 44-2 and it is not necessary to use a gate structure having a conductive portion to form a step. (*Id*.)

In view of the above, Petitioner has not established that *Lee* discloses that the "dummy pattern" is a "patterned conductive layer" as required by claim 1.

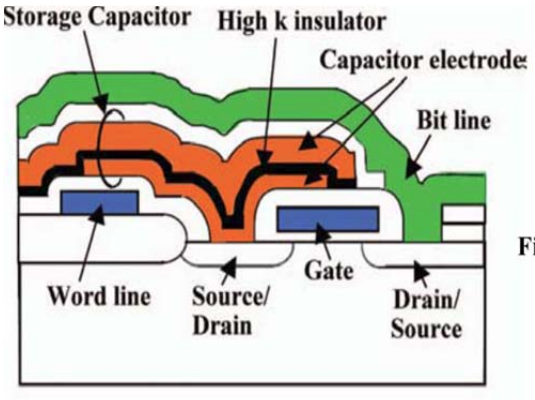
2. *Lee* Does Not Disclose or Suggest that the "Dummy Pattern" is "Electrically Isolated from the Substrate and Circuits Thereon"

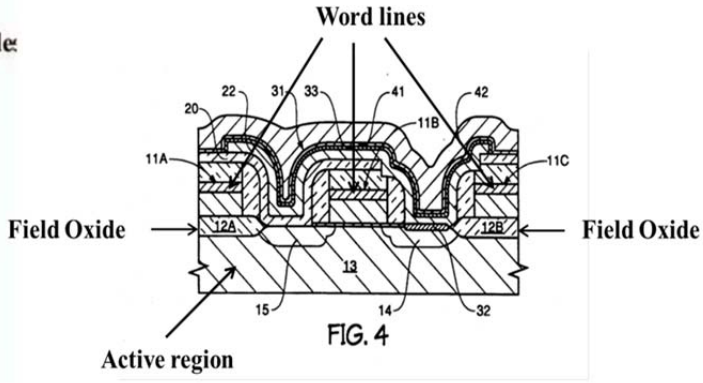
Building on its above faulty analysis, Petitioner contends that the "dummy pattern" in *Lee* must be "electrically isolated from the substrate and circuits thereon." (Pet. at 37-38; *see also* Decision at 13.) Petitioner provides four rationales for this conclusion, each of which should be rejected for the following reasons.

Petitioner first contends that the "dummy pattern" is electrically isolated because it does not extend over the active region and is disposed on the field oxide layer. (Pet. at 37; Decision at 13, relying on this representation.) Under this rationale, however, the internal connection line 44-3 would also be "electrically isolated" because the internal connection line 44-3 is also formed over the field oxide layer. (Ex. 2006 at ¶¶ 42-43; *see* Ex. 1107 at Fig. 4.) But during his deposition, Petitioner's declarant himself conceded that internal connection 44-3 is not "electrically isolated from the substrate and circuits thereon." (Ex. 2005 at

154:13-17; *see also* Pet. at 37, contending that "internal connection line" has connections and dummy pattern does not.) Accordingly, even assuming that the "dummy pattern" is situated over the field oxide layer, which Patent Owner does not concede, such an assumption cannot lead to a conclusion that the "dummy pattern" is "electrically isolated from the substrate and circuits thereon."

Dr. Lee's allegations should be dismissed for the additional reason that the literature prior to 1996 was replete with semiconductor devices in which conductive layers formed on field oxide layers were not "electrically isolated." For instance, as shown in the annotated figures below, well known semiconductor devices had "word lines" disposed on the field oxide layer. (Ex. 2006 at ¶ 44.) A stacked capacitor DRAM cell invented in the 1970s had a "word line" disposed on a field oxide layer. (Ex. 2006 at ¶ 44; Ex. 2007 at 1.) Another stacked capacitor DRAM cell from the early 1990s disclosed in U.S. Patent No. 5,142, 438 had two word lines 11A and 11C "traversing field oxide regions 12A and 12B respectively." (Ex. 2006 at ¶ 44; Ex. 2008 at 2:20-27, Fig. 4.) And as the Board recognized in the related proceeding, IPR2015-01320, a word line is not "electrically isolated." IPR2015-01320, Paper No. 9 at 13-14. Positioning a "dummy pattern" over the field oxide layer, which is not necessarily taught in *Lee*, cannot lead to a conclusion that the "dummy pattern" is "electrically isolated from the substrate and circuits thereon."

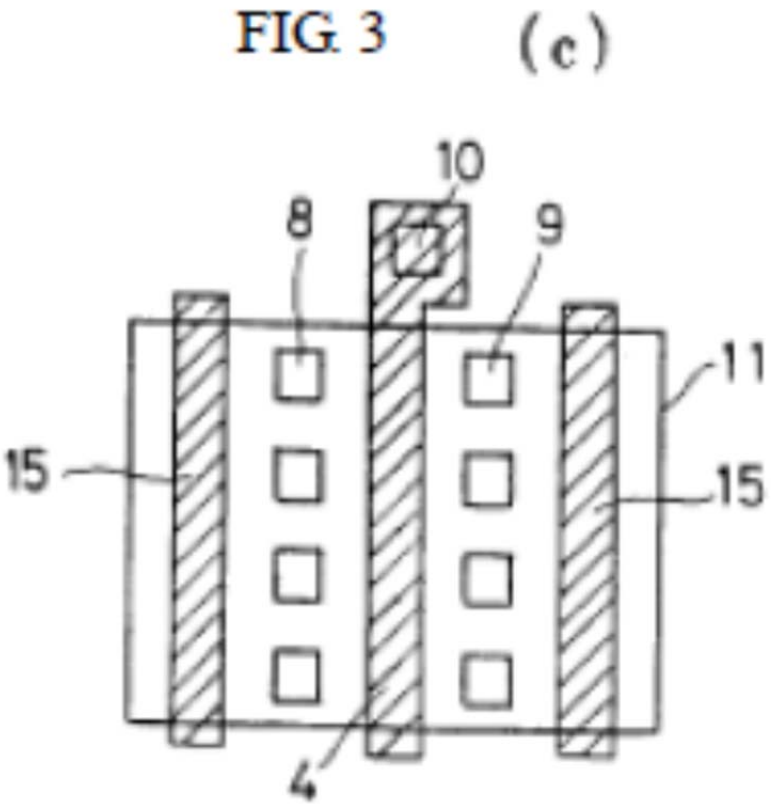




(Ex. 2007 at 1, annotated) (Ex. 2008 at Fig. 4, annotated)

Petitioner next contends that because the "dummy pattern" is not an "internal connection line," it cannot have any connections. (Pet. at 37; *see also* Decision at 13; Ex. 2005 at 155:17-20, "the dummy pattern is not a connection line, meaning that is not connected to the substrate or the circuit.") Petitioner's position, which amounts to an inherency argument, is not supported by *Lee*'s disclosure or the understanding of one of ordinary skill in the art. As an initial matter, Petitioner's inherency argument fails because it has not provided any proof that a non-internal connection line *necessarily* has no connections. (Pet. at 37-38); *see In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999); *see also Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003) ("A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present."). In any case, just because the "dummy pattern" is not an "internal connection line," does not mean that the "dummy pattern" must be "electrically isolated." (Ex. 2006 at ¶ 45.) For instance,

one of the prior art references cited during prosecution of the ’902 Patent, Japanese Patent Application Publication H4-63437 (“Michihiro”) (Ex. 1104) discloses “dummy patterns” 15 formed on the active region that are not “internal connection lines” but are still electrically coupled to the substrate (i.e., not electrically isolated). (Ex. 1104 at 4, Fig. 3(c).) These dummy patterns have “the exact same configuration as the gate electrode 4.” (*Id*. at 4.) Because “dummy patterns 15” have the same configuration as the gate electrode 4 and they are formed on the active region, one of ordinary skill in the art would have understood that the “dummy patterns 15” are electrically coupled to the underlying substrate. (Ex. 2006 at ¶ 45, citing Ex. 2009 at 241-42.) Moreover, one of ordinary skill in the art would have understood that the “dummy patterns 15” are not “internal connection lines” at least because they do not connect to any other circuit in Fig. 3(c). Therefore, it is incorrect for Petitioner and Dr. Lee to conclude that because the “dummy pattern” is not an “internal connection line,” it has to be electrically isolated from the substrate and circuits thereon. (*Id*.)



(Ex. 1004 at Fig. 3(c); Ex. 2006 at ¶ 46.)

Petitioner next contends that the "dummy pattern" in *Lee* would be "electrically isolated" because a "POSITA would know that keeping the mechanical structure electrically isolated is the best and most efficient practice to prevent accidental electrical connections or shorting damage." (Pet. at 38, citing Ex. 1116 at ¶ 104.) This is incorrect for two reasons. First, Petitioner's theory assumes that the "dummy pattern" has no electrical function to begin with. (Ex. 2006 at ¶ 47.) But nothing in *Lee* prevents the "dummy pattern" from having an electrical function. (*Id.*) Second, Dr. Lee's testimony, which is the basis for

Petitioner's conclusion, is conclusory and lacks factual support. For instance, other than offering a single sentence conclusion that "keeping the mechanical structure electrically isolated is the best and most efficient practice to prevent accidental electrical connections or shorting damage," Dr. Lee offers no facts to back up this statement. It provides no "facts, data, or analysis to support the opinion stated," and should be given no weight. *Kinetic Technologies, Inc.*, Paper No. 8 at 14-15.

Relying on the testimony of its declarant, Petitioner finally contends that a "dummy pattern" must be "electrically isolated" based on the definition of the term "dummy" as understood by one of ordinary skill in the art. (Pet. at 38-39, citing Ex. 1116 at ¶ 105; *see also* Decision at 13.) According to Petitioner's declarant, "a dummy pattern is a gate pattern that performs no electrical function, as confirmed by contemporary electrical engineering and microelectronics dictionaries." (Ex. 1116 at ¶ 105; s*ee also* Ex. 2005 at 155:24-156:7, contending that the term "dummy pattern" would be "universally understood by one of ordinary skill in the art as not performing an electrical function.") This is incorrect for several reasons. First, the dictionary definitions that Dr. Lee cites do not refer to a "dummy pattern." (Ex. 1116 at ¶ 105.) They only provide a definition of "dummy" and "dummy connector plug." It is improper for Dr. Lee to extrapolate these definitions to arrive at his desired definition of a "dummy pattern." Second,

Petitioner's declarant is mistaken that there is "universal" definition of a "dummy pattern" and that such a pattern must be "electrically isolated from the substrate and circuits thereon." (Ex. 2006 at ¶ 48.) For instance, Michihiro discloses that "dummy patterns" 15 can be electrically coupled to the substrate, i.e., not electrically isolated. (Ex. 1104 at 4, Fig. 3(c); *see also* Ex. 2006 at ¶ 48.)

For at least the above reasons, Petitioner has not established that the "dummy pattern" in *Lee* is "electrically isolated from the substrate and circuits thereon," as required by claim 1.

3. *Lee* Does Not Disclose an "Insulating Spacer Along a Sidewall of the Second Patterned Conductive Layer. . . [That] Is a Dummy Pattern"

Claim 1 also recites "an insulating spacer along a sidewall of the second patterned conductive layer," which is "a dummy pattern electrically isolated from the substrate and circuits thereon." Therefore, claim 1 recites an insulating spacer along a sidewall of a dummy pattern. Petitioner contends that the "etch stop layer 44-3" is the claimed "insulating spacer" because it is allegedly formed on a sidewall of "dummy pattern 44-3." (Pet. at 32-33; Ex. 1116 at ¶¶ 95-98; *see also* Decision at 12.) Petitioner is incorrect for at least the following reasons.

First, as discussed above in Section IV.C.1, *Lee* does not disclose that element 44-3 corresponds to the "dummy pattern" recited in *Lee*. Therefore, it is improper for Petitioner to assume from the disclosure of figure 4 (which shows

"internal connection line 44-3" and "etch stop layer 44-2") that the etch stop layer 44-2 is also formed on the "dummy pattern" in *Lee*. (Ex. 2006 at ¶¶ 49-50.)

Second, one of ordinary skill in the art would not have understood that the etch stop layer 44-2 is an "insulating spacer" if, as Dr. Lee contends, the "dummy pattern" in *Lee* is a conductive portion and that 44-3 is a gate structure. (*See* Pet. at 36-37, alleging that 44-3 is formed to have a gate structure and includes a conductive portion like in a MOS gate; *see also* Ex. 1116 at ¶ 102.) *Lee* discloses that the etch stop layer 44-2 may be both "conductive or non-conductive." (Ex. 1107 at 7.) But it was well understood by one of ordinary skill in the art that a "spacer" for a gate structure *must* be an insulator. (Ex. 2006 at ¶ 51.) Dr. Lee's testimony in a related proceeding (IPR2016-00134) confirms this understanding. (IPR2016-00134, Ex. 1103 at ¶ 92-"Given that the spacers are in contact with both the gate electrode and the source and drain regions, if they were not electrically insulating, the gate electrode would be short circuited with the source and drain regions, thereby causing the transistor to malfunction.") Therefore, given *Lee*'s disclosure that the etch stop layer 44-2 may be both "conductive and non-conductive," one of ordinary skill in the art would not have understood the etch stop layer to be an "insulating spacer." (Ex. 2006 at ¶ 51.)

Therefore, under Petitioner's analysis, *Lee* does not disclose an insulating spacer along a sidewall of the second patterned conductive layer," which is "a

dummy pattern electrically isolated from the substrate and circuits thereon," as recited in claim 1.

4. *Lee* Would Not Have Been Combined With *Yasushige* as Proposed by Petitioner

Showing a lack of confidence in its primary position, Petitioner states that, "[t]o the extent the limitation 'the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon' is not explicitly disclosed in *Lee*, this limitation is obvious based on *Lee* in view of *Yasushige*." (Pet. at 39.) Relying on Petitioner and Dr. Lee's representations, the Board adopted this position. (Decision at 14-15.) Specifically, citing *Yasushige's* disclosure of dummy pattern 7d formed on field oxide layer 5, Petitioner contends that one of ordinary skill in the art would have been motivated to combine the teachings of *Lee* and *Yasushige* such that the "dummy pattern" in *Lee* becomes "electrically isolated." (Pet. at 39.) Put more simply, Petitioner proposes to make *Lee*'s dummy pattern "electrically isolated from the circuits and substrate thereon" based on *Yasushige*'s disclosure that dummy pattern 7d is electrically isolated. (*Id*.) Petitioner is incorrect for several reasons.

As an initial matter, *Yasushige* does not disclose that the dummy pattern 7d is "electrically isolated *from the substrate and circuits thereon*," as required by claim 1. (Ex. 2006 at ¶¶ 52-53.) *Yasushige* simply states that it includes a "conductive film identical to the gate electrode of [a] MOS transistor [that] is

formed around the base region of [a] bipolar transistor, and said conductive film is electrically isolated from the base region." (Ex. 1109 at ¶ [0029]; *see also id*. at ¶ [0041].) *Yasushige* does not disclose, nor does Petitioner allege that *Yasushige* discloses, that the "conductive film" is electrically isolated from anything other than the "base region." (*See id*. at ¶¶ [0029], [0041].) So even if *Yasushige* discloses electrically isolating dummy pattern 7d from the "substrate," which Patent Owner does not concede, *Yasushige* has no disclosure whether dummy pattern 7d is also electrically isolated from the circuits on the substrate. (Ex. 2006 at ¶ 53.) As discussed in Section IV.C.2, *Lee* does not disclose that the "dummy pattern" in *Lee* is electrically isolated from either the substrate or the circuits on the substrate. Therefore, even if the teachings of both *Lee* and *Yasushige* are combined, the combined teachings do not disclose all of the features of claim 1. For this reason alone, the combination of *Lee* and *Yasushige* does not render claim 1 obvious.

Additionally, one of ordinary skill in the art would not have been motivated to combine the teachings of *Lee* and *Yasushige* in the manner proposed by Petitioner. (Ex. 2006 at ¶ 54.) A proper obviousness analysis requires an explanation "why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*." *Kinetic Technologies, Inc.*, Paper No. 8 at 15 (emphasis in original) (citing *ActiveVideo*

Networks, Inc. v. Verizon Commc'n, Inc., 694 F.3d 1312, 1328 (Fed. Cir. 2012)). "Obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim . . . Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id*. (citing *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011)). As discussed in detail below, Petitioner has simply attempted to combine prior art elements using *impermissible hindsight* without articulating why person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the manner recited in claim 1.

For instance, *Yasushige* does not offer any reasons, nor does Petitioner allege otherwise, for why it would have been desirable to *electrically isolate* the dummy pattern 7d. (Pet. at 19-21, 39-40; Ex. 2006 at ¶ 54.) Petitioner nevertheless contends that "electrically isolating the dummy pattern on a field oxide layer would improve the functionality of *Lee*'s disclosure of the dummy pattern and etch stop layer along its sidewall." (Pet. at 40; Ex. 1116 at ¶ 108.) Specifically, Petitioner contends:

> positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole formation process. By not

> positioning the dummy pattern on the active region itself, there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes.

(Pet. at 40; Ex. 1116 at ¶ 108.) But the above reasons relate to the placement of the "dummy pattern" and do not explain why a "dummy pattern" would be "electrically isolated." (Ex. 2006 at ¶ 55.) They do not even come close to explaining any advantage that would result by electrically isolating *Lee*'s "dummy pattern." (*Id*.) And even if the above reasons provide motivation to place a "dummy pattern" on the field oxide region, such placement does not ensure that the "dummy pattern" is "electrically isolated." (*See supra* section IV.C.2, explaining that placement of a layer over the field oxide region does not result in the layer being "electrically isolated.")

Petitioner additionally contends that "keeping the dummy pattern electrically isolated ensures that the dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern." (Pet. at 40; Ex. 1116 at ¶ 108.) This is not correct because the reasoning assumes that adding a layer of insulation around a dummy pattern prevents etching of the layer(s) of the dummy pattern whatever those layer(s) may be. (Ex. 2006 at ¶ 56.) An insulator is not necessary for preventing etching of an underlying layer. (*Id*.) This is evident from *Lee*

where the etch stop layer is "conductive or non-conductive" and serves as an etch stopper. (Ex. 1107 at 6-8.)

For at least the above reasons, Patent Owner submits that it would not have been obvious to combine the teachings of *Lee* with *Yasushige* in the manner proposed by Petitioner. Therefore, for all the reasons discussed in sections IV.C.1, IV.C.2, IV.C.3, and IV.C.4, Petitioner has failed to prove by a preponderance of the evidence that claim 1 is unpatentable.

D. *Lee* and *Yasushige*, Alone or in Combination, Do Not Render Obvious Claims 3-5, 7-12, 14-16, and 18

Each of the remaining independent claims 11, 12, 15, and 18 recite a "patterned conductive layer" that "is a dummy pattern electrically isolated from the substrate and circuits thereon." Moreover, Petitioner's analysis with respect to this limitation of claims 11, 12, 15, and 18 mirrors Petitioner's analysis for claim 1 for these features (Pet. at 51-54), which as discussed above is not disclosed or suggested by *Lee* or *Lee* in combination with *Yasushige*. Therefore, Petitioner has also failed to prove by a preponderance of the evidence that claims 11, 12, 15, and 18 are unpatentable. (Ex. 2006 at ¶ 57.) Petitioner has similarly failed to prove the unpatentability of claims 3-5, 7-10, 14, and 16 because they depend from one of independent claims 1, 12, and 15, and thus also require the limitation discussed above for claims 1, 12, and 15. (*Id.*)

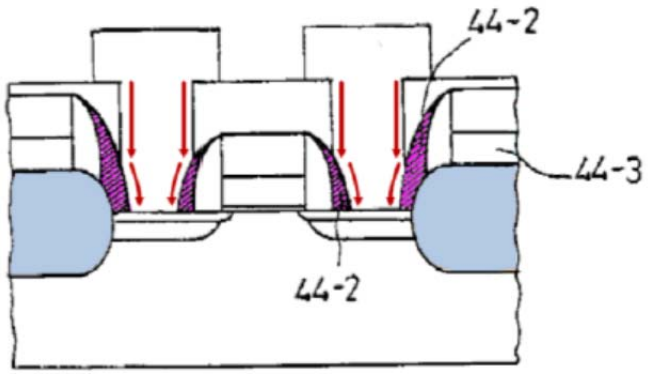
1. Claim 7

For claim 7, Petitioner's analysis is incorrect for an additional reason. Claim 7 recites that "the insulating spacer of the etch inhibiting layer extends to the active region of the substrate." Petitioner contends that *Lee* discloses this feature because the "etch stop layer 44-2 is formed partially on the field oxide layer . . . ." (Pet. at 46; Ex. 1116 at ¶ 122; *see also* Decision at 15.) But as discussed above in Section IV.C.3, one of ordinary skill in the art would have understood that the "etch stop layer 44-2" is not an "insulating spacer." For this additional reason, claim 7 is not unpatentable. (Ex. 2006 at ¶ 58.)

2. Claim 10

For claim 10, Petitioner's analysis fails for an additional reason. Specifically, claim 10 recites, *inter alia*, "at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer." Petitioner contends that *Lee* discloses that the "etch stop layer (44-2) is formed along the sidewalls of both a first patterned conductive layer and a dummy pattern," and relies on figure 4 of *Lee* for support. (Pet. at 49; *see also* Decision at 15.) An annotated version of figure 4 which Petitioner relies upon is

reproduced below[3]:



(*Id*.)

In the above annotated figure, Petitioner assumes that 44-3 refers to a "dummy pattern," which as discussed above in Section IV.C.1 is not correct. Because Petitioner's entire analysis for claim 10 is based on this assumption (Pet. at 49-50), which is not true as discussed in Section IV.C.1., Petitioner's analysis falls apart. (Ex. 2006 at ¶¶ 59-60.) Claim 10 is not unpatentable for this additional reason.

E. *Lee* In View of *Yasushige* and *Nowak* Does Not Render Claims 2 and 17 Unpatentable

Petitioner does not contend that *Nowak* remedies the deficiencies of *Lee* and *Yasushige* identified above in Section IV.C with regards to independent claims 1 and 15. (*See* Pet. at 27-55.) *Nowak* is only relied upon by Petitioner to remedy the

[3] The corresponding figure is not found in the declaration of Dr. Lee. (*See* Ex. 1116 at ¶ 128.)

deficiencies of *Lee* and *Yasushige* with respect to the features of claims 2 and 17. (*Id*. at 55-57.) Therefore, claims 2 and 17 are not unpatentable at least because they include the limitations of their respective independent claims, which as discussed in Section IV.C are not disclosed by *Lee* and *Yasushige*. (Ex. 2006 at ¶ 61.)

F. *Lee* In View of *Yasushige* and *Lee II* Does Not Render Claims 6 and 13 Unpatentable

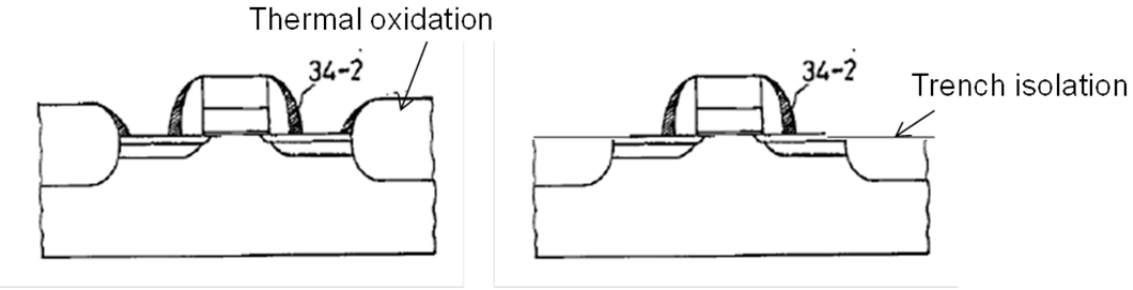
Petitioner does not contend that *Lee II* remedies the deficiencies of *Lee* and *Yasushige* identified above in Section IV.C with regards to independent claims 1 and 12. (*See* Pet. at 27-55.) Instead, Petitioner only relies on *Lee* II for the teaching of a trench isolation method for forming the field oxide layer disclosed in *Lee*. (Pet. at 58-60.) Therefore, claims 6 and 13 are not unpatentable at least because they include the features of their respective independent claims, which as discussed in Section IV.C are not disclosed by *Lee* and *Yasushige*.

Claims 6 and 13 are not unpatentable for an additional reason. (Ex. 2006 at ¶¶ 62-63.) For example, claim 6 recites "forming a trench in said substrate, and wherein said field isolation layer fills said trench." (Ex. 1001 at 7:18-21.) Claim 13 recites a similar feature. Petitioner concedes that *Lee* does not disclose the features of claims 6 and 13, but contends that one of ordinary skill in the art would have combined the teachings of *Lee* and *Lee II* such that the combination yields the claimed invention. (Pet. at 58-60; Ex. 1116 at ¶¶ 58-60; *see also* Decision at 17-

18.) But modifying *Lee* to incorporate *Lee II*'s techniques as proposed by Petitioner would render *Lee* inoperable for its intended purpose thereby rendering the purported modification unobvious. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984). The figures of *Lee* make clear that the field oxide layer is formed by a process known as local oxidation of silicon (LOCOS) by thermal oxidation. (Ex. 2006 at ¶ 63.) In LOCOS thermally grown field oxide is grown by consuming silicon such that the upper surface of the field isolation region is above the substrate surface. (*Id*.) This effect is caused by silicon dioxide having about twice the volume as silicon. (*Id*., citing Ex. 2010 at 17-28.) Based on the shape of *Lee*'s field oxide layer 32, one of ordinary skill in the art would have understood that *Lee* obviously used thermal oxidation to form field oxide layer 32, i.e., used LOCOS. (*Id*.). LOCOS, however, is different from forming a trench and filling the trench with oxide, which is what claims 6 and 13 require. (*Id*.) Thus, claims 6 and 13 of the '902 patent does not read on LOCOS field isolation layers formed by thermal oxidation. (*Id*.)

Lee's embodiments require the field oxide layer 32 to be formed using the LOCOS method because they require the field oxide layer 32 to protrude above the substrate surface. (*Id*.) For instance, *Lee* discloses (in Fig. 3(b)) forming the etch-stop layer on the field oxide layer by using the protruded field oxide layer as a step. (Ex. 1107 at 7; Ex. 2006 at ¶ 64.) In trench isolation, the trench is only filled with

oxide and then made flush with the substrate surface, as shown below. (Ex. 2006 at ¶ 64.) Thus *Lee* could not have implemented of figure 3(b) without using LOCOS field isolation. (*Id*.) A side-by-side comparison of Fig. 3(b) implemented with LOCOS (left) and trench isolation (right) shows why a trench isolation technique would not be desired for *Lee*'s purpose. (*Id*.)



(Ex. 1107 at Fig. 3(b), annotated.)

Similarly, *Lee* bases his third embodiment (*see* Ex. 1107 at Fig. 5) on utilizing the field oxide layer as a mask for forming etch stop layer (54-2), which again suggests that *Lee* uses LOCOS field isolation layer for forming an etch stop layer (54-2). (Ex. 2006 at ¶ 65; Ex. 1107 at 7, "formed by etching the semiconductor substrate using the oxide layers on the substrate (field oxide layer, gate sidewall, cap oxide layer) as mask.")

In view of the above, one of ordinary skill in the art would not have modified *Lee* to incorporate *Lee II*'s techniques because they would render *Lee* inoperable for its intended purpose. (Ex. 2006 at ¶ 66.)

G. The Claims Should Be Confirmed Because Petitioner Has Not Met Its Burden to Establish *Lee* as Statutory Prior Art

As explained above, *Lee* in combination with other references does not render the claims obvious. Thus, the claims should be confirmed. They should be confirmed for the additional reason that Petitioner has not shown that *Lee* qualifies as statutory prior art.

Prior art relied on in a petition for *inter partes* review may only consist of "patents or printed publications." 35 U.S.C. § 311(b). Each of the instituted grounds relies on *Lee*, which is not a "patent." Therefore, the only way *Lee* can qualify as prior art for purposes of this proceeding is if it qualifies as a "printed publication." It is Petitioner's burden to prove by a preponderance of the evidence that *Lee* qualifies as a "printed publication" prior to the effective filing date of the '902 patent. *See Kinetic Technologies, Inc. v. Skyworks Solutions, Inc*., IPR2014-00690, Paper No. 43 at 16-20 (October 19, 2015). To establish that *Lee* qualifies as a "printed publication," the Petitioner must establish by a preponderance of the evidence that the reference was "sufficiently accessible to the public interested in the art." *See In re Klopfenstein*, 380 F.3d 1345, 1348 (Fed. Cir. 2004). "A given reference is 'publicly accessible' 'upon a satisfactory showing that such document has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it . . . .'" *Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d

1374, 1378 (Fed. Cir. 2006) (citation omitted). On this record, Petitioner has not established by a preponderance of the evidence that *Lee* qualifies as a "printed publication."

As an initial matter, Petitioner has not provided any evidence that *Lee* (a Korean patent application) was actually disseminated to the public or that it was published. (Pet. at 9-10.) Rather, Petitioner alleges that when KR Patent Pub. No. 1996-0009001 (Ex. 1112) published on March 22, 1996, it provided sufficient information for anyone to "search and inspect the full *Lee* application." (*Id*.) Put simply, Petitioner alleges that *Lee* constitutes a "printed publication" because the '001 publication "serves as an index, or roadmap to a POSITA to go find the" underlying patent application (i.e., *Lee*). (*Id*., citing *In re Wyer*, 655 F.2d 221 (CCPA 1981).) Petitioner, however, fails to address an important aspect of the "public accessibility inquiry," which is whether in 1996, the Korean patent office would have actually provided a copy of *Lee* to anyone interested in inspecting *Lee*. The institution decision overlooked this aspect of the "public accessibility inquiry" when it instituted this proceeding. (Decision at 10.)

Even assuming *arguendo* that the '001 publication would have served as "roadmap" or "index" for an interested party to locate the underlying patent

application, *see Bruckelmyer*[4], 445 F.3d at 1379, that does not end the "public accessibility" inquiry. A key component of this inquiry, which dooms Petitioner's public accessibility showing, is whether the document was *actually* accessible to an interested person once they were able to locate the patent application, i.e., once they came to know of the existence of the underlying patent application.

"The date on which the public *actually* gained access to the invention by means of the publication is the focus of [the public accessibility] inquiry." *In re Bayer*, 568 F.2d 1357, 1360 (CCPA 1978). It is not sufficient that an interested person be able to locate the document via an index or catalogue (like the '001 publication); the interested person must also be able to access the reference and examine its contents. *In re Lister*, 583 F.3d 1307, 1312 (Fed. Cir. 2009) (emphasis added) ("we must . . . determine whether an interested researcher would have been sufficiently capable of finding the reference *and examining its contents*."). On this record, Petitioner has not provided adequate proof that an interested person could actually obtain a copy of *Lee* and examine its contents in such a way that demonstrates that *Lee* constitutes a "printed publication." *See Northern Telecom,*

[4] In *Bruckelmyer*, the Federal Circuit found that a published patent from the foreign patent office may provide a "roadmap that would have allowed one skilled in the art" to locate the underlying application.

Inc. v. Datapoint Corp., 908 F.2d 931, 936–37 (Fed.Cir.1990) (finding that documents housed in a library, which restricted access to only authorized persons, did not constitute "printed publications"). No wonder, in holding that an Australian patent application constituted a "printed publication," the *Wyer* court went to great lengths to explain how the Australian Patent Office allowed anyone to obtain a copy of the Australian patent application:

> Equipment was available to the public in the Patent Office and in the sub-offices for providing an enlarged reproduction of the diazo copies on a display screen. Equipment was also available for producing enlarged paper copies for purchase by the public. Moreover, diazo copies were also available for sale to the public upon application to the Australian Patent Office, these latter diazo copies being produced to order from the second microfilm copy * * *.

Wyer, 655 F.2d at 226.

The Board has similarly held that any restrictions placed on the accessibility of a document weighs against a finding of "public accessibility." *See, e.g.*, *Samsung Elecs. Co. v. Rembrandt Wireless Techs., LP*, IPR2014-00514, Paper No. 20 at 2-4 (Oct. 24, 2014) (finding that a "password-protected" draft IEEE standard did not constitute a "printed publication" because, among other things, the password protection served to limit distribution of the IEEE draft). As the Board

explained in *Samsung Elecs. Co.*, "the fact that an interested individual needed to contact IEEE in order to obtain a password or other means of accessing Draft Standard (and needed to know who to contact in the first place) weighs against public accessibility." *Id*.

Petitioner's evidence does not show that *Lee* was actually accessible to anyone interested in examining its contents and does not address any restrictions the Korean Patent Office may have placed on a person interested in examining *Lee*. While "laying open [a patent application] for public inspection" may support a finding that the patent application constitutes a printed publication," (Pet. at 10; Decision at 10), Petitioner has not adduced any evidence establishing that *Lee* was available for "public inspection" in March 1996-the alleged publication date for *Lee*. There is simply no evidence in the record regarding the Korean Patent Office's practices in 1996 with respect to making Korean applications (as opposed to mere abstracts) available to anyone interested in examining them and what if any restrictions were placed on such interested persons. This lack of evidence weighs against a finding of "public accessibility." *See Northern Telecom, Inc.*, 908 F.2d at 936–37; *Samsung Elecs. Co.*, Paper No. 20 at 2-4. To the extent *Lee* may have been available to Korean Patent Office personnel, such accessibility is insufficient to establish "public" accessibility. *Garrett Corp. v. United States*, 422 F.2d 874, 878 (Ct. Cl. 1970) ("distribution to government agencies and personnel

alone may not constitute publication").

The above deficiencies in Petitioner's evidence cannot be remedied by conclusory testimony from Petitioner's declarant, Dr. Lee, who opines that based on his "understanding of the law constituting a printed publication for purposes of prior art, the Korean Patent Office's laying open process is sufficient to make *Lee* a printed publication as of March 22, 1996." (Ex. 1116 at ¶ 39.) As an initial matter, the Petition does not cite to or discuss Dr. Lee's testimony regarding *Lee*'s public accessibility. (Pet. at 9-10.) Accordingly, the Board should not give any weight to this testimony. 37 C.F.R. § 42.104(b)(5); *see also Google Inc. v. Art+Com Innovationpool GMBH*, IPR2015-00788, Paper No. 7 at 10 (Sep. 2, 2015) (declining to give any weight to expert testimony regarding public accessibility because it was neither cited nor discussed in the Petition). But the institution decision nevertheless relied on Dr. Lee's testimony to conclude that Petitioner has made a threshold showing of *Lee* being publicly accessible. (Decision at 10[5], citing Ex. 1116 at ¶ 39.) The Board should not rely on Dr. Lee's

[5] The institution decision states that "[n]otably, Patent Owner . . . does not assert that *Lee* was not publicly accessible in 1996." (Decision at 10.) Patent Owner respectfully submits that it is Petitioner's burden to prove that *Lee* was publicly accessible as of March 22, 1996, not Patent Owner's burden to prove otherwise.

testimony, however, in its final decision. During cross-examination Dr. Lee admitted that he is neither an expert in the Korean Patent Office laying-open process in 1996 nor does he possess any personal knowledge that *Lee* was publicly available to interested persons in March 1996. (Ex. 2005 at 79:15-21, 75:23-79:11, 80:1-9.) Indeed, he derived his conclusion that *Lee* is a printed publication as of March 1996 based on discussions he had with Petitioner's attorneys. (*Id*.) Under these circumstances, his testimony should not be accorded any weight for purposes of determining *Lee*'s status as a printed publication. *Dish Network L.L.C. v. Dragon Intellectual Property, LLC*, IPR2015-00499, Paper No. 7 at 11 (July 17, 2015).

Petitioner may try to submit with its reply additional evidence[6] regarding this issue. But the Board should not allow Petitioner to submit such evidence as it could and should have submitted such evidence before the reply stage of the

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35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, *the petitioner* shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.") (emphasis added).

[6] Petitioner may have in its possession additional evidence that it plans on using at trial in the corresponding district court case. Petitioner should bear the consequences of its strategic choice to withhold such additional evidence.

proceeding. The Board should not allow petitioners to provide such evidence with their replies, especially in a proceeding like this one where this issue was squarely raised during the preliminary response stage. Office Patent Trial Practice Guide, 77 Fed. Reg. 157 at 48767 (Aug. 14, 2012) ("While replies can help crystalize issues for decision, a reply that raises a new issue or belatedly presents evidence will not be considered and may be returned. . . . Examples of indications that a new issue has been raised in a reply include new evidence necessary to make out a prima facie case for the patentability or unpatentability of an original or proposed substitute claim, and new evidence that could have been presented in a prior filing.")

Therefore, Petitioner has not met its burden to establish *Lee* as a printed publication and, as a result, all of the instituted grounds (each of which relies on *Lee*) fail. The Board should enter judgment against Petitioner and confirm the claims for this reason alone.

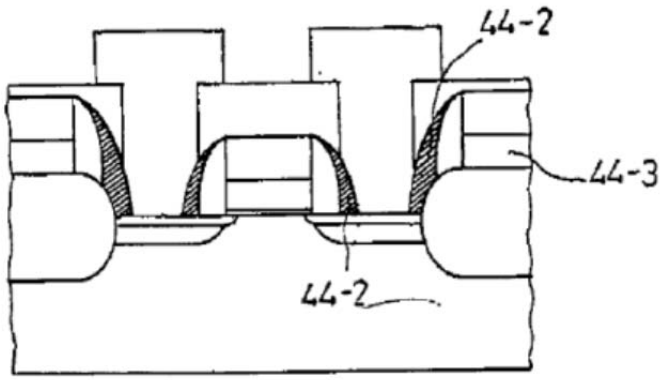
H. The Board Should Not Accord Dr. Lee's Testimony Any Weight

As discussed above in Sections IV.C, IV.D, and IV.F, Petitioner relies heavily on Dr. Lee's testimony in support of its positions. But his testimony should not be accorded any weight. In fact, as discussed in the foregoing sections, Dr. Lee's testimony was result-oriented and hindsight driven. Indeed, as discussed extensively in Sections IV.C, IV.D, and IV.F, Dr. Lee's interpretation of the

references is not supported by the references themselves and other literature from the relevant timeframe. These sections discuss in detail the extensive leaps Dr. Lee took to arrive at his ultimate conclusion that the claims of the ’902 patent are not patentable. Dr. Lee’s deposition uncovered many other such leaps, a few of which are discussed below.

For example, Dr. Lee assumed several facts that have no basis in the cited references. In connection with the claim feature of “an insulating spacer along a sidewall of the second patterned conductive layer,” Dr. Lee opined that etch stop layer 44-2 in *Lee* “touch[es]” the sidewall of element 44-3 in *Lee*. (Ex. 2005 at 146:7-22.) According to Dr. Lee, “44-2 touches 44-3, and therefore it is along the sidewall of the second patterned conductive layer.” (*Id*. at 147:4-9.) When Dr. Lee was asked how his analysis was supported by *Lee*, he stated that the “figure clearly shows that it touches.” (*Id*. at 147:18-23.) But the figures are hardly “clear” in this regard. For instance, only under a hindsight driven result-oriented view of figure 4, can one conclude that the figure “clearly” shows etch stop layer 44-2 touching 44-3.

FIG. 4



(Ex. 1107 at 17, Fig. 4.) When pressed on how the specification of *Lee* supports his opinion, Dr. Lee gave a rather convoluted response picking on random portions of *Lee*. For instance, Dr. Lee contended that *Lee* discloses fabricating the etch stop layer "in the form of sidewall" and "through a deposition and etch-back process." (Ex. 2005 at 147:24-149:18.) But the portion that Dr. Lee cites relates to figure 3(b) of *Lee* and shows how the etch stop layer is formed as a sidewall *of the field oxide layer* (not element 44-3). (Ex. 1107 at 7, "At this time, the etch stop layer is formed . . . in the form of a sidewall . . . using the step area formed on the lower layer . . . .") Dr. Lee confirms this. (Ex. 2005 at 149:7-24.) That is, the cited portion says nothing about whether *Lee* considers etch stop layer 44-2 as a sidewall of *44-3* (*see* Ex. 1107 at Fig. 4) and whether 44-2 touches 44-3. Dr. Lee's analysis is simply not supported by *Lee* and raises serious doubts regarding his credibility.

Another instance of Dr. Lee's result-oriented review of *Lee* can be seen from the discussion of the "cap oxide layer" in *Lee*. *Lee* discloses a cap oxide layer with

reference to figure 5. (Ex. 1107 at 7.) Dr. Lee initially contended that the "cap oxide layer" is only present in the gate shown in figure 5 but is not present in the gate structures shown in the other figures (3(a), 3(b), 3(c), 3(d), and 4.) (Ex. 2005 at 183:23-184:11.) Dr. Lee even thought of a reason why the gate structure of figure 5 in *Lee* is different from the gate structures in the remaining figure-"Figure 5 is . . . a new embodiment in which they purposely etch the substrate to create a higher step, and by doing so, they would have to add a cap oxide layer." (*Id*. at 184:4-11.) Dr. Lee confirmed that he firmly believed in his analysis stating that the embodiment of figure 5 is "clearly" different from the embodiments of figures 3 and 4:

> Figure 4 basically describe that . . . using a new -- using an etch-inhibiting layer which could be internal connection line or a dummy pattern. But the rest of the fabrication basically the same as Figure 3, (a), (b), (c), and (d). So Figure 3 and Figure 4 are the same in terms of this -- the fabrications of the first patterned conductive layer and the MOS gate structure, while, on the other hand, Figure 5 clearly is a -- describing a embodiment that modified the gate structure in order to form and etch the substrate using the gate oxide -- using the oxide layer on the substrate as a mask. Do you see the difference?

(*Id*. at 185:7-20; *see also id*. at 188:21-189:3.) Indeed, Dr. Lee stated unequivocally that the MOS gates of figures 3 and 4 are different from the MOS

gate of figure 5 deriving support for his analysis from a scant description of the figures in *Lee*. (*Id*. at 190:19-191:7.) But when asked whether the gates in figures 3 and 4 have the same layer structure now that he had concluded that figure 5 has a different structure, Dr. Lee resorted to generalities without giving any rational basis for why the gates in figures 3 and 4 have the same structure. (*Id*. at 191:8-193:8.)

All of this is relevant because it raises the question whether Dr. Lee can properly conclude from *Lee*'s scant disclosure that the MOS gate of figure 4 has the same layer structure as the MOS gate of figure 3 now that he agrees figure 5 has a different structure. As discussed in Section IV.C.1, Dr. Lee analogizes between the "dummy pattern" and MOS gate 34 (which is in figure 3) to conclude that the "dummy pattern" in *Lee* is a patterned conductive layer. Specifically, Petitioner contends that "dummy pattern 44-3" is formed in the same masking process as MOS gate 34 and "is formed from depositing the same materials, gate oxide layer, poly, and gate cap layers in sequence" as MOS gate 34. (Pet. at 36-37; *see also* Ex. 1116 at ¶ 102.) Because the layers of MOS gate 34 are patterned and include a poly layer, Petitioner presumes that "dummy pattern 44-3" is also "patterned" and is a "conductive layer," as required by claim 1. (Pet. at 36-37.) But for this analysis to hold water, Dr. Lee had to conclude at a minimum that the gates in figures 3 and 4 have the same structure. This is what he tried to do after

conceding that figure 5 has a different gate structure. Not surprisingly, after his cross-examination finished, Dr. Lee changed his extensive deposition testimony on re-direct to say that all the figures (including figure 5) have the same gate structure.

Specifically, after Dr. Lee's cross-examination ended, Dr. Lee met with Petitioner's counsel where they discussed the substance of the cross-examination testimony. (Ex. 2005 at 273:16-276:4.) When Dr. Lee came back from this meeting, Petitioner's counsel asked Dr. Lee leading questions to get him to clarify his testimony regarding the cap oxide layer. (*Id*. at 272:5-7.) Dr. Lee answered that all the figures of *Lee* (including figure 5) have the same gate structure. (*Id*. at 272:7-273:11.) All of this is after Dr. Lee repeatedly characterized his earlier testimony (figure 5 has a different gate structure compared to the gates in the other figures) as being "clearly" supported by *Lee*.

For at least the above reasons, the Board should not give any weight to Dr. Lee's result-oriented hindsight-driven testimony.

V. Conclusion

As explained above, Petitioner has failed to prove by a preponderance of the evidence that the challenged claims are unpatentable. Patent Owner respectfully requests that the Board confirm these claims and enter judgment against Petitioner.

Dated: March 10, 2016

Respectfully submitted,

/Naveen Modi/

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Counsel for Patent Owner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on March 10, 2016, I caused a true and correct copy of the foregoing Patent Owner's Response to Petition for *Inter Partes* Review of U.S. Patent No. 6,287,902 to be served by electronic means on Counsel for Petitioner at the following addresses of record:

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