**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|
| In re *Inter Partes* Review of: | ) |
| U.S. Patent No. 6,287,902 | ) |
| Issued: Sept. 11, 2001 | ) |
| Application No.: 09/318,188 | ) |
| Filing Date: May 25, 1999 | ) |

For: **Methods of Forming Etch Inhibiting Structures on Field Isolation Regions**

**FILED VIA PRPS**

**PETITION NO. 2 FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,287,902**

For ease of reference, Petitioner refers to this Petition as "'902 Petition No. 2" challenging all claims of the '902 patent.

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## EXHIBIT LIST

1101 U.S. Patent No. 6,287,902 ("'902 patent")

1102 File History for the '902 patent

1103 Curriculum Vitae of Dr. Jack Lee

1104 JP 4-63437 ("Michihiro")

1105 U.S. Patent No. 5,550,076 ("Chen")

1106 U.S. Patent No. 5,441,916 ("Motonami")

1107 KR Patent App. No. 1994/021255 ("Lee")

1108 Certified English Translation of Korean Ministry of Government Legislation, Enforcement Decree of the Patent Act effective January 1, 1994, partially amended by Presidential Decree No. 14059 on Dec. 31, 1993

1109 JP Pub. No. H7-86158 ("Yasushige")

1110 U.S. Patent No. 4,916,514 ("Nowak")

1111 U.S. Patent No. 4,952,524 ("the '524 Patent")

1112 KR Patent Pub. No. 1996-0009001 ("Lee")

1113 The Electronic Packaging, Microelectronics, and Interconnection Dictionary, 1993.

1114 IEEE Standard Dictionary of Electrical and Electronics Terms at 322, 6th ed.

1115 Joint Identification of Claim Terms for Construction, *Samsung Electronics Co. Ltd., et al. v. NVIDIA Corp. et al.*, 3:14-cv-00757-REP (E.D. Va.)

1116 Declaration of Dr. Jack Lee in Support of Petition No. 2 for *Inter Partes* Review of U.S. Patent No. 6,287,902

# I. INTRODUCTION

On behalf of NVIDIA Corp. ("Petitioner") and under 35 U.S.C. § 311 and 37 C.F.R. 42.100, *inter partes* review of claims 1–18 ("challenged claims") of U.S. Patent No. 6,287,902 ("'902 patent"), titled "Methods of Forming Etch Inhibiting Structures on Field Isolation Regions," is requested. According to United States Patent and Trademark Office ("Patent Office") records, the '902 patent was originally assigned to, and is currently owned by, Samsung Electronics Co., Ltd. ("Patent Owner"). A copy of the '902 patent is attached as Ex. 1101, and the prosecution history is attached as Ex. 1102.

# II. REQUIREMENTS FOR PETITION FOR *INTER PARTES* REVIEW

## A. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the '902 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the '902 patent on the grounds below.

## B. Notice of Lead and Backup Counsel and Service Information

Under 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

| LEAD COUNSEL | BACKUP COUNSEL |
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Under 37 C.F.R. § 42.10(b), a Power of Attorney is attached.

### C. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real-party-in-interest is NVIDIA Corporation. No other party exercised or could have exercised control over this petition; no other party funded or directed this petition. (*See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759–60.)

### D. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

*Samsung Electronics Co., Ltd., et al. v. NVIDIA Corp. et al.*, 3:14-cv-00757-REP (E.D. Va.). Petition for *Inter Partes* Review, Case No. IPR2015-01320. According to Patent Office records, no applications claim the benefit of priority to the filing date of the ’902 patent.

### E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 506269.

### F. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence address of record for the ’902 patent is attached.

## III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))

Claims 1-18 of the ’902 patent (the “challenged claims”) are unpatentable in view of the following prior art: (i) KR App. No. 1994/021255 (“Lee”) (Ex. 1107); (ii) JP Pub. No. H7-86158 (“Yasushige”) (Ex. 1109); (iii) U.S. Patent 4,916,514 (“Nowak”) (Ex. 1110); and (iv) U.S. Patent 4,952,524 (“the ’524 Patent”) (Ex. 1111).

Specifically, the challenged claims are invalid under 35 U.S.C. § 103 on the following grounds:

**Ground 1:** claims 1, 3-5, 7-12, 14-16, and 18 are rendered obvious by Lee and Yasushige.

**Ground 2:** claims 2 and 17 are rendered obvious by Lee in combination with Yasushige and Nowak.

**Ground 3:** claims 6 and 13 are rendered obvious by Lee in combination with Yasushige and the ’524 patent.

## IV. DESCRIPTION OF PURPORTED INVENTION

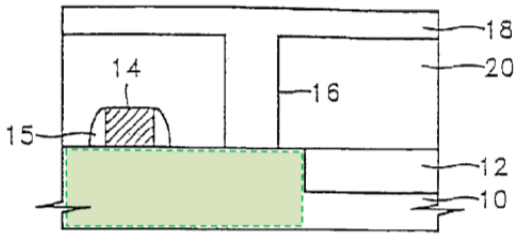
The ’902 patent relates to methods for forming contact holes in microelectronic structures. Ex. 1116 (Decl. of Dr. Jack Lee in support of Petition No. 2 for *Inter Partes* Review of U.S. Patent No. 6,287,902) (“Lee Decl.”) at ¶ 23.

### A. Background

The purported invention of the ’902 patent relates to forming contact holes

in microelectronic structures. For example, integrated circuit memory devices include a plurality of memory cells, and each memory cell is connected to other cells by conductive (metal) lines. '902 patent at 1:23-25. The cells and conductive (metal) lines are connected to the substrate by contact holes. *Id.* at 1:25-27. The contact holes expose active regions of the substrate. *Id.* at 1:28-29. Patterned gate electrode layers are generally arranged around the contact holes and are electrically isolated from the contact holes. *Id.* at 1:32-33. Lee Decl. at ¶ 23.

Such structures are formed on a semiconductor substrate, as illustrated in Fig. 1. First, a field oxide layer **12** is formed on the substrate **10**. *Id.* at 1:52-53. The field oxide layer may be formed using either a LOCOS field oxide layer or a trench field oxide layer. *Id.* at 1:45-50, 4:16-18. The field oxide layer defines the active region on the substrate **10**. *Id.* at 1:52-55. Annotated Fig. 1 of the '902 patent shows a cross-section of an integrated circuit device. *Id.* at Fig. 1.

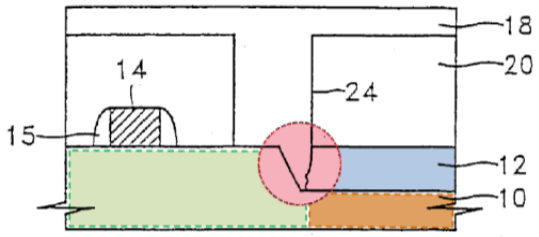



A gate electrode **14** is formed over the active region (green), and spacers **15** are formed along the sidewall. *Id.* at 1:52-56. An insulating layer **20** is formed on the surface of the substrate including the gate electrode **14** and the field oxide layer **12**. *Id.* at 1:56-58. Contact hole **16** is formed by etching insulating layer **20** between

the gate and field oxide layer to expose a portion of the active region. *Id.* at 1:58-60. Conductive layer **18** is formed on the insulating layer and fills the contact hole, creating a contact with the active region. *Id.* at 1:60-65. Lee Decl. at ¶ 24.

As integrated circuit devices become more highly integrated, the space available for forming devices is reduced. '902 patent at 1:18-20. For example, the space between the patterned layers is reduced, and accordingly the space available for forming the contact holes is also reduced. *Id.* at 1:36-38. Thus increased integration reduces the margin available in the placement of the holes, and leads to an increased risk in misaligned contact holes. *Id.* at 1:41-50. Lee Decl. at ¶ 25.

Annotated Fig. 2 of the '902 patent shows a cross-sectional view of an integrated circuit device with a misaligned contact hole **24** exposing a portion of the active region (green) as well as a portion of the field oxide layer **12** (blue) on the field region (brown) in the substrate **10**. '902 patent at 2:10-12. This mis-alignment results in the formation of a well (red circle) through field oxide layer **12** thus exposing a portion of a field region. *Id.* at 2:12-15. Lee Decl. at ¶ 26.

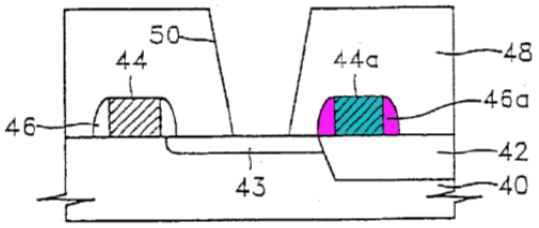



When the contact hole **24** is filled with the conductive layer **18**, the conductive layer **18** is brought into contact with the well. *Id.* at 2:17-19. Leakage current may

thus flow through the conductive layer **18** into the well area and cause a delay or malfunction in the device. *Id.* at 2:20-23. Lee Decl. at ¶ 26.

### B. Description of '902 Patent Alleged Invention

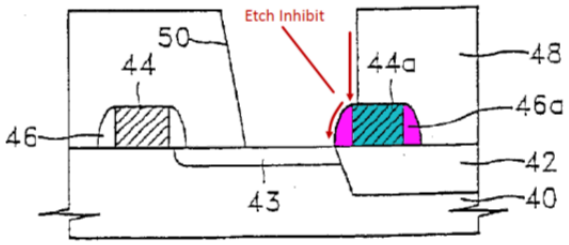
The '902 patent addresses the problem of contact hole misalignment by forming a second patterned conductive layer **44a** with insulating sidewall spacers **46a** on the field region:




'902 patent, Fig. 4. Compared to the first patterned conductive layer **44**, the second patterned conductive layer is electrically isolated and thus serves as a dummy pattern. *Id.* at 4:27-30. Lee Decl. at ¶ 27.

An insulating layer is then formed over the surface of the substrate and the first and second patterned conductive layers. *Id.* at 3:31-33. A contact hole **50** is formed in the insulating layer **48** exposing a portion of the active region **43**. *Id.* at 3:33-35. Because the insulating layer is preferably formed of a material more susceptible to etching than the material used to form the sidewall spacers **46a**, some misalignment of the contact hole **50** can be tolerated. *Id.* at 4:37-42. In particular, if the contact hole extends beyond the active region of the substrate encroaching into the field region, a second patterned conductive layer **44a** and its

sidewall spacers **46a** act as an etch inhibitor when etching the insulating layer **48**:




'902 patent, Fig. 4; *Id.* at 4:42-48. Lee Decl. at ¶ 28.

In the structure of the '902 patent invention, the area over which the contact hole can be formed is larger than the area available using the structure of the prior art cited in the '902 patent specification. *Id.* at 4:52-55. In the prior art Fig. 1, the contact hole must be formed between the gate electrode and the field oxide layer so as not to risk operational problems. *Id.* at 4:55-57. When using the structure of the '902 patent, the area over which the contact hole can be formed extends over a portion of the field region covered by the second patterned conductive layer. *Id.* at 4:58-61. Accordingly, a greater contact margin is allowed when forming the contact hole. *Id.* at 6:31-32. Etching margins can be increased without risk of damaging the field isolation layer. *Id.* at 6:33-34. Reliability of the integrated circuit device can be increased because leakage current generated by damage to the field isolation layer can be reduced. *Id.* at 6:35-37. Lee Decl. at ¶ 29.

### C. '902 Patent Prosecution History

While the Patent Office discussed several references during prosecution, it did not discuss the Lee, Yasushige, Nowak, or the '524 patent references discussed

below, nor were they cited. The Examiner thus likely did not consider any of these references.

In the Notice of Allowance, the Examiner stated: "the prior art of record fails to disclose all the process limitations recited in the base claims, including a combination of a step of forming a dummy pattern as an etch inhibiting layer on a field isolation layer and a step of forming along the sidewalls of a dummy pattern the spacers that will prevent damage to the field oxide layer in the event the contact hole is misaligned." However, as explained below in the Overview of the Prior Art and Motivations to Combine the Prior Art References sections, both primary reference Lee secondary reference Yasushige disclose the use of dummy patterns and using the dummy patterns or their spacers to prevent damage to the field oxide layer. Further details of the prosecution history are described in Lee Decl. at Section V.D.

## V. LEVEL OF ORDINARY SKILL IN THE ART IN THE RELEVANT TIMEFRAME

For purposes of this review, a person of ordinary skill in the art is a person with an undergraduate degree in electrical engineering (or equivalent subject) together with either:

1) three to four years of post-graduate experience designing semiconductor devices and fabrication processes; or
2) a master's degree in electrical engineering (or equivalent subject)

> together with one to two years of post-graduate experience in designing semiconductor devices and fabrication processes.

Lee Decl. at ¶ 19. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa.

## VI. OVERVIEW OF THE PRIOR ART

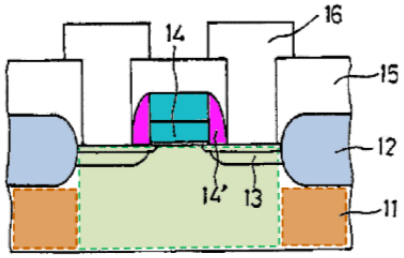
### A. KR App. No. 1994/021255 ("Lee")

The purported invention of the '902 patent relates to the forming of a dummy pattern and spacers on a field oxide layer to serve as an etch inhibitor layer when forming contact holes. However, a Korean company Gold Star Electron Co., Ltd. had already addressed the very same problems and designed and filed a patent application on the features described in the '902 patent more than two years prior to the filing date of the earliest parent application of the '902 patent. The patent application, KR App. No. 1994/021255 (Ex. 1107, "Lee"), is titled "Fabrication Method for Semiconductor Device" and lists Jeung Sang Lee of Korea as an inventor. Lee is a Korean application filed on August 27, 1994. On March 22, 1996, in accordance with its patent laws (Ex. 1108), the Korean Patent Office published in the Patent Gazette for "publication" KR Patent Pub. No. 1996-0009001 (Ex. 1112), providing information on: 1) the applicant; 2) the application number, classification code and filing date; 3) the inventor; 4) application publication number and date of publication; ***5) title of invention; 6) scope of***

***patent claims; 7) drawings;*** 8) priority claims; ***9) summary;*** and 7) other matters for the Lee application. By providing a publication of the title, claims, drawing, and summary of the invention of the Lee application, anyone can search and inspect the full Lee application. *See id.* In *In re Wyer*, 655 F.2d 221 (CCPA 1981), the Court determined that a very similar Australian process for publishing an abstract serves as an index, or roadmap to a POSITA to go find the underlying specification, and therefore a foreign procedure for "laying open for public inspection" can serve as 102(b) prior art. *See also* MPEP 901.05 II.C. Lee is thus prior art to the '902 patent under 35 U.S.C. § 102(a) as of March 22, 1996 and was not before the examiner during prosecution of the '902 patent. *See* http://www.uspto.gov/web/offices/pac/mpep/s2132.html (printed publication satisfies "known or used" prong of 35 U.S.C. § 102(a)).

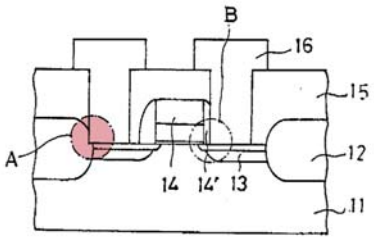
Lee discloses a method for fabricating an improved semiconductor device with an etch stop layer for improving the alignment margin when forming a contact hole. Lee Decl. at ¶ 40. Lee teaches in annotated Figure 1 below that in the prior art, a structure is formed by isolating an active region (green) with a field oxide layer **12** (blue) on a field region (brown) on a semiconductor substrate **11**, and patterning a gate **14** on the substrate. Lee at 17-2. A gate sidewall **14'** (purple) is formed on the gate using a deposition and etch-back process. *Id.* An interlayer insulation film **15** is deposited on top of the substrate and over the gate. Then, a

contact hole that opens the source and drain region is formed through etching an interlayer insulation film **15**:

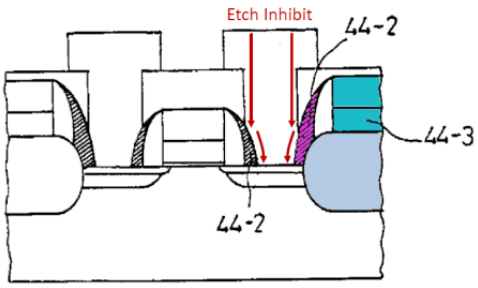



Lee at Fig. 1. The process is completed by depositing a conductive layer **16** into the contact hole to form the contact. *Id.* at 17-2.

Lee recognized that the prior art method depended on the alignment accuracy of a photolithography process. *Id.* In the case of misalignment, the field oxide layer may be damaged, as shown in area A of annotated Fig. 1(b):




Such damage becomes the cause of junction leakage. *Id.* at 17-2. To address this problem, Lee discloses a method of forming an etch stop layer around the source and drain region by depositing and etching back a spacer having a high etch selectivity **44-2** along the sidewalls of both an active gate and a gate **44-3** on a field oxide layer, as shown in annotated Fig. 4:



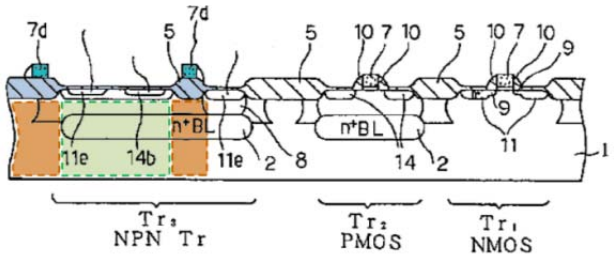

*Id.* at Fig. 4. Lee discloses that the etch stop layers 44-2 are "in the form of a sidewall" and formed using the same process discussed by Lee to form a sidewall on the gate, by deposition and conducting etch-back. *Id.* at 17-5; *see* 17-2 ("forming a gate sidewall (14') using a deposition and etch-back process"). Lee discloses that the gate 44-3 serving as an etch inhibiting layer may be an adjacent internal connection line or a "dummy pattern."

**B. JP Pub. No. H7-86158 ("Yasushige")**

Claim 1 of the '902 patent describes the use of a "dummy pattern" to serve as an etch inhibiting layer. While a POSITA would understand that Lee discloses that the dummy pattern is electrically isolated from the substrate and circuits thereon, Lee does not explicitly use the term "electrically isolated." Lee Decl. at ¶ 43. However, the patent application publication, JP Pub. No. H7-86158 (Ex. 1109, "Yasushige") discloses a dummy pattern and explicitly states that it is "electrically isolated" to solve the same problems of etching that Lee addressed. While Yasushige does not explicitly disclose a first patterned layer on an adjacent active region, the dummy pattern disclosed by Yasushige is formed on a field isolation

layer, and serves as an etch stopper when etching an insulation layer formed over the substrate. The dummy pattern, made of a conductive film, serves in part to protect other insulation layers on the substrate, during an etch. Lee Decl. at ¶ 43. Yasushige was filed by Sony Corporation almost three and a half years prior to the filing date of the earliest parent application of the '902 patent, on June 30, 1993. It is titled "BICMOS Semiconductor Device and Manufacturing Method Thereof" and lists Hiroaki Yasushige and Norikazu Ouchi of Sony Corporation in Tokyo, Japan as inventors. Yasushige was published on March 31, 1995 and is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

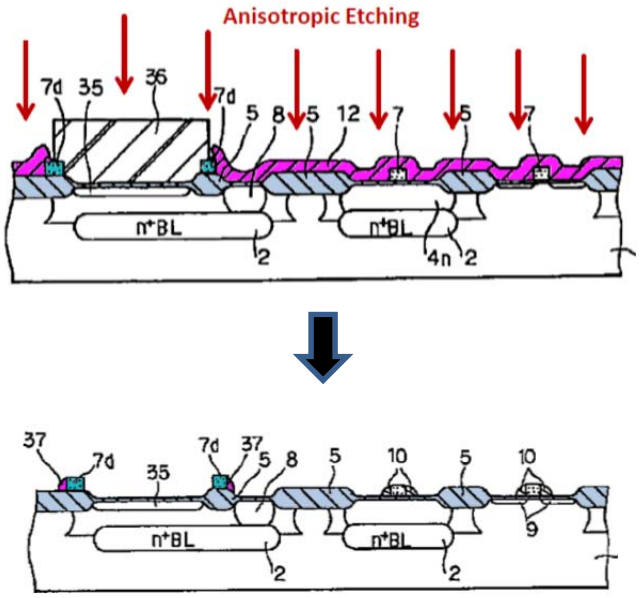
Yasushige discloses a technique for forming a dummy pattern **7d** around the base region of a semiconductor device, as shown in annotated Fig. 1:




The dummy pattern **7d** is "identical" and formed "simultaneously" to the gate electrode **7** on the active region. Yasushige at ¶¶ 31, 41. Both dummy pattern and active gate electrode are made of a conductive material, poly Si film doped with phosphorus. *Id.* at ¶ 44. The dummy pattern is "formed around the base region

**14b** of the bipolar transistor Tr3" on a field oxide layer made of an SiO2 film **5** and "***electrically isolated***."[1] *Id.* at ¶ 29. As was known in the field, ion implantation is carried out on the base region to form diffused active regions. *Id.* at ¶ 42.

Yasushige recognized that during an etching process of an insulation film **12**, a mask alignment shift may cause damage to a field oxide region **5**, unless a dummy pattern protects the field oxide region. *Id.* at ¶ 50. As shown in annotated Fig. 6 to Fig. 7, the insulation film **12** is etched by performing an anisotropic etching process over the entire surface, where the dummy patterns protect the field oxide region **5**. *Id.* at ¶ 49.

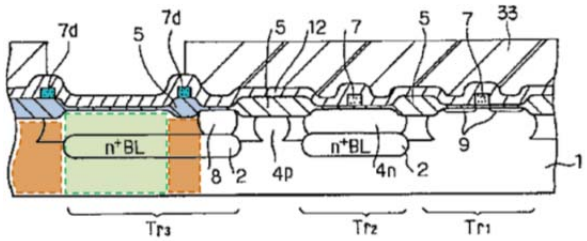



Without the dummy patterns, such over-etching would cause damage to the field oxide region 5, leading to an increase of the leakage current in the substrate. *Id.* at

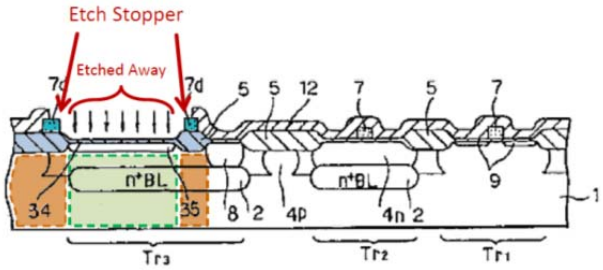
[1] All emphasis added unless otherwise indicated.

¶ 50, 53; *see also id.* at ¶ 46.

Yasushige further discloses that the dummy pattern **7d** can serve as an etch stopper when an insulating film of the base region is removed by wet etching. Like Lee, Yasushige recognizes that a dummy pattern provides good etch selectivity against insulation layers formed on the substrate. As shown in annotated Fig. 4, a resist pattern 33 is set up first over the substrate with an opening to the base region:




Then, a wet etching process is used to remove the insulating film **12**, as shown in annotated Fig. 5:




In Fig. 5, the the dummy pattern stops the etch. *Id.* at 46.

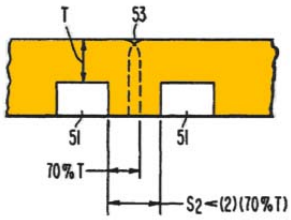
### C. U.S. Patent 4,916,514 ("Nowak")

The '902 patent describes the use of an insulating layer comprising nitride. While Lee discloses an insulating layer, Lee does not explicitly disclose that the

insulating layer comprises nitride, as recited in dependent claims 2 and 17. However, this is an obvious design choice, as there are limited options in semiconductor fabrication for insulating materials (mainly oxides or nitrides). Lee Decl. at ¶ 48. Further, the well-known use of silicon nitride or oxynitride as the material for the insulation layer is disclosed by Unisys Corporation in U.S. Patent No. 4,916,514 (Ex. 1110, "Nowak"), listing Matthew Nowak as an inventor and titled "Integrated Circuit Employing Dummy Conductors for Planarity." Nowak was filed on May 31, 1988 and issued on April 10, 1990, more than six years prior to the filing date of the earliest parent application of the '902 patent. Nowak is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

While Nowak does not explicitly disclose the specific configuration of forming a contact hole between a dummy conductor and a gate on an active region like the '902 patent, Nowak discloses forming electrically isolated dummy conductors on an insulating layer on a substrate. Nowak at 3:18-22. The dummy conductors are made of the same material, patterned with the same mask, and are formed by the same fabrication steps as signal conductors on the substrate. *Id.* at 2:59-66. The dummy conductors have no electrical function, and thus are "open circuited" and carry no signals. *Id.* at 3:1-3, Abstract. Nowak further discloses that a layer of insulating material, such as silicon nitride or oxynitride, is "used to

cover the dummy conductors" and form conformally over the substrate, as shown in annotated Fig. 5B:




*Id.* at 3:65-4:2.

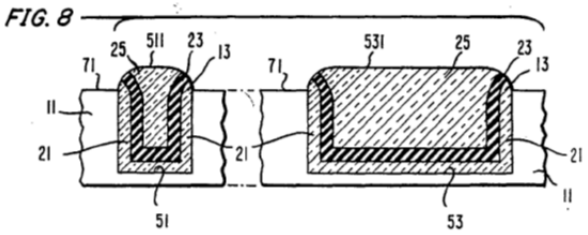
**D. U.S. Patent 4,952,524 ("the '524 Patent")**

The '902 Patent describes the use of a field oxide layer formed in a trench of the substrate and recites this limitation in claims 6 and 13. While Lee does not explicitly use the word "trench," a POSITA would understand that the disclosure in Lee may include a trench field oxide layer. Lee Decl. at ¶ 51. Further, this is an obvious design choice, and is explicitly disclosed by AT&T Bell Labs in U.S. Patent No. 4,952,524 (Ex. 1111, "the '524 Patent"), listing Kuo-Hua Lee and Chih-Yuan Lu as inventors and titled "Semiconductor Device Manufacture Including Trench Formation." Lee Decl. at ¶ 51. The '524 Patent was filed on May 5, 1989 and issued on Aug. 28, 1990, six years prior to the filing date of the earliest parent application of the '902 patent. The '524 Patent is thus prior art to the '902 patent under 35 U.S.C. § 102(b) and was not before the examiner during prosecution of the '902 patent.

While it does not discuss the use of a dummy gate as an etch inhibitor, the

'524 Patent discloses a method for forming an improved trench isolation layer in a semiconductor substrate. The '524 Patent discloses using "trenches for inter-device isolation." '524 Patent at 1:9. Traditionally, "trench isolation involves etching a narrow, deep trench or groove in a silicon substrate and then filling the trench with a filler material such as a silicon oxide or polysilicon." *Id.* at 1:24-25. The '524 Patent discloses both a "narrow trench" and a "wide trench." *Id.* at 2:60-61, Figs. 7-9. It further discloses at least one specific etching recipe for forming a trench. *Id.* at 3:30-38. Then, trenches may be filled with multiple layers, "an exemplary candidate for filler layer 25 is an oxide." *Id.* at 4:28-29.

These techniques result in oxide-filled trenches with upper surfaces that protrude somewhat beyond the upper surface of the substrate:




'524 Patent at Fig. 8, 6:6-8. Fig. 8 shows a narrow trench **51** and a wide trench **53**. The '524 Patent further discloses trenches with slanted sidewalls, as a technique known to a POSITA. *Id.* at 7:29-31.

## VII. MOTIVATIONS TO COMBINE THE PRIOR ART REFERENCES

### A. Motivation To Combine Lee with Yasushige

A POSITA would have been motivated to combine the teachings of Lee and

Yasushige to achieve the methods claimed in the ’902 patent. Lee Decl. at ¶ 55.

**1. Same Technology**

A POSITA would have been motivated to combine Lee with Yasushige because both Lee and Yasushige are directed to forming etch stoppers on field oxide regions surrounding an active region on a semiconductor substrate. In particular, as shown above, both patents disclose forming dummy pattern structures on a field oxide layer. Both Lee and Yasushige recognize that dummy patterns provide good etch selectivity against the insulation layers formed on the substrate, and particularly as a barrier to protect other insulating layers on the substrate from the etch, such as underlying field oxide regions. Both patents teach that the dummy pattern structures are identical to adjacent MOS gate transistors. Both patents further discuss the other processes for forming structures for an electronic device, such as ion implantation on the active region, forming patterned conductive gates, forming gate sidewalls using an anisotropic etching process, and depositing an interlayer insulating film. Lee Decl. at ¶ 56.

**2. Same Problem**

Both Lee and Yasushige use dummy patterns to solve the problem of a misalignment in an etching process resulting in over-etching of an insulating layer and causing damage to a field oxide layer. Lee at 17-2; Yasushige at 50 (“The case where there is no dummy pattern 7d is considered . . . the SiO2 film 5 of the field

is shaved at the time of anisotropic etching."). In both Lee and Yasushige, the dummy patterns are used as etch stoppers for etching an insulating layer formed on the substrate. Lee disclosed that damage to the field oxide layer from etching "becomes the cause of junction leakage." Lee at 17-2. Yasushige recognized that etching could shave the field oxide region (Yasushige at 50), leading to damage that could result in "problems such as an increase in the leakage current." Yasushige at ¶ 53. Lee Decl. at ¶ 57.

While Lee discloses an etch stop layer on a dummy pattern, Yasushige also discloses using dummy patterns on field oxide layers to serve as an etch stopper around a base, or active, region, and protecting a field oxide layer. Yasushige at ¶¶ 45, 46, 49, 50. A POSITA would have recognized that Lee and Yasushige were solving a common problem and been motivated to combine the teachings of forming a dummy pattern as an etch stopper. Lee Decl. at ¶ 58. Based on the similar concern over damage from etching insulation layers, a POSITA would have looked to combine Lee with the teaching from Yasushige so as to ensure that the dummy pattern is electrically isolated on a field oxide region. *Id.* Since the dummy pattern is intended to protect against an etch on insulation layers, a POSITA knew to position the dummy pattern completely over other insulation layers, such as a field oxide layer, for best coverage. *Id.* Further, a POSITA understood that keeping the dummy pattern electrically isolated ensures that the

dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern. *Id.* A POSITA would have been motivated to keep the dummy pattern electrically isolated, given that its sole function is for a mechanical purpose as an etch stop, and avoid adding additional electrical connections to the subtrate that are unnecessary. *Id.*

**3. Nothing Incompatible**

Nothing in these prior references teaches away from their combination. There is no essential feature in any of these references that conflicts with an essential feature of any other reference. To the contrary, these references are a natural fit, as evidenced by both Lee and Yasushige teaching the use of a dummy pattern on a field oxide layer to serve as an etch stop for an etching process. Many aspects of forming gates and transistors on a semiconductor substrate were well-known to a POSITA, and Lee and Yasushige use many of the same techniques, e.g., ion implantation, patterning gates, anisotropic etching. Lee Decl. at ¶ 59.

**4. Additional Reasons to Combine**

There were additional reasons to combine Lee and Yasushige. As discussed in the ’902 Patent, devices were becoming more integrated, reducing the space available on a substrate. Lee Decl. at ¶ 60. Thus, there is less room for error in the process steps of semiconductor manufacturing. *Id.*

Members of the semiconductor field were constantly looking for ways to make circuits smaller. *Id.* at ¶ 61. Both Lee and Yasushige teach methods of manufacturing intended to both increase the margin for error while not introducing extra process steps. *Id.* For example, both Lee and Yasushige use dummy patterns that are identical and simultaneously created with the active gates, thus not requiring extra deposition or patterning steps. *Id.* Lee discloses that because etch stop spacers are "formed through self-alignment without a separate mask, there is no additional process." Lee at 17-7. And as discussed above, both Lee and Yasushige focus on solving issues of misalignment, and improving room for error. Lee Decl. at ¶ 61. Especially in this field, a POSITA would have been motivated to combine Lee and Yasushige to attempt to improve the manufacturing process. *Id.*

### B. Motivation To Combine Lee and Yasushige with Nowak

A POSITA would have been motivated to combine the teachings of Lee and Yasushige with Nowak in the manner described above for several reasons.

A POSITA would have been motivated to look to Nowak for details regarding the semiconductor fabrication processes disclosed in Lee and Yasushige. All three of these references disclose a technology for forming well-known structures, such as gates, field isolation layers, and insulation layers on a semiconductor substrate. Lee, Yasushige, and Nowak all teach methods of

forming electrically isolated dummy patterns on a substrate to perform mechanical functions.

While all three references disclose a method for fabricating a semiconductor device, and describe similar structures and fabrication techniques, each reference provides different levels of details, which are well known to a POSITA. For example, Nowak discloses forming an insulation layer over dummy conductors, similar to Lee and Yasushige, but describes the well-known use of silicon nitride or oxynitride as the material for the insulation layer, which is claimed in dependent claims 2 and 17. Lee Decl. at ¶ 64.

Nothing in these prior references teaches away from their combination. There is no essential feature in any of these references that conflicts with an essential feature of any other reference. To the contrary, these references are a natural fit, as evidenced by all three of the references, Lee, Yasushige, and Nowak teaching the use of electrically isolated dummy patterns formed on insulation layers to perform mechanical functions.

### C. Motivation To Combine Lee, Yasushige, and the ’524 Patent

A POSITA would have been motivated to combine the teachings of Lee, Yasushige, and the ’524 Patent in the manner described above for several reasons. A POSITA would have been motivated to look to the ’524 Patent for details regarding the semiconductor fabrication processes disclosed in Lee and Yasushige.

All three of these references disclose a technology for forming well-known structures, such as gates, field isolation layers, and insulation layers on a semiconductor substrate. Lee and Yasushige both teach methods of forming electrically isolated dummy patterns on a substrate to perform mechanical functions. The ’524 patent describes in detail the insulation layers formed over the dummy patterns.

The ’524 Patent discloses forming trench isolation layers, to provide electrical isolation for active regions on a substrate. It was well known to a POSITA to use either a LOCOS method or trench isolation method to form a field oxide layer. Lee Decl. at ¶ 68. Moreover, the benefits and drawbacks of LOCOS and trench isolation were well known to a POSITA. *Id.* As discussed in the ’524 Patent for the prior art, a LOCOS method for growing a field oxide layer would often result in encroachment of the oxide layer onto the active region. While Lee discloses the formation of a field oxide layer, Lee does not explicitly disclose the method. *Id.* However, a POSITA would know that the issue described in Lee—increasing margin of error for forming a contact hole over a field oxide layer—would benefit from using a trench isolation technique that decreased the area used by the field oxide layer. *Id.* Accordingly, a POSITA certainly would have been motivated to combine Lee with the teaching of a trench isolation layer in the ’524 Patent. *Id.*

Nothing in these prior references teaches away from their combination. Lee is a natural fit with the teaching of a trench isolation layer in the '524 Patent. For example, while Lee teaches the formation of an etch stop layer on the side of a field oxide layer, Lee appears to contemplate that the field oxide layer may be formed in a trench with a lower protrusion—thus having insufficient "step" to form the etch stop layer (Lee at 17-6)—and proposes an embodiment where a dummy pattern formed on the trench serves as the "step" for the etch stop layer to be formed. Lee Decl. at ¶ 69.

## VIII. CLAIM CONSTRUCTIONS

Petitioner provides below a construction, under the broadest reasonable construction standard, of claim terms "insulating spacer along a sidewall of the [second] patterned conductive layer," "an insulating layer," and "forming a trench in said substrate, and wherein said field isolation layer fills said trench." Petitioner reserves the right to propose alternate or additional constructions in any other proceedings, where the standard may differ.

### A. "insulating spacer along a sidewall of the [second] patterned conductive layer"

The term "insulating spacer along a sidewall of the [second] patterned conductive layer" is used in challenged independent claims 1, 11, 12, 15, and 18.

A POSITA would have generally understood "insulating spacer along a sidewall of the [second] patterned conductive layer," in light of the specification,

to mean "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." Lee Decl. at ¶ 74. The specification describes the "present invention" to "allow[] the misalignment of the contact hole without damaging the field isolation layer." *Id.* at 2:49-54, *see also id.* at 3:44-48 ("The methods and structures of the present invention thus provide protection for the field isolation layer during the formation of a contact hole.") Further, in "the present invention" (*Id.* at 4:62-64) "a contact hole can thus be self-aligned using the spacers 46 and 46a," (*Id.* at 5:26-32) as illustrated in Fig. 8.

As discussed in Section IV.C, the specification is confirmed by the prosecution history, where the Applicant distinguished prior art that did not "suggest[] that there is need to include spacers that would prevent damage to the field oxide layer in the event the contact hole is misaligned," and the Examiner agreed and re-stated this understanding in the Reasons for Allowance. (Ex. 1102, 3/5/2001 Amendment, p. 9; 5/2/2001 Reasons for Allowance, p. 2.)

Accordingly, the broadest reasonable construction of the term "insulating spacer along a sidewall of the [second] patterned conductive layer" is, consistent with the specification, "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." Lee Decl. at ¶ 76.

### B. "an insulating layer"

This term has a plain and ordinary meaning and does not require construction. In the District Court Action, patent owner Samsung has taken the position that the term "an insulating layer" should be construed to mean "a structure comprising one or more electrically insulating sublayers." (Ex. 1115 at 2.) As explained further below, the prior art relied upon in this petition meets Samsung's proposed construction of this term in the District Court Action. Lee Decl. at ¶ 77.

### C. "forming a trench in said substrate, and wherein said field isolation layer fills said trench"

This term has a plain and ordinary meaning and does not require construction. In the District Court Action, patent owner Samsung has taken the position that the term "forming a trench in said substrate, and wherein said field isolation layer fills said trench" should be construed to mean "etching a recess into said substrate and subsequently filling said recess with a field isolation layer." (Ex. 1115 at 2.) As explained further below, the prior art relied upon in this declaration meets Samsung's proposed construction of this term in the District Court Action. Lee Decl. at ¶ 78.

## IX. PRECISE REASONS FOR THE RELIEF REQUESTED

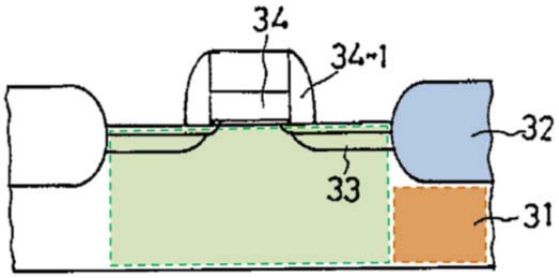
### A. Ground 1: Claims 1, 3-5, 7-12, 14-16, and 18 are rendered obvious by Lee and Yasushige.

**Claim 1: [1pre] "A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:"**

To the extent the preamble is a limitation, Lee discloses this limitation. Lee discloses "[a] method for fabricating a semiconductor device, and specifically pertains to a method for fabricating semiconductor device, in which the characteristics of the device are improved by securing an align margin upon formation of the contact hole." Lee at 17-1.

**[1a] "defining adjacent active and field regions on a substrate, and circuits thereon;"**

In the '902 patent, an active region is defined by forming a field isolation layer, such as an oxide layer, on a field region of the substrate. '902 patent at 4:11-16 ("Portions of the substrate not covered by the field isolation layer ***define the active region*** where microelectronic devices will be formed."). Lee discloses "defining adjacent active and field regions on a substrate." Lee discloses "an active region is ***isolated electrically from the surrounding active regions by forming a field oxide layer*** (32) on a semiconductor substrate (31)" as shown in annotated Fig. 3(a):

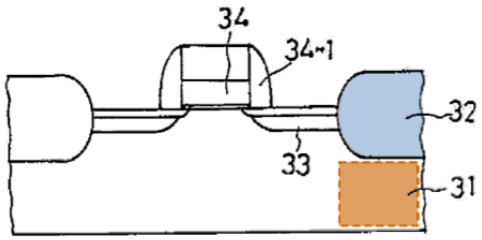


Lee at 17-5, Fig. 3(a). The active region (green) is adjacent the field oxide layer 32 (blue). A POSITA understands that the field region (brown) is then defined by the area of the substrate where field oxide layer 32 is formed. Lee Decl. at ¶ 86.

Lee further discloses defining "circuits thereon." A junction contact is formed with a conductive layer **36** composed of conductive material. Lee at 17-6, Fig. 3(d). A POSITA understands that a circuit is defined by forming a transistor and junction contacts. Lee Decl. at ¶ 87.

**[1b] "forming a field isolation layer on said field region;"**

Lee discloses "an active region is ***isolated electrically from the surrounding active regions by forming a field oxide layer*** (32) on a semiconductor substrate (31)." as shown in annotated Fig. 3(a):

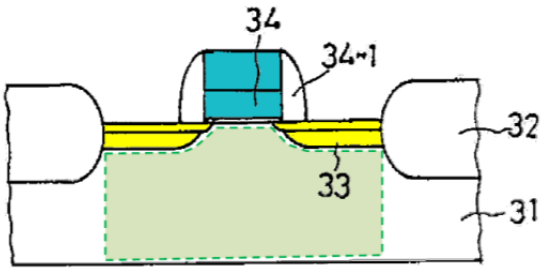



Lee at 17-5, Fig. 3(a). The field oxide layer 32 is on the field region (shaded brown) of the substrate **31** and is a field isolation layer.

**[1c] "forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;"**

Lee discloses "an ***active region*** is isolated electrically from the surrounding active regions by forming a field oxide layer (32) on a semiconductor substrate

(31), and an ***MOS gate (34)*** is formed by ***depositing and etching*** gate oxide layer, ***poly*** and gate cap in order" as shown in annotated Fig. 3(a):

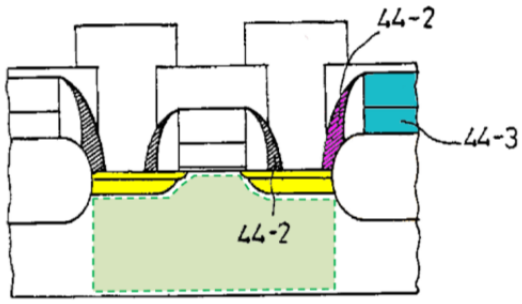



Lee at 17-5, Fig. 3(a). Lee's disclosure of depositing layers and etching the layers discloses forming a "patterned" layer. *Id.* at 17-5. The "poly" layer is understood by a POSITA to be a conductive polysilicon layer. Lee Decl. at ¶ 89. As further shown in Lee at Fig. 3(a), the MOS gate is formed on the active region (shaded green) separated from the field oxide layer **32**. It would have been a natural design choice for the MOS gate to be formed entirely on the active region, and spaced apart from the field region (shaded brown) defined by the field oxide layer **32**. *Id.* at ¶ 90.

**[1d] "forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate,"**

Lee discloses forming an etch stop layer by "depositing a material having a high etch selectivity with an interlayer insulation film." Lee at 17-5. "[T]he etch stop layer is formed with a conductive or non-conductive material." *Id.* at 17-6. Fig. 4 shows that the etch stop layer is formed on the field isolation layer as a spacer (44-2) on the sidewall of a dummy pattern (44-3), and is adjacent to the

active region:



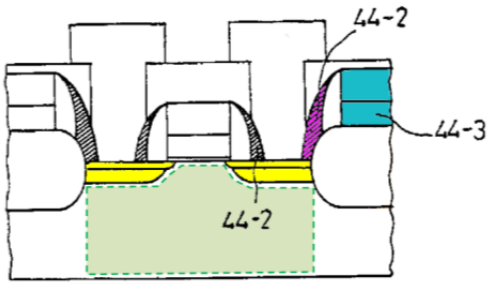

*Id.* at annotated Fig. 4, 17-6.

Lee further confirms that the "etch stop layer" of the contact etching process is "***formed around the impurity region*** in the form of a sidewall." *Id.* at 17-5. Lee discloses that a high concentration impurity region is formed in the active region to make a source and drain region (33). Lee at Fig. 3(a), 17-5; *see also* 17-4 ("making a source and drain region which is formed by doping impurity on the gate in the active region on a semiconductor substrate and the substrate around the gate"). Thus the etch stop layer is formed ***around*** the active region, or the impurity region, and since it is formed along the side of the dummy pattern, accordingly the dummy pattern and the etch stop layer formed on it are adjacent to the active region. Lee Decl. at ¶ 93.

> **[1e] "the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer,"**

As discussed in element [1c], Lee discloses that the active region includes

the first patterned conductive layer. Lee further discloses that said etch inhibiting layer comprises a second patterned conductive layer. In Fig. 4, the etch stop layer (44-2) is formed using "an internal connection line (44-3) passing adjacently or the step of a ***dummy pattern***":




Lee at Fig. 4 (annotated), 17-6. As shown in Fig. 4, the etch inhibiting layer comprises a second patterned conductive layer (44-3), that may be a dummy pattern. Lee Decl. at ¶ 95.

Lee also discloses an insulating spacer along a sidewall of the second patterned conductive layer. As discussed above, "an insulating spacer along a sidewall of the second patterned conductive layer" should be construed as "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." The analysis below is not impacted under Samsung's construction proffered in district court for this limitation. As shown above in annotated Fig. 4, Lee discloses forming the etch stop layer **44-2** as a spacer along a sidewall of the second patterned conductive layer (**44-3**). Lee Decl. at ¶ 97. The etch stop layer is formed

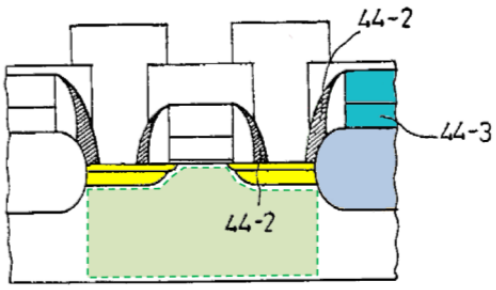
with a "non-conductive material," and is thus an insulating layer. Lee at 17-6; Lee Decl. at ¶ 97. Lee teaches that "a process alignment margin is secured when forming a contact hole by forming an etch stop layer on the contact hole area to protect the lower insulating layer," (Lee at 17-4), and as further shown in Fig. 4, etch stop layer 44-2 prevents etch damage to the field isolation layer if the contact hole is misaligned. Lee Decl. at ¶ 97.

The etch stop layer 44-2 in Lee is identical in structure to the insulating spacer formed along a sidewall of the patterned conductive layer 44-3, and is formed right next to a first insulating spacer. *Id.* at ¶ 98. Lee discloses that the etch stop layer (44-2) is formed in the "form of a sidewall" and using the same "deposition and etch-back" process for making a sidewall. Lee at 17-6. The deposition and etch-back process is the same process for making an insulating sidewall spacer disclosed by Lee. *Id.* at 17-5 ("forming a gate sidewall (34-1) using a deposition and etch-back process"); Lee Decl. at ¶ 98. Thus, Lee's disclosure of the etch stop layer 44-2 formed on the dummy pattern 44-3 meets the limitation "an insulating spacer along a sidewall of the second patterned conductive layer." Lee Decl. at ¶ 98.

**[1f] "wherein the second patterned conductive layer does not extend over the active region of the substrate,"**

Lee discloses that the second patterned conductive layer does not extend over the active region of the substrate. For example, Lee discloses that a high

concentration impurity region is formed in the active region to make a source and drain region (33). Lee at Fig. 3(a), 17-6. In Fig. 4 the conductive pattern (44-3) is formed on the field isolation layer, and is adjacent to the active region (highlighted green):




*Id.* at Fig. 4, 17-6. Lee further confirms that the etch stop layer **44-2** of the contact etching process is "formed ***around the impurity region*** in the form of a sidewall." *Id.* at 17-5. Because the etch stop layer is formed around the active, or impurity, region, and is thus sitting on the border of the active and field regions as shown in Fig. 4, the second patterned conductive layer inside the etch stop layer is formed is formed entirely on the field isolation layer and does not extend over the active region of the substrate. Lee Decl. at ¶ 99.

As further discussed in Lee, the etch stop layer is intended to protect the field oxide layer when forming a contact hole. Lee at Fig. 1(b), 17-2. Fig. 1(b) shows that a misalignment in the photolithography process to form a contact hole may cause damage to the field oxide layer and result in junction leakage. *Id.* Accordingly, based at least on Lee's disclosures that 1) the etch stop layer 44-2 is

formed ***around*** the active region; 2) the etch stop layer protects the edge of the field oxide layer from damage in a contact hole formation process; and 3) the etch stop layer is formed along the sidewall of the second patterned conductive layer, as shown in Fig. 4 and further discussed in element 1[e], a POSITA would know that the second patterned conductive layer does not extend over the active region of the substrate. Lee Decl. at ¶ 100.

To the extent that this limitation of "the second patterned conductive layer does not extend over the active region of the substrate" is not explicitly disclosed in Lee, this limitation is obvious based on Lee in view of Yasushige. Yasushige explicitly discloses a dummy pattern that is "electrically isolated from the base region by an isolation region," and thus the dummy pattern does not extend to the active region. Yasushige at Fig. 1 (base region 14b corresponds to active region), 29, 41; Lee Decl. at ¶ 101. A POSITA would have combined the teaching in Lee of a dummy pattern used as an etch inhibiting layer, with the explicit disclosure in Yasushige that such a dummy pattern does not extend to the active region, to meet the claim limitation. Lee Decl. at ¶ 101. In addition to the reasons to combine Lee and Yasushige discussed above in Section VII.A, for a dummy pattern that serves as the "step" for forming an etch stop layer to protect the edge of the field oxide layer, as discussed in Lee, positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole

formation process. *Id.* A POSITA would have been motivated to combine Lee with Yasushige's teaching to ***not*** form the dummy pattern extending into the active region, so that there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes. *Id.* The semiconductor industry is constantly focused on developing smaller dimensions, and it would be beneficial to actively avoid forming nonfunctional dummy patterns onto an active region. *Id.* Accordingly, Lee in view of Yasushige renders this limitation obvious.

**[1g] "and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;"**

Lee discloses and makes obvious that "the second patterned conductive layer is a dummy pattern." Lee contemplates in one embodiment illustrated in Fig. 4 that the etch stop layer may be formed as a spacer along an "internal connection line passing adjacently" ***or*** a "dummy pattern." Fig. 4, 17-6. Fig. 4 shows that dummy pattern 44-3 has identical structure to the first patterned conductive layer on the active region. Lee Decl. at ¶ 102. A POSITA would know as a matter of design choice that the dummy "pattern" is formed from depositing the same materials, gate oxide layer, poly, and gate cap layers in a sequence and patterning, as disclosed by Lee. Lee at 17-2; Lee Decl. at ¶ 102. The term "pattern" also conveys to one of skill in the art that the dummy pattern was formed in the same

masking process as the first patterned conductive layer. Lee Decl. at ¶ 102. Accordingly, the dummy pattern is also a "conductive layer," as it is made of the same conductive poly material as the first patterned conductive layer. *Id.*

Lee discloses that the dummy pattern is "electrically isolated from the substrate and circuits thereon." First, as disclosed in element 1[f], the dummy pattern does not extend over the active region of the substrate. It is thus electrically isolated over the field oxide layer, similar to the disclosure of "electrically isolated" in the '902 patent. *See* '902 patent at 5:43-45 ("the second patterned conductive layer is preferably electrically isolated over the field region"); Lee Decl. at ¶ 103.

In addition, Lee explicitly contemplates two embodiments—one where the conductive pattern is an "internal connection line" and the other where the conductive pattern is a "dummy pattern." Lee Decl. at ¶ 104. Lee's contemplation of alternative embodiments where one has connections is further confirmation to a POSITA that the dummy pattern embodiment does not have electrical connections. *Id.* For example, Lee teaches that where an internal connection line is not conveniently located to form the etch stop layer on the field oxide layer, a dummy pattern may be created to serve this mechanical function. *Id.* While other mechanical structures are possible, forming a gate pattern is most efficient given the already existing patterning process for gates throughout the chip. *Id.* And

where a dummy pattern was created for the purpose of serving as a step for forming the etch stop layer, a POSITA would know that keeping the mechanical structure electrically isolated is the best and most efficient practice to prevent accidental electrical connections or shorting damage. *Id.*

A POSITA would understand that a dummy pattern is a gate pattern that performs no electrical function, as confirmed by contemporary electrical engineering and microelectronics dictionaries for the term "dummy"[2]:

> "dummy": "Pertaining to a nonfunctioning item used to satisfy some format or logic requirement or to fulfill prescribed conditions." (Ex. 1114, p. 322.)
>
> "dummy connector plug": "A part included in the total design of a connector to mate with a connector but not to perform an electrical function." (Ex. 1113, p. 61.)

Lee Decl. at ¶ 105. As recognized in the '902 patent, an electrically isolated conductive pattern serves no electrical function. '902 patent at 6:20-23. Thus, Lee discloses forming a dummy pattern, on an isolation layer, which is electrically

[2] Nowak (Ex. 1110) also provides background on dummy conductors and their electrical isolation: "[T]he integrated circuit further includes dummy conductors on the insulating layers in the spaces between the signal conductors. ***These dummy conductors are open circuited, and thus they carry no signals.*** Their function is purely mechanical." 2:13-22.

isolated from the substrate and circuits.

However, to the extent that this limitation of "the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon" is not explicitly disclosed in Lee, this limitation is obvious based on Lee in view of Yasushige. Yasushige explicitly discloses a dummy pattern that is "electrically isolated." Yasushige at 29, 41. A POSITA would have combined the teaching in Lee of a dummy pattern used as an etch inhibiting layer, with the explicit disclosure in Yasushige that such a dummy pattern used as an etch inhibiting layer is electrically isolated, to meet the claim limitation "wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon." Lee Decl. at ¶ 106.

A POSITA would have been motivated to combine the teaching of a dummy pattern in Lee with the teaching in Yasushige that the dummy pattern is electrically isolated from the substrate and circuits, for the reasons stated in Section VII.A. In addition, Lee and Yasuhige disclose similar structure and positioning of the dummy pattern, indicating a shared intent to electrically isolate the dummy pattern from the substrate and circuits. Lee Decl. at ¶ 107. Both Lee and Yasushige disclose that the etch stopper was formed ***on*** a field oxide layer and ***around*** the active region. *See* Lee at 17-5 ("an etch stop layer . . . is formed around the impurity region"); Yasushige ("a conductive film 7d . . . is formed around the base

region of the bipolar transistor").

Further, A POSITA would have recognized that Yasushige's teaching of electrically isolating the dummy pattern on a field oxide layer would improve the functionality of Lee's disclosure of the dummy pattern and etch stop layer along its sidewall. Lee Decl. at ¶ 108. First, positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole formation process. *Id.* By not positioning the dummy pattern on the active region itself, there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes. *Id.* Second, keeping the dummy pattern electrically isolated ensures that the dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern. *Id.* A POSITA would have recognized these benefits of Yasushige's teaching of electrical isolation of the dummy pattern on the field oxide layer, and applied those teachings to Lee. *Id.*

Thus, given the identical disclosure of function, structure, and positioning on an isolation layer around an active region, of the dummy pattern, a POSITA would have either understood that the disclosure of a dummy pattern in Lee comprises a dummy pattern that is electrically isolated from the substrate and circuits, as explicitly disclosed in Yasushige, or would have been highly motivated to design

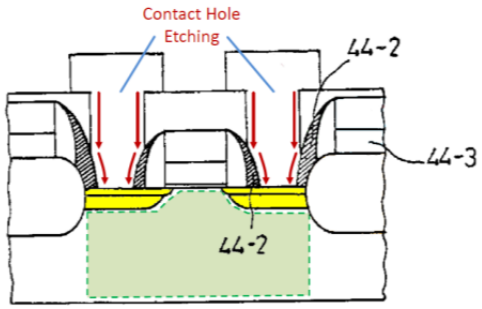
the dummy pattern in Lee so that it was electrically isolated from the substrate and circuits, as disclosed in Yasushige. *Id.*

**[1h] "forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer;"**

Lee discloses that "a contact hole is formed by depositing an interlayer insulation film (**35**) and etching the interlayer insulation film." Lee at Fig. 3(c), 17-6. Lee further discloses that the interlayer insulating film is deposited "on the following transistor." *Id.* at 17-2. As further shown in Fig. 4, the interlayer insulating film is also formed on the etch stop layer and dummy pattern, and the field isolation layer. The analysis does not change under Samsung's construction proffered in district court for this limitation.

**[1i] "forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer."**

Lee discloses that "a contact hole that ***opens the source and drain region*** is formed by depositing an interlayer insulation film (15) on the following transistor and etching the interlayer insulation film." Lee at 17-2. Lee thus discloses that the contact hole exposes a portion of said active region. As further shown in annotated Fig. 4, the contact hole is formed between the first patterned conductive layer on the active region (yellow source/drain region on green active region) and the etch inhibiting layer, comprising the etch stop layer and dummy pattern:




Therefore, for the reasons set forth above, I find that all elements of claim 1 are rendered obvious by Lee in combination with Yasushige.

> **<u>Claim 3</u>: "A method according to claim 1 wherein said first patterned conductive layer comprises a conductive portion and insulating spacers along sidewalls thereof."**

As discussed in Claim 1(c), Lee discloses a first patterned conductive layer formed on an active region and a conductive portion comprising a "poly" layer. Lee further discloses "forming a gate sidewall (34-1) using a deposition and etch-back process," which meets the limitation of a spacer, and as shown in Fig. 3(a) is formed along the sidewall of the first patterned conductive layer. Lee further discloses that the gate sidewall is an "oxide layer." Lee at 17-6 (". . . oxide layers on the substrate (field oxide layer, ***gate sidewall***, cap oxide layer . . .)"). A POSITA understands that an oxide layer is an insulating material. Lee Decl. at ¶ 113.

Lee further discloses forming an etch stop layer **44-2** on the first patterned conductive layer, as shown in Fig. 4. As discussed in Claim 1(e), etch stop layer 44-2 on the second patterned conductive layer is an insulating spacer along a

sidewall, and for the same reasons the etch stop layer 44-2 on the first patterned conductive layer is an insulating spacer along a sidewall. *Id.* at ¶ 114. As shown in Fig. 4, the etch stop layers 44-2 are labeled identically, and appear identical. *Id.*

> **Claim 4: "A method according to claim 3 wherein said steps of forming said etch inhibiting layer and forming said patterned conductive layer are performed simultaneously."**

As discussed in Claim 1(c), Lee discloses forming a first patterned conductive layer. As discussed in Claim 1(e), Lee further discloses forming an etch inhibiting layer, comprising a second patterned conductive layer and an etch stop layer formed next to a gate sidewall of the second patterned conductive layer. Lee discloses that the second patterned conductive layer is a "dummy pattern," and as shown in Fig. 4, is identical to the first patterned conductive layer. Lee at 17-6, Fig. 4. Lee discloses that a MOS gate is "formed by depositing gate oxide layer, poly and gate caps in this sequence and then etching them." *Id.* at 17-2. This is a well-known process for patterning a MOS gate, and a POSITA would know that the first conductive layer and the second conductive layer, called a "dummy pattern," are formed and patterned simultaneously. Lee Decl. at ¶ 115. Patterning gates that are identical, as the two in Fig. 4 are, simultaneously is a well-known design choice and indeed is the only design choice that would be practical from a manufacturing standpoint. *Id.* A semiconductor has thousands of gates formed on the substrate. *Id.* Chip designers create masks that provide a pattern to deposit all

gates at the same level simultaneously. *Id.* Compared to forming gates in different processes, forming gates simultaneously saves substantially on cost, time, and complexity. *Id.*

Lee also shows in Fig. 4 the formation of etch stop layers 44-2 and 44-3 on the first and second patterned conductive layers, through a "deposition and etch-back process." *See* Lee at 17-6. The gate sidewalls (*see* Fig. 3(a) at 34-1) are also formed through a "deposition and etch-back process." *Id.* at 17-5. This deposition and etch-back process happens simultaneously to be efficient. Lee Decl. at ¶ 116. As shown in Fig. 4, the first and second patterned conductive layers have the same number and appearance of spacers. *Id.* Performing the deposition and etch-back process for all gates on the same level simultaneously is the only feasible design choice and known for semiconductor fabrication. *Id.* Thus, to the extent Lee does not explicitly disclose forming the etch inhibiting layer and first patterned conductive layer simultaneously, Lee strongly suggests this obvious limitation to a POSITA. *Id.* at ¶ 117.

In the alternative, to the extent Lee does not explicitly disclose or make obvious this limitation, this limitation is obvious based on Lee in view of Yasushige. Yasushige discloses that a dummy pattern is formed on a field oxide layer "simultaneously with the gate electrode of the MOS transistor." Yasushige at 31. Like Lee, Yasushige uses dummy patterns to solve the problem of a mis-

alignment in an etching process resulting in over-etching a field oxide layer. Yasushige at 50; Lee Decl. at ¶ 119. Yasushige discloses that the dummy pattern **7d** is "identical to the gate electrode **7** of the MOS transistor." Yasushige at 41.

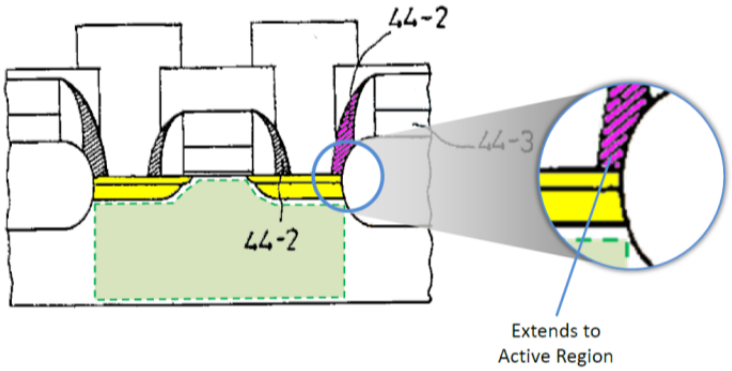
A POSITA would have been motivated to combine the teaching of a dummy pattern in Lee with the teaching in Yasushige that the dummy pattern is formed simultaneously with the MOS transistor. In addition to the reasons discussed in section VII.A., both Lee and Yasushige disclose an additional active MOS gate that is identical to the dummy pattern. Lee at 17-5 ("MOS gate is formed"); *id.* at Fig. 4; Yasushige at 41 ("a conductive film 7d identical to the gate electrode 7 of the MOS transistor is formed . . . and this conductive film 7d is electrically separated from the base region"). Thus, given the similarity in use of a dummy pattern as an etch stop, to complement the function of a MOS transistor identical to the dummy pattern, a POSITA would have been strongly motivated to look to Yasushige's manufacturing process to simultaneously form a first patterned conductive layer and a dummy pattern. Lee Decl. at ¶ 120.

**Claim 5: "A method according to claim 1 wherein said field isolation layer comprises oxide."**

Lee discloses "an active region is isolated electrically from the surrounding active regions by ***forming a field oxide layer*** (32) on a semiconductor substrate (31)." Lee at 17-5, Fig. 3(a) (annotated). Lee's disclosure of a "field oxide layer" that isolates the active region is a field isolation layer comprising oxide.

> **<u>Claim 7</u>: "A method according to claim 1 wherein the insulating spacer of the etch inhibiting layer extends to the active region of the substrate."**

As discussed in Claim 1(e) Lee's disclosure of forming an etch stop layer **44-2** as an insulating spacer along the second patterned conductive layer (**44-3**) meets the limitation "insulating spacer of the etch inhibiting layer." As shown in annotated Fig. 4, Lee discloses forming the etch stop layer 44-2 extending to the active region (highlighted yellow) of the substrate:




The etch stop layer 44-2 is formed partially on the field oxide layer and partially on the active region, so that it can protect the field oxide layer from damage when etching a contact hole to expose the active region. Lee Decl. at ¶ 122.

> **<u>Claim 8</u>: "A method according to claim 1 wherein the insulating spacer and the insulating layer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer."**

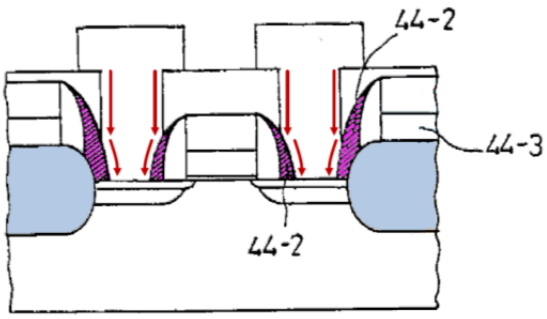
Lee discloses "a step of forming an etch stop layer around said source and drain region by depositing a ***material having a high etch selectivity with an***

***interlayer insulation film***." Lee at 17-4. As discussed in Claim 1(e), Lee further discloses that the etch stop layer can be formed as an insulating spacer along the sidewall of a dummy pattern. *Id*. at Fig. 4, 17-6. Accordingly, Lee meets this limitation.

> **<u>Claim 9</u>: "A method according to claim 1 wherein contact hole is formed over the field isolation layer and exposes a portion of the etch inhibiting layer without exposing the field isolation layer to thereby increase the area over which the contact hole can be formed without damaging the field isolation layer."**

Lee discusses the problem of misalignment when forming a contact hole, where the contact hole is formed over the field isolation layer and damages the field isolation layer causing junction leakage. Lee at Fig. 1(b) (circled and labeled "A"), 17-2.

Lee discloses forming an etch stop layer to solve this problem, and discloses forming an etch stop layer on a dummy pattern formed over a field isolation layer:




Lee at Fig. 4 (annotated), 17-6. As discussed in Claim 8, the etch stop layer 44-2 is formed with a "material having a high etch selectivity with an interlayer insulation

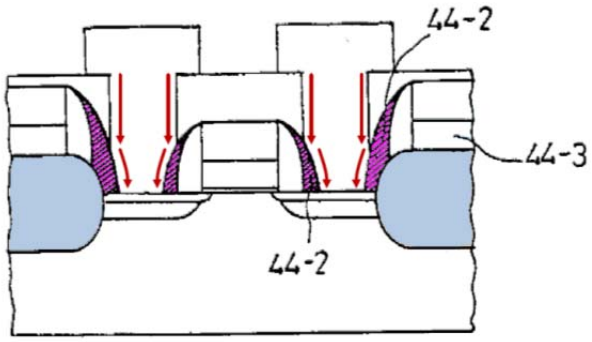
film," so that an etching process can etch a contact hole through the interlayer insulation film without etching the etch stop layer. Lee Decl. at ¶ 126. As shown in annotated Fig. 4, the formation of the contact hole exposes a portion of the etch stop layer without exposing the field isolation layer. *Id.* While Fig. 4 does not illustrate the contact hole formed directly over the field isolation layer, it is shown on the edge of the field isolation layer and Lee discloses that "since the heavily stressed site is protected by the etch stop layer, the area in which junction leakage can happen can be protected from the etching process." Lee at 17-7; Lee Decl. at ¶ 126. Thus a POSITA would know that if the contact hole were formed slightly more misaligned, the end result would be the same—the contact hole would expose the etch stop layer without etching it, and the contact hole would not expose the field oxide layer. *Id.* at ¶ 126.

Lee further discloses that the invention "relates to the structure of a semiconductor device in which ***a process alignment margin is secured*** when forming a contact hole by forming an etch stop layer on the contact hole area to ***protect the lower insulation layer***." Lee at 17-4. Thus a POSITA would understand that a contact hole formed over the field isolation layer (referred to in 17-4 as a "lower insulation layer") would expose the etch stop layer without exposing the field isolation layer. Lee Decl. at ¶ 127. Further, given Lee's disclosure that "a process alignment margin is secured," (Lee at 17-4) a POSITA

would understand that Lee discloses an invention to increase the area over which the contact hole can be formed without damaging the field isolation layer. *Id.*

> **<u>Claim 10</u>: "A method according to claim 1 wherein at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer."**

Lee discloses that a problem with forming contact holes is the possibility of damage to a field oxide layer, or a first patterned conductive layer on an active region. Lee at Fig. 1(b), 17-2. Lee discloses that "when a mis-alignment occurs, **the gate sidewall ('14) is damaged as shown in the area B** or the field oxide layer that separates an active region is also damaged **(area A of the drawing)** and thus, it becomes the cause of junction leakage." *Id.* In order to protect these two areas, an etch stop layer **(44-2)** is formed along the sidewalls of both a first patterned conductive layer and a dummy pattern:




Lee at Fig. 4 (annotated). As shown in Fig. 4, the bottom portion of the contact hole is self-aligned with respect to both the first patterned conductive layer and the etch inhibiting layer, or etch stop layer on the dummy pattern. Lee Decl. at ¶ 128.

Lee further discloses that the present invention "relates to the structure of a semiconductor device in which a ***process alignment margin is secured*** when forming a contact hole." Lee at 17-4; *see also id.* at 17-7 ("an alignment margin can be secured easily at contact photographing"). A POSITA would understand that disclosure of securing a process alignment margin, coupled with the illustration in Fig. 4 of a contact hole aligning with the etch stop layers **(44-2)** on both the first conductive pattern and the dummy pattern, satisfies this limitation. Lee Decl. at ¶ 129.

**Claim 12: [12pre] A method for forming a microelectronic structure, said method comprising the steps of:**

Lee discloses "[a] method for forming a microelectronic structure." *See* Lee at 17-1 ("The present invention relates to a method for fabricating a semiconductor device").

**[12a] defining adjacent active and field regions on a substrate, and circuits thereon;**

Lee discloses limitation [12a] of claim 12 for the reasons set forth above as to limitation [1a] of claim 1. Lee Decl. at ¶ 131.

**12[b] forming a field isolation layer which covers said field region;**

Lee discloses limitation [12b] of claim 12 for the reasons set forth above as to limitation [1b] of claim 1. The only distinction is the claiming of a field isolation layer "which covers" said field region, rather than "on" said field region.

As discussed in limitation [1b], the disclosure in Lee also shows forming a field isolation layer which covers said field region. Lee Decl. at ¶ 132.

**12[c] forming a first patterned layer on said active region of said substrate spaced apart from said field region;**

Lee discloses limitation [12c] of claim 12 for the reasons set forth above as to limitation [1c] of claim 1. Lee Decl. at ¶ 133.

**12[d] forming a second patterned layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;**

Lee in combination with Yasushige renders obvious the limitation [12d] of claim 12 for the reasons set forth above as to limitation [1d, 1e, 1f, and 1g] of claim 1. The only distinction is the claiming of a "second patterned layer" instead of an "etch inhibiting layer." But as discussed in limitation [1e], Lee in combination with Yasushige renders obvious the limitation of a second patterned layer by Lee's disclosure of the dummy pattern, (Fig. 4, 17-6) which comprises a patterned conductive layer and an etch stop layer formed along the spacer of the patterned conductive layer. Lee Decl. at ¶ 134.

**12[e] forming an insulating layer covering said substrate,**

**said field isolation layer, and said first and second patterned layers; and**

Lee discloses limitation [12e] of claim 12 for the reasons set forth above as to limitation [1h] of claim 1. The only distinction is the claiming of an insulating layer "covering" said substrate, rather than "on" said substrate. As discussed in limitation [1h], the disclosure in Lee also shows an insulating layer covering said substrate, said field isolation layer, and said first and second patterned layers. Lee Decl. at ¶ 135.

**12[f] forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers;**

Lee discloses limitation [12f] of claim 12 for the reasons set forth above as to limitation [1i] of claim 1. The only distinction is the claiming of a portion of said active region between said "first and second patterned layers," rather than an "etch inhibiting layer and said first patterned conductive layer" as claimed in limitation [1i] of claim 1. As discussed in limitation [1i] of claim 1, the disclosure in Lee also shows forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said active region between said first and second patterned layers, because the etch inhibiting layer is also a second patterned layer. Thus Lee in combination with Yasushige renders obvious claim 12. *Id.* at ¶ 136.

**Claim 11:**

Claim 11 contains the limitations of claim 12, with one additional limitation

added. Lee combined with Yasushige discloses the limitations of claim 11 that also appear in claim 12, for the reasons set forth as to claim 12. Lee Decl. at ¶ 137.

> **11[g] wherein said steps of forming said first patterned layer and forming said second patterned layer are performed simultaneously.**

Lee discloses limitation [11g] of claim 11 for the reasons set forth above as to claim 4. *Id.* at ¶ 138. The only distinction is the claiming of forming first and second patterned layers simultaneously, rather than a patterned layer and an etch inhibiting layer as claimed in claim 4. As discussed in claim 4, the disclosure in Lee also shows forming a first patterned layer and second patterned layer simultaneously, because the etch inhibiting layer is also a second patterned layer. *Id.* at ¶ 138.

> **<u>Claim 14</u>: A method according to claim 12 wherein the insulating layer and the insulating spacer comprise different materials so that the insulating layer can be etched selectively with respect to the insulating spacer.**

Lee in combination with Yasushige renders obvious claim 14 for the reasons set forth above as to claim 8. Lee Decl. at ¶ 139.

> **<u>Claim 15</u>:**

Claim 15 contains the limitations of claim 12, with one limitation added. Lee in combination with Yasushige discloses the limitations of claim 15 that also appear in claim 12, for the reasons set forth as to claim 12. Lee Decl. at ¶ 140.

**15[g] wherein each of said first and second patterned layers comprises insulating spacers along sidewalls thereof.**

Lee discloses wherein second patterned layer comprises insulating spacers along sidewalls for the reasons set forth above as to limitation [1e] of claim 1. *Id.* at ¶ 141. Lee further discloses said first patterned layer comprises insulating spacers along sidewalls thereof. The etch stop layer **44-2** is formed as a spacer along sidewalls of the first and second patterned conductive layers, as shown in Fig. 4. Lee Decl. at ¶ 142. The etch stop layer 44-2 is formed with a "non-conductive material," and is thus an insulating layer. Lee at 17-6; Lee Decl. at ¶ 142.

The etch stop layer 44-2 is identical in structure to the insulating spacer formed along a sidewall of the patterned conductive layer 44-3, and is formed along side the insulating spacer. *Id.* at ¶ 143. Lee discloses that the etch stop layer (44-2) is formed in the "form of a sidewall" and using the same "deposition and etch-back" process for making a sidewall. Lee at 17-6; *see also id.* at 17-5 ("forming a gate sidewall (34-1) using a deposition and etch-back process"). In Fig. 4, Lee illustrates the etch stop layer 44-2, and it has similar structure to the insulating spacer formed onto the conductive patterned layer. Lee Decl. at ¶ 143.

**<u>Claim 16</u>: A method according to claim 15 wherein said insulating layer can be selectively etched with respect to said insulating spacers.**

Lee in combination with Yasushige renders obvious claim 16 for the reasons

set forth above as to claim 8. Lee Decl. at ¶ 145.

**Claim 18:**

Claim 18 contains the limitations of claim 12, with one limitation added. Lee in combination with Yasushige discloses the limitations of claim 18 that also appear in claim 12, for the reasons set forth as to claim 12. Lee Decl. at ¶ 146.

> **18[g] wherein the first patterned layer comprises a patterned gate layer and an insulating gate spacer along a sidewall thereof.**

Lee discloses that a "MOS gate **(14)** is formed by depositing ***gate oxide layer***, poly and gate caps in this sequence and then ***etching them***." Lee at 17-2; *see also* Fig. 4. A POSITA would understand that depositing a sequence of layers and then etching the layers to form a MOS gate is a patterning process to create a patterned gate layer. Lee Decl. at ¶ 147. Lee discloses an insulating gate spacer along a sidewall for the reasons set forth above as to claim 3. *Id.* at ¶ 148.

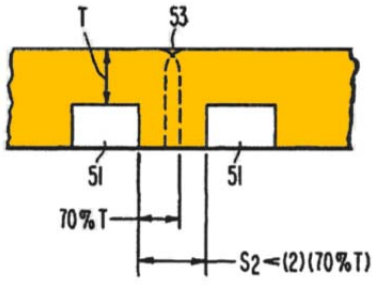
## B. Ground 2: Claims 2 and 17 are rendered obvious by Lee in combination with Yasushige and Nowak.

**Claim 2: "A method according to claim 1 wherein said insulating layer comprises nitride."**

As discussed in Claim 1[h], Lee discloses forming an insulating layer. "[A] contact hole is formed by depositing an interlayer insulation film and etching the interlayer insulation film." Lee at 17-6. While Lee does not explicitly disclose that the insulating layer comprises nitride, this limitation is obvious based on Lee

in view of Nowak. Lee discloses the insulation film is an insulating material, of which one well-known group of materials is nitride, among just a few others including oxides and spin-on polymers. Lee Decl. at ¶ 150. Lee discloses that the etch stop layer may comprise a material that has "high etch selectivity with an interlayer insulation film." Lee at 17-5. Lee further discloses "oxide layers on the substrate (field oxide layer, ***gate sidewall*** []) as mask," (*id.* at 17-6) and that the etch stop layer may be formed "in the form of a sidewall." *Id.* at 17-5. Where the etch stop layer is also an oxide layer, a POSITA would have been motivated to use another material with high etch selectivity as the interlayer insulation film, and looked to other references such as Nowak which provide details on the materials in insulating layers. Lee Decl. at ¶ 150.

Nowak explicitly discloses forming a dummy conductor gate on a substrate and depositing "a conformal layer of insulating material, such as SiO2 or ***Si3N4 or oxynitride*** . . . to cover the dummy conductors." Nowak at 3:61-4:4; *see also id.* at annotated Fig. 5B:




Thus while Nowak confirms that several materials may be used for the insulating

layer, Nowak explicitly discloses that the insulating layer comprises Si3N4, which is silicon nitride, or oxynitride. Both of these materials are well-known nitrides used to form insulating layers on a semiconductor substrate. Lee Decl. at ¶ 151.

A POSITA would have been motivated to combine the disclosure of an interlayer insulation film in Lee with the disclosure in Nowak that the insulating layer can be silicon nitride or oxynitride, for the reasons discussed in Section VII.B. Further, both Lee and Nowak both discuss forming contact holes through an insulating layer, and while Lee does not disclose the well-known technique of forming an insulating layer from a nitride, a POSITA would have been motivated to look to Nowak for details on the material composition of an insulating layer with similar function and structure as the insulating layer in Lee. Lee Decl. at ¶ 152. Further, the disclosure in Lee motivates a POSITA to try different materials that will result in high etch selectivity between the insulating layer and spacers on a gate. *Id.* The combination of Lee, Yasushige, and Nowak renders this claim obvious. Lee Decl. at ¶ 153.

**<u>Claim 17:</u> "A method according to claim 16 wherein said insulating layer comprises nitride."**

Lee in combination with Yasushige and Nowak renders obvious claim 17 for the reasons set forth above as to claim 2. Lee Decl. at ¶ 154.

### C. <u>Ground 3:</u> Claims 6 and 13 are rendered obvious by Lee in combination with Yasushige and the '524 patent.

> **<u>Claim 6:</u> "A method according to claim 1 wherein said step of defining said field and active regions comprises the step of forming a trench in said substrate, and wherein said field isolation layer fills said trench."**

This limitation is obvious based on Lee in combination with the '524 Patent. Lee discloses forming a field oxide layer. Lee at Fig. 4, 17-5. While Lee does not explicitly use the word "trench," a POSITA would know that forming a trench in the substrate that is filled by a field isolation layer is common practice in the industry, and an obvious design choice. Lee Decl. at ¶ 156.

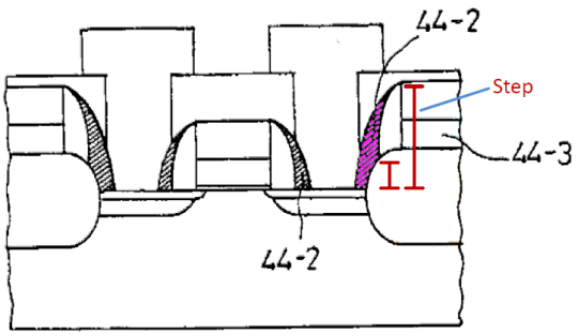
The '524 Patent discloses using "trenches for inter-device isolation." '524 Patent at 1:9. Traditionally, "trench isolation involves etching a narrow, deep trench or groove in a silicon substrate and then filling the trench with a filler material such as a silicon oxide or polysilicon." *Id.* at 1:24-25. The '524 Patent discloses both a "narrow trench" and a "wide trench." *Id.* at 2:60-61, Figs. 7-9. It further discloses at least one specific etching recipe for forming a trench. *Id.* at 3:30-38. Then, the '524 Patent discloses filling in the trench with multiple layers, "an exemplary candidate for filler layer 25 is an oxide." *Id.* at ¶ 157.

The '524 Patent issued six years prior to the filing of the parent application of the '902 Patent, and discusses an improvement on trench isolation technology ('524 Patent at 1:24-25), showing that trench isolation was well known years before the filing date of the '902 Patent. Lee Decl. at ¶ 158. The '524 Patent notes the limitations of conventional means of growing a field oxide layer, including the

"birds beaks and other formations" which cause "undesirable encroachments" into device areas. '524 Patent at 1:20-23. In contrast, a trench isolation process has advantages of consuming less space than conventional methods of forming field oxide layers. *Id.* at 1:35-38.

A POSITA would have been motivated to combine Lee with the '524 Patent to form trench isolation layers. For example, the main purpose of Lee was to prevent damage to the field oxide layer during formation of a contact hole. Lee at 17-2; Lee Decl. at ¶ 159. A POSITA would recognize that a method, such as the LOCOS method, would create a bird's beak which encroaches into the active regions and decrease the room for error in forming a contact hole. *Id*. In contrast, the trench isolation process creates field oxide layers with a "narrow, deep trench" which generally "consume less space" and accordingly helps solve the problem of contact hole misalignment into the field oxide layer, recognized by Lee. Lee at 1:27-28; Lee Decl. at ¶ 159.

Lee also contemplates that the field oxide layer may be a trench, which are typically less protruded from the surface, in its teaching of forming the etch stop layer. *Id.* at ¶ 159. While the '524 Patent teaches that a trench isolation layer "protrude somewhat beyond upper surface of the silicon wafer," Lee specifically contemplates that the "step" of the field oxide layer may not be "sufficient" and so the "step of a dummy pattern" is used to form the etch stop layer:




*Id.*; Lee at Fig. 4 (annotated), 17-6. Thus, where the protrusion of the trench isolation layer in the '524 Patent is not sufficient a "step," Lee addresses that issue by providing the dummy pattern **44-3** to form etch stop layer **44-2** along the sidewall. Lee Decl. at ¶ 160.

Accordingly the combination of Lee, Yasushige, and the '524 Patent renders this claim obvious. Lee Decl. at ¶ 161. This analysis applies to Samsung's narrower construction proffered in district court for this limitation.

> **Claim 13: A method according to claim 12 wherein said field region comprises a trench in said substrate, and wherein said field isolation layer fills said trench.**

Lee in combination with Yasushige and the '524 Patent renders obvious claim 13 for the reasons set forth above as to claim 6. Lee Decl. at ¶ 162.

Respectfully submitted,

Dated: June 2, 2015 By: /Robert Steinberg/

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## CERTIFICATE OF SERVICE

The undersigned certifies that a complete copy of this Petition No. 2 for *Inter Partes* Review of U.S. Patent No. 6,287,902 and all Exhibits and other documents filed together with this Petition were served on the official correspondence address for U.S. Patent No. 6,287,902 shown in PAIR and Samsung Electronics Co., Ltd.'s current patent counsel:

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