

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,	§	
	§	
Petitioner,	§	
	§	Case IPR2015-01320
VS.	§	Patent No. 6,287,902
	§	
SAMSUNG ELECTRONICS	§	Case IPR2015-1327
COMPANY, LTD.,	§	Patent No. 6,287,902
	§	
Patent Owner.	§	

ORAL DEPOSITION OF
JACK CHUNG-YEUNG LEE, Ph.D.
FEBRUARY 25, 2016
VOLUME 1 OF 2

ORAL DEPOSITION OF JACK CHUNG-YEUNG LEE, PH.D., produced as a witness at the instance of the Patent Owner and duly sworn, was taken in the above styled and numbered cause on Thursday, February 25, 2016, from 9:16 a.m. to 5:25 p.m., before Tamara Chapman, CSR, RPR, CCR (LA) in and for the State of Texas, reported by computerized stenotype machine, at the offices of Regus, 901 Mopac Expressway South, Building 1, Suite 300, Austin, Texas.

Job No. 103798

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MOSIS Scalable CMOS Design Rules
(Revision 7)
(No Bates - 28 pages)

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2 (All parties present have hereby
3 waived the necessity of the reading of the
4 statements by the deposition officer as required
5 by Rule 30(b)(5).)

6 JACK CHUNG-YEUNG LEE, Ph.D.,
7 having been first duly sworn, testified as
8 follows:

9 EXAMINATION

10 BY MR. MODI:

11 Q. Good morning, Dr. Lee.

12 A. Good morning.

13 Q. Can you please state your full name for
14 the record?

15 A. Yes. Jack Chung Yeung Lee, C-H-U-N-G,
16 Y-E-U-N-G, Lee, yes.

17 Q. Have you been deposed before?

18 A. Yes.

19 Q. How many times?

20 A. I don't remember off the top of my head.
21 Half a dozen times to ten times. I don't remember
22 exactly.

23 Q. What about -- have you testified in court?

24 A. Yes.

25 Q. How many times?

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2 A. One time in ITC and one time in
3 arbitration.

4 Q. And the testimony in a deposition, at the
5 ITC and the arbitration, are these all patent cases?

6 A. Yes.

7 Q. So you understand you're under oath today?

8 A. Yes.

9 Q. You understand we'll take breaks?

10 A. Yes.

11 Q. And your lawyer may object, but you have
12 to answer anyways unless you're instructed not to
13 answer. Do you understand that?

14 A. Yes.

15 Q. If the question is not clear, let me know
16 and I'll rephrase it. If not, I'm going to assume
17 you understand it.

18 A. Okay.

19 Q. Is that clear?

20 A. Yes.

21 Q. Any reason you cannot testify completely
22 and accurately today?

23 A. No.

24 Q. Do you have any questions for me?

25 A. Not at this point.

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2 Q. Okay. Who retained you for this
3 proceeding?

4 And just for the record, we'll be dealing
5 with IPR 2015-1327 today. So who retained you for
6 this?

7 A. NVIDIA.

8 Q. And when were you retained?

9 A. I'll say early last year, 2015.

10 Q. And you submitted a declaration in this
11 proceeding?

12 A. Yes.

13 Q. How much time did you spend preparing your
14 declaration?

15 A. I don't recall. I really have to look
16 back on my record, you know. I spent quite a bit of
17 time preparing it.

18 You mean both declarations or this
19 particular one?

20 Q. We can say both.

21 A. Okay.

22 Q. That's fine.

23 A. I will say that including reading all the
24 documents and prior art and drafting the declaration,
25 discussion with the attorneys working in this case, I

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2 would say at least approximately 40, 50 hours per
3 declaration, I would say. That's a rough estimate.

4 Q. How much money have you charged for your
5 services in connection with these proceedings?

6 A. For the IPR, these two patents or these
7 two declarations? So -- so about 90 hours, let's
8 say, times \$475 an hour.

9 Q. Other than NVIDIA, are you consulting with
10 any other companies regarding patents that are at
11 issue?

12 A. These patent -- these --

13 Q. I'm sorry. Let me rephrase it. Other
14 than NVIDIA, are you currently consulting for any
15 other companies in patent matters?

16 A. Any patents? Not these particular ones?

17 Q. (Nods.)

18 A. There is one case -- a few cases, I would
19 say. And some -- yeah, maybe a couple, two, three
20 cases or so.

21 Q. Have you submitted declarations in
22 proceedings before the Patent Office before?

23 A. You mean similar IPR declarations?

24 Q. Yes.

25 A. Yes.

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2 Q. And when was that?

3 A. Last year.

4 Q. And what were the cases?

5 A. Those are related to this case of NVIDIA
6 versus Samsung.

7 Q. So those are different than the --
8 these -- the two proceedings we are here for today
9 and tomorrow?

10 A. That's right.

11 Q. Okay. And -- and were the -- did the --
12 what patents were at issue? Were they NVIDIA patents
13 or Samsung patents in those cases?

14 A. These are Samsung's patent, yes.

15 Q. Other than the cases you just mentioned,
16 have you provided declarations in any other cases
17 before the Patent Office?

18 A. No, I have not.

19 Q. How many times have you been deposed in
20 connection with proceedings before the Patent Office?

21 A. Before the Patent Office, I don't
22 understand that.

23 Q. So you're being deposed today, right, for
24 proceedings in front of the Patent Office, that are
25 before the Patent Office?

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2 A. Oh, I see. Okay. So related to IPR?

3 Q. That's right.

4 A. Once.

5 Q. So once before?

6 A. Once before, yes.

7 Q. And that was the Samsung-NVIDIA IPR you
8 were talking about?

9 A. That's right.

10 Q. Did you spend any time preparing for
11 today's deposition?

12 A. Yes.

13 Q. When did you begin to prepare?

14 A. Probably a couple weeks ago I started
15 reviewing the documents and the prior art.

16 Q. Approximately how much time do you think
17 you spent preparing for your deposition today?

18 A. Probably 20 hours or so. Maybe more. I
19 don't know. I haven't looked at the records.

20 Q. Did you prepare with anyone for this
21 deposition?

22 A. What do you mean by that?

23 Q. Did you meet with the attorneys to prepare
24 for this deposition?

25 A. Yes.

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2 Q. Who did you meet with?

3 A. With -- with Eugene, Bob, and Clem here.

4 Q. Anyone else?

5 A. No, I don't think so.

6 Q. And how long did you meet with the
7 attorneys?

8 A. We met the last couple days, Tuesday and
9 Wednesday of this week.

10 Q. Did you meet with them before Tuesday and
11 Wednesday?

12 A. Regarding what?

13 Q. Preparing for the deposition.

14 A. No, I -- I have not.

15 Q. Did you review any documents to prepare
16 for your deposition?

17 A. Yes.

18 Q. What did you review?

19 A. All the declarations, the two declarations
20 that I wrote, all the prior art, and the preliminary
21 response, and -- and the PTAB decisions. I think
22 that's -- there might be some -- some more documents
23 that I prepared, but those are the main ones.

24 Q. What else comes to mind?

25 A. And the, I believe, two IPR petitions that

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2 came to my mind at this point. And there is some --
3 some other ones, but I can't recall exactly.

4 Q. When you say "some other ones," what are
5 you referring to, petitions?

6 A. No, the -- the two IPR petitions I already
7 mentioned. Nothing specific came to my mind at this
8 point, but I think there might be something that
9 I'm -- that I reviewed, but that didn't come to my
10 mind at this point.

11 Q. Can you recall anything -- let me withdraw
12 that.

13 Did you review anything other than the
14 things you mentioned and what was submitted with your
15 declaration?

16 A. Like I said, I think I have, but I don't
17 recall exactly what.

18 Q. Did you bring anything to help you testify
19 today?

20 A. My -- my laptop has a lot of -- all the
21 documents in there, so during a break I might look
22 through it. I don't know.

23 Q. And when you said your laptop has a lot of
24 documents, what documents are you referring to?

25 A. The ones that I mentioned.

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Q. Dr. Lee, you mentioned you looked at the two IPR petitions earlier.

A. Yes.

Q. When was the first time you saw those petitions?

A. I don't recall.

Q. Was it before today?

A. Oh, yeah.

Q. Did you see them in connection with preparation of your declaration?

A. You mean during the last couple days?

Q. When you were engaged -- let's say when -- or let me withdraw that.

Did you see the petition when you were preparing your declaration for this case?

A. I saw them, but I already focused on my declarations.

Q. And why were you looking at them when you were working on your declarations?

A. Well, those are one of the documents that was in folder that was given to me.

Q. The petitions?

A. Yes.

Q. And what were you -- why were you engaged

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2 for this proceeding?

3 A. I don't understand the question.

4 Q. What were you asked to do for this
5 proceeding?

6 A. You mean today proceedings?

7 Q. For these IPRs.

8 A. For the IPRs. Well, I was asked to
9 provide technical assistance and my expert opinion on
10 the related matters to the IPR.

11 Q. And you looked at some -- I think you
12 mentioned prior art references in connection with
13 your declaration. Right?

14 A. Yes.

15 Q. And those are discussed in your
16 declarations?

17 A. Yes.

18 Q. How did you select the references you
19 ended up using in your declaration?

20 A. Well, as you know, there is an ongoing
21 case in the Eastern District of Virginia. So during
22 that case we look -- also looked at prior arts, and
23 these set of prior arts that is included in the -- in
24 these two declaration we felt that -- I felt that
25 it's -- those are very strong prior arts, and so,

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2 therefore, we used them in the IPR.

3 Q. How did you locate the prior art?

4 A. I don't understand the question.

5 Q. How did you -- how did you find this prior
6 art that you used?

7 A. Well, I worked with the attorneys in this
8 case and we search the -- you know, on the web and --
9 and also, you know, we searched for prior arts and we
10 found these.

11 Q. And how -- what did you do to search for
12 the prior art?

13 A. I myself obviously using, for example,
14 patent -- Google Patents search on Google, and the
15 attorney also searched in parallel and -- and we
16 found these set of prior arts.

17 Q. Which one did you find?

18 A. I don't recall. I mean, we exchanged so
19 many of them. We e-mail each other things that we
20 found. So I don't recall exactly which ones I found
21 and which ones they found.

22 Q. And so the prior art that you searched
23 for, you only did searching online?

24 A. I mean, we exchanged so many documents, so
25 many references. Some I basically look at my

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2 collection of books and journal papers on my
3 bookshelves, and sometimes I make copies of that and
4 scan it, and so I -- I don't -- I mean, there are
5 more ways to find prior arts than just search on the
6 web.

7 Q. Did you continue to look for prior art
8 after your declaration was submitted in this case?

9 A. I don't recall.

10 Q. So would you say you're familiar with
11 patents?

12 A. These particular patents?

13 Q. Patents in general.

14 A. I don't understand the question. What do
15 you mean, "familiar with patents"?

16 Q. Would you say you're well-versed in
17 patents generally?

18 A. I mean, I work with patent cases, so I
19 would think that I have some understanding and good
20 understanding of what patents are, and I followed a
21 number of patents and issued a number of patents.

22 Q. Would you say you have a good
23 understanding of patent law?

24 A. Probably not as much as you do. But some
25 understanding.

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2 Q. Are you offering any legal opinions here?

3 A. Well, based on my analysis, I found that
4 those patents -- I mean, that particular -- the '902
5 patent invalid, and -- and obviously that's a legal
6 opinion.

7 Q. Earlier you said you had searched for
8 prior art for the patent here that's at issue. Is
9 that right?

10 A. Yes, I've done some searching.

11 Q. What words did you use to search?

12 A. What what?

13 Q. What were some of the words you used to
14 search for the patent in question?

15 A. Well, there's so many -- so many words
16 that I used. The '902 patent talk about etching,
17 talk about contact, semiconductors, and so there's so
18 many that one can use. I don't -- I don't have the
19 complete list for you.

20 Q. What comes to mind sitting here today?

21 A. Well, like I said, there's semiconductor,
22 contact etch, borderless contact, insulator, etch
23 selectivity, planarizations, and so on and so forth.
24 There's DRAM. D-R-A-M, yes.

25 Q. Do you understand what anticipation is?

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2 A. As I detail in my declaration, I have a
3 section talk about what is anticipation and that the
4 prior art basically anticipate the claims and the
5 elements in the -- in the patent.

6 Q. What do you mean, "prior art anticipate
7 the claims"?

8 MR. CHIU: Doctor, do you want to
9 have your declaration?

10 THE WITNESS: Yeah.

11 A. May I have my declaration?

12 MR. MODI: Counsel, no speaking
13 objections.

14 A. I'm obviously not an attorney, so I want
15 to make sure that I use the right terms in these --
16 in these answer when related to legal matters. Is
17 that okay?

18 Q. (BY MR. MODI) That's fine.

19 Dr. Lee, your attorney just handed you
20 something. Can I see what that is, sir?

21 A. (Hands document to Mr. Modi.)

22 Q. Dr. Lee, can you identify for me what was
23 just handed to you by your attorney?

24 A. This is Exhibit 1116.

25 Q. And what is it?

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2 A. It's Declaration of Dr. Jack Lee in
3 Support of Petitions No. 2 for Inter Partes Review of
4 U.S. Patent No. 6,287,902.

5 Q. Do you agree this is one of the two
6 declarations that we've been discussing today?

7 A. Are we discussing both declaration today
8 or --

9 Q. Well, we've been mentioning both
10 declarations. We're going to focus on 1327 today,
11 but I think some of the preliminary questioning went
12 to both.

13 A. Yes, this is one of the two declarations
14 that we mentioned today.

15 Q. I'm going to note for the record the
16 witness has been looking at the LiveNote feed when
17 answering the questions.

18 So I was asking you earlier --

19 A. Am I not allowed?

20 MR. NAPLES: You can look at that.

21 THE WITNESS: Oh, okay.

22 A. Am I not allowed to look at the live feed?

23 Q. (BY MR. MODI) Dr. Lee, I'm asking the
24 questions.

25 A. No, I --

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2 Q. So if you could answer my questions, I
3 would appreciate it.

4 MR. CHIU: You can look at the
5 live feed.

6 THE WITNESS: Okay. Thank you.

7 Q. (BY MR. MODI) So, Dr. Lee, I asked you
8 about anticipation earlier?

9 A. Yes.

10 Q. Would you tell me what is your
11 understanding of anticipation, sir?

12 A. "I understand that anticipation of a claim
13 requires that every limitation" -- "every element of
14 a claim is disclosed expressly or inherently in a
15 single prior art reference, arranged as in the
16 claim."

17 Q. Where are you reading from, Dr. Lee?

18 A. This is on Page 4 of the declaration.

19 Q. What does it mean to disclose inherently?

20 A. It means that it might not be expressly
21 disclosed but is inherent, that a person of ordinary
22 skill in the art understand that in this prior art
23 reference, that the claim element and each and every
24 claim element is expressly or inherently disclosed,
25 and so certain claims might not be expressly

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2 disclosed, but it is inherent.

3 Q. So what does "inherent" mean?

4 MR. CHIU: Objection; calls for a
5 legal conclusion.

6 MR. MODI: Counsel, no speaking
7 objections, please.

8 A. "Inherent" means that it is implicitly
9 disclosed in this -- in the prior art. The claim
10 element is implicitly disclosed, is there.

11 Q. (BY MR. MODI) What do you mean,
12 "implicitly"?

13 A. That means if it -- by not explicitly or
14 expressly, but it is disclosed.

15 Q. But then what's the difference?

16 A. The difference that is one is expressly,
17 one is not expressly.

18 Q. Can you give me an example?

19 MR. CHIU: Objection; legal
20 conclusion and beyond the scope.

21 A. (Reviewing document.)

22 Are you asking an example in this
23 declaration or just a general example? I wasn't --

24 Q. (BY MR. MODI) Well, you just spent the
25 last few minutes looking at your declaration. Did

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2 you find any example in your declaration, sir?

3 A. I just -- I -- I don't think so. I
4 haven't seen any, so -- there might be, but, you
5 know, I haven't looked at it too carefully. But let
6 me give you perhaps a -- a general example. Is that
7 what you like, what is inherent, inherently
8 expressed?

9 Q. Sure.

10 A. So --

11 MR. CHIU: Again, this is beyond
12 the scope of this deposition.

13 A. For example, if the claim, let's say --
14 say that the substrate is silicon and the prior art
15 says the substrate is semiconductor, and when it's
16 thermally grown in oxygen and silicon dioxide is
17 formed, even though it does not specifically
18 expressly say that the semiconductor substrate is
19 silicon, when it's thermally grown in oxygen to form
20 SiO₂, silicon dioxide, I believe that's an example
21 that the claim limitation or claim element of the
22 substrate being silicon is inherently expressed.

23 Q. (BY MR. MODI) And what is the inherent
24 disclosure there?

25 MR. CHIU: Objection; legal

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2 conclusion, beyond the scope.

3 A. That the substrate is silicon. That is
4 expressly -- inherently disclosed in this example.

5 Q. (BY MR. MODI) So in your example, what
6 was in the claim, sir?

7 MR. CHIU: Objection; legal
8 conclusion, beyond the scope of what's in
9 Dr. Lee's declaration.

10 A. Well, I think, if you read it back, it
11 says if the claim says the substrate is silicon.

12 Q. (BY MR. MODI) So the claim would say the
13 substrate is silicon?

14 MR. CHIU: Same objection.

15 Q. (BY MR. MODI) Is that right?

16 MR. CHIU: Same objection.

17 A. That's -- that's the example that I have,
18 yes.

19 Q. (BY MR. MODI) Okay. And what did you say
20 was in the prior art?

21 MR. CHIU: Objection; outside the
22 scope of Dr. Lee's deposition.

23 A. The prior art says the substrate is
24 semiconductor, and when it's thermally exposed in
25 oxygen, silicon dioxide is formed.

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2 Q. (BY MR. MODI) And that, in your view, is
3 an inherent disclosure of the substrate being
4 silicon?

5 MR. CHIU: Calls for a legal
6 conclusion, outside the scope of Dr. Lee's
7 declaration.

8 A. That's my understanding, that even though
9 it does not expressly discloses that the substrate is
10 silicon, but it's inherently disclosed.

11 MR. STEINBERG: Counsel, at
12 8 o'clock [sic] I want to take a break. I'm
13 going to switch out for a call, and I don't want
14 to disrupt you. I need to talk to these two
15 guys.

16 THE WITNESS: May I?

17 MR. MODI: Can we finish this line
18 of questioning?

19 MR. STEINBERG: Sure.

20 Q. (BY MR. MODI) So can you not deposit
21 silicon on top of nonsilicon, and thermally grow
22 silicon oxide from the deposited silicon?

23 MR. CHIU: Objection; calls for a
24 legal conclusion, outside the scope of Dr. Lee's
25 deposition.

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2 A. Can you repeat? Because this doesn't make
3 sense.

4 Q. (BY MR. MODI) Can you not deposit silicon
5 on top of nonsilicon and thermally grow silicon oxide
6 from the deposited silicon?

7 MR. CHIU: Objection; vague,
8 outside the scope of Dr. Lee's declaration.

9 (Discussion off the record.)

10 A. In this example of the prior art, the
11 semiconductor wafer does not have a layer of silicon
12 deposit on top.

13 MR. MODI: Why don't we take a
14 break.

15 THE WITNESS: Thank you.

16 (Break.)

17 Q. (BY MR. MODI) Dr. Lee?

18 A. Yes.

19 Q. During the break did you talk to your
20 attorneys?

21 A. Yes. But when I walked in that office
22 there, they told me that we cannot talk anything --
23 anything substance, so I left the room. I said,
24 "Well, let me leave the room."

25 And they just said, "You're doing fine."

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2 Fine. Relax." That's it. Nothing else.

3 Q. What is your understanding of obviousness?

4 MR. CHIU: Calls for a legal
5 conclusion.

6 A. Well, as I stated in Paragraph 15, that
7 "Obviousness of a claim requires that the claim be
8 obvious from the perspective of a person of ordinary
9 skill in the art, in the relevant art, at the time
10 the invention was made."

11 So in analyzing obviousness, my
12 understanding is that it is important to understand
13 the scope of the claim and the level of the skills in
14 the relevant art, and the scope and the content of
15 the prior art, and the differences between the prior
16 art and the claims, and any secondary considerations.

17 So "understand that if a technique can be
18 used to improve one device and a person of ordinary
19 skill in the art would recognize that, that it would
20 improve similar devices in the same way, using the
21 technique is obvious unless the actual application is
22 beyond his or her skill."

23 Q. (BY MR. MODI) Dr. Lee, let me just stop
24 you --

25 A. Yes.

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2 Q. -- for a minute. I obviously have read
3 your declaration, sir.

4 A. Right.

5 Q. I want to know what is your understanding
6 of obviousness.

7 A. That is my --

8 MR. CHIU: Calls for a legal
9 conclusion.

10 A. That is my understanding.

11 Q. (BY MR. MODI) What is stated in
12 Paragraph 15 of your declaration?

13 A. That's right.

14 Q. Okay. You mentioned secondary
15 considerations. What is your understanding of
16 secondary considerations, sir?

17 MR. CHIU: Calls for a legal
18 conclusion. Outside the scope of Dr. Lee's
19 declaration.

20 A. (Reviewing document.)

21 I was told secondary consideration, what
22 they are, and -- but since I'm not a lawyer and --
23 and I just don't recall right at this moment. And --
24 yeah, it's -- it's -- my mind is kind of -- have not
25 focused on this particular issues of secondary

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2 consideration, but hold on one second.

3 (Reviewing document.)

4 No, I just don't recall the definitions of
5 "secondary considerations" at this moment. I'm
6 really a technical person.

7 Q. But your declaration uses the word
8 "secondary considerations." Right?

9 A. Right.

10 Q. And you told me earlier that those should
11 be considered in an obviousness analysis. Right?

12 A. Right.

13 Q. But you're not able to tell me what
14 secondary considerations are?

15 A. I can tell you the legal definition of
16 what is secondary considerations.

17 Q. I'm just asking for your understanding
18 as -- what understanding of secondary considerations
19 did you apply in forming your opinions?

20 MR. CHIU: Calls for a legal
21 conclusion. Outside the scope of Dr. Lee's
22 declaration.

23 A. I'm not -- I don't think I've used
24 "secondary considerations." I'm not sure. I don't
25 think I have used "secondary considerations" in this

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2 declaration.

3 Q. (BY MR. MODI) So you have not considered
4 any secondary considerations in your obviousness
5 analysis? Would it be fair to say that, that you
6 have not considered any secondary considerations in
7 your obviousness analysis? Fair?

8 MR. CHIU: Outside the scope of
9 Dr. Lee's declaration.

10 A. (Reviewing document.)

11 In this declaration I don't think I've
12 used secondary considerations. I think that -- that
13 was not considered at this point, if I recall
14 correctly.

15 Q. (BY MR. MODI) What is the difference in
16 anticipation and obviousness?

17 MR. CHIU: Objection; calls for
18 legal conclusion, outside the scope of Dr. Lee's
19 declaration.

20 Q. (BY MR. MODI) Actually, let me withdraw
21 that, Dr. Lee.

22 What is your understanding of the
23 difference between anticipation and obviousness as
24 you have applied it to your declaration?

25 MR. CHIU: Objection; calls for a

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2 legal conclusion, outside the scope of Dr. Lee's
3 declaration.

4 A. Well, anticipation is that -- when every
5 element of the claim is disclosed expressly or
6 inherently in the prior art, in a single prior art
7 reference; and when it is not expressly or inherently
8 disclosed, that the claim can still be invalid by
9 obviousness.

10 Q. (BY MR. MODI) Are you finished?

11 A. Yes. So when -- when it is not expressly
12 or inherently disclosed -- when the element is not
13 disclosed expressly or inherently, it can still be
14 disclosed by obviousness.

15 Q. Can I have you turn to Page 38 of
16 Exhibit 1116, which is your declaration.

17 Let me know when you're there.

18 A. Page 38?

19 Q. Yes, Dr. Lee.

20 A. Yes.

21 Q. Do you have that in front of you?

22 A. Yes.

23 Q. Can you go ahead and read Paragraphs 80,
24 81, and 82 into the record for me?

25 A. Paragraph 80 says, "Claims 1, 3-5, 7-12,

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2 14-16, and 18 are rendered obvious by Lee and
3 Yasushige."

4 Paragraph 81 says, "Claims 2 and 7 are
5 rendered obvious by Lee in combination with Yasushige
6 and Nowak."

7 Paragraph 82 says, "Claim 6 and 13 are
8 rendered obvious by Lee in combination with Yasushige
9 and the '524 patent."

10 Q. So in this particular proceeding and in
11 this declaration, do you agree that the only opinions
12 you have offered are obviousness opinions?

13 MR. CHIU: Objection; vague.

14 A. That in this declaration, that my opinion
15 is summarized in the paragraph I just read.

16 Q. (BY MR. MODI) Dr. Lee, that's not what I
17 asked you.

18 Let me ask you a different way. Are you
19 offering any anticipation opinions in this
20 declaration, sir?

21 A. (Reviewing document.)

22 My opinion is that all the claims are
23 rendered obvious and -- and those are the -- my --
24 those are the obviousness opinions, yes. And so
25 they're not anticipation opinion.

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2 Q. And can I ask you, sir, can you go back to
3 Paragraph 15 of your declaration on Page 5?

4 A. Okay.

5 Q. In that paragraph, and I think you read
6 this earlier to me, you say "I understand that it is
7 important to understand the scope of the claims."

8 Do you see that?

9 A. Yes.

10 Q. What do you mean by "understanding the
11 scope of the claims"?

12 A. It means that it's important to understand
13 what the claim encompass, what -- based on the
14 perspective of the ordinary skill in the art in those
15 relevant arts at the time of the invention.

16 Q. And how did you interpret -- or, actually,
17 let me withdraw that.

18 What standard did you apply to interpret
19 the claims in this proceeding?

20 MR. CHIU: Objection; vague, calls
21 for a legal conclusion.

22 MR. MODI: Counsel, you cannot
23 make a vague objection. I've been giving you
24 leeway. You can only object to form.

25 A. Well, the standard I apply is from the

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2 perspective of a person of ordinary skill in the art
3 at the time of the invention --

4 Q. (BY MR. MODI) Then what is the --

5 A. -- was made.

6 Q. -- time frame?

7 A. Say early 1996.

8 Q. And where are you getting that from, sir?

9 A. What do you mean where do I -- where do I
10 get it from?

11 Q. How did you come to the early 1996 time
12 frame?

13 A. When I go through this analysis, I recall
14 that as -- that's the time frame that I'm using to
15 analyze this -- these two -- these patents and these
16 prior art.

17 Q. And you said you were applying -- I think
18 you mentioned the words "level of ordinary skill"?

19 A. Yes.

20 Q. What was that level of ordinary skill that
21 you're applying here?

22 A. Well, as I stated in Paragraph 19, that an
23 ordinary skill level of -- a "person of ordinary
24 skill in the art would have had an undergraduate
25 degree in electrical engineering (or equivalent

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2 subject) together with three to four years of
3 post-graduate experience designing semiconductor
4 devices and fabrication process" --

5 Q. So where are you reading that from, sir?

6 A. I mentioned Paragraph 19.

7 Q. I'm sorry. I missed that.

8 A. -- "or a master's degree in electrical
9 engineering (or equivalent subject) together with one
10 or two years of post-graduate experience in designing
11 semiconductor devices and fabrication process."

12 Q. You consider yourself an expert in this
13 case. Right?

14 A. Yes.

15 Q. Would you agree that you are one of
16 extraordinary skill?

17 MR. CHIU: Objection; vague, form.

18 A. I would say that I'm at least qualified as
19 a person of ordinary skill in the art, and I have a
20 lot more experience than what is stated here for the
21 level of ordinary skill in the art. I have 30 years
22 of experience after my Ph.D. degree, and -- and I
23 have not just a bachelor's degree in electrical
24 engineering, but also a master's degree and a Ph.D.
25 degree. So I would say that I'm more than qualified

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2 as a person of ordinary skill in the art.

3 Q. (BY MR. MODI) So would you agree that
4 you're one of extraordinary skill?

5 MR. CHIU: Objection; form.

6 A. I'm not sure what you mean by
7 "extraordinary skill." Definitely exceeding the
8 ordinary skill in the art -- of the skill in the art,
9 yeah.

10 Q. (BY MR. MODI) And that is what you
11 applied here for your opinions?

12 MR. CHIU: Objection; vague.

13 A. What do you mean by that?

14 Q. (BY MR. MODI) The level that you just
15 articulated is what you applied to form your opinions
16 in this case?

17 MR. CHIU: Objection; vague.

18 A. Well, I approach these technical issues
19 from the perspective of such a person of ordinary
20 skill in the art.

21 Q. (BY MR. MODI) But you would agree that
22 you exceed the level of skill in the art?

23 A. Well, I -- my own level of skill might be
24 exceeded the ordinary skill in the art, but I apply
25 the standard of the person of ordinary skill in the

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2 art that I describe in Paragraph 19 from my
3 declaration in analyzing the technical issues related
4 to this matter.

5 Q. How did you go about doing that, Dr. Lee,
6 given your -- given you exceed the level of ordinary
7 skill in the art?

8 MR. CHIU: Objection; form,
9 outside the scope of Dr. Lee's declaration.

10 A. Very carefully.

11 Q. (BY MR. MODI) Can you tell me how?

12 MR. CHIU: Same objection.

13 A. Very, very carefully.

14 Q. (BY MR. MODI) I understand you're saying
15 very carefully. But how did you divorce your
16 knowledge that you have beyond the level of skill in
17 forming your opinions?

18 MR. CHIU: Objection; form. This
19 is all outside the scope of Dr. Lee's
20 declaration.

21 A. Well, I try to think of it as if I were a
22 person of ordinary skill in the art or have only a
23 master's degree and only a couple of years of
24 post-graduate experience, how would I understand and
25 how would I approach these technical issues.

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2 Q. (BY MR. MODI) So you erased your
3 knowledge beyond what you just articulated to form
4 your opinions?

5 A. Wait.

6 MR. CHIU: Objection; form.

7 A. No, that's not what I said. I didn't -- I
8 didn't say that I raised my knowledge beyond. What
9 do you mean by "you raised your knowledge beyond"?

10 Q. (BY MR. MODI) I said "erased."

11 A. Erased. Oh, I thought you -- it says
12 "raised."

13 THE REPORTER: I heard "raised."

14 THE WITNESS: I did too.

15 MR. CHIU: Mischaracterizes the
16 witness's testimony.

17 A. Let me give you an example. When I talk
18 to my kids who are in high school and first year of
19 college, I try to think of myself in their
20 perspective. Okay? So do I erase all the knowledge
21 beyond high school and college?

22 I assume that I have the same level of
23 understanding and perspective of my kids in
24 understanding some of the issues that they're going
25 through.

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2 Similarly, in this case, that although I
3 have a level of skill might be exceed the ordinary
4 skill of the art -- in the art, I still approach
5 this -- these technical issue from the perspective of
6 such person, such ordinary level of skill in the art.

7 Q. (BY MR. MODI) Dr. Lee, we talked about
8 anticipation and obviousness earlier?

9 A. Yes.

10 Q. Do you remember that?

11 A. Yes.

12 Q. And I took you to Page 38 of your
13 declaration. Can you go there again?

14 A. Yes. Yes.

15 Q. And Paragraphs 80 to 82 summarize your
16 opinions in this case. Right?

17 A. Yes. In Section IX is a summary of my
18 opinions.

19 Q. And 80 to 82 list your obviousness
20 opinions. Right?

21 A. It summarizes my obviousness opinion, yes.

22 Q. Do you agree that Lee does not anticipate
23 the claims?

24 MR. CHIU: Objection; vague,
25 beyond the scope of Dr. Lee's declaration.

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2 A. (Reviewing document.)

3 No, I disagree.

4 Q. (BY MR. MODI) In your summary of the
5 opinions, you only list obviousness conclusions.
6 Right?

7 MR. CHIU: Asked and answered.

8 A. If you read my declaration, that the
9 claims are anticipated and -- and disclosed by Lee,
10 and -- and that in some claim, to the extent that --
11 in some claim limitation, that to the extent that
12 those claim limitation is not explicitly disclosed,
13 that those limitations is at least obvious based on
14 Lee itself or in combination with other references.

15 So the summary opinion basically
16 summarizes that those -- these claims are at least
17 rendered obvious. And, in fact, a lot of the claim
18 limitations and elements -- limitations are disclosed
19 explicitly by Lee.

20 Q. (BY MR. MODI) So you're changing your
21 earlier answer?

22 MR. CHIU: Objection; form.

23 A. I'm giving you -- I'm clarifying my
24 earlier answer.

25 Q. (BY MR. MODI) So give me one example.

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2 A. Well, Claim 1, for example.

3 Q. Okay. Can you show me where in your
4 declaration? What are you referring to? What
5 example are you thinking of?

6 A. Claim 1 of -- as an example, from Page 38
7 to 57 of my declaration.

8 Q. But I thought for Claim 1 you were relying
9 on another reference in addition to Lee, aren't you?

10 A. Only if -- to the -- to the extent that
11 the limitation is not explicitly disclosed, that
12 limitation is rendered obvious based on Lee, perhaps
13 in view of other references.

14 Q. And in this case, Yasushige?

15 A. In Claim 1, yes.

16 Q. Okay. And what is the limitation that you
17 believe makes it an obviousness --

18 MR. CHIU: Objection; form.

19 Q. (BY MR. MODI) -- opinion for Claim 1?

20 A. No. I'm saying that in Claim 1, it is
21 anticipated and -- but to the extent that it is not
22 explicitly disclosed, that the limitation is obvious.

23 So I'm not sure what you mean by "I
24 believe it makes it an obviousness."

25 Q. So when you -- you keep on saying "to the

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2 extent it's not explicitly disclosed, that limitation
3 is obvious."

4 A. Right.

5 Q. Do you have a particular limitation in
6 mind when you say that, sir?

7 A. Well, for example -- Element 1f.

8 Q. What page are you looking at?

9 A. Page 46.

10 Q. So what about Element 1f?

11 A. You asked me to give an example. I'm
12 giving you an example of 1f.

13 Q. Right. I understand that. But -- so
14 example -- what is it, Element 1f, an example of?

15 MR. CHIU: Objection; form.

16 A. You asked me to give an example where I
17 said to the extent that the limitation is not
18 explicitly disclosed, that the limitation, it's
19 obvious. And 1f is one such example.

20 Q. (BY MR. MODI) Can you go to Page 41 of
21 your declaration?

22 A. Yes.

23 Q. Do you see Element 1c listed there?

24 A. Yes.

25 Q. Is it your opinion that Lee explicitly

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discloses the Limitation 1c?

A. May I have the Lee reference?

Q. Yes, you may. Before I give it to you, can you look at your declaration and tell me what is your position based on your recollection?

MR. CHIU: He asked for -- he asked for a reference.

MR. MODI: Counsel, I will give it to him.

Q. (BY MR. MODI) Please answer it.

A. Say it again.

Q. Can you answer the question based on your declaration?

A. Based on my declaration?

Q. Yes, sir.

A. Yeah. The declaration disclose that the -- that Lee discloses Limitation 1c.

Q. Does Lee explicitly disclose Limitation 1c? That was my question, Dr. Lee.

A. Well, in light of the figure and also the Lee specifications, that -- in my opinion, that 1c is disclosed by Lee.

Q. It is explicitly disclosed by Lee. That is your opinion?

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2 A. All the evidence disclosed in Lee shows
3 the limitations -- meets the limitations of 1c, and
4 no evidence -- Lee does not show any evidence
5 contrary to the -- to the limitation of 1c.

6 Q. Dr. Lee, I don't think you answered my
7 question. My question is simple. Does Lee disclose
8 Element 1c explicitly? Yes or no.

9 A. Yes.

10 Q. So you're not relying on obviousness for
11 Element 1c. Correct?

12 A. Well, like I said, if you give me my --
13 the Lee reference, I can point to you that -- not
14 just the figure, but also specification -- the
15 specification specifically disclose in conjunction
16 with the figure that Limitation 1c is met --

17 Q. So, again --

18 A. -- explicitly.

19 Q. So you are not relying on obviousness for
20 Element 1c. Correct?

21 A. I believe that a person of ordinary skill
22 in the art would not have to rely on obviousness for
23 Element 1c, but to the extent that this limitation is
24 not explicitly disclosed in Lee, that this limitation
25 is obvious.

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2 Q. Dr. Lee, that's not my question. It's
3 very simple. I'm asking you for your opinion, sir.
4 For Element 1c, are you relying on obviousness? Yes
5 or no.

6 MR. CHIU: Asked and answered.

7 A. No, because the -- Lee discloses that the
8 "first patterned conductive layer on said active
9 region of the substrate is spaced apart from said
10 field region," based on what is disclosed in the
11 figures and also in the specification.

12 Q. (BY MR. MODI) And you're referring to
13 Figure 3(a) here?

14 A. All the figures.

15 Q. Including Figure 3(a)?

16 A. Including Figure 3(a).

17 Q. Okay. Can I ask you to go back --

18 A. Can I have the Lee reference, please?

19 Q. I will give it to you.

20 A. Can I have it now?

21 Q. Again, I will give it to you. We will get
22 to it. So I'd like to move on. You've answered my
23 question, and I'd like to move on, and then we'll
24 come back to it.

25 So can I ask you to go to Paragraph 18,

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2 please.

3 A. Yes.

4 Q. And in Paragraph 18 you indicate that you
5 looked at the prosecution history. Is that right,
6 sir?

7 A. Yes.

8 Q. What is your understanding of the
9 prosecution history?

10 MR. CHIU: Objection; form.

11 A. My understanding of the prosecution
12 history, if I -- is that --

13 Q. (BY MR. MODI) Let me withdraw that.

14 I'm just generally asking you, what is
15 your understanding of the prosecution history of a
16 patent? What does that mean to you?

17 MR. CHIU: Objection; form.

18 A. Of not -- not specific to '902. I thought
19 that's what you were asking.

20 Q. (BY MR. MODI) Sorry.

21 A. Well, during the prosecution of a patent
22 to the Patent Office, the patent reviewer will
23 provide feedback and make decisions whether they
24 accept the patents and the claims or reject. And the
25 patent applicant will respond, perhaps, with

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2 modifications of the patents and the claims.

3 And until the -- that process is called
4 prosecution history. It's the process from the start
5 of the applications of the -- for the patents and
6 until the patent is issued.

7 Q. Dr. Lee, can I ask you to go to
8 Paragraph 16 in your declaration, Exhibit 1116?

9 A. Right.

10 Q. If you can, just take a minute and read it
11 to yourself. And can you let me know when you're
12 done reading it?

13 A. (Reviewing document.)

14 Okay. I'm done.

15 Q. You use a term in this paragraph called
16 "the broadest reasonable interpretation." Do you see
17 that?

18 A. Yes.

19 Q. What is your understanding of that term,
20 as you applied it to your declaration, sir?

21 MR. CHIU: Objection; calls for a
22 legal conclusion.

23 A. It means that the claim constructions are
24 given the widest but reasonable understanding and
25 interpretations, but have to be consistent with the

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2 specification in the patent.

3 Q. (BY MR. MODI) I think you said "widest."
4 Is that right?

5 A. Yeah, kind of --

6 Q. What do you mean by that?

7 A. Very -- not narrow. Very -- very broad,
8 the broadest. The -- instead of a very narrow
9 interpretation, it's as broad as possible, it's as
10 wide as possible.

11 Q. Dr. Lee, it sounds like you're reading
12 your answer on the live feed. And it seems like you
13 have -- you're not happy with the way it was
14 transcribed.

15 Why don't you go ahead and tell us what
16 you -- what is your -- what did you mean by "widest"?

17 MR. CHIU: Objection; form.

18 A. What I said was the broadest. It is not a
19 very narrow -- it is not a narrow interpretation.

20 MR. MODI: Okay. Why don't we
21 take a break?

22 THE WITNESS: Okay.

23 (Break.)

24 Q. (BY MR. MODI) Dr. Lee, during the break
25 did you review any materials?

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2 A. No.

3 Q. Did you talk with your attorneys?

4 A. Yes.

5 Q. What did you talk about?

6 A. I was upset that you didn't give me the
7 reference.

8 Q. And?

9 A. And they said, "Just ask for it."

10 Q. Anything else?

11 A. That's it.

12 Q. And I think during the break, when we came
13 back, I see you have some documents in front of you.
14 Can you identify those for us, please, for the
15 record?

16 A. That's exhibit -- one of them is
17 Exhibit 1107 that I have been asking for, which is
18 the Lee reference. And Exhibit 1013 is "Declaration
19 of Dr. Jack Lee In Support of Petition No. 1 For
20 Inter Partes Review of U.S. Patent No. 6,287,902."

21 Q. Can I see those documents for a minute?
22 I'll give them back to you.

23 A. (Hands documents to Mr. Modi.)

24 MR. MODI: Just for the record,
25 just to clarify the record, I'll note

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2 Exhibit 1013 is from IPR 2015-01320.

3 Q. (BY MR. MODI) Dr. Lee, why were you
4 looking at Exhibit 1013?

5 A. I was just comparing the -- the early --
6 the beginning sections of the 1013 in comparison to
7 1116, Exhibit 1116, if there is any differences.
8 That's all.

9 Q. And why were you doing that?

10 A. Just curious.

11 Q. Did you find any differences?

12 A. Based on just a brief scan, I have not.
13 The first few pages looks very similar.

14 Q. Can I ask you to go to Paragraph 30 of
15 your declaration, Exhibit 1116, please?

16 A. Yes.

17 Q. Let me know -- if you want to read
18 Paragraph 30 to yourself, let me know when you're
19 done.

20 A. (Reviewing document.)

21 Yes.

22 Q. So you've reviewed the prosecution history
23 of the '902 patent. Is that right?

24 A. Yes.

25 Q. Can I ask you to turn to Paragraph 32 of

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2 your declaration?

3 A. Yes.

4 Q. And why don't you read that to yourself.
5 Let me know when you're done.

6 A. (Reviewing document.)

7 Yes.

8 Q. In this paragraph you mention Michihiro.
9 Do you see that?

10 A. Yes, I see that. Yes.

11 Q. What is Michihiro?

12 MR. CHIU: Objection; form.

13 A. It is one of the prior arts that the
14 Patent Office considered.

15 Q. (BY MR. MODI) Did you look at Michihiro
16 in forming your opinions?

17 A. I looked at the file history and -- and
18 review Michihiro.

19 Q. This Paragraph 32 in Exhibit 1116 relates
20 to a non-final rejection. Is that correct?

21 A. Yes, in Paragraph 32 it says in a
22 non-final rejection that the examiner stated such and
23 such, as disclosed in Paragraph 32.

24 Q. And in your review of the prosecution
25 history you looked at the non-final rejection. Is

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2 that right?

3 A. Yes, I have.

4 Q. Can I ask you to go -- and actually,
5 before I go there -- and you see right before
6 Paragraph 32 there is a heading that says "Michihiro
7 in view of Chen." Do you see that? It's right
8 before Paragraph 32.

9 A. Yes. Yes.

10 Q. And Chen is another reference that the
11 examiner was using. Is that correct?

12 A. Yes. Chen is one of the references that
13 has been considered and cited by the examiner.

14 Q. And you also looked at Chen in your -- in
15 conjunction with your review of the prosecution
16 history?

17 A. Yes, I have.

18 Q. So can I ask you to go to Page 14, please,
19 sir.

20 A. Yes.

21 Q. Actually, before I go to Page 14, I'm
22 sorry, if I can have you go back to Page 13,
23 Paragraph 32 for me.

24 A. Okay.

25 Q. There you said, "...the examiner stated

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2 that Michihiro disclosed in Figs. 2(e), 4(b)..." Do
3 you see that?

4 A. Yes.

5 Q. Okay. And then if you go to Page 14 of
6 your declaration, I believe you produced Figure 2(e)
7 there. Is that right?

8 A. Yes.

9 Q. And then there is another figure that's
10 reproduced there. I believe you may have mislabeled
11 that. You say it's 4(a), but I believe it's 4(b).

12 A. Okay. I'll take your word for it.

13 Q. Okay. Let me give you the prosecution
14 history. I wanted to ask you a few questions about
15 that.

16 So, Dr. Lee, I'm going to hand you what
17 has been previously marked as Exhibit 1102.

18 A. Okay.

19 Q. Can you identify this exhibit for me,
20 please?

21 A. I believe this is a prosecution history of
22 the patent '902.

23 Q. And we were just discussing that in
24 connection with your declaration. Right?

25 A. Yeah. We -- on Page 13 we discussed the

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2 prosecution history of '902 patent.

3 Q. And this is the prosecution history you
4 reviewed in connection with forming your opinions in
5 this case. Right?

6 A. Well, in addition to all -- all the
7 materials that I cited.

8 Q. Fair enough. So can I ask you, please, to
9 turn to Page 097.

10 A. Okay.

11 Q. And can you confirm for me that Page 097
12 is the December 5th, 2000 Office Action that we
13 were -- that's discussed in your declaration?

14 A. Yeah. The date mailed, according to
15 Page 097, was 12/05/2000.

16 Q. So you agree that this is the Office
17 Action that you are discussing in your declaration in
18 Paragraph 32?

19 A. (Reviewing document.)

20 Yes, that's -- is related to -- those are
21 the material that's discussed in Paragraph 32 and 33
22 and 34.

23 Q. Okay. So can I have you look at Page 101
24 of Exhibit 1102, please?

25 A. Okay.

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2 Q. It's the same Office Action?

3 A. Yes.

4 Q. Right?

5 A. Right.

6 Q. And I'm going to ask you some questions
7 about this page. Do you see here the examiner states
8 that certain claims are rejected "as being
9 unpatentable over Michihiro in view of Chen"? Do you
10 see that?

11 A. That's what it says there.

12 Q. And then on Page 101, the examiner states
13 that "Michihiro discloses a field oxide isolation
14 layer 2." Correct?

15 A. I believe that paragraph simply restate
16 the abstract of the Michihiro.

17 Q. So here the examiner states that
18 "Michihiro discloses in Figures 2(e) and 4(b)." Do
19 you see that?

20 A. And the abstract.

21 Q. Right. And then the examiner goes on and
22 says "a method of forming." Right? Do you see that?

23 A. No. It doesn't say that.

24 Q. What does it say?

25 A. "Forming a field oxide" -- earlier you

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2 said "disclosed a field oxide isolation layer." This
3 says "forming a field oxide layer" -- "oxide
4 isolation layer 2." Is that what you're referring
5 to?

6 Q. Yes. So he says -- would you agree that
7 the examiner here says "Michihiro discloses a field
8 oxide isolation layer 2"?

9 A. (Reviewing document.)

10 Yes. It says that the examiner said that
11 Michihiro discloses a list of things, including
12 "forming a field oxide isolation layer 2 on field" --
13 "on the field region."

14 Q. And can I -- you have your declaration in
15 front of you?

16 A. Yes.

17 Q. You were looking at it?

18 And when you were looking at the figures
19 in your declaration -- do you have those in front of
20 you, sir?

21 A. Figure 4(b)?

22 Q. Right.

23 A. And Figure 2(c)?

24 Q. Right.

25 A. Yes. Or 2(e). I'm sorry.

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2 Q. Right. So if you look at Figure 4(b) on
3 Page 14 of your declaration, do you agree with the
4 examiner that Michihiro discloses a field oxide
5 isolation layer 2?

6 MR. CHIU: Objection; relevance,
7 outside the scope.

8 A. Yes, I believe that Michihiro discloses
9 forming a field oxide isolation 2.

10 Do you have the Michihiro reference?

11 Q. (BY MR. MODI) I can get that for you.

12 A. Yes, please.

13 Q. Okay.

14 A. May I have that, please?

15 Q. I will get it for you.

16 A. May I have that, please?

17 Q. I will get it for you. Let me just ask
18 you one more question, and I will give it to you.

19 MR. MODI: Just note for record
20 the witness turned away from the examining
21 attorney and waited for his attorney to give him
22 the reference.

23 Q. (BY MR. MODI) So do you have the
24 Michihiro reference?

25 A. First of all, I did not turn away from the

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2 examining attorney. I simply looked back and -- and
3 waiting for the prior art that I asked for since you
4 refused to give it to me. So I think you
5 mischaracterized my action saying that I turned away
6 from the examining attorney. I simply looked back
7 and waiting for my prior art.

8 Q. Fine. You looked back.

9 So could you please tell me, what are you
10 looking at in front of you right now?

11 A. I'm looking at Exhibit 1104.

12 Q. And what is Exhibit 1104?

13 A. It is the prior art by Michihiro Yamada.

14 Q. So is this the reference that you were
15 looking for earlier from me?

16 A. Yes.

17 Q. Okay. So if you can go --

18 A. That you refused to give me.

19 Q. If you go to Page 101 of Exhibit 1102, I
20 asked you earlier whether on Page 101 the examiner
21 stated that Michihiro discloses a field oxide
22 isolation layer 2. Do you agree?

23 MR. CHIU: Objection; relevance,
24 outside the scope of Dr. Lee's declaration.

25 A. I believe I answered the question already.

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2 Q. (BY MR. MODI) And what is your answer,
3 sir?

4 A. If you look back, I said "Yes, I believe
5 that Michihiro discloses forming a field oxide
6 isolation 2."

7 Q. And then my next question was, can you
8 look at Figure 4(b) on Page 14 of your declaration
9 and let me know whether you agree that Michihiro
10 discloses a field oxide isolation layer 2.

11 MR. CHIU: Objection; relevance,
12 outside the scope of Dr. Lee's declaration.

13 A. (Reviewing document.)

14 Yes. The examiner stated that Michihiro
15 discloses a field oxide isolation layer 2. Yes, I
16 agree.

17 Q. (BY MR. MODI) My question was a little
18 different. I said, looking at Figure 4(b), do you
19 agree with the examiner's statement?

20 A. Well, Figure 4(b) shows layer 2. And
21 Figure 4(a) shows the plan view of the schematic of
22 this gate structure, n-Channel MOSFET, in the midst
23 of being fabricated.

24 So it appears that, although in the
25 specifications does not say specifically in

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2 Figure 4(a) and 4(b) what layer 2 is, however, in a
3 similar figure, such as Figure 2(a) to Figure 2(e),
4 that it show a device separation insulating film 2,
5 and a device separation insulating film is a field
6 isolation layer.

7 Q. So can I ask you to go back to Page 101 of
8 Exhibit 1102.

9 A. Okay.

10 Q. There the examiner states that "Michihiro
11 discloses forming a second pattern layer 15 on the
12 field isolation layer 2." Do you see that?

13 A. It says "simultaneously forming a second
14 pattern layer 15 on the field isolation layer 2."
15 Yes.

16 Q. Do you agree with that statement based on
17 your review of Michihiro?

18 MR. CHIU: Objection; form,
19 outside the scope of Dr. Lee's declaration, lacks
20 foundation.

21 A. (Reviewing document.)

22 In the specification of Hiroshima --
23 sorry -- Michihiro, when describing Figure 4(a) and
24 Figure 4(b), is a dummy pattern 15 are formed on the
25 device separating -- separation insulating film 2.

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2 So that dummy layer or dummy pattern is
3 what the examiner called that -- the second patterned
4 layer, and the device separation insulating -- or
5 insulation film 2 is what examiner called that the
6 field isolation layer 2.

7 Q. (BY MR. MODI) So you agreed with the
8 examiner?

9 A. So I agree that --

10 MR. CHIU: Same objections.
11 Objection; form, outside the scope of Dr. Lee's
12 declaration, lacks foundation.

13 A. So I agree that Michihiro discloses
14 forming a second patterned layer 15 on the field
15 isolation layer 2.

16 Q. (BY MR. MODI) So if I can have you now
17 look at Page 101 again of Exhibit 1102. The examiner
18 states, "Michihiro discloses forming a first pattern
19 layer 4a on the active region of the substrate spaced
20 apart from the field isolation region." Do you see
21 that?

22 A. Yes.

23 Q. Can you look at Figure 4(b) of Michihiro
24 and let me know whether you agree with the examiner?

25 MR. CHIU: Objection; form,

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2 outside the scope of Dr. Lee's declaration, lacks
3 foundation.

4 A. (Reviewing document.)

5 I disagree that Michihiro discloses
6 forming a first patterned layer 4a on the active
7 region of the substrate spaced apart from the field
8 isolation region.

9 Q. (BY MR. MODI) And why do you disagree?

10 A. Because -- I disagree because in this
11 particular prior art -- and that's why I asked for
12 this prior art, because it shows more information
13 than what I summarize in the declaration.

14 In this particular prior art of Michihiro,
15 normally it shows the cross-section but also shows
16 the plan view of the device. And the device and the
17 plan view discloses that the first patterned layer
18 4a -- in fact, 4b and 4c -- is not spaced apart from
19 the field isolation region.

20 Q. And why is that?

21 MR. CHIU: Objection; asked and
22 answered, form, lacks foundation, outside the
23 scope of Dr. Lee's declaration.

24 A. As a person of ordinary skill in the art
25 would understand from Figure 4(a), which is the plan

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2 view of the device, that the first patterned layer
3 touches and crosses over the field isolation layer.
4 So, therefore, the first patterned layer is not
5 spaced apart from the field region.

6 Q. (BY MR. MODI) So you would disagree with
7 the examiner's interpretation of "spaced apart" here?

8 MR. CHIU: Objection; form, lacks
9 foundation, outside the scope of Dr. Lee's
10 declaration, calls for speculation.

11 A. I believe that a device is a
12 three-dimensional device. It's not a 1-D or 2-D
13 device. So one -- especially in this particular
14 patent, it shows not only one cross-section but also
15 the plan view of the device. One can see that the
16 first patterned layer touches and crosses over the
17 field region, so therefore it is not spaced apart.

18 So I disagree with the examiner
19 interpretation of "spaced apart." I don't know what
20 his -- what the examiner interpretation of "spaced
21 apart," but I disagree with the conclusion that the
22 examiner made, which is that -- let me read that --
23 that "a first pattern layer 4a on the active region
24 of the substrate spaced apart from the field
25 isolation region."

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2 Q. (BY MR. MODI) So for you to determine
3 whether something is spaced apart in the context of
4 this case, what interpretation are you using,
5 Dr. Lee?

6 MR. CHIU: Objection; form.

7 A. When you say "something," don't -- are you
8 referring to the first patterned layer.

9 Q. (BY MR. MODI) I'm asking you --

10 A. I don't understand what you mean by
11 "something is spaced apart."

12 Q. So we can go with the first patterned
13 layer.

14 A. Huh?

15 Q. We can go with the first pattern spaced
16 apart.

17 MR. CHIU: Objection; form.

18 A. I still don't understand what you mean by
19 "the first pattern is spaced apart."

20 Q. (BY MR. MODI) So what I'm asking you
21 is --

22 A. From what?

23 Q. Fair enough.

24 We were looking at Page 101 of
25 Exhibit 1102. Right?

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2 A. Yes.

3 Q. And there it says "forming a first pattern
4 layer 4a on the active region of the substrate spaced
5 apart from the field isolation region." Do you see
6 that?

7 A. Yes.

8 Q. And you just told me that, in your
9 opinion, Michihiro does not disclose that feature.
10 Do you agree?

11 A. That is correct.

12 Q. Okay. In coming to that answer, what
13 interpretation of "spaced apart" are you relying on?

14 MR. CHIU: Objection; form.

15 A. "Spaced apart" means not touching and not
16 crosses over.

17 Q. (BY MR. MODI) And that is the
18 interpretation you have applied in this case?

19 MR. CHIU: Objection; form.

20 A. I think that's the interpretation I apply
21 in analyzing the '902 patent, and so would a person
22 of ordinary skill in the art would apply in analyzing
23 the '902 patent and the prior arts.

24 Q. (BY MR. MODI) So if a gate extends to the
25 field oxide region, is it your opinion that such a

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2 gate cannot be spaced apart from the field oxide
3 region?

4 MR. CHIU: Objection; form, lacks
5 foundation, incomplete hypothetical.

6 A. Well, Figure 4(a) does show that the gate
7 extends to, touches the field region, and even
8 crosses over the field region, so the first patterned
9 layer, which is what you call the gate, is not spaced
10 apart from the field oxide region.

11 So if a gate extends to the field oxide
12 region, understand that when you say "extend to," it
13 means touching or crosses over. Correct? Then it's
14 my opinion, and I believe that it is the opinion of a
15 person of ordinary skill in the art would conclude
16 that such a gate is not spaced apart from the field
17 oxide isolation region -- isolation layer. Not
18 region. Well, isolation region, isolation layer.

19 Q. (BY MR. MODI) Can you ever tell, without
20 looking at a plan view of a device, whether the gate
21 is spaced apart from the field oxide region?

22 MR. CHIU: Objection; form, lacks
23 foundation.

24 A. Well, there are other ways of concluding
25 whether a gate is spaced apart from the field region

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2 or not. In addition to looking at the plan view,
3 there is other ways of determining that, such as
4 description on the -- and the specification or the
5 body of the article and other things, such as the
6 other cross-section view.

7 Q. (BY MR. MODI) So let's look at Michihiro.
8 Right. You looked at Figure 4(a) in Michihiro, which
9 discloses the plan view. You agree?

10 A. Yes, that's what it says. It's a plan
11 view showing the schematic structure of the metal
12 gate electrodes n-Channel MOSFET.

13 Q. Assuming Michihiro did not have
14 Figure 4(a), with that assumption, can you tell me
15 whether your answer would change?

16 MR. CHIU: Objection; form,
17 outside the scope of Dr. Lee's declaration, lacks
18 foundation, incomplete hypothetical.

19 A. If Figure 4(a) is absent from the patent,
20 your question is whether one can conclude the gate is
21 spaced apart from the field isolation region or not?

22 Q. (BY MR. MODI) That's right.

23 A. And I believe that without the plan view,
24 one would have to look into the specifications to see
25 if there's any descriptions of the fabrications or

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2 the design of the device to make that conclusion.

3 Q. And can you go ahead and look at Michihiro
4 and let me know if Figure 4(a) and the corresponding
5 description wasn't there, what would your answer be?

6 MR. CHIU: Objection; form,
7 outside the scope of Dr. Lee's declaration, lacks
8 foundation, incomplete hypothetical.

9 A. Well, I have not read this for a long
10 time, so it's going to take me a while to read
11 through this.

12 MR. CHIU: Counsel, this is
13 outside the scope of his declaration. Do you
14 really intend to make him sit here and review
15 this patent to answer your question?

16 MR. MODI: Counsel, I'll ask you
17 not to -- stop making speaking objections and
18 coaching the witness. Now you are crossing the
19 line.

20 MR. CHIU: No, no. I'm addressing
21 you. This is outside the scope of his
22 declaration.

23 MR. MODI: No, no, you're not.
24 You're addressing the witness and you have done
25 that in the past. So I would --

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2 MR. CHIU: This is outside the
3 scope of his declaration.

4 MR. MODI: Let me finish. Let me
5 finish. If you want to go ahead -- why don't you
6 go ahead then?

7 MR. CHIU: I mean, do you want to
8 take this up with the PTAB?

9 MR. MODI: We can.

10 MR. CHIU: Because this is clearly
11 outside the scope of his declaration.

12 MR. MODI: He has discussed
13 Michihiro and the prosecution history in his
14 declaration.

15 MR. CHIU: And nothing to do with
16 these issues.

17 MR. MODI: I disagree.

18 MR. CHIU: Michihiro has nothing
19 to do with these issues.

20 Q. (BY MR. MODI) So, Dr. Lee, can you please
21 answer my question?

22 MR. CHIU: So this is outside the
23 scope of his declaration. And you're sitting
24 here and making him review an entire patent in
25 trying to come up with an answer to your

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2 question.

3 Same objections, form, outside the
4 scope of Dr. Lee's declaration, lacks foundation,
5 incomplete hypothetical.

6 A. Well, even without Figure 4(a), there is
7 Figure 2, Figure 1(a), Figure 3(a), Figure 3(b),
8 Figure 3(c) of similar devices, Figure 6(a),
9 Figure 8(a).

10 So without Figure 4(a), one would --
11 looking at the other figures, one would conclude that
12 if a similar fabrication sequence is used to
13 fabricate Figure 4(b), the device shown in
14 Figure 4(b), one would conclude that a -- that the
15 first patterned layer is not spaced apart from the
16 field isolation layer.

17 Q. (BY MR. MODI) Okay. What if we took away
18 the figures showing the plan view, would your answer
19 change?

20 MR. CHIU: Again, counsel, this is
21 all outside the scope of his declaration. Should
22 we address this with the PTAB? We can give them
23 a call right now.

24 I'm going to instruct the witness
25 not to answer any more of this line of

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2 questioning. If you want to take it up with the
3 PTAB, we can give them a call.

4 MR. MODI: So are you instructing
5 him not to answer?

6 MR. CHIU: Yes. This is all
7 outside the scope of his declaration.

8 MR. MODI: So I haven't heard you
9 instruct the witness not to answer.

10 MR. CHIU: Okay. Well, I'm going
11 to instruct the witness not to answer the
12 question. Do you want to call the PTAB?

13 MR. MODI: Well, I'll consider it.
14 That's fine. If that's your objection, you can
15 obviously make it and tell your witness not to
16 answer.

17 MR. CHIU: Okay. Well, I've
18 instructed him not to answer. This is all
19 outside the scope of his declaration, form, lacks
20 foundation, incomplete hypothetical, so...

21 MR. MODI: So is it your position
22 that issues relating to "spaced apart" are
23 outside the scope of his declaration?

24 MR. CHIU: No. There are -- there
25 is discussion in his declaration of "spaced

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2 apart," but you're going to a reference that was
3 never used in connection with that issue. And he
4 has some discussion of Michihiro in the
5 declaration. None of that has to do with "spaced
6 apart."

7 So you're clearly going outside
8 the scope of his declaration and you're asking
9 him to review a multipage patent on the fly to
10 answer vague and incomplete hypotheticals.

11 MR. MODI: Okay. You've stated
12 your objection and we'll -- we'll consider
13 whether we want to call the board or not.

14 Let's take a break.

15 (Break.)

16 Q. (BY MR. MODI) Dr. Lee, welcome back from
17 lunch. Did you talk to your attorneys about the
18 substance of your testimony during lunch?

19 A. No.

20 Q. Did you look at any documents during
21 lunch?

22 A. No.

23 Q. Do you have the Lee reference in front of
24 you?

25 A. Yes.

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2 Q. And just for the record, what exhibit is
3 it?

4 A. That would be 1107.

5 Q. Can I have you go to Paragraph 39 of your
6 declaration?

7 A. 39?

8 Q. Yes.

9 A. Okay.

10 Q. Can you read the last sentence of
11 Paragraph 39 into the record for us?

12 A. "Lee is thus prior art to the '902 patent
13 under 35 U.S.C. 102(a)."

14 Q. And there do you agree that you're talking
15 about Exhibit 1107?

16 A. Lee is the prior art, and is in the
17 Exhibit 1007.

18 Q. So that sentence refers to Exhibit 1107.
19 Right?

20 A. Yes, sir. I think so. Yes, I agree.

21 Q. Okay. In here you refer to that it's
22 prior art under 35 U.S.C. 102(a). What do you mean
23 by that?

24 A. 102(a) -- let's see. I forgot all these
25 102(b), 102 -- you're the lawyer. Can you explain

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2 what is 102(a)? I forgot what this is.

3 Q. It's your opinion, Dr. Lee.

4 A. Yeah, I know. I do not remember what is
5 102(a).

6 Q. So sitting here today you don't know what
7 you meant when you wrote this?

8 A. No, I knew what --

9 MR. CHIU: Objection; form.

10 A. I knew what I meant when I wrote this.
11 The attorney explained to me what is 102(a), but I
12 just don't remember all these legal meaning, legal
13 terms, 102(a), 102(b), or whatnot. I don't remember.

14 Q. (BY MR. MODI) Do you agree with this
15 statement, sir?

16 A. Yes. When I wrote it, I have a clear
17 understanding of what it is, and I agree with it.

18 Q. Okay. So what is the basis for that
19 statement?

20 A. Well, I don't remember exactly what is
21 102(a). However -- that under -- that the basis of
22 the statement is that the Lee reference is published
23 prior to the '902 patent; in other words, that the
24 Lee patent is a printed publication as of March 22,
25 1996. And the Lee patent -- and the '902 patent was

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2 filed after that date. The priority date is after
3 March 22nd, 1996. Let me see...

4 (Reviewing document.)

5 The priority date is June 28, 1996. The
6 '902 patent.

7 Q. Can I have you read the statement, the
8 second-to-last sentence in Paragraph 39 of your
9 declaration, Exhibit 1116?

10 A. "Based on my understanding of the law
11 constituting a printed publication for the purposes
12 of prior art, the Korean Patent Office's laying-open
13 process is sufficient to make Lee a printed
14 publication as of March 22nd, 1996."

15 Q. What did you mean when you said "based on
16 my understanding of the law constituting a printed
17 publication for purposes of prior art"?

18 MR. CHIU: Objection; form.

19 A. Well, my understanding is that the Lee --
20 that the Korean application was filed in August 27 of
21 1994, but, accordingly, that the patent -- Korean
22 Patent Office actually published a patent gazette for
23 the publications, and that was on March 22nd of 1996,
24 which provides all the information that I listed in
25 Paragraph 39, the applicant, application number,

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2 classification code, filing date, inventors,
3 application publication number, the date of
4 publications, the title of the invention and the
5 scope of patent claims, the drawings, priority
6 claims, summary, and other matters for the Lee
7 application.

8 So, as such, that the priority date is
9 March 22nd, 1996, that's my understanding.

10 Q. (BY MR. MODI) And where did you gain this
11 understanding from?

12 A. Well, as you know, I'm not a lawyer. So
13 this is an information that the attorney that I work
14 with -- attorneys that I work with explained to me
15 the process, particularly with the Korean
16 applications and the Korean Patent Office and what
17 they call the Patent Gazette, and -- and that's how I
18 got the information about the process of the
19 prosecutions of the Lee patent.

20 Q. So it would be fair to say that it was
21 based on your discussions with the attorneys?

22 MR. CHIU: Objection; form.

23 A. (Reviewing document.)

24 Well, through the discussion and a clear
25 explanations of the process. And if I recall

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2 correctly, they even show me some, like -- an
3 illustration of what a Patent Gazette looked like.
4 And so, yeah, it's -- the understanding of the law is
5 really through other -- through explanation of the
6 legal issues and matters by the attorney, obviously,
7 because I'm not a lawyer.

8 Q. (BY MR. MODI) Okay. And then here you
9 say, "The Korean Patent Office's laying-open
10 process." Do you see that?

11 A. Right.

12 Q. What is your understanding of the Korean
13 Patent Office's laying-open process?

14 A. I believe that -- my understanding, again,
15 if I recall correctly, is that the -- those who get
16 access to the Patent Gazette can have and access and
17 request for the full Korean applications. That's my
18 understanding.

19 Q. And how did you gain that understanding,
20 Dr. Lee?

21 A. Again, I'm not a lawyer. That's explained
22 by the attorney that I work with.

23 Q. So would it be fair to say that -- well,
24 let me ask you this way.

25 Do you have any personal knowledge with

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2 respect to the Korean Patent Office's laying-open
3 process?

4 MR. CHIU: Objection; form.

5 A. My personal knowledge is a knowledge that
6 is taught by my attorney and also previous cases that
7 I worked with -- worked on about --

8 Q. (BY MR. MODI) So you --

9 A. -- about Korean Patent Office. The
10 previous cases that I also involved with Korean
11 Patent Office, so that -- through that, I also gained
12 a little bit of understanding.

13 Q. And how did you gain that understanding of
14 those previous cases?

15 A. Obviously is by explanation with --
16 from -- by the attorneys that I work with.

17 Q. Okay. So other than the -- what the
18 attorneys have told you about the Korean Patent
19 Office's laying-open process --

20 A. Right.

21 Q. -- do you have any other knowledge with
22 respect to the Korean Patent Office's laying-open
23 process?

24 MR. CHIU: Objection; form.

25 A. Mostly it's from all the previous cases

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2 and current case that attorney explained the legal
3 issues, and in this, you know, case, particularly
4 about the Patent Office in Korea laying-open process.

5 But in the past, I have discussed with
6 other colleagues who are also serve as -- serving as
7 expert witness, and we discuss, you know, legal
8 definitions and things like that. And so other than
9 the attorney directly, I also gained a little bit of
10 knowledge from discussion with other colleague as
11 well.

12 Q. (BY MR. MODI) Okay. So let me get this
13 straight. So these discussions with your other
14 colleagues --

15 A. Right.

16 Q. -- these related to the Korean office's
17 laying-open process?

18 A. No, I don't recall. I recall discussion
19 of different patent offices at different countries
20 and -- but I don't recall a particular laying-open
21 processes. And so, yeah, I -- no, it's -- most of it
22 is really understanding from the -- education from
23 the attorney. And most of the -- no, go ahead.

24 Q. Finish your thought.

25 A. No. Go ahead.

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2 Q. I was going to say, you keep on saying
3 "most."

4 A. Yeah.

5 Q. So I'm trying to get what's left.

6 A. What's left of what?

7 Q. You keep saying most of your knowledge
8 about this Korean Patent Office's laying-open process
9 is coming from attorneys. So I'm trying to get at,
10 to the extent you have any other knowledge, where did
11 it come from?

12 A. I think that the reason why I said "most"
13 is because I don't recall a lot of the conversations
14 that I have with other colleagues and whether we talk
15 about this or not. But I don't recall that. But
16 perhaps we did.

17 So you talked -- you asked about Korean
18 Patent Office. We did talk about that. But talking
19 about patent -- what did you say? -- laying-open
20 process? I don't recall. But that doesn't mean that
21 we haven't talked about it. I don't recall.

22 Q. Sitting here today, other than you
23 recalling that you've had discussions with attorneys
24 regarding the Korean Patent Office's laying-open
25 process, would it be fair to say that you don't have

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2 any other knowledge about the Korean Patent Office's
3 laying-open process?

4 A. I don't recall.

5 Q. Sitting here today, you don't have --

6 A. Yeah, I don't --

7 Q. -- have any recollection?

8 A. I don't recall whether we have -- whether
9 I have discussed Korean patents laying-open process
10 with attorney other than -- with anyone other than
11 attorneys.

12 Q. Would it be fair to say that you're an
13 expert in semiconductors? Is that right?

14 A. Yes.

15 Q. And would it be fair to say that you're
16 not an expert in Korean Patent Office's laying-open
17 process?

18 MR. CHIU: Objection; form.

19 A. Yeah. I mean, I don't claim to be an
20 expert in Korean Patent Office laying-open process.
21 No, I'm not.

22 Q. (BY MR. MODI) And sitting here today --

23 A. I'm sure you -- go ahead.

24 Q. Go ahead. Finish your thought.

25 A. Oh, I said, I'm sure you are, but I'm not.

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2 Q. And sitting here today, the only thing you
3 can recall in terms of learning about the Korean
4 Patent Office laying-open process is from your
5 attorneys. Is that right?

6 MR. CHIU: Objection; form.

7 A. From the -- my attorneys in this and other
8 cases. And perhaps other -- other colleagues, but I
9 don't recall exactly.

10 Q. (BY MR. MODI) Do you consider yourself an
11 expert who can opine on what is or is not a printed
12 publication?

13 MR. CHIU: Objection to form.

14 A. By legal definition you mean, when you say
15 "printed publications"?

16 Q. (BY MR. MODI) As it's understood in your
17 declaration or as you've used it in your declaration.

18 So let me -- let me simplify it for you,
19 Dr. Lee. Do you consider yourself as an expert on
20 whether a particular publication is a printed
21 publication, as you've used the term "printed
22 publication" in your declaration?

23 A. Well, I have some opinion of whether the
24 particular publication is a printed publication or
25 not. But in terms of under the law, I believe that

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2 I'm definitely not an expert. But as explained by my
3 attorneys and also others, that based on the
4 explanation and my understanding of the law,
5 particularly related to this case, that a printed
6 publication for the purpose of the prior art, that
7 Lee is a printed publication as of March 22nd, 1996.

8 Q. Can I have you turn on Paragraph 44.

9 A. Okay.

10 Q. In Paragraph 44 you say, "Yasushige was
11 published on March 31st, 1995 and is thus prior art
12 to the '902 patent under 35 U.S.C. Section 102(b)."
13 Do you see that?

14 A. Yes.

15 Q. Do you feel you're qualified to make
16 representations about whether a prior reference is
17 prior art under a particular statute?

18 MR. CHIU: Objection; form.

19 A. May I see Yasushige?

20 Q. (BY MR. MODI) I'll give it to you.

21 (Hands document to witness.)

22 A. Thank you, sir.

23 So do you have a question? I'm sorry.

24 "Do you remember representations about
25 whether a prior art" --

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Q. Dr. Lee, let me ask my question again.

A. Okay.

Q. Do you consider yourself -- so do you consider yourself to be an expert who can opine on whether a particular patent or patent publication is prior art under the particular section of this statute?

MR. CHIU: Objection; form, lacks foundation.

A. You mean particular -- by particular sections of the statute, you mean, like, 35 U.S.C. 102(b) or 102(a)? No, I'm not an expert in that, although I know that the Yasushige was published in March 31st, 1995.

Q. (BY MR. MODI) Dr. Lee, you've answered my question, so I need to move on.

MR. CHIU: Do you have anything you want to clarify?

If he wasn't finished, don't cut him off.

Q. (BY MR. MODI) Your counsel can ask you on redirect if he has questions. I think I'm going to move on.

MR. CHIU: Did he cut you off?

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2 THE WITNESS: I'd like to clarify
3 my answer.

4 Q. (BY MR. MODI) Dr. Lee, you can clarify
5 your answer, like I said, when your attorney asks you
6 questions on redirect.

7 A. Well, it was published March 31st, 1995,
8 so therefore it is a prior art to the '902 patent.

9 And, by the way, it was not before the
10 examiner during the prosecution of the '902 patent.

11 MR. MODI: Move to strike that as
12 nonresponsive.

13 Q. (BY MR. MODI) Can we go to the Lee
14 reference, please?

15 A. What exhibit is this?

16 Q. 17-6.

17 A. I beg your pardon?

18 Q. I'm sorry. It's 1107. Do you have it?

19 A. Yes.

20 Q. Do you have it?

21 A. Yes.

22 Q. Do you agree that the Lee reference
23 describes a fabrication method for a semiconductor
24 device?

25 MR. CHIU: Objection; form.

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2 A. Well, on a high level, the Lee reference
3 relates to fabricating a semiconductor device. But
4 more specifically, it's related to or pertained to a
5 method of fabricating a semiconductor device in which
6 the characteristics of the device is improved by
7 securing an alignment margin when it's forming the
8 contact hold. So it's not -- it is related to
9 fabrication of semiconductor device.

10 Q. (BY MR. MODI) Can I have you look at
11 Figure 1 of Lee. Do you agree that it describes the
12 prior art structure?

13 A. Figure 1 of the drawing is a drawing of
14 the prior art of Lee, yes.

15 Q. Do you agree that the prior art structure
16 includes a gate 14 on a semiconductor substrate 11?

17 A. (Reviewing document.)

18 Yeah, in Figure 1(a) it disclosed the
19 cross-section view of a semiconductor device in which
20 a MOS gate, M-O-S, gate 14 is formed on a
21 semiconductor substrate, 11.

22 Q. So the answer is yes? I'll ask you again.

23 The prior art structure in Figure 1 of Lee
24 includes a gate 14 on a semiconductor substrate 11?

25 MR. CHIU: Asked and answered.

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2 Objection.

3 A. You're referring to Figure 1(a) or
4 Figure 1(b)?

5 Q. (BY MR. MODI) Figure 1(a).

6 A. Figure what?

7 Q. 1(a).

8 A. 1(a).

9 MR. CHIU: Objection; asked and
10 answered.

11 A. Yes. I mentioned that as -- the prior art
12 structure in Figure 1(a) shows an MOS gate No. 14 on
13 a semiconductor substrate 11.

14 Q. (BY MR. MODI) So the gate 14 is a gate of
15 a MOSFET. Right?

16 A. Yes. This is a MOSFET structure, and 14
17 is the gate of that structure.

18 Q. The MOSFET has a source region and a drain
19 region. Right?

20 A. That's right. And it's illustrated in
21 region 13.

22 Q. And the Lee reference also describes
23 certain problems with the prior art structure of
24 Figure 1. Right?

25 A. Are you referring to Figure 1(b)?

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2 Q. Either Figure 1(a) or 1(b).

3 A. Figure 1(a) doesn't -- doesn't illustrate
4 certain problems of the prior art structure.
5 Figure 1(b) depicts a certain problem associated with
6 the prior art structure.

7 Q. Do you agree that the Lee reference is
8 concerned that a contact hole form to contact the
9 source of drain region of the MOSFET may be
10 misaligned?

11 MR. CHIU: Objection; form.

12 A. Well, it's showing an alignment accuracy.
13 Figure 1(b) describes the alignment accuracy issues
14 of the photolithography process.

15 Q. (BY MR. MODI) So do you agree that the
16 Lee reference is concerned that a contact hole formed
17 to contact the source of drain region of the MOSFET
18 may be misaligned?

19 MR. CHIU: Objection; asked and
20 answered, form.

21 A. Yeah. In Figure 1(b) it shows that when a
22 misalignment occurs, that the gate is damaged and
23 possibly the field oxide is also damaged, which lead
24 to leakage occurring, particularly junction leakage.

25 Q. (BY MR. MODI) So, Dr. Lee, I'm going to

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2 ask the question again. If you can't give me a yes
3 or no, can you tell me why? Because I'm going to ask
4 you the question again.

5 So does the Lee reference concern that a
6 contact hole formed to contact the source of drain
7 region of the MOSFET may be misaligned, yes or no?

8 MR. CHIU: Objection; asked and
9 answered. He said "yeah" in his response.

10 Q. (BY MR. MODI) Dr. Lee, what is your
11 answer, yes or no?

12 A. Well, I think I did answer that.

13 MR. CHIU: Objection; asked and
14 answered.

15 Q. (BY MR. MODI) And what is your answer,
16 sir?

17 A. Can you read that? It said, "Yes. And
18 Figure B shows when a misalignment occurs, that the
19 gate is damaged and possibly the field oxide is also
20 damaged, will lead to junction leakage."

21 MR. MODI: Counsel, I'm going to
22 warn you one last time. If you make one more
23 speaking objection, we're going to call the
24 board.

25 Let's mark that objection.

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2 Q. (BY MR. MODI) And I think you would
3 agree, Dr. Lee, that when the contact hole is
4 misaligned, the field oxide layer may be damaged,
5 causing junction leakage. Right?

6 MR. CHIU: Objection; form, lack
7 of foundation.

8 A. Well, as I said earlier, that when a
9 misalignment occurs, then the gate is damaged and the
10 field oxide could also be damaged, which lead to
11 leakage. And I believe that's what I said. And then
12 you're rephrasing that, and asked me whether that's
13 right or wrong. Obviously that's right.

14 Q. (BY MR. MODI) So would one solution to
15 the misalignment problem be to make the contact hole
16 smaller so that the chances of misalignment and
17 damaging of the field oxide layer become lesser?

18 MR. CHIU: Objection; form.

19 A. (Reviewing document.)

20 MR. CHIU: Outside the scope of
21 Dr. Lee's declaration.

22 A. (Reviewing document.)

23 Wait. What are you asking me? That's
24 ridiculous. Making a contact hole smaller? What do
25 you mean by that?

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2 Q. (BY MR. MODI) What don't you understand,
3 Dr. Lee?

4 A. Technically, how do you make the contact
5 hole smaller, and that the chances of misalignment
6 and damaging the field oxide become lesser? Can you
7 clarify what -- what -- what invention are you doing?
8 What are you talking about?

9 Q. What don't you understand, Dr. Lee?

10 A. Explain your question, please.

11 Q. So when we're talking about the contact
12 hole smaller, we're talking about the -- reducing the
13 diameter of the hole.

14 A. Huh?

15 Q. Reducing the diameter of the hole, the
16 contact hole. Okay?

17 MR. CHIU: Objection; form,
18 outside the scope.

19 A. So you're assuming that the contact hole
20 is circular?

21 Q. (BY MR. MODI) Let's assume that.

22 A. Okay.

23 MR. CHIU: Objection; form.

24 Q. (BY MR. MODI) With that assumption, would
25 you agree that one solution to the misalignment

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2 problem will be to make the contact hole smaller so
3 that the chances of misalignment and damaging the
4 field oxide layer becomes less?

5 MR. CHIU: Objection to form,
6 outside the scope, incomplete hypothetical.

7 A. What process node are you talking about?

8 Q. (BY MR. MODI) What process node is the
9 Lee reference talking about?

10 MR. CHIU: Objection; outside the
11 scope.

12 A. Well, this is so hypothetical scenario.
13 Back in 1996, depending on the process, depending on
14 the etching, depending on the minimum feature size --
15 are you saying that you make the contact hole even
16 smaller than minimum feature size? Is that what
17 you're talking about?

18 I mean, in order to answer your question
19 you got to give me the boundary conditions, given A,
20 B, C, D, E. Right? If you don't define the boundary
21 conditions and just arbitrarily say "making the
22 contact hole smaller," smaller than what?

23 Q. (BY MR. MODI) So let's assume we've been
24 talking about Lee. Right? The Lee reference, yes?
25 We've been talking about the Lee reference, Dr. Lee?

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2 A. Well, we've been talking about my
3 declaration, the Lee, Yasushige, yes.

4 Q. In the last few minutes we've been talking
5 about the Lee reference?

6 A. Yes.

7 Q. In the context of the Lee reference, my
8 question is one solution to the misalignment problem
9 would be to make the contact hole smaller so the
10 chances of misalignment and damaging the field oxide
11 layer become lesser. Do you agree?

12 MR. CHIU: Objection; form, lacks
13 foundation, incomplete hypothetical, outside the
14 scope.

15 A. (Reviewing document.)

16 MR. CHIU: I also had a form
17 objection in there too.

18 A. (Reviewing document.)

19 Okay. I'm trying to understand
20 technically what your question is. Making the
21 contact hole smaller. I mean, in general when you
22 try to make the dimensions in smaller size for the
23 purpose of high-density integration, right, and that
24 things become even more difficult. I don't
25 understand what you mean by making the problem

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2 lesser.

3 Q. (BY MR. MODI) Let me -- do you have the
4 '902 patent in front of you?

5 A. No, I don't.

6 Q. Okay. Let me hand you what's previously
7 marked as Exhibit 1101.

8 A. Uh-huh.

9 Q. Can you identify Exhibit 1101 for us,
10 please?

11 A. It is the U.S. Patent No. 6,287,902.

12 Q. Yes.

13 A. B1.

14 Q. So it's the '902 patent?

15 A. Yes.

16 Q. Can I have you turn to Column 1, Lines 36
17 through 40? Why don't you read that to yourself, and
18 if you need more context, go ahead and read the
19 passage around it.

20 A. (Reviewing document.)

21 Okay.

22 Q. What is your understanding of this
23 passage?

24 A. Well, it talk about that when the space in
25 patent layer is reduced, then the space that's

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2 allowed for forming the holes, contact holes, may
3 also be reduced. Right? And that there is a
4 physical limit in terms of how much -- how small you
5 can have that hole. And so, in other words, that
6 when you have the integration density increases, the
7 margin allowed or available for the placement of the
8 hole becomes smaller. Right?

9 And that this margin, of course, depends
10 on many things is what they are -- what they are
11 saying. It depends on the etching process, the
12 process limitation of all these steps of forming
13 adjacent pattern, and whether the isolation layer,
14 the field isolation layer, is whether it's made by
15 trench isolation or so-called low-cost isolation. It
16 also describes the difference between low cost and
17 trench, that low cost encroach into the active region
18 more than the trench isolation. And that would even
19 reduce the margin for the formation of the hole.

20 So basically that is talk about the
21 problem associated with reducing the size and
22 increasing the integration density. That's why I was
23 very confused about what you said, that reducing the
24 size of the hole can make the problem lesser. That's
25 why I was like, whoa, wait a minute.

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2 Q. So let me see if I -- if I can try to get
3 at what I was trying to get at earlier.

4 A. Yeah.

5 Q. So would you agree that reducing the size
6 of the contact hole, wouldn't it be possible that the
7 margin available in the placement of the contact
8 holes increases?

9 A. No. You're just saying the opposite of
10 what this says right here.

11 Q. So you disagree with that statement?

12 A. What exactly are you saying? The size of
13 the contact hole.

14 Q. Hole, H-O-L-E.

15 A. The margin available increases.

16 Are you saying that the size of the
17 holes -- contact holes is below the minimum feature
18 size? How do you make it smaller than it already is?
19 I mean, this is just saying the opposite of what
20 you're proposing. The increased integration reduces
21 the margin available in the placement of holes.

22 In other words, if you make things
23 smaller, the margins available in placement of the
24 hole become less.

25 Q. Okay. So let's --

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2 A. So I don't get your proposal.

3 Q. Okay. So let's assume that the contact
4 hole is more than the minimum feature size. Okay?

5 A. Okay.

6 Q. Would you agree that if we bring the
7 contact hole size -- if we reduce that, the margin
8 would increase?

9 MR. CHIU: Objection; form,
10 outside the scope, lacks foundation, incomplete
11 hypothetical.

12 A. Well, what is your -- what is the gate
13 dimension? Can you give me some parameters? What is
14 the gate dimension? What is the source string
15 dimension? What is the contact etch recipe? What is
16 the isolation process?

17 Unless you give me all these parameters,
18 there is -- you know, you can't answer this
19 hypothetical question because in general you -- if
20 you understand the microprocessor process, right,
21 microelectronic process, when you increase
22 integrations, when you make the size smaller, you
23 reduce the margins available in placement of contact
24 holes or other layers or other -- other pattern. So
25 I just confused about your parameters.

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2 Q. (BY MR. MODI) Would you agree that a
3 contact hole in the context of the '902 patent is an
4 electrical connection between the first metal layer
5 and transistor regions?

6 MR. CHIU: Objection; form.

7 A. So you're saying that is the contact hole
8 in the context of the '902 patent the electrical
9 contact between the first metal layer and the
10 transistor region.

11 When you say "transistor region" you mean
12 the source drain region?

13 Q. (BY MR. MODI) Yes.

14 A. Yes. As shown in the figure, and as
15 described in the '902 patent, the contact holes are
16 made for microelectronic structure which has an
17 active region and a field region, but is not
18 necessarily about transistor alone. It could be
19 applied to other microelectronic devices, such as
20 capacitors and other microelectronics device. So
21 it's not just to the source and drain region.

22 Q. Would you agree that contact hole is an
23 electrical connection between a first metal layer,
24 say, Metal 1, and transistor regions?

25 MR. CHIU: Objection; asked and

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2 answered, form, lacks foundation.

3 A. In the context of '902 or in general?

4 Q. (BY MR. MODI) We can start in the context
5 of '902.

6 A. Well, in the context --

7 MR. CHIU: Objection; asked and
8 answered, form, lacks foundation.

9 A. In the context of '902, the contact hole
10 is an electrical connection between the first metal
11 layer and the device -- and the microelectronic
12 devices. It could be transistor or capacitors and
13 other microelectronic devices, such as a diode. So
14 it's not limited to transistor regions.

15 Q. (BY MR. MODI) Would you agree that it is
16 an electrical connection between the first metal
17 layer and the active region?

18 MR. CHIU: Objection; form, lacks
19 foundation, incomplete hypothetical.

20 A. Well, in the -- in the claims it talks
21 about forming a contact hole in the isolation
22 layer -- in the insulating layer, I'm sorry -- and
23 exposing a portion of the active region. But the
24 specification talks about this can be applied to
25 capacitors and other microelectronic devices. So

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2 capacitor -- it could be that it's a contact opening
3 to the underlying capacitors.

4 Q. (BY MR. MODI) And where are you looking
5 at when you said in this specification?

6 A. Well, if you look at Column 2.

7 Q. Okay. Where in Column 2?

8 A. Line 23. It says, "If a capacitor is
9 formed, then the life of the capacitor may be
10 reduced."

11 And in the introduction it also say that
12 it's a -- the present invention relates to
13 microelectronic structure, which is not limited to
14 transistors. And also integration -- integrated
15 circuit memory devices.

16 Q. So, Dr. Lee, why does one need to contact
17 the source and drain region?

18 MR. CHIU: Objection; lacks
19 foundation, outside the scope, form.

20 A. How do you communicate the source and
21 drain to the external world without contact?

22 Q. (BY MR. MODI) So if you go back to Lee --

23 A. Yes.

24 Q. -- would you agree that the same logic
25 would apply in that the MOSFET gate also needs a

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2 contact to provide a voltage signal to the gate?

3 MR. CHIU: Objection;
4 mischaracterizes testimony.

5 A. What do you mean, "same logic"?

6 Q. (BY MR. MODI) Well, why we use contact
7 holes.

8 MR. CHIU: Objection; form.

9 A. That the contact hole is made in order to
10 have contact to the metal lines such that it can
11 communicate it to the rest of the circuit. Is that
12 what you're saying?

13 Q. (BY MR. MODI) Uh-huh.

14 A. Yeah, of course. There will be contact to
15 the gate, to the source drain, and to other
16 microelectronic devices on the substrate.

17 MR. MODI: Let's take a break.

18 (Break.)

19 Q. (BY MR. MODI) Dr. Lee, during the break,
20 did you talk to your attorney about the substance of
21 your testimony?

22 A. No.

23 Q. Did you review any documents?

24 A. No.

25 Q. So I understand that you're an expert.

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2 Would you say you're an expert in semiconductor
3 fabrication?

4 A. Yes.

5 Q. And you have over 200 journal publications
6 that deal with semiconductor fabrication. Right?

7 A. Where did you get the number 200?

8 Q. Let me take the number out. How about if
9 I just say that you have several journal publications
10 dealing with semiconductor fabrication?

11 A. I think it's more than several.

12 Q. Before you publish these articles, do you
13 test the theories you're publishing in your articles?

14 A. I'm not sure if I understand your
15 question. What theories?

16 Q. The topics that -- that are discussed in
17 your publications.

18 A. Do I test the topics? I don't understand.
19 What do you mean by that?

20 Q. Okay. Maybe let me ask you more directly.
21 Have you used a foundry to fabricate a chip in your
22 30 years of experience?

23 A. For my devices that my students test?

24 Q. Sure. Let's go with that.

25 MR. CHIU: Objection; outside the

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2 scope.

3 A. Well, we do collaboration with colleagues
4 in companies and startup, so a lot of times the
5 devices are not fabricated in our lab and is
6 fabricated in the companies. At least part of the
7 process. And sometimes the collaborator will give me
8 some chips that I might not even told where they're
9 from and just say that this is the device for certain
10 structure and that we collaborate to test it and try
11 to understand the characteristics and the underlying
12 physics behind it.

13 So there could be that some of the chips
14 that I use are fabricated in foundry, but not
15 directly. I don't think I actually outsource my own
16 chip to a foundry.

17 Q. (BY MR. MODI) Okay. Have you heard of
18 MOSIS?

19 A. Yes.

20 Q. What is MOSIS?

21 A. It's a company that also do fabrications.

22 Q. Have you worked with MOSIS?

23 A. I don't think so. I don't recall.

24 Q. When you fabricate a chip, do you
25 generally upload an electronic file to the foundry's

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2 website?

3 MR. CHIU: Objection; outside the
4 scope.

5 A. Like I said, I did not actually fabricate
6 my own chip in a foundry.

7 Q. (BY MR. MODI) Well, let me ask you this
8 way. When a chip is fabricated, is an electronic
9 file generally uploaded to the foundry's website?

10 MR. CHIU: Objection; lacks
11 foundation, outside the scope of the deposition.

12 A. Where is the chip fabricated?

13 Are you saying when the chip is
14 fabricated -- can you give me some parameters? What
15 chips are you talking about?

16 Q. (BY MR. MODI) The kind of chips we're
17 talking about in -- that are discussed in the '902
18 patent.

19 A. The '902 patent is not talking about a --
20 a chip. It's talking about a process --

21 Q. Okay.

22 A. -- of forming a contact holes. It's not
23 about fabricating a entire chip. It talk about
24 related to a microelectronic structure, such as
25 transistor, capacitor, diode, and so on and so forth.

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Q. I guess let me --

A. So I'm not sure what do you mean by --
what chip are you talking about?

Q. (BY MR. MODI) Okay. Let me maybe ask you
a question different -- this way, Dr. Lee.

A. Yes.

Q. It's very simple. When you go to a
foundry to get a chip fabricated, what do you give
them?

MR. CHIU: Objection; form, lacks
foundation.

A. I don't go to foundry. I never gone to
foundry, so --

Q. (BY MR. MODI) Let's say someone in your
field.

A. Who?

MR. CHIU: Same objection.

Q. (BY MR. MODI) Collaborators that you work
with.

MR. CHIU: Incomplete
hypothetical; outside the scope. Objection.

A. When someone go to a foundry -- let me
rephrase your question and see if I can understand.

When someone go to a foundry to get a chip

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2 fabricated, what do that person give them?

3 Q. (BY MR. MODI) Yes.

4 A. Money.

5 Q. Okay. Other than money?

6 A. Money. I mean, it costs money to
7 fabricate a chip. There's also a design rule -- now,
8 are you saying that someone -- are you saying that
9 that someone is a researcher or someone is a circuit
10 designer or someone that is a test structure
11 designer? Who is that someone? Can you give me more
12 parameters?

13 Q. Sure. So you mentioned design rules.
14 What is a design rule?

15 MR. CHIU: Objection; outside the
16 scope.

17 A. Design rule basically is related to a
18 process that tells how -- what are the rules and
19 guidelines related to each structure on each layer
20 and also related to different structure at different
21 layers. Dimensions, space separations, maximum
22 length, minimum length.

23 So basically you have all kinds of rules
24 related to a certain fabrication process. Even a
25 research lab have certain rules, including

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2 thicknesses, for example.

3 Q. (BY MR. MODI) Dr. Lee, I'm going to hand
4 you what's been marked as Samsung Exhibit 2003, and
5 it's in IPR 2015-1327.

6 (Exhibit 2003 was marked.)

7 Q. (BY MR. MODI) And it's entitled "MOSIS
8 Scalable CMOS Design Rules."

9 A. By the way, this copy that I have is all
10 marked up.

11 Q. Where is it marked? Well, go ahead and
12 identify it for the record.

13 A. Page 3, Page 2.

14 Q. Let me see.

15 A. One sec.

16 Q. I think we may have marked the wrong one.
17 Sorry about that.

18 MR. CHIU: This one has marks too.

19 MR. MODI: Let me see. I think
20 it's okay. I think the first page has a line on
21 it. It's the same. You have the same. It's
22 okay. Let's use this copy. You have the same.

23 A. No, this one has Page 1, Page 2, and Page
24 3 are marked up. Not just Page 2 and 3 now.

25 Q. (BY MR. MODI) I understand. Let's work

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2 with that copy, if that's okay.

3 Why don't you do this? Just so that the
4 record is clear, why don't you go ahead and identify
5 which pages have markings for us?

6 A. Well, I did.

7 Q. Okay. What is Exhibit 2003, Dr. Lee?

8 A. I have never seen this one before. I can
9 tell you what the title says.

10 Q. Okay. Go ahead.

11 A. "MOSIS Scalable CMOS Design Rules
12 (revision 7)."

13 Q. Why don't you take a few minutes to take a
14 look at it? Let me know when you're done.

15 A. (Reviewing document.)

16 You just handed me a document that I've
17 never seen before and asked me to take a few minutes
18 to read it and understand it. I feel very
19 uncomfortable to make any comment on this at all.

20 Q. Okay. Well, let's see if you can do your
21 best and see where we can get.

22 A. No, I feel very uncomfortable giving any
23 response to this.

24 Q. So you don't understand any of this
25 document, Dr. Lee?

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2 A. I'm saying -- that's not what I'm saying.
3 I don't feel comfortable making any comment on this
4 document. It will take me some time to understand
5 it. It will take me to understand what are the
6 previous revisions, what are the design technology,
7 what is the process that they use, what is the --
8 what is the Caltech Intermediate Form, CIF. CIF
9 Version 2.0. Where is Version 1? And a reference to
10 a couple -- a reference, 1 and 2, and 1, 2, and 3,
11 that it's not available.

12 Do you have those references for me? You
13 do?

14 Q. Are you done talking?

15 A. No. Do you -- no, I'm asking you, do you
16 have those references?

17 Q. Well, let me ask you my next question. If
18 you try the best -- let's see if you can answer it.

19 Can you look at Page 1 of Exhibit 2003 for
20 me and go ahead, read Section 1.1 and let me know
21 when you're done.

22 A. (Reviewing document.)

23 It will take me a few hours to read it and
24 understand it and search it, and to give you a
25 complete, honest answer.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 Q. So let me just understand. It is your
3 testimony under oath today that it will take you a
4 few hours to read --

5 A. No. I'm saying that it --

6 Q. -- four paragraphs on Page 1 of --

7 A. -- it will --

8 Q. Dr. Lee, let me finish my question, sir.

9 So is it your sworn testimony today that
10 it will take you a few hours to read four paragraphs
11 on Page 1 of Exhibit 2003?

12 MR. CHIU: Objection; misstates
13 the witness's testimony.

14 A. It will take me at least a few hours to
15 read, understand it, analyze it, and do research on
16 some of the references that they are referring to in
17 order to make any statement under oath because I
18 don't want to just read it as if, like, I'm reading a
19 novel and try to answer your question. Because there
20 is a lot of references that it refer to. A lot of
21 different version that it refer to.

22 Q. (BY MR. MODI) So can I ask you to look
23 at, again, Exhibit 2003, Page 1, and read into the
24 record for me what the first sentence says.

25 MR. CHIU: Objection. This is

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 outside the scope of the deposition, lacks
3 foundation.

4 Look, he's already said he hasn't
5 seen this document before. This is the same
6 issue that we talked about before. Do you want
7 to call the PTAB about this?

8 You're asking him questions about
9 a very technical document that he's never seen
10 before. He's already said it would take him
11 hours to analyze this.

12 Q. (BY MR. MODI) Dr. Lee, can you answer my
13 question, please? I asked you to read one sentence
14 from this document. Are you able to do that, sir?

15 MR. CHIU: Objection. Harassing
16 the witness.

17 A. I read it.

18 Q. (BY MR. MODI) Can you read it into the
19 record for me?

20 MR. CHIU: Look, this --

21 A. You didn't say that.

22 Q. (BY MR. MODI) Well, I'm asking you to do
23 it now.

24 MR. CHIU: I'm going to instruct
25 the witness not to answer your question. So you

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 want to take this up with the PTAB?

3 MR. MODI: Yeah, let's call the
4 PTAB.

5 THE WITNESS: Can we take a break?

6 MR. MODI: Yeah.

7 (Break.)

8 Q. (BY MR. MODI) So, Dr. Lee, we're going to
9 go back to before lunch. We were talking about the
10 reference in the prosecution history. Do you
11 remember that?

12 A. Which one?

13 Q. The Chen reference, we talked about that.
14 We talked about Michihiro. Do you remember?

15 A. Yes. Michihiro.

16 Q. And we were looking at the spaced apart
17 issue. We were talking about the spaced apart issue.
18 Do you remember that?

19 A. Yes.

20 Q. And I had asked you several questions
21 about spaced apart and -- when we were talking about
22 Michihiro. Do you recall that?

23 A. Recall the questions or recall that you
24 asked?

25 Q. Just our discussion. Our discussion.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. Yeah. Yes, we did talk about that.

3 Q. And you disagreed with the examiner's
4 statement -- one of the examiner's statements.
5 Right?

6 MR. CHIU: Objection;
7 mischaracterizes the witness's testimony.

8 Q. (BY MR. MODI) Let me take you there. So
9 I believe it was Page 101 in Exhibit 1102.

10 Are you there?

11 A. Is there a question?

12 Q. Yes. The question is, I had asked you
13 whether you agree with the examiner's statement that
14 "Michihiro discloses forming a first patterned layer
15 4a on the active region of the substrate spaced apart
16 from the field isolation region."

17 Do you remember that question?

18 A. Yes. Are you asking me again?

19 Q. I'm asking -- and I believe your answer
20 was -- well, let's see if I can do this. Your answer
21 was that you disagreed with that statement.

22 MR. CHIU: Objection;
23 mischaracterizes the witness's testimony.

24 A. (Reviewing document.)

25 I think you were referring to Figure 4(b)

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 and Figure 4(a). Right?

3 Q. (BY MR. MODI) (Nods.)

4 A. Yes. The evidence shown in this patent,
5 Michihiro patent, shows that the first patterned
6 layer 4a, 4b, and 4c on the active region of the
7 substrate are not spaced apart from the field
8 isolation region.

9 Q. And when you referred to the evidence,
10 what are you referring to?

11 MR. CHIU: Objection; form.

12 A. I was referring to Figure 4(a).

13 Q. (BY MR. MODI) Anything else?

14 A. Well, there's one of the evidence.
15 Anything else in the patent? I don't know. I have
16 to -- I have to look at it again. I have not read
17 this for quite some time. So I have to look at the
18 patent and see if there is anything else that --
19 indicating that it is not spaced apart. But
20 Figure 4(a) clearly shows that the first patterned
21 layer is not spaced apart from the field region.

22 Q. And if you recall, I asked you what if you
23 took away Figure 4(a), would your answer change?

24 MR. CHIU: Objection; lacks
25 foundation, incomplete hypothetical.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. Well, do you want me to answer your
3 previous question if anything else?

4 Q. (BY MR. MODI) No, that's okay.

5 A. Okay.

6 MR. CHIU: Objection; lacks
7 foundation, incomplete hypothetical, outside the
8 scope of this deposition.

9 A. What is your question now?

10 Q. (BY MR. MODI) The question is if
11 Figure 4(a) was not in Michihiro, would you still
12 disagree with the examiner's statement?

13 MR. CHIU: Objection; lacks
14 foundation, incomplete hypothetical, outside the
15 scope of this deposition.

16 A. Would I still disagree with examiner's
17 statement? Which statement? There is so many
18 statements.

19 Q. (BY MR. MODI) The one we were looking at.

20 A. Which is?

21 MR. CHIU: Same objections.

22 Q. (BY MR. MODI) "Forming your first pattern
23 layer 4a on the active agent of the substrate spaced
24 apart from the field isolation region."

25 MR. CHIU: Same objections.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. No. Now that I know what the patent is
3 about, just because you take away that figure doesn't
4 change the process of the patent and -- and the
5 layout of the design. So, no, I mean, now that it's
6 known that the first patterned layer touches and
7 crosses over the field region and it's not spaced
8 apart, you arbitrarily hypothetically take away that
9 figure, it doesn't change the fact.

10 Q. (BY MR. MODI) Is it your opinion that
11 Gate 4B is not spaced apart from field region 2
12 because it crosses over to field region 2?

13 MR. CHIU: Objection; form, lacks
14 foundation, incomplete hypothetical, outside the
15 scope of this deposition.

16 A. If you go back to one of my answer before,
17 you would -- you will see that I already answered
18 that question.

19 Q. (BY MR. MODI) Would you please answer it
20 again for me?

21 MR. CHIU: Same objections, asked
22 and answered.

23 A. Let me tell you where it is. The evidence
24 shows in this patent, Michihiro patent, shows that
25 the first patterned layer 4a, 4b, 4c on the active

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 region of the substrate are not spaced apart from the
3 field isolation region.

4 Q. (BY MR. MODI) Dr. Lee, my question was a
5 little different. Would you like me to reread it to
6 you?

7 A. And followed by the answer, if you look at
8 my answer, previous answer, that those gates 4A, 4B,
9 4C touches and crosses over the field region, the
10 field isolation region.

11 Q. So the answer is yes to my question?

12 MR. CHIU: Objection; form,
13 mischaracterizes the witness's testimony.

14 A. Gate 4B is not spaced apart from the field
15 region 2 because it touches and crosses over the
16 field region 2.

17 Q. (BY MR. MODI) Is gate 2 a gate electrode
18 of a MOSFET?

19 MR. CHIU: Objection; form.

20 A. I think you're confused. Gate 2? Where
21 is gate 2?

22 Q. (BY MR. MODI) Sorry. Is gate 4B?

23 A. What about it?

24 Q. Is gate 4B a gate electrode of a MOSFET?

25 MR. CHIU: Objection; lacks

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 foundation, outside the scope of this deposition.

3 A. (Reviewing document.)

4 Well, this is a multiple gate electrode
5 MOSFET. Gates -- or gate electrodes 4A, 4B, 4C are
6 the gate electrodes.

7 Q. (BY MR. MODI) Can I ask you to look at
8 Figure 4(a) for me and tell me what 10 represents in
9 Figure 4(a)?

10 MR. CHIU: Objection; outside the
11 scope of this deposition.

12 A. (Reviewing document.)

13 Well, if you look at Column 1 of 210, it
14 shows that the reference numeral 10 is a contact hole
15 for electrical contact to the gate electrode 4, but
16 that is referring to Figure 1(a).

17 And Figure 4 -- well, so parts in
18 Figure 4(a) and (b) are identical, and corresponding
19 to parts in Figure 1(a) and (b) are given the same
20 reference numeral, and the detailed description
21 thereof is omitted.

22 So I assume that they are saying
23 that the same numerals are given for Figure 4(a)
24 and (b) as in Figure 1(a) and (b). So with that
25 in mind, the reference numeral 10 is a contact

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 hole for electrical connection with the gate
3 electrodes 4a, B, and C.

4 Q. (BY MR. MODI) For a MOSFET, can you make
5 a contact hole with the gate electrode on the active
6 region?

7 MR. CHIU: Objection; form, lacks
8 foundation, outside the scope.

9 A. Can you clarify your question? Because it
10 seems like you're saying that -- make a contact hole
11 with the gate electrode and the contact hole on the
12 active region. Are you saying making a contact hole
13 on the active regions or making a contact hole with
14 the gate inside the active regions?

15 Q. In the latter.

16 MR. CHIU: Same objections.

17 A. So what -- what gate electrode are you
18 talking about? What material it is?

19 Q. (BY MR. MODI) The ones that we're talking
20 about in the -- in the patent. Polysilicon.

21 MR. CHIU: Same objections.

22 A. It's polysilicon.

23 Q. (BY MR. MODI) Uh-huh.

24 A. Is it built with boron or arsenic? What
25 is it built with?

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 Q. I'd say boron.

3 A. And what kind of metal are you talking
4 about to make contact with the gate electrode? Are
5 you talking about tungsten? Are you talking about
6 polysilicon itself or tungsten silicide, copper?
7 What -- can you give me some parameters in this
8 hypothetical -- hypothetical question scenario like
9 that?

10 Q. Let's say tungsten.

11 A. Okay.

12 MR. CHIU: Same objections.

13 A. What dimension -- what technology node are
14 you referring to? 20-nanometer, 10-nanometer, or
15 65-nanometer?

16 Q. (BY MR. MODI) Let's go with 28.

17 A. 28-nanometer. What is the contact hole
18 size are you referring to? And what is the gate
19 electrode pattern? Is it a rectangle, rectangular
20 shape, or is it a ring shape, or is it a circular
21 ring? What does it look like?

22 Q. Are you done with your --

23 A. Yeah. I'm asking your parameters. Define
24 your question so that I can answer you thoroughly
25 and, you know, make sure that there is no

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 misunderstanding what -- what problems are you
3 referring to. Because if I give a question like this
4 to my undergraduate class, they will say, "Sir, what
5 kind of parameters are you referring to? Given
6 what?"

7 Q. Okay. Assume we're talking about the
8 reference that's in front of you.

9 A. Which is? There's quite a few references.
10 Michihiro?

11 Q. Yes.

12 A. Okay.

13 Q. Can you answer my question?

14 MR. CHIU: Same objections and
15 incomplete hypothetical.

16 A. You know, I have not read this for quite
17 some time, and I need to read it more carefully and
18 see what the process is, the technology node, and how
19 that relate to your hypothetical question.

20 (Reviewing document.)

21 So it looks like Figure 4(a) and (b) are
22 referring to a MOSFET. Okay. And the gate is -- is
23 the same as Figure 2, is polysilicon film.

24 (Reviewing document.)

25 Let me understand your question. Are you

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 talking about in general, whether you can make
3 contact with a gate electrode within the active
4 region?

5 Q. Let's start with that.

6 A. Sure. Sure you can.

7 Q. And you can do that for a MOSFET?

8 A. We do that all the time at UT. Sure.

9 Q. Okay.

10 A. Why not? I don't see why not. I mean --
11 I mean, annular transistor, we fabricate those.
12 Yeah, sure. We make contact to the -- to the gate
13 electrode within the active region.

14 Q. And what fabrication process are you
15 using?

16 A. Well, various. Are you saying back in
17 1988 when I first started or 2016 when I -- at this
18 point?

19 Q. Well, let's start with 2016.

20 A. 2016 we -- we fabricate the device and --
21 you know, depends on the students, what -- whether
22 they use e-beam lithography or contact printing or
23 projection printing, the dimension could be as small
24 as 50 nanometer and as much as 2 or 3 micron.

25 Q. How about in 1996?

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. 1996 we -- 1996, do we have an e-beam
3 lithography already? I think we already have because
4 we move into the new clean room already. The
5 capability at that time is -- still can be quite
6 good, you know, .8 microns with contact printing, and
7 e-beam lithography can be as small as -- e-beam
8 lithography is -- as you know, is very good
9 resolution.

10 Q. So what is the -- was that available in
11 1996?

12 MR. CHIU: Objection; form.

13 (Brief interruption.)

14 (Break.)

15 Q. Let's -- just so the record is clear, in
16 1996, what fabrication process could be used?

17 MR. CHIU: Objection to form,
18 lacks foundation, outside the scope of this
19 deposition.

20 A. What fabrication process could be used.
21 Well, back in 1996 we have -- you mean in our lab?

22 Q. (BY MR. MODI) No. So remember my
23 question was -- we were talking about for a MOSFET,
24 right? Can you take a contact hole, or can you make
25 a contact hole with the gate electrode on the active

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 region. Right? That's what we were referring to?

3 A. Yeah. You could do that even back in
4 1996.

5 Q. I just want to focus back in 1996.

6 A. Yes, you can do that.

7 Q. Can you tell me what fabrication processes
8 were used back then --

9 MR. CHIU: Objection --

10 Q. (BY MR. MODI) -- to make that happen?

11 MR. CHIU: Objection to form,
12 lacks foundation, and outside the scope of this
13 deposition.

14 A. What fabrication were used back then?
15 Well, in those days, 1996, dual polysilicon gate is
16 still used -- was still used, and metal contact, I
17 believe, is either aluminum or titanium, barium and
18 aluminum fill. Yeah, I mean, that can be done.
19 Yeah. Sure. Why not?

20 Q. (BY MR. MODI) But, Dr. Lee, I'm asking
21 about the process.

22 A. Are you talking about CMOS process?

23 Q. No. I asked you what process could be
24 used for a MOSFET to make a contact hole with the
25 gate electrode on the active region.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. The same process --

3 MR. CHIU: Objection; form, lacks
4 foundation, outside the scope of this deposition.

5 A. Same process that you use to make contact
6 to the gate electrode in the field. There's -- I
7 mean, we do that all the time --

8 Q. (BY MR. MODI) I'm talking about in 1996.

9 A. Yeah. We did that all the time back in
10 1996.

11 Q. Okay. Give me the name of a process that
12 you used.

13 A. CMOS process.

14 (Discussion off the record.)

15 A. The CMOS process.

16 Q. Okay. Can you give me more details about
17 the CMOS process in 1996?

18 A. In what sense? The minimum dimension,
19 minimum feature size?

20 Q. Sure. Let's go with feature size.

21 A. Okay.

22 MR. CHIU: Objection; outside the
23 scope.

24 A. Well --

25 MR. CHIU: Counsel, what's the

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 relevance of any of this line of questioning? I
3 mean, none of this is in his declaration.

4 MR. MODI: It relates to the
5 issues we've been talking about.

6 MR. CHIU: And what issues are
7 those?

8 MR. MODI: I'm not going to tell
9 you in the presence of the witness, so we can go
10 off line and we can have a discussion. But a
11 question is pending, so let him answer.

12 A. In our lab we use -- the dimension could
13 be -- could vary quite a bit. It depends on what
14 technology node we use. I mean, it depends on what
15 equipment we use for defining the geometry.

16 Q. (BY MR. MODI) So sitting here today, can
17 you give me the name of a process you used in 1996?

18 A. That we -- that I used?

19 Q. Yes, Dr. Lee.

20 MR. CHIU: Objection; relevance,
21 form, outside the scope of this deposition.

22 A. The process that we use in 1996 in the
23 lab, microelectronic research lab in UT Austin, could
24 range from CMOS process to NMOS process to PMOS
25 process to MMOS capacitor, PMOS capacitor, diodes.

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2 Remember, we're a research lab. We don't
3 have a baseline CMOS process, so we can fabricate all
4 kinds of devices. So the range of processes that we
5 use in our lab is tremendous.

6 Q. (BY MR. MODI) But sitting here today, you
7 don't -- you can't tell me any specific process other
8 than generality?

9 A. Okay. Which process are you referring to?

10 Q. CMOS.

11 A. That I used at that time?

12 Q. Let's go with that.

13 A. It's dual poly gate process.

14 Q. And what feature size?

15 MR. CHIU: Objection; relevance,
16 outside the scope of this deposition.

17 A. What equipment are you referring to when
18 you ask what feature size?

19 Q. (BY MR. MODI) Well, I'm asking you what
20 you used.

21 A. I could go down to 50 nanometer in those
22 days, up to 20 micron. It depends on what equipment
23 you use, what the process photoresist you use,
24 what -- whether it's projection printing, whether you
25 use ashing or not, whether you use oxygen and plasma

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2 for reducing the dimensions of the photoresist.
3 There's all kinds of process one can use to define
4 the dimension on the chip.

5 So, again, this is a research lab. We
6 don't have a set baseline process. So I'm not sure,
7 when you say what process do I use, which student are
8 you referring to? What Ph.D. project are you
9 referring to?

10 Q. So let me make sure I understand your
11 testimony. So are you saying that, in 1996 in the
12 20-nanometer CMOS process, the gate contact could be
13 made over the active region?

14 MR. CHIU: Objection;
15 mischaracterizes the witness's testimony, outside
16 the scope of the deposition, relevance.

17 A. I didn't say 20-nanometer. Did I say
18 20-nanometer?

19 Q. (BY MR. MODI) Let's take 20 out.

20 A. What do you want to put in?

21 MR. CHIU: Same objections.

22 Q. (BY MR. MODI) Are you saying that in a --
23 in -- how about 20-micrometer?

24 MR. CHIU: Same objections;
25 mischaracterizes the witness's testimony, outside

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 the scope of the deposition, and relevance.

3 A. Your question is whether that can be done.

4 Q. (BY MR. MODI) Whether you did it in 1996.

5 MR. CHIU: Same objections.

6 A. Whether I did it or one of my students in
7 my group did it or a student in the microelectronics
8 lab did it? What are you referring that I -- what do
9 you mean, I? I personally go into the lab to do it?

10 Q. (BY MR. MODI) Let me try to make it
11 easier for you.

12 Can you name one commercially available
13 fabrication process in 1996 in which the gate contact
14 could be made over the active region?

15 MR. CHIU: Objection; lacks
16 foundation, outside the scope of this deposition.

17 A. Well, I can tell you that commercially
18 available chips and fabrication process in 1996, or
19 even now, are highly confidential and is not easily
20 accessible to general public. So I wouldn't be able
21 to tell you whether a commercially available
22 fabrication process in 1996, whether the contact can
23 be made over the active region.

24 However, I can tell you that there are
25 publications and prior art that shows the transistor,

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2 such as annular transistor, where the gate are
3 entirely on the active region, and such contacts are
4 made into the gate electrode within the active
5 region.

6 Q. (BY MR. MODI) This publication that
7 you're thinking of, does it relate to MOSFETs?

8 A. There are a number of publications, and
9 some are related to MOSFET, some are related to other
10 devices. Sure.

11 Q. Any particular one come to mind?

12 A. A particular publications that describe
13 that -- is that what you're asking? -- in 1996?

14 Q. (Nods.)

15 A. I cannot think -- I cannot tell you off
16 the top of my head what publication, but I know for
17 sure there are some.

18 Q. But sitting here today, you can't tell me
19 the name of a commercial process or the name of a
20 publication. Is that fair?

21 A. Again, the public -- the commercial
22 fabrication process are highly confidential. No one
23 outside of the company would have access to those
24 commercial fabrication process, and -- and I'm
25 telling you that there are publications and patents

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2 about those devices.

3 Now, if you ask me to tell you exactly
4 what's a patent number, I cannot.

5 Q. Or the author names?

6 MR. CHIU: Objection to form.

7 A. I recall one of them is even -- I believe
8 is a patent filed by Samsung.

9 Q. (BY MR. MODI) And who is it?

10 A. Who?

11 Q. What's the name?

12 A. Samsung.

13 Q. So you just said you don't know the --
14 other than company name, you don't know anyone else?

15 A. Anyone else?

16 Q. You don't recall the author's name. You
17 just recall the company's name?

18 A. No, I don't recall the author's name.

19 MR. MODI: Why don't we take a
20 couple-minute break.

21 (Break.)

22 Q. (BY MR. MODI) Dr. Lee, you ready?

23 A. Yes.

24 Q. Okay. Can we go to the Lee reference,
25 please?

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2 A. Okay.

3 Q. So we talked about Figure 1 earlier, and I
4 believe we may have touched on Figure 2. But
5 Figure 2 is prior art. Right?

6 A. Figure 1 and 2 are prior art.

7 Q. Is that right?

8 A. Yes. Figure 1 and 2 are prior art.

9 Q. And would you agree that to remedy the
10 problems associated with the prior art, the Lee
11 reference proposes several embodiments in Figures 3,
12 4, 5, and 6?

13 MR. CHIU: Objection to form.

14 A. Yes. Figure 3, 4, 5 and 6 are
15 illustrations of the Lee invention.

16 Q. (BY MR. MODI) Can you please turn to
17 Figure 3(a). Let me know when you're there.

18 A. Yes.

19 Q. Do you see a gate sidewall 34-1?

20 A. Yes. It says sidewall spacers.

21 Q. And in Figure 3(b) next to gate sidewall
22 34-1, do you see an etch stop layer 34-2?

23 A. Yes. 34-2 is an etch stop layer.

24 Q. The etch stop layer 34-2 is also formed on
25 the field oxide layer 32. Right?

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2 A. That's right.

3 Q. The etch stop layer 34-2 on the field
4 oxide layer is formed on a step area of the field
5 oxide layer 32. Correct?

6 A. Yes. The etch stop process -- the etch
7 stop layer is formed on the field isolation region
8 using the step area of the field isolation layer.

9 Q. So can you go to Page 17-6 for me --

10 A. Okay.

11 Q. -- of the reference --

12 A. Sure.

13 Q. -- first paragraph. Are you there?

14 A. Yes.

15 Q. Do you see where it says, "At this time
16 the etch stop layer is formed..."? Do you see that?

17 A. Yes.

18 Q. And it goes on and says, "...using the
19 step area formed on the lower layer..." Do you see
20 that?

21 A. Yes.

22 Q. Do you agree that the lower layer that's
23 referred to there is the first of the field oxide
24 layer 32?

25 MR. CHIU: Objection to form.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 A. Yes. The lower layer is referred to the
3 oxide isolation layer.

4 Q. (BY MR. MODI) 32. Right?

5 A. Yeah. Oxide -- field oxide layer 32.

6 Q. Now, can I ask you to look at Figure 4.

7 A. Okay.

8 Q. Would you agree Figure 4 is an alternative
9 embodiment to Figure 3?

10 A. Yes. It's the second --

11 MR. CHIU: Objection to form.

12 A. Figure 4 illustrate the second embodiment
13 of the present invention.

14 Q. (BY MR. MODI) It's a different embodiment
15 than what's in Figure 3. Right?

16 A. That's right. And Figure 3 is the first
17 embodiment, and Figure 4 is the second embodiment.

18 Q. Okay. So if you go to the embodiment of
19 Figure C -- of Figure 4, do you see a gate structure
20 in between the two field oxide layers?

21 MR. CHIU: Objection to form.

22 A. Are you saying the gate structure on the
23 active region?

24 Q. (BY MR. MODI) Yes.

25 A. Yeah, there is a gate structure on the

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2 active region.

3 Q. Between the two field oxide layers?

4 MR. CHIU: Objection to form.

5 A. Yeah, it's between -- and spaced apart
6 from the field region.

7 Q. (BY MR. MODI) How do you know it's spaced
8 apart?

9 A. Well, the cross-section here shows that
10 the first patterned layer, which it's a gate on the
11 active region, is spaced apart from the field region.
12 So this evidence right here illustrates that the gate
13 on the active region is spaced apart from the field
14 region.

15 Q. When you said "the cross-section here,"
16 what are you referring to?

17 A. Figure 4.

18 Q. You were able to tell us that it's spaced
19 apart just based on the cross-section?

20 MR. CHIU: Objection to form.

21 A. Well, the evidence as shown in the Lee
22 reference all show that the first patterned
23 conductive layer on the active region of the
24 substrate is spaced apart from the field region. And
25 no evidence contrary to that is shown or disclosed in

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2 the Lee reference.

3 Q. (BY MR. MODI) Dr. Lee, that's what I'm
4 asking you. Can you identify the evidence? What
5 evidence are you referring to?

6 A. Well...

7 (Reviewing document.)

8 If you look at Page 17-4.

9 Q. Okay. I'm there.

10 A. The third paragraph.

11 Q. Okay.

12 A. If you read it. Let me know when you're
13 done.

14 Q. Well, why don't you just point to me what
15 you believe in that paragraph leads you to your
16 conclusion?

17 A. Well, the method of the present invention
18 comprises of the step of fabricating a transistor by
19 making a source and drain region which is formed by
20 doping impurities on the gate in the active region on
21 a semiconductor substrate and the substrate around
22 the gate.

23 And it further describe the subsequent
24 process. But the important thing is that it
25 illustrate that the gate is spaced apart from the

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2 field region.

3 Q. And why did this sentence lead you to
4 believe that?

5 A. Well, if you read the sentence carefully,
6 you'll see that it's doping impurity -- introducing
7 doping impurity on the substrate around the gate.
8 Okay? Not on two side of the gate, but around the
9 gate, meaning that it's surrounding the gate.

10 So if the gate -- what they're saying is
11 that the gate is not touching the field region.
12 Otherwise one would not be able to dope the substrate
13 around the gate.

14 Q. So that -- that's your understanding of
15 what this sentence says?

16 A. I think that would be an understanding of
17 a person of ordinary skill in the art in 1997 --
18 1996, and it's also my understanding, and it's
19 clearly disclosed that the first patterned conductive
20 layer on the active region of the substrate is spaced
21 apart from the field region, not only by the figures,
22 but also by the specifications.

23 Q. So what in the figures shows this,
24 Dr. Lee?

25 A. Well, do you see the gate touching the

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2 field?

3 Q. Well, I didn't see it touching the field
4 in Michihiro.

5 A. Michihiro shows additional evidence that
6 the -- which is contrary to spaced apart. It shows
7 the top plan view that the gate touches and crosses
8 over the field region and --

9 Q. So let me ask you this. If you --

10 A. May I finish?

11 Q. Sorry. Go ahead.

12 A. And in Lee, all the evidence pointed to
13 the fact that the first patterned conductive layer is
14 spaced apart from the field region, including the
15 figures and the specifications.

16 Q. Does Lee show a plan view to confirm your
17 understanding?

18 A. You don't need to. It's clear.

19 Q. Okay. Let's -- assuming if the board
20 disagrees with you with respect to your reading of
21 17-4, okay, that sentence, what else in Lee do you
22 have that supports your conclusion?

23 A. Well, the specification is clearly
24 indicating that the doping impurity is done on the
25 substrate around the gate. So I believe that the

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2 board will agree with me with respect to my reading
3 of 17.4. And if -- if the board -- if that -- that
4 is not clear, that all the figures that's shown, and
5 all the evidence that's disclosed in Lee references
6 show that the first patterned conductive layer is
7 spaced apart from the field region.

8 Furthermore, it is also obvious, as I
9 stated in my declaration, that, "It would have been
10 the natural design choice for a MOS gate to be formed
11 entirely on the active region, and spaced apart from
12 the field region."

13 Q. Where are you reading from, Dr. Lee?

14 A. In my declaration.

15 Q. What paragraph?

16 A. Paragraph 90. You can take a look at
17 that.

18 Q. Okay. So let's break this down. The
19 evidence that you're pointing to is this sentence on
20 17-4. Right?

21 A. The evidence that I pointed to is all the
22 evidence that's disclosed in all the figures in the
23 Lee reference, plus the specifications, particularly
24 the 17.4, and also that there are no evidence that's
25 shown in Lee that disclosed the contrary to spaced

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2 apart.

3 Q. Okay. So --

4 A. Furthermore, to the extent that this
5 limitation is not explicitly disclosed, it would have
6 been a natural design choice for a MOS gate to be
7 formed entirely on the active region and spaced apart
8 from the field region.

9 Q. Okay. I want you to just focus on Lee.
10 Remember we talked about the explicit --

11 A. This is Lee.

12 Q. I understand. Let me finish my question.
13 Can I finish?

14 A. Yes.

15 Q. We talked about explicit disclosure
16 before. Right?

17 A. Yes.

18 Q. This morning?

19 A. Yes.

20 Q. Okay. I want to just focus on that.

21 A. Okay.

22 Q. I want you to tell me what explicit
23 disclosure is there in Lee that supports your
24 conclusion? I don't want obviousness. I want you to
25 tell me what explicit disclosure in Lee supports --

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2 A. I answered you the question already, all
3 the evidence.

4 Q. Okay. I want you to itemize it for me.

5 A. Okay. For example, in Figure 3, that's
6 what I describe and use in Paragraph 89 on my
7 declaration, that "discloses 'an active region is
8 isolated electrically from the surrounding active
9 regions by forming a field oxide layer (32) on a
10 semiconductor substrate (31), and a MOS gate (34) is
11 formed by depositing and etching of gate oxide layer,
12 poly and gate cap in order'" to show in this Figure
13 3(a).

14 And that it discloses that the MOS gate is
15 formed separate from the field oxide region, and that
16 it is gate showing spaced apart from the field
17 region. So Figure 3(a), Figure 4(a) -- I'm sorry --
18 Figure 4, Figure 5, Figure 3(b), Figure 3(c),
19 Figure 3(d), Figure 6 all shows the first patterned
20 conductive layer on said active region of the
21 substrate spaced apart from the field region.

22 Q. Dr. Lee, did you not find it important to
23 list all of those figures in your declaration?

24 A. Say it again.

25 Q. Did you not find it important to list

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2 those figures in your declaration?

3 A. I'm telling you now.

4 Q. So you're changing your testimony?

5 A. I'm not changing my testimony. I am
6 telling you that in addition to Figure 3(a) that I've
7 shown in the declaration, Paragraph 89, all the other
8 figures in Figure 3(b), Figure 3(c), Figure 3(d),
9 Figure 4, Figure 5, Figure 6, are all showing that
10 the first patterned conductive layer on the active
11 region of the substrate spaced apart from the field
12 region.

13 Q. And if you just had those figures, and
14 there was no disclosure, would your testimony be the
15 same, sir?

16 MR. CHIU: Objection; form.

17 A. Well, the disclosure is there. Okay?

18 Q. (BY MR. MODI) And --

19 A. Listen. The specification clearly
20 disclosed that the gate is spaced apart from the
21 field region.

22 Q. Okay.

23 A. You cannot take that away.

24 Q. Fine. Let me -- I'm sorry. I'm going to
25 interrupt you because I want to try to speed this up.

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2 Okay?

3 I want you to focus on the specification.
4 Okay? Only on the specification of Lee. I want you
5 to tell me what passages in the specification are you
6 relying on to support your opinion.

7 MR. CHIU: Asked and answered.
8 Objection.

9 A. I think I read that a few minutes ago.

10 Q. (BY MR. MODI) Like I said, sir, I want to
11 make sure I understand your opinion because some of
12 this is not in your declaration.

13 A. It doesn't --

14 Q. Okay?

15 A. I'm telling you now.

16 Q. Exactly. So I want to make sure I get
17 every single support that you're relying upon in your
18 declaration. Okay? In the specification.

19 A. Can you look back? I read it.

20 Q. Hold on, Dr. Lee.

21 A. Let me read that to you. Do you want me
22 to read that to you? You asked me to read that to
23 you.

24 Q. I just want you to point it to me. I
25 don't want you to read it to me.

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2 MR. CHIU: Objection; form, asked
3 and answered.

4 A. It's in -- on Page 17-4 --

5 Q. (BY MR. MODI) Okay. So let me make
6 sure --

7 A. -- third paragraph --

8 Q. Hold on one second. Let me make sure.
9 Again, I'm trying to speed this up because your
10 counsel wants us to speed this up.

11 17-4, the only sentence on -- on Page 17-4
12 that you're relying upon is the one that's on the
13 third paragraph that says "a step of fabricating a
14 transistor." Right? That's the sentence you're
15 referring to?

16 A. The sentence is the entire paragraph. The
17 periods come at the end of the paragraph.

18 Q. But you're relying upon the Subpart a. Is
19 that fair?

20 A. Yes. Subpart a clearly shows that the
21 first patterned conductive layer is spaced apart from
22 the field region.

23 Q. Okay. Besides that sentence -- and I only
24 want you to focus on the specification -- what else
25 supports your opinion?

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2 A. (Reviewing document.)

3 Only talking about specification?

4 Q. That's right.

5 A. Yeah. That's the key sentence or part of
6 the sentence that support my argument, and that
7 clearly shows that the first patterned conductive
8 layer is spaced apart from the field region and that
9 there's no other sentences that I -- in the
10 specification that I rely on.

11 Q. So this key sentence that you just
12 mentioned, is there a reason why it doesn't appear in
13 Paragraph 89 of your declaration, sir?

14 MR. CHIU: Objection to form,
15 argumentative.

16 A. No. I -- I said that Figure 3(a) is
17 disclosing that, and this describe all the figures,
18 including Figure 3(a).

19 Q. (BY MR. MODI) Sir, where is this sentence
20 on Paragraph 89 or 90 of your declaration?

21 MR. CHIU: Objection to form.

22 A. It's not -- it's not there, but the reason
23 is that the evidence of all the figures support and
24 illustrate that and clearly shows that the first
25 patterned conductive layer is spaced apart from the

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2 field region.

3 And I'm -- I'm here clarifying 89 and 90,
4 Paragraph 89 and 90, and tell you that the
5 specification further confirm that what's shown in
6 the figures, that the active region -- that the first
7 patterned conductive layer on the active region is
8 spaced apart from the field region.

9 Q. (BY MR. MODI) When did you realize this
10 sentence was the key sentence, Dr. Lee?

11 MR. CHIU: Objection to form,
12 argumentative.

13 A. I don't recall, but it is definitely there
14 and that we -- that I know that that support the
15 further -- and other evidence supporting the figures
16 in that the first patterned conductive layer on the
17 active region is spaced apart from the field region.

18 Q. (BY MR. MODI) Can I have you go back to
19 Lee, Dr. Lee?

20 A. Yes.

21 Q. Lee reference. Let's go back to Figure 4.

22 A. Okay.

23 Q. Figure 4 shows a structure on the right
24 side on the top of the field oxide layer 32. Right?

25 A. Shows a structure on the right side. What

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2 are you talking about?

3 Q. What do you see on the right side of
4 Figure 4, Dr. Lee?

5 A. Right side of what?

6 MR. CHIU: Objection; form.

7 Q. (BY MR. MODI) The right side of the --
8 the gate 34.

9 MR. CHIU: Objection to form.

10 A. There is no gate 34. What are you talking
11 about?

12 Q. (BY MR. MODI) Okay. So let's look at
13 Figure -- you have Figure 4. Right?

14 A. I do.

15 Q. Okay. And Figure 4 -- does Figure 4
16 disclose a field oxide layer?

17 A. Yes.

18 Q. Okay. And do you see that the Figure 4
19 has a reference number 44-3? Do you see that?

20 A. Yes.

21 Q. So if you look at 44-3 --

22 A. Yes.

23 Q. -- there is a first insulating spacer
24 along the sidewall of 44-3. Correct?

25 MR. CHIU: Objection to form.

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2 A. Are you referring to the region between
3 44-3 and 44-2?

4 Q. (BY MR. MODI) Yes, sir.

5 A. Yes, there is a region of a sidewall
6 layer.

7 Q. So you would agree that next to area 44-3
8 there is a region along the sidewall of 44-3.
9 Correct?

10 A. Well, there are more than just one region
11 along the sidewall of 44-3. There are -- there are
12 that white region that we're talking about and also
13 44-2. The dummy -- the etch stop layer is also along
14 the sidewall of 44-3.

15 Q. But you would agree 44-2 does not touch
16 the sidewall of 44-3. Right?

17 MR. CHIU: Objection; form.

18 A. Sure it does.

19 Q. (BY MR. MODI) Where?

20 A. It does touch the second patterned
21 conductive layer as I describe in Paragraph 95 in my
22 declaration.

23 Q. So 44-3 -- actually, can you explain to me
24 how it touches it?

25 A. Well, you see that -- at the top of 44-3,

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2 touches the 44-2 and is still along the sidewall of
3 the second patterned conductive layer.

4 Q. So it's your testimony that because it
5 touches the top, it is along a sidewall of the second
6 patterned conductive layer?

7 A. Yes. 44-2 touches 44-3, and therefore it
8 is along the sidewall of the second patterned
9 conductive layer.

10 Q. And it touches -- and it's your opinion
11 that 44-2 touches 44-3 at the top. Is that right?

12 A. Yes. At the top, it's probably -- in
13 reality, not just at one point but a region up in the
14 top.

15 Q. Do you have any support in the spec for
16 that statement?

17 A. The spec in what? '902 or '675?

18 Q. In Lee. In Lee. Does the specification
19 support your opinion that you just gave me?

20 A. My opinion that it touches?

21 Q. Yes.

22 A. Well, the figure clearly shows that it
23 touches.

24 Q. Okay. Besides the figure, does anything
25 else support your opinion?

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2 A. (Reviewing document.)

3 Well, a person of ordinary skill in the
4 art would understand that the way you form these
5 layers, right, particularly in this Lee reference, it
6 says that -- the white part is what they refer to as
7 34-1. Okay? And that -- which is formed by
8 depositing an etch-back process to form the -- the
9 first spacer.

10 And, subsequently, the etch stop layer is
11 formed by the same process, is a conformal deposition
12 photo by etch-back. And based on these processes,
13 one can -- a person of ordinary skill in the art
14 would know that in -- especially that deposits
15 describe and with the support of the figure, that the
16 44-2 does touch the second patterned conductive
17 layer, and, therefore, the insulating spacer is along
18 the sidewall of the second patterned conductive
19 layer.

20 Q. So -- but in the Lee reference, I asked
21 you where in the specification it gives you support.
22 Can you -- what sentence were you referring to?

23 A. Well, if you look at 17.6, it says, "The
24 etch stop layer is formed with conductive or
25 non-conductive material. It is formed in the form of

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2 sidewall" -- you see it's along the sidewall --
3 "through a deposition and etch-back process using a
4 step," and that -- so this describe how the etch stop
5 process -- etch stop layer is formed. And Figure 4
6 basically talk about the etch stop layer.

7 Q. So just so that I am clear, Dr. Lee, so
8 you're referring to 17-6. Right?

9 A. Yes.

10 Q. And which sentence on 17-6?

11 A. The first paragraph.

12 Q. The one that starts with "At this time"?

13 A. "At this time, the etch stop layer" -- it
14 describe how the etch stop layer is formed in the --
15 in the Lee reference.

16 You know how the spacers are formed,
17 right? It's a conformal deposition of either
18 conductive material or nonconductive material and
19 followed by etch-back process.

20 Q. So the paragraph you're referring to on
21 17-6, right, the one that says "At this time" --

22 A. Yes.

23 Q. -- that refers to Figure 3. Right?

24 A. Yes.

25 Q. When you refer to 44-3 --

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2 A. Yes.

3 Q. -- and you are calling it -- you're saying
4 that's the second patterned conductive layer. Right?

5 A. That's right. Yeah, that's the second
6 patterned conductive layer.

7 Q. And what are you including in that 44-3?

8 A. Well, if you look at Paragraph 95, I show
9 a picture where you have the blue region. It's the
10 second patterned conductive layer, which is a dummy
11 pattern.

12 Q. So 44-3, you're saying the entirety of the
13 44-3 that's colored in blue is the second patterned
14 conductive layer?

15 A. That is correct, that the region colored
16 in blue is the second patterned conductive layer.

17 Q. What does that second patterned conductive
18 layer have?

19 A. It has the poly and a silicide kind --
20 it's a metal silicide contact gate cap.

21 Q. Where is that? Where are you getting that
22 from?

23 A. Well, if you look at paragraph on
24 Page 17-5, it show you what the gate look like.

25 Q. But that's talking about Figure 3.

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2 A. And Figure 4 use the same process.

3 Q. And where are you getting that from, sir?

4 A. It's described that it's forming the etch
5 stop layer, and it's also for -- the etch stop layer
6 is -- I mean the dummy pattern is formed at the same
7 time as the active gate -- than the first patterned
8 conductive layer, and so that the first patterned
9 conductive layer shown in Figure 3 comprised of the
10 gate cap and the poly.

11 Q. Is gate cap conducted?

12 A. In general, poly -- the gate --
13 polysilicon gate is pretty high resistive. So you do
14 add a layer of silicide, and that's in general called
15 a gate cap.

16 Q. So I want to go back and understand the
17 answer you gave me previously, the one before this.
18 You were saying the sentence from Figure -- that
19 talks about Figure 3 applies to Figure 4. Can you
20 tell me again how it applies to Figure 4?

21 A. Well, first of all -- you mean the
22 sentence apply to the formation of the gate or the
23 formulation of the second patterned conductive layer?
24 What are you referring to?

25 Q. We'll start with the -- I'm talking about

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2 formation of 44-3.

3 A. You mean the dummy pattern. Right?

4 Q. 44-3.

5 A. Yeah, that's the dummy pattern.

6 Well, the dummy pattern is identical to
7 the first patterned conductive layer.

8 Q. Lee does not call it a dummy pattern.
9 Does it?

10 A. Sure it does.

11 Q. It calls it an internal connection line.

12 A. No. It's a dummy pattern if you read
13 carefully.

14 Q. Go ahead and enlighten me.

15 A. Look at 17.6.

16 Q. Okay.

17 A. "Using internal connection lines...or the
18 step of dummy pattern."

19 Q. And when it talks about connection line,
20 it says 44-3, and when it talks about dummy pattern,
21 it doesn't have the reference numeral next to it.
22 Right?

23 MR. CHIU: Objection;
24 argumentative, form.

25 A. Well, a person of ordinary skill in the

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2 art would understand what this sentence is saying is
3 that the etch stop layer is formed using either
4 internal connection line or a step of dummy pattern
5 and that the dummy pattern is referred to at 44-3.

6 Q. (BY MR. MODI) So that's your reading of
7 the sentence?

8 MR. CHIU: Objection to form,
9 argumentative.

10 A. (Reviewing document.)

11 I believe that a person of ordinary skill
12 in the art would read this as embodiment, as either
13 an internal connection line or a dummy pattern.

14 Q. (BY MR. MODI) So, Dr. Lee, is it your
15 testimony under oath today that Lee explicitly states
16 to one of ordinary skill that 44-3 is a dummy
17 pattern?

18 A. 44-3 is either a internal connection line;
19 alternatively, it is a dummy pattern.

20 Q. What is the difference between the two?

21 MR. CHIU: Objection to form.

22 A. Well, an internal connection line means
23 that is a -- what's sometimes referred to as a local
24 interconnect, that it is connecting between two
25 regions of the -- of the chip. So it's a connection

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2 line.

3 And a dummy pattern means that it is a --
4 by "dummy" means that it does not perform any
5 electrical function, and it's also shown that it is
6 electrically isolated from the substrate and the
7 circuit thereof.

8 Q. (BY MR. MODI) So the interconnection line
9 connects the stack to other circuits?

10 A. What stack?

11 Q. I think that was in your answer.

12 A. No, that's not my answer.

13 Q. So let's say, the interconnection line
14 connects 44-3 to other circuits?

15 A. The interconnection line is a conductive
16 line -- a conductive layer that connect one part of
17 the circuit to another part of the circuit.

18 The reason why it's called internal means
19 that it's not going through metal lines. Okay? Or
20 going through metal 1 or metal 2. And that's why
21 it's called internal connection line. And that it is
22 a local -- so-called local interconnect.

23 So there's two embodiment that Lee
24 explicitly contemplates here. One is the conductive
25 pattern is a internal connection line, and the other,

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2 that is -- that the conductive pattern is a dummy
3 pattern.

4 Q. So the dummy pattern that you -- I think
5 you mentioned was electrically isolated. Where does
6 Lee say that?

7 A. Well, a person of ordinary skill in the
8 art would understand that -- first of all, from the
9 figure, you can see that 44-3 is completely
10 surrounded by insulators.

11 Second of all, if it is not a connection
12 line and, furthermore, is -- and that it is a
13 dummy -- it says it's a dummy pattern. A dummy
14 pattern is a pattern that perform no electrical
15 function, and therefore that it is not a connection
16 line, right, because there's two alternatives: a
17 connection line or a dummy pattern. So it's clearly
18 saying that the dummy pattern is not a connection
19 line, meaning that it is not connected to the
20 substrate or the circuit.

21 Q. So are you -- you don't have a top view
22 here. Right?

23 A. Lee does not disclose the plan view.

24 Q. Is it your opinion that a dummy pattern
25 would be universally understood by one of ordinary

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2 skill in the art as not performing an electrical
3 function?

4 A. Yes. If you look at the microelectronics
5 dictionary and look at "dummy," and -- you'll find
6 that it pertain to nonfunctional item, and that it
7 does not perform any electrical function.

8 Q. Where are you reading from in your
9 declaration, Dr. Lee?

10 A. Page 52 on Paragraph 105.

11 Q. So you are relying on the term
12 "nonfunctioning." Is that right?

13 A. Nonfunctioning -- pertaining to a
14 nonfunctioning item used to satisfy some format or
15 logic requirement or fulfill prescribed conditions.

16 Q. So you agree that nonfunction -- so you
17 are basically saying nonfunctional means no
18 electrical function here. Is that right?

19 A. Well, further, if you read on, you'll find
20 that it also means that not perform an electrical
21 function.

22 Q. Well, there are two different definitions
23 here. Right? So let's focus on the first one.

24 Is that right? In Paragraph 105 you list
25 two different definitions. One is dummy. Do you see

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2 that?

3 A. Yes.

4 Q. Okay. For that particular definition
5 you're relying on the term "nonfunctioning." Is that
6 right?

7 A. Well, I'm relying on the complete
8 definition.

9 Q. Okay. And the -- that particular
10 definition does not use "no electrical function."
11 Right?

12 A. Well, nonfunction -- nonfunctioning item
13 means that it's not performing any function.

14 Q. Whether electrical or otherwise?

15 MR. CHIU: Objection to form.

16 A. Generally, yeah. It says -- on the other
17 hand this says that logic requirement.

18 Q. (BY MR. MODI) So nonfunctioning item
19 means not performing any function. Right?

20 A. Well, this is about electrical
21 engineering. Okay? This is not about mechanical
22 engineering. So this is referring to nonelectrical
23 function. And if you go on and read the dummy
24 connecting -- connector plug, it clearly shows that
25 it's a connector, does not perform any electrical

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2 function.

3 Q. So the claim actually requires no -- let's
4 go back to the claim language. Can we?

5 A. Sure.

6 Q. So the claim language says a dummy pattern
7 electrically isolated from the substrate and circuits
8 thereon. Right?

9 A. Yes.

10 Q. So is it your opinion that 44-3 is
11 electrically isolated from the substrate and circuits
12 thereon?

13 A. Yes.

14 Q. Can you point me to what supports your
15 opinion?

16 A. Well, as I --

17 MR. CHIU: Objection; asked and
18 answered.

19 A. As I described earlier, that in -- in
20 Figure 4 of Lee, Lee explicitly contemplates two
21 embodiments. One where the conductive pattern is an
22 internal connection line and the other where the
23 connection -- conductive pattern is a dummy pattern.
24 Right? So, in other words, that dummy pattern is not
25 doing any connection at all.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 Q. (BY MR. MODI) So it's that magical
3 Paragraph 17-6?

4 MR. CHIU: Argumentative.
5 Objection.

6 A. I don't understand what you mean by
7 "magical."

8 Q. (BY MR. MODI) So it's that paragraph on
9 17-6 that starts with Figure 4. That's the basis for
10 your testimony?

11 A. Is it magical? What do you mean by
12 magical?

13 Q. Can you answer the last question?

14 A. What was the last question?

15 Q. I'll make it easy for you. Will a dummy
16 pattern not be connected to the substrate or any
17 other circuits?

18 MR. CHIU: Objection; lacks
19 foundation.

20 A. Well, a dummy pattern performed no
21 electrical functions. Furthermore, in Lee it said
22 that that conductive pattern is either an internal
23 connection line or dummy pattern.

24 In other words, that if it is a dummy
25 pattern, it is not a connection line. By connection

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2 line means that it is connected to the substrate or
3 the circuit. So if it is not a connection line, then
4 it means that it is not connected to the substrate or
5 the circuit.

6 Furthermore, in addition to this -- this
7 paragraph that you call "magical," the figures
8 support and clearly illustrate that -- clearly
9 disclose that the second patterned conductive layer
10 is electrically isolated from the substrate and the
11 circuit thereof.

12 Q. (BY MR. MODI) So, Dr. Lee, I want to go
13 back to 44-1. And -- or, sorry, 44-3. Earlier you
14 told me what does 44-3 include. Right?

15 A. Yes.

16 Q. Do you remember that?

17 A. Yes.

18 Q. And I think you relied on a -- relied on
19 the support for Figure 3 to support that opinion.
20 Right?

21 MR. CHIU: Objection to form.

22 A. Okay. Can you rephrase your question?

23 Q. Sure.

24 A. It's breaking up into two separate sub
25 questions.

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/25/16

2 Q. (BY MR. MODI) Let's do that. So earlier
3 you told me what does 44-3 include. Right?

4 A. Yes.

5 Q. Okay. So the record is clear, can you
6 tell me again what 44-3 includes, in your opinion?

7 A. It include, as I've shown in
8 Paragraph 102, highlighted in blue, which is the poly
9 and the gate cap.

10 Q. Okay. And where in the specification
11 does -- where does the specification of Lee support
12 that conclusion?

13 A. Well, first of all -- first of all,
14 patterning the gate, which is the first patterned
15 conductive layer and the second patterned conductive
16 layer -- the dummy pattern, that is -- a person of
17 ordinary skill in the art would know that that is
18 formed and patterned simultaneously. Okay? That it
19 will be impractical to use different masks for the
20 dummy pattern and the first patterned conductive
21 layer.

22 And so the first patterned conductive
23 layer in Figure 4 is processed at the same time as
24 the dummy pattern, simultaneously, as I described in
25 my declaration regarding Claim 4.

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2 And Figure 3 describe each layer, right,
3 in -- on Page 17-5 it says that Figure 3(a) is an
4 active region which has field oxide 32 on the
5 substrate 31 and a MOS gate, which is formed by
6 depositing and etching the gate oxide layer, the
7 poly, and gate cap in order. Okay?

8 And Figure 4 shows the second embodiment
9 of the present invention. And it doesn't describe a
10 completely different process. It shows a figure that
11 shows the first conductive layer identical to Figure
12 3(a).

13 So for those of us who read a lot of
14 technical papers all the time would understand that
15 is the same process that fabricate in Figure 3(a),
16 the first patterned conductive layer is used for the
17 gate first patterned conductive layer for Figure 4.

18 Q. So I want to go to the first part of your
19 answer. You said the first patterned conductive
20 layer and the second patterned conductive layer are
21 formed simultaneously.

22 A. Yes.

23 Q. Where does Lee teach that?

24 A. (Reviewing document.)

25 So, as I mentioned earlier, that Lee

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2 discloses a MOS gate that is formed by depositing the
3 gate electrode within this. The gate --

4 Q. What page? I'm sorry.

5 A. Page 17.5.

6 -- discloses a MOS gate that is formed by
7 depositing and etching the gate oxide layer, poly,
8 and gate cap in order.

9 It also...

10 One second.

11 (Reviewing document.)

12 There is another place saying a similar
13 thing. I want to get to that. Not only in
14 Figure 3 -- 3(a).

15 There is another place that shows the
16 same -- that is depositing gate oxide layer, poly and
17 gate cap in this sequence, and then etch them. I
18 want to look for that.

19 Oh, incidentally, earlier you mentioned
20 that -- about the doping impurity around the gate.
21 All right? Earlier you mentioned that besides
22 Page 17.4, the last paragraph, I pointed to that
23 doping impurity in the substrate around the gate.
24 Right? You said any other place. Right? And at
25 that time I couldn't find the other location that

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2 shows that. Now, actually, it dawned on me, now that
3 I remember.

4 On Page 17-8, it also show in one of the
5 claim, Claim 1(a), saying that it's "formed by doping
6 impurity on the gate in the active region on the
7 substrate and the substrate around the gate." Okay.
8 I just want to point out that it's not just in one
9 location. There is another location that says the
10 same thing.

11 (Reviewing document.)

12 If you may go to page 59 of my
13 declaration, before the footnote I wrote, "Lee
14 discloses that a MOS gate is 'formed by depositing
15 gate oxide layer, poly and gate caps in this sequence
16 and then etching them.'"

17 So that phrase is taken out from the Lee
18 patent, but I -- at this point I can't locate it.

19 MR. MODI: Why don't we take a
20 break, Dr. Lee, and then we can come back and you
21 can try to find it.

22 THE WITNESS: Okay. I'll find it
23 now.

24 (Break.)

25 Q. (BY MR. MODI) Okay. So, Dr. Lee, I think

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2 you were looking for a citation before we took a
3 break. Do you have it?

4 A. Yes.

5 Q. Okay. Can you give it to us?

6 A. Yes. It's on Page 17-2 of the Lee
7 reference, that -- it says that "in order to make a
8 structure" -- it's referring to the transistor
9 structure -- "an active region is isolated by a field
10 oxide layer (12) on a semiconductor substrate (11)
11 and a MOS gate (14) is formed by" -- which this is
12 what I quoted in my declaration -- "depositing gate
13 oxide layer, poly and gate cap in this sequence and
14 then etching them."

15 So it's the same as -- basically
16 describing the same as what is described in
17 Figure 3(a) that I cited earlier.

18 Q. So you're relying -- just to make sure.
19 So you're relying on the prior art disclosure for
20 Figure 4?

21 A. No. I'm saying that the prior art
22 disclosure and the invention disclosure are basically
23 saying the same thing, that it -- the MOS gate in
24 general is by depositing and etching the -- the
25 gate -- the gate oxide, poly, gate cap in order. So

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2 I'm saying that the invention in the prior art
3 described the gate formation process the same way.
4 That's all.

5 Q. So earlier I asked you -- or I think you
6 testified that the gate cap is a metal silicide
7 layer. Do you remember that?

8 A. Yes.

9 Q. Can you point me to where in Lee it
10 discloses that?

11 A. It does not specifically say that.
12 However, the gate cap back in 1996 is -- refer to the
13 silicide that's formed on top of the poly. So it's a
14 conductive layer. That's why, in the figure in
15 Paragraph 95, that layer is highlighted in blue.

16 Q. So you agree that the reference doesn't
17 disclose it explicitly. Right?

18 MR. CHIU: Objection; form,
19 mischaracterizes testimony.

20 A. (Reviewing document.)

21 No, it does not explicitly disclose that
22 the gate cap is a silicide layer. However, as I
23 mentioned, back in 1996, the gate cap -- the term
24 "gate cap" is referred to a silicide layer on top of
25 poly in order to reduce the overall resistance.

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2 Q. (BY MR. MODI) So let me -- can I take you
3 to 17-6.

4 A. Yes.

5 Q. If you can look at the last paragraph on
6 17-6 and let me know when you're done.

7 A. (Reviewing document.)

8 Q. Are you done?

9 A. Not yet. I want to look at...

10 (Reviewing document.)

11 Okay. Yes.

12 Q. So it refers to a cap oxide layer. Do you
13 see that?

14 A. Yes.

15 Q. So is the gate cap made of that -- is an
16 oxide layer?

17 A. I don't think that is -- refer to the gate
18 cap. It doesn't say "gate cap oxide layer." It's
19 not -- it referred -- it's not referred to the gate
20 cap at all.

21 Q. What is it, then?

22 A. See, this is a different embodiment than
23 Figure 5, and it's saying that it uses a step which
24 etching into the substrate, using oxide layers on the
25 substrate. Okay? So, in other words, that -- these

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2 are -- we're talking about the oxide layer on the
3 substrate. So this is referring to a cap oxide layer
4 on top of the substrate.

5 Q. But didn't you rely on Figure 5 in your
6 opinions earlier today?

7 A. I don't think I ever used Figure 5.

8 Q. Okay.

9 MR. MODI: Why don't we stop
10 there, and then we can pick it up in the morning.

11 THE WITNESS: Thank you.

12 (THE DEPOSITION ADJOURNED AT 5:25 P.M.)
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1 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 NVIDIA CORPORATION, §
4 §
5 §
6 § Case IPR2015-01320
7 Petitioner, §
8 §
9 § Case IPR2015-1327
10 VS. § Patent No. 6,287,902
11 §
12 SAMSUNG ELECTRONICS § Case IPR2015-1327
13 COMPANY, LTD., § Patent No. 6,287,902
14 §
15 §
16 Patent Owner. §

17 REPORTER'S CERTIFICATION
18 DEPOSITION OF JACK CHUNG-YEUNG LEE, Ph.D.
19 TAKEN FEBRUARY 25, 2016

20 I, Tamara Chapman, Certified Shorthand
21 Reporter in and for the State of Texas, hereby
22 certify to the following:

23 That the witness, JACK CHUNG-YEUNG LEE,
24 Ph.D., was duly sworn by the officer and that the
25 transcript of the oral deposition is a true
26 record of the testimony given by the witness;

27 That the original deposition was delivered
28 to Mr. Naveen Modi;

29 That a copy of this certificate was served
30 on all parties and/or the witness shown herein on
31 3/2/2016.

32 I further certify that pursuant to FRCP
33 No. 30(f)(i) that the signature of the deponent:
34 _____ was requested by the deponent or a
35

1 party before the completion of the deposition and
2 that the signature is to be returned within 30
3 days from date of receipt of the transcript. If
4 returned, the attached Changes and Signature Page
5 contains any changes and the reasons therefor;

6 X was not requested by the deponent or
7 a party before the completion of the deposition.

8 I further certify that I am neither counsel
9 for, related to, nor employed by any of the
10 parties in the action in which this proceeding
11 was taken, and further that I am not financially
12 or otherwise interested in the outcome of the
13 action.

14 Certified to by me this 2nd day of March, 2016
15
16
17

18 Tamara Chapman, CSR, RPR, CCR (LA)
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(Notary Public) MY COMMISSION EXPIRES: _____

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,	§	
	§	
Petitioner,	§	
	§	Case IPR2015-01320
VS.	§	Patent No. 6,287,902
	§	
SAMSUNG ELECTRONICS	§	Case IPR2015-1327
COMPANY, LTD.,	§	Patent No. 6,287,902
	§	
Patent Owner.	§	

ORAL DEPOSITION OF
JACK CHUNG-YEUNG LEE, Ph.D.
FEBRUARY 26, 2016
VOLUME 2 OF 2

ORAL DEPOSITION OF JACK CHUNG-YEUNG
LEE, PH.D., produced as a witness at the instance
of the Patent Owner and duly sworn, was taken in
the above styled and numbered cause on Friday,
February 26, 2016, from 9:06 a.m. to 2:36 p.m.,
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stenotype machine, at the offices of Regus,
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Suite 300, Austin, Texas.

Job No. 103799

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* * *

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1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/26/16

2 FURTHER EXAMINATION

3 BY MR. MODI:

4 Q. Good morning, Dr. Lee.

5 A. Good morning.

6 Q. You understand that you're still under
7 oath today?

8 A. Yes.

9 Q. What, if anything, did you do between when
10 we left here yesterday and now to prepare for the
11 rest of the deposition today?

12 A. I just review some documents. That's all.

13 Q. What did you review?

14 A. The declarations.

15 Q. Anything else?

16 A. Some patents.

17 Q. Which ones?

18 A. Dennison, Lee. That's it.

19 Q. Anything else?

20 A. No.

21 Q. Did you talk with your attorneys regarding
22 your testimony?

23 A. No.

24 Q. So let's pick up where we left off
25 yesterday. So if you can go to -- or let me actually

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2 do it this way. I believe you testified yesterday
3 that in Lee Figure -- Figures 3(a), Figure 4,
4 Figure 5, Figure 3(b), Figure 3(c), Figure 3(d),
5 Figure 6 all show the first patterned conductive
6 layer on the active region of the substrate spaced
7 apart from the field region. Do you recall that?

8 A. Let me get to that, please.

9 MR. CHIU: Objection;
10 mischaracterizes the witness's testimony.

11 Just to be clear, Counsel, you did
12 say yesterday you were not continuing with the
13 Lee reference today. Are you changing that?

14 MR. MODI: No. But I think we --
15 at the end of the day, we decided to quit early,
16 so I'm just finishing up.

17 MR. CHIU: Well, I think you had
18 said yesterday on the record that you were going
19 to continue with Dennison the next day. You also
20 represented that to me off the record yesterday.

21 MR. MODI: That was in the
22 morning. And in the evening, Dr. Lee had to
23 leave early, and I said, "That's fine. He can
24 leave early." So I don't --

25 MR. CHIU: I don't want to use up

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2 your time, so why don't you just go ahead.

3 MR. MODI: Okay.

4 A. No. I think that what I said was
5 Figure 3(a), (b), (c), (d), Figure 4, Figure 5, and
6 Figure 6 and including the prior art, Figure 1 and
7 Figure 2 -- Figure 1(a) and (b), Figure 2(a) and (b)
8 all shows that the first patterned layer is spaced
9 apart from the field region.

10 Q. (BY MR. MODI) Can you turn to Figure 5
11 for me?

12 A. Yes. Okay.

13 Q. In your opinion, the gate structure shown
14 in the middle of Figure 5 is a first patterned
15 conductive layer. Correct?

16 MR. CHIU: Objection; form.

17 A. In the Figure 5, the gate structure --
18 there is only one gate structure. Are you referring
19 to that one?

20 Q. (BY MR. MODI) Yes, sir.

21 A. Yeah. That is the first patterned layer
22 on the active region.

23 Q. And would you agree that the conductive
24 portion of the first patterned conducted layer is
25 made up of poly and gate cap?

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2 MR. CHIU: Objection; form.

3 A. In the context of the '902. Is that
4 right? In the context of the '902 patent. Right?

5 Q. (BY MR. MODI) I'm not sure I understand.
6 What do you mean?

7 A. Is your question that the conductive
8 portion of the first patterned layer is made up of
9 poly and gate cap? Is that in the context of the
10 '902 patent?

11 Q. Does your answer change?

12 A. Well, the reason is that the first
13 patterned conductive layer in '902, Claim 3,
14 comprises conductive portions and insulating spacers.
15 So the first patterned conductive layer actually
16 contain both the conductive portion and the
17 insulating spacer along the side wall.

18 Oh, you're saying only the conductive
19 portion. Okay. The conductive portion is -- I
20 didn't understand your questions. Yes, the
21 conductive portion comprises the poly and gate cap.

22 Q. And you would agree that the lower portion
23 is a poly and the upper portion is a gate cap.
24 Correct?

25 MR. CHIU: Objection to form.

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2 A. The lower portion of the conductive
3 portion is the poly and the upper portion is a gate
4 cap.

5 Q. (BY MR. MODI) And yesterday you testified
6 that the gate cap is a silicide layer. Correct?

7 A. Yes. That's the term that's used in --
8 back in 1996 or so, referring to gate cap --
9 referring to tungsten silicide or titanium silicide
10 or some silicide as a gate cap.

11 Q. Can you go to Page 17-6 for me --

12 A. Yes.

13 Q. -- of Lee. At the bottom, the last line
14 of Lee, it refers to cap oxide layer. Do you see
15 that?

16 A. Yes.

17 Q. Do you recall our discussion of that --

18 A. Yes.

19 Q. -- last night?

20 A. Yes.

21 Q. What is your understanding of the cap
22 oxide layer in Lee?

23 MR. CHIU: Objection to form.

24 A. (Reviewing document.)

25 The -- Figure 5 is a different embodiment

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2 as in Figure 3(a) and Figure 4. And the gate
3 sidewall and cap oxide layer, I believe the cap --
4 the cap oxide layer is on top of the silicide layer,
5 on top of the gate cap.

6 Q. (BY MR. MODI) Can you point for my
7 benefit where you believe it's shown in Figure 5,
8 where it would be?

9 A. Well, it's not drawn very clearly, but I
10 think there is a layer of the -- oxide layer on top
11 of the gate cap.

12 Q. Can you show me where it is, Dr. Lee?

13 A. I think this is slightly -- this might be
14 a thicker layer up here on top of the gate cap, which
15 is, in turn, on top of the poly.

16 (Exhibit 2004 was marked.)

17 Q. (BY MR. MODI) Dr. Lee, I'm going to hand
18 you what's been marked as Samsung Exhibit 2004 in IPR
19 2015-1327. Can you tell us what Exhibit 2004 is?

20 A. It's Exhibit 1107, Page 17 and Page 18.

21 Q. So it's Page 17 and 18 of Lee. Is that
22 correct?

23 A. Yes.

24 Q. Okay. I'm going to hand you a pen. I
25 would like you to mark what you believe is the cap

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2 oxide in Figure 5.

3 A. Okay. Let me read that one more time.

4 (Reviewing document.)

5 I don't think my declaration discuss
6 Figure 5 at all. So I believe this is not discussed
7 in my declaration and that -- isn't it outside the
8 scope of my declaration?

9 Q. Would you please do what I asked you to
10 do?

11 MR. CHIU: Objection to form.

12 A. (Complies.)

13 Q. (BY MR. MODI) Dr. Lee, I'm going to hand
14 you Exhibit 2004. Can you go ahead and indicate what
15 you just did.

16 A. So this layer, which the figure did not
17 clearly indicate, is that that's the cap oxide layer
18 on top of the gate cap which, in turn, on top of the
19 poly.

20 Q. Can you go ahead and indicate for me the
21 gate cap and poly as well.

22 A. (Complies.)

23 MR. CHIU: Objection to form.
24 Outside the scope of his declaration.

25 Q. (BY MR. MODI) Dr. Lee, does the Lee

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2 reference describe the cap oxide anywhere?

3 MR. CHIU: Objection; beyond the
4 scope of his declaration.

5 A. (Reviewing document.)

6 Yes.

7 Q. (BY MR. MODI) Where?

8 A. In fact, if you look at Claim 14.

9 Q. Okay. I'm there.

10 A. It's clearly indicating that the gate
11 oxide layer is the -- is the oxide -- is the cap
12 oxide layer, and, furthermore, it says, "The gate cap
13 is a conductive layer," it says, "for which gate
14 oxide layer and gate" -- "a conductive layer gate
15 cap."

16 So it describe that a gate cap, as I said,
17 is a conductive layer, such as a silicide.

18 Q. Anywhere else?

19 A. (Reviewing document.)

20 I think that's the one place that I found
21 at this point. Again, I -- in preparing the
22 declaration, I did not look at Figure 5, but this
23 support what I said, that the gate cap is a
24 conductive layer and the -- on top of that, it's a
25 cap oxide layer, in which they call that gate oxide

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2 layer.

3 Q. So, in your opinion, the oxide cap is the
4 same thing as gate oxide?

5 MR. CHIU: Objection; beyond the
6 scope of Dr. Lee's declaration.

7 A. (Reviewing document.)

8 No. I'm sorry. I think that the gate
9 oxide layer is referred to the gate oxide underneath
10 the poly. But here it does describe what is a gate
11 cap. It's a conductive layer. And that's the key
12 that -- what I said yesterday, that the gate cap is a
13 conductive layer.

14 Q. (BY MR. MODI) So do you still stand by
15 your testimony that the cap oxide layer is on top of
16 the gate cap?

17 A. Again, I have not looked at Figure 5 in
18 forming my opinion put in my declaration. So the
19 last -- when you asked me at this point, yeah, I
20 think that the gate -- the cap oxide layer is -- for
21 this to be seems like it's used as a mask to etch the
22 semiconductor substrate is on top of the gate cap.

23 Q. So would you agree that the gate in
24 Figure 5 -- in the Figure 5 embodiment is made
25 differently from the gate in Figure 3?

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2 MR. CHIU: Objection to form.

3 Beyond the scope of Dr. Lee's declaration.

4 A. Well, it appears that the cap oxide layer
5 have not been -- were not described and -- and used
6 in Figure 3(a), Figure 3(b), Figure 3(c), and
7 Figure 3(d) and Figure 4 and only used in Figure 5.

8 So based on that, it appears that Figure 5
9 is -- is a new embodiment in which they purposely
10 etch the substrate to create a higher step, and by
11 doing so, they would have to add a cap oxide layer.

12 THE REPORTER: I need to take a
13 very quick technology break.

14 (Break.)

15 Q. So, Dr. Lee, you said Figure 5 is a new
16 embodiment. I believe that was the term you used.

17 MR. CHIU: Objection;
18 mischaracterizes the witness's testimony.

19 A. Well, Figure 5 is a drawing of the third
20 embodiment of the invention.

21 Q. (By MR. MODI) So you're changing your
22 testimony. I believe you said new embodiment.

23 A. Well, "new" meaning that it's different
24 from the second and first embodiment.

25 Q. Would you agree that Figure 4 is new in

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2 the sense it's different from the other embodiments?

3 MR. CHIU: Objection to form.

4 A. What other embodiment?

5 Q. (BY MR. MODI) Figure 3.

6 MR. CHIU: Objection to form.

7 A. No. Figure 4 basically describe that
8 use -- using a new -- using an etch-inhibiting layer
9 which could be internal connection line or a dummy
10 pattern. But the rest of the fabrication basically
11 is the same as Figure 3, (a), (b), (c), and (d).

12 So Figure 3 and Figure 4 are the same in
13 terms of this -- the fabrications of the first
14 patterned conductive layer and the MOS gate
15 structure, while, on the other hand, Figure 5 clearly
16 is a -- describing a embodiment that modified the
17 gate structure in order to form and etch the
18 substrate using the gate oxide -- using the oxide
19 layer on the substrate as a mask. Do you see the
20 difference?

21 Q. (BY MR. MODI) So you said Figure 5
22 modified the gate structure?

23 A. Well --

24 MR. CHIU: Objection to form,
25 mischaracterizes the witness's testimony.

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2 A. No. I said that the Figure 5 -- that the
3 gate structure has added a cap oxide layer on top of
4 the conductive layer gate cap.

5 Q. (BY MR. MODI) Does Figure 5 have any
6 commonality with Figures 4 or 3?

7 MR. CHIU: Objection to form,
8 beyond the scope of Dr. Lee's declaration.

9 A. What do you mean, commonality?

10 Q. (BY MR. MODI) In the gate structure.

11 MR. CHIU: Objection; form, beyond
12 the scope of Dr. Lee's declaration.

13 A. Well, you could see that it is different,
14 the gate structure.

15 Q. (BY MR. MODI) From Figure 4?

16 A. Figure 4, yeah.

17 Q. And it's different from Figure 3?

18 A. Yes.

19 Q. In what way?

20 A. Well, the -- the spacer, 54-2, is go
21 deeper into the -- into the substrate, as you can
22 see. And that's how they create a bigger step, you
23 see.

24 Q. So you're basing that simply on the
25 drawing?

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2 A. Well -- and the description in -- in
3 Page 17.6.

4 Q. What description in particular?

5 A. If you read it, it says "using the step
6 (57) randomly formed by etching the semiconductor
7 substrate."

8 So, in other words, that the spacer is --
9 go deeper into the -- into the substrate, and you can
10 see that even drawing shows that -- that spacer 54-2
11 is -- go deeper into the substrate than Figure --
12 than 44-2 in Figure 4.

13 Q. What about the gate stack itself? Is that
14 different from Figure 4?

15 MR. CHIU: Objection to form,
16 beyond the scope of Dr. Lee's declaration.

17 A. That is part of the gate stack.

18 Q. (BY MR. MODI) Okay. What else do you see
19 that's different?

20 MR. CHIU: Objection; form, beyond
21 the scope of Dr. Lee's declaration.

22 A. You mean the drawing itself?

23 Q. (BY MR. MODI) I'm just asking you for the
24 differences, Dr. Lee, in the gate structure.

25 Identify for me all the differences.

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2 A. Right. So the --

3 MR. CHIU: Same objections.

4 A. The gate structure on -- in Figure 5
5 consists of the poly and gate cap, a conductive layer
6 gate cap, as discussed in Claim 14. And in order for
7 this embodiment to work, one has to add what the
8 patent called a cap oxide layer as a mask on top of
9 the gate cap, the conductive layer gate cap.

10 Q. (BY MR. MODI) So, Dr. Lee, I'm sorry for
11 asking the same question again, but I don't think you
12 answered my question. I'm just asking you for the
13 differences.

14 A. I told you the differences.

15 MR. CHIU: Same objections.

16 Q. (BY MR. MODI) Okay. Can you list them
17 for me?

18 MR. CHIU: Same objection.

19 Objection to form, outside the scope of Dr. Lee's
20 declaration.

21 A. In Figure 4, the gate -- the first
22 patterned conductive layer, as described in 17.5 and
23 17.6, comprise of the poly and conductive layer gate
24 cap.

25 In Figure 5, the first patterned

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2 conductive layer comprised of the poly, the gate cap,
3 and the cap oxide layer.

4 Q. (BY MR. MODI) Can I ask you to -- so we
5 were looking at 17-6 of Lee?

6 A. Yes.

7 Q. And we were looking at the cap oxide
8 layer. Right? Yes?

9 A. In the last sentence?

10 Q. Right.

11 A. Yes.

12 Q. And we've also talked about gate cap.
13 Right?

14 A. The conductive layer gate cap, yes.

15 Q. Okay. Can you point me -- if you can look
16 through Lee, can you point to me what disclosure of
17 "cap" there is other than in 17-6?

18 A. I don't understand your question.

19 MR. CHIU: Objection to form.

20 Q. (BY MR. MODI) What don't you understand?

21 A. The word "cap"?

22 Q. Yes.

23 MR. CHIU: Objection to form,
24 outside the scope of Dr. Lee's declaration.

25 A. And only on Page 17.6?

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2 Q. (BY MR. MODI) No. I'm saying other than
3 17-6. Can you look through Lee and identify for me,
4 do you see any other disclosure of "cap"?

5 MR. CHIU: Same objections.

6 A. Well, there's cap oxide layer, there's
7 gate cap, there's conductive layer gate cap in
8 Claim 14. Do you want me to search for the word
9 "cap"?

10 I mean, you seem to imply that cap -- the
11 word "cap" represent the same thing. Obviously it is
12 not. I think...

13 I think that might be it.

14 Q. (BY MR. MODI) So you mentioned -- let me
15 ask you this. Does every embodiment of Lee include a
16 cap oxide layer?

17 MR. CHIU: Objection to form,
18 beyond the scope of Dr. Lee's declaration.

19 A. Well, on Page 17.5, when it describe
20 Figure 3(a), it simply saying that there's a poly and
21 gate cap in order. So it appears that Figure 3(a),
22 which also saying that's Figure 3(b), Figure 3(c),
23 Figure 3(d), only consists of poly and the conductive
24 layer gate cap.

25 Q. (BY MR. MODI) What about Figure 4?

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2 A. Figure 4 -- since Figure 4 is only
3 describing the additional dummy layer on the field
4 region, so that the gate structure will be the same
5 as the Figure 3, (a), (b), (c), and (d), which is the
6 conductive layer, consists of poly and gate cap,
7 which is conductive.

8 Q. How do you know that the dummy
9 structure -- or the dummy layer is the same --
10 actually, let me withdraw that.

11 How do you know that the dummy layer in
12 Figure 4 is the same as the gate structure in
13 Figure 3?

14 MR. CHIU: Objection to form.

15 A. Well, as I describe in my declaration on
16 Page 59 and 60, that "This is a well-known process
17 for patterning a MOS gate," that a person of ordinary
18 skill in the art "would know that the first
19 conductive layer and the second conductive layer,"
20 which is called a "dummy pattern" in Lee, "are formed
21 and patterned simultaneously" and is the only design
22 choice that would be practical in manufacturing,
23 because there are thousands and thousands of these
24 gates formed on the substrate. And one of the things
25 that is important is to minimize the number of steps

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2 and the number of masks, so a chip designer would
3 create a mask that would provide a pattern to deposit
4 all gates at the same time simultaneously.

5 Q. (BY MR. MODI) Dr. Lee, where are you
6 reading from?

7 A. I told you, on Page 60.

8 Q. Of which declaration, just for the record?

9 A. Declaration 2.

10 Q. Can you identify the exhibit number?

11 A. 1116.

12 Q. So is -- what you just read, does that
13 appear explicitly in Lee?

14 MR. CHIU: Objection to form.

15 A. Well, as you can see in Figure 4, the
16 formation of the etch stop layer, 44-2 and 44-3, on
17 the first and second patterned conductive layer, this
18 says is through deposition and etch-back process.
19 Okay.

20 And the gate sidewall in Figure 3(a),
21 which is 34-1, are also formed through etch-back --
22 deposition and etch-back process.

23 And as you can see as shown in Figure 4,
24 the first and second patterned conductive layers have
25 the same number and the appearance of the spacers.

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2 So performing the deposition and etch-back for all
3 the gate at the same level simultaneously is well
4 known in the semiconductor fabrications. And that
5 even though Lee does not explicitly use the word
6 "simultaneously," that the figures and the
7 specification clearly disclose that they are formed
8 simultaneously. And as I -- let me stop here.

9 Q. (BY MR. MODI) Can the dummy pattern be
10 another mechanical structure other than a gate stack?

11 MR. CHIU: Objection to form.

12 A. What other material are you referring to?
13 I don't understand the question.

14 Q. (BY MR. MODI) Do you understand the term
15 "mechanical structures"?

16 A. Well, the dummy -- dummy pattern -- you're
17 right, the dummy pattern only serve as a mechanical
18 purpose. So it is a mechanical structure.

19 Q. So my question is, can the dummy pattern
20 be another mechanical structure other than a gate
21 stack?

22 MR. CHIU: Objection to form.

23 A. You mean formed with a different layer of
24 material?

25 Q. (BY MR. MODI) I'm just trying to

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2 understand what other mechanical structures can a
3 dummy pattern constitute.

4 MR. CHIU: Objection to form.

5 A. Why would anyone do that?

6 Q. (BY MR. MODI) Can you just answer my
7 question?

8 A. Yeah, I am answering your question. That
9 is -- that is not reasonable to use a different
10 material when you deposit -- you just cannot deposit
11 different material in different part of the substrate
12 on the layer.

13 And if you deposit a layer of -- for the
14 gate stack and then remove it and then put -- remove
15 part of it and then put down another layer different
16 from that, that's -- makes the process very
17 complicated, unreliable. That's not the right way to
18 do things, and that's unreasonable, and it's kind
19 of -- kind of stupid in some way. I'm sorry to say
20 that, but it is.

21 A person of ordinary skill in the art
22 would not choose such a complicated process to
23 achieve something that is doable and much simpler
24 using a same material and same step and formed
25 simultaneously as the gate stack.

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2 Q. Does Lee say that you cannot do that?

3 MR. CHIU: Objection; form.

4 A. Well, Lee discloses that it does that, as
5 I mentioned. But to the extent that Lee does not
6 explicitly disclose, then it's obvious that this --
7 that this dummy gate or dummy pattern is formed at
8 the same time and the same material as the gate stack
9 on the active region.

10 Q. (BY MR. MODI) I don't think you answered
11 my last question, Dr. Lee.

12 MR. CHIU: Is there a question
13 pending?

14 A. Does Lee say that you cannot do that? Is
15 that the question?

16 Q. (BY MR. MODI) Uh-huh.

17 MR. CHIU: Asked and answered.
18 Objection; asked and answered and objection to
19 form.

20 A. You're saying does Lee say that you cannot
21 use a different materials and process as the first
22 conductive layer -- first patterned conductive layer
23 on the active region? Is that what you're saying?

24 Q. (BY MR. MODI) Yeah. Start with that.

25 A. I think I answered the question, that it

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2 does say that -- at several places -- that through
3 deposition and etch-back process.

4 And so a person of ordinary skill in the
5 art would understand that that -- that means that the
6 process of Figure 3 and Figure 4 are the same and
7 that the etch stop layer is done by -- on the same
8 way. So I don't see how it is not disclosed or at
9 least make obvious that the two structures are the
10 same.

11 Q. So let me ask you this. Is it your
12 testimony today that, unless Lee says otherwise, a
13 dummy pattern must be a gate stack?

14 MR. CHIU: Objection to form,
15 mischaracterizes the witness's testimony.

16 A. Well, first of all, all of the figures,
17 the dummy pattern and the first patterned conductive
18 layer, looks the same. Second of all, the
19 descriptions of the process are the same, and so
20 there's no disclosure in Lee indicating the contrary.
21 In other words, there's no description in Lee saying
22 that it's using a different structure and process.

23 And, as I mentioned, that forming the
24 first patterned conductive layer and second patterned
25 conductive layer, which is a dummy pattern,

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2 simultaneously are the only design choice that would
3 be practical from a manufacturing standpoint.

4 Q. (BY MR. MODI) Dr. Lee, you did not answer
5 my question. It's a very simple question. Can you
6 give me a yes or no?

7 And the question is, so it is your
8 testimony today that, unless Lee says otherwise, a
9 dummy pattern must be a gate stack? Yes or no.

10 MR. CHIU: Objection; form,
11 mischaracterizes the witness's testimony.

12 A. No, I think I answered your question, that
13 all the indication, in the figure, the
14 specifications, and a knowledge of a person of
15 ordinary skill in the art, that the first patterned
16 conductive layer and second patterned conductive
17 layer are formed the same way and patterned
18 simultaneously.

19 So Lee does not disclose -- what do you
20 say? -- that -- that the dummy pattern and the gate
21 stack are formed differently and at the different --
22 using different masks. So I think it is unreasonable
23 to say that the dummy patterned and the first
24 patterned conductive layer are formed differently,
25 unless Lee specifically say that.

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2 Q. (BY MR. MODI) So the answer is yes to my
3 question?

4 A. No. I think I -- I -- the answer is yes,
5 and also I want to clarify that, what it means.

6 Q. Do all structures made with the deposition
7 and etch-back have to end up with the same structure?

8 MR. CHIU: Objection to form.

9 A. I don't understand what you mean by "same
10 structure." You mean same dimension, same width, or
11 what? I mean, it depends on the -- what -- it's such
12 a general question. What do you mean by that?

13 Q. (BY MR. MODI) Same sequence of layers?

14 A. Are you talking about Figure 3, Figure 4?

15 Q. I'm talking about --

16 A. In general, hypothetical?

17 Q. I'm talking about in the context of Lee.

18 A. In the context of Lee, it shows that the
19 structures end up at same structure in the figures.
20 You can see.

21 Q. So it's your --

22 A. And the specification also say that.

23 Q. So it's your sworn testimony today that
24 all structures made with the deposition and etch-back
25 in Lee and not with the same layer configuration?

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2 A. No, I'm not saying that. You can see that
3 Figure 5 looks different from the other figures, even
4 though it's also deposition and etch-back, because
5 it's etched into the substrate more, so that the
6 sidewall is now effectively taller. This is what
7 Figure 5, the third embodiment, is trying to do.

8 Q. So with the exception of Figure 5, is it
9 your sworn testimony today that all structures made
10 with the deposition and etch-back have to end up with
11 the same layer configuration?

12 MR. CHIU: Objection to form.

13 A. Well, what I'm saying is that -- only that
14 the structures made with deposition and etch-back
15 shown in Lee and in the specification, but also in
16 the figures also shows that -- support the fact that
17 they are the same layer configurations.

18 Q. (BY MR. MODI) So are you saying that
19 deposition and etch-back does not mean you're going
20 to end up with the same layer configuration?

21 MR. CHIU: Objection to form.

22 A. Are you saying formation of the sidewall
23 through that process?

24 Q. (BY MR. MODI) The gate structure.

25 MR. CHIU: Objection; form.

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2 A. No, what I'm saying is that the -- the
3 gate structure are the same in all the figures.
4 Figure 3, Figure 4, Figure 5. But Figure 5, the
5 difference is that the sidewall is different. That's
6 all.

7 Q. (BY MR. MODI) Okay. Is that the only
8 difference?

9 A. Difference what?

10 MR. CHIU: Objection to form.

11 Q. (BY MR. MODI) You said only the sidewall
12 is different.

13 A. Well, also that the --

14 MR. CHIU: Objection to form.

15 A. -- in Figure 5 -- also in Figure 5 the
16 substrate is etched to create a step. So that's
17 another difference. And Figure 5 does not show a
18 dummy pattern on the field region.

19 MR. MODI: Should we take a break?

20 THE WITNESS: Sure.

21 (Break.)

22 Q. (BY MR. MODI) Dr. Lee, during the break
23 did you talk to you attorneys about the substance of
24 your deposition?

25 A. No.

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2 Q. Did you discuss anything with them?

3 A. About the flights, getting the luggage.

4 MR. CHIU: Objection; relevance.

5 Q. (BY MR. MODI) So do you have the '902
6 patent in front of you, Dr. Lee?

7 A. Yes.

8 Q. Can I have you go to Claim 1, please?

9 A. Yes.

10 Q. In Claim 1 we talked about a limitation
11 yesterday, specifically the one that says "an
12 insulating spacer along a sidewall of the second
13 patterned conductive layer." Do you remember that?

14 A. Yes.

15 Q. Is it your opinion that this claim feature
16 requires that a spacer directly touch the sidewall of
17 the second patterned conductive layer?

18 A. (Reviewing document.)

19 Well, in Lee the spacer does touch the
20 sidewall and also is along the sidewall. So does it
21 have to be? Probably not.

22 Q. Can I have -- do you have the Yasushige
23 reference in front of you?

24 A. Yes.

25 Q. Do you have it? It's your opinion that

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2 Yasushige discloses a dummy pattern. Is that right?

3 A. Yes.

4 Q. And I believe it's -- you say it's
5 referenced numeral 7d?

6 A. Yes. Yes, the dummy pattern 7d.

7 Q. And I believe it's your position that
8 Yasushige -- in Yasushige, the dummy pattern protects
9 the field oxide layer from etching?

10 A. Yes. Yasushige recognize that during the
11 etching process of the insulator, that any mask
12 misalignment can cause damage to the field oxide,
13 unless a dummy pattern protect the field oxide.

14 Q. Can I have you turn to Figure 6 of
15 Yasushige. Are you there?

16 A. Yes.

17 Q. In Figure 6, does reference numeral 5
18 denote the field oxide region?

19 A. Yes, 5 is the field oxide region.

20 Q. And do you see dummy pattern 7d on two of
21 the regions denoted as 5?

22 A. Yes, there is 7d on top of 5.

23 Q. And then there is also two other regions
24 denoted as 5 that don't have dummy pattern 7d. Is
25 that right?

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2 A. That's right, yes.

3 Q. And you agree that the device of Figure 6
4 undergoes an isotropic etching to form sidewalls of
5 gate 7?

6 A. Sidewall, you mean 37? Did you say 7 or
7 37?

8 Q. I said sidewalls of gate 7.

9 A. Oh, on the active region of gate 7. Okay.
10 Yes.

11 Q. And you agree that there is no dummy
12 pattern 7d to protect two of the field oxide regions
13 5?

14 A. Yeah, 7d, the two 7d's in Figure 5
15 through 7 and some of the field oxide do not have 7d
16 on top.

17 Q. So the ones that don't have 7d on top,
18 they don't protect those regions. Right?

19 A. That's right. Those oxide are not
20 protected by the etch-inhibiting layer, the dummy
21 layer 7d.

22 Q. Dr. Lee, can I have you turn to the '902
23 patent again for me, please?

24 A. Okay.

25 Q. And if you can go -- turn to Paragraph 27

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of your declaration for me.

A. Which declaration?

Q. Which one do you have in front of you?

A. I have both of them.

Q. Okay. I don't think it matters, so...

A. What page?

Q. Which declaration do you have, for the record?

A. 1013.

Q. Okay. I'm just handing this back to you. It's just the exhibit for the court reporter.

Can you go to Paragraph 27 of Exhibit 1013? Are you there?

A. Yes.

Q. Can you read Paragraph 27 to yourself and let me know when you're done?

A. (Reviewing document.)

Yes.

Q. Do you agree that in Figure 4, Element 44 denotes a first patterned conductive layer and Element 44A denotes a second patterned conductive layer?

MR. CHIU: Objection; compound.

Q. (BY MR. MODI) Dr. Lee, let me know when

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2 you're ready. Actually, I'll just read it for the
3 benefit of the court reporter.

4 Do you agree that in Figure 4, Element 44
5 denotes a first patterned conductive layer, and
6 Element 44A denotes a second patterned conductive
7 layer?

8 MR. CHIU: Objection; form.

9 A. Well, I think the first patterned
10 conductive layer comprised of the conductive portion
11 and the insulating spacer along the sidewall. If you
12 look at Claim 3 of the patent, it says that the
13 "first patterned conductive layer comprises a
14 conductive portion and insulating spacers along
15 sidewalls thereof."

16 Q. (BY MR. MODI) I think my question was
17 simple. Let's go back. Can you look at Paragraph 27
18 of your declaration for me?

19 A. Yes.

20 Q. Okay. You have that in front of you.
21 Right?

22 A. Yes.

23 Q. In that paragraph, you testify that 44A is
24 a second patterned conductive layer. Yes or no?

25 A. Yes.

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2 Q. Okay. And in that same paragraph you
3 testified that Item 44 is the first patterned
4 conductive layer. Do you see that?

5 A. Yes. That it -- that is, the first
6 patterned conductive layer is the conductive portion
7 of the first patterned conductive layer. The first
8 patterned conductive layer, according to Claim 3,
9 comprises both conductive portions and the insulating
10 spacers, but other -- I mean, you could say that the
11 first patterned conductive layer only conduct -- only
12 the first -- only the conductive portion, and that's
13 fine too.

14 But I think with respect to Claim 3, that
15 the first patterned conductive layer comprise both a
16 conductive portion and the insulating spacers. So --

17 Q. Dr. Lee, is Paragraph 27 correct?

18 A. Yes.

19 Q. In Paragraph 27 you say, under the figure,
20 that "...the second patterned conductive layer is
21 electrically isolated and thus serves as a dummy
22 pattern." Do you see that?

23 A. Where are you reading?

24 Q. Right under the figure, Paragraph 27. It
25 starts "the second."

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2 A. I see, yeah.

3 (Reviewing document.)

4 Yes, it is electrically isolated.

5 Q. And you point to Column 4, Lines 27
6 through 30?

7 A. Yes.

8 Q. Do you see that?

9 A. Yes.

10 Q. Can you go to Column 4, Lines 27 through
11 30 of the '902 patent?

12 A. Okay.

13 Q. Read that to yourself and let me know when
14 you're done.

15 A. (Reviewing document.)

16 Yes.

17 Q. Do you agree that in Column 4, Lines 27
18 through 30, the '902 patent explicitly states that
19 the second patterned conductive layer is electrically
20 isolated?

21 A. That's what it says on Column 4.

22 Q. Can I have you go to Column 5, Lines 36
23 through 38?

24 A. Line 36 to what?

25 Q. 38. If you could read those to yourself

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2 and let me know when you're done.

3 A. (Reviewing document.)

4 Yes, I'm done.

5 Q. Do you agree that in Column 5, Lines 36
6 through 38, the '902 patent explicitly states that
7 the second patterned conductive layer serves no
8 electrical function. Right?

9 A. Yes.

10 Q. So let me ask you, if you only had in
11 front of you Figure 4 of the '902 patent without the
12 benefit of the language in the specification that we
13 just read, would you still say that Element 44A is
14 electrically isolated and thus serves as a dummy
15 pattern?

16 MR. CHIU: Objection; form,
17 incomplete hypothetical.

18 A. (Reviewing document.)

19 Well, I mean, now that the process and the
20 descriptions of the structures are disclosed, then a
21 person of ordinary skill in the art would know that
22 that is electrically isolated and does not serve any
23 electrical function.

24 So by just taking away the description, it
25 still doesn't take away the fact that it is

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2 electrically isolated and serves no electrical
3 function. I mean, every figure have some description
4 and caption -- at least some caption associated with
5 it.

6 Q. (BY MR. MODI) Okay. So let me break this
7 down for you. So assume the language in Column 4,
8 Lines 27 through 30, and Column 5, Lines 36 through
9 38, does not exist in the '902 patent.

10 A. Yes.

11 Q. Is it your opinion that Element 44A is
12 electrically isolated and thus serves as a dummy
13 pattern?

14 MR. CHIU: Objection; form,
15 incomplete hypothetical.

16 A. No. There are many other places in the --
17 in the specification talk about the purpose of the
18 invention, and that it is electrically isolated in
19 Column 3, and many other places talk about
20 etch-inhibiting layer. So I don't understand -- just
21 taking those lines out would not take away the fact
22 that 44A is electrically isolated and serve as a
23 dummy pattern.

24 Q. (BY MR. MODI) Okay. Let me ask you this
25 way. Assuming the specification did not use

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2 electrical isolation language, but you had a figure
3 like Figure 4 that shows a cross-sectional view of a
4 conductive layer with insulators on all sides, would
5 your opinion change as to whether the second
6 conductive layer is electrically isolated?

7 MR. CHIU: Objection; form,
8 incomplete hypothetical.

9 A. Are you saying that you change the problem
10 completely, take away the whole specifications, and
11 tell me that 44A is not electrically isolated? Then,
12 yeah, it's not electrically isolated, then.

13 Q. (BY MR. MODI) That wasn't my question,
14 Dr. Lee. Would you like me to ask it again?

15 A. Yes, please.

16 Q. Assuming the specification does not use
17 the electrical isolation language but you had a
18 figure like Figure 4 that shows a cross-sectional
19 view of the conductive layer with insulators on all
20 sides, would your opinion change as to whether the
21 second conductive layer is electrically isolated?

22 MR. CHIU: Objection; form,
23 incomplete hypothetical.

24 A. So you're saying that in the specification
25 you arbitrarily take away the word "electrically

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2 isolated" from everywhere?

3 Q. (BY MR. MODI) Yes.

4 A. What are you replacing with? That's not a
5 complete sentence there.

6 Q. I want you to assume that that doesn't
7 exist in the specification.

8 MR. CHIU: Objection; form,
9 incomplete hypothetical.

10 A. No. The -- if you read the specification
11 and understand the problem that's trying to solve,
12 and knowing what the problem that you're trying to
13 solve, and you take away, arbitrarily, that -- first
14 of all, the paragraph doesn't make sense anymore.
15 And -- and knowing the fact that it is electrically
16 isolated, you're taking away some paragraph and
17 change the problem completely, it still doesn't take
18 away the fact that 44A is electrically isolated.

19 Q. (BY MR. MODI) Do you agree that Figure 4
20 shows a cross-section?

21 MR. CHIU: Objection to form.

22 A. I mean, cross-section of what?

23 Q. (BY MR. MODI) Cross-section of an
24 embodiment that's shown.

25 A. Yeah, it does show a cross-section.

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2 Q. Of what?

3 A. Of a microelectronic structure.

4 Q. And do you agree that Figure 4 there is a
5 conductor with insulating layers on all sides?

6 A. Are you referring to 44A?

7 Q. Sure. Let's go with that.

8 A. Now, are you taking away all the
9 specification again, that -- the description of 40a,
10 46a, 42, 40? Are you taking away all the description
11 again? What's the boundary condition of your
12 hypothetical question?

13 Q. I haven't gotten there yet.

14 A. So what's your question?

15 Q. My last question was do you agree that
16 Figure 4, there is a conductor 44A with insulating
17 layers on all sides?

18 MR. CHIU: Objection to form.

19 A. At the point of the fabrications at this
20 point.

21 Q. (BY MR. MODI) Assume that you only had
22 this information and nothing else. Would you say
23 that 44A is electrically isolated?

24 MR. CHIU: Objection; form.

25 A. Assume that I only have this information.

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2 What information?

3 Q. (BY MR. MODI) That Figure 4 shows a
4 cross-section, and that Figure 4, there is a
5 conductor 44A with insulating layers on all sides.

6 A. So you're saying that -- assuming that I
7 only have the figure?

8 Q. And the information I just gave you.

9 MR. CHIU: Objection to form.

10 A. The information that the insulators are on
11 all four sides. Okay. So let's assume that.

12 Q. (BY MR. MODI) Would you say that 44A is
13 electrically isolated?

14 A. Well, knowing '902 patent, and knowing
15 what it says, you know, you change the problem, and
16 the '902, the specification clearly say that 44A is
17 electrically isolated. So if you change a problem
18 and, you know, that doesn't take away the fact that
19 44A is electrically isolated.

20 Q. So, Dr. Lee, I asked you to assume certain
21 facts. You're an expert here. Right?

22 A. Yeah.

23 Q. So I'm entitled to ask you hypotheticals.
24 Do you understand that?

25 A. Okay.

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2 MR. CHIU: Objection. Harassing
3 the witness.

4 Q. (BY MR. MODI) So I'm asking you a
5 hypothetical.

6 A. Okay.

7 Q. All right? Assume you only had the
8 information that I gave you, which is Figure 4.
9 There is a conductor 44A with insulating layers on
10 all sides. That is all the information you had.
11 Would you say that 44A is electrically isolated?

12 MR. CHIU: Objection to form,
13 incomplete hypothetical.

14 A. Is that a cross-section representative of
15 the entire structure or what is -- you know, give me
16 the description of your cross-section, if you have
17 this hypothetical.

18 Q. (BY MR. MODI) It's the cross-section that
19 you're seeing in front of you.

20 A. No, what is the cross-section of? The
21 cross-section of --

22 Q. A microelectronic structure.

23 A. -- a microelectronic structure of -- of
24 the entire microelectronic structure?

25 Q. Let's say it's a cross-section of a gate

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2 structure.

3 A. But is it representing -- representative
4 of the cross-section of across the -- the device or
5 how do you cut the structure?

6 Q. It would be the same type of cross-section
7 that you have in front of you in Figure 4.

8 A. Cutting across the device?

9 Q. Yes.

10 A. Okay. Then if you cut across the device
11 uniformly, it is still electrically isolated.

12 Q. And let's say if I did not give you the
13 cross-section information, that it's cut uniformly,
14 can you not answer the question?

15 MR. CHIU: Objection; form,
16 incomplete hypothetical.

17 A. You're saying that if you only show one
18 cross-section of a specific cut and telling me that
19 another cross-section would look different? Are you
20 saying that?

21 Q. (BY MR. MODI) I don't think I'm saying
22 that. I was just trying to --

23 A. Well, what are you saying? What's the
24 boundary condition you have here?

25 Q. I was trying to understand what you were

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2 saying. You were saying "cut across a device
3 uniformly."

4 A. Right.

5 Q. So let me ask you this way. Are you not
6 able to answer the question unless you have more
7 information about the cross-section?

8 MR. CHIU: Objection to form.

9 A. Well, you got to tell me that -- I mean,
10 in this figure, the cross-section does show that 44A
11 is electrically isolated and --

12 Q. (BY MR. MODI) How does -- I'm sorry.
13 Finish.

14 A. So based on this, one can conclude that
15 44A is electrically isolated unless you show me data
16 that's contrary to that. Are you saying that there
17 is another cross-section that shows contrary to that?

18 Q. Are you finished?

19 A. (Nods.)

20 Q. So cross-section 44A -- sorry. So the
21 figure that you're looking at, Figure 4. Right? How
22 does it tell you that it's electrically isolated?

23 A. Well, as you see, that it is surrounded by
24 insulators.

25 Q. So you're basing it on the fact that it's

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2 surrounded by insulators that it's electrically
3 isolated?

4 A. Now, are you saying that the specification
5 is not --

6 Q. Right.

7 A. -- given?

8 Q. It's not.

9 A. And what's the description of the figures?
10 Are those numbers still corresponding to the
11 interlayer dielectric field oxide insulating spacers
12 48, 42, 46a?

13 Q. Yes, sir.

14 A. And this is a cross-section of a
15 microelectronic device?

16 Q. Yes.

17 A. Yeah. If all the information you gave me
18 is this, and not showing any data that contraries to
19 that, based on this cross-section, yeah, 44A is
20 electrically isolated --

21 Q. Can I have --

22 A. -- especially --

23 Q. -- can I have you turn to --

24 MR. CHIU: Were you finished?

25 A. -- especially with, you know, knowing the

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2 description of the invention in '902.

3 Q. (BY MR. MODI) Can we go to Dennison?

4 A. Yes.

5 Q. Do you have the Dennison reference in
6 front of you?

7 A. Yes.

8 MR. CHIU: Can we take a break?

9 MR. MODI: Yes.

10 (Break.)

11 (Mr. Naples not present for the
12 rest of the deposition.)

13 MR. CHIU: And just to get on the
14 record, we've been going for seven hours, so the
15 parties have agreed that the questioning with
16 respect to the IPR 2015-1327 petition has
17 concluded, and we're moving on with IPR
18 2015-1320.

19 Q. (BY MR. MODI) Dr. Lee, can we go to
20 Dennison, please?

21 A. Yes, please.

22 Q. You have Exhibit 1007?

23 A. Yes.

24 Q. Can you please turn to Figure 1 of
25 Dennison for me.

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2 Dr. Lee, do you have Figure 1?

3 A. Yes, I do.

4 Q. So you have Figure 1 of Dennison in front
5 of you? And I believe you have the corresponding
6 page of your declaration in front of you. Is that
7 right?

8 A. Which page are you referring to?

9 Q. I think you have a specific page open,
10 don't you, from your declaration?

11 A. Okay. Sure.

12 Q. Which page do you have open?

13 A. I think I have 47. I don't know what your
14 question is. So I just opened some page.

15 Go ahead.

16 Q. Is there a reason why you went to Page 47?

17 A. I suspect that you were asking -- going to
18 ask electrically isolated. That's why.

19 Q. Do you have Figure 1 of Dennison?

20 A. Yes, I do.

21 Q. Do you agree that Dennison discloses two
22 elements marked as 20B and 20C are gate members of
23 two MOSFETs?

24 MR. CHIU: Objection; form.

25 A. Yeah. In Column 10, it says "transistor

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2 gate members 20B, 20C."

3 Q. (BY MR. MODI) And each of these gates,
4 20B and 20C, include a gate conducting layer 22 and a
5 gate insulating protective layer 28. Right?

6 A. Yeah. It's in Column -- Column 10,
7 Line 52 to 56 says that.

8 Q. And it is your understanding that a third
9 gate structure is formed just to the right of
10 gate 20B. Is that right?

11 A. That's right.

12 Q. And that the third gate structure contains
13 the same layers as gate 20B. Is that right?

14 MR. CHIU: Objection to form.

15 A. (Reviewing document.)

16 I'm saying that the third gate structure
17 and the patterned conductive layer, the first
18 patterned conductive layer, such as 20B, are formed
19 using the same set of steps, and the process is
20 formed -- performed simultaneously.

21 Q. (BY MR. MODI) Dr. Lee, I know what you
22 said in your declaration. Can you focus on my
23 question, sir?

24 MR. CHIU: Objection to form.

25 Q. (BY MR. MODI) So the question is, is it

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2 your understanding that the third gate structure
3 contains the same layers as gate 20B?

4 MR. CHIU: Objection to form.

5 A. Well, as I -- as I said, there's form
6 using the same set of steps, so, therefore, each gate
7 member is form of the same layer, the polysilicon
8 layer, tungsten silicide layer, the gate oxide
9 protective layer, and the insulating spacer members.

10 Q. (BY MR. MODI) So you agree that the third
11 gate structure also has a conductive layer 22.
12 Right?

13 MR. CHIU: Objection to form,
14 mischaracterizes the witness's testimony.

15 A. Well, it has -- the dummy structure has
16 the same polysilicon layer, which is 24, and tungsten
17 silicide layer, which is 26.

18 Q. (BY MR. MODI) Both of which are referred
19 to as the conductive layer 22. Right?

20 MR. CHIU: Objection to form.

21 A. Well, in Column 10 it only specifically
22 call out 20B and 20C that specifically call that gate
23 conductive -- conducting layer 22. And -- yeah.

24 Q. (BY MR. MODI) So --

25 A. So, yeah, 26 and 24 combined -- is that

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2 what they call 22?

3 MR. CHIU: Objection to form.

4 A. (Reviewing document.)

5 I think, based on the description of the
6 figure and the specification, that one of ordinary
7 skill in the art would understand that Dennison
8 discloses that the dummy structure, the third gate
9 comprise polysilicon gate layer, polysilicon
10 layer 24, and the tungsten silicide layer 26 because
11 it's formed using the same step as the first
12 patterned conductive layer.

13 Now, of course, the patent does not call
14 out those layer as 22.

15 Q. (BY MR. MODI) So it's your testimony
16 today that what's labeled as 22 in Figure 1 does not
17 include 24 and 26?

18 MR. CHIU: Objection;
19 mischaracterizes the witness's testimony.

20 A. In the specification, it identified 20B
21 and 20C, those two layer, as 22, and it actually does
22 not label the dummy structure.

23 Q. (BY MR. MODI) But it's your testimony,
24 right, that that third gate structure contains the
25 same layers as gate 20B?

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2 MR. CHIU: Objection;

3 mischaracterizes the witness's testimony.

4 A. Well, it was formed in the same set of
5 steps, and each member is formed of the same layers,
6 namely, 24, polysilicon, tungsten silicide, and gate
7 protective layer, 28, and insulating spacers.

8 Q. (BY MR. MODI) But you don't agree that
9 the third gate structure includes conductive
10 layer 22?

11 A. Well, if you call that 22 -- 24 plus 22 is
12 22, then, yeah, sure, that it contains 22 layers
13 also.

14 Q. Dr. Lee, you are the expert here, so I
15 want your testimony.

16 A. Okay. So if the layer 24 plus 26 -- yeah,
17 the gate conducting layer 22 comprises 24 and 26. So
18 the dummy gate has a polysilicon layer and the
19 silicide layer. So, therefore, the -- one can say
20 that, yeah, you -- that's called 22. Yes.

21 Q. Where are you -- what portion of Dennison
22 are you looking at? Can you tell me the column and
23 line numbers, please?

24 A. Well, I'm looking at Column 10.

25 Q. And what lines?

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2 A. Lines, say, 51 to 59.

3 Q. And in your opinion, those lines describe
4 the first, second, and third gate structures?

5 A. No. What I said is that on -- on Line 57,
6 it says that 22 comprises 24 and 26. Starting 20 --
7 52, it only describe the two gate members on the
8 active region, 20B and 20C.

9 Q. So do you agree that that portion does not
10 describe the third gate structure?

11 MR. CHIU: Objection; form.

12 A. Well, Line 52 specifically only talk about
13 20B and 20C and not about the dummy -- dummy layer --
14 or dummy pattern. The third gate.

15 Q. (BY MR. MODI) Can you point me to a
16 portion of Dennison which describes the third gate
17 structure?

18 MR. CHIU: Objection to form.

19 A. (Reviewing document.)

20 The specification does not explicitly call
21 out the third gate structure, but the figures and the
22 fact that it says that -- in Column 3 it says that
23 "It is well-known in the art to reduce the number of
24 mask step in the integration -- integrated circuit
25 manufacturing process not only reduces the

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2 manufacturing costs and time but generally increases
3 the quality and reliability of the end product."

4 That basically describe that the third
5 gate, the dummy gate, is formed at the same time as
6 the first patterned conductive layer.

7 Q. (BY MR. MODI) What lines are you reading
8 from?

9 A. Column 3, Lines 13 through 18.

10 Q. And would you agree that Dennison doesn't
11 actually refer at all to the third gate structure in
12 the specification? Right?

13 MR. CHIU: Objection to form.

14 A. Like I said, Dennison specification does
15 not explicitly call out and refer to the third gate
16 structure, but the figures and the specifications
17 talk -- in Column 3 that I talk about, describe and
18 discloses that the third gate, that is, the dummy
19 gate, is formed simultaneously with the first
20 patterned conductive layer.

21 Q. (BY MR. MODI) Do you -- does Dennison use
22 the terms "dummy pattern"?

23 A. You mean in the specifications?

24 Q. Let's start there.

25 A. No, it does not.

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2 Q. Does it use the words "dummy gate"?

3 A. No, it does not. It doesn't mean that
4 it's not there.

5 Q. Does it use the word "dummy"?

6 A. No, it does not. But that doesn't mean
7 it's not there.

8 Q. But you're not able to point me to any
9 other passage other than this Column 3 that supports
10 your opinion?

11 A. And the figures that support my opinion.
12 And --

13 Q. So can I have you go to your declaration,
14 on Page 46, please.

15 A. Okay.

16 Q. You have a figure on Page 46 of your
17 declaration?

18 MR. MODI: And just for the
19 record, I'm referring to Exhibit 1013.

20 Q. (BY MR. MODI) Do you see that?

21 A. Yes.

22 Q. And you see there you've annotated the
23 conductive layer in purple on Page 46 of your
24 declaration. Do you see that?

25 A. Yes.

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2 Q. And you equate it to the patterned
3 conductive layer. Is that right?

4 A. Yes.

5 Q. So that the record is clear, I'll refer to
6 that as the purple conductive layer today. Is that
7 okay?

8 A. Sure.

9 Q. Now, it is your opinion that the purple
10 conductive layer is a dummy pattern. Is that right?

11 A. Yes, that the purple conductive layer on
12 the -- of the -- of the third gate is the -- is the
13 dummy pattern.

14 Q. And it's your opinion that the purple
15 conductive layer is electrically isolated from the
16 substrate and circuits thereon. Right?

17 A. That is correct, that it -- it is
18 electrically isolated --

19 Q. Can you show me --

20 A. -- from the circuit.

21 Q. -- where in Dennison's specification it
22 causes conductive -- the purple conductive layer is
23 electrically isolated?

24 A. First of all, that the figure clearly
25 shows that it is electrically isolated, and,

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2 furthermore, in specific -- in Column 10, Line 1
3 to 3, Dennison discloses that the "wafer include an
4 array region, which include many identical cells (one
5 cell show)."

6 That means that each identical cell the
7 patterned conductive layer passes through that is
8 similar and that it is electrically isolated from the
9 substrate and circuit thereon.

10 Q. So you said figure -- the figure clearly
11 shows it's electrically isolated. What in the figure
12 shows that?

13 A. Well, the figure clearly shows that and
14 discloses that the patterned conductive layer, the
15 purple layer that you're talking about, is surrounded
16 on all sides by insulating layers: the thick field
17 oxide layer, which is highlight in blue; the
18 transistor insulating spacer, which is highlight in
19 orange on each side; and the gate insulating
20 protective layer, which highlight in green.

21 Q. So it's your opinion that the figure by
22 itself shows that it's electrically isolated?

23 MR. CHIU: Objection;
24 mischaracterizes the witness's testimony.

25 A. Well, the figure together with the

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2 specification that I told you.

3 Q. (BY MR. MODI) If I took away the portion
4 of the specification you told me, would you agree
5 that the figure supports your opinion?

6 A. No. The specification already indicate --
7 discloses that the structure is isolated everywhere.
8 And the fact that you just take out that
9 specification and change the story doesn't mean that
10 it's taking away the fact that it is electrically
11 isolated everywhere.

12 Q. So what I would want you to do is
13 everywhere that you're using to support your opinion
14 that it's electrically isolated, can we go through
15 the spec and can you identify those passages for me?
16 We can start with Column 10, Lines 1 through 3. I
17 believe that's the first one you told me.

18 And just so the record is clear, can you,
19 just for the record, read the sentence into the
20 record that you believe supports your opinion that
21 the purple conductive layer is electrically isolated?

22 A. In Column 10, Line 1 says, "Wafer 10
23 includes an array region 11, which includes many
24 identical cells (one cell shown)."

25 Q. So does that phrase use the words

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2 "electrically isolated"?

3 A. No, it does not.

4 Q. So if you have an array of cells, they
5 must be electrically isolated. Is that your opinion?

6 MR. CHIU: Objection;
7 mischaracterizes the witness's testimony.

8 A. No. I'm saying that -- first of all, the
9 figures and the figure captions that describe the
10 figures shows that the purple gate, the patterned
11 conductive layer, is surrounded all sides by
12 insulating layer -- layers.

13 Q. (BY MR. MODI) Does Column 10, Lines 1
14 through 3 --

15 MR. CHIU: Wait. Were you done?

16 A. Which are, you know, the layers that I
17 talk about. The blue layer, which is the field
18 oxide, the spacer, the orange, which is insulating,
19 and the gate protective layer 28, which is orange --
20 green. I'm sorry.

21 Q. (BY MR. MODI) So Column 10, Lines 1
22 through 3, do they refer to the third structure?

23 A. Yes.

24 Q. In what sense?

25 A. Well, it's saying that the figure shows an

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2 array, and that this array includes many identical
3 cells, and one cell shown, and that cell include the
4 third patterned layer, the dummy gate.

5 Q. Okay. What else in the specification
6 supports your electrically isolated opinion?

7 A. Well, if you look at, for example,
8 Column 7 through Column 8, Column 7, Line 7, to
9 Column 8, Line 31, it describe the process and the
10 methods of the invention, and nowhere it discloses
11 that the third gate is connected to the substrate or
12 the circuit.

13 And together with the figures, which
14 clearly discloses that the third patterned -- that
15 the patterned conductive layer, the third gate you're
16 referring to, is surrounded by insulator in all
17 sides. And together with the specification in
18 Column 10 that I was referring to, it clearly
19 discloses that the patterned conductive layer is a
20 dummy pattern electrically isolated from the
21 substrate and circuits.

22 Q. So Column 7 through Column 8, does it use
23 the word "electrically isolated" there?

24 A. No, it does not.

25 Q. Does it specifically mention the third

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2 gate structure there? Well, let me use the word that
3 you use -- explicitly mention the third gate
4 structure there?

5 A. Well, it does not explicitly mention the
6 word "third gate structure."

7 Q. What besides Column 7 through Column 8 and
8 Column 10, Lines 1 through 3, support your opinion,
9 if any?

10 A. Well, in fact, the entire specification
11 discuss the process and the methods of Dennison's,
12 and there is -- all the evidence support the fact
13 that the third -- or that the third gate, what you
14 call the third gate, the patterned conductive layer,
15 is a dummy pattern electrically isolated from the
16 circuit and the substrate.

17 Q. Dr. Lee --

18 A. And there is nowhere in the specification
19 show the contrary.

20 Q. So, Dr. Lee, I asked you for specific
21 references. Okay? So, so far you've given me
22 Column 7 to Column 8, and you've given me Column 10.
23 Can you give me any other specific references that
24 support your electrically isolated opinion?

25 A. (Reviewing document.)

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2 So, for example, in Column 11, when it
3 describe Figure 2, it talks about that using the
4 dummy pattern as a mechanical purpose for etch
5 inhibiting. And nowhere there talks about that gate
6 is connected to the substrate or the circuits.

7 Q. Dr. Lee, can I just -- so I'm following
8 you, what exactly -- what lines are you looking at in
9 Column 11?

10 A. Column 11, say, starting from 34, all the
11 way to Column 12, Line 2.

12 Q. Okay. So it's your opinion that that
13 column talks about the dummy pattern?

14 A. It talks about using that as an
15 etch-inhibiting layer.

16 Q. But you agree that it doesn't use --
17 specifically mention the third gate structure -- or
18 actually let me withdraw this.

19 Would you agree that it explicitly does
20 not mention the third gate structure?

21 A. (Reviewing document.)

22 No, it does not.

23 Q. And it doesn't use the term "electrically
24 isolated." Right?

25 A. No, it does not.

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2 Q. Okay. What else in the specification
3 supports your electrically isolated opinion?

4 A. No. Those -- those are -- I mean,
5 Figure 1 through 16 all discloses that the -- the
6 patterned conductive layer is a dummy pattern
7 electrically isolated from the substrate and circuit.

8 And in the specification, those places
9 that I told you in Column 7 and 8, and Column 11
10 and 12, and Column 10 all support that fact that the
11 arrays include many identical cells and one cell
12 shown, meaning that if each cell is -- it --

13 Q. Dr. Lee, I'm going to stop you.

14 A. Okay.

15 MR. CHIU: Wait. Hold on.

16 MR. MODI: No, no. Hold on. No,
17 no. You're not going to coach. You're not going
18 to coach. We're going to call the board.

19 MR. CHIU: All I'm saying is he
20 hasn't finished his answer.

21 MR. MODI: No, no, no. You have
22 been coaching. If you want to -- he can tell me.
23 No, no, no.

24 MR. CHIU: How have I been
25 coaching him?

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2 MR. MODI: You have been coaching
3 him, so please stop.

4 MR. CHIU: I'm just saying let him
5 finish his answer.

6 MR. MODI: Let me talk to the
7 witness.

8 Q. (BY MR. MODI) So, Dr. Lee, I do not want
9 you to review --

10 A. I am not finished.

11 Q. Your attorney --

12 MR. CHIU: I am not coaching
13 anything. I'm just telling -- asking you to
14 allow the witness to finish the answer.

15 MR. MODI: Okay. I will allow him
16 to finish the answer.

17 Q. (BY MR. MODI) Okay. But let me ask you a
18 question, Dr. Lee. My question was very simple.
19 Okay? I asked you what else in the specification
20 supports your electrically isolated opinion.

21 A. That's it.

22 Q. That was my question.

23 A. Yeah. So that's it.

24 Q. So just to be clear, because I want to
25 make sure the board knows what your opinions are.

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2 Okay? So you said Columns 7 through 8. Yes?
3 Columns 11 through 12, and Column 10. That's it.
4 Right? Those are the portions of the specification
5 that support your electrically isolated opinion. Yes
6 or no?

7 A. Sir, you don't have to scream.

8 Q. I'm not screaming.

9 MR. CHIU: Yeah, counsel, I'd
10 appreciate it if you'd lower your voice. You're
11 harassing the witness.

12 MR. MODI: I disagree.

13 Q. (BY MR. MODI) Would you answer my
14 question?

15 THE WITNESS: May I take a break?
16 I cannot take this.

17 MR. CHIU: Agreed? Take a break?

18 MR. MODI: Well, a question is
19 pending. So he needs to answer my question
20 before he takes a break.

21 MR. CHIU: Why don't you just
22 answer the question?

23 THE WITNESS: Okay.

24 A. Yes, those are the places in the
25 specification that I refer to that support my

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2 opinion, together with the figures.

3 Q. (BY MR. MODI) Is there anything else in
4 the specification that supports your electrically
5 isolated opinion other than Column 7 to 8, Column 10,
6 and 11 to 12?

7 A. Like I said, in fact, all the
8 specification describe the process, and nowhere in
9 the description describe that the patterned
10 conductive layer on the third gate is electrically
11 connected to the substrate and the circuit. Unless
12 you can show me any place contrary to that, all the
13 supporting data and the figures support the fact that
14 the pattern is a dummy pattern electrically isolated
15 from the substrate and the circuits.

16 Q. Dr. Lee, this will go much more quickly if
17 you answer -- if you focus on my question and answer
18 the question, please. I have been asking you for the
19 last 15, 20 minutes to point me to the specific
20 passages in the specification that support your
21 electrically isolated opinion. Would you list them
22 for me?

23 MR. CHIU: Objection; asked and
24 answered.

25 A. If you look at Column 12, for example --

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2 Q. (BY MR. MODI) Dr. Lee, please, if you
3 would listen to my question. I asked you to list. I
4 just want a list, and then we will discuss them.

5 MR. CHIU: He's about to give you
6 a specific passage. I don't understand what the
7 issue is, counsel.

8 Q. (BY MR. MODI) I want you to list all the
9 different passages in the specification. Just a
10 list. I want it by column and line number. That is
11 all I want right now.

12 MR. CHIU: He started giving you a
13 column, "if you look at Column 12, for example,"
14 and then you just cut him off.

15 MR. MODI: Are you going to stop
16 this or no?

17 MR. CHIU: I'm just telling you,
18 you got to let him answer the question. He was
19 answering the question.

20 MR. MODI: I have been very
21 patient with you over the last two days. I will
22 ask you to please stop your coaching objections.
23 Okay?

24 MR. CHIU: Okay. If you want go
25 to the PTAB with this, "if you look at Column 12,

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2 for example," and then you cut him off, and now
3 you're saying, "I want a list of all the specific
4 passages." Okay. Well...

5 MR. MODI: Are you done?

6 MR. CHIU: I'm done. I ask you to
7 just let him answer the question.

8 MR. MODI: Okay.

9 Q. (BY MR. MODI) Dr. Lee, if you would, let
10 me withdraw my last question. If you would please
11 focus on my question, I promise you this will go much
12 more quickly.

13 All I want you to do is give me, by column
14 and line number, that's all I want, is a list that
15 supports your electrically isolated opinion.

16 MR. CHIU: Objection to form.

17 A. Column 12, Line 3 to Column 14, Line 26,
18 which describe the process.

19 Q. (BY MR. MODI) Anything else?

20 A. That's it.

21 Q. So sitting here today, it's your testimony
22 that Column 12 through 14 is what supports your
23 electrically isolated opinion?

24 A. In addition to all the other ones that I
25 told you.

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2 Q. Let's go through them again. I want to
3 make sure. Because every time I ask you a question,
4 you add one. So let's make sure I have all of them.

5 A. Okay. Column --

6 MR. CHIU: Objection; asked and
7 answered.

8 A. -- Column 7.

9 Q. (BY MR. MODI) What line?

10 A. Line 8, to Column 8, Line 40. Column 10.
11 Well, Column 9, Lines 62, to Column 10, Line 40. In
12 particular, Column 10, Line 1 to 3. Column 11,
13 Line 34, to Column 14, Line 26.

14 Q. Are you done? Is that your list?

15 A. Yes.

16 Q. And you agree that in that list that
17 you've given me, nowhere does it refer to the third
18 gate structure explicitly. Right?

19 MR. CHIU: Objection to form.

20 A. That is correct.

21 Q. (BY MR. MODI) And nowhere in these
22 passages does it use the words "electrically
23 isolated." Correct?

24 MR. CHIU: Objection; form.

25 A. That is -- that is correct. However, like

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2 I said, in -- for example, in Column 10, it says that
3 the -- many identical cells, and furthermore, nowhere
4 in these passages discloses that the patterned
5 conductive layer is connected to the substrate or the
6 circuits.

7 Q. (BY MR. MODI) And nowhere in these
8 passages does it use the words "dummy."

9 A. No. Nowhere -- that is correct. However,
10 that doesn't mean that they're not dummy gate.

11 Q. Is every electrical -- electrically
12 isolated gate stack a dummy pattern?

13 MR. CHIU: Objection; form, lacks
14 foundation.

15 A. Well, I can tell you that the purple gate
16 that we're referring to, that is electrically
17 isolated, and that one knows that when the gate
18 are -- the patterned conductive layer are
19 electrically isolated and, therefore, will play no
20 electrical function in the operations of the
21 circuits. In this case, the memory cell.

22 Q. (BY MR. MODI) Where are you reading from,
23 Dr. Lee?

24 A. No, I'm just telling you.

25 Q. I thought you were looking at your

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2 declaration.

3 A. No. No. I was looking down.

4 Q. So when you have many identical cells, is
5 it your opinion that it must be electrically
6 isolated?

7 MR. CHIU: Objection; form.

8 A. Well, if one cell shows that the
9 conductive layer is electrically isolated, and that
10 all the cells are identical, and that cell is shown,
11 then obviously that patterned conductive layer is
12 electrically isolated.

13 Q. (BY MR. MODI) So can you go to Column 10,
14 Lines 1 through 3, and show me where it says that one
15 cell is electrically isolated?

16 A. No. It says that --

17 MR. CHIU: Objection;
18 argumentative.

19 A. -- Wafer 10 includes an array region,
20 includes many identical cell, one cell shown. It
21 does not say that it is electrically isolated. But
22 the figure does.

23 Q. (BY MR. MODI) And what does one cell
24 have?

25 A. Well, the one cell has a purple gate, as

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2 shown in Figure 1, which is surrounded by insulator
3 on all sides.

4 Q. Anything else?

5 A. Anything else for what?

6 Q. The cell. What else does a cell have?

7 A. Well, it has 20B, 20C. It has the
8 substrate, it has the capacitors, it has a bit line
9 contract, it has a word line contact, so on and so
10 forth.

11 Q. Let me ask you, if a cross-section shows a
12 conductive layer as being surrounded by insulative
13 layers, can the conducting layer have an electrical
14 function?

15 MR. CHIU: Objection; lacks
16 foundation.

17 A. Wait. Let me understand your question.
18 You're saying that a conductive layer is being
19 surrounded by insulator in all sides?

20 Q. (BY MR. MODI) Yes.

21 A. Completely surrounded by insulator?

22 Q. It's surrounded as, let's say, it's shown
23 in Figure 1.

24 A. And also supported by the spec?

25 Q. No. All I'm saying is all -- if all you

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2 had is a cross-section that shows a conductive layer
3 being surrounded by insulative layers, as in
4 Figure 1, can the conductive layer have an electrical
5 function?

6 A. Well, Figure 1 of Dennison says more
7 information than just showing in the Figure 1.
8 Right? It also described in the specification, which
9 clearly shows that it's completely surrounded by an
10 insulator, so there is no electrical function.

11 Q. When you say it's "completely surrounded
12 by insulator," what do you mean by that?

13 A. It's a three-dimensional device. Right?
14 It says that all the cell looks identical and it is
15 all -- in other words, that the purple gate is always
16 surrounded by insulator.

17 Q. How do you get to that completely
18 surrounded in Dennison? Does Figure 1 show that?

19 A. Figure 1 shows that it is not connected to
20 the substrate or the circuits. The purple gate is
21 not connected to the substrate or the circuits.

22 Q. Does Figure 1 show that it is completely
23 surrounded by an insulator?

24 MR. CHIU: Objection; form.

25 A. Well, Figure 1 shows that -- and the

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2 specification shows that 20B and 20C are specifically
3 called out by Dennison that those are the word lines,
4 and the cells repeated, and they are identical.

5 In other words, that the purple gate are
6 surrounded by an insulator and is isolated from the
7 substrate and the circuit.

8 In other words, that this cross-section is
9 representative of all cross-sections. So, therefore,
10 that it is always isolated, electrically isolated.

11 Q. (BY MR. MODI) So, Dr. Lee, does Dennison
12 show a plan view of Figure 1?

13 A. No, it does not.

14 Q. Do you need a plan view?

15 MR. CHIU: Objection; form.

16 A. To do what?

17 Q. (BY MR. MODI) To determine whether it's
18 completely surrounded by an insulator.

19 MR. CHIU: Objection to form.

20 A. What is "it"?

21 Q. (BY MR. MODI) The purple layer.

22 MR. CHIU: Objection to form.

23 A. You don't need a plan view because the
24 specifications, together with the figure, clearly
25 discloses that the purple gate is a dummy layer or

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2 dummy pattern electrically isolated from the
3 substrate and circuit.

4 Q. (BY MR. MODI) Okay. And just so that I
5 have your testimony -- so I understand it, when
6 you're referring to the electrically isolated, you're
7 referring to the passages of the specification that
8 you identified earlier. Is that right?

9 A. Yes. All the specification I talk about.

10 Q. Okay. Let me --

11 A. The plan view -- in this case the
12 specification, together with the figures alone,
13 already discloses that the purple gate is a dummy
14 layer electrically isolated from the substrate and
15 circuit.

16 Now, if there is a plan view, which
17 shows -- well, let me stop there.

18 Q. When we talk about -- I think in your
19 declaration you refer to electrical function and
20 electrical isolation?

21 A. Yes.

22 Q. Are you ascribing any differences between
23 them?

24 A. Well, if a patterned conductive layer is
25 electrically isolated from the circuit and the

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2 substrate, then one can conclude that that does
3 not -- that conductive layer does not perform any
4 electrical function. Okay?

5 Now, some pattern may be formed on the
6 substrate, so it's not electrically isolated from the
7 substrate, but if the circuit is designed in such a
8 way that that does not perform any function, it can
9 still -- a layer that is not perform any electrical
10 function. So that's the distinction.

11 Q. So just so I understand, so not having an
12 electrical function is the same as electrically
13 isolated?

14 MR. CHIU: Objection;
15 mischaracterizes the witness's testimony.

16 A. No. I'm saying that all pattern that are
17 electrically isolated are electrically isolated and
18 perform no electrical function. But not all pattern
19 that perform no electrical function are electrically
20 isolated.

21 MR. CHIU: Good time to take a
22 break at any time?

23 THE WITNESS: Yes, please.

24 MR. MODI: Let me just finish with
25 this line of questioning.

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2 Q. (BY MR. MODI) Dr. Lee, just -- I'm not
3 sure we -- can you say that one more time just to
4 make sure I understand it.

5 A. All patterns that are electrically
6 isolated would perform no electrical function. But
7 patterns that are not electrically isolated can still
8 perform no electrical function. In other words, you
9 could design a circuit and put a structure on the
10 substrate in such a way that it doesn't perform any
11 electrical function.

12 Q. And you would say in that sense, in that
13 case, the circuit is not electrically isolated?

14 A. That layer is not electrically isolated.

15 MR. MODI: Why don't we take a
16 break now.

17 THE WITNESS: Okay.

18 (Break.)

19 Q. (BY MR. MODI) Dr. Lee, did you talk with
20 your attorney about the substance of your testimony
21 during the break?

22 A. No.

23 Q. Do you have Dennison in front of you?

24 A. Yes.

25 Q. Can you look at Figure 1 for me.

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2 A. Yes. I'm here.

3 Q. Would you agree that for the structure of
4 Figure 1 to be operational, gate 20B must receive an
5 input signal to turn the gate on or off?

6 A. Yes.

7 Q. Would that input signal come from a gate
8 contact to the conductive layer 22?

9 A. Well, there are multiple contacts. Right?
10 There's a contact to the gate and a contact to the
11 source and drain.

12 Q. Are you finished, Dr. Lee?

13 A. Yes.

14 Q. So you said there are multiple contacts?

15 A. Right. You're saying that in order to
16 receive any signal, you only contact to the gate.
17 I'm saying that, well, the transistor three terminals
18 device, that all three terminals are connected to the
19 rest of the circuit.

20 Q. So let's -- just for purposes of my
21 questioning, let's focus on the gate contact.

22 A. Okay.

23 Q. Does Dennison disclose a gate contact for
24 conductive layer 22?

25 MR. CHIU: Objection; form.

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2 A. Not explicitly.

3 Q. (BY MR. MODI) Are you finished?

4 A. Yeah.

5 Q. So when you say "not explicitly," what
6 about implicitly?

7 MR. CHIU: Objection to form.

8 A. I think implicitly a person of ordinary
9 skill in the art would know that the contact to the
10 gate is a contact to the gate from the metal word
11 line directly to the gate member, 20B, in the active
12 region.

13 Q. (BY MR. MODI) So such a gate contact for
14 20B would be from the metal layer -- or from a metal
15 layer to conductive layer 22?

16 A. Yes, at the gate contact from the metal
17 layer to the layer 26, which is a silicide, and 24,
18 poly gate. So basically to 22 in the active region.

19 Q. Is it your testimony that Dennison does
20 not explicitly disclose a gate contact for conductive
21 layer 22?

22 MR. CHIU: Objection; form.

23 A. For the transistor 20B? Is that what
24 you're saying?

25 Q. (BY MR. MODI) Yes.

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2 A. Yes, not explicitly, but implicitly
3 that -- from the specifications and the knowledge of
4 the person of ordinary skill in the art at the time
5 of the filing date of Dennison '677 would understand
6 that the gate contact to the conductive layer 22 in
7 transistor gate 20B is from the metal gate directly
8 to 22 in the active region.

9 Q. So where will the contact be?

10 A. The contact will be from the metal line,
11 the word line, to the gate member 20B.

12 Q. And would it be in the active region or
13 outside the active region?

14 A. No. I said in the active region.

15 Q. And what's the basis for that testimony?

16 A. Well, if you look at Column 7, starting
17 from Line 8, through Column 8, Line 31, okay, it
18 describe the methods of fabricating contacts and the
19 process of fabricating the device, and in Line 12 it
20 says "a plurality of transistor gate member, one on
21 either side of the active region" -- "active area, a
22 transistor insulating spacer member between
23 transistor gate members and the active area." Okay?

24 And it also further describe, using the
25 same language, down in -- on Line 64, "the plurality

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2 of transistor gate member, one on either side of the
3 active area, a transistor insulating spacer member
4 between each of the transistor gate member and the
5 active area." Okay? In other words, that the spacer
6 is formed between each of the gate members and the
7 active area.

8 So, in other words, that in order for that
9 to happen, that the gate does not crosses over and --
10 does not touch and crosses over to the field region.
11 So, therefore, the only conclusion that one can make
12 is that the contact to the gate members 22 has to be
13 from the gate contact from the metal, metal 1, to the
14 gate conductive layer 26 in the active region.

15 Q. So is it your testimony sitting here today
16 that Dennison does not disclose a gate contact for
17 conductive layer 22 outside the active region?

18 A. Yes.

19 Q. So based on your review of Dennison,
20 Dr. Lee -- I just want to make sure that -- you
21 reviewed the entirety of Dennison. Right? And it's
22 your opinion that Dennison does not disclose a gate
23 contact for conductive layer 22 outside the active
24 region?

25 A. Conductive layer of 20B, yes.

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2 Q. So you mentioned you limited your answer
3 to conductive layer 20B. Are there any other
4 transistors that have conductive layer 22?

5 A. What I'm saying is that this is refer --
6 my answer is referring to the memory core. Okay?
7 Memory portion of the DRAM chip. There is also a
8 peripheral portion, and what's happening there is how
9 the contacts are formed to the gate could be a
10 different story. Okay?

11 But the contact to the gate members within
12 the memory core, memory portion, basically is a
13 contact to the -- from the metal one to the gate
14 member in the active region.

15 Q. What about the memory -- the peripheral
16 portion?

17 A. The peripheral portion is a logic circuit,
18 and that could -- that could have different design.
19 But in this case, it's talk about the DRAM cell, how
20 the DRAM cells are formed, and the figure shows that
21 the gate member, the first patterned layer in the
22 active region, does not crosses over the field
23 region, and the specification also support that. And
24 so, therefore, the contact to the gate has to be in
25 the active region.

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2 Q. So you said that the figure shows that the
3 gate member -- what gate are you referring to in your
4 last answer?

5 A. All the figures in the Dennison patent
6 related to the memory portion. So Figure 1, for
7 example, Figure 2, Figure 3, Figure 4, Figure 5,
8 Figure 6(a), Figure 6(b), and so on and so forth.

9 Q. And you say here the first pattern in the
10 activation does not cross over the field region?
11 What's your basis for saying that?

12 A. Well, the figure shows that the first
13 patterned layer on the active region does not cross
14 over the field region. In other words, it's spaced
15 apart from the field region.

16 Q. Where does it show that?

17 A. The figures.

18 Q. Which figure?

19 A. Figure 1, for example, and all the other
20 figures in -- for the memory portion.

21 Q. So just from looking at Figure 1, you can
22 tell us that it's spaced apart?

23 MR. CHIU: Objection; form.

24 A. Well, from the -- all the evidence and all
25 the figures in Dennison's discloses that the first

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2 patterned layer in the active region is spaced apart
3 from the field region and that Dennison does not
4 disclose any evidence contrary to that. Furthermore,
5 the specification that I quoted just now further
6 support that the first patterned layer on the active
7 region is spaced apart from the field region.

8 Q. (BY MR. MODI) So, Dr. Lee, I want to
9 break that down to make sure I understand it. Okay?
10 And I want you to just give me a list again so we
11 don't go back and forth like we have in the morning
12 to try to speed this up.

13 So if you can just give me a list -- let's
14 start with the figures. If you can give me a list of
15 the figures that support your opinion that Dennison
16 discloses that the first patterned layer is spaced
17 apart from the field region.

18 MR. CHIU: Objection; form.

19 A. All right. Figure 1, Figure 2, Figure 3,
20 Figure 4, Figure 5, Figure 6(a), Figure 6(b),
21 Figure 9, Figure 11, Figure 12, Figure 13, Figure 14.

22 So those are the figures.

23 Q. (BY MR. MODI) Do any of these figures
24 show your plan view?

25 A. No.

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2 Q. Now, can you go to the specification and
3 point me to where in the specification -- again, I'm
4 just looking for a list -- that supports your opinion
5 that Dennison discloses that the first patterned
6 layer is spaced apart from the field region?

7 A. Okay. Specifically in Column 7, Line 8,
8 to Column 8, Line 40, it describes the method of
9 fabricating the DRAM memory cell. And nowhere there
10 discloses that the first patterned layer crosses over
11 to the field region. Furthermore, on Line 14 to 15
12 and on Line 66 to 68 states that "a transistor
13 insulating spacer member between the transistor gate
14 members and the active area."

15 Q. Dr. Lee, I asked you for a list.

16 A. Yes, that's it.

17 Q. Okay. Does gate 20B have conductive layer
18 22?

19 A. Yes. 22 comprises 24 and 26.

20 Q. And conductive layer 22 has a polysilicon
21 layer?

22 A. Yes. 24 is a polysilicon layer.

23 Q. So if we're talking about the gate contact
24 to 22 -- let me withdraw that.

25 So if we're talking about the gate

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2 contact to 22, you will make the contact from
3 metal to polysilicon layer 22. Right?

4 Let me withdraw that and --

5 (Discussion off the written
6 record.)

7 Q. (BY MR. MODI) So if you have to make a
8 gate contact to 22, you will make a contact from
9 metal to polysilicon layer of 22. Correct?

10 A. No.

11 Q. Why not?

12 A. Because on top of the polysilicon layer,
13 which is 24, there is a tungsten silicide layer,
14 which is 26. So you actually make a contact to 26.

15 Q. Is that always the case?

16 A. We're talking about the memory core
17 portion. Right?

18 Q. (Nods.)

19 A. Yes. That is, if you contact metal 1
20 to -- it's tungsten silicide, which is part of the
21 gate member, the first patterned layer on the active
22 region.

23 Q. Will the gate contact be a metal-to-poly
24 contact?

25 A. No.

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2 Q. Why not?

3 A. Again, on top of the poly, there's a
4 tungsten silicide. So it's actually contact to the
5 silicide, metal-to-silicide contact.

6 Q. And that's Item 26?

7 A. Yes.

8 Q. Is silicide a metal?

9 MR. CHIU: Objection to form,
10 beyond the scope of Dr. Lee's declaration.

11 A. Silicide -- tungsten silicide comprises a
12 metal, tungsten.

13 Q. (BY MR. MODI) So earlier you said -- you
14 gave me a number of figures that you said support
15 your opinion that the first patterned conductive
16 layer is spaced apart from the field region. Do you
17 remember that?

18 A. Yeah. Those figures -- the list of
19 figures discloses that the first patterned layer on
20 the active region of the substrate spaced apart from
21 the field region.

22 Q. So would you agree that those figures by
23 themselves disclose that?

24 A. All the figures discloses that -- all the
25 figures disclose that the -- let me start over.

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2 All the figures that I pointed out earlier
3 disclose that the first patterned layer on the active
4 region of the substrate is spaced apart from the
5 field region, and that Column 7, Line 8, to Column 8,
6 Line 40, disclose the methods of fabrications, and
7 nowhere there or any other place in the
8 specifications disclose anything contrary to that.

9 Q. Dr. Lee, my question is simple. If you
10 were to just look at the figures, do they support
11 your opinion that the first patterned layer is spaced
12 apart from the field region?

13 MR. CHIU: Objection to form.

14 A. Yes. The figures support my opinion --

15 Q. (BY MR. MODI) Without more?

16 A. -- that the first patterned layer is
17 spaced apart from the field region.

18 Q. So the figures by themselves support your
19 opinion?

20 MR. CHIU: Objection; form.

21 A. Yeah, the figures themselves support my
22 opinion.

23 MR. MODI: Okay. Why don't we
24 take --

25 A. But there are other supports.

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MR. MODI: Why don't we take a break?

THE WITNESS: Okay.

(Break.)

Q. (BY MR. MODI) Dr. Lee, earlier we talked about Column 7.

A. Yes.

Q. Do you remember that?

A. Yes.

Q. Can you show me in any of the figures where the transistor insulating spacer member between the transistor gate members and the active area is located?

MR. CHIU: Objection to form.

A. Well, for example, in Figure 1.

Q. Can you explain that to us, please?

A. Transistor gate member -- transistor insulating -- let me start over.

A transistor insulating spacer member, it's No. 19 in Figure 1, between transistor gate members, which is 26 and 24, and the active area, which is 12, and is highlighted in yellow on Page 44 of my declaration.

Q. Can I have you go to Column 11 for me?

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2 A. Yes.

3 Q. And can you look at starting around
4 Line 64 to 66?

5 A. 64?

6 Q. To about 66. And you can read if you need
7 more context around that.

8 A. This is related to Figure 7. Is that what
9 you mean?

10 Q. Yes. Why don't you just read it, look at
11 that portion, and let me know when you're done.

12 A. (Reviewing document.)

13 Okay.

14 Q. Do you agree that based on what you read
15 in Column 11, Dennison discloses that a gate contact
16 to the conducting layer 22 will be formed in
17 region 38?

18 A. Region 38.

19 The lines that you quoted is talking about
20 Figure 7, which is contact to the cell poly. Is that
21 what you're talking about?

22 Q. Dr. Lee, if you could just answer my
23 question, I would appreciate it.

24 Based on the disclosure in Column 11, does
25 Dennison disclose that a gate contact to the

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2 conducting layer 22 will be formed in region 38?

3 A. Yeah, but region 38 are referring to the
4 peripheral circuits.

5 Q. So can you answer my question?

6 A. Are you saying contact to layer 22 of the
7 transistor member 20B?

8 Q. Yes.

9 A. No, I don't think so.

10 Q. So then what does this disclosure teach
11 you?

12 A. I believe this is talking about the
13 peripheral circuit. 38 is about the peripheral
14 portions of the DRAM chip, not the memory portion of
15 the DRAM chip.

16 Q. So would you agree that the peripheral
17 circuits you're talking about include conductive
18 layer 22?

19 A. Yeah, because all the gates are fabricated
20 at the same time. Yeah. The -- 22 -- the gate 22
21 not only in the memory portion, but also in the
22 peripheral portion for performing logic circuits in
23 the peripheral circuit.

24 Q. What does a peripheral circuit do in
25 Dennison?

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2 A. Well, peripheral circuits control the flow
3 of information in and out of the memory -- of the
4 DRAM memory portion. And it could also perform some
5 other function, but mainly it's controlling the flow
6 of information, putting in the DRAM memory portion
7 and taking out the memory portion information or
8 controlling the refresh cycles.

9 Q. Where is that disclosed in Dennison?

10 A. It's common knowledge.

11 Q. Is there explicit disclosure of that in
12 Dennison?

13 A. (Reviewing document.)

14 Right. You know how a DRAM work. Right?
15 DRAM chips have a memory portion and a peripheral
16 portion. A person of ordinary skill in the art would
17 know that the memory portion contains the memory, but
18 the peripheral portion, one of the functions is to
19 communicate the stored memory data to the external
20 world. And that's what the memory peripheral portion
21 is function -- functioning for.

22 And let me see. I mean, this is so basic,
23 I'm not sure if they even talk about this in the --
24 in the patent itself.

25 Q. So, Dr. Lee, let me ask you this. Does

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/26/16

2 the disclosure in Column 11 discuss a gate contact
3 for conductive layer 22?

4 A. Yes, but it is in the peripheral portion.

5 Q. Does -- and where is that shown in any of
6 the figures, conductive layer 22 for the peripheral
7 portion?

8 A. Well, if you look at Figure 2, for
9 example, the region 38 is only in the peripheral
10 portion.

11 Q. And conductive layer 22 is shown in the
12 memory core portion. Right?

13 A. Right. But the gates, right, as we
14 mentioned for Claim 4, all the gates are formed
15 simultaneously, including those in the memory
16 portion, as well as in peripheral portion.

17 Q. So are you saying that the conductive
18 layer, which is contacted in 38, is not present in
19 gate 20B?

20 MR. CHIU: Objection to form,
21 mischaracterizes the witness's testimony.

22 A. I'm not saying that. I'm saying that 22,
23 not only are the gate materials, which is poly and
24 tungsten silicide, not only are used in the memory
25 portion, but also are used in the peripheral portion,

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2 which you call that 22, is a combination of 24 and
3 26.

4 Q. (BY MR. MODI) So do you disagree with my
5 question?

6 MR. CHIU: Objection to form.

7 A. You say -- let me read your question. So
8 you are saying that the conductive layer, which is
9 contacted in 28.

10 Q. (BY MR. MODI) In 38.

11 A. I'm sorry.

12 Q. Actually, why don't I re-ask my question?

13 A. Yes, please.

14 Q. If you can give me a yes or no. Do you
15 agree that conductive layer 22, which is contacted in
16 38, is not present in gate 20B?

17 MR. CHIU: Objection to form.

18 Q. (BY MR. MODI) Yes or no?

19 A. No, I disagree. 22 -- the conductive
20 layer 22 is in both the memory core area and the
21 peripheral area. So I disagree.

22 Q. Where does Dennison teach that it has
23 conductive layer 22 in the periphery region?

24 A. Well, I have to take some time to look for
25 it. But as I mentioned, related to Claim 4. Okay.

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2 Let me show you. That in Column 3, Line 13 to 18 it
3 says, "It is well-known in the art that reducing the
4 number of mask steps in the integration" --
5 "integrated circuits manufacturing process not only
6 reduces manufacturing costs and time but also
7 generally increases the quality and reliability of
8 the end product..."

9 So, therefore, it is well-known, and the
10 only design choice that would be practical, from a
11 manufacturing standpoint, to form all the gates
12 simultaneously, instead of forming gates in different
13 process with different masks.

14 So the gates that are formed in the
15 periphery would be the -- at the same time with the
16 gates that are formed in the memory core. So,
17 therefore, the 22 -- gate conductive layer 22 would
18 also be in the peripheral circuit.

19 Now, it might have described somewhere
20 specifically in the -- in the specification.

21 But if you want me to spend some time and
22 look for it, I could, but I don't -- you know, it's
23 very clear to a person of ordinary skill in the art
24 that all the gates are formed simultaneously.

25 MR. MODI: Let's take a break.

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2 (Break.)

3 Q. (BY MR. MODI) So, Dr. Lee, you were
4 saying that separate gates 20B exist in the memory
5 area and the peripheral area. Right?

6 A. No. 22. I'm saying gate 22. 20B has a
7 special meaning. Okay? I'm saying that the
8 similar -- a same set of steps are used to form
9 identical structure in the periphery as in the memory
10 portion of the chip.

11 Q. So you're saying that gate 22 is formed in
12 the memory area and the peripheral area?

13 A. Well, I'm saying that each gate member on
14 the chip, including the memory portion and the
15 peripheral portion, the gate in the active area of
16 the memory portion, and the dummy gate on the field
17 region are formed using the same set of steps; that
18 each gate member is formed of polysilicon layer 24,
19 tungsten silicide layer 26, and the insulating
20 protective layer 28 and insulating spacer member 19.

21 Q. So let me ask you this. So would you
22 agree that separate gates exist in the memory area
23 and the peripheral area?

24 MR. CHIU: Objection; form.

25 A. What do you mean by "separate gates"?

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2 Q. (BY MR. MODI) Do gates exist in the
3 memory area?

4 A. Yes.

5 Q. Do gates exist in the peripheral area?

6 A. Yes.

7 Q. For the gate in the memory area, which is
8 20B -- okay? Do you agree?

9 So let me ask you this. Is gate 20B in
10 the memory area?

11 A. It's in the active region of the memory
12 area, yes.

13 Q. And that's shown in Figure 1?

14 A. Yes.

15 Q. For that particular gate 20B, the gate
16 contact is not shown?

17 A. Not in the figures.

18 Q. But for the gate in the peripheral area,
19 the gate contact is shown?

20 A. Yes.

21 Q. And you would agree that there are
22 different transistors in the peripheral area and
23 memory area?

24 A. What do you mean by "different"?

25 Q. Are the transistors the same?

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2 A. They're made and formed using the same set
3 of steps and consist of same set of layers.

4 I don't know what you mean by "different."
5 I mean, obviously they're not one transistor.

6 Q. So let me ask you this way. Do you
7 consider 20B and 20C to be different transistors?

8 A. Can you define "different"? It's two
9 separate transistor.

10 Q. Okay. That's fine. Let's go with
11 separate.

12 A. Yeah, it's two separate transistor.

13 Q. Okay. So are there separate transistors
14 in the peripheral area and memory area?

15 A. There are thousands of transistors.
16 Billions of transistors. Is that what you mean?
17 Yeah, of course they're separate.

18 Q. And there's some for the memory area and
19 some for the peripheral area?

20 A. Not just some. Many. Billions. On the
21 memory area and one -- and many in the peripheral
22 area.

23 Q. Does a gate 20B from memory area extend to
24 the peripheral area?

25 MR. CHIU: Objection; form.

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2 A. As I described earlier, the first gate --
3 let me see -- show you the -- the first patterned
4 layer is spaced apart from the field region, so it
5 does not extend or touch or crosses over to the field
6 region, and therefore it does not extend to the
7 peripheral region.

8 Q. (BY MR. MODI) So the answer is no to my
9 question, Dr. Lee?

10 MR. CHIU: Objection to form.

11 A. The gate member does not extend to the
12 peripheral area, no. The gate member itself doesn't
13 extend to the peripheral circuit.

14 Q. (BY MR. MODI) What about the conductive
15 layer 22 of the gate member?

16 MR. CHIU: Objection to form.

17 A. No, it does not. Again, I show you that
18 the gate member, the first patterned layer on the
19 active region of the substrate, is spaced apart from
20 the field region as shown in the figures and
21 illustrated in the specifications and supported by
22 the specification.

23 Q. (BY MR. MODI) Is 38 in the peripheral
24 area?

25 A. Yes.

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2 MR. MODI: Let's take a two-minute
3 break.

4 (Break.)

5 MR. MODI: Dr. Lee, thank you for
6 your time. We have no further questions.

7 MR. CHIU: Take a break.

8 (Break.)

9 EXAMINATION

10 BY MR. CHIU:

11 Q. Dr. Lee, do you recall testifying
12 yesterday about draft petitions?

13 A. Yes.

14 Q. Did you want to clarify your testimony on
15 the draft petition?

16 MR. MODI: Objection; leading.

17 A. Yes. During the course of preparing the
18 declaration, I did not and had not seen a draft of
19 petition.

20 Q. (BY MR. CHIU) And when is the first time
21 that you saw any copy of the petition with a draft or
22 a final copy?

23 MR. MODI: Objection; form.

24 A. Early this week. On Tuesday.

25 Q. (BY MR. CHIU) And do you recall

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2 testifying earlier about the Lee reference with
3 respect to the gate cap and the cap oxide?

4 A. Yes.

5 Q. And did you have a clarification you
6 wanted to make about the gate cap and the cap oxide?

7 MR. MODI: Objection; leading.

8 A. Yes. Figure 5 of the Lee reference
9 indicating that there's a layer of cap oxide layer,
10 and it's used as a mask during the etching of the
11 semiconductor substrate. And that the Figure 3 and 4
12 all says that the layer contain the gate oxide, poly
13 and gate cap, and all the figures are drawn the same
14 in terms of the gate stack, and the way that Lee sets
15 up discloses that the gate of the same formation.
16 So, therefore, it is my opinion that each gate
17 actually consists of the gate oxide layer, the poly
18 layer, the gate cap, and the cap oxide layer.

19 And the reason why Figure 5 specifically
20 talk about cap oxide layer is that it needs to use
21 that to do the etching of the oxide.

22 So, therefore, actually either that the
23 cap oxide --

24 MR. MODI: Hold on one second,
25 Dr. Lee.

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2 THE WITNESS: Yeah.

3 MR. MODI: You are modifying an
4 exhibit. Please identify for the record what
5 you're doing.

6 THE WITNESS: Oh, I want to
7 clarify my point on the exhibit of 2004 that the
8 Figure 4 and Figure 3 in that figure would have a
9 additional layer or that the layer -- the upper
10 layer actually consists of both a cap layer --
11 cap oxide layer and the gate cap.

12 MR. CHIU: No further questions.

13 (Break.)

14 EXAMINATION

15 BY MR. MODI:

16 Q. Dr. Lee, after I finished my examination,
17 did you talk to your attorney about your testimony?

18 A. He told -- he asked me what I want to
19 clarify, and I told him that I want to clarify these
20 two things: the petitions and this Figure 5 of Lee
21 and Figure 4 of Lee.

22 Q. Okay. And did you discuss anything else?

23 A. No.

24 Q. And did you discuss what exactly you were
25 going to clarify?

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2 A. Well, I told him that I need to clarify
3 what -- the petition, and -- and that's it. And
4 that --

5 Q. And you were in the room with your
6 attorney for about nine minutes. Is that right?

7 A. I don't know. I didn't -- I didn't count.

8 Q. So it took you nine minutes to discuss
9 that with your attorney, sir?

10 MR. CHIU: Objection;
11 argumentative, harassing the witness.

12 A. Well, we kept asking each other, "Anything
13 else?" And we keep thinking and want to make sure
14 that we have -- did not leave anything out, and so we
15 just keep thinking and looking at -- thinking of what
16 I have said the last two days and see if there's
17 anything else. So we want to be thorough, so we sit
18 there and keep thinking about it.

19 Q. (BY MR. MODI) So you had a discussion in
20 terms of what to clarify. Is that fair?

21 MR. CHIU: Objection;
22 mischaracterizes the witness's testimony.

23 A. No. I said that we -- I'd like to clarify
24 two things, the petition and the gate cap and cap
25 oxide layer in Lee. And he said "anything else?"

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2 And so we sit there, think, and it doesn't look like
3 there is anything else.

4 Q. (BY MR. MODI) What else did your attorney
5 tell you?

6 A. No. He asked me what -- what about spaced
7 apart? I said, "No, I don't think that we need to
8 talk about that anymore." And "What about electro --
9 electrically isolated?" I said, "No, we don't -- I
10 think it's okay." So we basically brainstormed, and
11 nothing particular.

12 Q. And when did you realize you needed to
13 clarify your testimony?

14 A. Which one?

15 Q. What you clarified during your redirect.

16 MR. CHIU: Objection; form.

17 A. Well, there is two of them.

18 Q. (BY MR. MODI) Both of them.

19 A. Well, the petition, I thought about it
20 last night, and -- and so during the break I told him
21 that, yeah, we need to -- I need to -- I'd like to
22 clarify that part of testimony.

23 Q. What about the other one?

24 A. The other one is during the break when he
25 said, "Anything else?" And I said, "Yeah, maybe that

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2 part."

3 Q. The petition, the clarification you made,
4 why didn't you clarify that this morning with me?

5 A. That was my --

6 MR. CHIU: Objection;
7 argumentative.

8 A. You didn't have any -- you didn't ask me.

9 Q. (BY MR. MODI) But you haven't answered
10 questions otherwise? You haven't added to your
11 testimony in the last two days when I haven't asked
12 you a question?

13 MR. CHIU: Objection;
14 argumentative.

15 You're harassing the witness,
16 counsel.

17 A. No, you didn't ask me a question related
18 to the petition today, did you, this morning?

19 Q. (BY MR. MODI) But you didn't think that
20 you could -- you could have clarified before I said I
21 had no questions?

22 MR. CHIU: Objection;
23 argumentative. Still harassing the witness.

24 A. So let me ask you. What -- was there
25 opportunity for me to say "Hey, I need to clarify

1 JACK CHUNG-YEUNG LEE, Ph.D. - 2/26/16

2 something?"

3 Q. (BY MR. MODI) Dr. Lee, how many
4 depositions have you done, sir?

5 A. I don't remember.

6 Q. That's okay. Let me ask you a different
7 question.

8 So after your counsel was done with his
9 redirect, we took a break. Right?

10 A. Right.

11 Q. And you modified Exhibit 2004 during the
12 break?

13 A. I just added --

14 Q. Can you give me a yes or no first?

15 A. Yes. I just added a label.

16 Q. Okay. For the record, can you tell us how
17 you modified Exhibit 2004 during the break?

18 A. During the break I added -- indicating
19 that the layer of -- underneath the gate cap is poly,
20 that underneath the cap oxide layer is gate cap. So
21 the substance did not change at all.

22 MR. MODI: We have no further
23 questions, but we want to note for the record
24 that Dr. Lee relied extensively on the LiveNote
25 feed during the last two days of his deposition.

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2 With that, we have nothing
3 further.

4 MR. CHIU: I just want to put on
5 the record that the LiveNote feed oftentimes did
6 not reflect actual dialogue that was actually
7 spoken during the deposition. It was not
8 entirely accurate. I think everybody saw that.
9 So I have no further comments.

10 (THE DEPOSITION CONCLUDED AT 2:36 P.M.)
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,	§	
	§	
Petitioner,	§	
	§	Case IPR2015-01320
VS.	§	Patent No. 6,287,902
	§	
SAMSUNG ELECTRONICS	§	Case IPR2015-1327
COMPANY, LTD.,	§	Patent No. 6,287,902
	§	
Patent Owner.	§	

REPORTER'S CERTIFICATION

DEPOSITION OF JACK CHUNG-YEUNG LEE, Ph.D.

TAKEN FEBRUARY 26, 2016

I, Tamara Chapman, Certified Shorthand
Reporter in and for the State of Texas, hereby
certify to the following:

That the witness, JACK CHUNG-YEUNG LEE,
Ph.D., was duly sworn by the officer and that the
transcript of the oral deposition is a true
record of the testimony given by the witness;

That the original deposition was delivered
to Mr. Naveen Modi;

That a copy of this certificate was served
on all parties and/or the witness shown herein on
3/2/2016.

I further certify that pursuant to FRCP
No. 30(f)(i) that the signature of the deponent:

_____ was requested by the deponent or a

1 party before the completion of the deposition and
2 that the signature is to be returned within 30
3 days from date of receipt of the transcript. If
4 returned, the attached Changes and Signature Page
5 contains any changes and the reasons therefor;

6 _X_ was not requested by the deponent or
7 a party before the completion of the deposition.

8 I further certify that I am neither counsel
9 for, related to, nor employed by any of the
10 parties in the action in which this proceeding
11 was taken, and further that I am not financially
12 or otherwise interested in the outcome of the
13 action.

14 Certified to by me this 2nd day of March, 2016
15
16
17

18 Tamara Chapman, CSR, RPR, CCR (LA)
19 CSR NO. 7248; Expiration Date: 12-31-16
20 TSG Reporting, Inc.
21 Firm Registration No. 615
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Case Name:

Deposition Date:

Deponent:

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THIS _____ DAY OF _____, 2016.

 (Notary Public) MY COMMISSION EXPIRES: _____

 Signature of Deponent