

Filed on behalf of: Samsung Electronics Company, Ltd.

By: Naveen Modi (nVidia-Samsung-IPR@paulhastings.com)  
Joseph E. Palys (nVidia-Samsung-IPR@paulhastings.com)  
Paul Hastings LLP

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

NVIDIA CORPORATION  
Petitioner

v.

SAMSUNG ELECTRONICS COMPANY, LTD.  
Patent Owner

---

Case IPR2015-01327  
Patent No. 6,287,902

---

**DECLARATION OF DR. RICHARD B. FAIR**

# TABLE OF CONTENTS

	Page
I. INTRODUCTION .....	1
II. RESOURCES CONSULTED.....	1
III. BACKGROUND AND QUALIFICATIONS .....	2
IV. LEVEL OF ORDINARY SKILL .....	7
V. SCOPE OF PROJECT .....	8
VI. CLAIM CONSTRUCTION.....	9
A. “an insulating spacer along a sidewall of the [second] patterned conductive layer” (Claims 1, 11, 12, 15, and 18).....	9
B. “an insulating layer” (Claims 1, 2, 8, 11, 12, 14-18).....	10
C. “forming a trench in said substrate, and wherein said field isolation layer fills said trench” (Claim 6).....	10
VII. OVERVIEW OF THE '902 PATENT AND CITED REFERENCES .....	11
A. Overview of the '902 Patent .....	11
B. Overview of <i>Lee</i> .....	13
C. Overview of <i>Yasushige</i> .....	15
VIII. RESPONSE TO PETITIONER’S MAPPING OF THE CLAIMED FEATURES TO THE CITED REFERENCES.....	19
A. Independent Claim 1 .....	19
1. <i>Lee</i> Does Not Disclose or Suggest a “Second Patterned Conductive Layer [that] Is a Dummy Pattern”.....	19
2. <i>Lee</i> Does Not Disclose or Suggest that the “Dummy Pattern” is “Electrically Isolated from the Substrate and Circuits Thereon”.....	22
3. <i>Lee</i> Does Not Disclose an “Insulating Spacer Along a Sidewall of the Second Patterned Conductive Layer. . . [That] Is a Dummy Pattern” .....	28
4. One of Ordinary Skill in the Art Would Not Have Combined <i>Lee</i> with <i>Yasushige</i> as Proposed by Petitioner .....	30
B. Claims 3-5, 7-12, 14-16, and 18 .....	32
1. Claim 7.....	33
2. Claim 10.....	34
C. Claims 2 and 17 .....	35
D. Claims 6 and 13 .....	35
IX. CONCLUSION.....	37

## **I. INTRODUCTION**

1. I have been retained by Samsung Electronics Company, Ltd. (“Patent Owner” or “Samsung”) for this *inter partes* review proceeding. I understand that this proceeding involves U.S. Patent No. 6,287,902 (“the ’902 patent”). I understand the ’902 patent is assigned to Samsung and issued from U.S. Patent Application No. 09/318,188, which is a division of U.S. Patent Application No. 08/748,148, filed on November 12, 1996 (now abandoned).

## **II. RESOURCES CONSULTED**

2. I have reviewed the ’902 patent, including claims 1-18. I have also reviewed the Petition for *Inter Partes* Review (Paper No. 2) filed with the U.S. Patent and Trademark Office (“Office”) by nVidia Corporation (“Petitioner” or “nVidia”) on June 2, 2015 (Paper No. 2, the “Petition”). I have also reviewed the Patent Trial and Appeal Board’s (“Board”) decision to institute *inter partes* review (Paper No. 9, the “Decision”) of December 9, 2015, and any other materials identified in this declaration.

3. I understand that in this proceeding the Board instituted review of the ’902 patent on three grounds: (1) obviousness of claims 1, 3-5, 7-12, 14-16, and 18 over KR App. No. 1994/021255 to Lee (“*Lee*”, Ex. 1107) in view of JP Pub. No. H7-86158 to Yasushige (“*Yasushige*”, Ex. 1109); (2) obviousness of claims 2 and 17 over *Lee*, *Yasushige*, and U.S. Patent No. 4,916,514 to Nowak (“*Nowak*”,

Ex. 1110); and (3) obviousness of claims 6 and 13 over *Lee, Yasushige*, and U.S. Patent No. 4,952,524 to Lee et al. ("*Lee II*", Ex. 1111). (Decision at 19.) I have reviewed the exhibits and other documentation supporting the Petition that are relevant to the Decision and the instituted grounds, and any other material that I reference in this declaration.

### **III. BACKGROUND AND QUALIFICATIONS**

4. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. A more detailed account of my work experience, qualifications, and publications is included in my *curriculum vitae*, which is appended to this declaration.

5. By way of summary, I have been a professor in the Department of Electrical and Computer Engineering at Duke University since 1981. My current tenured position is the Lord-Chandran Professor of Engineering in the Pratt School of Engineering.

6. I received my Bachelor of Science degree in Electrical Engineering from Duke University in 1964. In 1966, I received a Master of Science degree in Electrical Engineering from Penn State University. In 1969, I received a Ph.D. in Electrical Engineering from Duke University.

7. Since 1969, I have been involved in the research, teaching, development, design, and manufacturing of semiconductor devices and processes.

For example, I have experience with thin film processes such as physical and chemical vapor deposition methods, modeling semiconductor technology, designing integrated circuits and semiconductor chips, designing high-density memory and analog circuit layouts, and fabricating integrated circuits. In addition, I have experience in the design, layout, and simulation of analog and digital integrated circuits.

8. From 1969 to 1981, I worked at Bell Laboratories and I had direct experience with the manufacturing, design, and testing of numerous semiconductor devices and integrated circuits, including metal-oxide-semiconductor (MOS) dynamic memory chips. I researched and developed numerous semiconductor devices, including silicon and gallium arsenide transistors, analog and digital integrated circuits, photovoltaic devices, and thin film transistors (“TFTs”) fabricated in laser recrystallized polycrystalline silicon.

9. During my time at Bell Laboratories, I worked on advanced silicon process development in the areas of photolithography, thin film deposition, metallization, etching, cleaning, plasma-assisted processing, LPCVD, ion implantation doping, and annealing/oxidation.

10. In 1981, I became Professor of Electrical Engineering at Duke University. At the same time, I also served in a joint role as Vice President of the Microelectronics Center of North Carolina (“MCNC”) in Research Triangle Park,

North Carolina. During 1990-1993, I led the Center for Microelectronic Systems. The MCNC and the Center for Microelectronic Systems were devoted to the development of advanced technologies for fabricating integrated circuits and for improvements in semiconductor manufacturing processes in general. My areas of responsibility as Vice President included analog and digital integrated circuit design, system design, semiconductor fabrication technology, advanced multichip module packaging, and studies in electronic materials, including amorphous semiconductors and multi-layered aluminum and copper interconnects. In my division at MCNC, we designed, fabricated, and tested the world's first one-million-transistor processor chip in 1987. I also was responsible for the MCNC analytical lab, which included electron microscopy, atomic composition analysis, and sample preparation for reverse engineering studies. I have used such analytical tools to perform reverse engineering of semiconductor devices.

11. While at MCNC, I helped setup a state-of-the-art CMOS processing facility and directed research on semiconductor processing including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin films, metallization, and anisotropic etching processes. I was also involved in the development of an advanced patterning program that included advanced photoresist development, DUV lithography, and the design and development of a magnetron reactive etching tool. We conducted research on

multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. We also had an active research program in characterizing point defects in ion implanted amorphous and single crystal silicon, with the goal of understanding implantation defect annealing effects on dopant impurity diffusion.

12. In 1994, I returned to Duke University full-time. Since then I have continued to teach courses on (1) the design and analysis of analog and digital integrated circuits, (2) semiconductor devices, (3) the chemistry and physics of transistor and integrated circuit fabrication, and (4) thin-film microfluidic devices, fluid dynamics, and applications. In addition, I have an active funded research program that involves undergraduate and graduate students.

13. I have published over 170 papers in refereed and peer-reviewed journals and conference proceedings, contributed chapters to 12 books, edited nine books or conference proceedings, given over 130 invited talks in the field of electrical engineering, and I am a named inventor on 30 granted U.S. patents and 24 pending U.S. patent applications.

14. I am also a Life Fellow of the Institute of Electrical and Electronic Engineers (“IEEE”), a Fellow of the Electrochemical Society, past Editor-in-Chief of the Proceedings of the IEEE, and past Associate Editor of the IEEE

Transactions on Electron Devices. I have been listed in Who's Who in America, Who's Who in Engineering, Who's Who in the Semiconductor Industry, Who's Who in Frontiers of Science and Technology, Who's Who in Technology Today, and American Men and Women in Science. I am a recipient of the IEEE Third Millennium Medal, and I was awarded the Solid State Science and Technology Medal of the Electrochemical Society in April 2003.

15. Based on my over 45 years of experience in thin film and bulk semiconductor device design, processing technology research and development, integrated circuit fabrication, research in point defects in amorphous and single crystal silicon, and the acceptance of my publications and professional recognition by societies in my field, I believe that I am considered to be an expert in the art of semiconductor processing, semiconductor device design and fabrication, and integrated circuit design and fabrication. I have extensive experience both in research and development, and in the implementation of semiconductor manufacturing processes. I have been qualified numerous times as an expert, and I have given expert opinion testimony relating to semiconductor processing, including MOSFET transistor gate formation, shallow-trench isolation, the use of dummy layer features in patterning, and chemical mechanical planarization. Additionally, I have extensive publications in the field of semiconductor



technology, and my accomplishments have been recognized by both academic and professional societies.

16. I am an independent consultant retained by Patent Owner to work on this case. I am compensated for my services in this case at the rate of \$600 per hour. My compensation is not dependent upon my opinions or testimony or the outcome of this case.

#### **IV. LEVEL OF ORDINARY SKILL**

17. I am familiar with the level of ordinary skill in the art with respect to the inventions of the '902 patent as of what I understand is the patent's November 12, 1996 effective filing date. Specifically, based on my review of the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in art at that time would have had (i) a bachelor's degree in electrical engineering, chemical engineering, materials science or physics and 2-3 years of experience in the development of semiconductor fabrication technology, or (ii) a master's degree in the same areas with 1-2 years of the same work experience. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art as I have defined it here.

18. Petitioner's expert, Dr. Jack C. Lee, has defined the person of ordinary skill in the art as a person with an undergraduate degree in electrical engineering (or an equivalent subject) together with three to four years of post-graduate experience designing semiconductor devices and fabrication processes, or a master's degree in electrical engineering (or an equivalent subject) together with one to two years of post-graduate experience in designing semiconductor devices and fabrication processes. (Ex. 1116 at ¶ 19.) In my opinion, my definition is similar to the definition of Dr. Lee offers. While my analysis is based on my definition of the person of ordinary skill in the art, I believe my analysis and opinion would apply equally even under the definition of a person of ordinary skill in the art Dr. Lee proposes.

## **V. SCOPE OF PROJECT**

19. I have been asked to respond to certain of Petitioner's positions and opinions offered by Dr. Lee, including consider how one of ordinary skill in the art would have understood the references mentioned above in relation to the claims of the '902 patent.<sup>1</sup> I understand that the Board relied on Petitioner's positions and Dr. Lee's opinions in its Decision. As such, when I respond to Petitioner's

---

<sup>1</sup> If I do not address a particular statement made by Petitioner, the Board, or Dr. Lee that does not mean that I necessarily agree with that statement.

positions and Dr. Lee’s opinions in this declaration, I am necessarily responding to the Board’s Decision as well. My findings are set forth below.

## VI. CLAIM CONSTRUCTION

20. I understand that Petitioner identified certain terms for construction in the Petition. (Pet. at 25-27; *see also* Ex. 1116 at ¶¶ 70-79.) Below is a what I understand to be a summary of the constructions proposed by Petitioner and Patent Owner, along with the construction (if any) adopted by the Board in its institution decision.

### A. “an insulating spacer along a sidewall of the [second] patterned conductive layer” (Claims 1, 11, 12, 15, and 18)<sup>2</sup>

Patent Owner’s Proposed Construction	Petitioner’s Proposed Construction	Board’s Construction
Plain and ordinary meaning	an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned	No construction proposed

---

<sup>2</sup> I identify only the challenged claims that expressly recite the terms at issue.

**B. “an insulating layer” (Claims 1, 2, 8, 11, 12, 14-18)**

Patent Owner’s Proposed Construction	Petitioner’s Proposed Construction	Board’s Construction
a structure comprising one or more electrically insulating sublayers	Plain and ordinary meaning	No construction proposed

**C. “forming a trench in said substrate, and wherein said field isolation layer fills said trench” (Claim 6)**

Patent Owner’s Proposed Construction	Petitioner’s Proposed Construction	Board’s Construction
Plain and ordinary meaning	Plain and ordinary meaning	No construction proposed

21. I also understand that the Board construed “dummy pattern,” which is a term recited in claims 1, 11, 12, 15, and 18, as “a patterned conductive layer that serves no electrical purpose and is electrically isolated from the substrate and circuits thereon.” (Decision at 7.)

22. I have considered the constructions proposed by the Petitioner, the Patent Owner, and the Board. My analysis and conclusions as set forth below in Section VIII remain the same under any of these constructions. For the remaining claim terms of the ’902 patent that were not identified for construction by any party (including the Board), I have given those terms their plain and ordinary meaning, as would be understood by a person of ordinary skill in the art, at the

time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record.

## **VII. OVERVIEW OF THE '902 PATENT AND CITED REFERENCES**

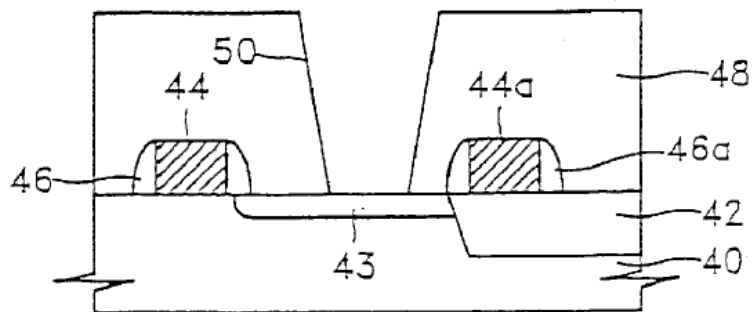
### **A. Overview of the '902 Patent**

23. The '902 patent is directed to a method of providing improved alignment tolerances for contact holes made to scaled microelectronic structures. (Ex. 1001 at 2:44-48.) A problem that the '902 patent addresses is how to reliably make contact holes for MOSFETs in smaller and smaller spaces on a wafer when device integration density increases. (*Id.* at 2:10-41.) For instance, the '902 patent notes that a misaligned contact hole 24 may expose a portion of the active region of a MOSFET and an adjacent field region that may lead to the flow of leakage currents into the well area of the MOSFET. (*Id.* at 2:10-20, Fig. 2.)

24. To remedy the above problem resulting from contact hole misalignment, the '902 patent discloses an exemplary method of forming etch inhibiting layers on the field isolation region adjacent to the active region (where transistors are formed). The etch inhibiting layer improves alignment tolerance for a contact hole between a first patterned conductive layer on an active region of the substrate and an adjacent field region (which isolates an active region). (*Id.* at 4:41-50.) The exemplary solution disclosed in the '902 patent may be better understood by referring to the description associated with figures 4-8.

25. Figure 4 of the '902 patent discloses an exemplary embodiment in which a contact hole 50 is placed between first and second patterned conductive layers 44, 44a to make contact to the doped area 43 (source or drain of a transistor) in the active region. (*Id.* at 4:10-37.)

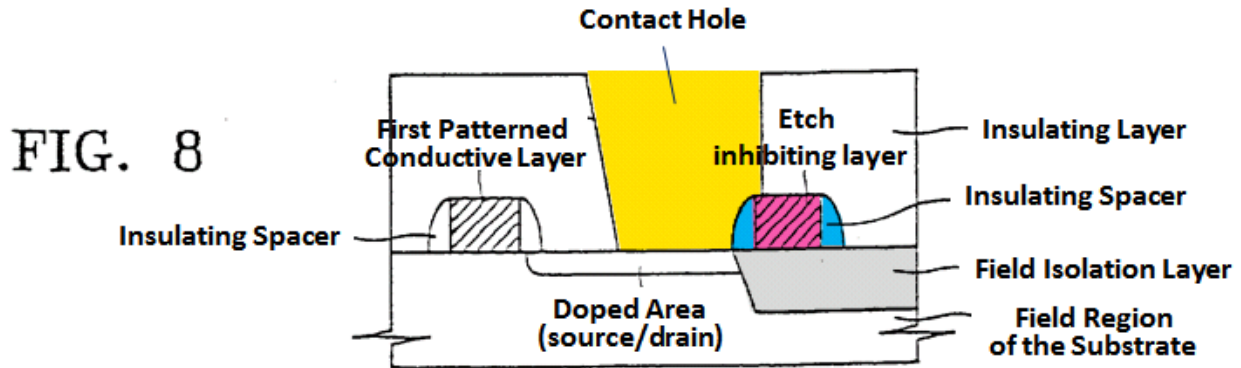
FIG. 4



26. An insulating layer 48 covering the first and second patterned conductive layers 44, 44a, active region 43, and field isolation layer 42 is etched to form contact hole 50. (*Id.* at 5:62-65, 6:8-11, Fig. 7.)

27. Conductive layer 44a (annotated in pink below), which is formed on the field isolation layer 42, in combination with sidewall spacers 46a (annotated in blue below) acts as an etch inhibiting layer protecting the field isolation layer from any undesired etching in case of a contact hole misalignment. (*Id.* at 6:1-18, Fig. 8 (annotated below).) Conductive layer 44a, which is electrically isolated, is a dummy pattern that protects against contact hole misalignment. (*Id.* at 4:25-30, 5:33-44, 6:20-23.) According to the '902 patent, forming an electrically isolated

conductive layer 44a that serves no electrical function was “unlike methods of the prior art.” (*Id.* at 5:33-44.)



(*Id.* at Fig. 8 (annotated).)

28. Claims 1-18 of the '902 patent recite some of the novel features discussed above that protect the field region from contact-hole misalignment, resulting in improved margins for forming contact holes. For instance, claim 1 of the '902 patent recites, *inter alia*, “forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, . . . wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, . . . wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.” (Ex. 1001, claim 1.)

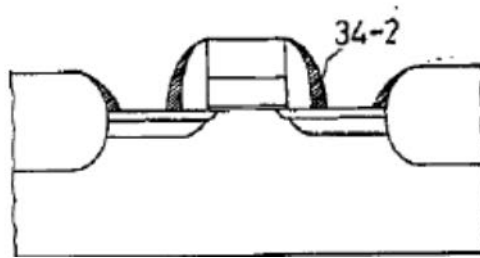
### **B. Overview of *Lee***

29. *Lee* discloses a prior art structure in Fig. 1(a), in which the active region is isolated by a field oxide layer 12 on a semiconductor substrate 11. (Ex.

1107 at 3.) A MOS gate 14 is also shown that is “formed by depositing gate oxide layer, poly and gate caps in . . . sequence and then etching them.” (*Id.*) *Lee* recognizes that in prior art devices, a contact hole misalignment may cause damage to the gate sidewall of the MOS gate or may damage the field oxide layer resulting in junction leakage. (*Id.*) *Lee* illustrates these issues in figure 1(b). (*Id.*)

30. *Lee*’s first embodiment is described with reference to figure 3b, which is shown below:

(b)



(*Id.* at Fig. 3(b).)

31. *Lee* describes the first embodiment as follows: “At this time, the etch stop layer is formed . . . in the form of a sidewall through a deposition and etch-back process using the step area formed on the lower layer without any additional mask.” (*Id.* at 6.). In Fig. 3b above, it can be seen that the step area referred to by *Lee* is the field oxide layer on which the etch stop layer 34-2 is formed “on the lower layer.” (*Id.*)



32. In a second embodiment, *Lee* discloses “forming an etch stop layer (44-2) using an internal connection line (44-3) passing adjacently or the step of a dummy pattern when the step at the lower layer used to form the etch stop layer in the first embodiment is not sufficient.” (*Id.* at 7.) *Lee* is completely silent on the structure or the constituent layers of the “dummy pattern.” For instance, *Lee* does not explain whether the “dummy pattern”<sup>3</sup> takes the shape of a gate (such as MOS gate 34 in Fig. 3(a)) or any other structure. Nor does *Lee* disclose whether the “dummy pattern” includes a conductive portion. Neither does *Lee* disclose that the “dummy pattern” is electrically isolated. All *Lee* discloses is that the etch stop layer 44-2 may be formed using a “dummy pattern” as a step when the step area of the field oxide layer is insufficient.

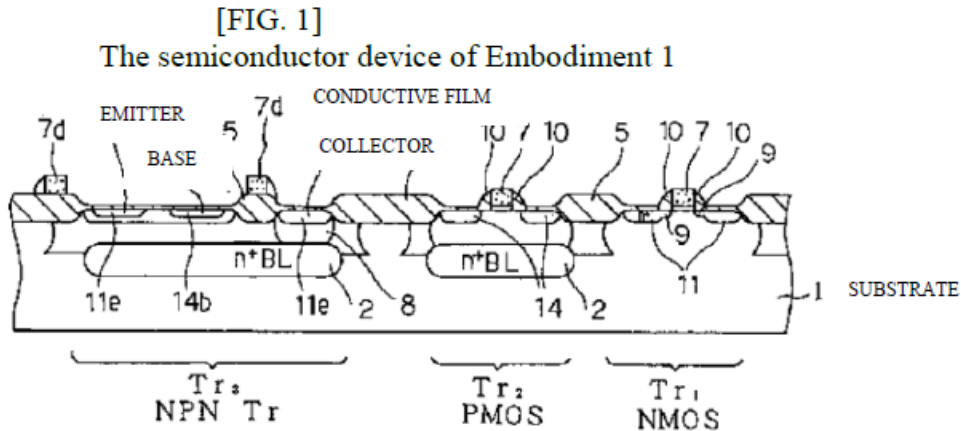
### **C. Overview of *Yasushige***

33. *Yasushige* relates to a method of forming a BiCMOS semiconductor device with a lightly doped drain (LDD) structure. (Ex. 1109 at abstract.) In certain embodiments of *Yasushige*, dummy patterns are formed around the base region of a bipolar transistor simultaneously with the gate electrode of a MOS

---

<sup>3</sup> The discussion here is specific to *Lee*’s disclosure of “dummy pattern” and is not to be confused with the term “dummy pattern” recited in the claims of the ’902 patent.

transistor. For instance, figure 1 of *Yasushige* illustrates dummy patterns (7d) formed on an insulation film (5).

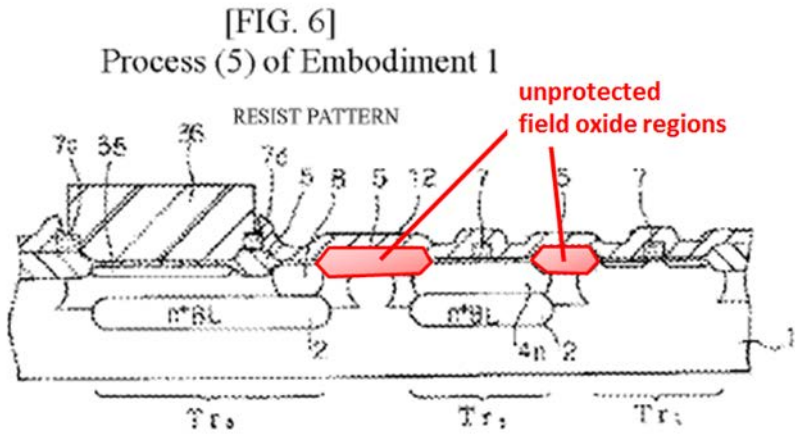


(*Id.* at Fig. 1.)

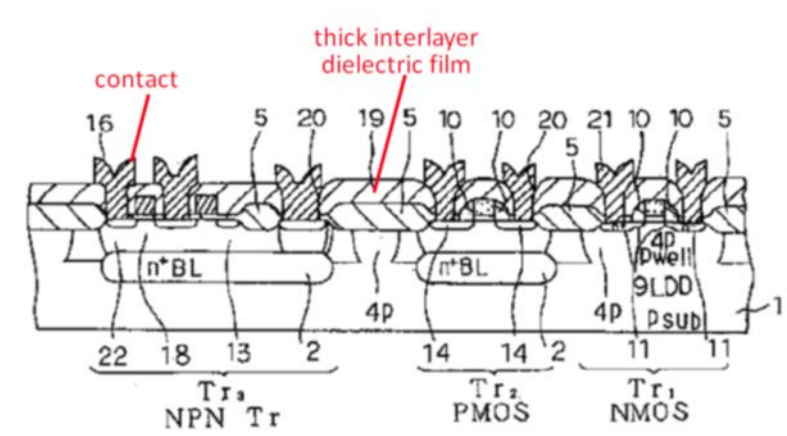
34. One of ordinary skill in the art would have understood that the problem *Yasushige* was trying to solve was how to form lightly doped drain (LDD) sidewalls on MOS transistors without deterioration in the base regions of bipolar transistors formed in the BiCMOS device. (*Id.* at ¶¶ [0027] – [0028].) As shown in figures 4 and 5, dummy patterns 7d are formed around the base region 14b of a bipolar transistor Tr3, and the dummy patterns 7d are “electrically isolated from the base region by an isolation region 5.” (*Id.* at ¶ [0041].) When film 12 of the base region is removed by wet etching, the dummy patterns 7d act as an etch stopper. (*Id.* at Figs. 4, 5, ¶¶ [0045]-[0046].) At this time, the MOSFET portion of the device is covered by a resist pattern 33. (*Id.* at Fig. 4.) But during this wet etch

of the base region isolation film, the sidewall spacers that would have formed on the side of the dummy patterns 7d are removed from one side of the dummy patterns 7d. (*See id.* at Fig. 7, illustrating that the dummy patterns only have spacers 37 on one side.) By doing so, the area of isolation region 5 adjacent to the active area in the bipolar junction portion is left unprotected during any subsequent etching, such as contact hole formation.

35. One of ordinary skill in the art would have also understood that *Yasushige* is not concerned about avoiding damage to the isolation region 5. This is evident from the fact that there is no dummy pattern 7d or any other mask present over the field oxide regions during the anisotropic etching of the SiO<sub>2</sub> film 12. (*See id.* at Fig. 6 (below with annotations added).) Rather, the dummy patterns 7d are added to provide larger tolerance during the formation of resist pattern 36. (*Id.* at ¶ [0049].) It is the resist pattern 36 that carries out *Yasushige*'s purpose of protecting the active region of the transistor (35) during the anisotropic etching process. (*Id.* at ¶ [0049].)



36. Moreover, one of ordinary skill in the art would have understood that *Yasushige* is not concerned about avoiding damage to the field oxide region during the contact hole formation. For instance, the only discussion of the contact hole, as shown in figure 8 of *Yasushige*, relates to an embodiment where dummy patterns are not used. In the embodiment relating to figure 8, the contact holes are made through the thick interlayer dielectric film (19), without any protection from a dummy gate and the sidewall spacers of the dummy pattern for any field oxide region. (See *id.* at Fig. 8 (annotated).)



37. As is shown in Figure 8, the field isolation regions (5) are covered only by the dielectric film (19) and are not protected by a dummy pattern.

## **VIII. RESPONSE TO PETITIONER’S MAPPING OF THE CLAIMED FEATURES TO THE CITED REFERENCES**

### **A. Independent Claim 1**

38. I understand that independent claim 1 recites a “second patterned conductive layer [that] is a dummy pattern electrically isolated from the substrate and circuits thereon.” I also understand that independent claim 1 further recites “an insulating spacer along a sidewall of the second patterned conductive layer.” It is also my understanding that Petitioner and Dr. Lee contend that *Lee* and *Yasushige* disclose these features. (Pet. at 31-41; Ex. 1116 at ¶¶ 95-108; *see also* Decision at 12-15.) In my opinion, this is not correct for at least the following reasons.

#### **1. *Lee* Does Not Disclose or Suggest a “Second Patterned Conductive Layer [that] Is a Dummy Pattern”**

39. *Lee* discloses a “second embodiment” with respect to figure 4. *Lee* does not provide a detailed discussion of figure 4 and simply states that figure 4 discloses “a method of forming an etch stop layer (44-2) using an internal connection line (44-3) passing adjacently *or* the step of a dummy pattern when the step at the lower layer used to form the etch stop layer in the first embodiment is not sufficient.” (Ex. 1107 at 7, emphasis added.) It is my understanding that

Petitioner assumes that element “44-3” in *Lee* refers to the “dummy pattern” and it is my understanding that Dr. Lee confirmed this assumption during his deposition. (Pet. at 36, “dummy pattern 44-3”; *see also* Ex. 2005 at 152:25-153:5, 153:18-19.) This is incorrect because *Lee* never annotates the “dummy pattern” by element 44-3. (*See* Ex. 1107 generally.) *Lee* only refers to an internal connection line 44-3 and not a dummy pattern 44-3.

40. Having assumed that *Lee* discloses a “dummy pattern 44-3,” which it does not, Petitioner and Dr. Lee try to analogize “dummy pattern 44-3” with MOS gate 34 and from that analogy, they conclude that the “dummy pattern” in *Lee* is a “patterned conductive layer” like the polysilicon layer in MOS gate 34. (Pet. at 36-37; *see also* Ex. 1116 at ¶ 102.) One of ordinary skill in the art would not have understood that the “dummy pattern” in *Lee* is a “patterned conductive layer” because there is no disclosure in *Lee* whether the internal connection line 44-3, let alone the “dummy pattern,” has the same structure and composition as MOS gate 34. Nor is there any disclosure in *Lee* that the layers of internal connection line 44-3, let alone the “dummy pattern,” would have been patterned in the same sequence as MOS gate 34. In fact, Petitioner and Dr. Lee acknowledge that “other mechanical structures are possible” for forming the “dummy pattern” in *Lee*. (Pet. at 37; Ex. 1116 at ¶ 104.) Therefore, it is my opinion that one of ordinary skill in the art would not have concluded from *Lee*’s silence regarding the “dummy pattern”

that the “dummy pattern”<sup>4</sup> has the same structure as MOS gate 34, and that by implication the “dummy pattern” is a “patterned conductive layer” because MOS gate 34 has a patterned poly layer.

41. It is my understanding that Dr. Lee contends that the “dummy pattern” in *Lee* is most likely to be a gate structure like MOS gate 34 because “forming a gate pattern is most efficient given the already existing patterning process for gates throughout the chip.” (Pet. at 37, citing Ex. 1116 at ¶ 104.) Dr. Lee also contends that a mechanical structure such as a “dummy pattern” should be “electrically isolated . . . to prevent accidental electrical connections or shorting damage.” (Ex. 1116 at ¶ 104.) However, one of ordinary skill in the art would have known that a simple way to prevent accidental electrical connection or shorting is to make the “dummy pattern” from a non-conductive material so that there is no chance of any shorting. This implies that the “dummy pattern” is not a gate structure.

Accordingly, if, as Dr. Lee contends, the “dummy pattern” should necessarily be “electrically isolated,” then the “most” efficient way to construct the “dummy pattern” would be to form the “dummy pattern” with a non-conductive material instead of using a gate structure like MOS gate 34. After all, *Lee* only utilizes the

---

<sup>4</sup> The term “dummy pattern” as used in the above discussion refers to the “dummy pattern” as recited in *Lee* and not as recited in the claims of the '902 patent.

“dummy pattern” as a step for the etch-stop layer 44-2 and it is not necessary to use a gate structure having a conductive portion to form a step.

**2. *Lee Does Not Disclose or Suggest that the “Dummy Pattern” is “Electrically Isolated from the Substrate and Circuits Thereon”***

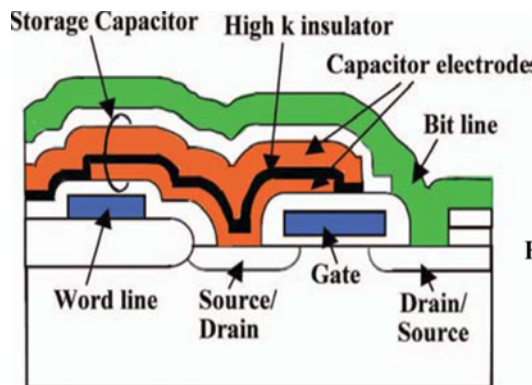
42. It is my understanding that Petitioner and Dr. Lee contend that the “dummy pattern” in *Lee* must be “electrically isolated from the substrate and circuits thereon.” (Pet. at 37-38; Ex 1116 at ¶¶ 103-05.) It is also my understanding that Petitioner provides four reasons for this conclusion. In my opinion, each of these reasons is incorrect.

43. Petitioner and Dr. Lee first contend that the “dummy pattern” is electrically isolated because it does not extend over the active region and is disposed on the field oxide layer. (Pet. at 37; Ex. 1116 at ¶ 103.) Under this rationale, the internal connection line 44-3 would also be “electrically isolated” because the internal connection line 44-3 is also formed over the field oxide layer. (Ex. 1107 at Fig. 4.) But one of ordinary skill in the art would have understood that an “internal connection line” is not “electrically isolated.” Dr. Lee himself confirms this. (Ex. 2005 at 154:13-17; *see also* Pet. at 37, contending that “internal connection line” has connections and dummy pattern does not.) Accordingly, even assuming for the sake of argument that the “dummy pattern” is situated over the field oxide layer, such an assumption cannot lead to a conclusion

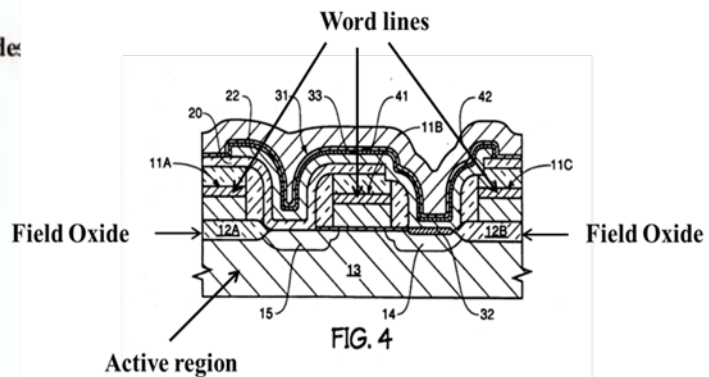


that the “dummy pattern” is “electrically isolated from the substrate and circuits thereon.”

44. Petitioner’s first reasoning is incorrect for the additional reason that the literature prior to 1996 was replete with semiconductor devices in which conductive layers formed on field oxide layers were not “electrically isolated.” For instance, as shown in the annotated figures below, well known semiconductor devices had “word lines” disposed on the field oxide layer. A stacked capacitor DRAM cell invented in the 1970s had a “word line” disposed on a field oxide layer. (Ex. 2007 at 1.) Another stacked capacitor DRAM cell from the early 1990s disclosed in U.S. Patent No. 5,142,438 had two word lines 11A and 11C “traversing field oxide regions 12A and 12B respectively.” (Ex. 2008 at 2:20-27, Fig. 4.) One of ordinary skill in the art would have understood that a word line is not “electrically isolated” despite being disposed on the field oxide layer.



(Ex. 2007 at 1, annotated)



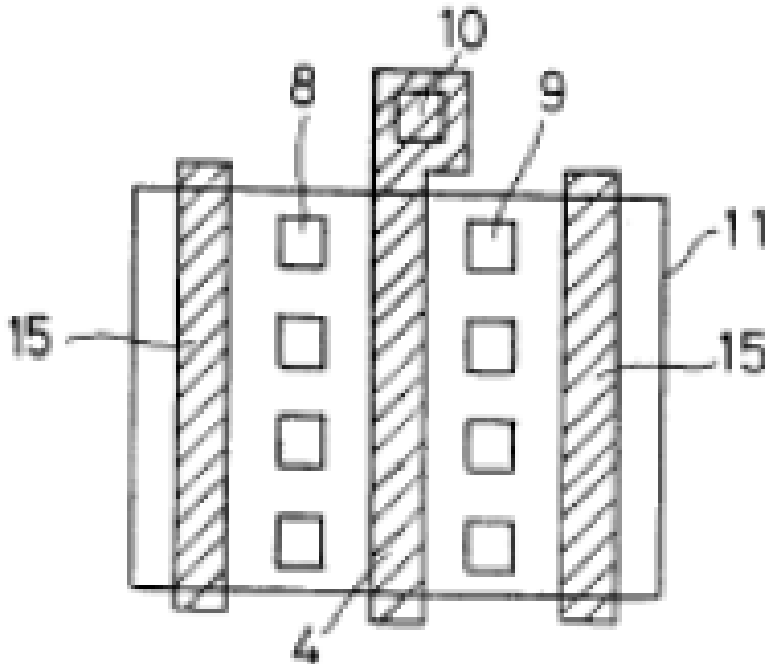
(Ex. 2008 at Fig. 4, annotated)

45. It is my understanding that Petitioner's second reasoning is that because "dummy pattern" is not an "internal connection line," it cannot have any connections and is therefore, "electrically isolated from the substrate and circuits thereon." (Pet. at 37; Ex. 1116 at ¶¶ 103, 104; *see also* Ex. 2005 at 155:17-20, "the dummy pattern is not a connection line, meaning that it is not connected to the substrate or the circuit.") In my opinion, neither *Lee*'s disclosure nor the understanding of one of ordinary skill in the art at the time of the invention of the '902 patent supports Petitioner's analysis. Just because the "dummy pattern" is not an "internal connection line," does not mean that the "dummy pattern" must be "electrically isolated." Dummy patterns can be located anywhere on active regions or on isolation regions. For instance, one of the prior art references cited during prosecution of the '902 Patent, Japanese Patent Application Publication H4-63437 ("Michihiro") (Ex. 1104) discloses "dummy patterns" 15 formed on the active region that are not "internal connection lines" but are still electrically coupled to the substrate (i.e., not electrically isolated). (Ex. 1104 at 4, Fig. 3(c).) These dummy patterns have "the exact same configuration as the gate electrode 4." (*Id.* at 4.) Because "dummy patterns 15" have the same configuration as the gate electrode 4 and they are formed on the active region, one of ordinary skill in the art would have understood that the "dummy patterns 15" are electrically coupled to the underlying substrate. One of ordinary skill in the art would know that such an

isolated gate structure over the active silicon region would modify the thermal equilibrium electrostatic potential in the silicon due to the difference in potential between the conductive dummy gate material and the silicon. (*See, e.g., C.G. Fonstad, Microelectronic Devices and Circuits, McGraw Hill, 1994, pp. 241-242 (Ex. 2009).*) That is, “dummy patterns 15” are not electrically isolated from the substrate.

46. Moreover, one of ordinary skill in the art would have understood that the “dummy patterns 15” are not “internal connection lines” at least because they do not connect to any other circuit in Fig. 3(c). Therefore, it is incorrect for Petitioner and Dr. Lee to conclude that because the “dummy pattern” is not an “internal connection line,” it has to be electrically isolated from the substrate and circuits thereon.

**FIG 3** (c)



(Ex. 1004 at Fig. 3(c).)

47. It is my understanding that Petitioner and Dr. Lee’s third reasoning is that the “dummy pattern” in *Lee* would be “electrically isolated” because a “POSITA would know that keeping the mechanical structure electrically isolated is the best and most efficient practice to prevent accidental electrical connections or shorting damage.” (Pet. at 38, citing Ex. 1116 at ¶ 104.) Petitioner’s theory, however, assumes that the “dummy pattern” has no electrical function to begin with. In my opinion, nothing in *Lee* prevents the “dummy pattern” from having an

electrical function. The following is the entirety of what *Lee* discloses regarding a dummy pattern in its second embodiment:

“FIG. 4 illustrates the second embodiment of the present invention. This is a method of forming an etch stop layer (44-2) using an internal connection line (44-3) passing adjacently or the step of a dummy pattern when the step at the lower layer used to form the etch stop layer in the first embodiment is not sufficient.”

Lee 17-6.

(Ex. 1107 at 7.)

“5. The method for fabricating a semiconductor device in Claim 1, wherein the sidewall use either the step of the connection line at the adjacent lower layer or uses the step by forming an adjacent dummy pattern.”

(*Id.* at 10.)

48. Petitioner and Dr. Lee’s fourth reasoning is that a “dummy pattern” must be “electrically isolated” based on the definition of the term “dummy” as understood by one of ordinary skill in the art. (Pet. at 38-39, citing Ex. 1116 at ¶ 105.) According to Dr. Lee, “a dummy pattern is a gate pattern that performs no electrical function, as confirmed by contemporary electrical engineering and microelectronics dictionaries.” (Ex. 1116 at ¶ 105; *see also* Ex. 2005 at

155:24-156:7, contending that the term “dummy pattern” would be “universally understood by one of ordinary skill in the art as not performing an electrical function.”) I disagree with Dr. Lee that a “dummy pattern” must always be “electrically isolated from the substrate and circuits thereon.” For instance, Michihiro discloses that “dummy patterns” 15 can be electrically coupled to the substrate. (Ex. 1104 at 4, Fig. 3(c).)

**3. *Lee Does Not Disclose an “Insulating Spacer Along a Sidewall of the Second Patterned Conductive Layer. . . [That] Is a Dummy Pattern”***

49. It is my understanding that claim 1 recites “an insulating spacer along a sidewall of the second patterned conductive layer,” which is “a dummy pattern electrically isolated from the substrate and circuits thereon.” Therefore, I understand that claim 1 recites an insulating spacer along a sidewall of a dummy pattern. I also understand that Petitioner and Dr. Lee contend that the “etch stop layer 44-3” is the claimed “insulating spacer” because it is allegedly formed on a sidewall of “dummy pattern 44-3.” (Pet. at 32-33; Ex. 1116 at ¶¶ 95-98.) I disagree with Petitioner and Dr. Lee for at least the following reasons.

50. First, as discussed above in Section VIII.A.2, *Lee* does not disclose that element 44-3 corresponds to the “dummy pattern” recited in *Lee*. Therefore, it is improper for Dr. Lee and Petitioner to assume from the disclosure of figure 4

(which shows “internal connection line 44-3” and “etch stop layer 44-2”) that the etch stop layer 44-2 is also formed on the “dummy pattern” in *Lee*.

51. Second, one of ordinary skill in the art would not have understood that the etch stop layer 44-2 is an “insulating spacer” if as Dr. Lee contends the “dummy pattern” in *Lee* is a conductive portion and that 44-3 is a gate structure. (See Pet. at 36-37, alleging that 44-3 is formed to have a gate structure and includes a conductive portion like in a MOS gate; see also Ex. 1116 at ¶ 102.) *Lee* discloses that the etch stop layer 44-2 may be both “conductive or non-conductive.” (Ex. 1107 at 7.) But it was well understood by one of ordinary skill in the art that a “spacer” for a gate structure *must* be an insulator. Dr. Lee’s testimony in a related proceeding (IPR2016-00134) confirms this understanding. (IPR2016-00134, Ex. 1103 at ¶ 92- “Given that the spacers are in contact with both the gate electrode and the source and drain regions, if they were not electrically insulating, the gate electrode would be short circuited with the source and drain regions, thereby causing the transistor to malfunction.”) Therefore, given *Lee*’s disclosure that the etch stop layer 44-2 may be both “conductive and non-conductive,” one of ordinary skill in the art would not have understood the etch stop layer to be an “insulating spacer.”

**4. One of Ordinary Skill in the Art Would Not Have Combined *Lee* with *Yasushige* as Proposed by Petitioner**

52. It is my understanding that relying on *Yasushige*'s disclosure of dummy pattern 7d formed on field oxide layer 5, Petitioner and Dr. Lee contend that one of ordinary skill in the art would have been motivated to combine the teachings of *Lee* and *Yasushige* such that the "dummy pattern" in *Lee* becomes "electrically isolated." (Pet. at 39; Ex. 1116 at ¶ 106; *see also* Decision at 14-15.) That is, I understand Petitioner proposes to make *Lee*'s dummy pattern "electrically isolated from the circuits and substrate thereon" based on *Yasushige*'s disclosure that dummy pattern 7d is electrically isolated. Petitioner and Dr. Lee are incorrect.

53. As an initial matter, *Yasushige* does not disclose that the dummy pattern 7d is "electrically isolated *from the substrate and circuits thereon*," as required by claim 1. *Yasushige* simply states that it includes a "conductive film identical to the gate electrode of [a] MOS transistor [that] is formed around the base region of [a] bipolar transistor, and said conductive film is electrically isolated from the base region." (Ex. 1109 at ¶ [0029]; *see also id.* at ¶ [0041].) *Yasushige* does not disclose, nor does Petitioner allege that *Yasushige* discloses, that the "conductive film" is electrically isolated from anything other than the "base region." (See *id.* at ¶¶ [0029], [0041].) So even if *Yasushige* discloses electrically isolating



dummy pattern 7d from the “substrate,” which I disagree with, *Yasushige* has no disclosure whether dummy pattern 7d is also electrically isolated from the circuits on the substrate.

54. In my opinion, one of ordinary skill in the art would not have been motivated to combine the teachings of *Lee* and *Yasushige* in the manner proposed by Petitioner. For instance, *Yasushige* does not offer any reasons, nor does Petitioner allege otherwise, for why it would have been desirable to *electrically isolate* the dummy pattern 7d. (See Pet. at 19-21, 39-40.) Petitioner and Dr. Lee nevertheless contend that “electrically isolating the dummy pattern on a field oxide layer would improve the functionality of *Lee*’s disclosure of the dummy pattern and etch stop layer along its sidewall.” (Pet. at 40.) Specifically, they contend:

“Positioning the dummy pattern around the active region would protect the edge of the field oxide layer from being etched by a contact hole formation process. By not positioning the dummy pattern on the active region itself, there is no encroachment onto active region, which would take up valuable space otherwise devoted to active transistors and contact holes.”

55. But the above reasons relate to the placement of the “dummy pattern” and do not explain why a “dummy pattern” would be “electrically isolated.” They do not explain any advantage that would result by electrically isolating *Lee*’s “dummy pattern.” And even if the above reasons provide motivation to place a

“dummy pattern” on the field oxide region, such placement does not ensure that the “dummy pattern” is “electrically isolated.” (*See supra* section VIII.A.1, explaining that placement of a layer over the field oxide region does not result in the layer being “electrically isolated.”)

56. Petitioner and Dr. Lee additionally contend that “keeping the dummy pattern electrically isolated ensures that the dummy pattern will not accidentally cause a short to other circuits of the device, should a contact hole be misaligned far enough to etch into the conductive material of the dummy pattern.” (Pet. at 40; Ex. 1116 at ¶ 108.) This is not correct because the reasoning assumes that adding a layer of insulation around a dummy pattern prevents etching of the layer(s) of the dummy pattern whatever those layer(s) may be. An insulator is not necessary for preventing etching of an underlying layer. This is evident from *Lee* where the etch stop layer is “conductive or non-conductive” and serves as an etch stopper. (Ex. 1107 at 6-8.) Additionally, Lee is unconcerned that his etch-stop layer might not protect any constituent structures beneath it, since his second embodiment forms an etch stop layer (44-2) over an internal connection line (44-3) in Fig. 4. Connection line (44-3) is not electrically isolated.

**B. Claims 3-5, 7-12, 14-16, and 18**

57. Each of the remaining independent claims 11, 12, 15, and 18 recite a “patterned conductive layer” that “is a dummy pattern electrically isolated from the

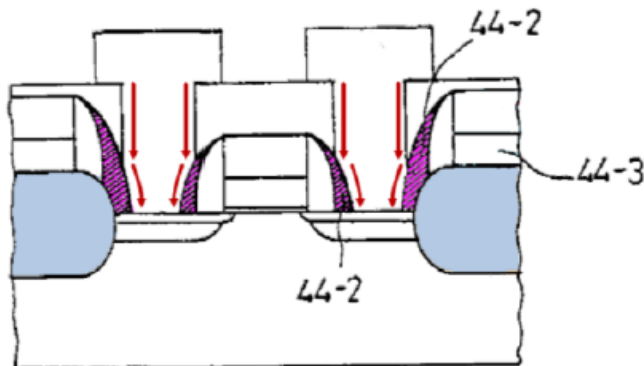
substrate and circuits thereon.” Moreover, Petitioner’s analysis with respect to this limitation of claims 11, 12, 15, and 18 mirrors Petitioner’s analysis for claim 1 for these features (Pet. at 51-54), which as discussed above are not disclosed or suggested by *Lee* and *Yasushige*. Furthermore, as discussed above, in my opinion, one of ordinary skill in the art would not have combined the teachings of *Lee* and *Yasushige* in the manner proposed by Petitioner. I understand that claims 3-5, 7-10, 14, and 16 depend from one of independent claims 1, 12, and 15, and thus require the limitations discussed above for claims 1, 12, and 15. Accordingly, the above discussed shortcomings of the cited references also applies to claims 3-5, 7-10, 14, and 16.

**1. Claim 7**

58. For claim 7, Petitioner’s analysis is incorrect for an additional reason. I understand that claim 7 recites that “the insulating spacer of the etch inhibiting layer extends to the active region of the substrate.” Petitioner and Dr. Lee contend that Lee discloses this feature because the “etch stop layer 44-2 is formed partially on the field oxide layer . . . .” (Pet. at 46; Ex. 1116 at ¶ 122.) But as discussed above in Section VIII.A.3, one of ordinary skill in the art would have understood that the “etch stop layer 44-2” is not an “insulating spacer.” For at least this reason, in my opinion, Lee does not disclose the recited feature of claim 7.

**2. Claim 10**

59. For claim 10, Petitioner's analysis is incorrect for an additional reason. I understand that claim 10 recites that "at least a portion of the contact hole is self-aligned with respect to the first patterned conductive layer and the etch inhibiting layer." Petitioner contends that *Lee* discloses that the "etch stop layer (44-2) is formed along the sidewalls of both a first patterned conductive layer and a dummy pattern," and relies on figure 4 of *Lee* for support. (Pet. at 49; Ex. 1116 at ¶¶ 128-29.) An annotated version of figure 4 which Petitioner relies upon is reproduced below<sup>5</sup>:



(Pet. at 49.)

60. In the above annotated figure, Petitioner assumes that 44-3 refers to a "dummy pattern," which as discussed above in Section VIII.A.1 is not correct. In

---

<sup>5</sup> The corresponding figure is not found in the declaration of Dr. Lee. (See Ex. 1116 at ¶ 128.)

fact, Petitioner's entire analysis for claim 10 is based on this assumption (Pet. at 49-50), which is not true as discussed in Section VIII.A.1.

**C. Claims 2 and 17**

61. I understand that for claims 2 and 17, Petitioner and Dr. Lee rely on *Nowak* in addition to *Lee* and *Yasushige*. (Pet. at 55; Ex. 1116 at ¶¶ 150-53; *see also* Decision at 16-17.) I have reviewed *Nowak* and in my opinion *Nowak* does not remedy the deficiencies of *Lee* and *Yasushige* I identified in Section VIII.A.

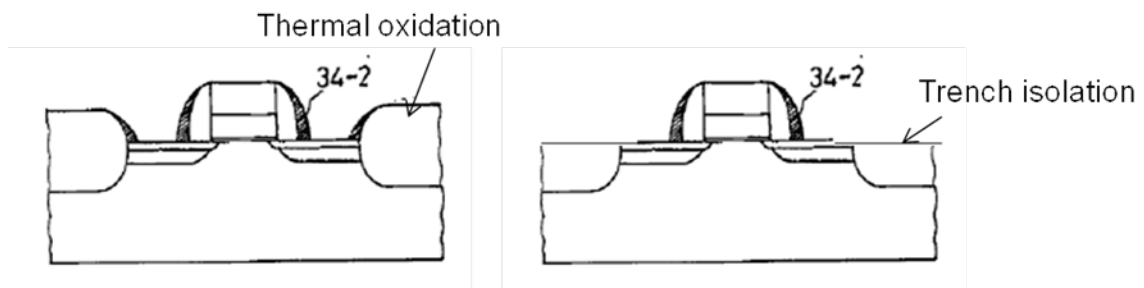
**D. Claims 6 and 13**

62. I understand that for claims 6 and 13, Petitioner and Dr. Lee rely on *Lee II* in addition to *Lee* and *Yasushige*. (Pet. at 58-60; Ex. 1116 at ¶¶ 58-60; *see also* Decision at 17-18.) They allege that *Lee* would have been modified based on the teachings of *Lee II*. I disagree.

63. In my opinion, one of ordinary skill in the art would have realized that modifying *Lee* to incorporate *Lee II*'s techniques as proposed by Petitioner would render *Lee* inoperable for its intended purpose. The figures of *Lee* make clear that the field oxide layer is formed by a process known as local oxidation of silicon (LOCOS) by thermal oxidation. In LOCOS thermally grown field oxide is grown by consuming silicon such that the upper surface of the field isolation region is above the substrate surface. This effect is caused by silicon dioxide having about twice the volume as silicon. (S. Wolf and R.N. Tauber, *Silicon Processing*, Vol. 2,

Lattice Press, 1990, pp. 17-28 (Ex. 2010).) Based on the shape of *Lee*'s field oxide layer 32, one of ordinary skill in the art would have understood that *Lee* used thermal oxidation to form field oxide layer 32, i.e., *Lee* used LOCOS. LOCOS, however, is different from forming a trench and filling the trench with oxide, which is what claims 6 and 13 require. Thus, claims 6 and 13 of the '902 patent do not cover the LOCOS field isolation layers formed by thermal oxidation.

64. *Lee*'s embodiments require the field oxide layer 32 to be formed using the LOCOS method because they require the field oxide layer 32 to protrude above the substrate surface. For instance, *Lee* discloses (in Fig. 3(b)) forming the etch-stop layer on the field oxide layer by using the protruded field oxide layer as a step. (Ex. 1107 at 7.) In trench isolation, the trench is only filled with oxide and then made flush with the substrate surface, as shown below. Thus, *Lee* could not have implemented the embodiment of figure 3(b) without using LOCOS field isolation. A side-by-side comparison of Fig. 3(b) implemented with LOCOS (left) and trench isolation (right) shows why a trench isolation technique would not be desired for *Lee*'s purpose.



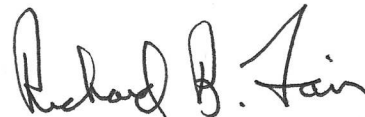
65. Similarly, *Lee* bases his third embodiment (*see* Ex. 1107 at Fig. 5) on utilizing the field oxide layer as a mask for forming etch stop layer (54-2), which again suggests that *Lee* uses the LOCOS field isolation layer for forming an etch stop layer (54-2). (Ex. 1107 at 7, “formed by etching the semiconductor substrate using the oxide layers on the substrate (field oxide layer, gate sidewall, cap oxide layer) as mask.”)

66. In view of the above, one of ordinary skill in the art would not have modified *Lee* to incorporate *Lee II*'s techniques because they would render *Lee* inoperable for its intended purpose.

#### IX. CONCLUSION

67. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the '902 patent.

Executed this 10<sup>th</sup> day of March 2016 in Durham, North Carolina.



---

Richard B. Fair, Ph.D.

# Appendix



## **RESUME**

Richard B. Fair  
3414 CAMBRIDGE RD.  
DURHAM, NORTH CAROLINA 27707

### **EDUCATION AND HONORS**

BSEE - Duke University, Durham, N.C., 1964, Presbyterian Church Scholarship, 1961.  
MSEE - Penn State University, University Park, Pa., 1966, Sylvania Fellow, 9-64/6-66.  
Ph.D. - Duke University, Durham, N.C., 1969, NDEA Fellow, 9-66/6-69.

### **Awards**

- (1) Outstanding Paper Award - IEEE Spring Symp., Duke University, 1969.
- (2) "Outstanding Young Men of America" Award, 1973.
- (3) "Outstanding Young Electrical Engineer of the Year" Award, 1974 -National Award from Eta Kappa Nu.
- (4) American Men and Women in Science, 1979 - Present
- (5) Who's Who in Technology Today, 1980, 81.
- (6) Adjunct Professor, Dept. of Electrical Eng., Duke University, 1980-81.
- (7) Who's Who in Frontiers of Science and Technology, 1985, 1986
- (8) Who's Who in the Semiconductor Industry, 1986.
- (9) Fellow Award, IEEE, 1990
- (10) Who's Who in Engineering, 1991, 1993
- [11] Who's Who in America, 1991, 1993
- (12) Fellow Award, Electrochemical Society, 1994
- (13) Professor James F. Gibbons Achievement Award, 4th International Conference on Advanced Thermal Processing, 1996
- (14) Third Millennium Medal, IEEE, 2000
- (15) Solid State Science and Technology Award – The Electrochemical Society, 2003

### **MEMBERSHIPS / PROFESSIONAL ACTIVITIES**

- (1) Member, Sigma Xi
- (2) Fellow, Electrochemical Society
  - a. Session Chairman numerous times, 1975-present
  - b. Symposium Chairman - "Diffusion Processes in Semiconducting Materials," St. Louis, 1980
  - c. Member of Electronics Division Executive Committee, 1987 -
  - d. Organizing Committee - 6th International Symposium on ULSI Science and Technology
  - e. Organizing Committee - 1<sup>st</sup> Inter. Conf. On ULSI Process Integration - 1999.
  - f. Organizing Committee - Joint Electronics/Dielectric General Session - 1997-
  - g. Co-chair, Sixth International Symposium on ULSI Science and Technology, Montreal (1997)

(3) Life Fellow- IEEE

- a. Session Chairman at 1977-78 International Electron Device Meetings (IEDM)
- b. Chairman, Solid State Device Committee for 1978 IEDM
- c. Member, Integrated Circuit Technology Subcommittee for 1982 IEDM
- d. Member of Editorial Board - Proceedings of the IEEE - 1988-
- e. Editor, Proceedings of IEEE - 1993- 2001
- f. Associate Editor - Trans. Electron Devices - 1990-1993
- g. Guest Editor, Special Issue on NSF Engineering Research Centers, Proceedings of IEEE, Jan. 1993.
- h. Member, IEEE Publications Board - 1993-

(4) Electronic Materials Committee of AIME - 1985 - 1989

(5) Materials Research Society

- a. Symposium Co-Chairman - "Impurity Diffusion and Gettering in Silicon" - 1984
- b. Member of Editorial Board - Bulletin of Materials Research Society - 1985-1987
- (6) Co-chair, 1st International Rapid Thermal Processing Conference, Phoenix (1993).
- (7) Co-chair, 2nd International Rapid Thermal Processing Conference, Monterey (1994).
- [8] Co-chair, 3rd International Rapid Thermal Processing Conference, Amsterdam (1995).
- (9) Co-chair, 4th International Rapid Thermal Processing Conference, Boise (1996).
- (10) Co-chair, 5th International Rapid Thermal Processing Conference, New Orleans (1997).
- (11) Co-Chair, Fourth International Workshop on Meas., Characterization, and Modeling of Ultra- shallow Doping Profiles in Semiconductors, Research Triangle Park, (1999).
- (12) Member of Editorial Advisory Board, Journal Microfluidics and Nanofluidics, (2008-

### **International Activities**

(1) Instructor, CEI Europe - 1985 - present

(2) Member, International Advisory Panel, Microelectronics Systems '91 Conference, Kuala Lumpur, Malaysia

(3) Member, International Advisory Committee, Annual Semiconductor Conference '92-99, Bucharest, Romania

(4) Member, International Advisory Committee, 1993 Symposium on Semiconductor Modeling and Simulation, Taipei, Taiwan

(5) Member, Program Committee, Inter. Symposium on Advanced Microelectronic Devices and Processing - 1993, Sendai, Japan

## **Employment Experience**

Present- - Lord-Chandran Professor of Engineering, Pratt School of Engineering

1993-1994 - Director, Microfabrication Technology and the associated Research Institute of MCNC; Professor, Electrical Engineering, Duke University

1990-1993 - Vice President, MCNC and Executive Director, Center for Microelectronic Systems Technologies; Professor, Electrical Engineering, Duke University

1986-1990 - Vice President, Design Research and Technology, MCNC; Professor, Electrical Engineering, Duke University

10/88-3/89 - Acting President, MCNC; Professor, Electrical Engineering, Duke University

1981-1985 - Vice President, Research Program Management, MCNC; Professor, Electrical Engineering, Duke University

1973-1981 - Supervisor, Bell Laboratories, Reading, PA.

1969-1973 - Member of Technical Staff, Bell Laboratories, Reading, PA.

## **Board Memberships**

1992-1994 - Advanced Technology Applications, Inc.

1993- Microelectronic Technology Corp.

1995- present -Engineering Advisory for the Aurora Fund.

1996- present - Technical Advisory Board, Thunderbird Technologies, Inc.

2003- present - Technical Advisory Board, R.J. Mears, Inc.

2004-present – Chairman, Scientific Advisory Board, Advanced Liquid Logic

## **Courses Taught**

EE218 (Integrated Circuit Engineering) Spring Semester 1982-present

EE163 ( Introduction to Integrated Circuits) Fall/Spring Semester, 1995-99

EE62 (Introduction to Semiconductor Devices), Spring Semester, 1999-present

ECE299 (Biochip Engineering), Fall Semester, 2005-2007

## **U.S Patents**

(1) U.S. Patent 4,033,027 - Dividing Metal Plated Semiconductor Wafers -  
July 5, 1977

- (2) U.S. Patent 6,911,132 – Apparatus for Manipulating Droplets by Electrowetting-based Techniques – June 28, 2005
- (3) U.S. Patent 6,989,234 – Method and Apparatus for Non-Contact Electrostatic Actuation of Droplets – January 24, 2006
- (4) U.S. Patent 7,329,545 – Methods for Sampling a Liquid Flow – February 12, 2008
- (5) U.S. Patent 7,439,014 – Droplet-based Surface Modification and Washing – October 21, 2008
- (6) U.S. Patent 7,569,129 – Methods for manipulating droplets by electrowetting-based techniques – August 4, 2009
- (7) U.S. Patent 7,727,723 – Droplet-based pyrosequencing – June 1, 2010.
- (8) U.S. Patent 7,759,132 – Methods for performing microfluidic sampling – July 20, 2010.
- (9) U.S. Patent 8,048,628 – Methods for nucleic acid amplification on a printed circuit board – Nov. 1, 2011
- (10) U.S. Patent 8,147,668 – Apparatus for manipulating droplets – April 3, 2012.
- (11) U.S. Patent 8,221,605 – Apparatus for manipulating droplets – July 17, 2012.
- (12) U.S. Patent 8,287,711 – Apparatus for manipulating droplets – October 16, 2012.
- (13) U.S. Patent 8,313,895 – Droplet-based surface modification and washing – Nov. 20, 2012
- (14) U.S. Patent 8,349,276 – Apparatus and methods for manipulating droplets on a printed circuit board – Jan. 8, 2013.
- (15) U.S. Patent 8,388,909 – Apparatus and methods for manipulating droplets – Mar.5, 2013.
- (16) U.S. Patent 8,389,297 – Droplet-based affinity assay device and system – Mar.5, 2013.
- (17) U.S. Patent 8,394,249 – Methods for manipulating droplets by electrowetting-based techniques – Mar.12, 2013.
- (18) U.S. Patent 8,613,889 – Droplet-based washing – December 24, 2013.
- (19) U.S. Patent 8,541,176 – Droplet-based surface modification and washing – September 24, 2013.
- (20) U.S. Patent 8,524,506 – Methods for sampling a liquid flow – September 3, 2013.
- (21) U.S. Patent 8,492,168 – Droplet-based affinity assays – July 23, 2013.
- (22) U.S. Patent 8,470,606 – Manipulation of beads in droplets and methods for splitting droplets – June 25, 2013.
- (23) U.S. Patent 8,685, 754 – Droplet actuator devices and methods for immunoassays and washing – April 1, 2014.
- (24) U.S. Patent 8,846,414 – Detection of cardiac markers on a droplet actuator – Sept. 30, 2014.
- (25) US Patent 8,871,071, “Droplet manipulation device”, Oct. 28, 2014.
- (26) US Patent 8,906,627, “Apparatuses and methods for manipulating droplets”, Dec. 9, 2014.
- (27) US Patent 8,951,721, “Droplet-based surface modification and washing,” Feb. 10, 2015
- (28) US Patent 8,980,198, “Filler fluids for droplet operations,” Mar. 17, 2015
- (29) US Patent 9,046,514, “Droplet actuator devices and methods employing magnetic beads,” - June 2, 2015
- (30) US Patent 9,110,017, “Apparatuses and methods for manipulating droplets”, Aug. 18, 2015.

### **U.S. Applications:**

- 1 20130252262 DROPLET-BASED AFFINITY ASSAYS
- 2 20130164742 Droplet-Based Pyrosequencing
- 3 20130146455 Droplet Manipulation Device
- 4 20120165238 Droplet-Based Surface Modification and Washing

- 5 20110076734 Electrowetting Microarray Printing System and Methods for Bioactive Tissue Construct Manufacturing
- 6 20100291578 Droplet-Based Pyrosequencing
- 7 20100140093 Droplet-Based Surface Modification and Washing
- 8 20100116640 Droplet-Based Surface Modification and Washing
- 9 20100025242 APPARATUSES AND METHODS FOR MANIPULATING DROPLETS
- 10 20090280475 Droplet-based pyrosequencing
- 11 20090260988 Methods for Manipulating Droplets by Electrowetting-Based Techniques
- 12 20080264797 Apparatus for Manipulating Droplets
- 13 20080247920 Apparatus for Manipulating Droplets
- 14 20080105549 Methods for performing microfluidic sampling
- 15 20070243634 Droplet-based surface modification and washing
- 16 20070241068 Droplet-based washing
- 17 20070217956 METHODS FOR NUCLEIC ACID AMPLIFICATION ON A PRINTED CIRCUIT BOARD
- 18 20070045117 Apparatuses for mixing droplets
- 19 20070037294 Methods for performing microfluidic sampling
- 20 20060194331 Apparatuses and methods for manipulating droplets on a printed circuit board
- 21 20060054503 Methods for manipulating droplets by electrowetting-based techniques
- 22 20040058450 Methods and apparatus for manipulating droplets by electrowetting-based techniques
- 23 20040055891 Methods and apparatus for manipulating droplets by electrowetting-based techniques
- 24 20040055536 Method and apparatus for non-contact electrostatic actuation of droplets

### **WO and EP Patents**

- |                      |                      |
|----------------------|----------------------|
| 1. EP1859330B1       | 17. EP1554568A2      |
| 2. EP2016189B1       | 18. WO/2004/030820A2 |
| 3. EP1479365B1       | 19. WO/2004/029608A1 |
| 4. EP2016091B1       | 20. WO/2004/029585A1 |
| 5. WO/2009/111723A1  | 21.                  |
| 6. WO/2009/111723A9  |                      |
| 7. EP2016189A2       |                      |
| 8. EP2016091A2       |                      |
| 9. EP1859330A2       |                      |
| 10. WO/2007/120241A3 |                      |
| 11. WO/2007/120241A2 |                      |
| 12. WO/2007/120240A2 |                      |
| 13. WO/2007/120240A3 |                      |

14. WO/2006/081558A2
15. WO/2006/081558A3
16. EP1554568A4

## **PUBLICATIONS**

### **REFEREED ARCHIVAL JOURNALS**

- (1) R. B. Fair, "A Wide Slit Scanning Method for Measuring Electron and Ion Beam Profiles," J. Phys. E., 4, 35 (1971).
- (2) R. B. Fair, "A Self-Consistent Method of Estimating Non-Step Junction Doping Profiles from Capacitance - Voltage Measurements," J. Electrochem. Soc., 118, 971 (1971).
- (3) R. B. Fair, "Analysis and Design of Ion Beam Deposition Apparatus," J. Appl. Phys., 42, 3176 (1971).
- (4) R. B. Fair, "Harmonic Distortion in the Junction Field-Effect Transistor with Field-Dependent Mobility," IEEE Trans. Electron Dev., ED-19, 9 (1972).
- (5) R. B. Fair, "Profile Estimation of High Concentration Arsenic Diffusion," J. Appl. Phys., 43, 1278 (1972).
- (6) R. B. Fair, "High Concentration Arsenic Diffusion in Silicon from A Doped Oxide Source," J. Electrochem. Soc., 119, 1389 (1972).
- (7) R. B. Fair and G. R. Weber, "The Effect of Complex Formation on the Diffusion of Arsenic in Silicon," J. Appl. Phys., 44, 273 (1973).
- (8) R. B. Fair, "Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," J. Appl. Phys., 44, 283 (1973).
- (9) Total Arsenic Concentration in Heavily Doped n and p Type Silicon," J. Appl. Phys., 44, 280 (1973).
- (10) R. B. Fair, "Explanation of Anomalous Base Regions in Transistors," Appl. Phys. Lett., 22, 186 (1973).
- (11) R. B. Fair, "Optimum Low-Level Injection Efficiency of Silicon Transistors with Shallow Arsenic Emitters," IEEE Trans. Electron Devices, Vol. ED-20, 642 (1973).
- (12) R. B. Fair, "Correction of Calculated Vacancy Diffusion Length at 1000 C in Silicon," J. Appl. Phys., 44, 3794 (1973).
- (13) R. B. Fair, "Cooperative Effects Between Arsenic and Boron in Silicon During Simultaneous Diffusions from Ion-Implanted and Chemical Source Predepositions," Solid State Electronics, 17, 17 (1974).
- (14) R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETS," IEEE Trans. Electron Devices, Vol. ED-21, 357 (1974).
- (15) R. B. Fair, "Boron Diffusion in Silicon-Concentration and Orientation Dependence, Background Effects and Profile Estimation," J. Electrochem. Soc., 122, 800 (1975).
- (16) R. B. Fair and P.N. Pappas, "Diffusion of Ion Implanted Boron in High Concentration P and As-Doped Silicon," J. Electrochemical Soc., 122, 1241 (1975).
- (17) R.B. Fair and P.N. Pappas, "The Gettering of Boron by an Ion-Implanted Antimony Layer in Silicon," Solid State Electronics, 18, 1131 (1975).
- (18) R. B. Fair, "Performance Estimation and Optimized Design Considerations for Microwave Power GaAs FETS," IEEE Trans. Electron Dev., ED-22, (1975).
- (19) R. B. Fair and J. C. C. Tsai, "The Diffusion of Ion-Implanted As in Si," J. Electrochem. Soc., 122, 1689 (1975).

- (20) R. B. Fair and J. C. C. Tsai, "Profile Parameters of Implanted-Diffused Arsenic Layers in Silicon," *J. Electrochem. Soc.*, 123, 583 (1976).
- (21) R. B. Fair, "Transistor Design Considerations for Low-Noise Preamplifiers," *IEEE Trans. Nuclear Sci.*, Vol. NS-23, 218 (Feb. 1976).
- (22) R. B. Fair, H. W. Wivell, "Zener and Avalanche Breakdown in As-Implanted Low-Voltage Si n-p Junctions," *IEEE Trans. Electron Dev.*, Vol. ED-23, p. 512 (May 1976).
- (23) R. B. Fair and J. C. C. Tsai, "A Quantitative Model of the Diffusion of Phosphorus in Silicon and the Emitter Dip Effect," *J. Electrochem Soc.*, Vol. 124, 1107 (1977).
- (24) R. B. Fair, "Analysis of Phosphorus-Diffused Layers in Silicon," *J. Electrochem. Soc.*, 125, 323-327 (Feb. 1978).
- (25) R. B. Fair, "Quantified Conditions for Emitter-Misfit Dislocation Formation in Silicon," *J. Electrochem. Soc.*, 125, 928-926 (June, 1978).
- (26) R. B. Fair and J. C. C. Tsai, "Discussion of A Quantitative Model for the Diffusion of Phosphorus in Silicon and the Emitter Dip Effect," *J. Electrochem. Soc.*, 125, 997-998 (June 1978).
- (27) R. B. Fair and J. C. C. Tsai, "Theory and Direct Measurement of Boron Segregation in SiO<sub>2</sub> During Dry, Near Dry, and Wet O<sub>2</sub> Oxidation," *J. Electrochem. Soc.*, 125, 2050 (1978).
- (28) R. B. Fair, "Effect of Strain-Induced Band Gap Narrowing on E-centre Concentrations in Si," *Inst. Phys. Conf. Ser.*, No. 46, Chapter 9, 559 (1979).
- (29) R. B. Fair, "The Effect of Strain-Induced Band-Gap Narrowing on High Concentration Phosphorus Diffusion in Silicon," *J. Appl. Phys.*, 50, 860 (1979).
- (30) R. B. Fair, "Modeling Laser-Induced Diffusion of Implanted Arsenic in Silicon," *J. Appl. Phys.*, 50, 6552 (1979).
- (31) R. B. Fair, "On the Role of Self-Interstitials in Impurity Diffusion in Silicon," *J. Appl. Phys.*, 51, 5828 (1980).
- (32) R. B. Fair, "Oxidation, Impurity Diffusion and Defect Growth in Silicon - An Overview," *J. Electrochem. Soc.*, 128, 1360 (1981).
- (33) R. B. Fair and R. C. Sun, "Threshold Voltage Instability in MOSFET's, Due to Channel Hot Hole Emission," *IEEE Trans. Electron. Devices*, ED-28, 83 (1981).
- (34) R. B. Fair, "Molecular Transport and Diffusion in Solids," *Sensors and Activators*, 1, 305 (1981).
- (35) R. B. Fair and A. Carim, "On the Doping Dependence of Oxidation-Induced Stacking Fault Shrinkage in Silicon," *J. Electrochem Soc.*, 129, 2319 (1982).
- (36) R. B. Fair, "The Silicon Process Balancing Act for VLSI," *Solid State Tech.*, 25, 220 (1982).
- (37) W. G. Meyer and R. B. Fair, "Dynamic Behavior of the Build-up of Fixed Charge and Interface States During Hot Carrier Injection in Encapsulated MOSFET's," *IEEE Trans. Electron Dev.*, Vol. ED-30, 96 (1983).
- (38) R. B. Fair, "MCNC-Organizing Research on the State Level," *IEEE Spectrum*, Vol. 20, p. 58 (1983).
- (39) R. B. Fair, J. J. Wortman, J. Liu, M. Tischler and N.A. Masnari, "Modeling Physical Limitations on Junction Scaling for CMOS," *IEEE Trans. Electron Dev.*, Vol ED-31, 1180 (1984).
- (40) R. B. Fair, J. J. Wortman and J. Liu, "Modeling Rapid Thermal Diffusion of Arsenic and Boron in Silicon," *J. Electrochem. Soc.*, 131, 2387 (1984).

- (41) R. B. Fair, "The Role of Vacancies and Self-Interstitials in Impurity Diffusion in Silicon," *Materials Science Forum*, Vol. 1. (Trans. Tech. Pub. Switzerland) pp. 109-132 (1984).
- (42) W. B. Wilson, H. Z. Massoud, E. T. Swanson, R. T. George and R. B. Fair "Measurement and Modeling of Charge Feedthrough in n-Channel MOS Analog Switches," *IEEE J. Solid State Cir.* Vol. SC-20, pp. 1206-1213 (1985).
- (43) J. Liu, J. J. Wortman and R. B. Fair, Shallow p+-n Junction for CMOS VLSI Application Using Germanium Preamorphization, *IEEE Trans. Electron. Dev.*, Vol ED-32, 2533 (1985).
- (44) R.B. Fair, "Modeling of Dopant Diffusion During Rapid Thermal Annealing," *J. Vac. Sci. Technology A4*, 926 (1986).
- (45) R. B. Fair, M. L. Manda and J. J. Wortman, "The Diffusion of Antimony in Heavily Doped n- and p-type Silicon," *J. Mater. Res.*, 1,705 -717 (1986).
- (46) J. C. C. Tsai, D. G. Schimmel, R. B. Fair and W. Maszara, "Point Defect Generation During Phosphorus Diffusion in Silicon-1. Concentrations Above Solid Solubility," *J. Electrochem. Soc.*, .134, 1508 (1987).
- (47) R. Subrahmanyam, H. Z. Massoud and R. B. Fair, "The Influence of HCl on the Oxidation - Enhanced Diffusion of Boron and Arsenic in Silicon," *J. Appl. Phys.*, 61, 4804 (1987).
- (48) J. C. Tsai, D. G. Schimmel, R. E. Ahrens and R. B. Fair, "Point Defect Generation During Phosphorus Diffusion in Silicon II. Concentrations below Solid Solubility, Ion-Implanted Phosphorus," *J. Electrochem. Soc.*, 134, 2348 (1987).
- (49) R. B. Fair, "Reply to Comments of F. F. Morehead," *J. Mater. Res.*, 2, 539 (1987).
- (50) R. B. Fair, "Low-Thermal Budget Process Modeling with the PREDICT Computer Program," *IEEE Trans. Electron. Dev.*, .35, 285 (1988).
- (51) A. C. Ajmera, G. A. Rozgonyi and R. B. Fair "Point Defect/Dopant Diffusion Considerations Following Preamorphization of Silicon via Si+ and Ge+ Implantation," *Appl. Phys. Lett.*, 52 (10), 813 (1988).
- (52) R.B. Fair and J.E. Rose, "Process Simulation of Submicron Technologies" *Semicond. Int.*,13, 72, (1987).
- (53) M. C. Ozturk, J. J. Wortman and R. B. Fair, "Very Shallow P+n Junction Formation by Low Energy BF<sub>2</sub><sup>+</sup> Ion Implantation into Crystalline and Germanium Preamorphized Silicon," *Appl. Phys. Lett.*, 52 (12), 963 (1988).
- (54) R. Subrahmanyam, H. Z. Massoud and R. B. Fair, "Experimental Characterization of Two-Dimensional Dopant Profiles in Silicon Using Chemical Staining," *Appl. Phys. Lett.*, 52 (25), 2145 (1988).
- (55) Y. Kim, H.Z. Massoud and R.B. Fair, "Boron Profile Changes During Low-Temperature Annealing of BF<sub>2</sub><sup>+</sup>-implanted Silicon," *Appl. Phys. Lett.*, .53, 2197 (1988).
- (56) Y. Kim, H.Z. Massoud and R.B. Fair, "The Effect of Ion-Implantation Damage on Dopant Diffusion in Silicon During Shallow-Junction Formation," *J. Electronic Mater.*, 18, 143 (1989).
- (57) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," *Nuclear Instr. and Methods*, B37/38, 371 (1989).
- (58) W.B. Rogers, H.Z. Massoud, R.B. Fair, U.M. Gosele, T.Y. Tan and G.A. Rozgonyi, "The Role of Silicon Self-Interstitials Supersaturation in the Retardation of Oxygen Precipitation in Czochralski Silicon," *J. Appl. Phys.*, 65, 4215-4219 (1989).
- (59) R.B. Fair, "Point Defect Charge-State Effects on Transient Diffusion of Dopants in Si," *J. Electrochem. Soc.*, 137, 667 (1990).
- (60) R.B. Fair and G.A. Ruggles, "Thermal Budget Issues for Deep Submicron ULSI," *Solid State Tech.*, .33, 107 (1990).



- (61) R.B. Fair, "Damage Removal/Dopant Diffusion Tradeoffs in Ultra-Shallow Implanted p+-n Junctions," IEEE Trans. Electron Dev., vol 37, 2237 (1990).
- (62) Y. Kim, H.Z. Massoud and R.B. Fair, "The Effect of Annealing Ambient on Dopant Diffusion in Silicon during Low Temperature Processing, J. Electrochem. Soc. 137, 2599-2603 (1990).
- (63) R.B. Fair (Invited), "Challenges to Manufacturing Submicron, Ultra-Large Scale Integrated Circuits," Proc. IEEE, .78, pp. 1687-1705, Nov. 1990.
- (64) R. Subrahmanyam, H.Z. Massoud and R.B. Fair, "Comparison of Measured and Simulated Two Dimensional Profiles in Si," J. Electrochem Soc., 137, 1573 (1990).
- (65) R.B. Fair, C.L. Gardner, M.J. Johnson, S.W. Kenkel, D.J. Rose, J.E. Rose and R. Subrahmanyam, "Two-Dimensional Process Simulation Using Verified Phenomenological Models," IEEE Trans. Computer-Aided Design, vol. 10, p. 643 (1991).
- (66) M.R. Mirabedini, S.H. Goodwin-Johansson, H.Z. Massoud and R.B. Fair, "Subquarter-micrometer Elevated Source and Drain MOSFET Structure using Polysilicon Spacers," Electronic Lett., 30, 1631 (1994).
- (67) R.B. Fair and R.A. Gafiteanu, "Modeling Boron Diffusion in Thin Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 17, 497-499 (1996).
- (68) R.B. Fair, "Oxide Thickness Effect on Boron Diffusion in Thin Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 17, 242 (1996).
- [69] R.B. Fair, "Physical Models of Boron Diffusion in Ultrathin Gate Oxides," J. Electrochem. Soc., 144, 708 (1997).
- (70) R.B. Fair, "Modeling Boron Diffusion in Ultrathin Nitrided Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 18, 244 (1997).
- (71) G. Chen, T. Borca-Tasciuc, and R.B. Fair, "Photon Effect on Radiative Properties of Silicon During Rapid Thermal Processing," J. Appl. Phys. 82, 830 (1997).
- [72] R.B. Fair, "History of Some Early Developments in Ion Implantation Technology Leading to Silicon Transistor Manufacturing," Proc. of IEEE, 86, 111 (1998).
- (73) R.B. Fair and S. Li, "Photonic Effects in the Deactivation of Ion Implanted Arsenic," J. Appl. Phys., 83, 4081 (1998).
- (74) N. Vasudevan, R.B. Fair, and H.Z. Massoud, "Energy Considerations During the Growth of a Molten Filament in Metal-to-metal Amorphous-silicon Antifuses," J. Appl. Phys., 84, 4979 (1998).
- (75) T.W. Tsuei, R.L. Wood, C.K. Malek, M.M. Donnelly, and R. B. Fair, "Tapered Microvalves Fabricated by Off-axis X-ray Exposures," Microsystem Technologies, 4, 201 (1998).
- (76) N. Vasudevan, R.B. Fair, and H.Z. Massoud, "ON-state Reliability of Amorphous-silicon Antifuses, J. Appl. Phys., 84, 6440 (1998).
- (77) N. Vasudevan, H.Z. Massoud, and R.B. Fair, "A Thermal Model for the Initiation of Programming in Metal-to-Metal Amorphous-Silicon Antifuses," J. Electrochem. Soc., 146, 1536-1539 (1999).
- (78) R.B. Fair, "Anomalous B Penetration Through Ultrathin Gate Oxides During Rapid Thermal Annealing," IEEE Electron Dev. Lett., 20, 466 (1999).
- (79) Y. Wu, H. Niimi, H. Yang, G. Lucovsky, and R.B. Fair, "Suppression of Boron Transport Out of p+ Polycrystalline Silicon at Polycrystalline Silicon Dielectric Interfaces," J. Vac. Sci. Technol. B, 17(4), 1813-1822 (1999).

- (80) T. Zhang, A. Dewey, and R.B. Fair, "A Hierarchical Approach to Stochastic Discrete and Continuous Performance Simulation Using Composable Software Components," *J. Microelectronics*, 31 (1999).
- (81) M.G. Pollack, R.B. Fair, and A.D. Shenderov, "Electrowetting-Based Actuation of Liquid Droplets for Microfluidic Applications," *Appl. Phys. Lett.*, 77, 1725 (2000).
- (82) T. Zhang, F. Cao, A. Dewey, R.B. Fair, and K. Chakrabarty, "Performance Analysis of Microelectrofluidic Systems Using Hierarchical Modeling and Simulation," *IEEE Trans. Circuits and Systems II: Analog and Digital Processing*, vol. 48, 482 (2001).
- (83) J. Ding, K. Chakrabarty and R. B. Fair, "Scheduling of Microfluidic Operations for Reconfigurable Two-Dimensional Electrowetting Arrays", *IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems*, 29, 1463-1468 (2001).
- (84) T. Zhang, K. Chakrabarty and R. B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 21, 987 (2002).
- (85) M.G. Pollack, A.D. Shenderov, and R.B. Fair, "Electrowetting-based Actuation of Droplets for Integrated Microfluidics," *Lab on a Chip*, vol. 2, pp. 96-101, 2002.
- (86) T. Zhang, K. Chakrabarty and R. B. Fair, "Integrated hierarchical design of microelectrofluidic systems using SystemC", *Microelectronics Journal*, vol. 33, pp. 459-470, May 2002.
- (87) H. Ren, R. B. Fair, M. G. Pollack and E. J. Shaughnessy, "Dynamics of Electro-wetting Droplet Transport, *Sensors and Actuators B: Chemical*, Volume 87, Issue 1, 15 November 2002, Pages 201-206.
- (88) P. Paik, V.K. Pamula, M.G. Pollack, and R.B. Fair, "Electrowetting-Based Droplet Mixers for Microfluidic Systems," *Lab on a Chip*, vol. 3, pp.28-33 (2003).
- (89) H. Ren, R.B. Fair, and M. Pollack, "Automated On-Chip Droplet Dispensing with Volume Control by Electrowetting Actuation and Capacitance Metering", *Sensors and Actuators B*, 98, 319-327 (2004).
- (90) P. Paik, V.K. Pamula, and R.B. Fair, "Rapid Droplet Mixers for Digital Microfluidic Systems," *Lab, on a Chip*, vol. 3, pp.253-259 (2003).
- (91) V. Srinivasan, V.K. Pamula, and R.B. Fair, "Droplet-based microfluidic lab-on-a-chip for glucose detection," *Analytica Chimica Acta*, Vol. 507, 145-150 (2004).
- (92) T. Zhang, K. Chakrabarty, and R.B. Fair, "Behavioral Modeling and Performance Evaluation of Microfluidics-Based PCR Systems Using System C", *IEEE Trans, Computer-Aided Design of Integrated Cir. And Sys.*, vol. 23, 843 (2004).
- (93) V. Srinivasan, V.K. Pamula, and R.B. Fair, "An Integrated Digital Microfluidic Lab-on-a-Chip for Clinical Diagnostics on Human Physiological Fluids," *Lab-On-A-Chip*, 4, 310 (2004).
- (94) F. Su, K. Chakrabarty, and R.B. Fair, "Microfluidics-Based Biochips: Technology Issues, Implementation Platforms, and Design Automation Challenges," *IEEE Trans. Computer-Aided Des. Of Integ. Cir. And Sys.*, vol. 25, pp. 211-223 (2006).
- (95) R.B. Fair, "Digital Microfluidics: is a true lab-on-a-chip possible?" *J. Microfluidics and Nanofluidics*, vol. 3, 245-281 (2007). (Invited)
- (96) R.B. Fair, A. Khylstov, T.D. Tailor, V. Ivanov, R.D. Evans, V.Srinivasan, V.K. Pamula, M.G. Pollack, P.B. Griffin, J. Zhou, "Chemical and Biological Applications of Digital Microfluidic Devices," *IEEE Design and Test of Computers*, 24, No. 1, pp.10-24, Jan-Feb (2007). (Invited)

- (97) J. Zhou, L. Lu, K. Byrapogu, D. Wootton; P. Lelkes, and R. Fair, "Electrowetting Based Multi-microfluidics Array Printing of High Resolution Tissue Construct with Embedded Cells and Growth Factors," *Virtual and Physical Prototyping*, 2:4, 217 – 223 (2007).
- (98) L. Luan, R.D. Evans, N.M. Jokerst, and R.B. Fair, "Integrated Optical Sensor in a Digital Microfluidic Platform," *IEEE Sensors J.*, vol. 8, pp. 628-635 (2008).
- (99) R. B. Fair and M. A. Shannon and O. K. Tan and O. Geschke and C. H. Ahn and O. Kaynak and M. J. Vellekoop, *Introduction for the special issue on sensors for microfluidic analysis systems*, *IEEE Sensors Journal*, (2008), vol. 8, pp. 427 – 429.
- (100) R.B. Fair, "What is a lab-on-a-chip?" *ACM/SIGDA Newsletter*, vol. 38, No. 12, (2008)
- (101) J.H. Song, R. Evans, Y.-Y. Lin, B.-N. Hsu, and R.B. Fair, "A Scaling Model for Electrowetting-on-Dielectric Microfluidic Actuators," *Microfluid Nanofluid Online First*, Nov. 2008. In print: vol. 7, 75-89 (2009)
- (102) K. Chakrabarty, R.B. Fair, and J. Zeng, "Design Tools for Digital Microfluidic Biochips: Toward Functional Diversification and More than Moore," *IEEE Trans. Computer-Aided Des. Integrated Cir. And Sys.*, vol 29, No. 7, pp. 1001-1017 (2010).
- (103) Y-Y Lin, R.D. Evans, E. Welch, B-N Hsu. A.C. Madison and R.B. Fair, Low-voltage electrowetting-on-dielectric platform using multi-layer insulators," *Sensors and Actuators B: Chemical*, v. 150, 465-470 (2010)
- (103) E.R. Welch, Y-Y Lin, A. Madison, R.B. Fair, "Picoliter DNA sequencing chemistry on an electrowetting-based digital microfluidic platform," *BioTechnology Journal*, v. 6, pp. 165-176 (2011)
- (104) D.J. Boles, J.L. Benton, G.J.Siew, M.H. Levy, P.K. Thwar, M.A. Sandahl, J.L. Rouse, L.C. Perkins, A.P. Sudarsan, R. Jalili, V.K. Pamula, V. Srinivasan, R.B. Fair, P.B. Griffin, A.E. Eckhardt, M.G. Pollack, "Droplet-based pyrosequencing using digital microfluidics," *Anal. Chem*, 83, 8439 (2011)
- (105) L. Luan, M.W. Royal, R. Evans, R.B. Fair, and N.M. Jokerst, "Chip scale microresonator sensors integrated with embedded thin film photodetectors on electrowetting digital microfluidics platforms," *IEEE Sensors Journal*, v. 12, pp. 1794-1800, (2012)
- (106) Y-Y Lin, E.F. Welch, R.B. Fair, "Low voltage picoliter droplet manipulation utilizing electrowetting-on-dielectric platforms," *Sensors & Actuators, B: Chem.* v. 173, pp. 338-345 (2012), <http://dx.doi.org/10.1016/j.snb.2012.07.022>
- (107) M.W. Royal, N.M. Jokerst, and R.B. Fair, "Integrated sample preparation and sensing: polymer microresonator sensors embedded in digital electrowetting microfluidic systems," *IEEE Photonics J.*, 4, 2126-35 (2012)
- (108) M.W. Royal, N.M. Jokerst, and R.B. Fair, "Droplet-based sensing: Optical microresonator sensors embedded in digital microfluidics systems, *IEEE Sensors J.*, 13, 4733-42, Dec. 2013.
- (109) L. Chen and R.B. Fair, "Digital microfluidics chip with integrated intra-droplet magnetic bead manipulation," *Microfluid Nanofluid*, published online 24 September, 2015. Print: vol. 19, No. 6, pp. 1335-1348, Dec, 2015.

### REFEREED CONFERENCE PROCEEDINGS

- (1) A. B. El-Kareh, R. B. Fair and C. R. Marsh, "A Machine-Scan Electron Beam Device," *Proc. 8th Electron and Laser Beam Symp.*, p. 331 (1966).
- (2) R. B. Fair, "Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," *1972 IEDM Tech. Dig.*, p. 96 (1972).

- (3) R. B. Fair, "Recent Advances in Implantation and Device Modeling for the Design and Process Control of Bipolar ICs, in Semiconductor Silicon 1977, Eds. H. R. Huff and E. Sirtl, pp. 968-987, (The Electrochemical Soc.) 1977.
- (4) R. B. Fair, "Modeling Laser-Induced Diffusion of Implanted Arsenic in Silicon," "Proc. of Laser and Electron Beam Processing of Electronic Materials," (Ed. by C. L. Anderson, G. K. Celler, G. A. Rozgonyi, The Electrochem. Soc., Princeton) p. 204.
- (5) R. B. Fair and R. C. Sun, "Threshold Voltage Instability in MOSFET's Due to Channel Hot Hole Emission," in Tech. Digest of the Inter. Electron Device Meeting, p. 746 (1980).
- (6) R. B. Fair, "Modeling Anomalous Phenomena in Arsenic Diffusion in Silicon," in Semiconductor Silicon/1981. Eds. H. R. Huff, R. J. Krogler and Y. Takeishi. (The Electronic Society, Inc., Pennington, N.J., 1981) p.963.
- (7) R. B. Fair and W. G. Meyer, "Anomalous Junctions Formed by Cross-contamination of Phosphorus During Arsenic Implantation in Silicon," in Silicon Processing, ASTM STP804, D.C. Gupta, Ed., American Society for Test and Mater., 1983, pp. 290-305.
- (8) R. B. Fair, "Impurity Concentration Doping Effects on Impurity Diffusion in Silicon," Semiconductor Processing and Equipment Sym. Tech. Proc., p. 230 (1983).
- (9) R. B. Fair, "Modeling of Dopant Diffusion and Associated Effects in Silicon" in Defects in Semiconductors II, Mat. Res. Soc. Symp. Proc. Vol. 14 (Elsevier, Amsterdam), pp. 61-74 (1983).
- (10) R. B. Fair, "MCNC - A New Multi-Institutional Thrust in Manufacturing Technology," Proceedings UGIM-83, IEEE, p. 10, 1983.
- (11) R. B. Fair, J. J. Wortman, J. Liu, "Modeling Rapid Thermal Annealing Processes for Shallow Junction Formation in Silicon," 1983 IEDM Tech. Dig., pp. 658-661 (1983).
- (12) B. Rogers, R. B. Fair, W. Dyson and G. A. Rozgonyi, "Computer Simulation of Oxygen Precipitation and Denuded Zone Formation," in VLSI Science and Technology 1984, Proceedings of the 2nd International Symposium on VLSI Science and Technology, Vol. 84-7 (The Electrochemical Society, Pennington, NJ) pp. 74- 84 (1984).
- (13) R. B. Fair, "Observations of Vacancies and Self-Interstitials in Diffusion Experiments in Silicon," in Thirteenth Inter. Conf. on Defects in Semiconductors, Vol. 14a (Metallurgical Soc., Warrendale, PA.) ed. L. C. Kimberling and J. M. Parsey, pp. 173-185 (1984).
- (14) R.B. Fair and R. Subrahmanyam, "PREDICT-A New Design Tool for Shallow Junction Processes," Proc., Adv. Applications of Ion Implantation, Vol. 530 (The Inter. Society for Optical Engineering, Bellingham, WA) ed. M.I. Current and D. K. Sadana, pp. 88-96 (1985).
- (15) R. B. Fair and J. E. Rose, "A deep Decision Tree Approach to Modeling Submicron Silicon Technologies," in ICCAD Dig. of Tech. Papers, (Computer Society Press, Los Angeles, CA), pp. 248-251 (1987).
- (16) R. B. Fair, "Process Models for Ultra-Shallow Junction Technologies," IEDM Tech. Digest, pp. 260-263 (1987).
- (17) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," Proc. Shanghai Workshop on Ion Implantation, Ed. Z. Shichang (Academia Seneca, Shanghai), 1989 pp.12-22.
- (18) R.B. Fair, "Oxidation-induced Defects and Effects in Silicon During Low-Thermal-Budget Processing" in The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface, eds. C.R. Helms and B.E. Deal (Plenum, New York), 1989, pp.459-468.

- (19) G.A. Ruggles, S.N. Hong, J.J. Wortman, M. Ozturk, E.R. Meyers, J.J. Hren and R.B. Fair, "A Comparison of Low Energy BF<sub>2</sub> Implantation in Si and Ge Preamorphized Silicon," in *Mat. Res. Symp. Proc.*, vol. 128 (Mat. Res. Soc., Pittsburgh, 1989), p. 611.
- (20) R. Subrahmanyam, H.Z. Massoud and R.B. Fair, "Accurate Junction-Depth Measurements Using Chemical Staining," in *Semiconductor Fabrication: Technology and Metrology ASTM STP 990*, D.C. Gupta, ed. (Am. Soc. for Testing and Materials, 1989), p. 126.
- (21) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," *Proc. First Inter Symp. on Adv. Materials for ULSI*, vol 88-19, M. Scott, Y. Akasaka and R. Reif, eds. (The Electrochem. Soc., Pennington, N.J., 1988) pp. 123-135.
- (22) R.B. Fair and R. Subrahmanyam, "Phenomenological Versus Point-Defect-Based Process Modeling-Where Should You Put Your Money?, in *Proc. 2nd Inter. Symp. on ULSI Science and Tech.*, vol. 89-9, C.M. Osburn and J.M. Andrews, eds. (The Electrochem. Soc. Pennington, N.J., 1989) pp, 133-143.
- (23) R.B. Fair, "Shallow Junctions-Modeling the Dominance of Point Defect Charge States During Transient Diffusion," *IEDM Tech. Digest*, pp. 691-693 (1989).
- (24) R.R. Ward, H.Z. Massoud and R.B. Fair, "The Thermal Oxidation of Heavily Doped Silicon in the Thin-Film Regime: Dopant Behavior and Modeling Growth Kinetics," in *Semiconductor Silicon 1990, Proceedings of the Sixth Inter. Symp. on Si Mater. Sci. and Tech.*, Eds. H.R. Huff, K.G. Barraclough and J. Chikawa, Vol. 90-7 (The Electrochem. Soc., Pennington) pp. 405-416, 1990.
- (25) R.B. Fair, "Process Model for Simulating the Effect of Amorphizing Implants on Phosphorus Diffusion," *ibid*, pp. 429-436, 1990.
- (26) Y. Kim, H.Z. Massoud, S. Chevacharoeukul and R.B. Fair, "The Role of End-of-Range Dislocation Loops as a Diffusion Barrier," *ibid*, pp. 437-446, 1990.
- (27) Y. Kim, H.Z. Massoud, U.M. Gosele, and R. B. Fair, "Physical Modeling of the Time Constant of Transient Enhancement in the Diffusion of Ion-Implanted Dopants in Silicon," in *Process Physics and Modeling in Semiconductor Technology, Proceedings of the 2nd International Sym.*, Eds. G.R. Srinivasan, J.D. Plummer and S.T. Pantelides, vol. 91-4 (The Electrochem Soc. Inc., Pennington) pp. 254-272 (1991).
- (28) Y. Kim, Y.T. Tan, H.Z. Massoud and R.B. Fair, "Modeling the Enhanced Diffusion of Implanted Boron in Silicon," *ibid* pp. 304-320 (1991).
- (29) R.B. Fair, "Challenges and Priorities for Two Dimensional Process Simulation," *ibid*, pp. 689-702 (1991).
- (30) R.B. Fair and I. Turlik, "Proof-of-Concept Collaboration Model for Advanced Packaging Research at MCNC", 1993 Proceedings, International Conference on Multichip Modules, p.552 (1993).
- (31) R.B. Fair, "Junction Formation in Silicon by RTA," in 1st International Rapid Thermal Processing Conference - RTP'93", Ed. R.B. Fair and B. Lojek, RTP'93, Phoenix , p. 174 (1993).
- (32) M.R. Neuman, R.B. Fair, M. Mehregany and H.Z. Massoud, "Micro-electromechanical Systems: A New Technology for Biomedical Applications," in *Proc. of the 15th Annual Intern. Conf. of the IEEE Engineering in Medicine and Biology Society*, A.Y.J. Szeto and R.M. Rangayyan, eds. IEEE Cat. No. 93CH33339-9, Piscataway, N.J., 15, 1545 (1993).
- (33) R. B. Fair, "Prospects for Ion Implantation in Scaled Devices," in *Proceedings of Inter. Conf. on Adv. Microelectronic Devices and Processing*, Eds. S. Ono, T. Ohmi and Y. Sawada, Sendai, p.689 (1994).

- (34) R.B. Fair. "Physically Based Modeling of Boron Diffusion in Thin Gate Oxides: Effects of F, H<sub>2</sub>, N, Oxide Thickness and Injected Si Interstitials," IEDM Tech Digest, p.85, December, 1995.
- (35) R.B. Fair. "Rapid Thermal Annealing Issues in Silicon Processing" in Transient Thermal Processing Techniques in Electronic Materials, Eds. N.M. Ravindra and R.K. Singh, (The Minerals, Metals and Materials Society, Warrendale, Pa.) p. 91 (1996).
- (36) R.B. Fair and W. Richards, "Process Simulation of Dopant Atom Diffusion in SiO<sub>2</sub>," in Process Physics and Modeling in Semiconductor Technology, eds. G.R. Srinivasan, C.S. Murthy, and S.T. Dunham, vol 96-4 (The Electrochemical Society, Pennington, NJ) pp. 179-194 (1996).
- (37) R.B. Fair, "Boron Diffusion in Ultrathin Silicon Dioxide Layers," in The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface -3, eds. H.Z. Massoud, E.H. Poindexter, and C.R. Helms, vol. 96-1, (The Electrochemical Society, Pennington, NJ) pp. 200-213 (1996).
- (38) G. Chen, T. Borca-Tasciuc, and R. B. Fair. "Fundamental Limit of the Use of Pyrometry in Rapid Thermal Processing," in 4th International Conference on Advanced Thermal Processing of Semiconductors, eds. R.B. Fair, M.L. Green, B. Lojek, and R.P.S Thakur, p. 157 (1996)
- [39] R.B. Fair, "Trends in Rapid Thermal Processing for Large Diameter Silicon Processes," in Proceedings of 2nd International Symp. on Advanced Science and Technology of Silicon Materials, ed. M. Umeno, Japan Soc. for Promotion of Science, pp. 7-15 (1996).
- [40] S. Bobbio, S. Goodwin-Johansson, T. DuBois, F. Tranjan, S. Smith, R. Fair, C. Ball, J. Jacobson, C. Bartlett, N. Eleyan, H. Makki, and R. Gupta, "Integrated force array: positioning drive applications", Proc SPIE Symp, 3046, 248-254 (1997).
- [41] R.B. Fair and M. Shen, "Ultrashallow 2D Dopant Profile Simulation Versus Experimental Measurement in the Low Thermal Budget Regime," Proceedings of Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-shallow Doping Profiles in Semiconductors, Research Triangle Park, NC, April, 1997 pp. 3.1 - 3.9
- [42] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin Gate Dielectrics from B+ Implantation and Thermal Processing," in ULSI Science and Technology 1997, eds. H.Z. Massoud, H. Iwai, C. Claeys, and R.B. Fair (The Electrochemical Society, Pennington, NJ) vol. 97-3, 247-261 (1997).
- [43] R.B. Fair, V. Pamula, and M. Pollack, "MEMS-based Explosive Particle Detection and Remote Particle Stimulation," Proceedings of SPIE - Detection and Remediation Technologies for Mines and Minelike Targets II, vol. 3079, 671 (1997).
- [44] R.B. Fair, "Dopant Diffusion in Si and SiO<sub>2</sub> during RTA," Extended Abstracts of International Conference on Solid State Devices and Materials, SSDM'97, Hamamatsu, Japan, Sept. 1997, p. 104.
- (45) R.B. Fair, M. Pollack, and V. Pamula, "MEMS Devices for Detecting the Presence of Explosive Material Residues in Mine Fields," SPIE Aerosense Conf., Orlando, vol. 3392, 409, April, 1998.
- (46) V.K. Pamula and R.B. Fair, "Detection of Nanogram Explosive Particles with a MEMS Sensor," Proceedings of SPIE, Detection and Remediation Technologies for Mines and Minelike Targets IV, vol. 3710, pp. 321-327 (1999).
- (47) A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," International Conf. Modeling and Simulation of Microsystems, April 1998.

- (47a) V.K. Pamula and R.B. Fair, "Detection of Dissolved TNT and DNT in Soil with a MEMS Explosive Particle Detector," *Proceedings of the SPIE - The International Society for Optical Engineering*, v 4038, pt.1-2, 2000, p 547-52
- (48) T. Zhang, K. Chakrabarty, and R.B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles," *Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems*, p. 148, March, 2001.
- (49) J. Jopling, D. Rose, and R.B. Fair, "The Coupled-Domain System Simulation/Simulatability Problem," *Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems*, p. 116, March, 2001.
- (50) J. Ding, K. Chakrabarty, and R.B. Fair, "Reconfigurable Microfluidic System Architecture Based on Two-Dimensional Electrowetting Arrays," *Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems*, p. 181, March, 2001.
- (51) R.B. Fair, "A Historical View of the Role of Ion-Implantation Defects in PN Junction Formation for Devices," in *Si Front End Processing- Physics and Technology of Dopant-Defect Interactions*, Materials Research Society, vol 610, pp.B4.1.1-12, (2001).
- (52) R. B. Fair, M.G. Pollack, R. Woo, V.K. Pamula, H. Ren, T. Zhang, and J. Venkatraman, "A Microwatt Metal-Insulator-Solution-Transport (MIST) Device for Scalable Digital Bio-Microfluidic Systems," *Technical Digest, Inter. Electron Device Meeting*, pp. 367-370 (2001).
- (53) H. Ren, V. Srinivasan, and R.B. Fair, "Design and Testing of an Interpolating Mixing Architecture for Electrowetting-Based Droplet On-Chip Chemical Dilution," *Digest of Technical Papers Transducers*, 2003, pp. 619-622 (2003).
- (54) R.B. Fair, V. Srinivasan, P. Paik, H. Ren, V.K. Pamula, and M.G. Pollack, "Electrowetting-Based On-Chip Sample Processing for Integrated Microfluidics, IEDM 2003, Washington, DC, December 10, 2003.
- (55) V. Srinivasan, V.K. Pamula, M.K. Pollack, and R.B. Fair, "Clinical diagnostics on human whole blood, plasma, serum, urine, saliva, sweat, and tears on a digital microfluidic platform. *Proceedings of MicroTAS 2003* 1287-1290 (2003)
- (56) V. Srinivasan, V. Pamula, P. Paik, and R.B. Fair, "Protein Stamping for MALDI Mass Spectrometry Using an Electrowetting-Based Microfluidic Platform," in *Lab-on-a-Chip: Platforms, Devices, and Applications*, L.A. Smith and D. Sobek, eds., *Proc. Of SPIE*, vol. 5591, pp. 26-34, Dec. 8, 2004.
- (57) R.B. Fair, A. Khlystov, V. Srinivasan, V.K. Pamula, K.N. Weaver, "Integrated Chemical/Biochemical Sample Collection, Pre-concentration, and Analysis on a Digital Microfluidic Lab-on-a-Chip Platform," in *Lab-on-a-Chip: Platforms, Devices, and Applications*, L.A. Smith and D. Sobek, eds., *Proc. Of SPIE*, vol. 5591, pp. 113-124, Dec. 8, 2004.
- (58) V.K. Pamula, V. Srinivasan, H. Chakrapani, R.B. Fair, and E.J. Toon, "A Droplet-Based Lab-On-A-Chip for Coplorimetric Detection of Nitroaromatic Explosives," *Proceedings of IEEE Inter. Conference on Micro Electro Mechanical Systems (MEMS 2005)*, pp. 722-725, (2005)
- (59) R. Evans, L. Luan, N.M. Jokerst, and R.B. Fair, "Optical detection heterogeneously integrated with a coplanar digital microfluidic lab-on-a-chip platform," *6<sup>th</sup> IEEE Conf. Sensors, IEEE Sensors 2007*, Atlanta, GA, Oct.28, 2007.
- (60) C. Geisler, D.M. Wootton, P.I. Lelkes, R.B. Fair, and J.G. Zhou, "Material study of electrowetting-based multimicrofluidics array printing of high resolution tissue construct with embedded cells and growth factors," *ASME 2010 First Global Congress NanoEngineering for Medicine and Biology*, Houston, TX, Feb. 7-10, 2010.

- (61) R.B. Fair, "Parallel Processing of Multifunctional, Point-of-Care Bio-Applications on Electrowetting Chips,  $\mu$ TAS 2010, Oct. 3-7 (2010), pp. 2095-2097.
- (62) M.W. Royal, R.B. Fair, and N.M. Jokerst, "Integrated sample preparation and sensing: Microresonator optical sensors embedded in digital electrowetting microfluidics systems," *IEEE Sensors*, p. 4 (2011)
- (63) B. -N. Hsu, A. C. Madison and R. B. Fair "Accelerate Sepsis Diagnosis by Seamless Integration of DNA Purification and qPCR," *Proceedings of the 16th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2012)*, Okinawa, Japan, October 28-November 1, 2012, pp. 830-832.

### **BOOK CHAPTERS**

- (1) R. B. Fair, "Concentration Profiles of Diffused Dopants in Silicon," in *Impurity Doping Processes in Silicon*, Ed. by F. Y. Want in the series *Material Processing: Theory and Practices*, North Holland Press, Amsterdam (1981) pp. 317-442.
- (2) R. B. Fair, "Physics and Chemistry of Impurity Diffusion and Oxidation of Silicon," in *Processing Technologies*, Ed. D. Khang in *Applied Solid State Science*, Academic Press, New York (1981), Supplement 2B, pp. 1-108.
- (3) R. B. Fair, "Diffusion in Silicon," in *Advances in Electronic Materials*, Ed. by B. W. Wessels and G. Y. Chin, American Society for Metals, Metals Park, Ohio (1986) pp. 119-145.
- (4) R.B. Fair, "Diffusion and Ion Implantation in Silicon," in *Semiconductor Materials and Process Technology Handbook*, Ed. G.E. McGuire, Noyes Publication (1988), pp. 455-538.
- (5) R.B. Fair, "Diffusion and Oxidation of Silicon," Eds. K.F. Jensen and D. Hess, American Chemical Society-Advances in Chemistry Series No. 221, Wash, D.C. (1989).
- (6) R.B. Fair, "Diffusion in Silicon," Ed. L.C. Kimerling, *Concise Encyclopedia of Electronic and Optoelectronic Materials*, (Pergamon Press, Oxford) Suppl. Vol. 2, pp. 901-904, 1990.
- [7] R.B. Fair, "Junction Formation in Silicon by Rapid Thermal Annealing", in *Rapid Thermal Processing: Science and Technology*, Ed. R.B. Fair, (Academic Press, Boston), pp. 169-226, 1993.
- [8] R.B. Fair, "Rapid Thermal Processing - A Justification", in *Rapid Thermal Processing: Science and Technology*, Ed. R.B. Fair, (Academic Press, Boston), pp. 1-11, 1993.
- (9) R.B. Fair, "Conventional and Rapid Thermal Processing," in *ULSI Technology*, Ed. C.Y. Chang and S.M. Sze (McGraw Hill, New York), pp. 144-204, 1996.
- (10) R.B. Fair, "Doping," Ed. J.D. Atwood, *Inorganic Reactions and Methods*, Sections 17.2.6-17.2.6.5, John Wiley & Sons, New York (1999)
- (11) T. Zhang, K. Chakrabarty, R.B. Fair, "A Hierarchical Design Platform for Microelectrofluidic Systems," Vol. 1, *MEMS/NEMS Handbook*, Ed. L. Cornelius (Springer), 2006.
- (12) R.B. Fair, "Scaling Fundamentals and Applications of Digital Microfluidic Microsystems," in *Microfluidics Based Microsystems*, Ed. S. Kakac, B. Kosoy, D. Li, and A. Pramuanjaroenkij (Springer), pp. 285-304 (2010).



## BOOKS EDITED/WRITTEN

- [1] "Impurity Diffusion and Gettering in Silicon," Materials Research Society Symposia Proceedings, Vol. 36, Eds. Richard B. Fair, Charles W. Pearce and Jack Washburn, Materials Research society, Pittsburgh, PA., (1985).
- [2] "Rapid Thermal Processing: Science and Technology", Ed. R.B. Fair, Academic Press, Boston, (1993).
- (3) "1st International Rapid Thermal Processing Conference - RTP'93", Ed. R.B. Fair and B. Lojek, RTP'93, Phoenix (1993)
- (4) "2nd International Rapid Thermal Processing Conference - RTP'94", Ed. R.B. Fair and B. Lojek, RTP'94, Monterey (1994)
- (5) "3rd International Rapid Thermal Processing Conference - RTP'95", Ed. R.B. Fair and B. Lojek, RTP'95, Amsterdam (1995)
- (6) "4th International Conference on Advanced Thermal Processing of Semiconductors - RTP'96", Ed. R.B. Fair, M.L. Green, B. Lojek, and R.P.S. Thakur, RTP'96, Boise (1996)
- (7) "ULSI Science and Technology 1997", Eds. H.Z. Massoud, H. Iwai, C. Claeys, and R.B. Fair (The Electrochemical Society, Pennington, NJ) vol. 97-3, Montreal (1997)
- (8) "5th International Conference on Advanced Thermal Processing of Semiconductors - RTP'97", Ed. R.B. Fair, M.L. Green, B. Lojek, and R.P.S. Thakur, RTP'97, New Orleans (1997)
- (9) "Microelectrofluidic Systems – Modeling and Simulation," CRC Press, Boca Raton, (2002).

## INVITED LECTURES/TALKS

- (1) "Transistor Design Considerations in Low-Noise Pre-Amplifiers," IEEE Nuclear Science Symposium, San Francisco (1975).
- (2) "Recent Advances in Implantation and Device Modeling for the Design and Process Control of Bipolar IC's," Electrochemical Society Meeting, Philadelphia (1977).
- (3) "Some New Insights into Process Modeling," Nat. Bureau of Standards, Washington, DC (1978).
- (4) "Recent Developments in Process Modeling," Stanford University Seminar, Stanford (1979).
- (5) "Thermal and Laser-Induced Diffusion of Dopants in Silicon," Sandia Laboratories Seminar, Albuquerque (1979).
- (6) "The Multiple-Charge State Vacancy Model for Impurity Diffusion in Silicon," Gordon Research Conf., Meriden, NH (1979).
- (7) "Impurity Diffusion in Silicon - The Long and the Short of It," ECS Society Lecture, North Texas Section, Dallas (1979).
- (8) "Point Defects and Diffusion in Silicon - The Current Controversies," Stanford University Seminar (1979).
- (9) "The Multiple-Charge-State Vacancy Model of Diffusion," Electrochemical Society Meeting, St. Louis (1980).
- (10) "Molecular Transport and Diffusion in Solids:, NATO Advanced Study Institute on Chemical Sensors," Hightstown, NJ (1980).
- (11) "A Consistent Model of Oxidation, Impurity Diffusion and Defect Growth in Silicon," Electronic Materials Conf., Cornell (1980).
- (12) "Diffusion in Silicon," Seminar at Texas Instruments, Inc., Dallas (1980).

- (13) "LSI Research Areas - Peeling the IC Technology Onion," Duke University, Durham, NC (1980).
- (14) "The Role of H<sub>2</sub> in SiO<sub>2</sub> on Integrated Circuit Reliability," Penn State University, State College, PA (1980).
- (15) "LSI Research Areas," Howard University, Washington, DC (Nov. 1980).
- (16) "LSI Research Areas - Peeling the IC Technology Onion," Western Electric, Merimack Valley, April 1981.
- (17) "Limitations and Benefits of Standard High Temperature processing in Producing Device Quality Silicon Surface Layers," Lasers in Microelectronics Workshop, MIT, Boston, May 1981.
- (18) "Modeling Anomalous Phenomena in Arsenic Diffusion in Silicon," Electrochemical Society Meeting, Minneapolis, MN, May 1981.
- (19) "The Role of the Microelectronics Center of North Carolina in University Research," Sigma Xi Lecture, North Carolina A&T State University, Greensboro, NC, Nov. 1981.
- (20) "Anomalous Junctions Formed by Cross-Contamination of Phosphorus During Arsenic Implantation in Silicon," Symposium on Silicon Processing, San Jose, CA., Jan. 1982.
- (21) "Materials Research Areas in Silicon Technology," North Carolina State University, Raleigh, NC, 1981.
- (22) "The Impact of Defects and Diffusion on Integrated Circuit Technology," North Carolina State University, Raleigh, NC, 1982.
- (23) "Impurity Diffusion in Silicon-Key to the VLSI Process Balancing Act," SIA Lecture at Stanford University, Stanford, CA, 1982.
- (24) "Developments in Microelectronics: Science and Industry," East Carolina University, Greenville, NC, 1982.
- (25) "Modeling of Dopant Diffusion and Associated Effects in Si," Materials Research Society, Boston, 1982.
- (26) "Research Interests and Goals of the Microelectronics Center of North Carolina," University of North Carolina, Chapel Hill, 1982.
- (27) "The Microelectronics Center - A New Force in Cooperative VLSI Signal Processing Research," University of Southern California, Los Angeles, 1982.
- (28) "Point Defects in Silicon," Katholieke University, Leuven Belgium, 1983.
- (29) "Impurity Concentration Doping Effects on Impurity Diffusion in Silicon," Semicon/Europa '83, Zurich, Switzerland, 1983.
- (30) "The Future of Microelectronics in North Carolina," ORT Seminar, Raleigh, 1983.
- (31) "An Overview of Technology Requirements for VLSI," Computer Science Seminar, NASA Langley Research Center, Hampton, Va., 1983.
- (32) "MCNC - A New Multi-Institutional Thrust in Manufacturing Technology Research," 5th University/Government/Industry Microelectronics Symposium, College Station, Texas, 1983.
- (33) "The Evolution of Digital Integrated Circuit Technologies," Keynote speech at Digital Integrated Circuits Workshop, John Wiley & Sons, Durham, N.C. 1983.
- (34) "Scaling of Junctions for CMOS," Symposium on Computer-Aided Design and Manufacturing of Integrated Circuits, Stanford University, 1983.
- (35) "Limitations in Scaling Junctions for CMOS," Burroughs Corp., San Diego, 1983.
- (36) "The Role of the Microelectronics Center of North Carolina in Industrial Development of North Carolina," keynote talk, Quality in Electronics Conference, Raleigh, N. C., 1983.
- (37) "The Role of Vacancies and Self-Interstitials in Impurity-Diffusion in Silicon," Indo./U.S. Workshop on Diffusion in Solids, Bombay, India, 1984.

- (38) "The Formation of Fixed Charge and Interface States During Hot Carrier Injection in MOSFET's," DEC, Hudson, Massachusetts, 1984.
- (39) "Cooperative Research at MCNC," Third Symposium on Semiconductor Processing, San Jose, California, 1984.
- (40) "The Role of Point Defects in Processing Phenomena in Silicon," Monsanto Corporation, St. Louis, 1984.
- (41) "Modeling Rapid Thermal Diffusion of Dopants in Silicon," Semiconductor Seminar, Research Triangle Park, 1984.
- (42) "Modeling Rapid Thermal Diffusion of Dopants in Silicon," Microelectronics Seminar Series, UNCC, Charlotte, N.C., 1984.
- (43) "Observations of Vacancies and Self-Interstitials in Diffusion Experiments in Silicon," International Conference on Defects in Semiconductors, San Diego, CA, 1984.
- (44) "Silicon Diffusion," Materials Science Seminar for American Society of Metals, Detroit, 1985.
- (45) "Microelectronics in North Carolina," Luncheon speaker to ASTM Committee F-1, Raleigh, 1984.
- (46) "Impurity Diffusion During RTA," Materials Research Society Meeting, Boston, 1984.
- (47) "PREDICT\_\_A New Design Tool for Shallow Junction Processes," SPIE Meeting on Advanced Applications of Ion Implantation, Los Angeles, 1985.
- (48) "The Self-Interstitial Versus Vacancy Debate in Silicon-Coincidences, Convictions and Controversies," Gordon Research Conference on Point Defects, Line Defects and Interfaces in Semiconductors, Plymouth, NH, 1985.
- (49) "On the Role of Rapid-Thermal Processing Scaled CMOS," Canadian VLSI Conference, Toronto, 1985.
- (50) "Process Modeling" - IEDM Short Course, Washington, D.C., 1985.
- (51) "Shallow Junction Technology for Sealed CMOS," SRC Topical Research Conference, Cornell University, Ithaca, 1985.
- (52) "New Results on Point Defects in Silicon," Seminar at Katholieke University, Leuven Belgium, 1985.
- (53) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1985.
- (54) "Diffusion Simulation," MCC Workshop on Process and Device Simulation, Austin, Texas, 1986.
- (55) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1986.
- (56) "Modeling Low Thermal Budget Silicon Processing - The Long and the Short of it," RPI, Troy, NY, 1986.
- (57) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1987- 1992.
- (58) "The Future of Ion Implantation," R. B. Fair, Greater Silicon Valley Implant User's Group, San Jose (1987).
- (59) "Pitfalls of Low-Thermal Budget Processing," Sematech Workshop, Denver (1987).
- (60) "Pitfalls of Low-Thermal Budget Processing," Hewlett-Packard, Fort Collins (1987).
- (61) "Process Models for Ultra-Shallow Junction Technologies," Digital Equip. Corp. Seminar, Hudson, MA (1988).

- (62) "Challenges for Submicron Silicon Processing," Fifth International Sym. on Semiconductor Processing, Santa Clara, CA (1988).
- (63) "Rapid Thermal Processing Issues in the Manufacturing of Semiconductor Devices," S.P.I.E. Conf. on Advanced Processing of Semiconductor Devices II, Newport Beach, CA (1988).
- (64) "Oxidation-Induced defects in Low-Thermal Budget Silicon Processing," Electrochemical Society Meeting, Atlanta, Georgia, May 1988.
- (65) "The Role of Transient Damage Annealing Shallow-Junction Formation," Electrochemical Society Meeting, Atlanta, Georgia, May 1988.
- (66) "Rapid Thermal Annealing of Low Energy Implants in Silicon," Shanghai Workshop on Characterization of Ion Implantation in Silicon, Hangzhou, China, June 1988.
- (67) "The Impact of Computing Technology on Design," The Technology Exchange Institute for Engineering Deans", Stanford Univ., Oct. 1988.
- (68) "VLSI Research Program at MCNC," 1989 VLSI Group Research Review, Univ. of Waterloo, May 1989.
- (69) "Phenomenological vs. Point-Defect-Based Modeling-Where Should You Put Your Money?" Electrochem. Soc. Meeting, Los Angeles, May 1989.
- (70) "Challenges and Priorities for Two-Dimensional Process Simulation," Electrochem. Soc. Mtg., Montreal, May 1990.
- (71) "Transient Diffusion in Silicon: Models and Cures," Electronics Materials Conf., Santa Barbara, CA, June 1990.
- (72) "Thermal Budget Issues for Submicron ULSI," Oregon Graduate Institute for Science and Technology, Beaverton, Nov. 1990.
- (73) "Damage Removal-Diffusion Tradeoffs in Ultra-Shallow Implanted p+ Junctions," Motorola Process Modeling Workshop, Mesa, Nov. 1990.
- (74) "A Unified View of Modeling Transient Dopant Diffusion in Silicon," Inter. Workshop on VLSI Process and Device Modeling, Oiso, Japan, May 1991.
- (75) "Defects Induced in Silicon During Ion Implantation and Rapid Thermal Annealing," Electrochem Soc. Meeting, Washington, DC, May 1991.
- (76) "Computer-Aided Process Modeling and Simulation," Silicon Processing for the VLSI Era, RTP, May 17, 1991.
- (77) "Process Simulation for ULSI - Tools, Models and Issues," ASIC Technology Seminar, Kawasaki Japan, September 1991.
- (78) "Process Simulation for ULSI," Teksel Seminar, Osaka, Japan, September 1991.
- (79) "Process Simulation for ULSI," Intellect, Inc. Seminar, Seoul, Korea, September 1991.
- (80) "Process Simulation for ULSI," Exartech Inter. Seminar, Hsinchu, Taiwan, October 1991.
- [81] "Challenges in Manufacturing ULSI Devices", SPE Regional Tech. Conf., Research Triangle Park, Nov. 1991.
- [82] "Defects in Silicon Induced by Ion Implantation" Symp. on Adv. Science and Tech. of Si Materials, Japan Soc. for Promotion of Science, Kona, Hawaii, Nov. 1991.
- [83] "The Role of Consortia in the Development of Materials and Processing Alternatives for Advanced Microelectronics", ISHM Workshop, Ojai, CA, Feb. 1992.
- [84] "Defects, Diffusion and Debacles in Shallow pn Junction Formation", AT&T Bell Labs, Murray Hill, N.J., March 1992.

- [85] "The Semiconductor Manufacturing Crisis - Opportunity for Global Cooperation?", Keynote speech, ISSMT'92 Conf., Tokyo, May 1992.
- [86] "Rapid Thermal Processing - Science and Technology", all seminars, May 1992, Kawasaki, Japan, Science Park, Hsingchu, Taiwan, Yonsei Univ., Seoul, Korea.
- [87] "Consortia - Help or Hindrance?", ISHM '92 Meeting, San Francisco, CA, October, 1992
- [88] "Junction Formation in Silicon by Rapid Thermal Annealing", Materials Research Society, San Francisco, CA, April, 1993
- [89] "Proof-of-Concept Collaboration Model for Advanced Packaging Research at MCNC", 2nd Inter. Conf. on Multichip Modules, Denver, April, 1993
- (90) "Rapid Thermal Processing," Seminar at SEMI, Mountain View Ca., July, 1993.
- (91) "Junction Formation in Silicon by RTA", 1st International Rapid Thermal Processing Conference, RTP'93, Phoenix, Az, Sept. 1993.
- (92) "Prospects for Ion Implantation in Scaled Devices," Conference on Advanced Microelectronic Devices and Processing, Sendai, Japan, March, 1994.
- (93) "Advances in Microchip Technology - Hitting the Wall in the Microchip Marathon," 8th Annual High Performance Computing and Communications Conference, FGIPC, Research Triangle Park, NC, June, 1994.
- (94) "Rapid Thermal Processing - Hot Solution for a Critical Processing Need?" Distinguished Lecture, Micron Technology, Inc., Boise ID, June 1995.
- (95) "Rapid Thermal Annealing Issues in Silicon Processing," 125th TMS Annual Meeting, Anaheim, CA, Feb. 1996.
- (96) "Modeling the Diffusion Barrier Role of Nitrogen in Ultrathin Gate Oxides," SRC Topical Research Conference on Ultrathin Gate Dielectrics Technology, Reliability, and Characterization, Raleigh, NC, March, 1996.
- (97) "Boron Diffusion in Ultrathin Silicon Dioxide Layers," in The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface -3 Symposium, Spring meeting of the Electrochemical Society, Los Angeles (1996).
- (98) "Ion Implantation and Annealing Technologies," Cambridge University, England June 1996.
- (99) "PREDICTive Process Simulation for the Non-Stanford Graduate Engineer," Computer-Aided Design of IC Processes and Devices Workshop, Stanford University, August, 1996.
- [100] "Trend of Rapid Thermal Processing in Large Diameter Silicon Processes," Plenary talk, 2nd International Symposium on Advanced Science and Technology of Silicon Materials, November 25-29, Kona, Hawaii (1996).
- [101] "Ultrashallow 2D Dopant Profile Simulation Versus Experimental Measurement in the Low Thermal Budget Regime," Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-shallow Doping Profiles in Semiconductors, Research Triangle Park, NC, April, 1997.
- [102] "MEMS Trace Particle, Vapor and Ultrasound Sensor," Aerosense Conference 3079, SPIE, Orlando, FL, April 24, 1997
- [103] "MEMS Trace Particle, Vapor and Ultrasound Sensor," Oak Ridge National Labs, May 12, 1997
- [104] "Dopant Diffusion in Si and SiO<sub>2</sub> During Rapid Thermal Annealing," Solid State Devices and Materials - SSDM'97, Hamamatsu, Japan, Sept., 1997.
- [105] "Activation of Ion Implanted Dopants in Silicon with Optical Radiation," Gordon Research Conf. on Materials Processes Far from Equilibrium, Meriden, NH., Aug. 1997.

- [106] "Dopant Diffusion in Si and SiO<sub>2</sub> during RTA," International Conference on Solid State Devices and Materials, SSDM'97, Hamamatsu, Japan, Sept. 1997.
- [107] "Sniffing Out Landmines: Mimicing Man's Best Friend," IEEE New Technology Directions Committee Workshop, Atlanta, Georgia, Nov. 1997.
- [108] "Advances in Silicon Technology- Hitting the Wall in the Microchip Marathon," keynote talk at 2nd Southeastern Workshop on Mixed-Signal VLSI and Monolithic Sensors," Knoxville, April, 1998.
- [109] A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," Int. Conf. on Modeling and Simulation of Microsystems, Semiconductors, Sensors, and Actuators, MSM98, April, 1998.
- [110] R.B. Fair, "PN Junction Profile Engineering," Short course at USJ'99, Research Triangle Park, March, 1999.
- [111] R.B. Fair, "A Historical View of the Role of Ion-Implantation Defects in PN Junction Formation for Devices," Materials Research Society, San Francisco, April, 2000.
- [112] R.B. Fair, "The Invention of the Self-Aligned Gate MOSFET," N.C. Section of the Materials Research Society, Research Triangle Park, Nov. 10, 2000.
- [113] R.B. Fair, "Research in Biochips and BioFLIPS," Workshop on Biomedical Imaging and Bioengineering Opportunities, N.C. State University, May 10, 2001.
- [114] R.B. Fair, "Advances in Droplet-Based Bio Lab-on-a-Chip," BioChips 2003, Boston, June, 2003.
- [115] R.B. Fair, A. Khlystov, V. Srinivasan, V. K. Pamula, K.N. Weaver, "Integrated chemical/biochemical sample collection, pre-concentration, and analysis on a digital microfluidic lab-on-a-chip platform," Lab-on-a-Chip: Platforms, Devices, and Applications, Conf. 5591, SPIE Optics East, Philadelphia, Oct. 25-28, 2004.
- [116] R.B. Fair, "Dynamically Reconfigurable Surfaces for Microfluidic Applications," MRS Spring Meeting, San Francisco, CA., Symp. Q, March 29, 2005.
- [117] R.B. Fair, V. Srinivasan, N. Weaver, "Bead-Based and Solution-Based Assays Performed on a Digital Microfluidic Platform," BMES 2005, Baltimore, MD, Oct. 1, 2005.
- [118] R.B. Fair, "Chemical and Biological Applications of Digital Microfluidic Devices," 5<sup>th</sup> Inter. Meeting on Electrowetting, Rochester, NY, June 1, 2006.
- [119] R.B. Fair, "Chemical and Biological Pathogen Detection in a Digital Microfluidic Platform," DARPA/MTO Workshop Microfluidic Analyzers, Keystone, CO, Oct. 4-5, 2006.
- [120] R.B. Fair, "Integrated Digital Microfluidic Functions for Chemical and Biological Applications", Materials Research Society Meeting, San Francisco, CA April 13, 2007.
- [121] R.B. Fair, "Integrated Digital Microfluidic Chips for Chemical and Biological Applications," Drexel University, Philadelphia, PA May 16, 2007.
- [122] R.B. Fair, "Digital Microfluidic Biochips," Materials Research Society, Boston, Nov. 27, 2007.
- [123] R.B. Fair, "Reconfigurable digital microfluidic chips for multiple chemical applications", American Chemical Society, Philadelphia, Aug. 20, 2008
- [124] R.B. Fair, J.H. Song, R.D. Evans, Y-T Lin, B-N Hsu, "Scaling EWD Actuators for Picoliter Applications," 6<sup>th</sup> Inter. Meeting on Electrowetting, Los Angeles, Aug. 21, 2008.
- [125] R.B. Fair, "Progress in Reconfigurable Microfluidic Systems for Evolvable Biochips," 8<sup>th</sup> International Conf. Evolvable Systems, Prague, Sept. 21, 2008. (Keynote)
- [126] R.B. Fair, "Is a True Lab-on-a-Chip Possible?," Bioengineering Applications to Address Global Health, Duke Univ., Durham, NC, Nov. 6, 2008.

- [127] R.B. Fair, "The \$1000 Genome: Sequencing DNA One Drop at a Time." Microfluidics Symposium, Harvard Medical School, January 15, 2009.
- [128] R.B. Fair, "Fundamentals of Droplet Flow in Microfluidics," NATO Advanced Study Institute on *Microsystems for Security – Fundamentals and Applications* – August 23 – September 4, 2009, Golden Dolphin Hotel, Cesme-Izmir, Turkey
- [129] R.B. Fair, "Implementation of Fluidic Functions in Digital Microfluidics," NATO Advanced Study Institute on *Microsystems for Security – Fundamentals and Applications* – August 23 – September 4, 2009, Golden Dolphin Hotel, Cesme-Izmir, Turkey
- [130] R.B. Fair, "Digital Microfluidics for Chemical and Biological Applications," 31st Annual International IEEE EMBS Conference, Minneapolis, Minnesota, USA, September, 2-6, 2009.
- [131] R.B. Fair, "Electrowetting Control of Droplets for On-chip Biomedical Applications," APS Mtg., Portland, OR, March 2010.
- [132] R.B. Fair, "Parallel Processing of Multifunctional, Point-of-Care Bio-Applications on Electrowetting Chips,  $\mu$ TAS 2010, Oct. 3-7 (2010), Groningen, The Netherlands.
- [133] N. M. Jokerst, M. Royal, S. Dhar, M. Brooke, R. Fair, T. Tyler, D. Arora, "Intergated Optical Sensing Ssystems: Sensors, Photonics, and Fluidics," Europtrode XI, Barcelona, April, 2012.
- [134] R.B. Fair, "Portable Digital Microfluidic LoCs with Integrated Analog Processing, Adaptive Control, and Sensing," IARPA Workshop, Bedford, MA, Oct. 10, 2012.

### OTHER TALKS AND LECTURES

- (1) "A Machine-Scan Electron Beam Device," 8th Annual Electron and Laser Beam Symposium, University of Michigan, Ann Arbor (1966).
- (2) "High Concentration Arsenic Diffusion in Silicon from Doped Oxide Sources," Electrochemical Society Meeting, Houston (1972).
- (3) "Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," Inter. Electron Device Meeting of IEEE, Washington, DC (1972).
- (4) "Diffusion of Ion-Implanted Boron in High Concentration P, As and Sb-doped Silicon," Electrochemical Society Meeting, Toronto (1975).
- (5) "The Diffusion of Ion-Implanted Arsenic in Silicon," Electrochemical Society Meeting, Dallas (1975).
- (6) "Zener and Avalanche Breakdown in As-Implanted Low Voltage Si N-P Junctions," Inter. Electron Device Meeting of IEEE, Washington, DC (1975).
- (7) "Quantitative Model of Phosphorus Diffusion in Silicon," Electrochemical Society Meeting, Las Vegas (1976).
- (8) "Quantitative Model of the Emitter-Dip Effect," Electrochemical Society Meeting, Las Vegas (1976).
- (9) "Analysis of Phosphorus Profiles," Electrochemical Society Meeting, Atlanta (1977).
- (10) "The Effect of Strain-Induced Bandgap Narrowing on Phosphorus Diffusion and E-Center Concentrations in Silicon," Inter. Conf. on Defects and Radiation Effects in Semicond., Nice (1978).
- (11) "Theory and Direct Measurement of Boron Segregation in SiO<sub>2</sub> During Dry, Near Dry and Wet O<sub>2</sub> Oxidation," Electrochemical Society Meeting, Pittsburgh (1978).
- (12) "Modeling Laser - Induced Diffusion of Implanted Arsenic in Silicon," Electrochemical Society Meeting, Los Angeles (1979).

- (13) "Influence of Strain on Impurity Diffusion in Silicon," Electrochemical Society Meeting, St. Louis (1980).
- (14) "Threshold Voltage Instability in MOSFET's Due to Channel Hot Hole Emission," Inter. Electron Device Meeting, Washington, DC (1980).
- (15) "The Effects of Impurity Diffusion and Surface Damage on Oxygen Precipitation in Silicon," Electrochemical Society Meeting, Montreal (1982).
- (16) "Dynamic Behavior of the Build-Up of Fixed Charge and Interface States During Hot Carrier Injection in Encapsulated MOSFET's," Electrochemical Society Meeting, Montreal (1982).
- (17) "Modeling Physical Limitations on Junction Scaling for CMOS," Device Research Conference, Burlington, VT (1983).
- (18) "Modeling Rapid Thermal Annealing Processes for Shallow Junction Formation in Silicon," International Electron Device Meeting, Washington, DC (1983).
- (19) "Computer Simulation of Oxygen Precipitation and Denuded Zone Formation," Electrochemical Society Meeting, Cincinnati, OH (1984).
- (20) "Stress Assisted Diffusion of Boron and Arsenic in Silicon," Materials Research Society Meeting, Boston, November 1984.
- (21) "Curve Fitting Models for Boron, Phosphorus and Arsenic Ion Implantations in Crystalline Silicon," Electrochemical Society Meeting, Toronto, Canada (1985).
- (22) "Shallow p+/n Junction Formation for CMOS VLSI Application Using Germanium Preamorphization," 43rd Device Research Conf., Boulder, CO, 1985.
- (23) "Point Defect Generation During Phosphorus Diffusion in Silicon," Electronic Materials Conf., Boulder, CO, 1985.
- (24) "Integrated Circuit Process Design Using a Hardwired Simulator" - PREDICT , NUPAD, Santa Clara, CA 1986.
- (25) "Point Defect Kinetics During Backside Oxidation Measured by Frontside Stacking Fault Growth," B. Rogers, H. Z. Massoud, R. B. Fair, U. M. Gosele, R. Shaw, H. Korb and M. Guse, Electrochem. Soc. Spring Meeting, Phila. (1987).
- (26) "Characterization and Modeling of the Diffusion of B and As in Si in Dry O<sub>2</sub>/HCl Mixtures," R. Subrahmanyam, H. Z. Massoud and R. B. Fair, Electrochem. Soc. Spring Meeting, Phila. (1987).
- (27) "A Deep Decision Tree Approach to Modeling Submicron Silicon Technologies," R. B. Fair and J. E. Rose, ICCAD, San Jose, (1987).
- (28) "Process Models for Ultra-Shallow Junction Technologies," R. B. Fair, IEDM, Wash., DC, 1987.
- (29) "Accurate Junction-Depth Measurements Using Chemical Staining," R. Subrahmanyam, H. Z. Massoud and R. B. Fair, Fifth International Conference on Silicon Processing, Santa Clara, CA, 1988.
- (30) "On the Role of Ion Implantation Damage in Silicon on Dopant Diffusion for Shallow Junction Formation," Y. Kim, R. B. Fair and H. Z. Massoud, Electronic Mater. Conf., Boulder, CO, June 1988.
- (31) "Two Dimensional Modeling of Implant Damage Effects on Impurity Diffusion," R. B. Fair, C. Gardner, M. Johnson, S. Kenkel, D. Rose, J. Rose, R. Subrahmanyam, Workshop on Num. Modeling of Processes and Devices for Integrated Circuits, San Diego, May 1988.



- (32) "A Comparison of Low Energy BF<sub>2</sub> Implantation in Si and Ge Preamorphized Silicon," G.A. Ruggles, S. Hong, J.J. Wortman, M. Ozturk, E.R. Myers, J.J. Hren and R.B. Fair, Materials Research Society Mtg., Boston, Nov. 1988.
- (33) "Modeling the Time Constant for Transient Diffusion Enhancement of Ion-Implanted Dopants in Silicon," Y. Kim, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
- (34) "Modeling the Oxidation of Heavily Doped Silicon in the Thin Regime," R. Ward, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
- (35) "Comparison of Measured and Simulated Two Dimensional P Profiles in Si," R. Subrahmanyam, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
- (36) "A Strategy for 2D Process Simulation," R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
- (37) "Shallow-Junctions-Modeling the Dominance of Point Defect Charge States During Transient Diffusion," IEDM, Wash., D.C., Dec. 1989.
- (38) "Technology Transfer at MCNC," SRC Workshop, Melbourne, FL, March, 1990.
- (39) "Physical Modeling of the Time Constant of the Transient Enhancement in Diffusion of Ion-implanted Dopants in Silicon," Y. Kim, H.Z. Massoud, U. Gosele and R.B. Fair, Electrochem. Soc. Meeting, Montreal, May 1990.
- (40) "Modeling The Enhanced Diffusion of Implanted Boron in Silicon," Y. Kim, T.Y. Tan, H.Z. Massoud and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
- (41) "The Thermal Oxidation of Heavily Doped Silicon in the Thin-Film Regime: Dopant Behavior and Modeling Growth Kinetics," R.R. Ward, H.Z. Massoud and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
- (42) "The Effect of Amorphizing Implants on Phosphorus Diffusion in Silicon," R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
- (43) "The Role of End-of-Range Dislocation Loops as a Diffusion Barrier," Y. Kim, H.Z. Massoud, S. Chevacharoeukul and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
- (44) "Technology Transfer Utilizing the Proof-of-Concept Facility," R.B. Fair and J.F. Freedman, Adv. Semicond. Manuf. Conf. & Workshop, Boston, October 1991.
- (45) "Spinoff Strategy for University-Based Applications Effort in Microsystems," Engineering Foundation Conference on Commercialization of Microsystems, Banff, Canada, Sept. 1994.
- (46) "Physically Based Modeling of Boron Diffusion in Thin Gate Oxides: Effects of F, H<sub>2</sub>, N, Oxide Thickness and Injected Si Interstitials," IEDM, Wash. DC, December, 1995.
- (47) "Process Simulation of Dopant Atom Diffusion in SiO<sub>2</sub>," in Process Physics and Modeling in Semiconductor Technology Symposium, Spring meeting of the Electrochemical Society, Los Angeles (1996).
- (48) G. Chen, T. Borca-Tasciuc, and R. B. Fair "Fundamental Limit of the Use of Pyrometry in Rapid Thermal Processing," in RTP'96, Boise, ID, Sept. 1996.
- [49] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin gate Dielectrics from B+ Implantation and Thermal Processing," Electrochemical Society Meeting, Montreal, May 6, 1997
- [50] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin Gate Dielectrics from B+ Implantation and Thermal Processing," Spring Meeting, Electrochemical Soc., Montreal, May, 1997.

- [51] T.W. Tsuei, R.L. Wood, C.K. Malek, M.M. Donnelly, and R.B. Fair, "Tapered Microvalves Fabricated by Off-Axis X-ray Exposures," HARMST 97
- (52) R.B. Fair, M. Pollack, and V. Pamula, "MEMS Devices for Detecting the presence of Explosive Material Residues in Mine Fields," SPIE Aerosense Conf., Orlando, vol. 3392, 409, April, 1998.
- (53) J.M. Zara, S. Bobbio, R. Fair, S. Goodwin-Johansson, and S.W. Smith, "A Forward Looking Intracardiac Ultrasound Scanner Using MEMS Technology," ONR Transducer Materials and Transducers Workshop, State College, PA, May, 1998.
- (54) Y. Wu, H. Niimi, H. Yang, G. Lucovsky, and R. Fair, "Microscopic Model for Boron-Atom Penetration Through Silicon Dioxide and Suppression of Boron Transport Through Silicon Nitride," 29th IEEE Semiconductor Interface Specialists Conference, San Diego, Dec., 1998.
- (55) V.K. Pamula and R.B. Fair, "Detection of Explosive Residues with a MEMS Sensor," SPIE Aerosense Conf., Orlando, April, 1999.
- (56) A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," International Conf. Modeling and Simulation of Microsystems, April 1998.
- (57) A. Dewey, R. Fair, J. Jopling, T. Zhang, F. Cao, B. Schreiner, and M. Pollack, "Towards Microfluidic System (MEFS) Computing Architecture," Third Inter. Conf. on Modeling and Simulation of Microsystems, San Diego, Mar. 27-29, 2000.
- (58) V.K. Pamula and R.B. Fair, "Detection of Dissolved TNT and DNT in Soil with a MEMS Explosive Particle Detector," SPIE Aerosense Conf., Orlando, April, 2000.
- (59) T. Zhang, K. Chakrabarty, and R.B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles," International Conf. Modeling and Simulation of Microsystems, March, 2001.
- (60) H. Ren, A. Jog, and R.B. Fair, "Statistical Optimal Design of Microelectromechanical Systems (MEMS)," 4<sup>th</sup> Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
- (61) J. Jopling, D. Rose, and R.B. Fair, "The Coupled-Domain System Simulation/Simulatability Problem," 4<sup>th</sup> Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
- (62) V.K. Pamula, A. Jog, and R.B. Fair, "Mechanical Property Measurement of Thin-Film Gold using Thermally Actuated Bimetallic Cantilever Beams," 4<sup>th</sup> Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
- (63) J. Ding, K. Chakrabarty, and R.B. Fair, "Reconfigurable Microfluidic System Architecture Based on Two-Dimensional Electrowetting Arrays," 4<sup>th</sup> Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
- (64) V. Srinivasan, A. Jog, and R.B. Fair, "Scalable Maxromodels for Microelectromechanical Systems," 4<sup>th</sup> Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
- (65) V.K. Pamula, P. Paik, M.G. Pollack, and R.B. Fair, "Microfluidic Reconfigurable Droplet Mixer," BioMEMS and Nano Technology World 2001, Columbus, Ohio, September, 2001.
- (66) P. Kolar and R.B. Fair, "Non-contact Electrostatic Stamping for DNA Microarray Synthesis," Smalltalk 2001, San Diego, CA, August, 2001.
- (67) M.G. Pollack, R.B. Fair, V.K. Pamula, and A. Shenderov, "Electrowetting Microfluidics for High Throughput Screening," Smalltalk 2001, San Diego, CA, August, 2001.
- (68) V.K. Pamula, P.Y. Paik, J. Venkatraman, M.G. Pollack, and R.B. Fair, "Microfluidic Electrowetting-Based Droplet Mixing," MEMS Conference, Berkeley, CA, August, 2001.

- (69) T. Zhang, K. Chakrabarty and R.B. Fair, "Performance Comparison between Continuous-flow and Droplet-based Microelectrofluidic Systems," Fifth International Conference on Modeling and Simulation of Microsystems, San Juan, Puerto Rico, April 22-25, 2002.
- (70) R. B. Fair, M.G. Pollack, R. Woo, V.K. Pamula, H. Ren, T. Zhang, and J. Venkatraman, "A Microwatt Metal-Insulator-Solution-Transport (MIST) Device for Scalable Digital Bio-Microfluidic Systems," Paper 16.4, Inter. Electron Devices Meeting (IEDM), Washington, DC (Dec. 2001).
- (71) H. Ren and R.B. Fair, "Micro/Nano Liter Droplet Formation and Dispensing by Capacitance Metering and Electrowetting Actuation," IEEE Nano-2002, Arlington, VA (August, 2002).
- (72) V. Srinivasan, V. K. Pamula, M.G. Pollack, and R.B. Fair, "A Digital Microfluidic Biosensor for Multianalyte Detection," 16<sup>th</sup> IEEE MEMS 2003 Conf., Kyoto, Jan. 2003.
- (73) H. Ren, V. Srinivasan, and R.B. Fair, "Design and Testing of an Interpolating Mixing Architecture for Electrowetting-Based Droplet On-Chip Chemical Dilution," Transducers, 2003, Boston, June, (2003).
- (74) V. Srinivasan, V.K. Pamula, K.D. Rao, M.G. Pollack, J.A. Izatt, and R.B. Fair, "3-D imaging of moving droplets for microfluidics using optical coherence tomography," Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (  $\mu$ TAS 2003), Lake Tahoe, October, 2003.
- (75) V. Srinivasan, V.K. Pamula, M.G. Pollack, and R.B. Fair, "Clinical diagnostics on human whole blood, plasma, serum, urine, saliva, sweat, and tears on a digital microfluidic platform," Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (  $\mu$ TAS 2003), Lake Tahoe, October, 2003.
- (76) M. G. Pollack, P. Y. Paik, A. D. Shenderov, V. K. Pamula, F. S. Dietrich, and R. B. Fair, "Investigation of electrowetting-based microfluidics for real-time PCR applications Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (  $\mu$ TAS 2003), Lake Tahoe, October, 2003.
- (77) H. Ren, V. Srinivasan, M.G. Pollack, and R.B. Fair, "Automated Electrowetting-Based Droplet Dispensing with Good Reproducibility," Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (  $\mu$ TAS 2003), Lake Tahoe, October, 2003.
- (78) R.B. Fair, V. Srinivasan, P. Paik, H. Ren, V.K. Pamula, and M.G. Pollack, "Electrowetting-Based On-Chip Sample Processing for Integrated Microfluidics, IEDM 2003, Washington, DC, December 10, 2003.
- (79) V. Srinivasan, V.K. Pamula, P. Paik, and R.B. Fair, "Protein Stamping for MALDI Mass Spectrometry Using an Electrowetting-based Microfluidic Platform," Lab-on-a-Chip: Platforms, Devices, and Applications, Conf. 5591, SPIE Optics East, Philadelphia, Oct. 25-28, 2004.
- (80) D. Vissani, K.N. Weaver, V. Srinivasan, R.B. Fair, and J.A. Stenken, "Adapting Theophylline Quantitation via Alkaline Phosphatase Inhibition to a Micro-Total Analytical System," Southern Regional Meeting of ACS, Research Triangle Park, NC, Nov. 10-13, 2004.
- (81) V.K. Pamula, V. Srinivasan, H. Chakrapani, R.B. Fair, and E.J. Toon, "A Droplet-Based Lab-On-A-Chip for Coplorimetric Detection of Nitroaromatic Explosives," 18<sup>th</sup> IEEE Inter. Conference on Micro Electro Mechanical Systems (MEMS 2005), Miami, Jan. 30 (2005).
- (82) P.B. Griffin, R.B. Fair, "A Continuous Flow Microchannel-based DNA Sequencing Scheme," Advances in Genome Biology and Technology Conf., Marco Island, FL, Feb. 9, 2006.
- (83) Y. Ma, A. Khlystov, V. Ivanov, R.B. Fair, "Digital Microfluidic Impactor for Determination of Sulfate in Ambient Aerosol," Inter. Aerosol Conf., St. Paul. MN, Sept. 15, 2006.

- (84) L. Luan, R.D. Evans, D. Schwinn, R.B. Fair, and N.M. Jokerst, "Chip Scale Integration of Optical Microresonator Sensors with Digital Microfluidics Systems," LEOS-2008, Newport Beach, CA, Nov. 9-13, 2008.
- (85) P. Thwar, J.L. Rouse, A.E. Eckhardt, P. Griffin, M.G. Pollack and R.B. Fair, "Digital Microfluidic DNA Sequencing," Advances in Genome Biology and Technology (AGBT) Meeting, Marco Island, Florida, Feb., 2009.
- (86) C.G. Geisler, J.G. Zhou, D.M. Wootton, P.I. Leikes1, R. Fair, "Electrowetting-based Multi-microfluidics Array Printing of High Resolution Tissue Construct with Embedded Cells and Growth Factors," International Cartilage Repair Society, ICRS, Miami, May 23, 2009.
- (87) R.D. Evans, B-N Hsu, Y-Y You, and R.B. Fair, "Electrostatic Printing of Sub-nanoliter Droplets for Tissue Engineering with Precise Concentration Control Via Digital Microfluidics," 13<sup>th</sup> ICACS International Conference on Surface and Colloid Science, New York, June 14-19, 2009.
- (88) C. Geisler, D.M. Wootton, P.I. Leikes, R.B. Fair, and J.G. Zhou, "Material study of electrowetting-based multimicrofluidics array printing of high resolution tissue construct with embedded cells and growth factors," ASME 2010 First Global Congress NanoEngineering for Medicine and Biology, Houston, TX, Feb. 7-10, 2010.
- (89) B. -N. Hsu, A. C. Madison and R. B. Fair "Accelerate Sepsis Diagnosis by Seamless Integration of DNA Purification and qPCR," Proceedings of the 16th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2012), Okinawa, Japan, October 28-November 1, 2012, pp. 830-832.
- (90) Kai Hu, Bang-Ning Hsu, Andrew Madison, Krishnendu Chakrabarty and Richard Fair, "Fault Detection, Real-Time Error Recovery, and Experimental Demonstration for Digital Microfluidic Biochips," Design Automation Technology Europe, paper # 586, Grenoble, March, 2013.
- (91) A. Madison, M. Royal, R. Fair, M. Sandahl, J. Harrington, S. Punnamaraju, A. Eckhardt, A. Sudarsan, and M. Pollack, "Software automated genomic engineering (SAGE) enabled by electrowetting-on-dielectric digital microfluidics," MicroTAS 2013, Freiburg, Oct. 2013.
- (92) A. Madison, M,W. Royal, and R.B. Fair, "An electrowetting on dielectric lab on a chip for multiplex automated genome engineering," 9<sup>th</sup> Inter. Meeting on Electrowetting, Cincinnati, June, 2014.
- (93) L. Chen, A. Madison, and R.B. Fair, "Intra-droplet magnetic bead manipulation on a digital microfluidic chip," MicroTAS 2014, Oct. 26, 2014, San Antonio.
- (94) K. Hu, M. Ibrahim, L. Chen, Z. Li, K. Chakrabarty, and R.B. Fair, "Experimental Demonstration of Error Recovery in an Integrated Cyberphysical Digital-Microfluidic Platform", BIOCAS 2015, Atlanta, Oct. 22-25, 2015.