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Paper 9
Entered: December 9, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

SAMSUNG ELECTRONICS CO., LTD.,
Patent Owner.

Case IPR2015-01327
Patent 6,287,902 B1

Before JAMESON LEE, PATRICK R. SCANLON, and JUSTIN BUSCH, *Administrative Patent Judges*.

BUSCH, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

NVIDIA Corp. ("Petitioner") filed a Petition for *inter partes* review of claims 1–18 ("the challenged claims") of U.S. Patent No. 6,287,902 B1 (Ex. 1101, "the '902 patent"). Paper 2 ("Pet."). Samsung Electronics Co., Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of the challenged claims.

A. Related Matters

The parties identify the district court proceeding *Samsung Electronics Co. v. NVIDIA Corp.*, Case No. 3:14-cv-00757-REP (E.D. Va.) as a related matter. Pet. 2; Paper 5, 2. Petitioner also has filed a second petition for *inter partes* review, IPR2015-01320, of the '902 patent. Pet. 2; Paper 5, 2.

B. The '902 Patent

The '902 patent is directed to improved contact hole structures on integrated circuits having isolation regions and methods of manufacturing the same. Ex. 1101, 1:12–35, 2:44–45. The '902 patent describes a problem of reduced space between patterned conductive layers in which to form contact holes due to increased density of structures formed on integrated circuits. *Id.* at 1:36–49. In particular, the '902 patent discloses forming a first patterned conductive layer on an active region of a substrate and a

second patterned conductive layer on a field isolation layer adjacent to the active region. *Id.* at 2:58–65. The ’902 patent explains that the second patterned conductive layer may serve as an etch-inhibiting layer in order to protect the field isolation layer during etching steps. *Id.* at 2:65–67. The second patterned conductive layer, therefore, may allow greater tolerance with respect to the formation of a contact hole, because damage to the field isolation layer that may otherwise occur when the contact hole extends over the field isolation region can be prevented by the second patterned conductive layer. *Id.* at 3:1–9.

Figures 2 and 8 of the ’902 patent are reproduced below:

FIG. 2
(PRIOR ART)

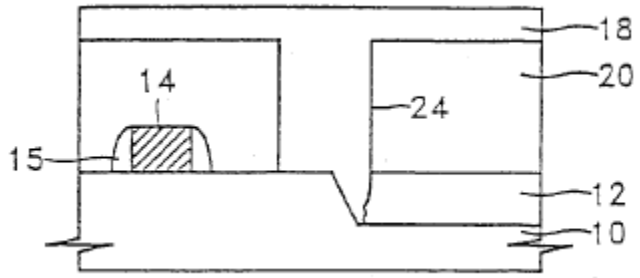


FIG. 8

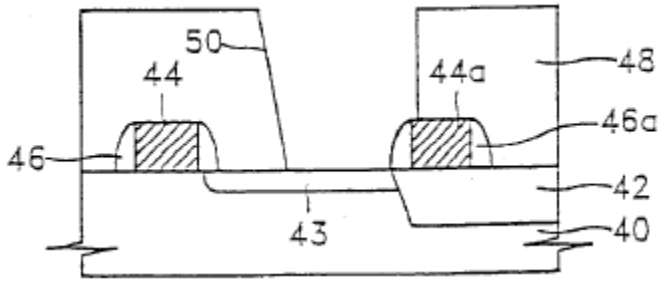


Figure 2 depicts damage caused to field isolation layer 12 caused by some prior art processes used to form contact hole 24. *Id.* at 3:53–54. Figure 8 depicts the retained integrity of field isolation layer 42 when the method described in the ’902 patent is used to form second conductive patterned layer 44a and spacers 46a prior to etching contact hole 50, even when

contact hole 50 is formed above field isolation layer 42. *Id.* at 4:41–50, 6:1–15.

C. Illustrative Claim

Among the challenged claims, claims 1, 11, 12, 15, and 18 are independent. Claim 1 is illustrative and reproduced below:

> 1. A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:
>
> defining adjacent active and field regions on a substrate, and circuits thereon;
>
> forming a field isolation layer on said field region;
>
> forming a first patterned conductive layer on said active region of said substrate spaced apart from said field region;
>
> forming an etch inhibiting layer on said field isolation layer adjacent said active region of said substrate, the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, wherein the second patterned conductive layer does not extend over the active region of the substrate, and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon;
>
> forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer; and
>
> forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer.

Id. at 6:49–7:6.

D. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable based on the following specific grounds:

References	Basis	Challenged Claims
Lee[1] and Yasushige[2]	35 U.S.C. § 103(a)	1, 3–5, 7–12, 14–16, and 18
Lee, Yasushige, and Nowak[3]	35 U.S.C. § 103(a)	2 and 17
Lee, Yasushige, and Lee II[4]	35 U.S.C. § 103(a)	6 and 13

Pet. 18–25, 27–60. In its analysis, Petitioner relies on the declaration testimony of Jack C. Lee, Ph.D. Ex. 1116.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1275–79 (Fed. Cir. 2015). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An inventor may provide a meaning for a term that is different from

[1] KR Patent App. 1994/021255, allegedly laid-open Mar. 22, 1996 (Ex. 1107, "Lee").
[2] JP Pub. No. H7-86158, Mar. 31, 1995 (Ex. 1109, "Yasushige").
[3] U.S. Patent 4,916,514, Apr. 10, 1990 (Ex. 1110, "Nowak").
[4] U.S. Patent 4,952,524, Aug. 28, 1990 (Ex. 1111, "Lee II").

its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner proposes a construction for "insulating spacer along a sidewall of the [second] patterned conductive layer" ("the spacer limitation"), and argues "an insulating layer" and "forming a trench in said substrate, wherein said field isolation layer fills said trench" ("the trench limitation") should be given their plain and ordinary meanings. Pet. 25–27. Specifically, Petitioner proposes that the spacer limitation should be construed to mean "an insulating spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." *Id.* at 25–26.

Patent Owner argues Petitioner's proposed claim constructions are defective. Patent Owner argues the spacer limitation and the trench limitation should be given their plain and ordinary meanings and "an insulating layer" should be construed as "a structure comprising one or more electrically insulating sublayers." Prelim. Resp. 12–17. In particular, Patent Owner contends that Petitioner's proposed construction of the spacer limitation introduces ambiguity and imparts limitations from the specification and prosecution history into the claim. *Id.* at 13–15.

We do not find it necessary to construe explicitly the trench limitation for purposes of this decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy). Moreover, for the spacer limitation and "an insulating layer," no extensive or special construction is required. They mean just

what they ostensibly appear to say. We reject Petitioner's contention that the spacer limitation must prevent "etch damage to the field isolation layer if the contact hole is misaligned." We also reject Patent Owner's proposed construction of "an insulating layer," because it provides no clarity beyond that provided by the claim language itself. Moreover, we determine that an ordinarily skilled artisan would have understood what is meant by the spacer limitation and "an insulating layer" in the context of semiconductor fabrication.

We also provide a construction of "a dummy pattern," which is recited in each of the independent claims. The specification of the '902 patent refers to a "dummy pattern" twice. The first instance explains that second patterned conductive layer 44a has the same structure as first conductive patterned layer 44, but "second patterned conductive layer 44a is electrically isolated" and "*[i]n other words*, the second patterned conductive layer 44a serves as a *dummy pattern*." Ex. 1101, 4:25–30 (emphases added). The second occurrence of "dummy pattern" in the '902 patent states that "second patterned conductive layer 44a can be a dummy pattern serving no electrical function." *Id.* at 5:37–38. Every recitation of a dummy pattern in the claims further recites that the pattern is "electrically isolated from the substrate and circuits thereon." We read this language as simply making explicit what is already meant by the term "dummy pattern." Therefore, for purposes of this decision, we construe "a dummy pattern" to be a patterned conductive layer that serves no electrical purpose and is electrically isolated from the substrate and circuits thereon.

B. Asserted Grounds Based on Lee and Yasushige

Petitioner contends claims 1, 3–5, 7–12, 14–16, and 18 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Lee and Yasushige. Pet. 18–22, 27–55. Relying on the testimony of Dr. Lee, Petitioner explains how Lee and Yasushige allegedly teach all the claim limitations, and argues a person of ordinary skill in the art would have combined Lee with Yasushige. *Id.* (citing Ex. 1116).

1. Lee (Ex. 1107)

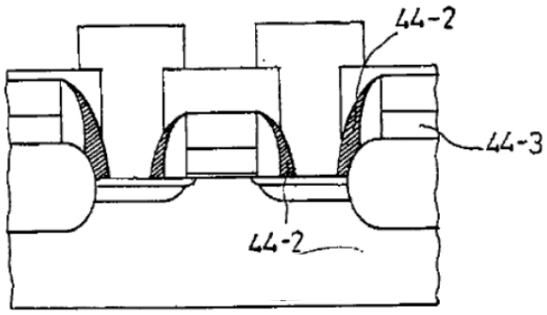
Lee is directed to "a method of fabricating a semiconductor device, in which the characteristics of the device are improved by securing an align margin upon formation of the contact hole." Ex. 1107, 2. Lee explains that the prior art "depended on the alignment accuracy of a photographic process," and that, when misalignment occurs, the field oxide layer that separates an active region may be damaged, resulting in junction leakage. *Id.* at 3. Lee further describes one prior art attempt to address this problem by forming side walls along the interlayer insulation film walls, which are created after a contact hole is formed in the interlayer insulation film, prior to forming a conductive layer in the contact hole. *Id.* at 4.

Lee proposes to address the identified problems by "forming an etch stop layer on the contact hole area to protect the lower insulation layer." Ex. 1107, 5. Lee's first embodiment describes forming an etch stop layer "around the impurity region in the form of a sidewall by depositing a material having a high etch selectivity with an interlayer insulation film," prior to forming the interlayer insulation film. *Id*. at 6. The etch stop layer may be formed of a conductive or non-conductive material and is formed via

deposition and etch-back processes "using the step area formed on the lower layer without any additional mask." *Id.* at 7.

Lee further discloses a second embodiment of its invention. Figure 4 of Lee is reproduced below:

FIG. 4



Ex. 1107, 17. Figure 4 depicts a view of a semiconductor fabricated according to one embodiment of Lee**.** *Id.* at 7. Specifically, Figure 4 is the result of "a method of forming an etch stop layer (44-2) using an internal connection line (44-3) passing adjacently or the step of a dummy pattern when the step at the lower layer used to form the etch stop layer in the first embodiment is not sufficient." *Id.*

Patent Owner argues that Petitioner has not sufficiently met its burden to establish that Lee constitutes prior art. Prelim. Resp. 2–5. Specifically, Patent Owner asserts Lee is not a patent and Petitioner has not established that Lee was sufficiently publicly accessible to qualify as a printed publication. *Id.* at 2–3. Patent Owner points out that Petitioner never alleges that Lee was ever published and Petitioner merely relies on the publication of a different document (KR Patent Pub. No. 1996-0009001 (the "Lee Publication"), submitted by Petitioner as Exhibit 1112), which provides various details about Lee, including the title, scope of claims, drawings, and summary, to establish the public accessibility of Lee. *Id.* at 3 (citing Pet. 9–10). Patent Owner asserts Petitioner's reliance on *In re Wyer*, 655 F.2d. 221

(CCPA 1981), is misplaced and that *In re Wyer* "actually supports a finding that Petitioner has failed to meet its burden to establish *Lee* as a printed publication." *Id.* at 4. Patent Owner contends that Petitioner has not asserted any facts regarding whether or how Lee would have been available to the public, simply based on the Lee Publication, because Petitioner fails to provide an explanation of the Korean Patent Office's practices regarding making applications publicly accessible in 1996. *Id.* at 5. Notably, Patent Owner merely asserts that Petitioner has not sufficiently established that Lee was publicly available and does not assert that Lee was not publicly accessible in 1996.

We find Petitioner has sufficiently demonstrated the public accessibility of Lee because Petitioner asserts Lee was available from a government entity (the Korean Patent Office) in accordance with that government's laws before the priority date of the '902 patent. Pet. 9–10. Petitioner further asserts that the "'laying open for public inspection' [of a patent application] can serve as 102(b) prior art." *Id.* at 10 (quoting *In re Wyer*, 655 F.2d at 221; citing MPEP 901.05 I.C). Petitioner supports its assertions with testimony from Dr. Lee. Ex. 1116 ¶ 39. On this record, without evidence to the contrary, we find Petitioner's argument and evidence sufficient to establish that Lee qualifies as 102(b) art and, therefore, may be asserted as prior art in an *inter partes* review petition. Thus, at this time, we are persuaded that Lee is prior art.

2. Yasushige (Ex. 1109)

Yasushige is directed to a semiconductor device "in which inconveniences as a result of overetching are resolved." Ex. 1109, Abs. Yasushige explains that it solves the problem by providing "a BiCMOS

semiconductor device having bipolar transistors and MOS transistors having an LDD structure, characterized in that a conductive film *identical to the gate electrode of said MOS* transistor is *formed around the base region* of said bipolar transistor, and *said conductive film is electrically isolated* from the base region. *Id.* ¶ 29 (emphases added). Figure 1 of Yasushige is reproduced below:

[FIG. 1]
The semiconductor device of Embodiment 1

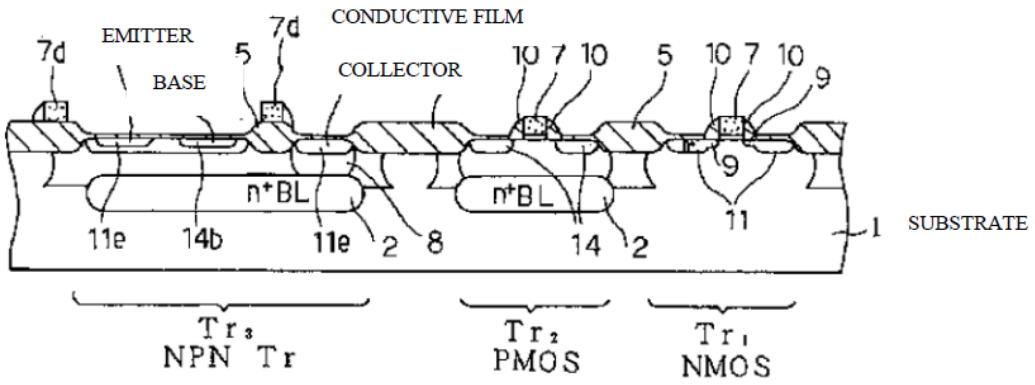


Figure 1 depicts "a cross-sectional view showing the structure of the semiconductor device" according to one embodiment. *Id.* ¶ 63. Figure 1 depicts "conductive film 7d identical to the gate electrode 7 of the MOS transistor formed around the base region 14b [which] is electrically isolated from the base region by an isolation region 5." *Id.* ¶ 64.

3. Analysis of Obviousness Challenge of Claims 1, 3–5, 7–12, 14–16, and 18

Petitioner asserts that the combination of Lee and Yasushige teaches all of the limitations of independent claim 1. Pet. 27–42. For example, Petitioner maps Lee's disclosure of a process for fabricating an improved semiconductor device "by securing an align margin upon formation of the contact hole" to the preamble of claim 1, which recites "[a] method for forming a contact hole for a microelectronic structure . . . ." Pet. 28 (citing

Ex. 1107, 2). Petitioner also points to disclosures in Lee allegedly meeting each of the recited limitations in claim 1 and disclosures in Yasushige allegedly teaching the limitations referred to by Petitioner as elements 1f and 1g. *Id.* at 28–35 (citing Ex. 1107, 3, 5–7, Figs. 1(b), 3(a), 4, Ex. 1109, 29, 41, Fig. 1, Ex. 1116 ¶¶ 86, 87, 89, 90, 93, 95, 97–101), 41–42 (citing Ex. 1107, 3, 7, Figs. 3(c), 4).

Regarding the limitation Petitioner refers to as 1f (i.e., "wherein the second patterned conductive layer does not extend over the active regions of the substrate"), Petitioner points to Figure 4 of Lee, which shows that conductive pattern 44-3 is formed on the isolation layer. Pet. 33–34. Figure 4 of Lee shows conductive pattern 44-3 is near, but does not extend over, the active region. Ex. 1107, Fig. 4. Petitioner further contends that an ordinarily skilled artisan would have understood Lee's disclosures, including the fact that the etch stop layer is used to protect the field oxide layer when forming a contact hole, to indicate that the conductive layer does not extend over the active region. Pet. 34–35. Petitioner further asserts that Yasushige also teaches limitation 1f, and provides a rationale for combing Lee and Yasushige. Pet. 35–36. We find Petitioner has demonstrated sufficiently that the combination of Lee and Yasushige teaches "wherein the second patterned conductive layer does not extend over the active regions of the substrate."

Petitioner argues Lee also discloses "wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon" (the "dummy pattern limitation"), as recited in claim 1, which Petitioner identifies as element 1g. Pet. 36–41. Petitioner alleges Figure 4, and the accompanying description, describe an embodiment where

Lee's "etch stop layer may be formed as a spacer along an 'internal connection line passing adjacently' ***or*** a 'dummy pattern.'" *Id.* at 36 (quoting Ex. 1107, 7). Petitioner further asserts that an ordinarily skilled artisan would have known[5] that one way to form a dummy pattern would be to form that pattern at the same time, and using the same process and materials, as the process for forming the first (functional) patterned conductive layer, resulting in a dummy pattern that is also a patterned conductive layer. *Id.* at 36–37 (citing Ex. 1107, 3, Ex. 1116 ¶ 102). Petitioner further contends that Lee's dummy pattern is electrically isolated from the substrate and circuits thereon because it is formed over the field oxide layer. *Id.* at 37. Petitioner asserts that Lee's distinction of an embodiment using a "dummy pattern" from an embodiment using an "internal connection line" is further evidence that the dummy pattern has no electrical connection to the substrate or circuits thereon. *Id.* Moreover, Petitioner argues an ordinarily skilled artisan would have understood that a dummy pattern is a gate pattern that serves no electrical function. *Id.* at 38 (citing Ex. 1114, 322 (dictionary definition of "dummy"), Ex. 1113, 61

[5] Patent Owner argues that Petitioner's "statement[s] regarding what a POSITA 'would know'" is not the proper inquiry, because obviousness focuses on what an ordinarily skilled artisan *would have known* at the time of the invention of the '902 patent. Prelim. Resp. 7. Patent Owner is correct in this regard. Nevertheless, based on the context of how the Petition applies the knowledge of an ordinarily skilled artisan, we find that the Petition's obviousness analysis is intended to be applied from the view of an ordinarily skilled artisan at the appropriate time, notwithstanding Petitioner's imprecise phrasing. *See* Pet. 8, Ex. 1116 ¶ 15 ("I further understand that obviousness of a claim requires that the claim be obvious from the perspective of a person of ordinary skill in the relevant art, at the time the invention was made.").

(dictionary definition of "dummy connector plug"), Ex. 1116 ¶ 105). Petitioner further argues that, to the extent not disclosed by Lee, Yasushige discloses conductive film 7d, which Petitioner maps to the recited electrically isolated dummy pattern, and that an ordinarily skilled artisan would have combined Lee and Yasushige. Pet. 18–22, 39–41.

Patent Owner argues that portions of the Petition regarding Lee's disclosure of the dummy pattern limitation do not cite to Lee and are merely conclusory statements. Prelim. Resp. 6–7. The portion of the Petition cited to by Patent Owner, however, expounds upon the prior statement in the Petition that "Lee contemplates in one embodiment illustrated in Fig. 4 that the etch stop layer may be formed as a spacer along an 'internal connection line passing adjacently' **or** a 'dummy pattern.' Fig. 4, 17-6." We find persuasive Petitioner's arguments that Lee's dummy pattern meets the recited dummy pattern limitation.

Patent Owner also argues that Petitioner merely has shown that Yasushige teaches a conductive film that is isolated from a base region, but that Yasushige does not disclose a dummy pattern "electrically isolated *from the substrate and circuits thereon*." Prelim. Resp. 7. As discussed above, we find Petitioner has demonstrated sufficiently that at least Lee alone teaches "the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon" and, therefore, we need not determine whether Petitioner has demonstrated sufficiently that Yasushige teaches that limitation.

At this time, we determine the portions of Lee that Petitioner maps to elements 1a–1e, and 1g–1i disclose or teach the respective recited limitations. We find persuasive, on this record, Petitioner's argument that

Lee alone, or the combination of Lee and Yasushige, teaches elements 1f and Petitioner's articulated rationale for combining Lee and Yasushige. Therefore, on this record we determine Petitioner has demonstrated a reasonable likelihood of establishing that the combination of Lee and Yasushige teaches each of the limitations recited in claim 1.

Independent claims 11, 12, 15, and 18 recite similar limitations to those recited in claim 1. Petitioner provides further explanation as to how the combination of Lee and Yasushige teaches each of the limitations recited in claims 11, 12, 15, and 18, accounting for the variations in claim language and for the additional limitations. Pet. 50–54.

Dependent claims 3–5, 7–10, 14, and 16 recite further limitations regarding materials used, or properties thereof, for certain layers (claims 3, 5, 8, 14, and 16) and methods and placement of certain layers or contact holes (claims 4, 7, 9, and 10). Petitioner maps disclosures in Lee (claims 3–5, 7–10, 14, and 16) and Yasushige (claim 4) to each of these additional limitations. We have reviewed Petitioner's arguments with respect to each of claims 1, 3–5, 7–12, 14–16, and 18 of the '902 patent. Upon consideration of Petitioner's explanations and supporting evidence and Patent Owner's Preliminary Response, we are persuaded by Petitioner's contentions. On the present record, Petitioner has shown sufficiently that Lee, or at least the combination of Lee and Yasushige, teaches the limitations recited in claims 1, 3–5, 7–12, 14–16, and 18, and Petitioner has articulated sufficient reasoning with rational underpinning for combining Lee and Yasushige. Accordingly, the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that

claims 1, 3–5, 7–12, 14–16, and 18 would have been rendered obvious by the combination of Lee and Yasushige.

C. Asserted Grounds Based on Lee, Yasushige, and Nowak

Petitioner contends claims 2 and 17 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Lee, Yasushige, and Nowak. Pet. 55–57. Relying on the testimony of Dr. Lee, Petitioner explains how Lee, Yasushige, and Nowak allegedly teach all the claim limitations, and argues a person of ordinary skill in the art would have combined Nowak with Lee and Yasushige. *Id.* at 22–23, 55–57 (citing Ex. 1116).

1. Nowak (Ex. 1110)

Nowak is directed to "[a]n integrated circuit having improved planarity," which includes "dummy conductors [that] are open circuited and consequently carry no signals [whose] function is purely mechanical; and specifically, they function to partially fill the spaces between the signal conductors such that an overlying insulating layer can be formed without peaks and valleys." Ex. 1110, Abs.

2. Analysis of Obviousness Challenge of Claims 2 and 17

Petitioner asserts that the combination of Lee, Yasushige, and Nowak teaches all of the limitations of dependent claims 2 and 17. Claims 2 and 17 further recite "said insulating layer comprises nitride." Ex. 1101, 7:7–8, 8:64–65. Petitioner argues nitride is one of a few insulating materials used in semiconductors, and Lee discloses various considerations, including choosing a material with "high etch selectivity with an interlayer insulation film," that would have led an ordinarily skilled artisan to look to other references to identify an appropriate insulator material. Pet. 55–56. Petitioner asserts Nowak is one such reference that an ordinarily skilled

artisan would have considered and that Nowak teaches using nitride for insulating layers over dummy conductor gates. *Id.* at 56–57. Petitioner provides reasons that a skilled artisan would have combined Nowak with Lee. *Id.* at 22–23, 57.

Upon consideration of Petitioner's explanations and supporting evidence and Patent Owner's Preliminary Response, we are persuaded by Petitioner's contentions. On the present record, Petitioner has shown sufficiently that the combination of Lee, Yasushige, and Nowak teaches the limitations recited in dependent claims 2 and 17, and Petitioner has articulated sufficient reasoning with rational underpinning for combining the references. Accordingly, the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that claims 2 and 17 would have been rendered obvious by the combination of Lee, Yasushige, and Nowak.

D. Asserted Grounds Based on Lee, Yasushige, and Lee II

Petitioner contends claims 6 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Lee, Yasushige, and Lee II. Pet. 57–60. Relying on the testimony of Dr. Lee, Petitioner explains how Lee, Yasushige, and Lee II allegedly teach all the claim limitations, and argues a person of ordinary skill in the art would have combined Lee II with Lee and Yasushige. *Id.* at 23–25, 57–60 (citing Ex. 1116).

1. Lee II (Ex. 1111)

Lee II is directed to a semiconductor device and manufacturing method for such a device that includes a "trench which provides electrical isolation between transistors on an integrated circuit substrate." Ex. 1111, Abs.

2. Analysis of Obviousness Challenge of Claims 6 and 13

Petitioner asserts that the combination of Lee, Yasushige, and Lee II teaches all of the limitations of dependent claims 6 and 13. Claims 6 and 13 further recite limitations relating to forming a trench in the substrate, "wherein said field isolation layer fills said trench." Ex. 1101, 7:18–21, 8:26–28. Petitioner argues that Lee does not disclose explicitly forming and filling (with the field isolation layer) a trench, but that such a process was common practice and an obvious design choice. Pet. 58. Petitioner further argues that Lee II discloses forming a trench and filling it with a field isolation layer, and Petitioner provides reasons that a skilled artisan would have combined Lee II with Lee and Yasushige. *Id.* at 23–25, 58–59. Petitioner, therefore, asserts that the combination of Lee and Lee II teaches the additional limitations recited in claims 6 and 13 and, because they depend from claims 1 and 12, respectively, claims 6 and 13 would have been obvious in view of the combination of Lee, Yasushige, and Lee II. *Id.* at 60.

Upon consideration of Petitioner's explanations and supporting evidence and Patent Owner's Preliminary Response, we are persuaded by Petitioner's contentions. On the present record, Petitioner has shown sufficiently that the combination of Lee, Yasushige, and Lee II teaches the limitations recited in dependent claims 6 and 13, and Petitioner has articulated sufficient reasoning with rational underpinning for combining the references. Accordingly, the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that claims 6 and 13 would have been rendered obvious by the combination of Lee, Yasushige, and Lee II.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that the challenged claims are unpatentable. At this preliminary stage, the Board has not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues.

IV. ORDER

Accordingly, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted as to claims 1–18 of the '902 patent on the following grounds of unpatentability:

A. Claims 1, 3–5, 7–12, 14–16, and 18 under 35 U.S.C. § 103(a) as obvious over Lee and Yasushige; and

B. Claims 2 and 17 under 35 U.S.C. § 103(a) as obvious over Lee, Yasushige, and Nowak; and

C. Claim 6 and 13 under 35 U.S.C. § 103(a) as obvious over Lee, Yasushige, and Lee II; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

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