

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.
Petitioner

v.

ATI TECHNOLOGIES ULC
Patent Owner

Case: IPR2015-00321

Patent 7,095,945

DECLARATION OF DAN SCHONFELD, PHD

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I. INTRODUCTION

1. My name is Dan Schonfeld, and I have been retained by the law firm of Mayer Brown LLP on behalf of LG Electronics, Inc. as an expert in the relevant art.

2. I have been asked to provide my opinions and views on the materials I have reviewed in this case related to Ex. 1001, U.S. Patent No. 7,095,945 (“the ’945 Patent”) (“the patent-at-issue”), and the scientific and technical knowledge regarding the same subject matter before and for a period following the date of the first application for the patent-at-issue was filed.

3. I am being compensated for my work on this case at my standard consulting rate of \$500 per hour. I am also being reimbursed for all incurred expenses. My compensation has not influenced any of my opinions in this matter and does not depend on the outcome of this proceeding or any issue in it.

4. My opinion and underlying reasoning for this opinion is set forth below.

A. Background And Qualifications

5. I am currently a Professor in the Department of Electrical and Computer Engineering at the University of Illinois at Chicago. I have been elected Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”) as well as Fellow of the International Society for Optics and Photonics (“SPIE”). I have also been elected University Scholar of the University of Illinois. A complete list of my publications, professional activities, and honors that I have received is fully set forth in my curriculum vitae, attached hereto as Appendix A.

6. I received my B.S. degree in Electrical Engineering and Computer Science from the University of California, Berkeley, California, and my M.S. and Ph.D. degrees in Electrical and Computer Engineering from The Johns Hopkins University, Baltimore, Maryland, in 1986, 1988, and 1990, respectively.

7. In August 1990, I joined the Department of Electrical Engineering and Computer Science at the University of Illinois, Chicago, Illinois, where I am currently a Professor in the Departments of Electrical and Computer Engineering, Computer Science, and Bioengineering. I serve as Co-Director of the Multimedia Communications Laboratory (“MCL”) and member of the Signal and Image Research Laboratory (“SIRL”). I have also served as Director of the University-Industry Engineering Research Center (“UIERC”), formerly known as the Manufacturing Research Center (“MRC”), in the College of Engineering.

8. I currently serve as Editor-in-Chief of the IEEE Transactions on Circuits and Systems for Video Technology. I have previously served as Deputy Editor-in-Chief of the IEEE Transactions on Circuits and Systems for Video Technology and Area Editor for special issues of the IEEE Signal Processing Magazine. I have also served as Associate Editor of the IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Image Processing, and IEEE Transactions on Signal Processing. I also served on the editorial board of the IEEE Signal Processing Magazine, EURASIP Journal of Image and Video Processing, and Research Letters in Signal Processing. I have served as guest editor of numerous special issues in various

journals in the area of multimedia systems.

9. I currently serve as Technical Program Chair of the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 2018. I have served as General Co-Chair of the IEEE International Conference on Multimedia and Expo (ICME) 2012. I have also served as Chair of the IEEE Workshop on Video Mining 2008 and the SPIE Conference on Visual Communication and Image Processing 2007. I have also served on the organizing committees of various conferences including the IEEE International Conference on Image Processing 1998 and 2012.

10. I have authored and co-authored over 200 technical papers for various journals and conferences. I was co-author (with Carlo Giulietti and Rashid Ansari) of a paper that won the Best Paper Award at the ACM Multimedia Workshop on Advanced Video Streaming Techniques for Peer-to-Peer Networks and Social Networking 2010. I was also co-author (with Junlan Yang) of a paper that won the Best Student Paper Award at the IEEE International Conference on Image Processing 2007. I was also co-author (with Wei Qu) of a paper that won the Best Student Paper Award at the IEEE International Conference on Image Processing 2006. I was also co-author (with Nidhal Bouaynaya) of a paper that won the Best Student Paper Award in Visual Communication and Image Processing 2006. My publications in the area of image and video processing and communications date back to 1988. A list of my publications within the past ten years is included in Appendix A.

11. I was invited as a Plenary Speaker and Keynote Speaker to the International Conference on Intelligent Control and Information Processing (ICICIP) 2013 and International Conference on Brain Inspired Cognitive Systems (BICS) 2013, IEEE/EIT International Conference on Audio, Language, and Image Processing 2010, the IEEE International Conference on Advanced Video and Signal-Based Surveillance 2009, and the ASME International Conference on Communications, Signals and Systems 1995 and 2001.

12. I have served as Region 1-6 (North America) representative on the Chapters Committee of the IEEE Signal Processing Society. I have also served as Chairman of the IEEE Signal Processing Chicago Chapter. I have also served on the IEEE Image, Video and Multidimensional Signal Processing Technical Committee as well as the IEEE Multimedia Communications Technical Committee. I also serve on the American National Standards Institute (ANSI)/Underwriters Laboratory (UL) Standards Technical Panel ("STP") on Multimedia Systems.

13. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my curriculum vitae (see Appendix A). Additionally, I have consulted for several companies in the area of multimedia systems. A list of cases in which I have testified as an expert at trial or by deposition is attached hereto as Appendix B.

B. Information Considered

14. In addition to my general knowledge gained as a result of my education and

experience in this field, I have reviewed and considered, among other things, the '945 Patent, the prosecution history of the '945 Patent, and the prior art of record.

15. The full list of information that I have considered in forming my opinions for this Declaration is set forth throughout the Declaration and listed in the attached Appendix C.

I. LEGAL STANDARDS

16. In forming my opinions and considering the patentability of the claims of the '945 Patent, I am relying upon certain legal principles that counsel has explained to me.

17. I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in light of what came before it. Patents and publications which predated the invention are generally referred to as “prior art.”

18. I understand that in this proceeding the burden is on the party asserting unpatentability to prove it by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely than not.

19. I understand that in this proceeding, the claims must be given their broadest reasonable interpretation consistent with the specification. The claims after being construed in this manner are then to be compared to information that was disclosed in the prior art.

A. Person Of Ordinary Skill In The Art

20. I have been informed that the claims of a patent are judged from the perspective of a hypothetical construct involving “a person of ordinary skill in the art.” The “art” is the field of technology to which the patent is related. I understand that the purpose of using a person of ordinary skill in the art’s viewpoint is objectivity. Thus, I understand that the question of validity is viewed from the perspective of a person of ordinary skill in the art, and not from the perspective of (a) the inventor, (b) a layperson, or (c) a person of extraordinary skill in the art. I have been informed that the claims of the patent-at-issue are interpreted as a person of ordinary skill in the art would have understood them in the relevant time period (*i.e.*, when the patent application was filed or the earliest effective filing date).

21. It is my opinion that a person of ordinary skill in the art relevant to the ’945 Patent at the time of the filing of the patent would have had a bachelor’s degree in electrical engineering, computer engineering, computer science, or the equivalent, and two (2) years of work experience in the area of multimedia systems, including time shifting of video data.

22. I understand that a “person of ordinary skill is also a person of ordinary creativity, not an automaton” and that would be true of anyone developing video time-shifting systems.

B. Anticipation

23. I understand that the following standards govern the determination of whether

a patent claim is “anticipated” by the prior art. I have applied these standards in my analysis of whether claims of the ’945 Patent were anticipated at the time of the invention.

24. I understand that a patent claim is “anticipated” by a single prior art reference if that reference discloses each element of the claim in a single embodiment. A prior art reference may anticipate a claim inherently if an element is not expressly stated, but only if the prior art necessarily includes the claim limitations.

25. I understand that the test for anticipation is performed in two steps. First, the claims must be interpreted to determine their meaning. Second, a prior art reference is analyzed to determine whether every claim element, as interpreted in the first step, is present in the reference. If all the elements of a patent claim are present in the prior art reference, then that claim is anticipated and is invalid.

26. I understand that it is acceptable to examine extrinsic evidence outside the prior art reference in determining whether a feature, while not expressly discussed in the reference, is necessarily present within that reference.

C. Obviousness

27. I understand that a claim can be invalid in view of prior art if the differences between the subject matter claimed and the prior art are such that the claimed subject matter as a whole would have been “obvious” at the time the invention was made to a person having ordinary skill in the art.

28. I understand that the obviousness standard is defined at 35 U.S.C. § 103(a). I

understand that a claim is obvious over a prior art reference if that reference, combined with the knowledge of one skilled in the art or other prior art references disclose each and every element of the recited claim.

29. I also understand that the relevant inquiry into obviousness requires consideration of four factors:

- a. The scope and content of the prior art;
- b. The differences between the prior art and the claims at issue;
- c. The knowledge of a person of ordinary skill in the pertinent art; and
- d. Objective factors indicating obviousness or non-obviousness may be

present in any particular case, such factors including commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and that the patentee proceeded contrary to the accepted wisdom of the prior art.

30. I understand that when combining two or more references, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissible hindsight. I have been informed that the application of the teaching, suggestion or motivation test should not be rigidly applied, but rather is an expansive and flexible test. For example, I have been

informed that the common sense of a person of ordinary skill in the art can serve as motivation for combining references.

31. I understand that the content of a patent or other printed publication (*i.e.*, a reference) should be interpreted the way a person of ordinary skill in the art would have interpreted the reference as of the effective filing date of the patent application for the '945 Patent. I have assumed that the person of ordinary skill is a hypothetical person who is presumed to be aware of all the pertinent information that qualifies as prior art. In addition, the person of ordinary skill in the art makes inferences and creative steps. He or she is not an automaton, but has ordinary creativity.

32. I have been informed that the application that issued as the '945 Patent was filed on November 6, 2000. Thus, the relevant time period for determining what one of ordinary skill in the art knew is November 6, 2000.

D. Claim Construction

33. I have been informed that a claim subject to *Inter Partes* Review is given its “broadest reasonable construction in light of the specification of the patent in which it appears.” I have been informed that this means that the words of the claim are given their plain meaning from the perspective of one of ordinary skill in the art unless that meaning is inconsistent with the specification. I understand that the “plain meaning” of a term means the ordinary and customary meaning given to the term by those of ordinary skill in the art at the time of the invention and that the ordinary and customary meaning of a term may be evidenced by a variety of sources, including the

words of the claims, the specification, drawings, and prior art.

34. I understand that in construing claims “[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art.” (MPEP § 2143.03, citing *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970)).

35. I understand that extrinsic evidence may be consulted for the meaning of a claim term as long as it is not used to contradict claim meaning that is unambiguous in light of the intrinsic evidence. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1324 (Fed. Cir. 2005) (citing *Vitronics Corp. v. Conceptiontronic, Inc.*, 90 F.3d 1576, 1583-84 (Fed. Cir. 1996)).

I also understand that in construing claim terms, the general meanings gleaned from reference sources must always be compared against the use of the terms in context, and the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is most consistent with the use of the words by the inventor. *See, e.g., Ferguson Beauregard/Logic Controls v. Mega Systems*, 350 F.3d 1327, 1338 (Fed. Cir. 2003) (citing *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1300 (Fed. Cir. 2003)).

II. TECHNOLOGY BACKGROUND

A. Multiplexers and Demultiplexers

36. A multiplexer combines a plurality of signals into a multiplexed signal. A demultiplexer performs the reverse operation by extracting the plurality of signals

from the multiplexed signal. Some well known¹ examples of signal multiplexing include: (a) frequency division multiple access (FDMA), where individual signals correspond to distinct frequency bandwidths in the multiplexed signal (*e.g.*, radio and television signals); (b) time division multiple access (TDMA), where individual signals correspond to distinct time slots in the multiplexed signal (*e.g.*, telephone signals); and (b) code division multiple access (CDMA), where individual signals correspond to distinct code sequences in the multiplexed signal (*e.g.*, cellular signals).

37. Multiplexing and demultiplexing is essential in multimedia data communication for the efficient representation, transmission, processing, and presentation of correlated multimedia streams. For example, sending a movie or television program to a viewer requires the transmission of an audio and a video stream as well as related control data (*e.g.*, subtitles). The audio, video, and control data streams are multiplexed together into a multiplexed signal, and thus the receiver can extract correlated data streams and synchronize the presentation of the audio, video, and control signals.

38. Similarly, broadcasting television signals to multiple viewers requires the simultaneous transmission of a plurality of television programs in a single multiplexed

¹ To be clear, when I refer to an element or concept as “well-known” or “known in the prior art,” I particularly mean to say that the element or concept was well-known as of November 6, 2000.

signal by combining the individual television programs (each of which is already a multiplexed signal representing audio, video and control signals) into a multiplexed signal that is broadcast to all viewers. The receivers of individual viewers are then instructed by the viewers to extract a specific television program from the multiplexed broadcast signal for presentation on the television set.

B. Packetized Data

39. Traditional communication was performed over circuit-switched networks. In such networks, signals are transmitted as uninterrupted data streams from the sender to the receiver. Examples of circuit-switched networks include analog multimedia communications such as radio, television, and telephone systems.

40. With the emergence of the Internet in the late 1960s, an alternative data communication method was introduced, known as packet-switched networks. In these networks, data is fragmented into a sequence of data chunks. The individual data chunks are then encapsulated in a packet. The packet consists of the data chunk, referred to as the packet payload, as well as additional information that is typically located in a packet header. The packet header consists of various parameters for efficient data communication (*e.g.*, packet identifier, sequence number, timestamp, cyclic redundancy check, etc.).

C. MPEG Streams

41. There are many different multimedia coding standards. For simplicity, I shall limit this discussion here to compression known as the Moving Picture Expert Group

(MPEG) compression standards. In particular, I will focus exclusively on aspects of the two earliest MPEG compression standards, known as MPEG-1 and MPEG-2.

42. MPEG-1 was aimed at compression and storage on a compact disc (CD) and was released in 1993. It is comprised of three parts: video compression, audio compression, and systems. The audio compression part portion includes the well known MPEG-1 Audio Layer III audio compression format, better known as MP3.

43. MPEG-2 targeted broadcast-quality television signals and was released in 1996. It was adopted for the representation of video signals on a digital video disc (DVD). MPEG-2 eventually emerged as a ubiquitous format for the representation of video signals and was adopted by the Advanced Television Systems Committee (ATSC), Digital Video Broadcasting (DVB), Integrated Services Digital Broadcasting (ISDB), and Blu-ray discs for the representation of high definition television (HDTV). It is comprised of multiple parts including video compression, audio compression, and systems.

44. The parts of the MPEG-1 and MPEG-2 standards germane to our discussion are MPEG-1 Systems and MPEG-2 Systems, formally known as ISO/IEC 11172-1 and ISO/IEC 13818-1, respectively. The systems part provides a container for the representation, multiplexing, and synchronization of audio and video data. There are two approaches to systems: Program Stream (PS) and Transport Stream (TS).

45. Both MPEG PS and MPEG TS are used to represent coded audio and video streams. The basic representation of MPEG data is known as an elementary stream

(ES) and contains the raw coded audio and video data.

46. The elementary audio and video streams are divided into variable length packets known as packetized elementary streams (PES). The PES includes a header that contains various parameters such as a stream identifier (SID) used to identify the stream.

47. The PES also includes optional timing information such as the presentation time stamp (PTS) and decoding time stamp (DTS). The PTS provides timing information that allows for synchronization of the multiple PESs. For example, PTS allows for synchronization between audio and video streams. It is thus used to determine when to display and then discard a program segment.

48. The DTS is needed because video frames are displayed and coded in different orders. More particularly, some video frames depend on the present or past, whereas other video frames depend on the future. It is therefore necessary to include a DTS which provides timing information that specifies when to decode a program segment.

1. MPEG Program Stream (PS)

49. Program Stream (PS) is used by MPEG-1, and a very similar extension of the MPEG-1 PS is used by MPEG-2, in a container format for storage of audio and video data in storage devices such as CDs and DVDs. MPEG-1 and MPEG-2 PS allow for random access of audio and video data from storage devices, thus allowing efficient trick play (*e.g.*, fast-forward, rewind, pause, and stop).

50. The MPEG PS combines multiple PESs (typically a single audio PES with a

single video PES) from a single program that share a common time base into a PS structure known as a multiplex. The combination of the multiple PESs is performed by interleaving through a process known as time-division multiplexing. The MPEG PS also includes timing information such as a system clock reference (SCR).

51. The '945 Patent describes the multiplexing of several packetized elementary streams into a program stream: “an elementary stream (ES) is a set of data generally consisting of compressed data from a single source, such as a video or audio source, with some additional ancillary data for identification, characterization and synchronization. ES streams are first packetized into either constant length or variable length Packetized Elementary Stream packets (PES packets) consisting of header and payload. Each PES packet header starts with start code (0x000001) followed with the stream id byte identifying type of ES underneath. PES packets from various elementary streams are merged together to form a program (service) with its own system time clock (STC). All ES component streams within one program are synchronized have periodic PTS stamps corresponding to the STC counter to indicate the proper timing for each ES.” '945 Patent, 1:64-2:12 (emphasis added).

2. MPEG-2 Transport Stream (TS)

52. Transport Stream (TS) was introduced in MPEG-2, and is a container format originally designed for transmission over ATM networks. It has since been adopted for communication over various networks including radio-frequency networks and cable networks. MPEG-2 TS has also been adopted by ATSC, DVB, and ISDB for

HDTV signal broadcasting.

53. MPEG-2 TS encapsulates PESs from multiple programs (unlike program streams) into fixed-size TS packets. Each packet is identified by a packet identifier (PID) that is unique to each program. It also contains an optional program clock reference (PCR).

54. MPEG-2 TS packets are multiplexed and transmitted over the network. The PID is used to extract the desired program from the multiplexed data stream. MPEG-2 TS that are associated with multiple programs are called Multi Program Transport Stream (MPTS); whereas MPEG-2 TS that correspond to a single program are referred to as Single Program Transport Stream (SPTS).

55. The '945 Patent describes the predefined packet identifier (PID) in MPEG-2 TS packets: "Each TS packet consists of a TS Packet header with optional Adaptation Field followed by useful data payload containing portion of a PES packet. The TS header consists of a sync byte, flags, indicators information for error detection and timing and Packet_ID (PID) field used to identify elementary stream carried underneath of a PES packet. In addition to identifying specific elementary streams, one PID is used to identify a program specific Information (PSI) table data. Each TS PSI table is sent in sections, usually occupying one or more TS packets. Four types of PSI tables exist: 1) Program Association Table (PAT) listing unique program_number (as an identifier of each program in one multiplex) and PID of the PMT table; 2) Program Map Table (PMT) listing PIDs of all component streams making a given

program. PMT may be constructed for each program separately or be common for a group of programs; 3) Conditional Access Table (CAT) identifying PID of Entitlement Management Messages and ID of used conditional access system if any scrambling of TS or PES packets is done; 4) Private Table carrying Network Information Table (NIT) or private data.” Ex. 1001, 2:18-39 (emphasis added).

D. Time Shifting

56. Generally, time shifting allows a viewer to step away from a multimedia presentation, such as a television program, without missing any part of the presentation.

57. Time shifting live programs requires receiving a multimedia data stream, such as an audio and/or video stream, and then storing the data stream in a storage device. When the viewer signals that he or she would like to pause the program, an indication of the location within the multimedia stream where the pause request had been made is recorded. Once the viewer signals that he or she wishes to resume the multimedia presentation, the stored data is retrieved and displayed from the location where the presentation was paused.

E. Clock Recovery And Timing Information

58. The location within the multimedia presentation where the data stream has been paused is typically identified by the time when the request has been made, and must be recorded in order to display the multimedia data stream from the correct location once the viewer wishes to resume the presentation.

59. As stated above, the received multimedia data stream typically includes timing information necessary for various tasks such as synchronization of distinct data streams; *e.g.*, simultaneous presentation of audio and video streams. The time when the multimedia data stream has been paused must be compared to timing information embedded in the multimedia data stream to determine the location where the stream has been paused.

60. In addition, once the viewer has indicated that he or she would like to resume the presentation of the multimedia stream, the recorded data must be sent to the decoder at the proper rate. This rate is typically also determined from the timing information embedded in the received multimedia data stream.

61. In order to ensure that the timing information generated by the receiver and the embedded timing information are compatible, they must be compared to the same clock. This is typically accomplished by embedding clock information in the received multimedia data stream and comparing it to the clock at the receiver.

62. Therefore, when recording the multimedia data stream, it is essential to also record the timing information embedded in the received data stream so that the location of the pause request and the rate at which the data should be sent to the decoder can be determined.

F. Coded Multimedia Data And Timing Information

63. The multimedia data stream is typically received and stored in coded form. As stated above, coded multimedia data streams generally arrange the data in a coding

order which allows for fast data decompression. For example, the order of frames in a coded video sequence is rearranged depending on whether the frames are compressed based on past or future frames. As a result, coded multimedia data streams will typically include timing information for both the decoding time and display time. In addition, both the decoding time and display time are generally recorded with respect to a reference clock which is usually included in the coded data stream.

64. Therefore, time shifting of coded multimedia data streams requires additional timing information. In particular, when a viewer wishes to pause the program, the timing information embedded as part of the coded multimedia data stream received must be recorded. This timing information is essential for proper decoding of the coded multimedia stream, and also used to determine the rate at which the coded multimedia stream must be sent to the decoder.

G. Real-Time Applications

65. The term “real time” is used in different contexts in different ways. In connection with multimedia data streaming, however, the term “real time” is generally used to connote that the system can process the data at a rate that is the same or higher than the rate at which the data is received. Real-time multimedia systems, therefore, ensure that all of the data received can be processed, and none of the data received must be discarded due to lack of computational or storage resources. Put simply, real-time multimedia applications must necessarily receive, process, and output

the multimedia signal in real time.

66. Real-time applications naturally impose several constraints on the processing of received multimedia data streams. For instance, multimedia data may be transmitted at a constant bit rate (CBR) or variable bit rate (VBR). Whether the data received has been sent as a CBR or VBR data stream, some data elements in the data stream need to be used immediately upon receipt; whereas other data elements in the stream must be temporarily stored until the data is required for presentation. Therefore, real-time multimedia applications typically rely on timing information to determine whether a received data element should be processed and immediately discarded, or if it should be temporarily stored prior to its presentation.

67. For example, transmission of a coded VBR video data stream includes timing information such as a decoding time stamp (DTS) and a presentation time stamp (PTS) that are used to ascertain when to decode and when to present the data, respectively. Real-time video decoding and presentation of this video data stream must therefore extract the timing information prior to storage of received data elements in temporary storage. In other words, the only way for such a system to determine whether to temporarily store data elements in the storage device is to first extract the timing information from a received data element and then decide whether the data element needs to be temporarily stored or sent directly to the decoder.

III. THE '945 PATENT

A. Background Of The '945 Patent

68. The '945 Patent relates to a method and system that enables a viewer, who may be interrupted from watching streaming video, to play back the video from the point of interruption while additional video is continually recorded.

69. This feature is known as “time shifting” a viewed program. As the use of digital video data became increasingly common, methods of transporting large amounts of various types of transport stream data have been developed. One such method is to use a multiplexed packetized data stream capable of carrying real-time multimedia programs, such as, *e.g.*, the ISO/IEC 13818-1 standard (*i.e.*, MPEG-2 Transport Stream). Such a transport stream facilitates fast programming access, channel hopping and synchronization between multiple programs within the transport stream.

70. The '945 Patent discloses a method for time-shifting such a transport stream, and more specifically, for efficient time shifting of multiplexed packetized data streams.

71. The '945 Patent discloses three time-shifting modes: a receive-only mode, a continuous time-shifting mode, and a part-time shifting mode. In the ***receive-only mode***, a digital transport stream receiver (DTSR) receives a live broadcast and

demultiplexes one program of a plurality of programs available in the live broadcast stream. This is referred to as “Transparent Mode” indicating that the transport stream is accessed immediately and not saved in a storage device, and therefore, from the point of view of the digital storage media (DSM), the received data is transparent.

72. In the ***continuous time-shifting mode***, time shifting is selected by the viewer to store part or all of a program for later viewing after a short or long intermission. During continuous time-shifting mode, a selected program from a given multiplex is received and stored on a hard disk, or other storage device, in the form of full transport stream packets.

73. In the ***part-time shifting mode***, when selected by the viewer, allows for replay of a time-shifted program or fast forward (FF) replay of a time-shifted program at user defined FF speed. In an embodiment disclosed, this time-shifting mode is the most demanding mode of the three described modes because: the host CPU system is receiving and storing a real-time event; at the same time, the host CPU is retrieving saved stream data from the storage device; simultaneously with the first two operations, the host CPU is performing transport stream de-multiplexing of video, audio, private and PSI/SI data on a host CPU; and at the same time the host CPU is restoring PCR/PTS time-base information as described later.

74. A high-level block diagram of the hardware associated with the alleged invention disclosed in the '945 Patent is shown in FIG. 6 below.

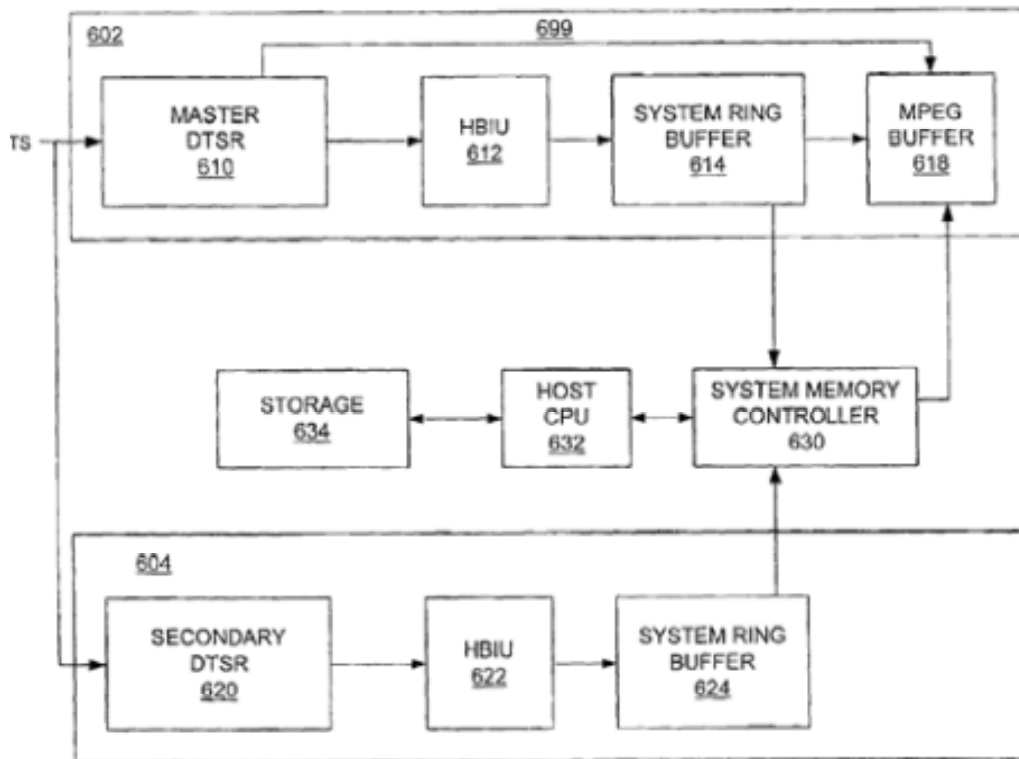


Figure 6

B. Prosecution History (Ex. 1002)

75. According to the face of the '945 Patent, U.S. Patent Application No. 09/707,060 ("the '060 application"), the application which issued as the '945 Patent, was filed on November 6, 2000.

76. The U.S. Patent and Trademark Office ("USPTO") mailed its first Office Action on October 10, 2004. In the first office action, the examiner allowed claims 18-20. Ex. 1002, at 133-134. The examiner also rejected (a) claims 21-27 under 35 USC 102 as being anticipated by U.S. Patent No. 6,792,000 to Morinaga et al. (*id.* at 124-127), (b) claims 1-13, 15 and 16 under 35 USC 103 as being obvious over Morinaga in view of U.S. Patent No. 5,521,922 to Fujinami et al. (*id.* at 127-132), and

(c) claims 14 and 17 under 35 USC 103 as being obvious over Morinaga in view of Fujinami and further in view of US Patent No. 6,233,389 to Barton (*id.* at 132-133).

77. In its response to the first office action on December 27, 2004, the applicant argued that the prior art cited did not anticipate or render the claims obvious. *Id.* at 145-148.

78. In the second office action on June 15, 2005, the examiner rejected (a) claims 21-27 under 35 U.C.S. 102 as being anticipated by U.S. Patent No. 6,148,135 to Suzuki (*id.* at 157-160), (b) claims 1-10 under 35 U.S.C. 103 as being obvious over Suzuki (*id.* at 160-164), and (c) claims 11-13, 15, and 16 under 35 U.S.C. 103 as being obvious over Suzuki in view of Morinaga (*id.* at 164-166), and (d) claims 14 and 17 under 35 U.S.C. 103 as being obvious over Suzuki in view of Morinaga and further in view of Barton (*id.* at 166-167).

79. In its response to the second office action on September 15, 2005, the applicant argued that the prior art cited did not anticipate or render the claims obvious. *Id.* at 203-205. Specifically, the applicant argued that “the system time clock (STC) 102 of Suzuki is not generated *before the multiplexed packetized data stream is stored in a storage device*, as provided by claim 21.” *Id.* at 203.

80. With respect to the examiner’s obviousness rejections, the applicant argued that “Suzuki discloses a video buffer memory 45 and an audio buffer memory 25, but makes no mention of an additional memory for storing a second portion of a packetized data stream, as recited in claim 1.” *Id.* at 204.

81. In the third office action on January 20, 2006, the examiner maintained the rejections made in the second office action on June 15, 2005. *Id.* at 212-222.

82. In response to the third office action on March 20, 2006, the applicants amended claim 21 to specify that the “storage device is to store the select[ed] packets.” *Id.* at 240. The applicant further argued that “[c]laim 21 further recites the features of a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.” *Id.* The applicants argued that claims 22-27 are thus distinguishable from Suzuki because Suzuki “fails to disclose the claimed feature of wherein the first clock recover module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.” *Id.* at 241.

83. The examiner allowed claims 1-27 in a notice of allowance issued on April 5, 2006. *Id.* at 255-258.

C. Challenged Claims

84. My analysis will focus on claims 18 and 21 of the '945 Patent. The claims themselves will be discussed in detail within the Prior Art Analysis section.

D. Claim Construction

85. I have been informed that in my analysis, I should interpret the claims to have

their broadest reasonable construction in light of the specification.

IV. PRIOR ART ANALYSIS

86. I now turn to the references applied in the grounds for rejections discussed in Petition for *inter partes* review. In my analysis, I will specifically address the following references:

No.	Reference	Referred To As
1005	U.S. Patent No. 6,233,389	Barton
1006	U.S. Patent No. 6,397,000	Hatanaka
1007	U.S. Patent No. 6,591,058	O'Connor
1008	U.S. Patent No. 5,521,922	Fujinami

A. U.S. Patent No. 6,233,389 (“Barton”)

87. Barton discloses a multimedia time-warping system using “an easily manipulated, low cost multimedia storage and display system that allows the user to view a television broadcast program with the option of instantly reviewing previous scenes within the program [and] . . . allows the user to store selected television broadcast programs while the user is simultaneously watching or reviewing another program. Ex. 1005, at 1:64-2:3.

88. Attached as Appendix D is a claim chart demonstrating where Barton discloses each of the limitations of claims 18 and 21 of the '945 Patent.

1. Claims 18 and 21 Are Anticipated By Barton

a. Claim 18

89. Claim 18 of the '945 Patent recites:

18. A method comprising: determining a mode of operation;
during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;
selecting a first program from the multiplexed packetized data stream;
decoding a video portion of the first program for display;
during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;
selecting the first program from the multiplexed packetized data stream;
storing the first program;
during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;
selecting the first program from the multiplexed packetized data stream;
storing a first program portion of the first program;
providing the first program portion to a second demultiplexer;
selecting at the second demultiplexer a video portion of the first program portion;
decoding the video portion of the first program portion for display; and
storing a second program portion of the first program simultaneous to the step of decoding.

90. Barton discloses a mode of operation. The user can watch and store programs using commands such as play, pause, fast forward and reverse. Barton specifically discloses that “[t]he invention additionally provides the user with the ability to store selected television broadcast programs while simultaneously watching or reviewing another program and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.”

Id. at 3:23-29.

91. Accordingly, Barton discloses “[a] method comprising: determining a mode of operation,” as required by claim 18.

92. Barton discloses receiving multiplexed packetized data stream at a first demultiplexer. According to Barton, “the invention has an Input Section 101, Media Switch 102, and an Output Section 103. **The Input Section 101 takes television (TV) input streams in** a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and **digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC).** DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that a TV receiver can disassemble the input stream to find programs in the multiplexed signal.” *Id.* at 3:30-43.

93. MPEG-2 Transport Stream is a standard for multiplexed packetized data streams. The MPEG-2 Transport Stream is referred to in the field as the ISO/IEC 13818-1 standard (*i.e.*, MPEG-2 Transport Stream). In fact, the ISO/IEC 13818-1 MPEG-2 Transport Stream standard is cited by both the '945 Patent and Barton as an example of a multiplexed packetized data stream. Barton further states that “[t]he Input Section 101 produces MPEG streams. **An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple**

video and audio feeds and private data. The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system. Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” *Id.* at 3:43-52 (emphasis added).

94. FIG. 3 discloses a multiplexed packetized data stream consisting of interleaved audio and video components.

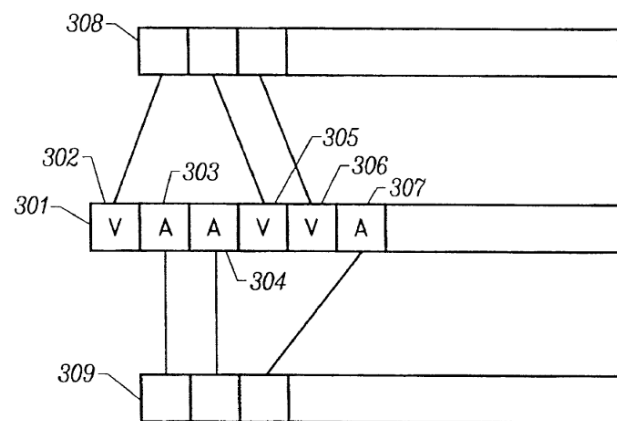


FIG. 3

95. The multiplexed packetized data stream is received at a first demultiplexer as shown by the “Input Streams” arrow pointing to “Input Module 101” of FIG. 1.

96. Accordingly, Barton discloses “during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;” as required by claim 18.

97. Barton discloses selecting a first program from the multiplexed packetized data stream.

98. According to Barton, “the invention has an Input Section 101, Media Switch

102, and an Output Section 103. The Input Section 101 takes television (TV) input streams in a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC). DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that **a TV receiver can disassemble the input stream to find programs in the multiplexed signal. The Input Section 101 produces MPEG streams.** An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds and private data. **The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system.** Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” *Id.* at 3:30-52 (emphasis added).

99. Accordingly, Barton discloses “selecting a first program from the multiplexed packetized data stream,” as required by claim 18.

100. Barton discloses decoding a video portion of the first program for display.

101. First, as shown in FIG. 7, Barton discloses an MPEG decoder that decodes a video portion of the first program for display.

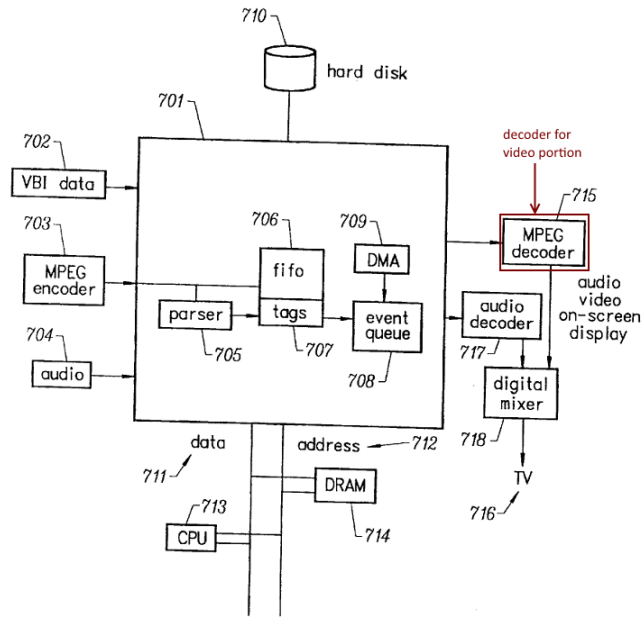


FIG. 7

102. Second, Barton explains that “[t]he video and audio components are stored on a storage device and when the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream which is sent to a decoder. The decoder converts the MPEG stream into TV output signals and delivers the TV output signals to a TV receiver.” *Id.* at Abstract.

103. Accordingly, Barton discloses “decoding a video portion of the first program for display,” as required by claim 18.

104. Barton discloses receiving the multiplexed packetized data stream at a first multiplexer during a second mode of operation. The first mode was live content. The second mode is storing this content. While the mode is different, the receiving of the multiplexed packetized data stream is the same. Barton discloses “receiving the multiplexed packetized data stream at the first demultiplexer,” as discussed above at

¶¶92-95. Accordingly, Barton discloses “during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18.

105. Barton discloses “selecting the first program from the multiplexed packetized data stream,” as discussed above at ¶¶97-98.

106. Barton also discloses storing the first program. According to Barton, “[t]he Media Switch 102 mediates between a microprocessor CPU 106, hard disk or storage device 105, and memory 104. Input streams are converted to an MPEG stream and sent to the Media Switch 102. **The Media Switch 102 buffers the MPEG stream into memory.** It then performs two operations if the user is watching real time TV: **the stream** is sent to the Output Section 103 and it is **written simultaneously to the hard disk or storage device 105.**” *Id.* at 3:62-4:2 (emphasis added). Specifically, “[t]he video and audio components are stored on a storage device. When the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream.” *Id.* at 2:26-29 (emphasis added).

107. Accordingly, Barton discloses “storing the first program,” as required by claim 18.

108. Barton discloses receiving the multiplexed packetized data stream at a first multiplexer during a third mode of operation. The first mode was live content. The second mode was storing this content. The third mode is storing and playing the

content. While the mode is different, the receiving of the multiplexed packetized data stream is the same. Barton discloses “receiving the multiplexed packetized data stream at the first demultiplexer,” as discussed above at ¶¶92-95. Accordingly, Barton discloses “during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18.

109. Barton discloses “selecting the first program from the multiplexed packetized data stream,” as discussed above at ¶¶97-98.

110. Barton discloses “storing a first program portion of the first program,” as discussed above at ¶106.

111. Barton discloses providing the first program portion to a second demultiplexer. Barton discloses that “[t]he invention **parses the resulting MPEG stream and separates it into its video and audio components.** It then stores the components into temporary buffers. Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred. The program logic is notified that an event has occurred and the data is extracted from the buffers.” *Id.* at 2:15-21 (emphasis added). In addition, “[r]eferring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. **These elements must be separated** and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the

decoders may be properly synchronized for accurate playback of the signal.” *Id.* at 4:24-33 (emphasis added). Barton explains that “[t]he input stream flows through a parser 401. The parser 401 parses the stream looking for MPEG distinguished events indicating the start of video, audio or private data segments. For example, when the parser 401 finds a video event, it directs the stream to the video DMA engine 402. . . .” *Id.* at 5:3-19.

112. Accordingly, Barton discloses “providing the first program portion to a second demultiplexer,” as required by claim 18.

113. Barton discloses selecting a video portion at the second demultiplexer. As stated above, the parser 401 separates the MPEG stream into its video and audio components. *See id.* at 2:15-21. And, as discussed above, when the parser finds a video event, it directs it to the video DMA engine 402. *See id.* at 4:24-33 and 5:3-19. Accordingly, Barton discloses “selecting at the second demultiplexer a video portion of the first program portion,” as required by claim 18.

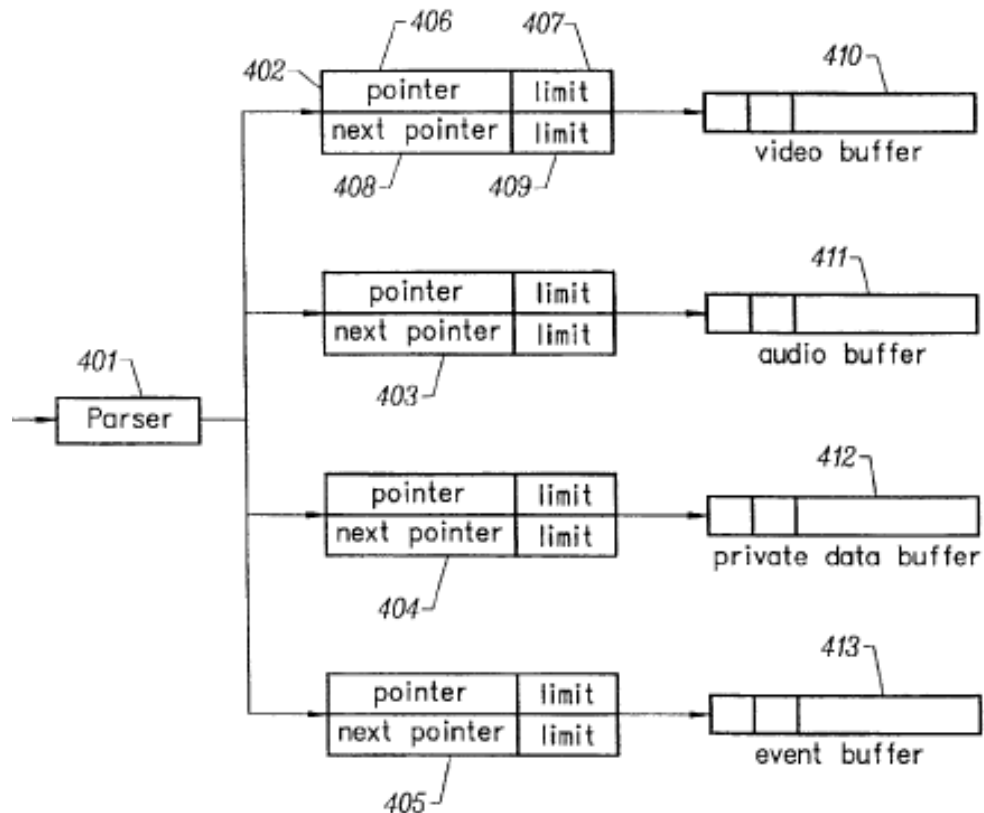


FIG. 4

114. Barton discloses “decoding the video portion of the first program portion for display,” as discussed above at ¶¶100-02.

115. Barton also discloses storing and decoding a program at the same time. According to Barton, the invention “provides the user with the ability to **store selected television broadcast programs while simultaneously watching or reviewing another program** and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.” *Id.* at 3:24-29 (emphasis added). Barton further explains that “[t]he **Media Switch 701 takes in 8-bit data and sends it to the disk, while at the same**

time extracts another stream of data off of the disk and sends it to the MPEG decoder 715. All of the DMA engines described above can be working at the same time.” *Id.* at 7:5-9 (emphasis added).

116. Accordingly, Barton discloses “storing a second program portion of the first program simultaneous to the step of decoding,” as required by claim 18.

117. Accordingly, Barton discloses all of the limitations of claim 18.

b. Claim 21

118. Claim 21 of the '945 Patent recites:

21. A system comprising:
a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;
a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;
a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;
a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and
a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.

119. Barton describes a system comprising “a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs.”

120. First, Barton discloses a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs. According to Barton, “the invention has an Input Section 101, Media Switch 102, and an Output Section 103.

The Input Section 101 takes television (TV) input streams in a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC). DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that a TV receiver can disassemble the input stream to find programs in the multiplexed signal.” Ex. 1005, at 3:30-43.

121. Second, MPEG-2 Transport Stream is a standard for multiplexed packetized data streams. The MPEG-2 Transport Stream is referred to in the field as the ISO/IEC 13818-1 standard (*i.e.*, MPEG-2 Transport Stream). In fact, the ISO/IEC 13818-1 MPEG-2 Transport Stream standard is cited by both the '945 Patent and Barton as an example of a multiplexed packetized data stream. Barton further states that “[t]he Input Section 101 produces MPEG streams. **An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with**

multiple video and audio feeds and private data. The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system. Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” *Id.* at 3:43-52 (emphasis added).

122. Third, the multiplexed packetized data stream that is received at a first input node carries real-time multimedia programs including video and audio components. Barton explains, “[r]eferring to FIG. 3, **the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments.** These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.” *Id.* at 4:23-33 (emphasis added).

123. FIG. 3 below discloses a multiplexed packetized data stream consisting of interleaved audio and video components.

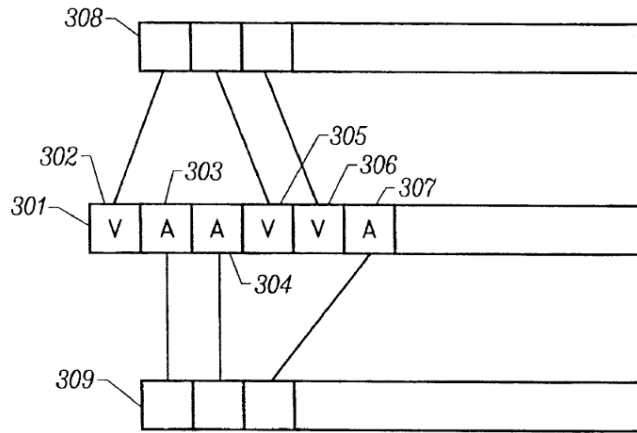


FIG. 3

124. The multiplexed packetized data stream is received at a first input node as shown by the “Input Streams” arrow pointing to “Input Module 101” of FIG. 1.

125. Accordingly, Barton discloses “[a] system comprising: a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs,” as required by the preamble of claim 21.

126. Barton discloses “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data.”

127. First, Barton discloses a first transport stream demultiplexer. According to Barton, “[i]f a digital TV signal is being processed instead, the MPEG encoder 703 is replaced with an MPEG2 Transport Demultiplexor, and the MPEG audio encoder 704 and VBI decoder 702 are deleted. The demultiplexor multiplexes the extracted audio, video and private data channel streams through the video input Media Switch port.” *Id.* at 6:30-36. Barton further discloses that “[t]he invention **parses the**

resulting MPEG stream and separates it into its video and audio components.

It then stores the components into temporary buffers. Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred. The program logic is notified that an event has occurred and the data is extracted from the buffers.” *Id.* at 2:15-21 (emphasis added). In addition, “[r]eferring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. **These elements must be separated** and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.” *Id.* at 4:24-33 (emphasis added).

128. Second, Barton inherently discloses that the packets of data selected have a predefined packet identifier. As stated above, both the ’945 Patent and Barton cite to the ISO/IEC 13818-1 MPEG-2 Transport Stream standard as an example of a multiplexed packetized data stream. The ’945 Patent describes the predefined packet identifier in MPEG-2 Transport Stream packets: “Each TS packet consists of a TS Packet header with optional Adaptation Field followed by useful data payload containing portion of a PES packet. The TS header consists of a sync byte, flags, indicators information for error detection and timing and **Packet_ID (PID) field used to identify elementary stream carried underneath of a PES packet. In**

addition to identifying specific elementary streams, one PID is used to identify a program specific Information (PSI) table data. Each TS PSI table is sent in sections, usually occupying one or more TS packets. Four types of PSI tables exist: 1) Program Association Table (PAT) listing unique program_number (as an identifier of each program in one multiplex) and PID of the PMT table; 2) Program Map Table (PMT) listing PIDs of all component streams making a given program. PMT may be constructed for each program separately or be common for a group of programs; 3) Conditional Access Table (CAT) identifying PID of Entitlement Management Messages and ID of used conditional access system if any scrambling of TS or PES packets is done; 4) Private Table carrying Network Information Table (NIT) or private data.” Ex. 1001, 2:18-39 (emphasis added).

129. Third, Barton discloses that the first transport stream demultiplexer has an input coupled to the first input node to select packets of data and an output to provide the select packets of data. According to Barton, “**The Input Section 101 produces MPEG streams.** An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds and private data. **The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system.** Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” Ex. 1005, at 3:43-52 (emphasis added). Barton further

explains, “Referring to FIG. 3, **the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers.** This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.” *Id.* at 4:24-33 (emphasis added). In addition, Barton states, “If a digital TV signal is being processed instead, the MPEG encoder 703 is replaced with an MPEG2 Transport Demultiplexor, and the MPEG audio encoder 704 and VBI decoder 702 are deleted. **The demultiplexor multiplexes the extracted audio, video and private data channel streams through the video input Media Switch port.**” *Id.* at 6:30-36 (emphasis added). And finally, Barton describes that “[a] hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. **The Media Switch 701 outputs streams** to an MPEG video decoder 715 and a separate audio decoder 717.” *Id.* at 6:62-65.

130. Accordingly, Barton discloses “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data,” as required by claim 21.

131. Barton discloses a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the

storage device is to store the select packets.

132. First, Barton discloses a storage device for storing data packets. “The Media Switch 102 mediates between a microprocessor CPU 106, hard disk or storage device 105, and memory 104. Input streams are converted to an MPEG stream and sent to the Media Switch 102. **The Media Switch 102 buffers the MPEG stream into memory.** It then performs two operations if the user is watching real time TV: the stream is sent to the Output Section 103 and **it is written simultaneously to the hard disk or storage device 105.**” *Id.* at 3:62-4:2.

133. Second, Barton discloses that the storage device has a data port coupled to the output of the first transport stream demultiplexer. According to Barton, “[a] **hard disk or storage device 710 is connected to one of the ports of the Media Switch 701.** The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717.” *Id.* at 6:62-65 (emphasis added).

134. And, third, the storage device stores select packets. Barton discloses that “[t]he video and audio components are stored on a storage device. When the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream.” *Id.* at 2:26-29.

135. The coupling of the “Hard Disk 105” and “Memory 104” to “Media Switch 102” is shown in FIG. 1. Similarly, a schematic diagram of the Media Switch is illustrated in FIG. 7, which shows the coupling of the “hard disk 710”, “DRAM 714”, and “fifo 706” to “parser 705”.

136. Accordingly, Barton discloses “a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets,” as required by claim 21.

137. Barton discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.”

138. First, Barton discloses a clock recovery module to generate a clock at the output. Barton discloses, **“The Media Switch enables the program logic to associate proper time sequence information with each segment, possibly embedding it directly into the stream. The time sequence information for each segment is called a time stamp.** These time stamps are monotonically increasing and start at zero each time the system boots up. This allows the invention to find any particular spot in any particular video segment. For example, if the system needs to read five seconds into an incoming contiguous video stream that is being cached, the system simply has to start reading forward into the stream and look for the appropriate time stamp.” *Id.* at 4:34-44 (emphasis added).

139. Second, the clock is generated based upon received timing information transmitted in packets of the multiplexed packetized data stream. As stated above, both the '945 Patent and Barton cite to the ISO/IEC 13818-1 MPEG-2 Transport

Stream standard as an example of a multiplexed packetized data stream. The '945 Patent describes the received timing information transmitted in MPEG-2 Transport Stream packets: "PES packets from various elementary streams are merged together to form a program (service) with its own system time clock (STC). **All ES component streams within one program are synchronized have periodic PTS stamps** corresponding to the STC counter to indicate the proper timing for each ES. The relatively long and most often variable length **PES packets are further packetized into shorter TS packets** having a constant size of 188 bytes. A small and constant TS packet size makes error recovery easier and faster. Usually, the transport stream carries several programs, each with its own STC. **Each TS packet consists of** a TS Packet header with optional Adaptation Field followed by useful data **payload containing portion of a PES packet. The TS header consists of** a sync byte, flags, indicators information for error detection and **timing** and Packet_ID (PID) **field** used to identify elementary stream carried underneath of a PES packet. In addition to identifying specific elementary streams, one PID is used to identify a program specific Information (PSI) table data." Ex. 1001, at 2:7-27 (emphasis added).

140. This same timing information received in the transmitted packets of the multiplexed packetized data stream is also described in Barton, which explains that "[i]f the stream was produced by encoding an analog signal, it will not contain Program Time Stamp (PTS) values, which are used by the decoders to properly present the resulting output. Thus, the program logic uses the generated time stamp

504 to calculate a simulated PTS for each segment and places that into the logical segment time stamp 607. In the case of a digital TV stream, **PTS values are already encoded in the stream. The program logic extracts this information and places it in the logical segment time stamp 607.**” Ex. 1005, at 5:40-49 (emphasis added). Consequently, Barton also discloses a first clock recovery module having an input coupled to the first input node and an output. *See id.* at 5:20-25.

141. And third, the generation of a clock at the output occurs before the select packets are stored in the storage device. Specifically, as described above, Barton discloses that the generation of a clock takes place in the “Media Switch 102”, which is located between the “Input Module 101” and the storage devices, namely the “Hard Disk 105” and “Memory 104.” *See id.* at 4:34-44; *see also id.* at FIG. 1.

142. Furthermore, Barton describes the use of the disclosed system for real-time applications. Specifically, Barton discloses that “[t]he parser and event buffer decouple the CPU from having to parse the MPEG stream and from the **real time nature of the data streams** which allows for slower CPU and bus speeds and translate to lower system costs.” *Id.* at Abstract (emphasis added); *see also id.* at 2:22-25. Specifically, Barton states that “the invention relates to the real time capture, storage, and display of television broadcast signals.” *Id.* at 1:6-8. Barton further explains that “[t]his invention utilizes an easily manipulated, low cost, multimedia storage and display system that allows the user to view a television broadcast program with the **option of instantly reviewing previous scenes within the program.**” *Id.*

at 1:64-67 (emphasis added). Finally, Barton explains that “[t]he user can switch to any video feed and examine (i.e., rewind, play, slow play, fast forward, etc.) a specific segment of the recorded video while **the external VCRs are being loaded with the real-time input video.**” *Id.* at 12:29-32(emphasis added). Because Barton discloses real-time applications, it inherently discloses that the generation of a clock at the output occurs before the select packets are stored in the storage device. More particularly, the only way for the system disclosed to determine whether to store packets in the storage device is to first extract the timing information from a packet and then decide whether the packet needs to be stored or sent directly to the decoder.

143. Accordingly, Barton discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device,” as required by claim 21.

144. Barton discloses “a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.”

145. First, Barton discloses a decoder having a first input coupled to the output of the first clock recovery module to receive the clock. In particular, Barton explains that “[i]f the stream was produced by encoding an analog signal, it will not contain

Program Time Stamp (PTS) values, which are used by the decoders to properly present the resulting output. Thus, the program logic uses the generated time stamp 504 to calculate a simulated PTS for each segment and places that into the logical segment time stamp 607. In the case of a digital TV stream, **PTS values are already encoded in the stream. The program logic extracts this information and places it in the logical segment time stamp 607.**” *Id.* at 5:40-49 (emphasis added).

146. Second, Barton discloses a second input coupled the data port of the storage device to receive the select packets. In particular, Barton discloses an MPEG decoder that decodes a video portion of the first program for display. Barton explains that “[t]he video and audio components are stored on a storage device and when the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream which is sent to a decoder. The decoder converts the MPEG stream into TV output signals and delivers the TV output signals to a TV receiver.” *Id.* at Abstract.

147. Further, the coupling of the “MPEG decoder 715” to the storage devices—namely, the “hard disk 710”, “DRAM 714” and “fifo 706”—through the Media Switch, is illustrated in FIG. 7 below.

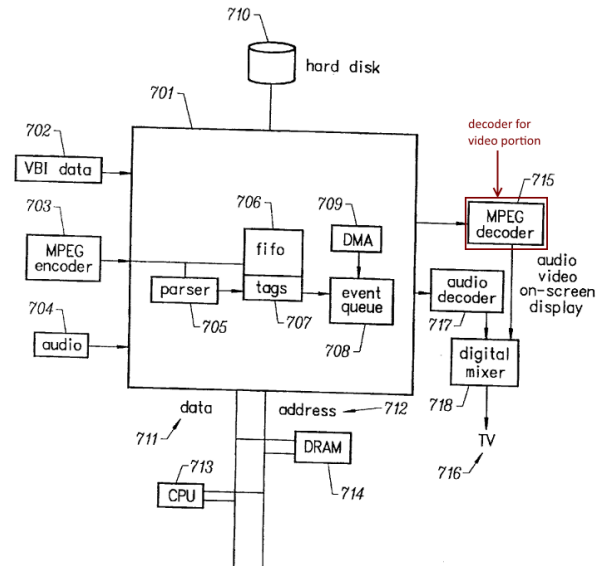


FIG. 7

148. Barton also explains that “[a] hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717.” *Id.* at 6:62-65.

149. Third, Barton discloses an output to provide decoded real-time data. Barton discloses that “[t]he decoder converts the MPEG stream into TV output signals and delivers the TV output signals to a TV receiver.” *Id.* at Abstract. Barton explains that “[t]he Output Section 103 takes MPEG streams as input and produces an analog TV signal according to the NTSC, PAL, or other required TV standards. The Output Section 103 contains an MPEG decoder, On-Screen Display (OSD) generator, analog TV encoder and audio logic.” *Id.* at 4:3-7 (emphasis added). Further, as explained above, Barton describes the use of the disclosed system for real-time applications. Because Barton discloses that the input video stream can

be used for real-time applications, the system disclosed by Barton must necessarily receive, decode, and output the video signal in real time for display. Therefore, Barton inherently discloses the output of decoded real-time video data. *See, e.g., id.* at 1:6-8.

150. Accordingly, Barton discloses “a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data,” as required by claim 21.

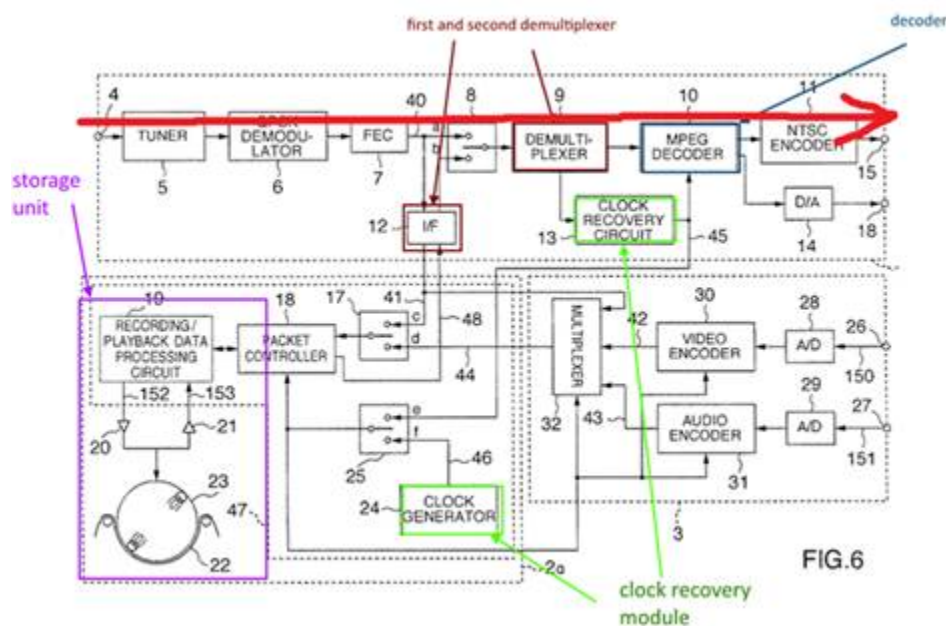
151. Accordingly, Barton discloses all of the limitations of claim 21.

B. U.S. Patent No. 6,397,000 (“Hatanaka”)

152. Hatanaka is directed to “digital signal recording devices, digital signal recording/playback devices, and digital signal receiving/recording/playback devices, for receiving/recording/playing back a digital signal.” Ex. 1006, at 1:8-11.

153. Hatanaka discloses that receiving systems were known. According to Hatanaka, “JP-A-8-98164 discloses a receiving system and a recording/playing back device for receiving/recording a transmitted multiplexed digital signal as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for receiving a transmitted multiplexed digital information signal and for selecting desired information, and recording means for recording the information received by the

receiving means.” *Id.* at 1:12-20. These prior art systems, however, could not convert analog TV signals to digital signals and record/playback a digital signal. *Id.* at 1:21-25. Hatanaka discloses a digital recording device that addresses this issue.



packetized data stream at the first demultiplexer;
selecting the first program from the multiplexed packetized data stream;
storing a first program portion of the first program;
providing the first program portion to a second demultiplexer;
selecting at the second demultiplexer a video portion of the first program portion;
decoding the video portion of the first program portion for display; and
storing a second program portion of the first program simultaneous to the step of decoding.

159. Hatanaka discloses determining a mode of operation. Modes of operation include recording and playback. For example, Hatanaka discloses **“[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet,** using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10.” Ex. 1006, at 3:16-22 (emphasis added). Further, Hatanaka discloses “[w]hen the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected

by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information.” *Id.* at 3:42-54.

160. Accordingly, Hatanaka discloses “[a] method comprising: determining a mode of operation,” as required by claim 18.

161. Hatanaka discloses during a first mode of operation, receiving a multiplexed packetized data stream at a first demultiplexer.

162. First, Hatanaka discloses receiving a multiplexed packetized data stream. Hatanaka discloses that “FIG. 2 shows a composition of a **transmitted digital broadcasting signal**. As shown in a packet composition of FIG. 2(A), **the transmission signal has a packet composition** of 204 bytes; a 4-byte header 50; a 184-byte data 51 **representing information on a video, audio, added data, etc.,** compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. **The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B).** Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis. . . .” *Id.* at 2:51-3:6 (emphasis added).

163. In fact, Hatanaka makes clear that receiving a multiplexed packetized data stream was well known in the prior art: “JP-A-8-98164 discloses **a receiving system**

and a recording/playing back device **for receiving/recording a transmitted multiplexed digital signal as a conventional technique** for recording/playing back a digital signal. This prior art publication describes a receiving system which includes **receiving means for receiving a transmitted multiplexed digital information signal** and for selecting desired information, and recording means for recording the information received by the receiving means.” Ex. 1006, at 1:12-20 (emphasis added).

164. Hatanaka also discloses receiving the multiplexed packetized data stream at a first demultiplexer. Hatanaka explains that “[w]hen the **broadcasting signal is outputted from the present device**, the playback changeover switch 8 is set at a contact to **input the output from the FEC 7** to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. . . . The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video

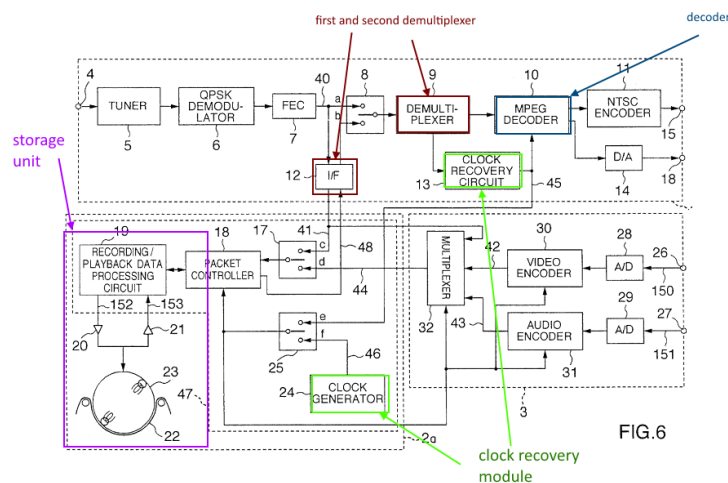
output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.” *Id.* at 3:16-41 (emphasis added).

165. Similarly, Hatanaka states that “[w]hen the received signal is recorded in the recording/playback device 2, **the output from the FEC 7 is inputted to the interface 12**, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35.

166. Hatanaka further explains that “[w]hile in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the**

demultiplexer 9 or packet control circuit 18.” *Id.* at 9:6-13 (emphasis added).

167. Thus, as shown in FIG. 6, Hatanaka illustrates receiving a multiplexed packetized data stream at a first demultiplexer, for example, interface 12, which connects to multiplexer 32.



168. Accordingly, Hatanaka discloses “during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer,” as required by claim 18.

169. Hatanaka discloses selecting a first program from the multiplexed packetized data stream. Hatanaka explains that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to **demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program,** and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information

representing the time when compression took place in a broadcasting station concerned.” *Id.* at 3:16-26 (emphasis added).

170. Hatanaka further explains that the first demultiplexer, interface 12, also selects packets. Hatanaka describes the use of interface 12 coupled to the input from FEC 7 to select packets of data and an output to provide the select packets of data. Hatanaka states that “[w]hen the received signal is recorded in the recording/playback device 2, **the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9.** When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35. More particularly, Hatanaka explains that “[w]hile in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection**

of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.” *Id.* at 9:6-13 (emphasis added).

171. Accordingly, Hatanaka discloses “selecting a first program from the multiplexed packetized data stream,” as required by claim 18.

172. Hatanaka discloses decoding a video portion of the first program for display. Specifically, Hatanaka discloses MPEG decoder 10 for decoding a video portion of a program. Hatanaka discloses that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., **relating to a specified program, and then outputs these packets to the MPEG decoder 10.** The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. **The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received**

separating signal and the data clock 45 reproduced by the clock reproducing unit 13, **and provides decoded video/audio signals.** The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.” *Id.* at 3:16-41 (emphasis added). Hatanaka also explains that “[i]n playback, the user selects one of the digital and analog broadcasts, the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, **and inputs the selected program packet to the MPEG decoder 10 to obtain the video and audio of the desired program.**” *Id.* at 6:47-52 (emphasis added).

173. Accordingly, Hatanaka discloses “decoding a video portion of the first program for display,” as required by claim 18.

174. Hatanaka discloses receiving the multiplexed packetized data stream at a first multiplexer during a second mode of operation. The first mode was live content. The second mode is storing this content. While the mode is different, the receiving of the multiplexed packetized data stream is the same. Hatanaka discloses “receiving the multiplexed packetized data stream at the first demultiplexer,” as discussed above at ¶¶162-67. Accordingly, Hatanaka discloses “during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18.

recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35.

179. More particularly, Hatanaka explains that “[w]hile in the above the **magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used.** Although not shown in FIGS. 1 and 6, a deciphering circuit which deciphers a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.**” *Id.* at 9:6-13 (emphasis added).

180. Accordingly, Hanataka discloses “storing the first program,” as required by claim 18.

181. Hatanaka discloses receiving the multiplexed packetized data stream at a first multiplexer during a third mode of operation. The first mode was live content. The second mode was storing this content. The third mode is storing and playing the content. While the mode is different, the receiving of the multiplexed packetized data stream is the same. Hatanaka discloses “receiving the multiplexed packetized data stream at the first demultiplexer,” as discussed above at ¶¶162-67. Accordingly, Hatanaka discloses “during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18.

182. Hatanaka discloses “selecting the first program from the multiplexed packetized data stream,” as discussed above at ¶¶169-70.

183. Hatanaka discloses “storing a first program portion of the first program,” as discussed above at ¶¶176-79.

184. Hatanaka discloses providing the first program portion to a second demultiplexer. Hatanaka discloses that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station

concerned.” *Id.* at 3:16-26 (emphasis added). More particularly, Hatanaka explains that “[w]hile in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.**” *Id.* at 9:6-13 (emphasis added).

185. Accordingly, Hatanaka discloses “providing the first program portion to a second demultiplexer,” as required by claim 18.

186. Hatanaka also discloses that the second demultiplexer selects a video portion of the program. As stated above, demultiplexer 9 separates packets relating to video, which are outputted to the MPEG decoder 10. Hatanaka discloses that “[i]n playback, the user selects one of the digital and analog broadcasts, **the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the MPEG decoder 10 to obtain the video** and audio of the desired program.” *Ex.* 1006, at 6:47-52 (emphasis added). Hatanaka also discloses that demultiplexer 9 selects a broadcasting station and outputs only the packet required for the MPEG decoder 10 for video signals. *See id.* at 4:22-35. Accordingly, Hatanaka discloses “selecting at the second demultiplexer a video portion of the first program portion,”

as required by claim 18.

187. Hatanaka discloses “decoding the video portion of the first program portion for display,” as discussed above at ¶172.

188. Storing a second program portion of the first program simultaneous to the step of decoding would have been obvious in view of Hatanaka.

189. Hatanaka discloses recording: “When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17. As shown in the main data of FIG. 3A, the packet control circuit 18 divides 188-byte packet data into 92-byte packet data A 99 and 96-byte packet data B 100, and adds 4-byte packet header 98 to the packet data A 99. The packet control circuit 18 also produces in the packet header 98 a time stamp, shown in a hatched area 102, which is data on a time when the packet is received.” Ex. 1006, at 3:42-63.

190. Hatanaka also discloses playback. *See id*; *see also id.* at FIG. 6. Hatanaka discloses that the “prior art system is capable of recording/playing back an incoming digital signal as it is” *Id.* at 1:21-22.

191. “Storing a second program portion of the first program simultaneous to the step of decoding” would have been obvious to a person of ordinary skill in the art in view of Hatanaka because Hatanaka discloses a system that allows one to simultaneously record and decode different portions of a program. Accordingly, “storing a second program portion of the first program simultaneous to the step of decoding,” as required by claim 18, is obvious in view of Hatanaka.

192. Accordingly, Hatanaka discloses all of the limitations of claim 18.

2. Claim 21 Is Anticipated By Hatanaka

a. Claim 21

193. Claim 21 of the '945 Patent recites:

21. A system comprising:
a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;
a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;
a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;
a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of

the multiplexed packetized data stream before the select packets are stored in the storage device; and a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.

194. Hatanaka discloses a system comprising “a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs.”

195. First, Hatanaka discloses receiving a multiplexed packetized data stream that carries real-time multimedia programs. Hatanaka discloses that “FIG. 2 shows a composition of a **transmitted digital broadcasting signal**. As shown in a packet composition of FIG. 2(A), **the transmission signal has a packet composition** of 204 bytes; a 4-byte header 50; a 184-byte data 51 **representing information on a video, audio, added data, etc.**, compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. **The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis. . . .**” *Id.* at 2:51-3:6 (emphasis added).

196. In fact, Hatanaka makes clear that receiving a multiplexed packetized data stream was well known in the prior art: “JP-A-8-98164 discloses **a receiving system**

and a recording/playing back device **for receiving/recording a transmitted multiplexed digital signal as a conventional technique** for recording/playing back a digital signal. This prior art publication describes a receiving system which includes **receiving means for receiving a transmitted multiplexed digital information signal** and for selecting desired information, and recording means for recording the information received by the receiving means.” Ex. 1006, at 1:12-20 (emphasis added).

197. Second, Hatanaka discloses a first input node to receive the multiplexed packetized data stream. Hatanaka explains that “[w]hen the **broadcasting signal is outputted from the present device**, the playback changeover switch 8 is set at a contact to **input the output from the FEC 7** to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. . . . The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video

output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.” 3:16-41 (emphasis added).

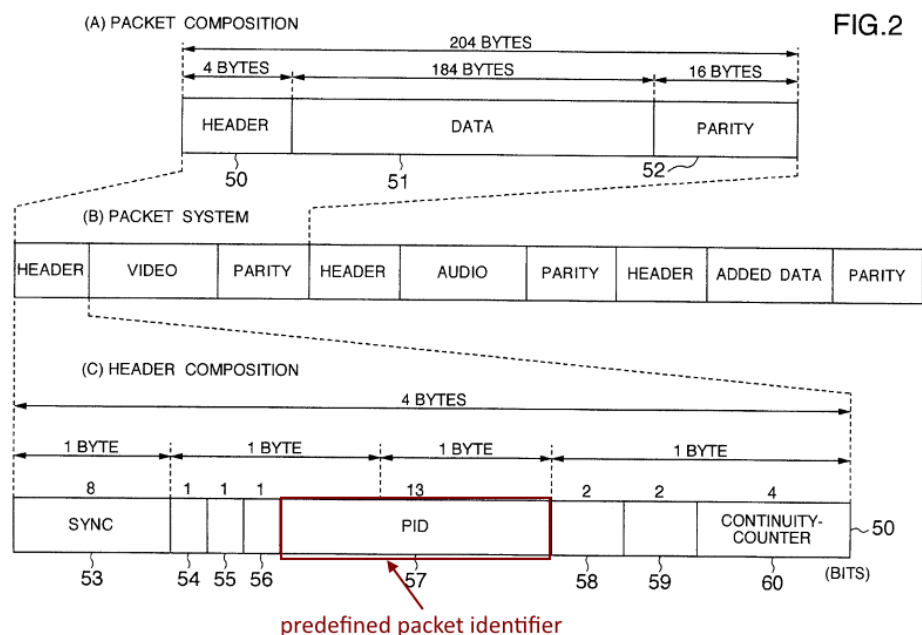
198. Similarly, Hatanaka states that “[w]hen the received signal is recorded in the recording/playback device 2, **the output from the FEC 7 is inputted to the interface 12**, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35.

199. Accordingly, Hatanaka discloses “[a] system comprising: a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs,” as required by claim 21.

200. Hatanaka discloses “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data.”

201. Hatanaka describes the use of demultiplexer 9 coupled to the input from FEC 7 to select packets of data using PID 57 and an output to provide the select packets of data. Hatanaka discloses that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to **input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets** to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned.” *Id.* at 3:16-26 (emphasis added).

202. FIG. 2 shows that a packet header includes predefined identifying information.



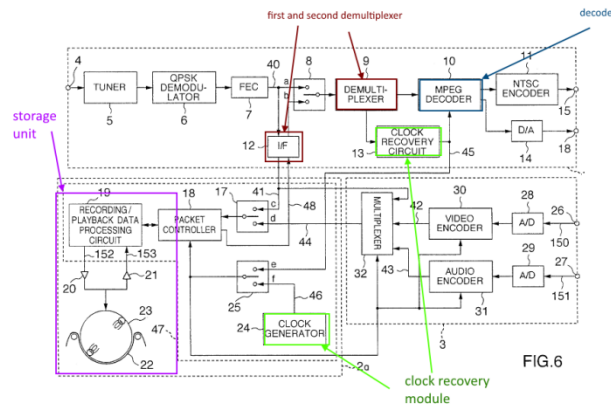
203. Similarly, Hatanaka describes the use of interface 12 coupled to the input from FEC 7 to select packets of data and an output to provide the select packets of data. Hatanaka states that “[w]hen the received signal is recorded in the recording/playback device 2, **the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9.** When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35. More particularly, Hatanaka explains that “[w]hile in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.**” *Id.* at 9:6-13 (emphasis added).

204. Accordingly, Hatanaka discloses “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data,” as required by claim 21.

205. Hatanaka discloses “a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets.”

206. Hatanaka discloses a storage device and refers to it as “recording/playback device 2.” For instance, Hatanaka describes that “FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), **2 a recording/playback device**, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner,” *Id.* at 2:30-50 (emphasis added); *see also id.*, FIGS. 1, 6, 9 and 10.

207. Hatanaka discloses that the storage device has a data port coupled to the output of the first transport stream demultiplexer as illustrated in FIG. 6.



208. Hatanaka further discloses that recording/playback device 2 has a data port coupled to the output of the demultiplexer to receive the select packets and store the select packets. Hatanaka explains that “[w]hen the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” *Id.* at 3:42-56 (emphasis added); *see also id.* at 4:16-35.

209. More particularly, Hatanaka explains that “[w]hile in the above the magnetic

tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.”** *Id.* at 9:6-13 (emphasis added).

210. Accordingly, Hatanaka discloses “a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets,” as required by claim 21.

211. Hatanaka discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.”

212. Hatanaka discloses a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream. Specifically, Hatanaka discloses a clock recovery unit 13 and packet controller 18. *See id.* at 2:41, *see also also id.* FIGS. 1 and 6.

213. More particularly, Hatanaka states, “When the broadcasting signal is outputted from the present device, the playback changeover switch **8** is set at a contact to input the output from the FEC **7** to **demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.”** *Id.* at 3:16-41 (emphasis added).

214. Hatanaka makes clear that the generation of a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream occurs **before the select packets are stored in the storage device**. In particular, Hatanaka explains that “at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, the time stamp **102** is added in the packet control circuit **18**. *Id.* at 4:38-42.

215. Hatanaka further clarifies that the clock is generated **before the select packets are stored in the storage device** when it discloses that “[i]n recording, as shown in FIGS. 7A-7D, the respective broadcasting (BR), video (VI), and audio (AU) packets of the broadcasting stream 41, video stream 42, and audio stream 43 are multiplexed on a time divisional basis and **PMT and PCR are added to the multiplexed packets to constitute a multiplexed stream**. In this case, the PAT is already contained in the broadcasting stream 41 (shown by a packet 130 of FIG. 7A), but only contains information on a program contained in the broadcasting stream. Thus, the information should be converted so as to include information on the analog broadcasting. In FIG. 7D, reference numeral 131 denotes a PAT converted by the multiplexer 32. In this case, the packet control circuit 18 uses the data clock 45 produced by the clock recovery unit 13. Thus, the clock changeover switch is set at a contact e, and the video and audio encoders 30 and 31 also use the decoder clock 45. In playback, the clock changeover switch 25 is

set at a contact f to use the fixed clock 46.” *Id.* at 6:28-46 (emphasis added).

216. Hatanaka also discloses the use of the disclosed system for real-time applications because it explains that the system disclosed will output data at a fixed transfer rate that is higher than the transmission rate: “As shown in FIGS. 5A-5E, the multiplexer **32** temporarily stores the video and audio streams **42** and **43**, and outputs them as the video and audio packet streams **45** and **46** at the same transfer rate. **The multiplexer 32 further outputs both the packets 45 and 46 in a time divisional manner onto a signal at a fixed transfer rate, which is generally higher than the sum of the transmission rates of the video and audio streams 42 and 43.**” *Id.* at 5:26-33 (emphasis added). Because Hatanaka discloses real-time applications, it inherently discloses that the generation of a clock at the output occurs before the select packets are stored in the storage device. More particularly, the only way for the system disclosed to determine whether to store packets in the storage device is to first extract the timing information from a packet and then decide whether the packet needs to be stored or sent directly to the decoder.

217. Accordingly, Hatanaka discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device,” as required by claim 21.

218. Hatanaka discloses “a decoder having a first input coupled to the output of the

first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.”

219. Hatanaka discloses that the MPEG decoder 10 has a first input coupled to the output of the clock recovery unit 13 to receive the clock, and a second input coupled the data port of the recording/playback device 2 and packet controller 18 to receive the select packets, and an output to provide decoded video signal. Hatanaka discloses that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and **then outputs these packets to the MPEG decoder 10.** The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. **The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45**

reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.” *Id.* at 3:16-41 (emphasis added).

220. Hatanaka further describes how the MPEG decoder 10 has a second input coupled the data port of the recording/playback device 2 and packet controller 18 to receive the select packets: “In reproduction, a signal 153 reproduced by the rotary head 23 is inputted via the playback amplifier 21 to the recording/playback data processing circuit 19, which detects the sync signal 92, signals ID1 (93), ID2 (94), etc., and corrects errors, using the CIP 101, C2P 76, etc., extracts packet data A 99 and packet data B 100, and then sends those data to the packet control circuit 18. **The packet control circuit 18 outputs the respective packets at the same intervals of time as in the recording in accordance with the time stamp 102 added when the data was recorded**, and then sends those packets via the interface 12 to the playback changeover switch 8. When a reproduced picture is to be obtained, the playback changeover switch 8 is set at the contact b to thereby send a reproduced packet to the demultiplexer 9. The demultiplexer 9 automatically selects a broadcasting station on the basis of the packet of program information which was selected and converted by the interface 12 when the data was recorded, and **outputs**

only a packet required for the MPEG decoder 10. Video/audio signals are obtained in a manner similar to that in which an output is obtained from a broadcasting signal.” Ex. 1006, at 4:16-35 (emphasis added).

221. Hatanaka also discloses that “in playback, the data clock 45 used in the MPEG decoder 10 is required to obtain the same frequency as it was compressed in the broadcasting station. To this end, at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, the time stamp 102 is added in the packet control circuit 18. **In playback, the respective packets are outputted by the packet control circuit 18 in accordance with the time stamps 102 to maintain the time intervals at which the packets are outputted.** To this end, clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18.” *Id.* at 4:36-50 (emphasis added).

222. As a result, Hatanaka explains that “[i]n playback, the user selects one of the digital and analog broadcasts, the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the MPEG decoder 10 to obtain the video and audio of the desired program.” *Id.* at 6:47-52.

223. The coupling of the MPEG decoder 10 to the output of the clock recovery unit

13 and the data port of the recording/playback device 2 via packet controller 18 and demultiplexer 9 is further illustrated in FIGS. 1 and 6.

224. Hatanaka also discloses an output to provide decoded real-time data. As discussed above, Hatanaka explains that “[t]he MPEG decoder 10 . . . provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15.” *Id.* at 3:16-41. Further, as explained above, Hatanaka describes the use of the disclosed system for real-time applications. Because Hatanaka discloses that the input video stream can be used for real-time applications, the system disclosed by Hatanaka must necessarily receive, decode, and output the video signal in real time for display. Therefore, Hatanaka inherently discloses the output of decoded real-time video data. *See id.* at 5:26-33.

225. Accordingly, Hatanaka discloses “a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data,” as required by claim 21.

226. Accordingly, Hatanaka discloses all of the limitations of claim 21.

C. U.S. Patent No. 6,591,058 (“O’Connor”)

227. O’Connor discloses that “a portion of the video stream may be stored in digital storage media at one instance while in the next instance another portion of the stream

is being read out of the storage media. Ex. 1007, at Abstract.

228. O'Connor discloses a technique to improve video streaming devices by providing for simultaneous recording and playback of the video stream. *Id.* at 4:9-24, 5:19-33.

229. Attached as Appendix F is a claim chart demonstrating where Hatanaka in view of O'Connor discloses each of the limitations of claim 18 of the '945 Patent.

1. Claim 18 Is Obvious Over Hatanaka In View of O'Connor

a. Claim 18

230. Claim 18 of the '945 Patent recites:

18. A method comprising: determining a mode of operation;
during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;
selecting a first program from the multiplexed packetized data stream;
decoding a video portion of the first program for display;
during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;
selecting the first program from the multiplexed packetized data stream;
storing the first program;
during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;
selecting the first program from the multiplexed packetized data stream;
storing a first program portion of the first program;
providing the first program portion to a second demultiplexer;
selecting at the second demultiplexer a video portion of the first program portion;

decoding the video portion of the first program portion for display; and
storing a second program portion of the first program simultaneous to the step of decoding.

231. Hatanaka discloses “[a] method comprising: determining a mode of operation,” as required by claim 18, and as discussed above at ¶¶159-60.

232. Hatanaka discloses “during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer,” as required by claim 18, and as discussed above at ¶¶161-68.

233. Hatanaka discloses “selecting a first program from the multiplexed packetized data stream,” as required by claim 18, and as discussed above at ¶¶169-71.

234. Hatanaka discloses “decoding a video portion of the first program for display,” as required by claim 18, and as discussed above at ¶¶172-73.

235. Hatanaka discloses “during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18, and as discussed above at ¶174.

236. Hatanaka discloses “selecting the first program from the multiplexed packetized data stream,” as required by claim 18, and as discussed above at ¶175.

237. Hanataka discloses “storing the first program,” as required by claim 18, and as discussed above at ¶¶176-80.

238. Hatanaka discloses “during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer,” as required by claim 18,

and as discussed above at ¶181.

239. Hatanaka discloses “selecting the first program from the multiplexed packetized data stream,” as required by claim 18, and as discussed above at ¶182.

240. Hatanaka discloses “storing a first program portion of the first program,” as required by claim 18, and as discussed above at ¶183.

241. Hatanaka discloses “providing the first program portion to a second demultiplexer,” as required by claim 18, and as discussed above at ¶¶184-85.

242. Hatanaka discloses “selecting at the second demultiplexer a video portion of the first program portion,” as required by claim 18, and as discussed above at ¶186 .

243. Hatanaka discloses “decoding the video portion of the first program portion for display,” as required by claim 18, and as discussed above at ¶187.

244. Hatanaka discloses “storing a second program portion of the first program simultaneous to the step of decoding,” as discussed above at ¶¶188-91.

245. O’Connor discloses simultaneously storing and decoding video data streams. Specifically, O’Connor discloses simultaneous recording and playback of the video stream.

246. Referring to FIG. 3, O’Connor “shows an embodiment of a method for **retrieving a portion of the video stream from the random access storage unit while continuing to record the incoming video stream** in accordance with the invention, although the invention is not restricted to this embodiment. In the disclosed embodiment, the substantially **simultaneous recording and playback of**

the video stream is performed by multiplexing or alternately storing the video stream to the random access storage unit and reading of the video stream from the random access storage unit. The multiplexed or alternated stores and reads may occur quickly enough that the user does not notice an appreciable delay in the playback of the video stream, and the incoming video stream is not lost, e.g., **all of the video stream is recorded. Thus, the record and playback are substantially simultaneous from the user's point of view.**” Ex. 1007, at 4:9-24 (emphasis added).

247. O’Connor also explains that “[a] user may initiate a playback cycle following block 506. For example, this may occur when the **user wishes to re-view a video clip that he just saw.** In one embodiment, the user stops recording to the temporary buffer and plays back the last portion of the temporary buffer. However, it **may be more desirable to the user to be able to continue recording as shown at block 508.** A record and playback cycle (as described with respect to FIG. 2) is started, in which the **incoming video stream is recorded while the user re-views the last portion of the temporary buffer. In this manner, after re-viewing the desired video clip, the user can resume sequentially watching the video stream from the current point of the incoming video for substantially simultaneous playback and record.**” *Id.* at 5:19-33 (emphasis added).

248. According to O’Connor, simultaneous recording and decoding has benefits to the user. O’Connor explains that “[t]imeshifting by substantially simultaneously recording and playing back a data stream enables the following type of

benefits/features for an end-user. While watching the season premiere of a television show, the viewer can literally “pause” the program in order to get up and answer the phone or get a snack from the refrigerator. After the interruption, the viewer can **resume watching again without having missed anything.** If the viewer came home 15 minutes late for the show but had started recording the program from the beginning, the viewer can begin watching right away instead of waiting for the show to be over and then rewinding the cassette tape. Also **the viewer can replay scenes during a “live” broadcast** (e.g. season premiere of a show or sporting event) in case the viewer missed a line or an exciting play. In addition, while watching a sports event the user can rewind back to a controversial play, replay the play in slow motion, and stop at the exact instance when the catch was made. To get a better view, the viewer can zoom in on a portion of the screen and apply image sharpening filters to magnify one part of the screen. *Id.* at 11:58-12:10 (emphasis added). O’Connor also discloses that “[b]ecause there is no need to decompress the data, **the speed of storage may be greatly increased** and the computational complexity may be reduced. **This facilitates a system which substantially simultaneously records and plays back a data stream,** of the type described herein, since large amounts of data may be stored at one time and the resources of the system may be taxed in undertaking this process. *Id.* at 16:3-10 (emphasis added).

249. Thus, O’Connor discloses simultaneous recording and playback of the video

stream. Playback of a video stream necessarily includes decoding the video stream. Therefore, O'Connor discloses storing and decoding a video stream at the same time.

250. It would have been obvious to one of skill in the art to combine O'Connor with Hatanaka because both are in the field of video streaming. Ex. 1007, at 1:14-16; Ex. 1006, at 1:29-35. Specifically, both O'Connor and Hatanaka relate to recording and playback of video streams. Additionally, both relate to time shifting in video systems. Ex. 1007, at 3:58-60; Ex. 1006, at 9:14-21. Because the techniques taught by O'Connor have been used to improve video streaming devices, a person of ordinary skill in the art would have been motivated to apply O'Connor's techniques to improve the video streaming device of Hatanaka.

251. Accordingly, Hatanaka in view of O'Connor discloses "storing a second program portion of the first program simultaneous to the step of decoding," as required by claim 18.

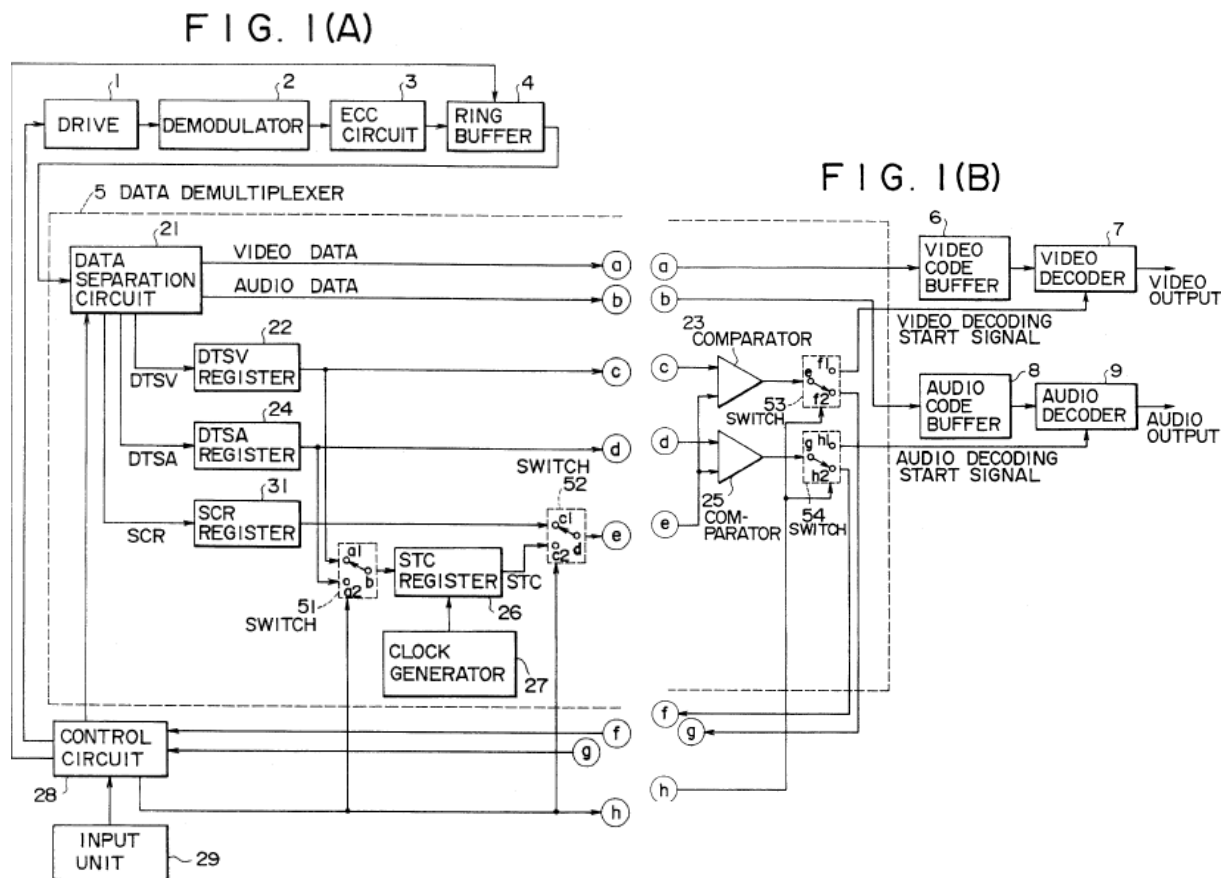
252. Accordingly, Hatanaka in view of O'Connor discloses all of the limitations of claim 18.

D. U.S. Patent No. 5,521,922 ("Fujinama")

253. Fujinama is directed to a data multiplexer. Fujinami discloses "a data demultiplexer adapted for producing time-division multiplex data recorded on an optical disk or the like and separating the same into video data and audio data." Ex. 1008, at 1:5-8.

254. The architecture of the data multiplexer system disclosed by Fujinami is depicted in FIGS. 1(A) and 1(B). Fujinami discloses multiplex bit streams composed of packets containing a pack header supplied to a data demultiplexer 5. *Id.* at 1:28-39. Fujinami discloses that the data demultiplexer 5 separates the multiplex bit stream into video and audio data as well as timing data such as SCR (system clock reference) and DTS (decoding time stamp). *Id.* at 1:22-27. The extracted video and audio data are then stored in video code buffer 6 and audio code buffer 8, respectively, whereas the timing information is stored in STC registers 26 and DTS registers 22 and 24 (for video and audio, respectively). *Id.* at 2:28-35. Finally, the stored video and audio data is read and supplied to video decoder 7 and audio decoder 9 along with a video and audio decoding start signal generated by comparators 23 and 25, respectively, based on the timing information. *Id.* at 2:6-15.

255. Attached as Appendix G is a claim chart demonstrating where the limitations of claim 21 of the '945 Patent are obvious over Fujinami.



1. Claim 21 Is Obvious Over Fujinami

a. Claim 21

256. Claim 21 of the '945 Patent recites:

21. A system comprising:
 - a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;
 - a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;
 - a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;
 - a first clock recovery module having an input coupled to

the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and
a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.

257. Fujinami describes a system comprising “a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs.”

258. Fujinami discloses receiving data from an optical disk via ring buffer 4. Fujinami explains that “the control circuit 28 sends a command to the drive 1 to thereby reproduce the data recorded on an optical disk incorporated in the drive 1. The reproduced data outputted from the drive 1 is supplied to the demodulator 2, and the demodulated data obtained therefrom is supplied to the ECC circuit 3 where a process of error detection and correction is executed. **The data thus processed is supplied via the ring buffer 4 to the data separation circuit 21 in the data demultiplexer 5.**” Ex. 1008, at 2:19-27 (emphasis added).

259. Fujinami discloses that the data supplied to data demultiplexer 5 contains real-time multimedia programs. Fujinami states, “**The data demultiplexer 5 has a data separation circuit 21 which demultiplexes the data supplied from the ring buffer 4 to thereby separate the same into video data and audio data, and further into timing data such as SCR (system clock reference) and DTS (decoding**

time stamp) inclusive of DTSV for the video data and DTSA for the audio data.” *Id.* at 1:22-27 (emphasis added).

260. Fujinami discloses that the data supplied to data demultiplexer 5 is a multiplexed bit stream (*i.e.*, multiplexed packetized data stream) composed of one or more packets: **“The format of the data supplied to the data demultiplexer 5 is so standardized as shown in FIG. 6 for example. This format is prescribed as a multiplex bit stream in the MPEG (ISO11172). As shown in FIG. 6, a multiplex bit stream is composed of one or more packs (PACKS), each of which is composed of one or more packets (PACKETS). A pack header (PACK HEADER) is disposed at the top of each pack and has a pack start code (PACK START CODE) indicating a start point of the pack, and also SCR and MUX__RATE. This SCR indicates the time when the last byte is inputted to the data demultiplexer 5 (the time when demultiplexing is started), and the MUX__RATE signifies a transfer rate.”** *Id.* at 1:28-39 (emphasis added).

261. Accordingly, Fujinami discloses “[a] system comprising: a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs,” as required by claim 21.

262. Fujinami discloses “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data.”

263. First, Fujinami discloses a first transport stream demultiplexer. In Fujinami,

the demultiplexer is data demultiplexer 5. Specifically, Fujinami discloses that “[t]he data demultiplexer 5 has a data separation circuit 21 which demultiplexes the data supplied from the ring buffer 4 to thereby separate the same into video data and audio data, and further into timing data such as SCR (system clock reference) and DTS (decoding time stamp) inclusive of DTSV for the video data and DTSA for the audio data.” *Id.* at 1:22-27.

264. Second, Fujinami discloses that the data demultiplexer 5 has an input coupled to the ring buffer 4 and an output to provide the demultiplexed data. Fujinami explains that “[t]he data separation circuit 21 [within the data demultiplexer 5] is controlled by the control circuit 28 and separates the output data of the ring buffer 4 into video data and audio data, which are then supplied to the video code buffer 6 and the audio code buffer 8, respectively. The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.” *Id.* at 2:28-35.

265. Third, Fujinami inherently discloses that data demultiplexer 5 selects packets of data having a predefined packet identifier. Fujinami discloses that “[t]he format of the data supplied to the data demultiplexer 5 is so standardized as shown in FIG. 6 for example. This format is prescribed as a multiplex bit stream in the MPEG (ISO11172). As shown in FIG. 6, a multiplex bit stream is composed of one or more packs (PACKS), each of which is composed of one or more packets

(PACKETS). **A pack header (PACK HEADER) is disposed at the top of each pack** and has a pack start code (PACK START CODE) indicating a start point of the pack, and also SCR and MUX__RATE. This SCR indicates the time when the last byte is inputted to the data demultiplexer 5 (the time when demultiplexing is started), and the MUX__RATE signifies a transfer rate.” *Id.* at 1:28-39 (emphasis added).

266. The “multiplex bit stream in the MPEG (ISO11172)” is a reference to MPEG-1 Program Stream, which is a standard for multiplexed packetized data streams. The MPEG-1 Program Stream is referred to in the field as the ISO/IEC 11172-1 standard (*i.e.*, MPEG-1 Program Stream). As is well known to those of skill in the art, the MPEG-1 Program Stream is a multiplex of video and audio packetized elementary streams (PES) and includes presentation time stamps (PTS) and decoding time stamps (DTS). Packetized elementary streams are in turn packets containing chunks of elementary video or audio streams as well as a system clock reference (SCR). They also contain a stream identifier (SID) used to identify the stream.

267. The '945 Patent describes the multiplexing of several packetized elementary streams into a program stream: “an elementary stream (ES) is a set of data generally consisting of compressed data from a single source, such as a video or audio source, with some additional ancillary data for identification, characterization and synchronization. ES streams are first packetized into either constant length or variable length Packetized Elementary Stream packets (PES packets) consisting of header and payload. **Each PES packet header** starts with start code (0x000001) followed with

the **stream id byte identifying type of ES underneath. PES packets from various elementary streams are merged together to form a program (service)** with its own system time clock (STC). All ES component streams within one program are synchronized have periodic PTS stamps corresponding to the STC counter to indicate the proper timing for each ES.” Ex. 1001, 1:64-2:12 (emphasis added).

268. It is therefore clear to those of ordinary skill in the art that the only way to extract a packetized elementary stream corresponding to a specific elementary stream is to select a packetized elementary stream having a predefined stream identifier (SID).

269. Accordingly, Fujinami “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data,” as required by claim 21.

270. Fujinami discloses “a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets.”

271. Fujinami discloses a storage device in the form of the video code buffer 6 and audio code buffer 8. Ex. 1008, at 2:28-35; *see also id.* at FIGS. 1(A) and 1(B).

272. Fujinami further discloses that the video code buffer 6 and audio code buffer 8 are coupled to the data demultiplexer 5 to receive and store the packets selected.

Fujinami discloses that “[t]he **data separation circuit 21 [within data demultiplexer 5] is controlled by the control circuit 28 and separates the output data of the ring buffer 4 into video data and audio data, which are then**

supplied to the video code buffer 6 and the audio code buffer 8, respectively.

The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.” *Id.* at 2:28-35 (emphasis added).

273. As stated above, Fujinami further discloses that the video data and audio data is separated from a multiplexed bit stream (*i.e.*, multiplexed packetized data stream) composed of one or more packets. *See id.* at 1:28-39.

274. The coupling of the video code buffer 6 and audio code buffer 8 to the data demultiplexer 5 is also shown in FIGS. 1(A) and 1(B). In particular, the data separation circuit 21 within the data demultiplexer 5 is connected via the data ports marked by “a” and “b” to the video code buffer 6 and audio code buffer 8, respectively.

275. Accordingly, Fujinami discloses “a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets.”

276. Fujinami discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.”

277. Fujinami discloses first clock recovery module having an input coupled to the

first input node, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream. Specifically, Fujinami discloses that the data separation circuit 21 within data demultiplexer 5 receives data from the ring buffer 4 and extracts timing information (*i.e.*, SCR (system clock reference) and DTS (decoding time stamp) inclusive of DTSV for the video data and DTSA for the audio data). According to Fujinami, “[t]he data demultiplexer 5 has a data separation circuit 21 which demultiplexes the data supplied from the ring buffer 4 to thereby separate the same into video data and audio data, and further into timing data such as SCR (system clock reference) and DTS (decoding time stamp) inclusive of DTSV for the video data and DTSA for the audio data.” *Id.* at 1:22-27 (emphasis added).

278. Further, Fujinami discloses that separation circuit 21 within data demultiplexer 5 (*i.e.*, first clock recovery module) receives a multiplex bit stream (*i.e.*, multiplexed packetized data stream) as an input which is composed of packets containing timing information (*e.g.*, SCR and MUX_RATE).

279. Fujinami discloses that “[t]he format of the data supplied to the data demultiplexer 5 is so standardized as shown in FIG. 6 for example. This format is prescribed as a multiplex bit stream in the MPEG (ISO11172). As shown in FIG. 6, a multiplex bit stream is composed of one or more packs (PACKS), each of which is composed of one or more packets (PACKETS). A pack header

(PACK HEADER) is disposed at the top of each pack and has a pack start code (PACK START CODE) indicating a start point of the pack, and also SCR and MUX__RATE. This SCR indicates the time when the last byte is inputted to the data demultiplexer 5 (the time when demultiplexing is started), and the MUX__RATE signifies a transfer rate.” *Id.* at 1:28-39 (emphasis added).

280. Fujinami then discloses that the timing information extracted from packets of the multiplexed packetized data stream is used to generate a clock at the output. Initially, the extracted timing information (*i.e.*, SCR and DTS) is sent to STC register 26 and DTS registers 22 and 24 for video and audio, respectively. Fujinami discloses that “[t]he data separation circuit 21 [within data demultiplexer 5] is controlled by the control circuit 28 and separates the output data of the ring buffer 4 into video data and audio data, which are then supplied to the video code buffer 6 and the audio code buffer 8, respectively. The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.”

Id. at 2:28-35 (emphasis added).

281. Fujinami discloses that the timing information stored is then used to generate a clock. In Fujinami, “The STC register 26 having stored the timing data SCR therein counts the clock pulses outputted from the clock generator 27 and increments the storage value in response to the clock pulses. The storage value of the STC register 26 is supplied as a system time clock (STC) signal to the comparators 23 and 25.” *Id.* at

2:36-41. Fujinami further explains that “[t]he reference timing data SCR corresponds to the time when demultiplexing is started after supply of the data from the ring buffer 4 to the data demultiplexer 5. More specifically, it corresponds to a time t1 in the timing chart of FIG. 7. Therefore, the STC register 26 outputs the time data (current time) from the time t1 to one input terminal of each of the comparators 23 and 25.” *Id.* at 2:53-59. That is, the data demultiplexer 5 separates the data packets, which include timing information and the data demultiplexer 5 further includes a system time clock generation for generating a clock based on the received timing information transmitted in the packets. *See id.* at 4:56-5:16.

282. Fujinami also discloses that the stored timing information is then used in comparators 23 and 25 to generate a decoding start signal. Fujinami discloses that “[t]he video data stored in the video code buffer 6 is read out therefrom and is supplied to a video decoder 7. Then, the video data is decoded to become a video signal, which is subsequently outputted to an unshown circuit. To the video decoder 7, **there is also supplied a video decoding start signal which is outputted from the comparator 23.** Similarly, the data outputted from the audio code buffer 8 is supplied to an audio decoder 9 so as to be decoded. To the audio decoder 9, **there is also supplied the output of the comparator 25 as an audio decoding start signal.**” *Id.* at 2:6-15 (emphasis added).

283. More particularly, Fujinami explains that “[a]fter such change of the internal state, the data demultiplexer 5 resumes its operation of inputting the data, and

simultaneously therewith, the STC register 26 starts its count (increment) at the time t8. **The comparator 23 compares the output DTSV of the DTSV register 22 (t8 in this stage) with the count value STC of the STC register 26 (which increases successively from t8). When the result of such comparison signifies that the STC is equal to or greater than the DTSV, a video decoding start signal is generated and outputted** to the video decoder 7, which then starts decoding the video data. Similarly, **the comparator 25 compares the output of the DTSA register 24 with the output of the STC register 26. When the result of such comparison signifies that the STC is equal to or greater than the DTSA, an audio decoding start signal is generated and outputted** to the audio decoder 9, which then starts decoding the audio data.” *Id.* at 9:9-25 (emphasis added).

284. To the extent that one assumes that the video and audio decoding start signals disclosed by Fujinami do not constitute a clock generated at the output of the clock recovery module, it would have been obvious to a person of ordinary skill in the art to use the stored timing information (*i.e.*, STC and DTS) disclosed by Fujinami as the clock generated at the output. In this case, a person of ordinary skill in the art would have simply incorporated comparators 23 and 25 disclosed by Fujinami as part of the video and audio decoders, respectively. I note, however, that the video and audio decoding start signals are clocks generated at the output because they are signals that provide timing information used to initiate decoding by the video and audio decoders.

285. Fujinami makes clear that the generation of a clock at the output based upon

received timing information transmitted in packets of the multiplexed packetized data stream occurs **before the select packets are stored in the storage device.**

286. Fujinami explains that “[i]n the conventional apparatus, as described above, the time period from the SCR to the DTS is calculated by counting clock pulses of a fixed frequency, and the data is written in the video code buffer 6 during such time period. Consequently, the data transfer rate is determined by the clock frequency to be eventually rendered low. However, in the above embodiment of the present invention, the data can be written in the video code buffer 6 at the maximum transfer rate when the DTS of a desired picture is inputted, then the SCR of the data stored in the buffer 6 is compared with the DTS successively, and a decision is made, on the basis of the result of such comparison, as to whether a required amount of the data for decoding the relevant picture has been written or not (whether the elapse has arrived at the decoding start time or not), whereby a fast response can be achieved.” *Id.* at 9-40-55 (emphasis added).

287. Fujinami also discloses the use of the disclosed system for real-time applications because it explains that the system disclosed can handle input at a higher transfer rate, thus enhancing its response time: “As described hereinabove, according to the data demultiplexer of the present invention, timing data indicative of a decoding start time and timing data indicative of a reference time are compared with each other, and in conformity with the result of such comparison, **the video and audio data can be inputted at a higher transfer rate designated in the bit**

stream, hence enhancing the responsivity at the start of reproduction.” *Id.* at 11:37-44 (emphasis added). Because Fujinami discloses real-time applications, it inherently discloses that the generation of a clock at the output occurs before the select packets are stored in the storage device. More particularly, the only way for the system disclosed to determine whether to store packets in the storage device is to first extract the timing information from a packet and then decide whether the packet needs to be stored or sent directly to the decoder.

288. Accordingly, Fujinami discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device,” as required by claim 21.

289. Fujinami discloses “a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.”

290. Fujinami discloses video decoder 7 and audio decoder 9 coupled to video code buffer 6 and audio code buffer 8. Fujinami also discloses that the video decoder 7 and audio decoder 9 are also coupled to comparators 23 and 25, which transmit the video and audio start signals, respectively. Finally, Fujinami discloses that the video decoder 7 and audio decoder 9 produce decoded video and audio signals at the

output. According to Fujinami, “[t]he video data stored in the video code buffer 6 is read out therefrom and is supplied to a video decoder 7. Then, the video data is decoded to become a video signal, which is subsequently outputted to an unshown circuit. To the video decoder 7, there is also supplied a video decoding start signal which is outputted from the comparator 23.

291. Similarly, the data outputted from the audio code buffer 8 is supplied to an audio decoder 9 so as to be decoded. To the audio decoder 9, there is also supplied the output of the comparator 25 as an audio decoding start signal.” *Id.* at 2:11-14.

292. Fujinami also discloses that the video and audio start signals provide a clock received by video decoder 7 and audio decoder 9. Specifically, Fujinami discloses that “[t]he DTSV register 22 supplies the video timing data DTSV, which indicates the decoding start time of the video decoder 7, to the other input terminal of the comparator 23. When the current time outputted from the STC register 26 has become coincident with the decoding start time outputted from the DTSV register 22 (i.e., at a time t_2 in FIG. 7), the comparator 23 outputs a video decoding start signal to the video decoder 7. In response to the video decoding start signal thus received, the video decoder 7 reads out one frame of the video data written in the video code buffer 6 and then starts its decoding.” *Id.* at 4:28-38.

293. More particularly, Fujinami explains that “[a]fter such change of the internal state, the data demultiplexer 5 resumes its operation of inputting the data, and simultaneously therewith, the STC register 26 starts its count (increment) at the time

t8. The comparator 23 compares the output DTSV of the DTSV register 22 (t8 in this stage) with the count value STC of the STC register 26 (which increases successively from t8). When the result of such comparison signifies that the STC is equal to or greater than the DTSV, a video decoding start signal is generated and outputted to the video decoder 7, which then starts decoding the video data. Similarly, the comparator 25 compares the output of the DTSA register 24 with the output of the STC register 26. When the result of such comparison signifies that the STC is equal to or greater than the DTSA, an audio decoding start signal is generated and outputted to the audio decoder 9, which then starts decoding the audio data.” *Id.* at 9:9-25 (emphasis added).

294. To the extent that one assumes that the video and audio decoding start signals disclosed by Fujinami do not constitute a clock generated at the output of the clock recovery module, it would have been obvious to a person of ordinary skill in the art to use the stored timing information (*i.e.*, STC and DTS) disclosed by Fujinami as the clock generated at the output. In this case, a person of ordinary skill in the art would have simply incorporated comparators 23 and 25 disclosed by Fujinami as part of the video and audio decoders, respectively. I note, however, that the video and audio decoding start signals are clocks generated at the output because they are signals that provide timing information used to initiate decoding by the video and audio decoders.

295. Fujinami also discloses an output to provide decoded real-time data. As discussed above, Fujinami explains, “As described hereinabove, according to the data

demultiplexer of the present invention, timing data indicative of a decoding start time and timing data indicative of a reference time are compared with each other, and in conformity with the result of such comparison, **the video and audio data can be inputted at a higher transfer rate designated in the bit stream, hence enhancing the responsivity at the start of reproduction.**” *Id.* at 11:37-44 (emphasis added). Further, as explained above, Fujinami describes the use of the disclosed system for real-time applications. Because Fujinami discloses that the input video stream can be used for real-time applications, the system disclosed by Fujinami must necessarily receive, decode, and output the video signal in real time for display. Therefore, Fujinami inherently discloses the output of decoded real-time video data.

296. Accordingly, Fujinami discloses “a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data,” as required by claim 21.

297. Accordingly, all of the limitations of claim 21 are obvious over Fujinami.

V. SUPPLEMENTATION

298. This Declaration, along with the attached Appendices, is based on my present assessment of material and information currently available to me.

299. I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be

true. Further, these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified patent.

Dated: 12/8/2014

Respectfully submitted,

A handwritten signature in black ink that reads "Dan Schonfeld". The signature is written in a cursive style with a large, circular flourish at the end.

By: _____
Dan Schonfeld, Ph.D.

APPENDIX A

DAN SCHONFELD

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Chicago, IL 60607-7053
URL: <http://www.ece.uic.edu/~ds>

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E-mail: dans@uic.edu

A. SUMMARY OF CREDENTIALS

- **Director, University-Industry Engineering Research Center (UIERC)**
- **Full Professor, Electrical & Computer Engineering, Computer Science, Bioengineering, University of Illinois at Chicago**
- **Consulting Services, Over 60 Companies**
- **University Scholar, University of Illinois**
- **Graduate Mentoring Award, University of Illinois at Chicago**
- **Fellow, IEEE**
- **Fellow, SPIE**
- **Editor-in-Chief, IEEE Transactions on Circuits and Systems for Video Technology**
- **Deputy Editor-in-Chief, IEEE Transactions on Circuits and Systems for Video Technology**
- **Area Editor, Special Issues, IEEE Signal Processing Magazine**
- **Guest Editor, 7 Special Issues (5 IEEE Transactions)**
- **Associate Editor, 4 IEEE Transactions**
- **Editorial Board, 6 Journals (1 IEEE Magazine)**
- **Member, 4 IEEE Technical Committees**
- **Member, ANSI/UL Standards Technical Panel**
- **Chair, 4 International Conferences (3 IEEE Conferences)**
- **Organizing Committee, 8 Conferences (6 IEEE Conferences)**
- **Presenter, 5 Keynote and Plenary Talks at International Conferences**
- **Author, Over 200 Technical Papers**
- **Co-Author and Advisor, 4 Best Paper Awards**
- **Advisor, 16 Doctoral and 9 Masters Thesis Students Graduated**
- **Inventor, 4 Patents (2 Issued)**
- **Funding, Over \$4 Million in Research Grants**
- **Instructor, Over 20 Different Undergraduate and Graduate Courses**

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C. PROFESSIONAL BIOGRAPHY

Dr. Schonfeld received the B.S. degree in Electrical Engineering and Computer Science from the University of California, Berkeley, California, and the M.S. and Ph.D. degrees in Electrical and Computer Engineering from The Johns Hopkins University, Baltimore, Maryland, in 1986, 1988, and 1990, respectively.

In August 1990, he joined the Department of Electrical Engineering and Computer Science at the University of Illinois, Chicago, Illinois, where he is currently a Professor in the Departments of Electrical and Computer Engineering, Computer Science, and Bioengineering. He has also served as Director of the University-Industry Engineering Research Center (UIERC), formerly the Manufacturing Research Center (MRC). He is also Co-Director of the Multimedia Communications Laboratory (MCL) and member of the Signal and Image Research Laboratory (SIRL).

Dr. Schonfeld has been elevated to the rank of Fellow of the IEEE “for contributions to image and video analysis.” He was also elevated to the rank of Fellow of the SPIE “for specific achievements in morphological image processing and video analysis.” Dr. Schonfeld has been elected University Scholar of the University of Illinois.

Dr. Schonfeld has authored over 200 technical papers in various journals and conferences. He was co-author (with Carlo Giuliatti and Rashid Ansari) of a paper that won the Best Paper Award at the ACM Multimedia Workshop on Advanced Video Streaming Techniques for Peer-to-Peer Networks and Social Networking 2010. He was also co-author (with Junlan Yang) of a paper that won the Best Student Paper Award in the IEEE International Conference on Image Processing 2007. He was also co-author (with Wei Qu) of a paper that won the Best Student Paper Award in the IEEE International Conference on Image Processing 2006. He was also co-author (with Nidhal Bouaynaya) of a paper that won the Best Student Paper Award in Visual Communication and Image Processing 2006.

Dr. Schonfeld is currently serving as Editor-in-Chief of the IEEE Transactions on Circuits and Systems for Video Technology. He has also served as Deputy Editor-in-Chief of the IEEE Transactions on Circuits and Systems for Video Technology and Area Editor for Special Issues of the IEEE Signal Processing Magazine. He has also served as Associate Editor of the IEEE Transactions on Image Processing (on image and video storage, retrieval and analysis), Associate Editor of the IEEE Transactions on Circuits and Systems for Video Technology (on video analysis), Associate Editor of the IEEE Transactions on Signal Processing (on multidimensional signal processing and multimedia signal processing), and Associate Editor of the IEEE Transactions on Image Processing (on nonlinear filtering). He has also served on the editorial board of various journal publications. He has also served as guest editor for numerous special issues in various journal publications.

Dr. Schonfeld is currently serving as Technical Program Chair of the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 2018. He has served as General Co-Chair of the IEEE International Conference on Multimedia and Expo (ICME) 2012. He has also served as Technical Chair of the IEEE Workshop on Genomic Signal Processing and Statistics (GENSIPS) 2009. He has also served as Chair of the Workshop on Video Mining 2008. He has also served as Chair of the SPIE Conference on Visual Communication and Image Processing (VCIP) 2007. He was a member of the organizing committees of the IEEE International Conference on Image Processing (ICIP) 1998, 2012, and 2018, IEEE/SPIE International Conference on Visual Communications and Image Processing (VCIP) 2010, and IEEE Workshop on Nonlinear Signal and Image Processing (NSIP) 1997. He was also organizer of the Thematic Symposium on Multimedia Search and Retrieval at the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 2009.

Dr. Schonfeld was keynote speaker at the International Conference on Intelligent Control and Information Processing (ICICIP) 2013 and International Conference on Brain Inspired Cognitive Systems (BICS) 2013. He was also plenary speaker at the IEEE/IET International Conference on Audio, Language and Image Processing (ICALIP), Shanghai, China, in 2010. He was also plenary speaker at the IEEE International Conference on Advanced Video and Signal Based Surveillance (AVSS), Genoa, Italy, in 2009. He was also plenary speaker at the INPT/ASME International Conference on Communications, Signals, and Systems (ICCS), Rabat Morocco, in 1995 and 2001.

Dr. Schonfeld has served as Representative of Regions 1-6 in the Chapters Committee of the IEEE Signal Processing Society. He has also served as Chairman of the Chicago Chapter of the IEEE Signal Processing Society. He has also served on the IEEE Image, Video, and Multidimensional Signal Processing (IVMSP) Technical Committee, formerly the IEEE Image and Multidimensional Signal Processing (IMDSP) Technical Committee, as well as the IEEE Multimedia Communications Technical Committee. He also served on the American National Standards Institute (ANSI)/Underwriters Laboratory (UL) Standards Technical Panel (“STP”) on Multimedia Systems.

Dr. Schonfeld has served as President of Multimedia Systems Corporation (MSC) and provided services as a consultant and expert witness for over 60 companies.

D. RESEARCH INTERESTS

Signal Processing, Image and Video Analysis, Video Retrieval and Communications, Multimedia Systems, Computer Vision, Medical Imaging, and Genomic Signal Processing.

E. SIGNIFICANT RESEARCH ACCOMPLISHMENTS

E.1. Morphological Image Analysis

We have been working in the area of mathematical morphology since the mid-1980s. In the course of our work, we have solved several fundamental problems in morphological image analysis. Our initial work was devoted to image restoration using morphological filters. We proved that the alternating sequential filter is the optimal morphological filter for image restoration. The proof introduced a new approach to optimization of nonlinear filters and solved a fundamental problem which had been posed several decades earlier. We later provided an analytical solution to the fundamental open problem of characterization of the optimal structuring element (window) in morphological image analysis.

We have also addressed the problem of morphological representation and skeletonization. We presented a unified approach to image representation and demonstrated its relation to the medial axis transform which is used for pattern recognition and image coding. We also established necessary and sufficient conditions for the invertibility of image representations and determined the optimal skeleton for image coding. We finally investigated the robustness of the skeleton to noise degradation and used random set theory and stochastic geometry to prove that redundancy in skeleton representations is beneficial in low-noise environments, whereas sparsity provides superior performance in high-noise systems.

More recently, we have focused on the topic of spatially-variant and adaptive morphological image analysis. We demonstrated a dramatic improvement in the performance of skeletons for pattern recognition and image coding as well as image restoration by using an adaptive structuring element (window). We later introduced a theoretical foundation for a new approach to morphological image

analysis based on spatially-varying structuring elements (windows) and illustrated the enormous improvement of this theory over classical methods in image analysis.

We have also presented several important practical solutions to various image processing applications. For instance, we have developed an algorithm for the implementation of morphological operations represented as thresholded linear convolution based on FFTs.

E.2. Video Tracking

In the late-1990s, we started to work in the area of video tracking. Our initial focus was on tracking in the compressed domain. We showed that we can exploit the structure of coded video sequences – motion vectors in MPEG-2 (HDTV) – to provide efficient target tracking in the compressed domain and thus improve the computational speed more than 4,000 times. We later extended the approach to an adaptive block matching algorithm for real-time video tracking. The proposed approach to video tracking on raw image sequences provides speed that is more than 10 times faster than previous methods for video tracking. The algorithm has been presented in consumer shows and incorporated into the software suite of the MiMagic Associate Processor Array (APA) by NeoMagic Corporation (two patents have been filed and issued on the adaptive block matching algorithm).

In the past few years, we have concentrated on the use of particle filtering for video tracking. We showed both theoretically and experimentally that we can achieve a dramatic improvement in the computational speed by using motion-based particle filters to reduce the number of particles required for efficient tracking from 1,000-4,000 down to 30-50 particles. We proposed techniques to improve the efficiency and accuracy of particle filters by adaptively determining the mean and covariance of the proposal (importance) density function. We finally derived a closed-form solution based on rate-distortion theory for particle allocation among multiple frames and objects for video tracking.

Our main focus on video tracking has been devoted to distributed tracking. We proposed a method for decomposition of graphical models used for the representation of the interaction among multiple objects and cameras in image sequences. We then derived a distributed particle filter for multiple object tracking based on statistical collaboration among interactive particle filters. The proposed approach can be used track occluded objects while its complexity grows linearly with the number of targets (compared to the exponential growth in computational complexity of methods that rely on joint representations). We have extended the approach to distributed particle filtering to tracking using multiple networked cameras as well as articulated object tracking by collaboration within units (e.g. hand and forearm) and among units (e.g. arm and leg) (two patents have been filed on the distributed particle filter algorithm).

E.3. Video Search and Retrieval

In the early 2000s, we began to work on retrieval and recognition in video databases. One of the key problems in video analysis is segmentation of image sequences into coherent visual scenes. We introduced statistical change detection theory to solve the classical problem of scene change detection in video sequences. This approach has been shown to yield far superior results for this fundamental problem for videos with both special effects and abrupt changes alike. It provides a single algorithm for scene change detection and avoids the need to use different methods for distinct special effects.

Since 2003, we focused on retrieval and recognition based on motion trajectories in video and sensor databases. We first proposed a framework based on principal component analysis for indexing and retrieval of segmented motion trajectories in video databases. We then extended the use of hidden

Markov models from speech recognition to address the problem of motion trajectory classification in video sequences. We later adapted tools from shape analysis to address the problem of view-invariance of motion trajectories for unknown and moving cameras. We finally proposed a new approach to view-invariance based on a null-space representation of motion trajectory information.

In the past few years, we have focused primarily on retrieval and recognition of motion events in video and sensor databases characterized by multiple interactive motion trajectories. We first presented an approach to multiple motion trajectory indexing and retrieval based on tensor decomposition. We later provided an efficient method for extraction and insertion of partial information in video database used for multiple motion trajectory representation based on high-order singular value decomposition of tensors. We also extended the null-space representation to tensors for view-invariant indexing and retrieval of multiple motion trajectories from unknown and moving cameras.

We finally provided a solution to classification and recognition of multiple interactive motion trajectories by deriving an extension of hidden Markov models to multiple dimensions. We provided a closed-form solution for the training and classification – general forward-backward, expectation-maximization, and Viterbi algorithms – for multiple dimensions in a causal system. We then presented an approach to multiple motion trajectory classification based on distributed multi-dimensional hidden Markov models for non-causal systems.

E.4. Genomic Signal Processing

Over the past few years, we have begun to work in the area of genomic and proteomic signal processing. Our aim thus far has been to address fundamental problems in system biology by using tools from signal processing and communications. We proposed a model of protein evolution as a communication system represented by a Markov chain and proved that it will converge to a probability distribution of amino acids that matches nearly perfectly the natural abundance of amino acids in nature. We further investigated the capacity and rate-distortion bounds of the protein communication model and showed it is consistent with an evolutionary pattern whereby the size of introns increases through time.

We also addressed the rationale for the presence of introns (junk DNA) in the genomic sequence by hypothesizing that introns serve as decoys that reduce the effect of mutations in gene expression. We showed that the exon length distribution that minimizes the probability of error due to mutations yields a long-tail density that is nearly identical to the histogram of exon lengths among eukaryotes. We finally investigated the statistical structure of genomic sequences and showed that coding and non-coding segments of the DNA can be distinguished by a measure of randomness defined based on tools from non-stationary analysis.

F. HONORS AND AWARDS

Graduate Mentoring Award

University of Illinois at Chicago
2014

University Scholar

University of Illinois
2010

Fellow

International Society for Optics and Photonics (SPIE)
“For Specific Achievements in Morphological Image Processing and Video Analysis”
2011

Fellow

Institute of Electrical and Electronics Engineers (IEEE)
“For Contributions to Image and Video Analysis”
2010

Senior Member

Institute of Electrical and Electronics Engineers (IEEE)
2005

Best Paper Award

C. Giulietti, D. Schonfeld, and R. Ansari
“A Novel Cache Optimization Algorithm and Protocol
for Video Streaming in Pure Peer-to-Peer Networks”
ACM Multimedia Workshop on Advanced Video Streaming Techniques
for Peer-to-Peer Networks and Social Networking
2010

Best Student Paper Award

J. Yang, D. Schonfeld and M. Mohamed
“Robust Focused Image Estimation from Multiple Images in Video Sequences”
IEEE International Conference on Image Processing
2007

Best Student Paper Award

W. Qu and D. Schonfeld
“Robust Kernel-Based Tracking Using Optimal Control”
IEEE International Conference on Image Processing
2006

Best Student Paper Award

N. Bouaynaya and D. Schonfeld
“Spatially-variant morphological image processing: Theory and applications”
SPIE Conference on Visual Communications and Image Processing
2006

Advising Award

College of Engineering
University of Illinois at Chicago
2013

Outstanding Associate Editor Award – IEEE Circuits and Systems Society

IEEE Circuits and Systems Society
IEEE Transactions on Circuits and Systems for Video Technology
2009

Most Active Chapter Award – IEEE Signal Processing Chicago Chapter Chair

IEEE – Region 4
2008

Service Award – IEEE Signal Processing Chicago Chapter Chair
IEEE – Chicago Section
2007

Certificate of Appreciation – IEEE Signal Processing Society
Chair, IEEE Signal Processing Chapter
Chicago Section
2006-2012

Certificate of Appreciation – IEEE Circuits and Systems Society
IEEE Circuits and Systems Society
Prize Paper Award Subcommittee
2010

Certificate of Appreciation – IEEE Circuits and Systems Society
IEEE Circuits and Systems Society
Deputy Editor-in-Chief of the IEEE Transactions on Circuits and Systems for Video Technology
2008 – 2010

Certificate of Appreciation – IEEE Circuits and Systems Society
IEEE Circuits and Systems Society
Associate Editor of the IEEE Transactions on Circuits and Systems for Video Technology
2008 – 2010

Certificate of Appreciation – IEEE Signal Processing Chicago Chapter Chair
IEEE – Chicago Section
2006

Worldwide Who's Who
2014 Edition

Who's Who in America (WWA)
2012 Edition

Who's Who in America (WWA)
2011 Edition

Who's Who in America (WWA)
2010 Edition

Who's Who in Engineering Education (WWE)
2002 Edition

University Fellowship
The Johns Hopkins University
1986—1990

G. IN THE NEWS

IEEE Fellow Dan Schonfeld: Helping Catch Thieves & Read Fuzzy Faxes

e-Scanfax: IEEE Chicago Section Newsletter

January 2010

<http://www.ieeechicago.org/LinkClick.aspx?fileticket=Py81tdr4GTM%3D&tabid=390&mid=884>

IEEE-Chicago Fellows Provide Words of Wisdom to New IEEE Members

e-Scanfax: IEEE Chicago Section Newsletter

May 2010

http://www.ieeechicago.org/LinkClick.aspx?fileticket=2GIDPZnZQ_M%3D&tabid=390&mid=884

What You See, What You Get

University Scholar Dan Schonfeld

Paul Francuch

UIC News

November 10, 2010

<http://www.uic.edu/htbin/cgiwrap/bin/uicnews/articledetail.cgi?id=14769>

Genomic Signal Processing May Yield Clues to Cancer Treatment

Paul Francuch

UIC News Release

November 17, 2010

[http://tiger.uic.edu/htbin/cgiwrap/bin/newsbureau/cgi-bin/index.cgi?](http://tiger.uic.edu/htbin/cgiwrap/bin/newsbureau/cgi-bin/index.cgi?from=Releases&to=Release&id=3073&start=1232172000&end=1329285600&topic=2&dept=64)

[from=Releases&to=Release&id=3073&start=1232172000&end=1329285600&topic=2&dept=64](http://tiger.uic.edu/htbin/cgiwrap/bin/newsbureau/cgi-bin/index.cgi?from=Releases&to=Release&id=3073&start=1232172000&end=1329285600&topic=2&dept=64)

New Camera Focuses Photos After They Are Taken

Morgen Peck

InnovationNewsDaily Contributor

November 4, 2011

<http://www.innovationnewsdaily.com/camera-focuses-photos-after-2358/>

H. EDUCATION

Ph.D. July 1990

The Johns Hopkins University

Department of Electrical & Computer Engineering

Concentration: Nonlinear Signal Processing / Image Analysis

Thesis Title: "Optimal Morphological Representation and Restoration of Binary Images: Theory and Applications"

First Reader: Prof. John Goutsias; Second Reader: Prof. Victor Solo

M.S. May 1988

The Johns Hopkins University

Department of Electrical & Computer Engineering

Concentration: Speech Processing / Biomedical Signal Processing

Advisor: Prof. Moise H. Goldstein

B.S. May 1986

University of California at Berkeley
Department of Electrical Engineering & Computer Science
Concentration: Computer Engineering / Systems Engineering
Advisor: Prof. Michael J. Sabin

I. WORK EXPERIENCE

Director

University-Industry Engineering Research Center (UIERC)
College of Engineering
University of Illinois at Chicago
Chicago, Illinois
2008—2011

Professor with Tenure

Department of Electrical & Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2007—Present

Professor (Courtesy Appointment)

Department of Computer Science
University of Illinois at Chicago
Chicago, Illinois
2007— Present

Professor

Department of Bioengineering
University of Illinois at Chicago
Chicago, Illinois
2007— Present

Associate Professor with Tenure

Department of Electrical & Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2001—2007

Associate Professor (Courtesy Appointment)

Department of Computer Science
University of Illinois at Chicago
Chicago, Illinois
2001—2007

Associate Professor

Department of Bioengineering
University of Illinois at Chicago
Chicago, Illinois
1998—2007

Associate Professor with Tenure

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
Chicago, Illinois
1996—2001

Co-Director

Multimedia Communications Laboratory (MCL)
Department of Electrical & Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
1997—Present

Assistant Professor

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
Chicago, Illinois
1990—1996

Member

Signal and Image Research Laboratory (SIRL)
Department of Electrical & Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
1990—2002

Instructor

Department of Electrical and Computer Engineering
The Johns Hopkins University
Baltimore, Maryland
1987—1990

Teaching Assistant

Department of Electrical and Computer Engineering
The Johns Hopkins University
Baltimore, Maryland
1986—1990

Software Engineer

Computer Aided Design
Teledyne Systems
Northridge, California
Summer 1984—85—86

J. VISITING POSITIONS

Distinguished Visiting Scholar

Advanced Analytics Institute (AAI)

University of Technology
Sydney, Australia
2012

Visiting Professor

Department of Information Engineering and Computer Science - DISI
University of Trento
Trento, Italy
May 2010

Visiting Professor

School of Computer Engineering
Nanyang Technological University
Singapore
July 2009

Visiting Associate Professor

Department of Electrical Engineering—Systems
Tel-Aviv University
Tel-Aviv, Israel
December 1996—January 1997

K. INTERDISCIPLINARY PROGRAMS

Collaborative Neuroimaging Environment for Connectomics (CoNECT)

University of Illinois at Chicago
2013—Present

Clinical and Translational Science (CCTS)

Biomedical Informatics Core Consult Group
University of Illinois at Chicago
2009—Present

Graduate Program in Neuroscience

University of Illinois at Chicago
2001—Present

Bioinformatics Program

Department of Bioengineering
University of Illinois at Chicago
2000—Present

L. PROFESSIONAL ACTIVITIES

L.1. Editorships

Editor-in-Chief (EIC)

IEEE Transactions on Circuits and Systems for Video Technology
2014—Present

Deputy Editor-in-Chief (DEIC)

IEEE Transactions on Circuits and Systems for Video Technology
2010—2013

Area Editor, Special Sections

Special Issues
IEEE Signal Processing Magazine
2009—2011

Editor

Video Search and Mining
Studies in Computational Intelligence Series
Springer-Verlag
2009

Associate Editor

IEEE Transactions on Image Processing
Image and Video Storage, Retrieval and Analysis
2007—2009

Associate Editor

IEEE Transactions on Circuits and Systems for Video Technology
Video Analysis
2006—2009

Associate Editor

IEEE Transactions on Signal Processing
Multidimensional Signal Processing &
Multimedia Signal Processing
1999—2000

Associate Editor

IEEE Transactions on Image Processing
Filtering and Enhancement
1994—1996

Guest Editor

IEEE Journal of Special Topics in Signal Processing
Special Issue on Mathematical Morphology
and Its Applications to Image and Signal Processing
2011—2012

Guest Editor

IEEE Transactions on Image Processing
Special Issue on Distributed Camera Networks:
Sensing, Processing, Communication and Computing
2010—2011

Guest Editor

EURASIP Journal on Image and Video Processing
Special Issue on Advanced Video-Based Surveillance
2010—2011

Lead Guest Editor

IEEE Journal of Special Topics in Signal Processing
Special Issue on Recent Advances in Video Processing for Consumer Displays
2009—2011

Guest Editor

IEEE Transactions on Circuits and Systems for Video Technology
Special Issue on Event Analysis in Videos
2008

Lead Guest Editor

IEEE Journal of Special Topics in Signal Processing
Special Issue on Genomic and Proteomic Signal Processing
2007—2008

Guest Editor

Journal of Advances in Multimedia
Special Issue on Plenoptic Signal and Image Processing
2007—2008

Editorial Board

Journal of Electrical and Computer Engineering
Hindawi Publishing Corporation
2009— Present

Editorial Board

EURASIP Journal of Image and Video Processing
2009—2013

Editorial Board

IEEE Signal Processing Magazine
2008—2011

Editorial Board

Research Letters in Signal Processing
Hindawi Publishing Corporation
2007—2009

Editorial Board

Recent Patents on Computer Science
Bentham Science Publishers, Ltd.
2007—Present

Editorial Board

Recent Patents on Electrical Engineering
Bentham Science Publishers, Ltd.

2007—2012

Contributor

Science and Technology: SPIE Newsroom
Electronic Imaging and Signal Processing
2005—2008

L.2. Committees

Best Paper Award Selection Committee

CSVT Best Paper Award
IEEE Circuits and Systems Society
2013

Travel Grant Selection Committee

IEEE Signal Processing Society
IEEE International Conference on Image Processing
2011

Steering Committee

International Society of Mathematical Morphology (ISMM)
International Symposium on Mathematical Morphology (ISMM)
2011—Present

Advisory Committee

IEEE Circuits and Systems Society
Visual Signal Processing and Communication (VSPC) Technical Committee
IEEE Conference on Visual Communications and Image Processing (VCIP)
2010—Present

Steering Committee

SPIE and IEEE Circuits and Systems Society
Conference on Visual Communications and Image Processing
2008—2010

Scientific Advisory Board

World Congress of NeuroTalk
From Nervous Functions to Treatment
Singapore Expo, Singapore
2010

Chair

Nominations and Elections Subcommittee
Image, Video, and Multidimensional Signal Processing (IVMSP) Technical Committee
IEEE Signal Processing Society
2010—2011

Associate Member

Image, Video, and Multidimensional Signal Processing (IVMSP) Technical Committee
IEEE Signal Processing Society

2014— 2015

Member

IEEE Multimedia Communications Technical Committee (MMTC) Technical Committee
IEEE Communications Society
2009— Present

Member

Image, Video, and Multidimensional Signal Processing (IVMSP) Technical Committee
IEEE Signal Processing Society
2009— 2012

Member

Image and Multidimensional Signal Processing (IMDSP) Technical Committee
IEEE Signal Processing Society
2007—2008

Member

Signal and Image Processing in Medicine Technical Committee
IEEE Circuits and Systems Society
1990—1996

Member

P2P Communication and Networking Technical Subcommittee
Multimedia Communications Technical Committee
IEEE Communications Society
2006—Present

Representative

Regions 1-6
Chapters Committee
IEEE Signal Processing Society
2006—2012

Chairman

Chicago IEEE Signal Processing Chapter
2006—2012

Member

American National Standards Institute/Underwriters Laboratory (ANSI/UL)
Standards Technical Panel (STP)
STP 0469: Musical Instruments and Accessories
STP 0813: Commercial Audio Equipment
STP 1492: Audio/Video Products and Accessories
STP 6500: Audio/Video and Musical Instrument Apparatus for Household, Commercial, and Similar General Use
STP 60065: Audio, Video and Similar Electronic Apparatus – Safety Requirements
STP 62368: Audio/Video, Information Technology, and Communication Technology Equipment
STP 62368-1: Audio/video, information and communication technology equipment – Part 1: Safety requirements

2002—Present

L.3. Review Panels

Member

Expert Panel
Faculty of Computing and Electrical Engineering
Tampere University of Technology (TUT)
Tampere, Finland
2011

Member

Paper Award Committee
IEEE International Conference on Advanced Video and Signal-Based Surveillance (AVSS)
Genoa, Italy
2009

Member

Technical Jury
NTT DoCoMo USA Labs Most Innovative Paper Awards
IEEE International Conference on Image Processing
San Diego, California
2008

Member

Technical Jury
NTT DoCoMo USA Labs Most Innovative Paper Awards
IEEE International Conference on Image Processing
San Antonio, Texas
2007

Member

Technical Jury
NTT DoCoMo USA Labs Most Innovative Paper Awards
IEEE International Conference on Image Processing
Atlanta, Georgia
2006

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Computing and Communication Foundations (CCF)
Communications and Information Foundations (CIF)
2012

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Computing and Communication Foundations (CCF)
Communications and Information Foundations (CIF)

2011

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Information & Intelligent Systems (IIS)
Databases and Data Mining (DB/DM)
2007

Member

NSF Review Panel
Small Business Innovation Research (SBIR) Program
Robotics II
Phase II
2007

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Information & Intelligent Systems (IIS)
Information Management (IM)
2006

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Information & Intelligent Systems (IIS)
Information & Knowledge Management (IKM)
2005

Member

NSF Review Panel
Small Business Innovation Research (SBIR) Program
Robotics II
Phase I
2005

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Advanced Networking Infrastructure and Research (ANIR)
Information Technology Research (ITR)
Networking Research
Small Grants
2002

Member

NSF Review Panel
Small Business Innovation Research (SBIR) Program
Diagnostic Systems and Signal Processing
Phase I

2002

Member

NSF Review Panel
Computer & Information Science & Engineering (CISE)
Information Technology Research (ITR)
Biology & Information Technology
Computational Biology / Biocomputation
Medium Grants
2003

L.4. Program Chair

Technical Program Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Seoul, Korea
2018

General Co-Chair

Workshop on Big Data in 3D Computer Vision
Held in conjunction with the IEEE International Conference on Computer Vision (ICCV)
Melbourne, Australia
2013

General Co-Chair

IEEE International Conference on Multimedia and Expo
Melbourne, Australia
2012

Technical Program Chair

IEEE International Workshop on Genomic Signal Processing and Statistics
Minneapolis, Minnesota
2009

Chair

Workshop on Video Mining
IEEE International Conference on Data Mining
Held in conjunction with the IEEE International Conference on Data Mining (ICDM)
Pisa, Italy
2008

Chair

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
2007

Multimedia Content Analysis Track Chair

IEEE International Conference on Multimedia and Expo
New York, New York
2009

Technical Program Committee / Area Chair

IEEE International Conference on Image Processing
San Diego, California
2008

Technical Program Committee / Area Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Las Vegas, Nevada
2008

Technical Program Committee / Area Chair

IEEE International Conference on Image Processing
San Antonio, Texas
2007

Associate Program Chair

ACM Multimedia
Juan Les Pins, France
2002

L.5. Organizing Committees

Technical Program Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Seoul, Korea
2018

General Co-Chair

Workshop on Big Data in 3D Computer Vision
Held in conjunction with the IEEE International Conference on Computer Vision (ICCV)
Melbourne, Australia
2013

General Co-Chair

IEEE International Conference on Multimedia and Expo
Melbourne, Australia
2012

Plenary Chair

IEEE International Conference on Image Processing
Plenary Chair
Orlando, Florida
2012

Publications Chair

IEEE Conference on Advanced Video and Signal-based Surveillance (AVSS)
Beijing, China
2012

USA Liaison Chair

IEEE Conference on Advanced Video and Signal-based Surveillance (AVSS)
Klagenfurt, Austria
2011

Publicity Co-Chair

IEEE/SPIE International Conference on Visual Communications and Image Processing
Huang Shan, An Hui, China
2010

Technical Program Chair

IEEE International Workshop on Genomic Signal Processing and Statistics
Minneapolis, Minnesota
2009

Organizer

IEEE International Conference on Acoustics, Speech, and Signal Processing
Thematic Symposium on Multimedia Search and Retrieval
Taipei, Taiwan
2009

Chair

Workshop on Video Mining
Held in conjunction with the IEEE International Conference on Data Mining (ICDM)
Pisa, Italy
2008

Chair

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
2007

Technical Organizing Committee

IS&T/SPIE Annual Symposium on Electronic Imaging: Science and Technology
San Jose, California
2007

Publications Chair

IEEE International Conference on Image Processing
Chicago, Illinois
1998

Plenary Talks and Special Session Chair

IEEE/EURASIP Workshop on Nonlinear Signal and Image Processing
Mackinac Island, Michigan
1997

L.6. Technical Program Committees

Program Committee

IEEE International Conference on Automatic Face and Gesture Recognition (FG 2013)
Shanghai, China
2013

Technical Program Committee

SPIE Conference on Video Surveillance and Transportation Imaging
San Francisco, California
2013

Technical Program Committee

SPIE Conference on Visual Information Processing and Communication
San Francisco, California
2013

Technical Program Committee

ICST International Conference on
Wireless Mobile Communication and Healthcare (MobiHealth)
Paris, France
2012

Technical Program Committee

SPIE Conference on Visual Information Processing and Communication
San Francisco, California
2012

Program Committee

International Workshop on Video Event Categorization, Tagging and Retrieval (VECTaR)
Held in conjunction with the International Conference on Computer Vision
Barcelona, Spain
2011

Technical Program Committee

ICST International Conference on
Wireless Mobile Communication and Healthcare (MobiHealth)
Kos Island, Greece
2011

Technical Program Committee

SPIE Conference on Visual Information Processing and Communication
San Francisco, California
2011

Technical Program Committee

IEEE International Workshop on Genomic Signal Processing and Statistics
Cold Spring Harbor Laboratory, New York
2010

Technical Program Committee

IEEE International Conference on Multimedia and Expo (ICME)
Singapore
2010

Technical Program Committee

International Conference on Pattern Recognition (ICPR)

Track I: Computer Vision

Istanbul, Turkey

2010

Technical Program Committee

ACM/IEEE International Conference on Distributed Smart Cameras (ICDSC)

Atlanta, Georgia

2010

Technical Program Committee

IEEE Workshop on Multimedia Computing and Communications (MCC)

Held in conjunction with the International Conference on Computer Communications and Networks (ICCCN)

Zurich, Switzerland

2010

Program Committee

ACM International Conference on Bioinformatics and Computational Biology (ACM-BCB)

Niagara Falls, New York

2010

Technical Program Committee

IEEE/SPIE International Conference on Visual Communications and Image Processing

Huang Shan, An Hui, China

2010

Technical Program Committee

ICST International Conference on

Wireless Mobile Communication and Healthcare (MobiHealth)

Ayia Napa, Cyprus

2010

Technical Program Committee

SPIE International Conference on Visual Information Processing and Communications

San Jose, California

2010

Program Committee

International Workshop on Video Event Categorization, Tagging and Retrieval (VECTaR)

Held in conjunction with the Asian Conference on Computer Vision

Xi'an, China

2009

Program Committee

IEEE International Workshop on Video-Oriented Object and Event Classification (VOEC)

Held in conjunction with the International Conference on Computer Vision (ICCV)

Kyoto, Japan

2009

Program Committee / Reviewer

IEEE International Conference on Computer Vision
Kyoto, Japan
2009

Technical Program Committee

IEEE International Conference on Advanced Video and Signal-Based Surveillance (AVSS)
Genoa, Italy
2009

Technical Program Committee

IEEE Workshop on Multimedia Computing and Communications (MCC)
Held in conjunction with the International Conference on Computer Communications and Networks (ICCCN)
San Francisco, California
2009

Technical Program Committee

International Conference on Image and Graphics
Xi'an, China
2009

Program Committee

International Conference on Advances in Multimedia (MMEDIA)
Colmar, France
2009

Technical Program Committee

IEEE International Workshop on Computational Advances
in Multi-Sensor Adaptive Processing (CAMSAP)
Dominican Republic
2009

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
2009

Technical Program Committee / Reviewer

IEEE International Conference on Image Processing
San Diego, California
2008

Program Committee

IEEE Conference on Computer Vision and Pattern Recognition
Anchorage, Alaska
2008

Technical Program Committee / Reviewer

IEEE International Conference on Acoustics, Speech, and Signal Processing

Las Vegas, Nevada
2008

Technical Program Committee

IEEE International Workshop on Genomic Signal Processing and Statistics
Phoenix, Arizona
2008

Technical Program Committee

International Workshop on Multimedia Analysis & Processing (IMAP)
U.S. Virgin Islands
2008

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
2008

Program Committee

IEEE International Conference on Computer Vision
Rio de Janeiro, Brazil
2007

Technical Program Committee / Reviewer

IEEE International Conference on Image Processing
San Antonio, Texas
2007

Technical Program Committee

IEEE International Workshop on Genomic Signal Processing and Statistics
Tuusula, Finland
2007

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
2007

Technical Program Committee

IEEE International Conference on Image Processing
Atlanta, Georgia
2006

Technical Program Committee

IEEE International Workshop on Genomic Signal Processing and Statistics
College Station, Texas
2006

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California

2006

Technical Program Committee / Reviewer

IEEE International Conference on Acoustics, Speech, and Signal Processing
Toulouse, France
2006

Technical Program Committee

IEEE International Conference on Image Processing
Genova, Italy
2005

Technical Program Committee / Reviewer

IEEE International Conference on Acoustics, Speech, and Signal Processing
Philadelphia, Pennsylvania
2005

Technical Program Committee

IEEE International Conference on Image Processing
Singapore
2004

Technical Program Committee

IEEE International Conference on Image Processing
Barcelona, Spain
2003

Technical Program Committee

IEEE International Conference on Image Processing
Rochester, New York
2002

Technical Program Committee

IEEE International Conference on Image Processing
Thessaloniki, Greece
2001

Technical Program Committee

IEEE International Conference on Image Processing
Vancouver, Canada
2000

Technical Program Committee

IEEE International Conference on Image Processing
Kobe, Japan
1999

Technical Program Committee

IEEE International Conference on Image Processing
Chicago, Illinois
1998

Technical Program Committee

International Symposium on Mathematical Morphology
Amsterdam, The Netherlands
1998

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
1998

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
San Jose, California
1997

Technical Program Committee

SPIE International Conference on Visual Communications and Image Processing
Orlando, Florida
1996

Technical Program Committee

IEEE International Conference on Image Processing
Austin, Texas
1994

Technical Program Committee

IEEE International Symposium on Circuits and Systems
Chicago, Illinois
1993

L.7. Session Organizer**Chair**

IEEE International Conference on Image Processing
Special Session on Face Recognition II
Orlando, Florida
2012

Organizer and Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Special Session on Video Search and Event Analysis
Taipei, Taiwan
2009

Organizer

Workshop on Global Multimedia Mobile Communications
University of Illinois at Chicago
Chicago, Illinois
2005

Organizer and Chair

IEEE International Conference on Image Processing
Special Session on Nonlinear Filtering
Austin, Texas
1994

Organizer and Chair

IEEE International Symposium on Circuits and Systems
Special Session on Medical Image and Signal Processing
Singapore
1991

Organizer and Chair

Conference on Information Sciences and Systems
Session on Nonlinear Image and Signal Processing I
Baltimore, Maryland
1991

L.8. Session Chair

Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Session on Image and Video Indexing and Retrieval
Prague, Czech Republic
2011

Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Session on Image/Video Semantic Understanding
Dallas, Texas
2010

Chair

IEEE International Conference on Advanced Video and Signal-Based Surveillance (AVSS)
Session on Trajectory Analysis and Learning
Genoa, Italy
2009

Chair

IEEE International Conference on Multimedia and Expo
Session on Multimedia Content Analysis and Synthesis IV
New York, New York
2009

Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Session on Stereoscopic and 3-D Processing
Taipei, Taiwan
2009

Chair

IEEE International Conference on Image Processing
Session on Enhancement and Denoising II
San Diego, California
2008

Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Session on Restoration and Enhancement
Las Vegas, Nevada
2008

Chair

SPIE Electronic Imaging Conference on Visual Communications and Image Processing
Session on Image Processing
San Jose, California
2008

Chair

IEEE International Conference on Image Processing
Session on Image and Video Restoration and Enhancement I
San Antonio, Texas
2007

Chair

IEEE International Conference on Image Processing
Session on Image and Video Filtering
Atlanta, Georgia
2006

Chair

IEEE International Conference on Multimedia and Expo
Session on Media Signal Processing
Toronto, Canada
2006

Chair

IEEE International Conference on Multimedia and Expo
Session on Multimedia Database Applications
Toronto, Canada
2006

Chair

IEEE International Conference on Multimedia and Expo
Session on Peer-to-Peer Multimedia Streaming
Toronto, Canada
2006

Chair

SPIE Electronic Imaging Conference on Visual Communications and Image Processing

Session on Computer Vision
San Jose, California
2006

Chair

IEEE International Conference on Acoustics, Speech, and Signal Processing
Session on Video Segmentation and Tracking
Philadelphia, Pennsylvania
2005

Chair

SPIE Electronic Imaging Conference on Image and Video Communications and Processing
Session on Selective Encryption for Image/Video
San Jose, California
2005

Chair

SPIE Electronic Imaging Conference on Image and Video Communications and Processing
Session on Object Tracking
San Jose, California
2005

Chair

INPT/ASME International Conference on Communications, Signals and Systems
Session on Signals and Data
Rabat, Morocco
2001

Chair

SPIE Conference on Multimedia Storage and Archiving Systems III
Session on Video Segmentation
Boston, Massachusetts
1998

Chair

IEEE International Conference on Image Processing
Session on Image Sequence Segmentation
Chicago, Illinois
1998

Chair

International Symposium on Mathematical Morphology
Session on Theory
Atlanta, Georgia
1996

Chair

INPT/ASME International Conference on Communications, Signals and Systems
Session on Signals and Data
Rabat, Morocco
1995

Chair

IEEE Workshop on Nonlinear Signal and Image Processing
Session on Mathematical Morphology and Fuzzy DSP
Neos Marmaras, Halkidiki, Greece
1995

Chair

IEEE International Conference on Image Processing
Session on Shape Representation and Image Modeling
Austin, Texas
1994

Chair

SPIE Conference on Visual Communications and Image Processing
Session on Mathematical Morphology
Boston, Massachusetts
1992

Chair

Conference on Information Sciences and Systems
Session on Signal Representation, Modeling, and Analysis
Baltimore, Maryland
1991

L.9. Panelist and Participant

Panelist

DOD Tri-Service Workshop on Stochastic Methods in Image Analysis
Session on Mathematical Morphology
U.S. Army Harry Diamond Laboratories
Adelphi, Maryland
1992

Participant

Institute for Mathematics and its Applications (IMA)
Workshop on Large Data Sets in Medical Informatics
Minneapolis, Minnesota
2011

Participant

NSF Workshop on Improving Domestic Student Participation
in Electrical and Computer Engineering Graduate Programs
University of Tennessee
Knoxville, Tennessee
2009

Participant

Workshop on Global Multimedia Mobile Communications
University of Illinois at Chicago

Chicago, Illinois
2005

Participant

Workshop on Extraction of Visual Information by Biological and Non-Biological Systems
University of Illinois at Chicago
Chicago, Illinois
2002

Participant

Workshop on Multimedia Information Systems
Capri, Italy
2001

Participant

NSF Advanced Networking Infrastructure Support
National Workshop on Developing Guidance
Research Competitiveness Program
Washington, D.C.
1999

Participant

Institute for Mathematics and its Applications (IMA)
Workshop on Applications and Theory of Random Sets
Minneapolis, Minnesota
1996

M. PUBLICATIONS

M.1. Thesis

- [1] D. Schonfeld, *Optimal Morphological Representation and Restoration of Binary Images: Theory and Applications*. Department of Electrical and Computer Engineering, The Johns Hopkins University, Baltimore, Maryland, 1990.

M.2. Books

- [1] C.-W. Chen, D. Schonfeld, and J. Liu, (Eds.), *Proceedings of the SPIE/IS&T International Conference on Visual Communication and Image Processing*. SPIE Press, 2007.
- [2] D. Schonfeld, C. Shan, D. Tao, and L. Wang, (Eds.), *Video Search and Mining*. Studies in Computational Intelligence Series, Springer-Verlag, 2010.

M.3. Book Chapters

- [1] M. Charif-Chefchaoui and D. Schonfeld, "Spatially-Variant Mathematical Morphology: Minimal Basis Representation," *Mathematical Morphology and Its Applications to Image and Signal*

Processing. P. Maragos, R.W. Schafer, and M.K. Butt, (ed.), pp. 49-56, Kluwer Academic Publishers: Boston, Massachusetts, 1996.

- [2] D. Schonfeld, "Weighted Composite Order-Statistics Filters: Optimal Morphological Pattern Recognition," *Mathematical Morphology and Its Applications to Image and Signal Processing*. P. Maragos, R.W. Schafer, and M.K. Butt, (ed.), pp. 163-170, Kluwer Academic Publishers: Boston, Massachusetts, 1996.
- [3] D. Schonfeld, "Image and Video Communication Networks," (**Invited Chapter**). *Handbook of Image and Video Processing*. A. Bovik (ed.), Academic Press: San Diego, California, Chapter 9.3, pp. 717-732, 2000.
- [4] D. Lelescu and D. Schonfeld, "Video skimming and summarization based on principal component analysis," *Management of Multimedia on the Internet*, Lecture Notes in Computer Science, E.S. Al-Shaer and G. Pacifici (Eds.), Springer-Verlag, pp. 128-141, 2001.
- [5] F. Bashir, S. Khanvilkar, A. Khokhar, and D. Schonfeld, "Multimedia systems: Content based indexing and retrieval," (**Invited Chapter**). *Electrical Engineering Handbook*. W-K. Chen (ed.), Academic Press: San Diego, California, pp. 379-400, 2004.
- [6] S. Khanvilkar, F. Bashir, D. Schonfeld, and A. Khokhar, "Multimedia networks and communication," (**Invited Chapter**). *Electrical Engineering Handbook*. W-K. Chen (ed.), Academic Press: San Diego, California, pp. 401-425, 2004.
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M.7. Presentations

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M.8. Patents

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N. KEYNOTE AND PLENARY TALKS

Stochastic noise process enhancement of nonlinear filtering

INPT/ASME International Conference on Communications, Signals and Systems

Rabat, Morocco

1995

VORTEX: Video Retrieval and Tracking from Compressed Multimedia Databases

INPT/ASME International Conference on Communications, Signals and Systems

Rabat, Morocco

2001

MotionSearch: Content-Based Video Retrieval and Activity Recognition in Video Surveillance

IEEE International Conference on Advanced Video and Signal Based Surveillance (AVSS)

Genoa, Italy

2009

Distributed Multi-Camera Networks: Graphical Models, Tensor Representation, and Plenoptic Functions

IEEE International Conference on Networking, Sensing, and Control (ICNSC)

Chicago, Illinois

2010

Signal Processing for Distributed Multi-Camera Networks: Theory and Applications
IEEE/IET International Conference on Audio, Language and Image Processing (ICALIP)
Shanghai, China
2010

The Visual Brain: Biologically-Inspired Imaging and Vision
International Conference on Intelligent Control and Information Processing (ICICIP)
International Conference on Brain Inspired Cognitive Systems (BICS)
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O. INVITED SEMINARS

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Morphological image representation: Theory and applications

DOD Tri-Service Workshop on Stochastic Methods in Image Analysis
U.S. Army Harry Diamond Laboratories
Adelphi, Maryland
1992

Morphological representation of nonlinear filters: Theory and applications

Department of Electrical and Computer Engineering
Illinois Institute of Technology
Chicago, Illinois
1993

Morphological image representation: Theory and applications

ONR Workshop on Vision and Optical Information Processing
Arlington, Virginia
1994

Nonlinear Signal and Image Processing

Department of Electrical Engineering and Computer Science
University of Illinois
Chicago, Illinois
1996

Nonlinear Operators: Theory and Application to Image Processing and Communications

School of Electrical and Computer Engineering
Technion – Israel Institute of Technology
Haifa, Israel
1996

Stochastic Noise Process Enhancement of Nonlinear Filtering

Department of Electrical Engineering
Northern Illinois University
DeKalb, Illinois
1996

Morphological Signal and Image Processing: Theory and Applications

Department of Electrical Engineering—Systems
University of Tel-Aviv
Tel-Aviv, Israel
1997

VORTEX: Video Retrieval and Tracking from Compressed Multimedia Databases

Department of Electrical and Computer Engineering
Illinois Institute of Technology
Chicago, Illinois
2001

Mathematical Morphology and Computer Vision
University of Illinois at Chicago
Chicago, Illinois
2002

VORTEX: Video Retrieval and Tracking from Compressed Multimedia Databases
Department of Electrical and Computer Engineering
Drexel University
Philadelphia, Pennsylvania
2002

**Time-Series Analysis Based on Statistical Signal Processing:
Segmentation, Prediction, and Tracking**
Global Electronic Trading Company (Getco)
Chicago, Illinois
2004

Particle Filtering for Head Tracking in Wireless Communications
Motorola Research Labs
Schaumburg, Illinois
2004

Real-Time Video Communications: Compression, Tracking, Retrieval, and Networking
University of Illinois
Chicago, Illinois
2005

Real-Time Video Tracking and Retrieval from Multimedia Databases
Motorola Research Labs
Schaumburg, Illinois
2005

**Real-Time Multiple Object Tracking and Motion Trajectory-Based Video Databases:
Indexing, Retrieval, and Activity Recognition**
Hewlett-Packard Research Labs
Haifa, Israel
2005

Real-Time Video Tracking Based on Particle Filtering
University of Illinois
Chicago, Illinois
2005

**Real-Time Collaborative Distributed Tracking and Trajectory Analysis from Multiple
Camera and Sensor Networks**
School of Electrical and Computer Engineering

Purdue University
West Lafayette, Indiana
2005

A New Method for Multidimensional Optimization and Its Application in Image and Video Processing

Department of Electrical Engineering and Computer Science
Northwestern University
Evanston, Illinois
2006

Protein Communication System: Evolution and Genomic Structure

Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign
Urbana-Champaign, Illinois
2006

Protein Communication System: Evolution and Genomic Structure

Bioinformatics Group
Mathematics and Computer Science Division
Argonne National Laboratory
Argonne, Illinois
2006

Distributed Image and Video Processing:

Directed Graphs, Bayesian Estimation, and Hidden Markov Models

College of Information Science and Engineering
Graduate School
Chinese Academy of Science
Beijing, P.R. China
2007

Distributed Image and Video Processing:

Directed Graphs, Bayesian Estimation, and Hidden Markov Models

Visual Computing Group
Microsoft Research Asia
Beijing, P.R. China
2007

Distributed Image and Video Processing:

Directed Graphs, Bayesian Estimation, and Hidden Markov Models

School of Electronic and Information Institute
Tongji University
Shanghai, P.R. China
2007

Distributed Image and Video Processing:

Directed Graphs, Bayesian Estimation, and Hidden Markov Models

School of Automation
Institute of Automation
Hangzhou Dianzi University

Hangzhou, P.R. China
2007

**Distributed Image and Video Processing:
Directed Graphs, Bayesian Estimation, and Hidden Markov Models**
Department of Information Science and Electronic Engineering
Institute of Information and Communication Systems
Zhejiang University
Hangzhou, P.R. China
2007

InteractiveVision: Distributed Image and Video Processing
Intellectual Property Technical Lecture Series
McAndrews, Held & Malloy, Ltd.
Chicago, Illinois
2007

**Distributed Image and Video Processing:
Directed Graphs, Bayesian Estimation, and Hidden Markov Models**
Departments of Computer Science and Electrical & Computer Engineering
Technion, Israel Institute of Technology
Haifa, Israel
2007

MotionSearch: Content-Based Video Retrieval and Classification
Joint Chapters of the IEEE
Rochester, New York
2008

Evolution and Genomic Structure: A Signal Processing Perspective
Bioinformatics Cluster
University of Rochester
Rochester, New York
2008

Evolution and Genomic Structure: A Signal Processing Perspective
Department of Electrical Engineering
Columbia University
New York, New York
2008

Evolution and Genomic Structure: A Signal Processing Perspective
Department of Electrical Engineering and Computer Science
Northwestern University
Evanston, Illinois
2008

MotionSearch: Content-Based Video Retrieval and Classification
Distinguished Speaker in the Joint College Colloquium Series
College of Engineering and Information Technology and College of Science and Mathematics
Department of Applied Science

University of Arkansas at Little Rock
Little Rock, Arkansas
2008

Evolution and Genomic Structure: A Signal Processing Perspective

Department of Electrical and Computer Engineering
University of Wisconsin – Madison
Madison, Wisconsin
2008

MotionSearch: Content-Based Video Retrieval and Classification

Department of Electrical & Computer Engineering
Tufts University
Medford, Massachusetts
2009

MotionSearch: Content-Based Video Retrieval and Classification

Department of Electrical & Microelectronics Engineering
Rochester Institute of Technology
Rochester, New York
2009

MotionSearch: Content-Based Video Retrieval and Classification

School of Computer Engineering
Nanyang Technological University
Singapore
2009

**Distributed Multi-Camera Networks: Graphical Models, Tensor Representation,
and Plenoptic Functions**

Department of Electrical and Computer Engineering
Illinois Institute of Technology
Chicago, Illinois
2010

**Personalized Visual Interaction: Robust Video-Conferencing and
Human-Computer Interaction Using a Two-Camera Computer System**

Qualcomm Corp.
San Diego, California
2010

Evolution and Genomic Structure: A Signal Processing Perspective

Department of Information Engineering and Computer Science - DISI
Microsoft Research-University of Trento Centre for Computational and Systems Biology
University of Trento
Trento, Italy
2010

**A Novel Cache Optimization Algorithm and Video Streaming Protocol
for Pure Peer-to-Peer Networks**

Motorola Research Labs

Schaumburg, Illinois
2010

**Distributed Multi-Camera Networks: Graphical Models, Tensor Representation,
and Plenoptic Functions**

Research Center of Automation
Northeastern University
Shenyang, P.R. China
2010

**Distributed Multi-Camera Networks: Graphical Models, Tensor Representation,
and Plenoptic Functions**

School of Automation and Electric Engineering
Zhejiang University of Science and Technology
Hangzhou, P.R. China
2010

**Distributed Multi-Camera Networks: Graphical Models, Tensor Representation,
and Plenoptic Functions**

Center for OPTical IMagery Analysis and Learning (OPTIMAL)
State Key Laboratory of Transient Optics and Photonics
Xi'an Institute of Optics and Precision Mechanics
Chinese Academy of Sciences
Xi'an, P.R. China
2010

Distributed Multi-Camera Networks: Graphs, Grammars, and Tensors

Dean's Leadership in Innovation Seminar Series
Advanced Analytics Institute (AAI)
University of Technology
Sydney, Australia
2012

Genomic Signal Processing: Evolution, Structure, and Regulation

Dean's Leadership in Innovation Seminar Series
Advanced Analytics Institute (AAI)
University of Technology
Sydney, Australia
2012

Distributed Multi-Camera Networks: Theory and Applications

Harbin Engineering University (HEU)
Harbin, China
2014

Distributed Multi-Camera Networks: Theory and Applications

Electrical and Computer Engineering Graduate Program
Ryerson University
Toronto, Canada
2014

P. GRADUATE STUDENTS AND VISTING SCHOLARS

P.1. Visiting Scholars

Mohammed Charif-Chefchaoui

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
Chicago, Illinois
1995

Position: Director and Professor, National Institute of Postes and Telecommunications, Morocco.

Yuesong Lin

Department of Electrical and Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2007

Position: Professor, Institute of Information and Control, Hangzhou Dianzi University, Hangzhou, P.R. China.

Haihong Chi

Department of Electrical and Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2010

Position: Associate Professor, College of Automation, Harbin Engineering University (HEU), Harbin, P.R. China.

Claudio Piciarelli

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
Chicago, Illinois
2010

Position: Postdoctoral Fellow, Department of Mathematics and Computer Science, University of Udine, Udine, Italy.

P.2. Postdoctoral Fellows

Mohammed Charif-Chefchaoui

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
Chicago, Illinois
1994

Position: Director and Professor, National Institute of Postes and Telecommunications, Morocco.

P.3. Visiting Students

Alessio Dore

Department of Electrical and Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2008

Former Position: Doctoral Candidate, DIBE - Department of Biophysical and Electronic Engineering,
University of Genova, Genoa, Italy.

Current Position: Postdoctoral Fellow, Imaging Sciences Centre, Institute of Biomedical Engineering,
Imperial College, London, United Kingdom.

Yunmei Gong

Department of Electrical and Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2008-09

Current Position: Doctoral Candidate, Information and Communication Engineering, College of
Electronics and Information Engineering, Tongji University, Shanghai, P.R. China.

Nicola Piatto

Department of Electrical and Computer Engineering
University of Illinois at Chicago
Chicago, Illinois
2010

Current Position: Doctoral Candidate, Department of Engineering and Computer Science – DISI,
Multimedia Signal Processing and Understanding Lab – MMLab, University of Trento, Trento, Italy.

P.4. Doctoral Students

Mohammed Charif-Chefchaoui

“Morphological Representation of Nonlinear Filters: Theory and Applications”

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
Chicago, Illinois
1993

Former Position: Professor, National Institute of Postes and Telecommunications, Rabat, Morocco.

Current Position: Director, National Institute of Postes and Telecommunications, Rabat, Morocco.

Dan Lelescu

“VORTEX: Video Retrieval and Tracking from Compressed Multimedia Databases”

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
Chicago, Illinois
2000

Former Position(s): Senior Research Scientist, Lead of Algorithms Group, Compression Sciences,
Campbell, California, USA; Senior Researcher, NTT DoCoMo Communications Laboratories USA, San
Jose, California, USA; Principal Scientist, Advanced Imaging Research & Development Laboratory,
Micron Technology, California, USA; Principal Engineer, Signal Processing, Pelican Imaging
Corporation, Mountain View, California, USA.

Current Position: Senior Director, Imaging and Signal Processing, Pelican Imaging Corporation,
Mountain View, California, USA.

Bulent Cavusoglu

“Real-Time Content-Based Video Communications over Heterogeneous Networks”

(Jointly Supervised with Prof. Rashid Ansari)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2005

Current Position: Assistant Professor, Ataturk University, Erzurum, Turkey.

Faisal Bashir

“MotionSearch: Object Motion Trajectory-Based Video Search and Classification System”

(Jointly Supervised with Prof. Ashfaq Khokhar)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2006

Internship: Mitsubishi Electric Research Laboratory (MERL), USA.

Former Position(s): Intern, Mitsubishi Electric Research Laboratory (MERL), Cambridge,

Massachusetts, USA; Senior Imaging Scientist, Retica Systems, Inc., Waltham, Massachusetts, USA;

Senior Vision Engineer, Heartland Robotics, Cambridge, Massachusetts, USA.

Current Position: Principal Engineer - Advanced Development Group, Security and Detection Systems, L-3 Communications, Woburn, Massachusetts, USA.

Wei Qu

“Real-Time Distributed Video Tracking of Multiple Objects from Single and Multiple Cameras”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2006

Internship: Mitsubishi Electric Research Laboratory (MERL), USA; Siemens Medical Systems, USA.

Former Position(s): Senior Research Scientist, Motorola Research Labs, Schaumburg, Illinois, USA;

Senior Scientist, Siemens Medical Solutions USA, Hoffman Estates, Illinois, USA; Associate Professor, Graduate University of Chinese Academy of Sciences, Beijing, China; CEO Special Assistant, Director of Technology, President of CSST Research, Hong Kong.

Current Position: Vice President, R&D, Special Assistant to CEO, President of Beijing Research Institute, Beijing, China.

Nidhal Bouaynaya

“Analysis of Proteomics and Genomics Based on Signal Processing and Communication Theory”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2007

Current Position: Assistant Professor, Department of Systems Engineering, University of Arkansas at Little Rock, Little Rock, Arkansas, USA.

Hunsop Hong

Constrained and Hierarchical Density Estimation for Image Reconstruction and Sensor Networks

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2008

Current Position: Senior Research Engineer, Samsung Information Systems America, Irvine, California, USA.

Pan Pan

Video Tracking Based on Particle Filters: Particle Allocation, Graphical Models, and Performance Evaluation

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2009

Internship: NTT Research Laboratory, Japan; Mitsubishi Electric Research Laboratory (MERL), USA.

Former Position: Project Manager, Fujitsu Research and Development, Beijing, China.

Current Position: Technical Expert, Alibaba Group, Beijing, China.

Xiang Ma

Motion Trajectory-Based Video Retrieval and Recognition: Tensor Analysis and Multi-Dimensional Hidden Markov Models

(Jointly Supervised with Prof. Ashfaq Khokhar)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2009

Internship: Knowledge Media Institute, Open University, United Kingdom; Siemens Medical Solutions USA, Hoffman Estates, Illinois, USA; Computer Vision Research Engineer, IntuVision, Inc., Woburn, Massachusetts, USA.

Former Position: Senior Research Scientist and Engineer, IntuVision, Inc., Woburn, Massachusetts, USA.

Current Position: Senior Engineer - R&D Computer Vision, Nokia Location and Commerce, Chicago, Illinois, USA.

Junlan Yang

Virtual Video Enhancement for Handheld Mobile Cameras: Stabilization, Auto-Focus, and Super-Resolution

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2009

Internship: Ricoh Research Laboratory, Menlo Park, California, USA; Sharp Laboratories of America, USA.

Former Position: Research Engineer, iKoa Corporation, Menlo Park, California, USA.

Current Position: Algorithm Engineer, Marseille Networks, Santa Clara, California, USA.

Chong Chen

Multi-Camera Vision Systems: Distributed Pose Estimation and Plenoptic Imaging

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2009

Internship: Siemens Research Laboratory, USA; FX Palo Alto Laboratory (FXPAL), USA; Abbott Laboratories, USA.

Former Position: Senior Research Engineer, Samsung Information Systems America, Irvine, California, USA.

Current Position: Video Engineer, Apple, Cupertino, California, USA.

Xu Chen

Localization and Trajectory Estimation of Mobile Objects from a Single Sensor

(Jointly Supervised with Prof. Ashfaq Khokhar)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

Internship: Institute of Electrical Engineering, Ecole Polytechnique Fédérale de Lausanne (EPFL),

Switzerland; Kodak Research Laboratories, USA.

Former Position(s): Postdoctoral Fellow, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan, USA; Postdoctoral Fellow, Department of Electrical and Computer Engineering, Duke University, Durham, North Carolina, USA.

Current Position: Senior Researcher, Sharp Laboratories of America, Camas, Washington, USA.

Lei Gao

Compiler Optimization for Translating Software Binaries onto FPGAs

(Jointly Supervised with Prof. Prith Banerjee)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

Internship: Binachip, Inc., Chicago, Illinois, USA.

Former Position: Senior Engineer, Binachip, Inc., Chicago, Illinois, USA.

Current Position: Senior R&D Engineer, Synopsis, Inc., Marlborough, Massachusetts, USA.

Liuling Gong

Machine Learning for Signal Processing:

Geometry, Kernels, and Symbolic Sequences

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

Internship: eBay Research Labs, USA.

Former Position: Postdoctoral Fellow, Center for the Study of Complex Systems, University of Michigan, Ann Arbor, Michigan, USA.

Current Position: Seismic Imager, CGGVeritas, Houston, Texas, USA.

Songqing Zhao

Multiple Description Coding for Correlated Multi-Path Networks

(Ex-Officio; Jointly Supervised by Profs. Rashid Ansari and Daniela Tuninetti)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

Internship: Mitsubishi Electric Research Laboratory (MERL), USA.

Former Position: Voice and Data Quality Engineer, Voice & Data Quality and Performance Analysis Group, Alcatel-Lucent, Murray Hill, New Jersey, USA.

Current Position: Wireless Engineer, Apple, Cupertino, California, USA.

Xiangqiong Shi

Bayesian Networks: Performance Analysis of Loopy Belief Propagation

(Jointly Supervised with Prof. Daniela Tuninetti)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2011

Internship: Motorola Research Labs, Schaumburg, Illinois, USA; Technicolor, Research & Innovation, Princeton, New Jersey, USA; Nokia Research Center, Palo Alto, California, USA.

Liming Wang

Genomic Signal Processing and Regulatory Networks: Representation, Dynamics and Control

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2011

Former Position: Postdoctoral Fellow, Department of Electrical Engineering, Columbia University, New York, New York, USA.

Former Position: Postdoctoral Associate, Department of Electrical and Computer Engineering, Duke University, Durham, North Carolina, USA.

Jing Huang

Distributed Signal and Image Processing:

Particle Filters, Context Grammars, and Dynamic Games

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2013

Internship: Fuji Xerox Palo Alto Laboratory (FXPAL), Palo Alto, California, USA; Motorola Mobility, Applied Research Center, Libertyville, Illinois, USA; Nokia Research Center, Berkeley, California, USA.

Current Position: Software Development Engineer, TeraRecon, Inc., Foster City, California, USA.

Qun Li

Multilinear Algebra in High-Order Data Analysis: Retrieval, Classification and Representation

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2013

Internship: Xerox Research Center, Xerox Innovations Group, Webster, New York, USA.

Current Position: Postdoctoral Fellow, Xerox Research Center, Xerox Innovations Group, Webster, New York, USA.

Johnson Jonaris GadElkarim Keiriz

From Micro to Macro: A Study of Human Brain Structure Based on Diffusion MRI and Neuronal Networks

(Jointly Supervised by Profs. Alex Leow and Richard Magin)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2013

Former Position: Postdoctoral Fellow, Department of Psychiatry, University of Illinois, Chicago, Illinois, USA.

Current Position: Lead Developer, nView medical Inc., Salt Lake City, Utah, USA.

Lingdao Sha

Three-Dimensional Television Systems

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2015 (exp.)

Haoyu Wang

Genomic Signal Processing

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2015 (exp.)

P.5. Masters Thesis Students

Vladimir Pavlovic

“Stochastic Noise Process Enhancement of Hopfield Neural Networks”

(Jointly Supervised with Prof. Gary Friedman)

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1993

Position: Associate Professor, Department of Computer Science, Rutgers University, New Jersey, USA.

Deepak K. Bal

“Transmission of Real-Time MPEG-2 Video Over Differentiated Services Networks”

(Jointly Supervised with Prof. Rashid Ansari)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2003

Position: Takata, Inc., Michigan, USA.

Karthik Hariharakrishnan

“Visual Tracking: New Methods Using Adaptive Block Matching and Particle Filters”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2003

Internship: NeoMagic Corp., USA.

Previous Position(s): National Instruments, India; Motorola, India; Senior Design Engineer, ARM, Ltd., United Kingdom.

Current Position: Staff Software Engineer, ARM, Ltd., United Kingdom.

Subhash Balam

“Associative Processors for Video Coding”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2004

Position: Senior Staff Engineer/Manager, Qualcomm Corp., California, USA.

Emir Mulabegovic

“Lightweight Streaming Protocol for Real-Time Video Communications”

(Jointly Supervised with Prof. Rashid Ansari)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2005

Former Position: PCTEL, Illinois, USA.

Current Position: Systems Architect, Personal, Inc., Sarajevo, Bosnia and Herzegovina.

Andrea De Mauro

“A Peer-to-Peer Network for Real-Time Multiple-Description Video Communications
Using Multiple Paths”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2006

Former Position: Financial Solutions Systems Analyst, Procter & Gamble, Newcastle, United Kingdom.

Current Position: Business Intelligence Manager, Procter & Gamble, Newcastle, Rome, Italy.

Claudio Rossi

“A Partially-Reliable Multihomed Transport Protocol for Real-Time Multiple-Description
Multimedia Traffic”

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2006

Position: Area Manager, IBM, Milan, Italy.

Amita Talati

Design and Evaluation of Data Compression and Decompression Applications on Field Programmable
Gate Arrays

(Jointly Supervised with Prof. Prith Banerjee)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2008

Former Position: Customer Applications Engineer, Newark Corporation, Cleveland, Ohio, USA.

Current Position: Senior Engineer, Newark Corporation, Cleveland, Ohio, USA.

Carlo Giuliatti

A Novel Cache Optimization Algorithm and Protocol for Video Streaming in Pure Peer-to-Peer Networks

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

Position: Software Engineer, Astek, Sophia Antipolis, France.

Edmond Gjondrekaj

Clustering and Similarity Analyses of miRNA Assay by Means of Reprogrammable Devices

Department of Electrical & Computer Engineering

University of Illinois at Chicago

Chicago, Illinois

2010

P.6. Masters Project Students

Neil Zalut

“Linear Restoration of Medical Images: An Overview”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1993

Branislav Kisacanin

“A Fast Thresholded Linear Convolution Representation of Morphological Operations”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1993

Alan Baumgartner

“Morphological Segmentation of Computed Tomography Images”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1994

Alvin Ng

“Spatially-Variant Morphological Skeleton Representation”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1994

Smriti Anand

“Efficient Fast Reconstruction Algorithms in Computerized Tomography”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois, May 1995

Stephan W. Wegerich

“Subband Image Restoration and Blur Identification Using the EM Algorithm and Cross-Filtering”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1995

Robert Werckmeister

“Performance Analysis of Video Communications in Multimedia Networks”

(Jointly Supervised with Prof. Ouri Wolfson)

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1996

Margaret Kelton

“A Fast Method for Transform Conversion for Use in Image Processing”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1998

Kailash Ravishankar

“Frequency Prediction of High-Order Autoregressive Moving Average Sequences”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1998

Amir Yafe

“Transmission of MPEG-2 Streams Over Packet-Switched Networks”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1998

Steven J. Doering

“Digital Modulation: Applications to CDMA Communication Systems (IS-95)”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1999

Abhijit Bhattacharya

“MPEG-1 and H.263 Video Decoding on Motorola GSM Cellular Phone”

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

1999

Qin Cai

“Differentiated Transmission of MPEG-2 Video Bitstream Over Communication Networks”

(Jointly Supervised with Prof. Rashid Ansari)

Department of Electrical Engineering and Computer Science

University of Illinois at Chicago

Chicago, Illinois

2000

Q. RESEARCH GRANTS

D. Schonfeld (PI)

“Morphological image representation: Theory and applications”

Office of Naval Research (ONR)

\$150,000

1991-1995

S. Corson (PI) and D. Schonfeld (Co-PI)

“Parallel processing research”

University of Illinois

Campus Research Board (CRB)

\$14,995

1994-1995

R. Ansari (PI), P. Hesketh (Co-PI), and D. Schonfeld (Co-PI)

“One-step process for instant ticket validation”

GTECH Corporation

\$5,000

1997

D. Schonfeld (PI)

“National Communications Forum”

International Engineering Consortium (IEC)

\$500

2000

D. Schonfeld (PI)

“Real-Time Very-Low Bit-Rate MPEG-4 Video Compression for Wireless Communication Application”

Neomagic Corporation

\$69,553

2001-2003

A. Khokhar (PI), R. Ansari (Co-PI), R. Grossman (Co-PI), D. Schonfeld (Co-PI), and C. Yu (Co-PI)

“High-Speed Terabyte Storage Server Based on Intelligent Disk Technology”

Army Research Office (ARO)

DURIP Program

\$422,626

2002-2004

D. Schonfeld (PI)
 “Computer Architectures for Real-Time Video Communications”
Neomagic Corporation
 \$76,075
 2002-2004

M. Dutta (PI) et al.
 “Design of a Super-Biological Eye Sensor System”
Defense Advanced Research Projects Agency (DARPA)
Army Research Office (ARO)
 \$200,000 (Seed Project)
 2002-2003

D. Schonfeld (PI)
 “OMAP Code Composure Studio Software for Real-Time Video Communications”
Texas Instruments, Inc.
 DSP University Program
 \$4,500
 2003

D. Schonfeld (PI)
 “Real-Time Object Tracking of Video Sequences on Associative Processor Arrays”
Neomagic Corporation
 \$68,750
 2003-2005

D. Schonfeld (PI)
 “Real-Time Low-Power High-Quality Interactive Video Telephony
 for Wireless Communication Applications”
Motorola, Inc.
 \$19,331
 2004-2005

D. Schonfeld (PI)
 “Real-Time Low-Power High-Quality Interactive Video Communications
 for Video Animation and Stereography”
Motorola, Inc.
 \$22,000
 2005-2006

D. Schonfeld (PI)
 “Real-Time High-Quality Video Communications from Handheld Cameras
 Using Video Stabilization and Auto-Focus”
Motorola, Inc.
 \$75,000
 2005-2008

D. Schonfeld (PI)
 “Interactive Video Communications Based on Stereographic Imaging
 From a Single Camera”
Motorola, Inc.

\$22,000
2006-2007

A. Khokhar (PI) and D. Schonfeld (Co-PI)
“MotionSearch: Motion Trajectory-Based Object Activity Retrieval and Recognition from Video and Sensor Databases”
National Science Foundation (NSF)
\$410,000
2006-2009

D. Schonfeld (PI)
“Real-Time Financial Forecasting Based on Statistical Signal Processing: Correlation Analysis and Fast Algorithms”
Gelber Group
\$66,522
2006-2007

D. Schonfeld (PI)
“Signal Communication and Processing in a RFID Sensor Network System”
Your Life Essentials
\$4,000
2006-2008

D. Schonfeld (PI)
“MobilePlenoptics: Panoramic Video Communications in Mobile Devices”
Motorola, Inc.
\$22,000
2007-2008

D. Schonfeld (PI)
“Machine Learning and Event Detection in Biological Systems”
VG Bioinformatics, Inc.
\$40,000
2007-2008

A. Khokhar (PI) and D. Schonfeld (Co-PI)
“International Supplement to MotionSearch: Motion Trajectory-Based Object Activity Retrieval and Recognition from Video and Sensor Databases”
National Science Foundation (NSF)
\$37,468
2007-2008

D. Schonfeld (PI)
“InteractiveVision: Collaborative Multiple-Input-Multiple-Output Inverse Problems with Application in Image and Video Processing”
National Science Foundation (NSF)
\$232,496
2007-2010

A. Khokhar (PI) and D. Schonfeld (Co-PI)

“Research Experiences for Undergraduates (REU) Supplement to MotionSearch: Motion Trajectory-Based Object Activity Retrieval and Recognition from Video and Sensor Databases”

National Science Foundation (NSF)

\$12,000

2008-2009

D. Schonfeld (PI)

“Real-time Superresolution for Enhanced Video Streaming”

iKoa Corporation

\$25,000

2008-2009

D. Schonfeld (PI)

“Tracking Performance Evaluation based on a Reflective Model and Perturbation Analysis”

Mitsubishi Electric Research Laboratories (MERL)

\$1,228

2009

R. Magin (PI), M. Ragozzino (Co-PI), K. Rockne (Co-PI), T. Royston (Co-PI), and D. Schonfeld (Co-PI)

“Acquisition of a High Field Magnetic Resonance Imaging System for Science and Engineering Research”

National Science Foundation (NSF)

\$1,995,000

2009

D. Schonfeld (PI), N. Bouaynaya (Key/Senior Personnel), and H.M. Fathallah-Shaykh (Key/Senior Personnel)

“Minimal-Perturbation Dynamic Control of the Melanoma Gene Regulatory Network” (R01)

National Institutes of Health (NIH)

\$1,200,000

2010-1014

R. ADMINISTRATIVE ACTIVITIES

R.1. Administrative Positions

Director

University-Industry Engineering Research Center (UIERC)

College of Engineering

University of Illinois at Chicago

2008—2011

Supervisor

Web Development

Department of Electrical & Computer Engineering

University of Illinois at Chicago

2001—2002

Director

Timetable Schedule

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1999—2000

R.2. University Committees

Co-Chair

University All-Campus Promotion and Tenure Committee

University of Illinois at Chicago
2010—2011

Member

University Vision and Strategy

(Recommendations to World Business Chicago)
University of Illinois at Chicago
2012—Present

Member

University Ad-Hoc Advisory Committee for the Office of Faculty Affairs

University of Illinois at Chicago
2012—2013

Member

University Task Force to Review Non-Tenure Promotion Guidelines

University of Illinois at Chicago
2011—2012

Member

University Promotion and Tenure Norms and Criteria Committee

University of Illinois at Chicago
2011—2012

Member

University Honorary Degree Nominating Committee

University of Illinois at Chicago
2010—2011

Member

University Promotion and Tenure Seminar Panel

Natural Science, Health Science, and Engineering
University of Illinois at Chicago
2010—2011

Member

University All-Campus Promotion and Tenure Committee

University of Illinois at Chicago
2008—2011

Member
University Campus Research Board Committee
University of Illinois at Chicago
2001—2004

Member
University Awards Committee
University of Illinois at Chicago
1998—2001

Member
Student Appeals Board
University of Illinois at Chicago
2004—2005

R.3. College Committees

Member
College Executive Committee
College of Engineering
University of Illinois at Chicago
2009-2012

Member
Dean of the College of Engineering Search Committee
College of Engineering
University of Illinois at Chicago
2007-2008

Member
Wexler Chair in Information Technology Search Committee
College of Engineering
University of Illinois at Chicago
2006

Member
Advisory Committee for Bioinformatics Program in Bioengineering
University of Illinois at Chicago
2000—2010

Chair
Networking Curriculum Subcommittee
College of Engineering
University of Illinois at Chicago
2005

Member
Departmental Reorganization and Formation Committee
College of Engineering
Department of Electrical Engineering & Computer Science

University of Illinois at Chicago
1999—2000

R.4. Departmental Committees

Chair

Departmental Faculty Search Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2006—2008; 2010-2011

Chair

Departmental Grievance Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2013—Present

Chair

Departmental Research & Colloquium Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1996—1998; 2003—2004

Chair

Departmental Seminar Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2008—2010

Chair

Departmental Web Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2001—2003

Member

Departmental Advisory Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
1995—1996; 1998—1999; 2000—2002; 2004—2005; 2007—2010

Member

Departmental Computer Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
1990—1992; 2001—2004

Member

Departmental Computer & Web Committee

Department of Electrical & Computer Engineering

University of Illinois at Chicago
2013—Present

Member

Departmental Electronics Instructional Laboratory Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1997—1998

Member

Departmental Faculty Search Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1994—1995; 1998—2001; 2006—2008; 2010-2011

Member

Departmental Graduate Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1995—2000; 2011—Present

Member

Departmental Grievance Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2012—Present

Member

Departmental Promotion & Tenure Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
1996—Present

Member

Departmental Research & Colloquium Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1992—1998; 2001—2004

Member

Departmental Scholarship Committee

Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1990—1996

Member

Departmental Seminar Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2008—2013

Member

Departmental Undergraduate Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
1998—2003; 2005—2011

Member

Departmental Web Committee

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2000—2011

R.5. Curriculum Committees

Chair

Departmental Communications and Networks Curriculum Subcommittee

of the Undergraduate and Graduate Committees
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2001—2002; 2004

Chair

Departmental Signal Processing Curriculum Subcommittee

of the Undergraduate and Graduate Committees
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2011

Member

Departmental Communications Curriculum Subcommittee

of the Undergraduate and Graduate Committees
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2011

Member

Departmental Communications and Networking Curriculum Subcommittee

of the Undergraduate and Graduate Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2001—2002; 2004

Member

Departmental Computer Engineering Curriculum Subcommittee

of the Undergraduate and Graduate Committee
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1998—2002

Member

Departmental Electrical Engineering Curriculum Subcommittee
of the Undergraduate and Graduate Committee
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1996—2000

Member

Departmental Imaging Curriculum Subcommittee
of the Undergraduate and Graduate Committees
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1993

Member

Departmental Information and Computer Systems Curriculum Subcommittee
of the Undergraduate and Graduate Committees
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2011

Member

Departmental Masters of Engineering Program Subcommittee
of the Graduate Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2005

Member

Departmental Multimedia Curriculum Subcommittee
of the Undergraduate and Graduate Committees
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
2005

Member

Departmental Networking Curriculum Subcommittee
of the Undergraduate and Graduate Committees
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1999—2000; 2005

Member

Departmental Signals and Systems Curriculum Subcommittee
of the Graduate Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2004

Member

Departmental Signal Processing Curriculum Subcommittee
of the Undergraduate and Graduate Committees

Department of Electrical & Computer Engineering
University of Illinois at Chicago
2011

Member

Departmental Signal Processing and Communications Curriculum Subcommittee
of the Undergraduate and Graduate Committees
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1991

Member

Departmental Student Cheating Policy Subcommittee
of the Undergraduate Committee
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1999

Member

Departmental Teaching Assistant Assignment Subcommittee
of the Undergraduate Committee
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1996—1997

Member

Departmental Teaching Assistant Award Subcommittee
of the Scholarship Committee
Department of Electrical Engineering & Computer Science
University of Illinois at Chicago
1994

R.6. Qualifier Committees

Chair

Departmental Communication Qualifier Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2003—2004; 2012

Chair

Departmental Computer Communication Network Qualifier Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago
2002—2003; 2005

Chair

Departmental Signal Processing Qualifier Committee
Department of Electrical & Computer Engineering
University of Illinois at Chicago

1991—1995; 2001; 2002; 2008—2009

Member

Departmental Communication Qualifier Committee

Department of Electrical & Computer Engineering

University of Illinois at Chicago

1997—2004; 2009—Present

Member

Departmental Computer Communication Networks Qualifier Committee

Department of Electrical & Computer Engineering

University of Illinois at Chicago

2002—2005

Member

Departmental Computer Vision Qualifier Committee

Department of Electrical Engineering & Computer Science

University of Illinois at Chicago

1993—2001

Member

Departmental Signal Processing Qualifier Committee

Department of Electrical & Computer Engineering

University of Illinois at Chicago

1991—2001; 2004—2009

R.7. Research Laboratories and Centers

Director

University-Industry Engineering Research Center (UIERC)

College of Engineering

University of Illinois at Chicago

2008—Present

Co-Director

Multimedia Communications Laboratory (MCL)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

1997—Present

Member

Departmental Signal and Image Research Laboratory (SIRL)

Department of Electrical & Computer Engineering

University of Illinois at Chicago

1991—2002

S. TEACHING ACTIVITIES

S.1. The Johns Hopkins University

ECE 137
Digital Signals and Systems
Fall 1987

ECE 137
Digital Signals and Systems
Fall 1988

ECE 137
Digital Signals and Systems
Fall 1989

S.2. University of Illinois at Chicago

EECS 212
Signal Processing
Fall 1990

EECS 212
Signal Processing
Winter 1991

EECS 416
Advanced Topics in Digital Signal Processing
Spring 1991

EECS 417
Digital Signal Processing
Fall 1991

EECS 554
Estimation Theory
Fall 1991

EECS 311
Communication Engineering
Spring 1992

EECS 554
Estimation Theory
Fall 1992

EECS / BioE 479
Real-Time Data Processing
Spring 1993

EECS / BioE 479
Real-Time Data Processing

Fall 1993

EECS 516

Optimal and Adaptive Digital Filters

Fall 1993

EECS 517

Image Processing

Spring 1994

EECS / BioE 479

Real-Time Data Processing

Fall 1994

EECS 517

Image Processing

Spring 1995

EECS 531

Detection and Estimation Theory

Spring 1995

EECS / BioE 479

Real-Time Data Processing

Fall 1995

EECS 517

Image Processing

Spring 1996

EECS 531

Detection and Estimation Theory

Spring 1996

EECS 530

Statistical Communication Theory

Fall 1996

EECS 517

Image Processing

Spring 1997

EECS / BioE 407

Pattern Recognition

Fall 1997

EECS 530

Statistical Communication Theory

Fall 1997

EECS / BioE 407

Pattern Recognition
Spring 1998

EECS 517
Image Processing
Spring 1998

EECS 517
Image Processing
Motorola Campus
Spring 1998

EECS 171
Introduction to Programming
Summer 1998

EECS 516
Optimal and Adaptive Digital Filters
Fall 1998

EECS 530
Statistical Communication Theory
Motorola Campus
Fall 1998

EECS 418
Digital Signal Processing II
Spring 1999

EECS 517
Image Processing
Spring 1999

EECS 531
Detection and Estimation Theory
Motorola Campus
Spring 1999

EECS 171
Introduction to Programming
Summer 1999

EECS 417
Digital Signal Processing I
Fall 1999

EECS 491
Multimedia Communication Networks
Spring 2000

EECS 311

Communication Engineering
Summer 2000

EECS 491
Multimedia Communication Networks
Internet Course (Preparation)
Fall 2000

EECS 516
Optimal and Adaptive Digital Filters
Fall 2000

EECS 531
Detection and Estimation Theory
Fall 2000

EECS 491
Multimedia Communication Networks
Internet Course
Spring 2001

EECS 517
Image Processing
Spring 2001

EECS 171
Introduction to Programming
Summer 2001

ECE 516
Optimal and Adaptive Digital Filters
Fall 2001

ECE 531
Detection and Estimation Theory
Fall 2001

ECE 434
Multimedia Communication Networks
Internet Course
Spring 2002

ECE 517
Image Processing
Spring 2002

CS 102
Introduction to Programming
Summer 2002

ECE 433

Computer Communication Networks
Fall 2002

ECE 434
Multimedia Communication Networks
Fall 2002

ECE 333
Computer Communication Networks
Laboratory (Preparation)
Spring 2003

ECE 311
Communication Engineering
Fall 2003

ECE 434
Multimedia Communication Networks
Fall 2003

ECE 517
Image Processing
Spring 2004

ECE 434
Multimedia Communication Networks
Fall 2004

ECE 516
Optimal and Adaptive Digital Filters
Fall 2004

ECE 517
Image Processing
Spring 2005

ECE 311
Communication Engineering
Summer 2005

ECE 434
Multimedia Communication Systems
Fall 2005

ECE 516
Optimal and Adaptive Digital Filters
Fall 2005

ECE 517
Image Processing
Spring 2006

ECE 311

Communication Engineering
Summer 2006

ECE 434

Multimedia Communication Systems
Fall 2006

ECE 516

Optimal and Adaptive Digital Filters
Fall 2006

ECE 531

Detection and Estimation Theory
Spring 2007

ECE 311

Communication Engineering
Summer 2007

ECE 434

Multimedia Communication Systems
Fall 2007

ECE 516

Optimal and Adaptive Digital Filters
Fall 2007

ECE 531

Detection and Estimation Theory
Spring 2008

ECE 434

Multimedia Communication Systems
Fall 2008

ECE 516

Optimal and Adaptive Digital Filters
Fall 2008

ECE 530

Random Signal Analysis
Spring 2009

ECE 517

Image Processing
Fall 2009

ECE/BIOE 407

Pattern Recognition

Spring 2010

ECE 434

Multimedia Communication Systems
Fall 2010

ECE 530

Random Signal Analysis
Spring 2011

ECE 434

Multimedia Communication Systems
Fall 2011

ECE 530

Random Signal Analysis
Spring 2012

ECE 594

Machine Learning
Spring 2012

ECE 434

Multimedia Communication Systems
Fall 2012

ECE 517

Image Processing
Fall 2012

ECE 530

Random Signal Analysis
Spring 2013

ECE 434

Multimedia Communication Systems
Fall 2013

ECE 517

Image Processing
Fall 2013

S.3. University of Trento

Content-Based Video Analysis: Tracking, Retrieval, and Classification

Information and Communication Technology (ICT) – International Doctoral School
Department of Information Engineering and Computer Science
University of Trento
May 2010

Last Updated: May 31, 2012

APPENDIX B

Expert Testimony During the Past Four Years (2010-2014):

Consultant and Expert Witness **

Quinn Emanuel Urquhart & Sullivan, LLP on behalf of Barnes & Noble, Inc.

and barnesandnoble.com LLC

in Barnes & Noble, Inc. v. LSI Corp.

(Involved exclusively with MPEG patents)

USDC Northern District of California

Civil Action No. 3:11-CV-2709-EMC

Multimedia Systems

San Francisco, California

2013—2014

Consultant and Expert Witness * **

McDermott Will & Emery, LLP on behalf of Panasonic Corporation and Panasonic Corporation of North America

in Black Hills Media, LLC v. Panasonic Corporation, et al.

ITC 337-TA-882

Multimedia Systems

Irvine, California

2013—2014

Consultant and Expert Witness *

Desmarais, LLP on behalf of Nokia Corporation and Nokia Inc.

in Nokia Inc. v. HTC Corp.

ITC 337-TA-885

Multimedia Systems

New York, New York

2013—2014

Consultant and Expert Witness * **

Quinn Emanuel Urquhart & Sullivan, LLP on behalf of Samsung Electronics Co., Ltd.,

Samsung Electronics America, Inc., and Samsung Telecommunications America, LLC

in Apple Inc. v. Samsung Electronics Co., Ltd., et al.

(Involved exclusively with counterclaims for patents asserted by Samsung Electronics)

USDC District of Northern District of California

Civil Action No. 12-cv-00630-LHK

Multimedia Systems

Redwood Shores, California

2013—2014

Consultant and Expert Witness * **

Desmarais, LLP on behalf of Intellectual Ventures I, LLC, and Intellectual Ventures II, LLC

in Intellectual Ventures I & II v. Canon Inc., et al.

(Involved exclusively with imaging patents)

USDC District of Delaware

Civil Action No. 1:11-CV-792
Multimedia Systems
New York, New York
2012—2014

Consultant and Expert Witness * **

McDermott Will & Emery, LLP on behalf of Funai Electric Co., Ltd. et al.
in LSI Corp. and Agere Systems, Inc. v. Funai Electric Company, Ltd. et al.
(Involved exclusively with MPEG patents)
ITC 337-TA-837
Multimedia Retrieval, Storage, and Communication Systems
Washington, D.C.
2012—2013

Consultant and Expert Witness * **

Quinn Emanuel Urquhart & Sullivan, LLP on behalf of MediaTek, Inc. et al.
in LSI Corp. and Agere Systems, Inc. v. Funai Electric Company, Ltd. et al.
(Involved exclusively with MPEG patents)
ITC 337-TA-837
Multimedia Retrieval, Storage, and Communication Systems
New York, New York
2012—2013

Consultant & Expert Witness *

Nixon & Vanderhye, P.C. on behalf of Touchtunes Music Corp.
in Touchtunes Music Corp. v. Rowe International Corp., Arachnid, Inc., AMI Entertainment,
Inc., and Merit Industries, Inc.
USDC Southern District of New York
Civil Action No. 07-cv-11450
Multimedia Retrieval, Storage, and Communication Systems
Arlington, Virginia
2012—2013

Consultant and Expert Witness * **

Heptig Law Group, Ltd and Cooley, LLP on behalf of Realtime Data, LLC
in Realtime Data, LLC v. MetroPCS Texas et al.
(Involved exclusively with infringement analysis)
USDC Eastern District of Texas
Civil Action No. 6:10-cv-00493-LED
Multimedia Retrieval, Storage, and Communication Systems
Dallas, Texas
2011—2013

Consultant and Expert Witness * **

Morgan, Lewis & Bockius LLP on behalf of ActiveVideo Networks, Inc.
in ActiveVideo Networks, Inc. v. Verizon Communications, Inc.

(Involved exclusively with claims for patents asserted by ActiveVideo Networks)
USDC Eastern District of Virginia
Civil Action No. 2:10-cv-248 RAJ/FBS
Cable Television Systems
Palo Alto, California
2011

Consultant and Expert Witness * **
Quinn Emanuel Urquhart & Sullivan, LLP on behalf of Cablevision Systems Corp.
in Cablevision Systems Corp. v. Verizon Communications, Inc.
(Involved exclusively with infringement analysis)
ITC 337-TA-712
Cable Television Systems
New York, New York
2010—2011

Consultant & Expert Witness *
Keker and Van Nest, LLP and Latham and Watkins, LLP on behalf of Broadcom Co.
in Broadcom Corp. v. SiRF Technology, Inc. and CSR plc
(Involved exclusively with graphics imaging patents)
USDC Central District of California
Civil Action No. SACV08-546 JVS (MLGx)
Graphics Processing and Display Systems
San Francisco, California
2010—2011

Consultant & Expert Witness *
Winston & Strawn, LLP on behalf of Lear Group, Ltd.
in Chamberlain Group, Inc. v. Lear Corp., Ltd
USDC Northern District of Illinois
Civil Action No. 05-cv-3449
Signal Processing Systems
Chicago, Illinois
2009—2011

Consultant and Expert Witness * **
Jones Day on behalf of Arris Group, Inc.
in Arris Group, Inc. v. SeaChange International, Inc.
USDC District of Delaware
Civil Action No. 01-011 (JJF)
Cable Television Systems
Chicago, Illinois
2009—2012

Consultant & Expert Witness *
McAndrews, Held & Malloy, Ltd. on behalf of Broadcom Co.

in Broadcom Corp. v. SiRF Technology, Inc. and CSR plc
(Involved exclusively with graphics imaging patents)
USDC Central District of California
Civil Action No. SACV08-546 JVS (MLGx)
Graphics Processing and Display Systems
Chicago, Illinois
2008—2010

* Testified by deposition.

** Testified at trial or hearing.

APPENDIX C

Information Considered

Description
U.S. Patent No. 7,095,945
Prosecution History of U.S. Patent No. 7,095,945
U.S. Patent No. 6,233,389 (“Barton”)
U.S. Patent No. 6,397,000 (“Hatanaka”)
U.S. Patent No. 6,591,058 (“O’Connor”)
U.S. Patent No. 5,521,922 (“Fujinami”)
Andrew S. Tanenbaum, <i>Computer Networks</i> . Prentice Hall, Third Edition, 1996
International Standard ISO/IEC 11172:1993 “Information Technology—Coding of Moving Pictures and Associated Audio for Digital Storage Media Up To About 1,5 Mbit/s
International Standard ISO/IEC 13818:1996 “Information Technology—Generic Coding of Moving Pictures and Associated Audio Information”
MPEG-2 Systems (<i>i.e.</i> , ISO/IEC 13818-1) is also referred to as H.222.0

APPENDIX D

'945 Claim Element	Barton (Ex. 1005)
18. A method comprising: determining a mode of operation;	<p>“<u>User control commands are accepted and sent through the system.</u> These commands affect the flow of said MPEG stream and allow the user to view stored programs with at least the following functions: <u>reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.</u>”¹ Ex. 1005, at 2:33-38; <i>see also id.</i> at 6:36-46.</p> <p>“The invention additionally provides the user with the ability to <u>store selected television broadcast programs while simultaneously watching or reviewing another program and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.</u>” <i>Id.</i> at 3:23-29; <i>see also id.</i> at 4:14-23, 4:45-54, 7:5-9.</p> <p>“The derived class and resulting objects described here <u>may be combined in an arbitrary way to create a number of different useful configurations for storing, retrieving, switching and viewing of TV streams.</u> For example, if multiple input and output sections are available, <u>one input is viewed while another is stored, and a picture-in-picture window generated by the second output is used to preview previously stored streams.</u> Such configurations represent a unique and novel application of software transformations to achieve the functionality expected of expensive, sophisticated hardware solutions within a single cost-effective device.” <i>Id.</i> at 11:27-38.</p> <p><i>See also id.</i> at FIGS. 1, 9, 13, Fig. 11, 9:66-10:9.</p>
[18.a] during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;	<p>“A preferred embodiment of the invention <u>accepts television (TV) input streams in</u> a multitude of forms, for example, analog forms such as National Television Standards Committee (NTSC) or PAL broadcast, and <u>digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC).</u> Analog TV streams are converted to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer</p>

¹ All underlining in the claim charts is emphasis added.

'945 Claim Element	Barton (Ex. 1005)
	<p>and manipulation, while pre-formatted MPEG streams are extracted from the digital TV signal and presented in a similar format to encoded analog streams.” Ex. 1005, at 2:4-14.</p> <p>“Referring to FIG. 1, a preferred embodiment of the invention has an Input Section 101, Media Switch 102, and an Output Section 103. <u>The Input Section 101 takes television (TV) input streams in a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC). DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that a TV receiver can disassemble the input stream to find programs in the multiplexed signal.</u>” <i>Id.</i> at 3:30-43.</p> <p>“The Input Section 101 produces MPEG streams. <u>An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds and private data.</u> The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system. . . .” <i>Id.</i> at 3:43-52; <i>see also id.</i> at 4:14-23.</p> <p>“Referring to FIG. 3, <u>the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments.</u> These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. . . . Such separate delivery requires that time sequence information be generated so that the decoders may be</p>

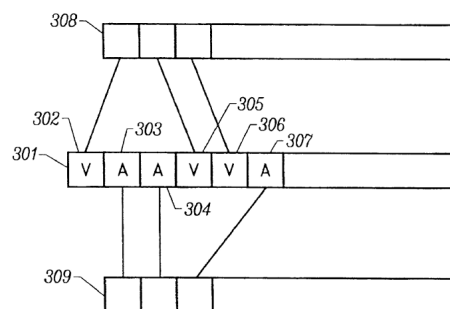


FIG. 3

'945 Claim Element	Barton (Ex. 1005)
	<p>properly synchronized for accurate playback of the signal.” <i>Id.</i> at 4:24-33.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 11, 13.</p>
<p>[18.b] selecting a first program from the multiplexed packetized data stream;</p>	<p>“<u>The Input Section 101 produces MPEG streams.</u> An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds and private data. <u>The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system.</u> Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” <i>Id.</i> at 3:43-52 (emphasis added).</p> <p>“A preferred embodiment of the invention <u>accepts television (TV) input streams in a multitude of forms</u>, for example, analog forms such as National Television Standards Committee (NTSC) or PAL broadcast, and digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC). Analog TV streams are converted to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation, while <u>pre-formatted MPEG streams are extracted from the digital TV signal</u> and presented in a similar format to encoded analog streams.” Ex. 1005, at 2:4-14.</p> <p>“<u>The invention parses the resulting MPEG stream and separates it into its video and audio components. It then stores the components into temporary buffers.</u> Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred. The program logic is notified that an event has occurred and the data is extracted from the buffers.” <i>Id.</i> at 2:15-21.</p> <p>“DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that <u>a TV receiver can disassemble the</u></p>

'945 Claim Element	Barton (Ex. 1005)
	<p><u>input stream to find programs in the multiplexed signal.</u>" <i>Id.</i> at 3:37-43.</p> <p><u>"If a digital TV signal is being processed instead, the MPEG encoder 703 is replaced with an MPEG2 Transport Demultiplexor, and the MPEG audio encoder 704 and VBI decoder 702 are deleted. The demultiplexor multiplexes the extracted audio, video and private data channel streams through the video input Media Switch port."</u> <i>Id.</i> at 6:30-36.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 11, 13.</p>
<p>[18.c] decoding a video portion of the first program for display;</p>	<p><u>"The MPEG stream is sent to a decoder. The decoder converts the MPEG stream into TV output signals and delivers the TV output signals to a TV receiver."</u> Ex. 1005, at 2:29-32.</p> <p><u>"The Output Section 103 takes MPEG streams as input and produces an analog TV signal according to the NTSC, PAL, or other required TV standards. The Output Section 103 contains an MPEG decoder, On-Screen Display (OSD) generator, analog TV encoder and audio logic."</u> <i>Id.</i> at 4:3-7.</p> <p><u>"Referring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal."</u> <i>Id.</i> at 4:24-33.</p> <p><u>"The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717."</u> <i>Id.</i> at 6:63-65.</p> <p><u>"The Media Switch 701 takes in 8-bit data and sends it to the disk, while at the same time extracts another stream of data off of the disk and sends it to the MPEG decoder 715. All of the DMA engines described above can be</u></p>

'945 Claim Element	Barton (Ex. 1005)
	working at the same time.” <i>Id.</i> at 7:5-9. <i>See also id.</i> at FIGS. 1, 7-9, 13.
[18.d] during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a above.
[18.e] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b above.
[18.f] storing the first program;	<p>“The invention parses the resulting MPEG stream and separates it into its <u>video and audio components</u>. It then <u>stores the components into temporary buffers</u>. Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred.” Ex. 1005, at 2:15-19.</p> <p><u>“The video and audio components are stored on a storage device.</u> When the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream.” <i>Id.</i> at 2:26-29; <i>see also id.</i> at 2:33-38.</p> <p>“The invention additionally provides the user with the <u>ability to store selected television broadcast programs</u> while simultaneously watching or reviewing another program and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.” <i>Id.</i> at 3:23-29.</p> <p>“The Media Switch 102 mediates between a microprocessor CPU 106, hard disk or storage device 105, and memory 104. Input streams are converted to an MPEG stream and sent to the Media Switch 102. <u>The Media Switch 102 buffers the MPEG stream into memory.</u> It then performs two operations if the user is watching real time TV: <u>the stream</u> is sent to the Output Section 103 and it is <u>written simultaneously to the hard disk or storage device 105.</u>” <i>Id.</i> at 3:62-4:2.</p>

'945 Claim Element	Barton (Ex. 1005)
	<p><u>“A hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717.”</u> <i>Id.</i> at 6:62-65.</p> <p><u>“The Media Switch 701 takes in 8-bit data and sends it to the disk, while at the same time extracts another stream of data off of the disk and sends it to the MPEG decoder 715. All of the DMA engines described above can be working at the same time.”</u> <i>Id.</i> at 7:5-9.</p> <p><i>See also id.</i> at 9:66-10:9, FIGS. 1, 4-5, 7-11, 13.</p>
[18.g] during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a above.
[18.h] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b above.
[18.i] storing a first program portion of the first program;	<i>See</i> citations to claim 18.f above.
[18.j] providing the first program portion to a second demultiplexer;	<p><u>“The invention parses the resulting MPEG stream and separates it into its video and audio components..”</u> Ex. 1005, at 2:15-16.</p> <p><u>“The input stream flows through a parser 401. The parser 401 parses the stream looking for MPEG distinguished events indicating the start of video, audio or private data segments.</u> For example, when the parser 401 finds a video event, it directs the stream to the video DMA engine 402. The parser 401 buffers up data and DMAs it into the video buffer 410 through the video DMA engine 402. At the same time, the parser 401 directs an event to the event DMA engine 405 which generates an event into the event buffer 413. When the parser 401 sees an audio event, it redirects the byte stream to the audio DMA engine 403 and generates an event into the event buffer 413. Similarly, when the parser 401 sees a private data</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>event, it directs the byte stream to the private data DMA engine 404 and directs an event to the event buffer 413. The Media Switch notifies the program logic via an interrupt mechanism when events are placed in the event buffer.” <i>Id.</i> at 5:3-19.</p> <p><i>See also id.</i> at FIGS. 1-7, 13.</p>
<p>[18.k] selecting at the second demultiplexer a video portion of the first program portion;</p>	<p>“The invention <u>parses the resulting MPEG stream and separates it into its video and audio components</u>. It then stores the components into temporary buffers. Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred. The program logic is notified that an event has occurred and the data is extracted from the buffers.” Ex. 1005, at 2:15-21.</p> <p>“The input stream flows through a parser 401. <u>The parser 401 parses the stream looking for MPEG distinguished events indicating the start of video, audio or private data segments. For example, when the parser 401 finds a video event, it directs the stream to the video DMA engine 402. The parser 401 buffers up data and DMAs it into the video buffer 410 through the video DMA engine 402.</u> At the same time, the parser 401 directs an event to the event DMA engine 405 which generates an event into the event buffer 413. When the parser 401 sees an audio event, it redirects the byte stream to the audio DMA engine 403 and generates an event into the event buffer 413. Similarly, when the parser 401 sees a private data event, it directs the byte stream to the private data DMA engine 404 and directs an event to the event buffer 413. The Media Switch notifies the program logic via an interrupt mechanism when events are placed in the event buffer.” <i>Id.</i> at 5:3-19.</p> <p><i>See also id.</i> at FIGS. 1-7, 13.</p>
<p>[18.l] decoding the video portion of the first program portion for display; and</p>	<p><i>See</i> citations to claim 18.c above.</p>

'945 Claim Element	Barton (Ex. 1005)
<p>[18.m] storing a second program portion of the first program simultaneous to the step of decoding.</p>	<p>“The invention provides a multimedia time warping system. The invention utilizes an easily manipulated, low cost multimedia storage and display system that allows the user to view a television broadcast program with the option of instantly reviewing previous scenes within the program. In addition, the invention <u>allows the user to store selected television broadcast programs while the user is simultaneously watching or reviewing another program.</u>” Ex. 1005, at 1:63-2:3. <i>see also id.</i> at 2:33-38.</p> <p>“The invention additionally provides the user with the ability to <u>store selected television broadcast programs while simultaneously watching or reviewing another program</u> and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.” <i>Id.</i> at 3:23-29.</p> <p>“The Media Switch 102 mediates between a microprocessor CPU 106, hard disk or storage device 105, and memory 104. Input streams are converted to an MPEG stream and sent to the Media Switch 102. The Media Switch 102 buffers the MPEG stream into memory. It then performs two operations <u>if the user is watching real time TV: the stream is sent to the Output Section 103 and it is written simultaneously to the hard disk or storage device 105.</u>” <i>Id.</i> at 3:62-4:2.</p> <p>“With respect to FIG. 2, the invention easily expands to accommodate multiple Input Sections (tuners) 201, 202, 203, 204, each can be tuned to different types of input. Multiple Output Modules (decoders) 206, 207, 208, 209 are added as well. Special effects such as picture in a picture can be implemented with multiple decoders. The <u>Media Switch 205 records one program while the user is watching another.</u> This means that a stream can be extracted off the disk while another stream is being stored onto the disk.” <i>Id.</i> at 4:14-23; <i>see also id.</i> at 4:34-44.</p> <p><u>“The Media Switch 701 takes in 8-bit data and sends it to the disk, while at the same time extracts another stream of data off of the disk and sends it to the MPEG decoder 715.</u> All of the DMA engines described above can be</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>working at the same time.” <i>Id.</i> at 7:5-9 (emphasis added).</p> <p>“The input section of the invention is connected to the casino's video surveillance system. Recorded video is cached and simultaneously output to external VCRs. The user can switch to any video feed and examine (i.e., rewind, play, slow play, fast forward, etc.) a specific segment of the recorded video while the external VCRs are being loaded with the real-time input video.” <i>Id.</i> at 12:27-32.</p> <p><i>See also id.</i> at FIGS. 1, 7-9, 11, 13.</p>
<p>21. A system comprising:</p> <p>[21.a] a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;</p>	<p>“A preferred embodiment of the invention <u>accepts television (TV) input streams in</u> a multitude of forms, for example, analog forms such as National Television Standards Committee (NTSC) or PAL broadcast, and <u>digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC).</u> Analog TV streams are converted to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation, while pre-formatted MPEG streams are extracted from the digital TV signal and presented in a similar format to encoded analog streams.” Ex. 1005, at 2:4-14.</p> <p>“Referring to FIG. 1, a preferred embodiment of the invention has an Input Section 101, Media Switch 102, and an Output Section 103. <u>The Input Section 101 takes television (TV) input streams in</u> a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and <u>digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC).</u> DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. <u>MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that a TV receiver can disassemble the input stream to find programs in the multiplexed signal.</u>” <i>Id.</i> at 3:30-43.</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>“The Input Section 101 produces MPEG streams. <u>An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds</u> and private data. The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system. Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” <i>Id.</i> at 3:43-52; <i>see also id.</i> at 4:14-23.</p> <p>“Referring to FIG. 3, <u>the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments.</u> These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.” <i>Id.</i> at 4:24-33; <i>see also</i> Fig. 3 above.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 11, 13.</p>
<p>[21.b] a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;</p>	<p>“A preferred embodiment of the invention accepts television (TV) input streams in a multitude of forms, Analog TV streams are converted to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation, while <u>pre-formatted MPEG streams are extracted from the digital TV signal</u> and presented in a similar format to encoded analog streams.” Ex. 1005, at 2:4-14.</p> <p>“<u>The invention parses the resulting MPEG stream and separates it into its video and audio components. It then stores the components into temporary buffers.</u> Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred. The program logic is notified that an event has occurred and the data is extracted from the buffers.” <i>Id.</i> at 2:15-21.</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>“Referring to FIG. 1, a preferred embodiment of the invention has an Input Section 101, Media Switch 102, and an Output Section 103. The Input Section 101 takes television (TV) input streams in a multitude of forms, for example, National Television Standards Committee (NTSC) or PAL broadcast, and digital forms such as Digital Satellite System (DSS), Digital Broadcast Services (DBS), or Advanced Television Standards Committee (ATSC). DBS, DSS and ATSC are based on standards called Moving Pictures Experts Group 2 (MPEG2) and MPEG2 Transport. MPEG2 Transport is a standard for formatting the digital data stream from the TV source transmitter so that <u>a TV receiver can disassemble the input stream to find programs in the multiplexed signal.</u>” <i>Id.</i> at 3:30-43.</p> <p>“<u>The Input Section 101 produces MPEG streams.</u> An MPEG2 transport multiplex supports multiple programs in the same broadcast channel, with multiple video and audio feeds and private data. <u>The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it, and feeds it to the rest of the system.</u> Analog TV signals are encoded into a similar MPEG format using separate video and audio encoders, such that the remainder of the system is unaware of how the signal was obtained.” <i>Id.</i> at 3:43-52.</p> <p>“Referring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. <u>These elements must be separated</u> and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.” <i>Id.</i> at 4:24-33.</p> <p>“<u>If a digital TV signal is being processed instead, the MPEG encoder 703 is replaced with an MPEG2 Transport Demultiplexor,</u> and the MPEG audio encoder</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>704 and VBI decoder 702 are deleted. <u>The demultiplexor multiplexes the extracted audio, video and private data channel streams through the video input Media Switch port.</u>” <i>Id.</i> at 6:30-36 (emphasis added).</p> <p>“A hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. <u>The Media Switch 701 outputs streams</u> to an MPEG video decoder 715 and a separate audio decoder 717.” <i>Id.</i> at 6:62-65.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 11, 13.</p>
<p>[21.c] a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;</p>	<p>“The invention parses the resulting MPEG stream and separates it into its video and audio components. <u>It then stores the components into temporary buffers.</u> Events are recorded that indicate the type of component that has been found, where it is located, and when it occurred.” Ex. 1005, at 2:15-19.</p> <p>“<u>The video and audio components are stored on a storage device.</u> When the program is requested for display, the video and audio components are extracted from the storage device and reassembled into an MPEG stream.” <i>Id.</i> at 2:26-29.</p> <p>“The invention additionally provides the user with the ability to <u>store selected television broadcast programs</u> while simultaneously watching or reviewing another program and to view stored programs with at least the following functions: reverse, fast forward, play, pause, index, fast/slow reverse play, and fast/slow play.” <i>Id.</i> at 3:23-29; <i>see also id.</i> at 3:43-52.</p> <p>“The Media Switch 102 mediates between a microprocessor CPU 106, hard disk or storage device 105, and memory 104. Input streams are converted to an MPEG stream and sent to the Media Switch 102. <u>The Media Switch 102 buffers the MPEG stream into memory.</u> It then performs two operations if the user is watching real time TV: <u>the stream is sent to the Output Section 103 and it is written simultaneously to the hard disk or storage device 105.</u>” <i>Id.</i> at 3:62-4:2; <i>see also id.</i> at 4:14-23.</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>“<u>A hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717.</u>” <i>Id.</i> at 6:62-65.</p> <p>“<u>The Media Switch 701 takes in 8-bit data and sends it to the disk, while at the same time extracts another stream of data off of the disk and sends it to the MPEG decoder 715. All of the DMA engines described above can be working at the same time.</u>” <i>Id.</i> at 7:5-9.</p> <p><i>See also id.</i> at FIGS. 1, 4-5, 7-11, 13.</p>
<p>[21.d] a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and</p>	<p>“Referring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304, 307 segments. These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. <u>Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.</u>” Ex. 1005, at 4:24-33.</p> <p>“<u>The Media Switch enables the program logic to associate proper time sequence information with each segment, possibly embedding it directly into the stream. The time sequence information for each segment is called a time stamp.</u> These time stamps are monotonically increasing and start at zero each time the system boots up. This allows the invention to find any particular spot in any particular video segment. . . .” <i>Id.</i> at 4:34-44.</p> <p>“Each stream is stored as a sequence of fixed-size segments enabling fast binary searches because of the <u>uniform time stamping</u>. If the user wants to start in the middle of the program, the system performs a binary search of the stored segments until it finds the appropriate spot, obtaining the desired results with a minimal amount of information. . . .” <i>Id.</i> at 4:45-54.</p> <p>“Referring to FIGS. 4 and 5, the event buffer 413 is filled</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>by the parser 401 with events. <u>Each event 501 in the event buffer has an offset 502, event type 503, and time stamp field 504.</u> The parser 401 provides the type and offset of each event as it is placed into the buffer.” <i>Id.</i> at 5:20-24.</p> <p>“If the stream was produced by encoding an analog signal, it will not contain <u>Program Time Stamp (PTS) values, which are used by the decoders to properly present the resulting output.</u> Thus, the program logic uses the generated time stamp 504 to calculate a simulated PTS for each segment and places that into the logical segment time stamp 607. In the case of a digital TV stream, <u>PTS values are already encoded in the stream. The program logic extracts this information and places it in the logical segment time stamp 607.</u>” <i>Id.</i> at 5:40-47.</p> <p>“This invention utilizes an easily manipulated, low cost, multimedia storage and display system that allows the user to view a television broadcast program with the <u>option of instantly reviewing previous scenes within the program.</u>” <i>Id.</i> at 1:64-67.</p> <p><i>See also id.</i> at FIGS. 4,-7, 9, 11, 5:51-61, 6:36-46.</p>
<p>[21.e] a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.</p>	<p>“The MPEG stream is <u>sent to a decoder. The decoder converts the MPEG stream into TV output signals and delivers the TV output signals to a TV receiver.</u>” Ex. 1005, at 2:29-32.</p> <p>“This invention utilizes an easily manipulated, low cost, multimedia storage and display system that allows the user to view a television broadcast program with the <u>option of instantly reviewing previous scenes within the program.</u>” <i>Id.</i> at 1:64-67.</p> <p>“<u>The Output Section 103 takes MPEG streams as input and produces an analog TV signal according to the NTSC, PAL, or other required TV standards. The Output Section 103 contains an MPEG decoder, On-Screen Display (OSD) generator, analog TV encoder and audio logic.</u>” <i>Id.</i> at 4:3-7; <i>see also id.</i> at 4:14-23, 5:51-61.</p> <p>“Referring to FIG. 3, the incoming MPEG stream 301 has interleaved video 302, 305, 306 and audio 303, 304,</p>

'945 Claim Element	Barton (Ex. 1005)
	<p>307 segments. These elements must be separated and recombined to create separate video 308 and audio 309 streams or buffers. This is necessary because separate decoders are used to convert MPEG elements back into audio or video analog components. <u>Such separate delivery requires that time sequence information be generated so that the decoders may be properly synchronized for accurate playback of the signal.</u>” <i>Id.</i> at 4:24-33.</p> <p><u>“The Media Switch enables the program logic to associate proper time sequence information with each segment, possibly embedding it directly into the stream. The time sequence information for each segment is called a time stamp.</u> These time stamps are monotonically increasing and start at zero each time the system boots up. This allows the invention to find any particular spot in any particular video segment. For example, if the system needs to read five seconds into an incoming contiguous video stream that is being cached, the system simply has to start reading forward into the stream and look for the appropriate time stamp.” <i>Id.</i> at 4:34-44.</p> <p><u>“If the stream was produced by encoding an analog signal, it will not contain Program Time Stamp (PTS) values, which are used by the decoders to properly present the resulting output.</u> Thus, the program logic uses the generated time stamp 504 to calculate a simulated PTS for each segment and places that into the logical segment time stamp 607. In the case of a digital TV stream, <u>PTS values are already encoded in the stream. The program logic extracts this information and places it in the logical segment time stamp 607.</u>” <i>Id.</i> at 5:40-49.</p> <p><u>“A hard disk or storage device 710 is connected to one of the ports of the Media Switch 701. The Media Switch 701 outputs streams to an MPEG video decoder 715 and a separate audio decoder 717.”</u> <i>Id.</i> at 6:62-65; <i>see also id.</i> at 7:5-9.</p> <p><u>“The buffer that is pointed to by the current pointer is handed to the Vela decoder class 916. The Vela decoder class 916 talks to the decoder 921 in the hardware. The</u></p>

'945 Claim Element	Barton (Ex. 1005)
	<p><u>decoder 921 produces a decoded TV signal that is subsequently encoded into an analog TV signal in NTSC, PAL or other analog format.</u> When the Vela decoder class 916 is finished with the buffer it calls releaseEmptyBuf.” <i>Id.</i> at 9:10-16.</p> <p><i>See also id.</i> at FIGS. 1, 7-9, 13.</p>

APPENDIX E

'945 Claim Element	Hatanaka (Ex. 1006)
18. A method comprising: determining a mode of operation;	<p><u>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10.”</u> Ex. 1006, at 3:16-22.</p> <p>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information.” <i>Id.</i> at 3:42-54.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[18.a] during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;	<p>“JP-A-8-98164 discloses a <u>receiving system</u> and a recording/playing back device <u>for receiving/recording a transmitted multiplexed digital signal</u> as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for <u>receiving a transmitted multiplexed digital information signal</u> and for selecting desired information, and recording means for recording the information received by the receiving means.” Ex. 1006, at 1:12-20.</p> <p>“FIG. 2 shows a composition of a <u>transmitted digital broadcasting signal</u>. As shown in a packet composition of FIG. 2(A), the <u>transmission signal has a packet composition</u> of 204 bytes; a 4-byte header 50; a 184-byte data 51 <u>representing information on a video, audio, added</u></p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p><u>data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis.</u> The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator, 55 a payload unit start indicator, 56 a transport priority, 57 a PID indicative of attributes of the packet, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” <i>Id.</i> at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at <u>a contact to input the output from the FEC 7</u> to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The <u>multiplexed signal</u> contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. . . . The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15.</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>inputted to the audio input terminal 27, and converted by the audio A/D converter 29 to a digital audio signal. The audio encoder 31 compresses the digital audio signal, and also <u>outputs this signal</u> to the multiplexer 32, which <u>multiplexes a video stream 42</u> produced by the video encoder 30 <u>and an audio stream 43</u> produced by the audio encoder 31.” <i>Id.</i> at 5:1-14.</p> <p>“As shown in FIGS. 5A-5E, <u>the video stream 42, audio stream 43, other packets, and NULs are multiplexed on a time-divisional basis to form a single signal.</u> <u>The respective video packets VIs 1 (110), 2 (111), etc., on the video stream 42 are the same in content as the VIs 1 (116), 2 (112) etc., on the multiplexed stream 44.</u> <u>Similarly, the respective audio packets AUs 1 (113), 2 (114) etc., of the audio stream 43 are the same in content as the AUs 1 (122), 2 (124) etc., of the multiplexed stream 44.</u> <u>Thus, the multiplexed stream 44 has a stream composition similar to the output of the interface 12 of the digital broadcasting receiver 1.</u> Thus, the recording signal changeover switch 17 selects a contact d and <u>inputs the multiplexed stream 44</u> to the packet control circuit 18 to thereby record/playback the multiplexed stream 44 <u>in the same manner as the digital broadcasting signal.</u>” <i>Id.</i> at 5:54-6:2.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[18.b] selecting a first program from the multiplexed packetized data stream;	<p>“FIG. 2 shows a composition of a transmitted digital broadcasting signal. As shown in a packet composition of FIG. 2(A), the transmission signal has a packet composition of 204 bytes; a 4-byte header 50; a 184-byte data 51 representing information on a video, audio, added data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>on a time divisional basis. The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator, 55 a payload unit start indicator, 56 a transport priority, 57 a PID indicative of attributes of the packet, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” Ex.1006, at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to <u>demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program,</u> and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned.” <i>Id.</i> at 3:16-26.</p> <p>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 <u>is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9.</u> When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. <u>Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information.</u> The signal separated by the interface 12 is inputted to the packet control circuit 18 by</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>selecting a contact c by the recording signal changeover switch 17. As shown in the main data of FIG. 3A, the packet control circuit 18 divides 188-byte packet data into 92-byte packet data A 99 and 96-byte packet data B 100, and adds 4-byte packet header 98 to the packet data A 99. The packet control circuit 18 also produces in the packet header 98 a time stamp, shown in a hatched area 102, which is data on a time when the packet is received.” <i>Id.</i> at 3:42-63; <i>see also id.</i> at 4:16-35.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. <u>Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9</u> or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10; <i>see also id.</i> at 9:6-14.</p>
[18.c] decoding a video portion of the first program for display;	<p>“FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), 2 a recording/playback device, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner, 6 a QPSK demodulator, 7 a forward error correction (FEC) unit for correcting an error involved in the transmission of a signal, 8 a playback changeover switch, 9 a demultiplexer, <u>10 a MPEG decoder</u>, 11 an NTSC encoder” Ex. 1006, at 2:30-50.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. . . . <u>The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.</u>” <i>Id.</i> at 3:16-41; <i>see also id.</i> at 4:30-50.</p> <p>“In playback, the user selects one of the digital and analog broadcasts, the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the <u>MPEG decoder 10 to obtain the video and audio of the desired program.</u>” <i>Id.</i> at 6:47-52; <i>see also id.</i> at 7:21-32.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[18.d] during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a above.
[18.e] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b above.
[18.f] storing the first program;	“JP-A-8-98164 discloses a receiving system and a recording/playing back device for receiving/recording a transmitted multiplexed digital signal as a conventional

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for receiving a transmitted multiplexed digital information signal and for selecting desired information, and <u>recording means for recording the information received by the receiving means.</u>” Ex. 1006, at 1:12-21.</p> <p>“In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), 2 a <u>recording/playback device</u>, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner,” <i>Id.</i> at 2:30-50.</p> <p>“<u>When the received signal is recorded in the recording/playback device 2</u>, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program <u>to be recorded as in the demultiplexer 9.</u> When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. . . .” <i>Id.</i> at 3:42-63.</p> <p>“As shown in FIGS. 5A-5E, the <u>multiplexer 32 temporarily stores the video and audio streams 42 and 43</u>, and outputs them as the video and audio packet streams 45 and 46 at the same transfer rate.” <i>Id.</i> at 5:26-29.</p> <p>“Thus, the <u>digital broadcasting signal and the digital signal to which the analog broadcasting signal is converted are easily recorded</u> simultaneously in a multichannel. If the video and audio streams 42 and 43 alone are multiplexed in a mode in which no broadcasting stream 41 is outputted in the multiplexer 32 of the FIG. 6 device, an operational mode similar to that described in FIG. 1 is obtained. In this case, the clock changeover switch 25 is required to be set at the contact f in the</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>recording operation.” <i>Id.</i> at 6:53-61.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[18.g] during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a above.
[18.h] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b above.
[18.i] storing a first program portion of the first program;	<i>See</i> citations to claim 18.f above.
[18.j] providing the first program portion to a second demultiplexer;	<p>“FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. . . . 9 a demultiplexer, 10 a MPEG decoder, 11 an NTSC encoder, 12 an interface between the devices 1 and 2, 13 a clock recovery unit,” <i>Id.</i> at 2:30-50.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned.” <i>Id.</i> at 3:16-26.</p> <p><u>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. . . .”</u> <i>Id.</i> at 3:42-63.</p> <p><i>See also id.</i> at 7:1-8,7:21-31, FIGS. 1-7, 9, 10.</p>
<p>[18.k] selecting at the second demultiplexer a video portion of the first program portion;</p>	<p>“In playback, the user selects one of the digital and analog broadcasts, <u>the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the MPEG decoder 10 to obtain the video and audio of the desired program.</u>” Ex. 1006, at 6:47-52.</p> <p><u>“. . . Alternatively, the video and audio signals may be selected from separate sources. For example, only the video signal may be selected from the broadcasting stream 41 and the audio signal may be selected from the audio stream 43. Conversely, only the audio signal may be selected from the broadcasting stream 41 and only the video signal may be selected from the audio stream 43.”</u> <i>Id.</i> at 6:61-67.</p> <p><u>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information</u></p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p><u>relating to a program to be recorded as in the demultiplexer 9.</u> When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. . . .” <i>Id.</i> at 3:42-63.</p> <p>“ When a reproduced picture is to be obtained, the playback changeover switch 8 is set at the contact b to thereby send a reproduced packet to the demultiplexer 9. <u>The demultiplexer 9 automatically selects a broadcasting station</u> on the basis of the packet of program information which was selected and converted by the interface 12 when the data was recorded, and outputs only a packet required for the MPEG decoder 10. Video/audio signals are obtained in a manner similar to that in which an output is obtained from a broadcasting signal.” <i>Id.</i> at 4:27-35.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. <u>Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9</u> or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[18.l] decoding the video portion of the first program portion for display; and	<i>See</i> citations to claim 18.c above.
[18.m] storing a second program portion of the	“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7

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<p>first program simultaneous to the step of decoding.</p>	<p>is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9. <u>When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station.</u> Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17. As shown in the main data of FIG. 3A, the packet control circuit 18 divides 188-byte packet data into 92-byte packet data A 99 and 96-byte packet data B 100, and adds 4-byte packet header 98 to the packet data A 99. The packet control circuit 18 also produces in the packet header 98 a time stamp, shown in a hatched area 102, which is data on a time when the packet is received.” Ex. 1006, at 3:42-63.</p> <p>“This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22.</p> <p>“The video A/D converter 28, audio A/D converter 29, video encoder 30, audio encoder 31 and multiplexer 32 may be built either in the recording/playback device 2 or in the digital broadcasting receiver 1. <u>Although not shown, the demultiplexer 9, MPEG decoder 10, NTSC encoder 11, and D/A converter 14 may also be provided in the recording/playback device 2 as well.</u> Thus, even the recording/playback device is capable of providing a reproduced video signal by itself. Of course, the digital broadcasting receiver 1, recording/playback device 2 and encoder 3 may be all integrated in one unit.” <i>Id.</i> at 7:21-32.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may</p>

'945 Claim Element	Hatanaka (Ex. 1006)
	<p>be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>

'945 Claim Element	Hatanaka (Ex. 1006)
<p>21. A system comprising:</p> <p>[21.a] a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;</p>	<p>“JP-A-8-98164 discloses a <u>receiving</u> system and a recording/playing back device <u>for receiving/recording a transmitted multiplexed digital signal</u> as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for <u>receiving a transmitted multiplexed digital information signal</u> and for selecting desired information, and recording means for recording the information received by the receiving means.” Ex. 1006, at 1:12-20.</p> <p>“FIG. 2 shows a composition of a <u>transmitted digital broadcasting signal</u>. As shown in a packet composition of FIG. 2(A), the <u>transmission signal has a packet composition</u> of 204 bytes; a 4-byte header 50; a 184-byte data 51 <u>representing information on a video, audio, added data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis.</u> The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator,</p>

	<p>55 a payload unit start indicator, 56 a transport priority, 57 a PID indicative of attributes of the packet, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” <i>Id.</i> at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at <u>a contact to input the output from the FEC 7</u> to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The <u>multiplexed signal</u> contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. . . .” <i>Id.</i> at 3:16-41.</p> <p>“When the received signal is recorded in the recording/playback device 2, <u>the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program</u> to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” <i>Id.</i> at 3:42-56; <i>see also id.</i> at 4:16-35.</p> <p>“When the analog broadcasting signal is recorded, an analog video signal 150 is inputted to the video input terminal 26 of the encoder 3 of FIG. 1. The video A/D</p>
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	<p>converter 28 converts the analog video signal to a digital video signal. The video encoder 30 compresses the image, using the MPEG 2, etc., as in the compression of the digital broadcasting signal, and <u>outputs the compressed signal</u> to the multiplexer 32. An analog audio signal 151 is inputted to the audio input terminal 27, and converted by the audio A/D converter 29 to a digital audio signal. The audio encoder 31 compresses the digital audio signal, and also <u>outputs this signal</u> to the multiplexer 32, which <u>multiplexes a video stream 42</u> produced by the video encoder 30 <u>and an audio stream 43</u> produced by the audio encoder 31.” <i>Id.</i> at 5:1-14.</p> <p>“As shown in FIGS. 5A-5E, <u>the video stream 42, audio stream 43, other packets, and NULs are multiplexed on a time-divisional basis to form a single signal. The respective video packets VIs 1 (110), 2 (111), etc., on the video stream 42 are the same in content as the VIs 1 (116), 2 (112) etc., on the multiplexed stream 44. Similarly, the respective audio packets AUs 1 (113), 2 (114) etc., of the audio stream 43 are the same in content as the AUs 1 (122), 2 (124) etc., of the multiplexed stream 44. Thus, the multiplexed stream 44 has a stream composition similar to the output of the interface 12 of the digital broadcasting receiver 1. Thus, the recording signal changeover switch 17 selects a contact d and <u>inputs the multiplexed stream 44</u> to the packet control circuit 18 to thereby record/playback the multiplexed stream 44 <u>in the same manner as the digital broadcasting signal.</u>” <i>Id.</i> at 5:54-6:2.</u></p> <p>“This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22. <i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
<p>[21.b] a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an</p>	<p>“FIG. 2 shows a composition of a transmitted digital broadcasting signal. As shown in a packet composition of FIG. 2(A), the transmission signal has a packet composition of 204 bytes; a 4-byte header 50; a 184-byte data 51 representing information on a video, audio, added data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as</p>

<p>output to provide the select packets of data;</p>	<p>an international standard, and a 16-byte parity 52. The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis. The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator, 55 a payload unit start indicator, 56 a transport priority, <u>57 a PID indicative of attributes of the packet</u>, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” Ex. 1006, at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 <u>to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program</u>, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned.” <i>Id.</i> at 3:16-26.</p> <p>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 <u>is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9.</u> When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. <u>Thus, in addition to the packets</u></p>
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	<p>selected by the demultiplexer 9, the interface 12 also <u>selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information</u>. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17. . . .” <i>Id.</i> at 3:42-63.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. <u>Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.</u>” <i>Id.</i> at 9:6-13</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
<p>[21.c] a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;</p>	<p>“JP-A-8-98164 discloses a receiving system and a recording/playing back device for receiving/recording a transmitted multiplexed digital signal as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for receiving a transmitted multiplexed digital information signal and for selecting desired information, and <u>recording means for recording the information received by the receiving means.</u>” Ex. 1006, at 1:12-21.</p> <p>“FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), <u>2 a recording/playback device</u>, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner,” <i>Id.</i> at 2:30-50.</p> <p><u>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 is inputted to the interface 12, which separates packets of</u></p>

	<p>video and audio information and added information relating to a program <u>to be recorded as in the demultiplexer 9</u>. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. . . .” <i>Id.</i> at 3:42-63.</p> <p>“As shown in FIGS. 5A-5E, the <u>multiplexer 32 temporarily stores the video and audio streams 42 and 43, and outputs them as the video and audio packet streams 45 and 46 at the same transfer rate.</u>” <i>Id.</i> at 5:26-29.</p> <p>“Thus, the <u>digital broadcasting signal and the digital signal to which the analog broadcasting signal is converted are easily recorded</u> simultaneously in a multichannel. If the video and audio streams 42 and 43 alone are multiplexed in a mode in which no broadcasting stream 41 is outputted in the multiplexer 32 of the FIG. 6 device, an operational mode similar to that described in FIG. 1 is obtained. In this case, the clock changeover switch 25 is required to be set at the contact f in the recording operation.” <i>Id.</i> at 6:53-61.</p> <p>“<u>While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used.</u> Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p>
[21.d] a first clock recovery module having an input coupled to the	<p>“In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), 2 a recording/playback device, 3 an</p>

<p>first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and</p>	<p>encoder, 4 a digital broadcasting signal input terminal, 5 a tuner, 6 a QPSK demodulator, 7 a forward error correction (FEC) unit for correcting an error involved in the transmission of a signal, 8 a playback changeover switch, 9 a demultiplexer, 10 a MPEG decoder, 11 an NTSC encoder, 12 an interface between the devices 1 and 2, <u>13 a clock recovery unit</u>, 14 a D/A converter, 15 a video output terminal, 16 an audio output terminal, 17 a recorded signal changeover switch, 18 a packet control circuit, 19 a recording/playback data processing, 20 a record amplifier, 21 a playback amplifier, 22 a magnetic tape, 23 a rotary head, 24 a clock generator, 25 a clock changeover switch, 26 a video input terminal, 27 an audio input terminal, 28 a video A/D converter, 29 an audio A/D converter, 30 a video encoder, 31 an audio encoder, 32 a multiplexer, and 47 a digital signal processor.” Ex. 1006, at 2:32-50.</p> <p><u>“The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals.”</u> <i>Id.</i> at 3:22-37.</p> <p><u>“Also, in playback, the data clock 45 used in the MPEG decoder 10 is required to obtain the same frequency as it was compressed in the broadcasting station. To this end, at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, the time stamp 102 is added in the packet control circuit 18. In</u></p>
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	<p> playback, the respective packets are outputted by the packet control circuit 18 in accordance with the time stamps 102 to maintain the time intervals at which the packets are outputted. To this end, <u>clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18.</u>” <i>Id.</i> at 4:36-50. </p> <p> “In recording, as shown in FIGS. 7A-7D, the respective broadcasting (BR), video (VI), and audio (AU) packets of the broadcasting stream 41, video stream 42, and audio stream 43 are multiplexed on a time divisional basis and <u>PMT and PCR are added to the multiplexed packets to constitute a multiplexed stream. In this case, the PAT is already contained in the broadcasting stream 41 (shown by a packet 130 of FIG. 7A), but only contains information on a program contained in the broadcasting stream. Thus, the information should be converted so as to include information on the analog broadcasting. In FIG. 7D, reference numeral 131 denotes a PAT converted by the multiplexer 32. In this case, the packet control circuit 18 uses the data clock 45 produced by the clock recovery unit 13. Thus, the clock changeover switch is set at a contact e, and the video and audio encoders 30 and 31 also use the decoder clock 45. In playback, the clock changeover switch 25 is set at a contact f to use the fixed clock 46.</u>” <i>Id.</i> at 6:28-46; <i>see also id.</i> at 6:3-16. </p> <p> “This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22. <i>See also id.</i> at FIGS. 1-7, 9, 10. </p>
<p> [21.e] a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the </p>	<p> “FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, <u>reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), 2 a recording/playback device, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner, 6 a QPSK demodulator, 7 a forward error</u> </p>

<p>select packets, and an output to provide decoded real-time data.</p>	<p>correction (FEC) unit for correcting an error involved in the transmission of a signal, 8 a playback changeover switch, 9 a demultiplexer, <u>10 a MPEG decoder</u>,” Ex. 1006, at 2:30-50.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and <u>then outputs these packets to the MPEG decoder 10</u>. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. <u>The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.</u>” <i>Id.</i> at 3:16-41.</p> <p>“<u>In reproduction, a signal 153 reproduced by the rotary head 23 is inputted</u> via the playback amplifier 21 to the recording/playback data processing circuit 19, which detects the sync signal 92, signals ID1 (93), ID2 (94), etc., and corrects errors, using the CIP 101, C2P 76, etc., extracts packet data A 99 and packet data B 100, and then sends those data to the packet control circuit 18. <u>The</u></p>
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	<p><u>packet control circuit 18 outputs the respective packets at the same intervals of time as in the recording in accordance with the time stamp 102 added when the data was recorded</u>, and then sends those packets via the interface 12 to the playback changeover switch 8. When a reproduced picture is to be obtained, the playback changeover switch 8 is set at the contact b to thereby send a reproduced packet to the demultiplexer 9. The demultiplexer 9 automatically selects a broadcasting station on the basis of the packet of program information which was selected and converted by the interface 12 when the data was recorded, and <u>outputs only a packet required for the MPEG decoder 10</u>. Video/audio signals are obtained in a manner similar to that in which an output is obtained from a broadcasting signal.” <i>Id.</i> at 4:16-35.</p> <p>“Also, in playback, <u>the data clock 45 used in the MPEG decoder 10 is required to obtain the same frequency as it was compressed in the broadcasting station</u>. To this end, at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, <u>the time stamp 102 is added in the packet control circuit 18</u>. In playback, the respective packets are outputted by the packet control circuit 18 in accordance with the time stamps 102 to maintain the time intervals at which the packets are outputted. To this end, clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18.” <i>Id.</i> at 4:36-50.</p> <p>“<u>In playback, the user selects one of the digital and analog broadcasts, the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the MPEG decoder 10 to obtain the video and audio of the desired program</u>.” <i>Id.</i> at 6:47-52.</p> <p>“This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22.</p>
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	<i>See also id.</i> at FIGS. 1-7, 9, 10.
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APPENDIX F

'945 Claim Element	Hatanaka (Ex. 1006) and O'Connor (Ex. 1007)
18. A method comprising: determining a mode of operation;	<i>See</i> citations to claim 18.preamble in Appendix E.
[18.a] during a first mode of operation: receiving a multiplexed packetized data stream at a first demultiplexer;	<i>See</i> citations to claim 18.a in Appendix E.
[18.b] selecting a first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b in Appendix E.
[18.c] decoding a video portion of the first program for display;	<i>See</i> citations to claim 18.c in Appendix E.
[18.d] during a second mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a in Appendix E.
[18.e] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b in Appendix E.
[18.f] storing the first program;	<i>See</i> citations to claim 18.f in Appendix E.
[18.g] during a third mode of operation: receiving the multiplexed packetized data stream at the first demultiplexer;	<i>See</i> citations to claim 18.a in Appendix E.
[18.h] selecting the first program from the multiplexed packetized data stream;	<i>See</i> citations to claim 18.b in Appendix E.
[18.i] storing a first program portion of the first program;	<i>See</i> citations to claim 18.f in Appendix E.

'945 Claim Element	Hatanaka (Ex. 1006) and O'Connor (Ex. 1007)
[18.j] providing the first program portion to a second demultiplexer;	<i>See</i> citations to claim 18.j in Appendix E.
[18.k] selecting at the second demultiplexer a video portion of the first program portion;	<i>See</i> citations to claim 18.k in Appendix E.
[18.l] decoding the video portion of the first program portion for display; and	<i>See</i> citations to claim 18.c in Appendix E.
[18.m] storing a second program portion of the first program simultaneous to the step of decoding.	<p><i>See</i> citations to claim 18.m in Appendix E.</p> <p>“FIG. 3 shows an embodiment of a method for <u>retrieving a portion of the video stream from the random access storage unit while continuing to record the incoming video stream</u> in accordance with the invention, although the invention is not restricted to this embodiment. In the disclosed embodiment, the substantially <u>simultaneous recording and playback of the video stream is performed by multiplexing or alternately storing the video stream to the random access storage unit and reading of the video stream from the random access storage unit</u>. The multiplexed or alternated stores and reads may occur quickly enough that the user does not notice an appreciable delay in the playback of the video stream, and the incoming video stream is not lost, e.g., <u>all of the video stream is recorded</u>. Thus, the <u>record and playback are substantially simultaneous from the user's point of view</u>. Ex. 1007, at 4:9-24.</p> <p>“A user may initiate a playback cycle following block 506. For example, this may occur when the <u>user wishes to re-view a video clip that he just saw</u>. In one embodiment, the user stops recording to the temporary buffer and plays back the last portion of the temporary buffer. However, it <u>may be more desirable to the user to be able to continue recording as shown at block 508</u>. A record</p>

'945 Claim Element	Hatanaka (Ex. 1006) and O'Connor (Ex. 1007)
	<p>and playback cycle (as described with respect to FIG. 2) is started, in which the <u>incoming video stream is recorded while the user re-views the last portion of the temporary buffer</u>. In this manner, <u>after re-viewing the desired video clip, the user can resume sequentially watching the video stream from the current point of the incoming video for substantially simultaneous playback and record.</u>" <i>Id.</i> at 5:19-33.</p> <p>"Using these techniques, the storage device is provided with enough time, through the operation of the buffers, <u>to write the incoming video while supplying enough data simultaneously to the output display</u>. Since the memory is used to make sure no content is dropped at the input end and the display is never starved at the output end, continuous display can be provided without losing information." <i>Id.</i> at 11:14-20.</p> <p><u>"Timeshifting by substantially simultaneously recording and playing back a data stream enables the following type of benefits/features for an end-user</u>. While watching the season premiere of a television show, the viewer can literally "<u>pause</u>" the program in order to get up and answer the phone or get a snack from the refrigerator. After the interruption, the viewer can <u>resume watching again without having missed anything</u>. If the <u>viewer came home 15 minutes late for the show but had started recording the program from the beginning</u>, the viewer can begin watching right away instead of waiting for the show to be over and then rewinding the cassette tape. Also the viewer can <u>replay scenes during a "live" broadcast</u> (e.g. season premiere of a show or sporting event) in case the viewer missed a line or an exciting play. In addition, while watching a sports event the user can <u>rewind</u> back to a controversial play, replay the play in slow motion, and stop at the exact instance when the catch was made. To get a better view, the viewer can zoom in on a portion of the screen and apply image</p>

'945 Claim Element	Hatanaka (Ex. 1006) and O'Connor (Ex. 1007)
	<p>sharpening filters to magnify one part of the screen. <i>Id.</i> at 11:58-12:10.</p> <p>“Because there is no need to decompress the data, the <u>speed of storage may be greatly increased</u> and the computational complexity may be reduced. This <u>facilitates a system which substantially simultaneously records and plays back a data stream</u>, of the type described herein, since large amounts of data may be stored at one time and the resources of the system may be taxed in undertaking this process. <i>Id.</i> at 16:3-10.</p>

APPENDIX G

'945 Claim Element	Fujinami (Ex. 1008)
<p>21. A system comprising:</p> <p>[21.a] a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;</p>	<p>“FIG. 5 is a block diagram showing an exemplary constitution of a conventional data demultiplexer known heretofore. In this diagram, a drive 1 reproduces the data recorded on an optical disk incorporated therein. <u>On this optical disk, there are recorded both video data and audio data in a time-division multiplex form.</u> The reproduced data outputted from the drive 1 is supplied to a demodulator 2 so as to be demodulated. An ECC circuit 3 detects and corrects any error in the data outputted from the demodulator 2 and supplies the processed data to a ring buffer 4. <u>Then the ring buffer 4 stores a predetermined amount of the supplied data therein and subsequently outputs the data</u> to a data demultiplexer 5.” Ex. 1008, at1:9-21.</p> <p><u>“The format of the data supplied to the data demultiplexer 5 is so standardized as shown in FIG. 6 for example. This format is prescribed as a multiplex bit stream in the MPEG (ISO11172). As shown in FIG. 6, a multiplex bit stream is composed of one or more packs (PACKS), each of which is composed of one or more packets (PACKETS). A pack header (PACK HEADER) is disposed at the top of each pack and has a pack start code (PACK START CODE) indicating a start point of the pack, and also SCR and MUX__RATE. This SCR indicates the time when the last byte is inputted to the data demultiplexer 5 (the time when demultiplexing is started), and the MUX__RATE signifies a transfer rate.”</u> <i>Id.</i> at 1:28-39.</p>
<p>[21.b] a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;</p>	<p><u>“The data demultiplexer 5 has a data separation circuit 21 which demultiplexes the data supplied from the ring buffer 4 to thereby separate the same into video data and audio data, and further into timing data such as SCR (system clock reference) and DTS (decoding time stamp) inclusive of DTSV for the video data and DTSA for the audio data.”</u> Ex. 1008, at 1:22-27.</p> <p><u>“The data separation circuit 21 is controlled by the control circuit 28 and separates the output data of the ring buffer 4 into video data and audio data, which are</u></p>

'945 Claim Element	Fujinami (Ex. 1008)
	<p>then supplied to the video code buffer 6 and the audio code buffer 8, respectively. The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.” <i>Id.</i> at 2:28-35.</p> <p>“<u>The format of the data supplied to the data demultiplexer 5 is so standardized as shown in FIG. 6 for example. This format is prescribed as a multiplex bit stream in the MPEG (ISO11172).</u> As shown in FIG. 6, a multiplex bit stream is composed of one or more packs (PACKS), each of which is composed of one or more packets (PACKETS). <u>A pack header (PACK HEADER) is disposed at the top of each pack and has a pack start code (PACK START CODE) indicating a start point of the pack,</u> and also SCR and MUX__RATE. This SCR indicates the time when the last byte is inputted to the data demultiplexer 5 (the time when demultiplexing is started), and the MUX__RATE signifies a transfer rate.” <i>Id.</i> at 1:28-39; <i>see also id.</i> at 1:40-52.</p> <p>“According to a first aspect of the present invention, there is provided <u>a data demultiplexer for separating multiplex data which includes at least first coded data such as video data,</u> first timing data indicative of a decoding start time of the first coded data, and second timing data indicative of a system clock reference time. <i>Id.</i> at 4:56-61.</p> <p>“The <u>data demultiplexer</u> further comprises a system time clock generation means for generating a system time clock signal by setting an initial value thereof on the basis of the first timing data and then incrementing predetermined clock pulses; and a means for generating a first decoding start signal by comparing the first timing data with the system time clock signal.” <i>Id.</i> at 5:4-10; <i>see also id.</i> at 5:11-16.</p>

'945 Claim Element	Fujinami (Ex. 1008)
	<p style="text-align: center;">FIG. 1(A)</p> <p style="text-align: center;">FIG. 1(B)</p> <p><i>See also id. at 5A, and 5B.</i></p>
<p>[21.c] a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;</p>	<p>“The <u>video data stored in the video code buffer 6</u> is read out therefrom and is supplied to a video decoder 7. Then, the video data is decoded to become a video signal, which is subsequently outputted to an unshown circuit. To the video decoder 7, there is also supplied a video decoding start signal which is outputted from the comparator 23.” Ex. 1008, at 2:6-11.</p> <p>“The <u>data separation circuit 21</u> is controlled by the control circuit 28 and <u>separates the output data of the ring buffer 4 into video data and audio data, which are then supplied to the video code buffer 6 and the audio code buffer 8, respectively.</u> The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.” <i>Id.</i> at 2:28-35.</p> <p><i>See id.</i> at FIGS. 1A-1B above and FIGS. 5A and 5B.</p>
<p>[21.d] a first clock recovery module having an input coupled to the first input node, and an output, wherein the first</p>	<p>“The data demultiplexer 5 has a data separation circuit 21 <u>which demultiplexes the data supplied from the ring buffer 4 to thereby separate the same into video data and audio data, and further into timing data such as SCR (system clock reference) and DTS (decoding time stamp)</u></p>

'945 Claim Element	Fujinami (Ex. 1008)
<p>clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and</p>	<p><u>inclusive of DTSV for the video data and DTSA for the audio data.</u>" Ex. 1008, at 1:22-27.</p> <p>"The data separation circuit 21 is controlled by the control circuit 28 and separates the output data of the ring buffer 4 into video data and audio data, which are then supplied to the video code buffer 6 and the audio code buffer 8, respectively. <u>The circuit 21 further separates the timing data into SCR, DTSV and DTSA, which are supplied respectively to the STC register 26, the DTSV register 22 and the DTSA register 24 and then are stored therein.</u>" <i>Id.</i> at 2:28-35.</p> <p>"<u>The STC register 26 having stored the timing data SCR therein counts the clock pulses outputted from the clock generator 27 and increments the storage value in response to the clock pulses. The storage value of the STC register 26 is supplied as a system time clock (STC) signal to the comparators 23 and 25.</u>" <i>Id.</i> at 2:36-41; <i>see also id.</i> at 2:42-46, 2:47-52.</p> <p>"<u>The reference timing data SCR corresponds to the time when demultiplexing is started after supply of the data from the ring buffer 4 to the data demultiplexer 5. More specifically, it corresponds to a time t1 in the timing chart of FIG. 7. Therefore the STC register 26 outputs the time data (current time) from the time t1 to one input terminal of each of the comparators 23 and 25.</u>" <i>Id.</i> at 2:53-59.</p> <p>"According to a first aspect of the present invention, there is provided a <u>data demultiplexer for separating multiplex data which includes at least first coded data such as video data, first timing data indicative of a decoding start time of the first coded data, and second timing data indicative of a system clock reference time. The demultiplexer comprises a separation means for separating the multiplex data into the first coded data, the first timing data and the second timing data; and a comparison means for comparing the time, which is indicated by the first timing data separated by the separation means, with the time indicated by the second timing data; wherein, when the time indicated by the second timing data is temporally anterior to the time</u></p>

'945 Claim Element	Fujinami (Ex. 1008)
	<p>indicated by the first timing data, the multiplex data is supplied at the maximum transfer rate to the separation means. <u>The data demultiplexer further comprises a system time clock generation means for generating a system time clock signal by setting an initial value thereof on the basis of the first timing data and then incrementing predetermined clock pulses; and a means for generating a first decoding start signal by comparing the first timing data with the system time clock signal.</u> <u>The multiplex data further includes second coded data such as audio data, and third timing data indicative of a decoding start time of the second coded data. The demultiplexer further comprises a means for generating a second decoding start signal by comparing the third timing data with the system time clock signal.</u>" <i>Id.</i> at 4:56-5:16.</p> <p><i>See id.</i> at FIGS. 1A-1B above and FIGS. 5A and 5B.</p>
<p>[21.e] a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.</p>	<p><u>"The video data stored in the video code buffer 6 is read out therefrom and is supplied to a video decoder 7. Then, the video data is decoded to become a video signal, which is subsequently outputted to an unshown circuit. To the video decoder 7, there is also supplied a video decoding start signal which is outputted from the comparator 23."</u> Ex. 1008, at 2:6-11.</p> <p><u>"Similarly, the data outputted from the audio code buffer 8 is supplied to an audio decoder 9 so as to be decoded. To the audio decoder 9, there is also supplied the output of the comparator 25 as an audio decoding start signal."</u> <i>Id.</i> at 2:12-15.</p> <p>"The DTSV register 22 supplies the video timing data DTSV, which indicates the decoding start time of the video decoder 7, to the other input terminal of the comparator 23. When the current time outputted from the STC register 26 has become coincident with the decoding start time outputted from the DTSV register 22 (i.e., at a time t2 in FIG. 7), the comparator 23 outputs a video decoding start signal to the video decoder 7. In response to the video decoding start signal thus received,</p>

'945 Claim Element	Fujinami (Ex. 1008)
	<p>the video decoder 7 reads out one frame of the video data written in the video code buffer 6 and then starts its decoding.” <i>Id.</i> at 4:28-38.</p> <p><i>See id.</i> at FIGS. 1A-1B above and FIGS. 5A and 5B.</p>