

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.
Petitioner

v.

ATI TECHNOLOGIES ULC
Patent Owner

Case: IPR2015-01620

Patent 7,095,945

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,095,945**

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PETITIONER’S EXHIBIT LIST

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Prosecution History of U.S. Patent No. 7,095,945	1002
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Declaration of Daniel Schonfeld, Ph.D. (“Schonfeld Decl.”)	1004
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U.S. Patent No. 6,591,058 (“O’Connor”)	1007
U.S. Patent No. 5,521,922 (“Fujinami”)	1008
U.S. Patent No. 5,517,250 (“Hoogenboom”)	1009
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Suppl. Declaration of Daniel Schonfeld, Ph.D. (“Suppl. Schonfeld Decl.”)	1011

Patent No. 7,095,945

Petition for *Inter Partes* Review

Pursuant to 35 U.S.C. §311, Petitioner hereby respectfully requests *inter partes* review of claim 21 of Ex. 1001, U.S. Patent No. 7,095,945 (“the ’945 Patent”) which issued on August 22, 2006. The challenged claims are unpatentable under 35 U.S.C. §§102 and 103 over the prior art identified and applied in this Petition.

I. MANDATORY NOTICES

Pursuant to 37 C.F.R. §42.8, Petitioner provides the following mandatory disclosures:

A. Real Parties-In-Interest. LG Electronics U.S.A., Inc. and LG Electronics MobilComm U.S.A. are real parties-in-interest with Petitioner, LG Electronics, Inc.

B. Related Matters. Pursuant to 37 C.F.R. §42.8(b)(2), Petitioner submits that the ’945 Patent is the subject of a patent infringement lawsuit brought by Advanced Micro Devices, Inc. in the Northern District of California: *Advanced Micro Devices, Inc., et al., v. LG Electronics, Inc., et al.*, Case No. 3:14-cv-01010. Petitioner also submits that the ’945 Patent is the subject of *inter partes* review case number IPR2015-00321.

C. Lead and Back-up Counsel.

Petitioner provides the following designation of counsel:

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D. Service Information. Pursuant to 37 C.F.R. §42.8(b)(4), Petitioner identifies the following service information: Please direct all correspondence regarding this proceeding to lead counsel at the address identified above. Petitioner consents to electronic service by email: rpluta@mayerbrown.com and astreff@mayerbrown.com, with a courtesy copy to AMDIPR@mayerbrown.com.

II. PAYMENT OF FEES

Pursuant to 37 C.F.R. §42.103, \$23,000 is being paid at the time of filing this petition, charged to Deposit Account **130019**. Should any further fees be required by the present Petition, the Patent Trial and Appeal Board (“the Board”) is hereby authorized to charge the above referenced Deposit Account.

III. STANDING

Pursuant to 37 C.F.R. §42.104(a), Petitioner certifies that the patent sought for review, the ’945 Patent, is available for *inter partes* review. IPR2015-00321 was instituted on June 26, 2015. A motion to join IPR2015-00321 is filed concurrently with this Petition and within one month of institution of IPR2015-

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00321 and thus the time periods set forth in 37 C.F.R. §42.101(b) do not apply to this Petition. Petitioner is not barred or estopped from requesting an *inter partes* review of the patent.

IV. REQUEST FOR *INTER PARTES* REVIEW OF CLAIM 21 OF THE '945 PATENT

Pursuant to 37 C.F.R. §42.104(b), Petitioner requests that the Board find unpatentable claim 21 of the '945 Patent. Such relief is justified as the alleged invention of the '945 Patent was described by others prior to the effective filing date of the '945 Patent.

A. Technology Background

Time shifting for viewing live programs at a later time was known at the time of the alleged invention of the '945 patent. Ex. 1001, at 1:12-13. Generally, time shifting allows a viewer to step away from a TV program and watch the TV program at a different time, without missing any part of the program. Ex. 1004, Declaration of Daniel Schonfeld, Ph.D. (“Schonfeld Decl.”), ¶¶56-57. The location within the multimedia presentation where the data stream has been paused is typically identified by the time when the request has been made, and must be recorded in order to display the multimedia data stream from the correct location once the viewer wishes to resume the presentation. *See id* at ¶58. The received multimedia data stream typically includes timing information necessary for various tasks such as synchronization of distinct data streams, *e.g.*, simultaneous

presentation of audio and video streams. *See id.* at ¶59. The time when the multimedia data stream has been paused must be compared to timing information embedded in the multimedia data stream to determine the location where the stream has been paused. *See id.* Once the viewer has indicated that he or she would like to resume the presentation of the multimedia stream, the recorded data must be sent to the decoder at the proper rate. *See id.* at ¶60. In order to ensure that the timing information generated by the receiver and the embedded timing information are compatible, they must be compared to the same clock. *See id.* at ¶61. When recording the multimedia data stream, it is essential to also record the timing information embedded in the received data stream so that the location of the pause request and the rate at which the data should be sent to the decoder can be determined. *See id.* at ¶62. The multimedia data stream is typically received and stored in coded form. *See id.* at ¶63. When a viewer wishes to pause the program, the timing information embedded as part of the coded multimedia data stream received must be recorded. *See id.* at ¶64. This timing information is essential for proper decoding of the coded multimedia stream, and also used to determine the rate at which the coded multimedia stream must be sent to the decoder. *See id.* at ¶64.

B. The Alleged Invention Of The '945 Patent

The '945 Patent relates “time shifting of video data, and more specifically to time shifting of digital video data.” Ex. 1001, at 1:6-8. As the '945 Patent acknowledges, “[s]ystems for time shifting a viewed program are known in the industry. For example, if a viewer is interrupted by a phone call during a television program, the program can be recorded for a few minutes and then played back from the point of interruption while addition video information is continually recorded.” *Id.* at 1:12-17. Also, the '945 Patent acknowledges that “[o]ne method of transporting large amounts of various types of transport stream data is to use a multiplexed packetized data stream capable of carrying real-time multimedia programs.” *Id.* at 1:46-49. The purported advantage of the alleged invention described in the '945 Patent relates to “a method and apparatus for efficient time shifting of multiplexed packetized data streams, such as a packet stream.” Ex. 1001, at 2:43-45.

The '945 Patent discloses three time shifting modes: a receive-only mode, a continuous mode, and a part-time mode. In the receive-only mode, or live play, a digital transport stream receiver (DTSR) receives a live broadcast and demultiplexes one program of a plurality of programs available in the live broadcast stream. *Id.* at 5:7-35. In continuous time shifting mode, storage mode, time shifting is selected by the viewer to store part or all of a program for later

viewing after a short or long intermission. *Id.* at 5:36-49. During continuous time shifting mode, a selected program from a given multiplex is received and stored on a hard disk, or other storage media, in the form of full transport stream packets. *Id.* In part-time shifting mode, or store and play mode, when selected by the viewer, allows for replay of a time shifted program or fast forward (FF) replay of a time shifted program at user defined FF speed. *Id.* at 6:13-27. These modes of operation are limitations of claim 21.

V. CLAIM CONSTRUCTION

A claim subject to *inter partes* review is given its “broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. §42.100(b). This means that the words of the claim are given their plain meaning from the perspective of one of ordinary skill in the art unless that meaning is inconsistent with the specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). Petitioner submits, for the purposes of *inter partes* review only, that the claim terms are presumed to take on their broadest reasonable interpretation in light of the specification of the '945 Patent.¹

¹ *Inter partes* review is limited to evaluating invalidity issues arising from the consideration of certain prior-art issues, *i.e.*, 35 U.S.C. §§ 102-103; and, therefore, excludes consideration of indefiniteness, enablement, and numerous other grounds for invalidity. Petitioner thus files this *inter partes* review without

VI. SUMMARY OF PRIOR ART TO THE '945 PATENT FORMING THE BASIS FOR THIS PETITION

A. U.S. Patent No. 6,397,000 (“Hatanaka”) (Ex. 1006)

Hatanaka discloses “digital signal recording devices, digital signal recording/playback devices, and digital signal receiving/recording/playback devices, for receiving/recording/playing back a digital signal.” Ex. 1006, at 1:8-11. Hatanaka qualifies as prior art under 35 U.S.C. §102(e), because Hatanaka was filed on June 5, 1998, before the November 6, 2000 filing date of the '945 Patent. Hatanaka was not cited or considered during the prosecution of the application that led to the '945 Patent.

B. U.S. Patent No. 5,517,250 (“Hoogenboom”) (Ex. 1009)

Hoogenboom discloses a system for efficiently acquiring data, such as video data, from a packetized data stream. Ex. 1009, at 1:7-10. Hoogenboom qualifies as prior art under 35 U.S.C. §102(b), because Hoogenboom issued as a patent on May 14, 1996, more than one year before the November 6, 2000 filing date of the '945 Patent. Hoogenboom was not cited or considered during the prosecution of the application that led to the '945 Patent.

C. U.S. Patent No. 6,275,507 (“Anderson”) (Ex. 1010)

prejudice to its right to challenge the validity of the subject patent in other forums and proceedings on any and all bases recognized by law and equity.

Anderson discloses a system for “[t]able filtering before memory storage by the transport demultiplexor [to] reduce[] the load on the application processor by filtering table sections before sending them to DRAM or other memory. . . .” Ex. 1010, at 11:57-65. Anderson qualifies as prior art under 35 U.S.C. §102(e), because Anderson was filed on September 26, 1997, before the November 6, 2000 filing date of the ’945 Patent. Anderson was not cited or considered during the prosecution of the application that led to the ’945 Patent.

VII. GROUNDS FOR UNPATENTABILITY OF EACH CLAIM

In light of the disclosures detailed below, the ’945 Patent is unpatentable for at least the reasons summarized in the chart below and discussed in more detail herein.

Ground #	Ground	Prior art	Exhibit(s) #	Claims
1	103(a)	Hatanaka and Hoogenboom	1006 and 1009	21
2	103(a)	Hatanaka and Anderson	1006 and 1010	21

Grounds 1 and 2 are not redundant with the grounds considered in IPR2015-00321. In IPR2015-00321, claim 21 was challenged based on two 102(e) grounds and one single reference 103 ground. Here, claim 21 is challenged based on a combination of Hatanaka with Hoogenboom and Hatanaka with Anderson. While the Board previously considered Hatanaka, it did not previously consider Hoogenboom or Anderson (or Hatanaka in combination with either reference), which disclose generating timing information based on packetized data streams

prior to storing the data signal in a storage device in a system similar to that of Hatanaka.

Additionally, Ground 2 is not redundant of Ground 1. While both Hoogenboom and Anderson disclose generating a clock prior to storage, as discussed below, the reason for doing so is different. As explained below, the process of generating the clock in Hoogenboom (*supra* Section A.2) is different than the process disclosed in Anderson (*supra* Section B.2). Also, the benefit resulting from generating the clock prior to storage disclosed in Hoogenboom (efficiently acquiring data out of storage) is different from the benefit disclosed in Anderson (reducing the load on the processor). Thus, Grounds 1 and 2 are also not redundant.

For the reasons discussed below, Petitioner has a reasonable likelihood of prevailing on claim 21 based on Grounds 1 and 2.

A. Ground 1: Claim 21 Is Unpatentable Under 35 U.S.C. §103(a) As Being Obvious Over Hatanaka In View Of Hoogenboom

1. Disclosure In Hatanaka

Hatanaka is directed to a “digital signal recording devices, digital signal recording/playback devices, and digital signal receiving/recording/playback devices, for receiving/recording/playing back a digital signal.” Ex. 1006, at 1:8-11. Hatanaka discloses a digital recording device with a first and second demultiplexer, a decoder, a clock recovery module, and a storage unit. Hatanaka

discloses first demultiplexer labeled as interface 12, second demultiplexer labeled as demultiplexer 9 (highlighted in red), MPEG decoder 10 (highlighted in blue), a clock recovery circuit 13 and clock generator 24 (highlighted in green), and a storage device (highlighted in purple). *See* Ex. 1006, at 3:16-56, 9:6-13. This can be seen in annotated Fig. 6 below.

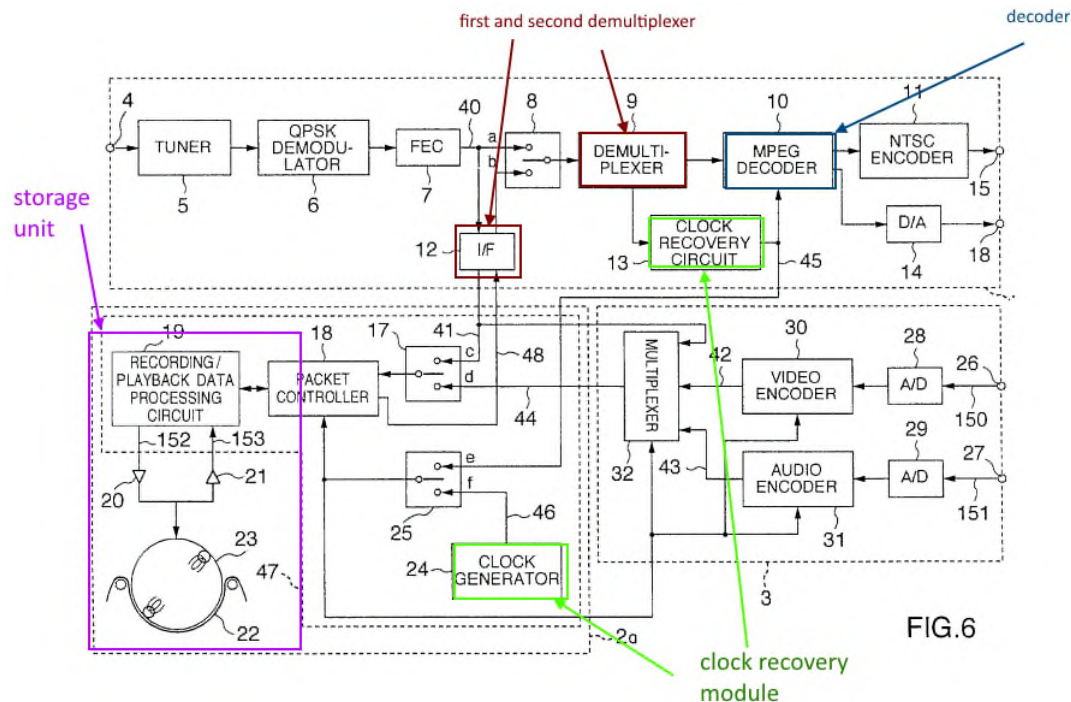


Fig. 6 and the descriptions in Hatanaka disclose the system of claim 21. First, as required by the first limitation of claim 21, Hatanaka discloses receiving a multiplexed packetized data stream that carries real-time multimedia programs. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶95-96. Specifically, Hatanaka discloses data streams in packet form that are received in a multiplexing manner. Hatanaka explains that “FIG. 2 shows a composition of a **transmitted digital broadcasting**

signal. As shown in a packet composition of FIG. 2(A), **the transmission signal has a packet composition** of 204 bytes; a 4-byte header 50; a 184-byte data 51 **representing information on a video, audio, added data, etc.,** compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. **The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B).** Generally, **not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis. . . .**” *Id.* at 2:51-3:6 (emphasis added). Here, Hatanaka explains that the transmitted signal is a multiplexed packet composition carrying real time information. Hatanaka also explains that receiving a multiplexed packetized data stream was well known in the prior art. Ex. 1006, at 1:12-20; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶96.

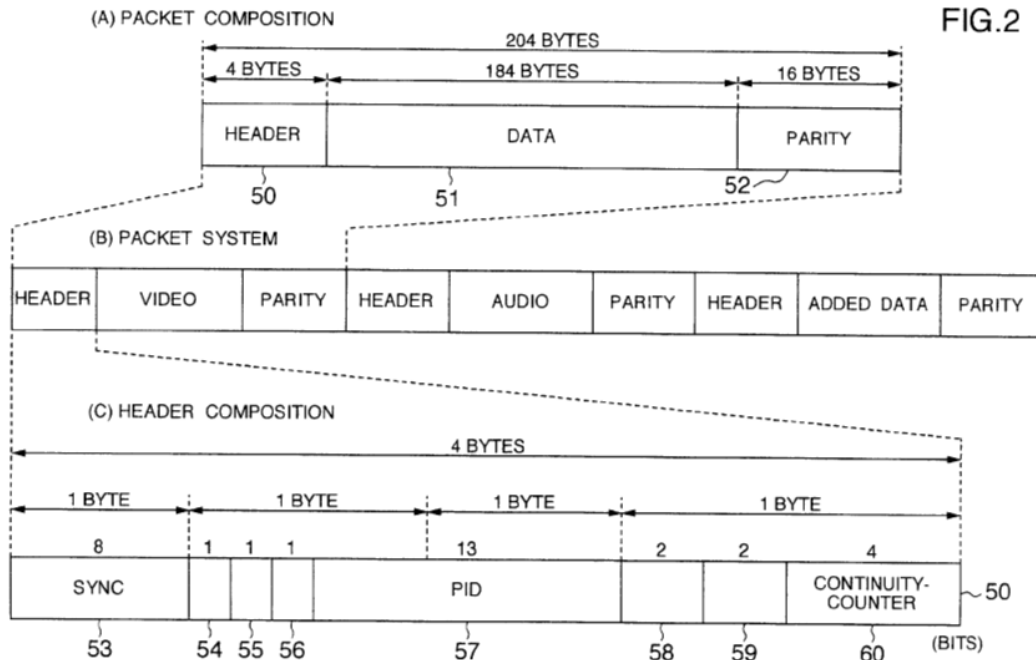
Also with respect to the first limitation of claim 21, Hatanaka discloses a first input node to receive the multiplexed packetized data stream. *See* Schonfeld Decl., at ¶¶97-98. Hatanaka explains that “[w]**hen the broadcasting signal is outputted from the present device,** the playback changeover switch 8 is set at a contact to **input the output from the FEC 7 to demultiplexer 9,** which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these

packets to the MPEG decoder 10. . . .” *Id.* at 3:16-41 (emphasis added); *see also* 3:42-56, 4:16-35. Thus, Hatanaka discloses “[a] system comprising: a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs,” as required by claim 21.

Hatanaka discloses the second limitation of claim 21: “a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data.” Dr. Schonfeld explains that Hatanaka describes the use of demultiplexer 9 coupled to the input from FEC 7 to select packets of data using PID 57 and an output to provide the select packets of data. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶101. Hatanaka discloses that “[w]hen the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to **input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets** to the MPEG decoder 10. . . .” *Id.* at 3:16-26 (emphasis added). Thus, in Hatanaka, the first transport stream demultiplexor is demultiplexer 9.

Hatanaka also discloses the first input node select packets of data having a predefined packet identifier. FIG. 2 shows that the packets of data have a packet

header 50 that includes predefined identifying information, PID 57.



Similarly, Hatanaka discloses interface 12 coupled to the input from FEC 7 to select packets of data and an output to provide the select packets of data. *See id.* at 3:42-56; *see also id.* at 4:16-35; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶103. Hatanaka explains that “[a]lthough not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. **Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.**” *Id.* at 9:6-13 (emphasis added).

Regarding the third limitation of claim 21, Hatanaka discloses “a storage

device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets.” Hatanaka “recording/playback device 2,” and which can be seen in Fig. 1 above. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶106-109. The storage device of Hatanaka is the “recording/playback device 2.” Hatanaka explains that “recording/playback device 2,” is shown in Fig. 1: “[i]n FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), **2 a recording/playback device**, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner,” *Id.* at 2:30-50 (emphasis added); *see also id.* at FIGS. 1, 6, 9 and 10.

The storage device of Hatanaka also has a data port coupled to the output of the first transport stream demultiplexer (demultiplexer 9) as illustrated in FIG. 1 above. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶108. Hatanaka explains that recording/playback device 2 has a data port coupled to the output of the demultiplexer 9 to receive the select packets and store the select packets. *See id.* at 3:42-56; *see also id.* at 4:16-35. This is explained by Hatanaka as follows:

While in the above the **magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used**. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7.

Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.

Id. at 9:6-13 (emphasis added).

Hatanaka also discloses “a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.” Hatanaka discloses a clock recovery unit 13 and packet controller 18. *See id.* at 2:41, *see also id.* FIGS. 1 and 6; *Id.* at 3:16-41 (emphasis added). These can be seen in annotated Fig. 6 above. Together clock recovery unit 13 and packet controller 18 are the clock recovery module. *See id.* at 4:41-50, 6:28-45.

In Hatanaka, the packet controller 18 produces the time stamp through the decoder clock 45. The decoder 45 is produced by the clock recovery unit 13. *Id.* at 3:22-37. In the recovery mode of Hatanaka, decoding of the stored data must be performed at the same rate used for encoding by the broadcasting station. Ex. 1006, at 4:36-38, 4:41-42. In the playback mode, the stored data is sent to the decoder in accordance with the time stamps 102. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶112-114. According to Dr. Schonfeld, this ensures that the time intervals between the embedded PCR is maintained and that the data clock 45 that

was recovered from the stored data will be the same as the data clock 45 originally recovered from the multiplexed signal. Ex. 1006, at 4:42-45; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶114. Dr. Schonfeld explains that this process discloses that clock recovery unit 13 uses embedded PCR in the received multiplexed signal to recover data clock 45, which is then used to generate time stamps 102. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶114. The time stamps 102 are then added along with the encoded data to the packet control circuit 18 for storage, and thus clearly discloses that data data clock 45 is recovered before the encoded data is stored in the storage device. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶114.

Hatanaka also makes it clear that the generation of a clock at the output is based upon received timing information transmitted in packets of the multiplexed packetized data stream. As noted above, Hatanaka discloses predefined packet identifier, PID 57. Hatanaka explains that “at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, the time stamp 102 is added in the packet control circuit 18.” *Id.* at 4:38-42; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶115-116. Hatanaka further discloses that:

In recording, as shown in FIGS. 7A-7D, the respective broadcasting (BR), video (VI), and audio (AU) packets of the broadcasting stream 41, video stream 42, and audio stream 43 are multiplexed on a time divisional basis and **PMT and PCR are added to the multiplexed**

packets to constitute a multiplexed stream. In this case, the PAT is already contained in the broadcasting stream 41 (shown by a packet 130 of FIG. 7A), but only contains information on a program contained in the broadcasting stream. Thus, the information should be converted so as to include information on the analog broadcasting. In FIG. 7D, reference numeral 131 denotes a PAT converted by the multiplexer 32. In this case, the packet control circuit 18 uses the data clock 45 produced by the clock recovery unit 13. Thus, the clock changeover switch is set at a contact e, and the video and audio encoders 30 and 31 also use the decoder clock 45. In playback, the clock changeover switch 25 is set at a contact f to use the fixed clock 46.

Id. at 6:28-46 (emphasis added). Thus, Hatanaka discloses a clock recovery module to generate a clock based on upon received timing information transmitted in packets of the multiplexed packetized data stream. As explained by Dr. Schonfeld, Hatanaka discloses generating the timing information prior to storing the data streams. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶116-117. As discussed in Sections 2 and 3 below, Hoogenboom explicitly discloses “generat[ing] a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device” and it would have been obvious to one of skill in the art to combine this disclosure with the system of Hatanaka.

Regarding the last limitation of claim 21, Hatanaka discloses “a decoder

having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.”

Hatanaka discloses that the MPEG decoder 10 has a first input coupled to the output of the clock recovery unit 13 to receive the clock, and a second input coupled the data port of the recording/playback device 2 and packet controller 18 to receive the select packets, and an output to provide decoded video signal. *See id.* at 3:16-41; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶133.

Hatanaka explains how the MPEG decoder 10 has a second input coupled the data port of the recording/playback device 2 and packet controller 18 to receive the select packets. *See id.* at 4:16-35 *Id.* at 4:36-50; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶134. Hatanaka explains that “[i]n playback, the user selects one of the digital and analog broadcasts, the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording, and inputs the selected program packet to the MPEG decoder 10 to obtain the video and audio of the desired program.” *Id.* at 6:47-52. As can be seen in Fig. 1 above, the MPEG decoder 10 is coupled to the output of the clock recovery unit 13 and the data port of the recording/playback device 2 via packet controller 18 and demultiplexer 9. Hatanaka also discloses an output to provide decoded real-time data. *See id.* at 3:16-41; 5:26-33.

2. Disclosure In Hoogenboom

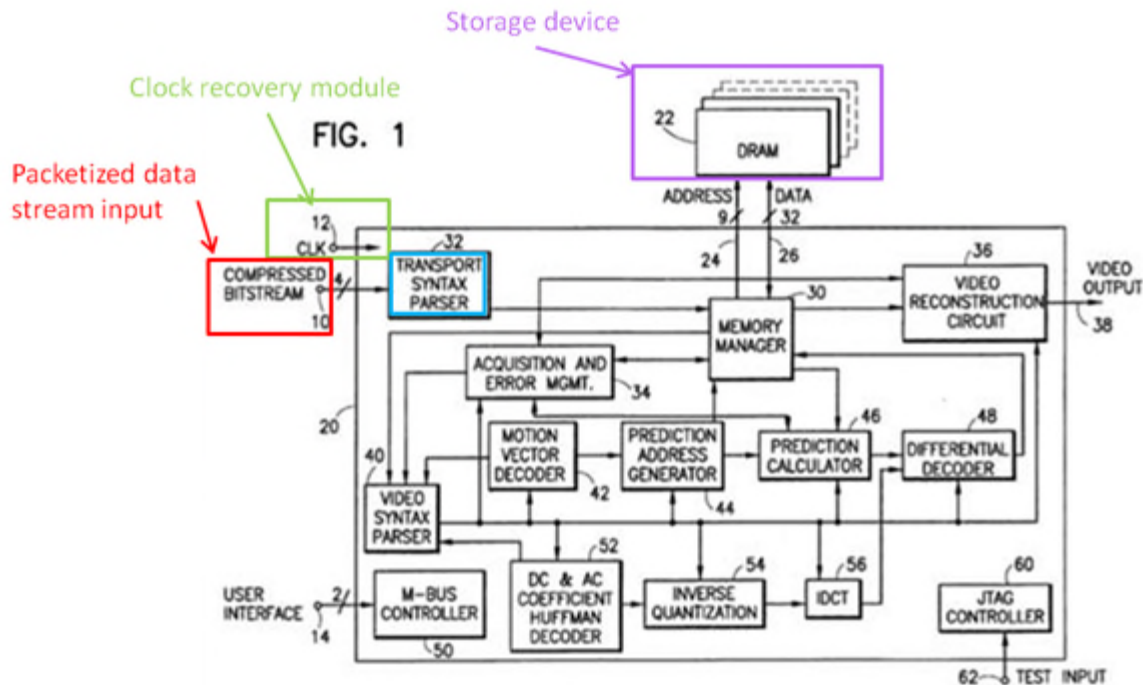
Hoogenboom is directed to “a video decompression processor, and more particularly to an efficient scheme for acquiring desired data, such as video data to be decoded, from a packetized data stream.” Ex. 1009, at 1:7-10. The efficient scheme of Hoogenboom is such that “[p]icture information can subsequently be read from the memory and decoded using the appended time information without having to reaccess the PES header.” *Id.* at Abstract, 4:19-22. This is because Hoogenboom discloses that:

A video decompression processor acquires video data for a desired service from a **packetized data stream**. The data stream includes transport packets carrying different components of the desired service. Each component is identified by a **unique packet identifier (PID)**. One of the components includes **a program clock reference (PCR) providing timing information for the desired service**. The PIDs of the transport packets are monitored to recover video packets. Header information from the recovered packets is processed to recover packetized elementary stream (PES) packets having a PES header and picture information. **Time stamp information obtained from the PES header is appended to the picture information for storage in a video memory.**

Id. at Abstract. In Hoogenboom, the data stream is a multiplexed packetized data stream. Hoogenboom also discloses the MPEG-2 compression standard for transporting digital video signals and subsequent storage and decoding of the

received MPEG-2 data. *See id.* at 2:10-46. In addition to disclosing generating a clock based on received timing information from packets of multiplexed packetized data, Hoogenboom makes it clear that the timing information is provided prior to storing the received data packets in a storage device. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶118. That is, Hoogenboom discloses “the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream **before** the select packets are stored in the storage device.”

First, Hoogenboom discloses some key components, which can be seen in Fig. 1. Fig.1, annotated and reproduced below, depicts a multiplexed packetized data stream input (discussed above), a clock 12, a transport syntax parser 32, and a DRAM 22, where the DRAM is the storage device of claim 21. Ex. 1009, at Fig. 1, 6:24-66.



With reference to Fig. 1, Hoogenboom explains that:

The video decompression processor 20 **receives a clock signal via terminal 12. The clock provides timing information that is used, e.g., to enable a transport syntax parser 32 to recover timing information and video information from transport packets contained in a packetized data stream input video terminal 10.** An acquisition and error management circuit 34 utilizes a program clock reference (PCR) and decode time stamp (DTS) detected by a video syntax parser 40 to synchronize the start of picture decoding. This circuit sets vertical synchronization and provides global synchronization for all video decode and display functions. The video layer is buffered in an input buffer (FIFO) **configured to the external DRAM 22 by memory manager 30.**

Ex. 1009, at 6:24-37 (emphasis added).

Hoogenboom discloses generating a clock based on received timing information transmitted in packets of the multiplexed packetized data stream. *See* Suppl. Schonfeld Decl., at ¶119. According to Hoogenboom, “[v]arious timing and identification information is provided in different portions of the transport stream. These include a packet identifier (PID) found in the transport header of each transport packet to provide a reference number for identifying the transport packets carrying a specific service component.” *Id.* at 2:47-52. Regarding the timing information, Hoogenboom further explains that the “[t]he timing information carried by the transport stream includes a program clock reference (PCR) which effectively represents a sample of the system time clock (STC) time base that underlies the service composed of the PIDs referenced in the service map. . . . The timing information carried by the transport stream also includes time stamps for the commencement of decoding and presentation of data for display.” *Id.* at 2:60-64, 3:7-9.

Hoogenboom discloses a method for acquiring video data for a desired service from the packetized data stream. *Id.* 3:64-66. In the method of Hoogenboom,

The data stream includes transport packets carrying different components of the service, such as a video component, audio component and control component. The component carried by a **particular transport packet is identified by a packet identifier**

(PID) for that component. One of the components includes a **program clock reference (PCR) that provides timing information for the desired service**. The method comprises the step of detecting the PCR for the desired service from the component carrying the PCR in the data stream. **The recovered PCRs are used to acquire and track a decoder time clock that corresponds to the encoder timing**. The PIDs of the transport packets are then monitored to recover those packets carrying a video component of the desired service. Header information from the recovered transport packets is processed to **recover packetized elementary stream (PES) packets** having a PES header and picture information. **Time stamp information is obtained from the PES header** of at least one of the PES packets. **The time stamp information is buffered and then is appended to the related picture information for storage in a memory**. In this manner, the picture information can be read from the memory and decoded using the time stamp information appended thereto without having to reaccess the PES header for the time stamp information.

Id. at 3:66-4:22 (emphases added). The process of generating a clock based on the timing information from the packets is best illustrated by Fig. 3 of Hoogenboom. “FIG.3 is a diagrammatic illustration showing how the received transport packets are processed at a decoder to recover picture information and time stamp information for storage in the dynamic random access memory (DRAM) of FIG. 1.” *Id.* at 5:51-55. Hoogenboom explains the components shown in Fig. 3 as follows:

One of the items contained in the **PES header 72** (or inferred from a PTS in the PES header) is the **decode time stamp (DTS) 104** which is required by the video syntax parser 40 in order to properly decode the picture data. Thus, in accordance with the present invention, **the DTS is extracted from the PES header 72 and reinserted following the picture header 100 in the video information (picture data) 102 stored in the FIFO portion of DRAM 22. The insertion of the DTS in the video information stored in DRAM 22 enables the decompression processor to process the video information without having to retrieve the DTS from a source outside the DRAM.** It should be noted that the PTS is also stored in DRAM 22 if it differs from the DTS.

Id. at 9:39-50 (emphases added).

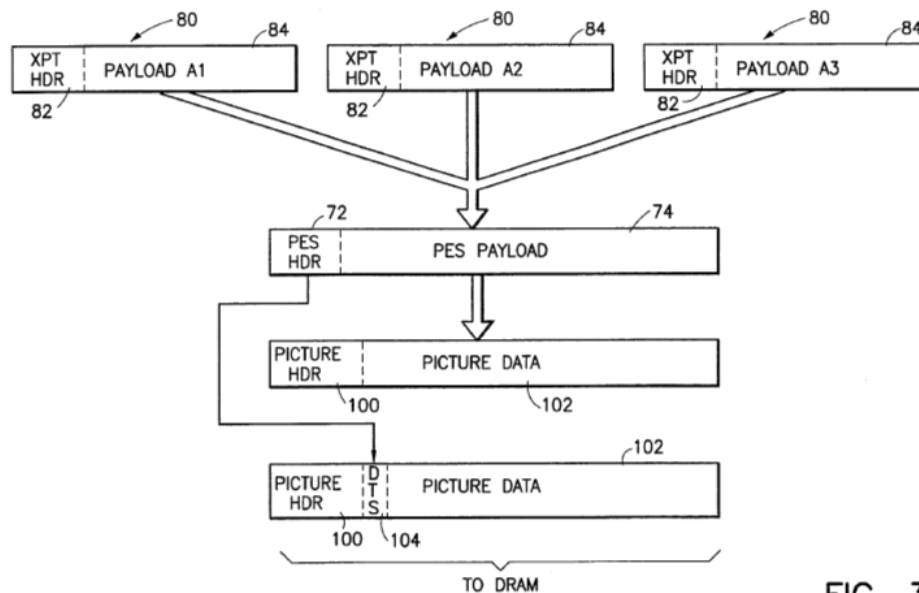


FIG. 3

According to Dr. Schonfeld, one of skill in the art would understand that these disclosures in Hoogenboom demonstrate that a clock is generated from received timing information prior to storage of the received data packets in a

storage device. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶120-124. Dr. Schonfeld explains that Hoogenboom explains a multistep process where the clock is generated from the received timing information and then the received timing information is appended to the picture data and then stored in a storage device. *Id.* at ¶125.

According to Dr. Schonfeld, the first step is that the system must recover the program clock reference (PCR), which is the clock, from the received packetized data stream. *Id.* at ¶125. Next, the PCR is used to acquire the decoder time clock that corresponds to the encoder timing. *Id.* The PIDs of the transport packets are then monitored to recover the video component of the desired data stream. *Id.* Next, the PES header information is extracted from the recovered video packets. *Id.* Then, the DTS is next obtained from the PES header. The DTS is the timing information used to indicate when the decoder should start to decode. The DTS is then appended to the picture data and stored in the DRAM, the storage device. *See* Ex. 1009 3:64-4:22; *see also* Suppl. Schonfeld Decl., at ¶125.

In Fig. 3, Hoogenboom depicts the timing information being extracted and appended to the picture data prior to storage of the data in the DRAM. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶126. Hoogenboom explains that timing information is appended to the related picture information based on a PCR providing timing information, which is one component of the packet identifier

(PID), as explained above. Ex. 1009, at 4:2-22. Dr. Schonfeld explains that this means a program clock reference (PCR) providing timing information is extracted from the packetized data stream and used to recover a decoding time clock. The decoding time clock is subsequently used to recover picture header information containing the DTS. Then the time stamp information is appended to the related picture information and stored in the memory device. *Id.* at 4:17-22. Therefore, Hoogenboom discloses “the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.”

3. Motivation To Combine Hoogenboom With Hatanaka

As discussed above, Hoogenboom discloses an improvement to video streaming—a scheme for efficiently acquiring desired data, such as video data, to be decoded from a packetized data stream. Ex. 1009, at 1:7-10. Under Supreme Court precedent, “any need or problem known in the field” can provide a reason for combining prior art elements. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007). Here, one of ordinary skill in the art would have been motivated to combine the teachings of Hoogenboom and Hatanaka because both references focused on a similar problem – improving the video decoding of stored digital tv/video signals. *Compare* Ex. 1006, at 1:29-35 *with* Ex. 1009, at 1:7-10, 1:21-29,

1:46-48; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶127. As explained above, Hoogenboom provides a solution to that problem by disclosing an efficient scheme for acquiring video data to be decoded from a packetized data stream. Ex. 1009, at 1:7-10, 1:21-29, 1:46-48. Dr. Schonfeld explains that Hoogenboom and Hatanaka present similar solutions. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶127. According to Dr. Schonfeld, both Hoogenboom and Hatanaka disclose appending timing information to the stored video data. Ex. 1006, at 4:36-48; Ex. 1009 at Abstract, 3:66-4:22. The difference is that Hatanaka stores time stamps generated from the data clock, whereas Hoogenboom provides a better solution of extracting the DTS and appending it to the video data. Ex. 1006, at 4:36-48; Ex. 1009 at 6:24-37, 9:39-50. Dr. Schonfeld explains that Hoogenboom's proposed solution has two benefits. First, Hoogenboom's solution provides for a simpler operation because the time stamps are simply extracted from the packetized stream instead of being generated from the recovered clock as done by Hatanaka. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶127. Second, Hoogenboom's proposed solution provides for a robust approach because the time stamps were generated by the clock at the encoder and are thus less prone to errors than the time stamps of Hatanaka which were generated from the recovered clock. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶127. To achieve the efficiency desired in Hoogenboom, Hoogenboom discloses extracting the PCR timing information, using it to recover a clock, which is

subsequently used to identify the DTS timing information, and appending it to the picture data prior to storage. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶127. As a result, the stream can be retrieved from storage faster and more efficiently without having to reaccess the timing information. In this regard, Hoogenboom explains the following:

- “Time stamp information obtained from the PES header is appended to the picture information for storage in a video memory. Picture information can subsequently be read from the memory and decoded using the appended time stamp information without having to reaccess the PES header.” Ex. 1009, at Abstract.
- “The time stamp information is buffered and then is appended to the related picture information for storage in a memory. In this manner, the picture information can be read from the memory and decoded using the time stamp information appended thereto without having to reaccess the PES header for the time stamp information.” *Id.* at 4:17-22.
- “Timing information extracted from a PES header is stored together with picture information in a video memory to facilitate the decoding of the picture information. Various techniques are provided for masking and recovering from transmission errors.” Ex. 1009, at 12:8-12.

Because of these benefits, one of skill in the art would have been motivated to apply the teachings of Hoogenboom, of generating the timing information prior to storage, to the similar system disclosed in Hatanaka to more efficiently acquire desired video data from storage. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶128. Therefore, it would have been obvious to one of skill in the art to combine the teachings of Hoogenboom and Hatanaka.

Hoogenboom also discloses a system like Hatanaka and thus, Hoogenboom discloses improving a system like the one disclosed in Hatanaka. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶129. Hoogenboom and Hatanaka both are in the field of video streaming. Ex. 1009, at 1:11-20, 12:4-12; Ex. 1006, at 1:29-35; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶129. As discussed above, both Hoogenboom and Hatanaka relate to recording and playback of video streams. *See id.* Also, Hoogenboom and Hatanaka both disclose the use of a transport stream compressed using an MPEG-2 compression system, and therefore use a PCR and DTS for timing information as discussed above. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶129. Because the techniques taught by Hoogenboom have been used to improve digital video streaming devices similar to the one disclosed in Hatanaka, a person of ordinary skill in the art would have been motivated to apply Hoogenboom's teachings regarding clock recovery and timestamp storage to improve the video streaming device of Hatanaka. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶129.

B. Ground 2: Claim 21 Is Unpatentable Under 35 U.S.C. §103(a) As Being Obvious Over Hatanaka In View Of Anderson

1. Disclosure In Hatanaka

Hatanaka discloses the limitations of claim 21 as discussed above in Ground 1. As discussed in Section 2 below, it would also have been obvious to one of skill in the art “to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device” in view of the disclosure in Anderson. As discussed in Section 3 below, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Anderson to the system of Hatanaka.

2. Disclosure In Anderson

Anderson is directed to a system for “[t]able filtering before memory storage by the transport demultiplexor [to] reduce[] the load on the application processor by filtering table sections before sending them to DRAM or other memory. . . .” Ex. 1010, at 11:57-65. As explained below, the system of Anderson also discloses a clock recovery process similar to Hatanaka.

First, Anderson discloses a clock recovery module shown in Fig. 6. Anderson explains that Fig. 6 shows “the dataflow of the transport demultiplexor of the invention.” Ex. 1010, at 7:34-35. Highlighted in green in the annotated version of Fig. 6 reproduced below, the clock recovery module occurs in the front end. Then,

packets are sent to the packet buffer on the back end. Anderson explains the front end and back end logic as follows:

The **front end** logic of the transport demultiplexor of the invention includes a packet synchronizer, **a packet parser having a packet ID (PID) filter, a clock recovery unit**, an optional descrambler, and a packet loader. The **back end** logic of the transport demultiplexor of our invention includes a buffer control and a data unloader, where the buffer control has a data link to the packet buffer and to the audio and video unloaders and to the data unloader. The buffer control includes an arbiter, packet management, and **static RAM control**.

Ex. 1010, at 6:61-7:4 (emphases added). Annotated Fig. 6 below depicts the input data stream (highlighted in red), clock recovery (highlighted in green), and packet parser with a PID filter (highlighted in blue) on the front end and packet buffer on the back end.

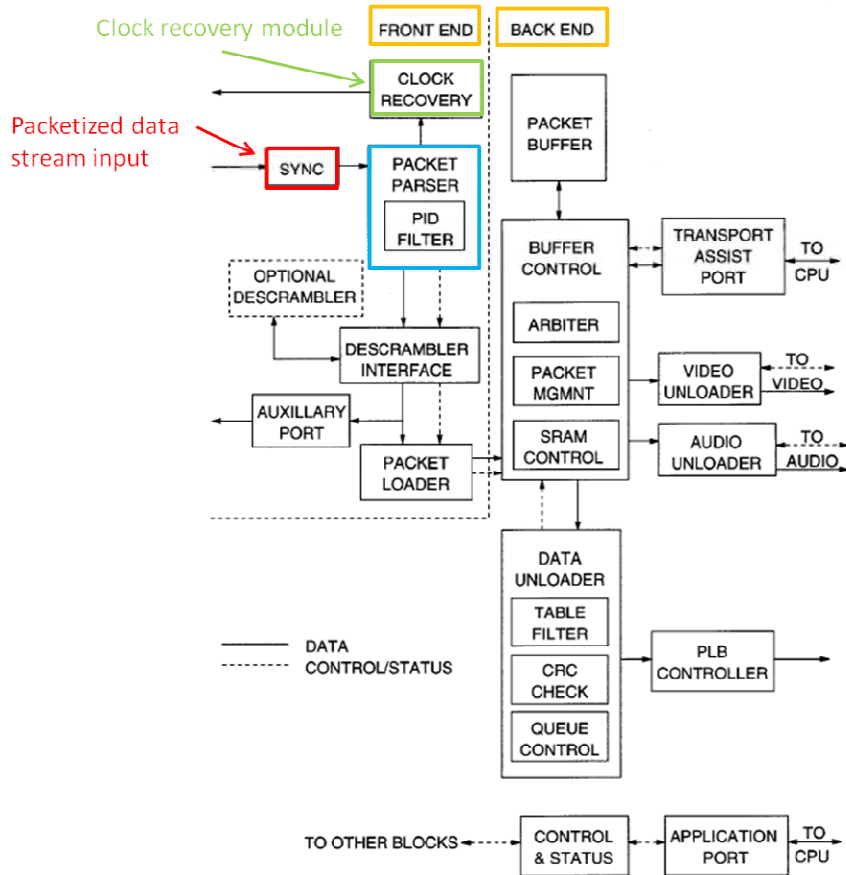


FIG. 6

Regarding Fig. 6, Anderson explains that “[t]he SYNC block determines the start of the transport packet.” Ex. 1010, at 7:66-67. In Anderson, the transport packet is a packetized multiplexed bitstream compressed based on the MPEG-2. *Id.* at 7:46-53; *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶147-150. Next, the packetized transport streams are sent to the packet parser. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶150-151. According to Anderson:

The PACKET PARSER extracts data from the transport packet header and adaptation field. The PID is one of these fields. The PID is

compared to active PIDs in the PID filter. If the [PID] matches one of the predefined values, the remaining fields are extracted and the packet is forwarded to the descrambler interface which will send filtered but scrambled data to a descrambler, if present.

Ex. 1010, at 8:1-7. Additionally, Anderson explains that “the packet parser sends PCRs from matching PCR packets to the clock recovery unit for reconstructing the System Time Clock (STC).” Ex. 1010, at 8:12-14. Next, “[s]tatus indicators representing parsed information are sent along with the complete transport packet to the packet loader to be stored in the packet buffer.” Ex. 1010, at 8:15-17. Anderson explains that “[t]he packet buffer holds a plurality, for example up to ten or more, transport packets while they are moved to the decoders and the DRAM or other memory [not shown in Fig. 6].” *Id.* at 8:17-20. In Anderson, the DRAM is the storage device.

According to Anderson, “[a] further need exists for transport demultiplexors to support additional processing and parsing functions to minimize the load on the host processor, **such as clock recovery**, table filtering, and error detection.” *Id.* at 6:4-7 (emphasis added). And, Anderson discloses that table filtering for minimizing the load on the process happens before storage in the memory device. Regarding the table filtering process, Anderson explains:

One aspect of the table processing of the transport demultiplexor of the invention is table section filtering before memory storage of the tables. **Table filtering before memory storage by the transport**

demultiplexor reduces the load on the application processor by filtering table sections before sending them to DRAM or other memory. Filtering reduces the application processor work load for parsing table sections and the required size of working areas in DRAM or other memory to manage table data.

Id. at 11:57-65 (emphasis added).

Therefore, Anderson discloses generating a clock on the front end based on PCR packets sent to the clock recovery unit for producing the STC. Ex. 1010, at 8:15-17. As explained below, it would have been obvious to one of ordinary skill in the art to combine Anderson's clock recovery disclosure with Hatanaka.

3. Motivation To Combine Anderson With Hatanaka

As discussed above, Anderson discloses an improvement to real-time video streaming. Specifically, Anderson discloses table filtering before storing in the memory to reduce the load on the application processor. Ex. 1010, at 11:57-65. A person of ordinary skill in the art would understand that the teachings of Anderson—"filtering table sections before sending them to DRAM or other memory"—would apply equally to clock recovery. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶154. That is, the motivation to perform clock recovery before sending the transport packets to DRAM or other memory would be motivated by the desire to "reduce[] the application processor work load ... and the required size of working

areas in DRAM or other memory,” as described in Anderson. *Id.* Anderson explains that:

Because of real-time processing constraints and system bandwidth requirements, there is a clear need for transport demultiplexors that can extract program clock references (PCRs) from the data stream and filter out unnecessary components through the use of Packet Ids (PIDs). A further need exists for transport demultiplexors to support additional processing and parsing functions to minimize the load on the host processor, such as clock recovery, table filtering, and error detection.

Ex. 1010, at 5:66-7:7.

Thus, a person of ordinary skill in the art have been motivated to use the teachings of Anderson to further improve real-time video streaming by performing clock recovery before storing the transport packets in memory device to further reduce the work load on the application processor. Under Supreme Court precedent, “any need or problem known in the field” can provide a reason for combining prior art elements. *KSR*, 550 U.S. at 420. Here, one of ordinary skill in the art would have been motivated to combine the teachings of Anderson and Hatanaka because both references focused on a similar problem – improving real-time video decoding of compressed MPEG-2 streams. *Compare* Ex. 1006, at 1:29-35 *with* Ex. 1010, at 1:5-15 and 5:66-7:7. Both Anderson and Hatanaka have a similar approach to video decoding based on extraction of PCR from the packet header for clock

recovery. *Compare* Ex. 1006, at 4:36-48 *with* Ex. 1010, at 8:1-14. *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶154-157. Dr. Schonfeld explains that one of skill in the art would have been motivated to apply the teachings of Anderson to the system in Hatanaka, which is similar, to extract the PCR from the packet header for clock recovery before storing the transport packets in memory to further reduce the work load on the processor. *see also* Ex. 1011, Suppl. Schonfeld Decl., at ¶157.

Based on the benefits disclosed as a result of the system described in Anderson, one of skill in the art would have been motivated to apply Anderson's disclosure of generating a clock on the front end and storage on the back end, to the similar system disclosed in Hatanaka to provide for additional processing while also reducing the load on the processor. Therefore, it would have been obvious to one of skill in the art to combine Anderson with Hatanaka.

Additionally, Anderson discloses a similar system to the one disclosed in Hatanaka. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶157. Both Anderson and Hatanaka are in the field of real-time video streaming. Ex. 1010, at 1:5-15; Ex. 1006, at 1:29-35. Also, Anderson and Hatanaka both disclose the use of a transport stream compressed in a MPEG-2 compression system and use a PID, PCR, and packet header for timing information as discussed above—both disclose real-time compression of MPEG-2 data. Because the techniques taught by Anderson have

been used to improve digital video streaming devices similar to the one disclosed in Hatanaka, a person of ordinary skill in the art would have been motivated to apply Anderson’s techniques regarding clock recovery on the front end to improve the video streaming device of Hatanaka. Thus, under *KSR*, it would have been obvious to generate the timing information based on the packetized data streams prior to storage in the SRAM, as taught by Anderson, to improve the video streaming system of Hatanaka. *See* Ex. 1011, Suppl. Schonfeld Decl., at ¶¶154-157.

In light of the above, the table below demonstrates how each limitation of claim 21 of the ’945 Patent is obvious over Hatanaka in view of Hoogenboom and Hatanaka in view of Anderson as set forth above in Grounds 1 and 2. For all these reasons, claim 21 is unpatentable in view of Hatanaka and Hoogenboom and Hatanaka and Anderson and thus, Petitioner has a reasonable likelihood of prevailing with respect to claim 21.

’945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010)²
21. A system comprising: [21.a] a first input node to receive a multiplexed packetized data stream that carries real-time	“JP-A-8-98164 discloses a <u>receiving</u> system and a recording/playing back device <u>for receiving/recording a transmitted multiplexed digital signal</u> as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for <u>receiving a transmitted multiplexed digital information signal</u> and

² All underlining in the claim chart represents emphasis added.

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
multimedia programs;	<p>for selecting desired information, and recording means for recording the information received by the receiving means.” Ex. 1006, at 1:12-20.</p> <p>“FIG. 2 shows a composition of a <u>transmitted digital broadcasting signal</u>. As shown in a packet composition of FIG. 2(A), the <u>transmission signal has a packet composition</u> of 204 bytes; a 4-byte header 50; a 184-byte data 51 <u>representing information on a video, audio, added data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. The packets of those video, audio, added data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis.</u> The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator, 55 a payload unit start indicator, 56 a transport priority, 57 a PID indicative of attributes of the packet, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” <i>Id.</i> at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at <u>a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10. The <u>multiplexed</u></u></p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p><u>signal</u> contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. . . .” <i>Id.</i> at 3:16-41.</p> <p>“When the received signal is recorded in the recording/playback device 2, <u>the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program</u> to be recorded as in the demultiplexer 9. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17.” <i>Id.</i> at 3:42-56; <i>see also id.</i> at 4:16-35.</p> <p>“When the analog broadcasting signal is recorded, an analog video signal 150 is inputted to the video input terminal 26 of the encoder 3 of FIG. 1. The video A/D converter 28 converts the analog video signal to a digital video signal. The video encoder 30 compresses the image, using the MPEG 2, etc., as in the compression of the digital broadcasting signal, and <u>outputs the compressed signal</u> to the multiplexer 32. An analog audio signal 151 is inputted to the audio input terminal 27, and converted by the audio A/D converter 29 to a digital audio signal. The audio encoder 31 compresses the digital audio signal, and also <u>outputs</u></p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p><u>this signal</u> to the multiplexer 32, which <u>multiplexes a video stream 42</u> produced by the video encoder 30 <u>and an audio stream 43</u> produced by the audio encoder 31.” <i>Id.</i> at 5:1-14.</p> <p>“As shown in FIGS. 5A-5E, <u>the video stream 42, audio stream 43, other packets, and NULs are multiplexed on a time-divisional basis to form a single signal. The respective video packets VIs 1 (110), 2 (111), etc., on the video stream 42 are the same in content as the VIs 1 (116), 2 (112) etc., on the multiplexed stream 44. Similarly, the respective audio packets AUs 1 (113), 2 (114) etc., of the audio stream 43 are the same in content as the AUs 1 (122), 2 (124) etc., of the multiplexed stream 44. Thus, the multiplexed stream 44 has a stream composition similar to the output of the interface 12 of the digital broadcasting receiver 1. Thus, the recording signal changeover switch 17 selects a contact d and <u>inputs the multiplexed stream 44</u> to the packet control circuit 18 to thereby record/playback the multiplexed stream 44 <u>in the same manner as the digital broadcasting signal.</u>” <i>Id.</i> at 5:54-6:2.</u></p> <p>“This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p> <p><i>See also</i> Ex. 1011, Suppl. Schonfeld Decl., at ¶¶94-99.</p>
[21.b] a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;	<p>“FIG. 2 shows a composition of a transmitted digital broadcasting signal. As shown in a packet composition of FIG. 2(A), the transmission signal has a packet composition of 204 bytes; a 4-byte header 50; a 184-byte data 51 representing information on a video, audio, added data, etc., compressed in a compression system called, for example, MPEG 2 (Moving Picture Expert Group 2) as an international standard, and a 16-byte parity 52. The packets of those video, audio, added</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>data, etc., are received in a multiplexing manner on a time divisional basis on a transmission line, as shown in FIG. 2(B). Generally, not only one program, but also a plurality of programs of video, audio and added data is multiplexed on a time divisional basis. The header composition of FIG. 2(C) shows a content of the header 50. In FIG. 2(C), reference numeral 53 denotes a sync byte indicative of the head of the packet, 54 a transport error indicator, 55 a payload unit start indicator, 56 a transport priority, <u>57 a PID indicative of attributes of the packet</u>, 58 a transport scrambling control, 59 an adaptation field control, and 60 continuity counter, each showing attributes and status of the packet, composed of 4 bytes in all. The numerals appearing on top of the packet each represent the number of bits of a respective subpacket.” Ex. 1006, at 2:51-3:6.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set at a contact to input the output from the FEC 7 <u>to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program</u>, and then outputs these packets to the MPEG decoder 10. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned.” <i>Id.</i> at 3:16-26.</p> <p>“When the received signal is recorded in the recording/playback device 2, the output from the FEC 7 <u>is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program to be recorded as in the demultiplexer 9.</u> When the received signal is recorded</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. <u>Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information.</u> The signal separated by the interface 12 is inputted to the packet control circuit 18 by selecting a contact c by the recording signal changeover switch 17. . . .” <i>Id.</i> at 3:42-63.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which decipheres a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. <u>Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.</u>” <i>Id.</i> at 9:6-13</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p> <p><i>See also</i> Ex. 1011, Suppl. Schonfeld Decl., at ¶¶100-104.</p>
<p>[21.c] a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;</p>	<p>“JP-A-8-98164 discloses a receiving system and a recording/playing back device for receiving/recording a transmitted multiplexed digital signal as a conventional technique for recording/playing back a digital signal. This prior art publication describes a receiving system which includes receiving means for receiving a transmitted multiplexed digital information signal and for selecting desired information, and <u>recording means for recording the information received by the receiving means.</u>” Ex. 1006, at 1:12-21.</p> <p>“FIG. 1 is a block diagram of a</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), <u>2 a recording/playback device</u>, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner,” <i>Id.</i> at 2:30-50.</p> <p>“<u>When the received signal is recorded in the recording/playback device 2</u>, the output from the FEC 7 is inputted to the interface 12, which separates packets of video and audio information and added information relating to a program <u>to be recorded as in the demultiplexer 9</u>. When the received signal is recorded and played back by the recording/playback device 2, it is required to also record and play back program information required for automatic selection of a broadcasting station. Thus, in addition to the packets selected by the demultiplexer 9, the interface 12 also selects a packet of program information relating to the program to be recorded and converts a part of the packet of program information. . . .” <i>Id.</i> at 3:42-63.</p> <p>“As shown in FIGS. 5A-5E, the <u>multiplexer 32 temporarily stores the video and audio streams 42 and 43</u>, and outputs them as the video and audio packet streams 45 and 46 at the same transfer rate.” <i>Id.</i> at 5:26-29.</p> <p>“Thus, the <u>digital broadcasting signal and the digital signal to which the analog broadcasting signal is converted are easily recorded simultaneously</u> in a multichannel. If the video and audio streams 42 and 43 alone are multiplexed in a mode in which no broadcasting stream 41 is outputted in the multiplexer 32 of the FIG. 6 device, an operational mode similar to that described in FIG. 1 is obtained. In this case, the</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>clock changeover switch 25 is required to be set at the contact f in the recording operation.” <i>Id.</i> at 6:53-61.</p> <p>“While in the above the magnetic tape is used as a recording medium, a magnetic disk, optical disk, semiconductor memory or other recording medium may be used. Although not shown in FIGS. 1 and 6, a deciphering circuit which deciphers a cipher signal may be provided between the QPSK demodulator 6 and the FEC 7. Selection of a packet and conversion of a packet on the program information by the interface 12 may be performed by the demultiplexer 9 or packet control circuit 18.” <i>Id.</i> at 9:6-13.</p> <p><i>See also id.</i> at FIGS. 1-7, 9, 10.</p> <p><i>See also</i> Ex. 1011, Suppl. Schonfeld Decl., at ¶¶105-110.</p>
<p>[21.d] a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and</p>	<p>“In FIG. 1, reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), 2 a recording/playback device, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner, 6 a QPSK demodulator, 7 a forward error correction (FEC) unit for correcting an error involved in the transmission of a signal, 8 a playback changeover switch, 9 a demultiplexer, 10 a MPEG decoder, 11 an NTSC encoder, 12 an interface between the devices 1 and 2, 13 a clock recovery unit, 14 a D/A converter, 15 a video output terminal, 16 an audio output terminal, 17 a recorded signal changeover switch, 18 a packet control circuit, 19 a recording/playback data processing, 20 a record amplifier, 21 a playback amplifier, 22 a magnetic tape, 23 a rotary head, 24 a clock generator, 25 a clock changeover switch, 26 a video input terminal, 27 an audio input terminal, 28 a video A/D converter, 29 an audio A/D converter, 30 a video encoder, 31 an audio encoder, 32 a multiplexer, and 47 a digital signal processor.” Ex. 1006, at 2:32-50.</p> <p>“The <u>multiplexed signal contains a packet called, for</u></p>

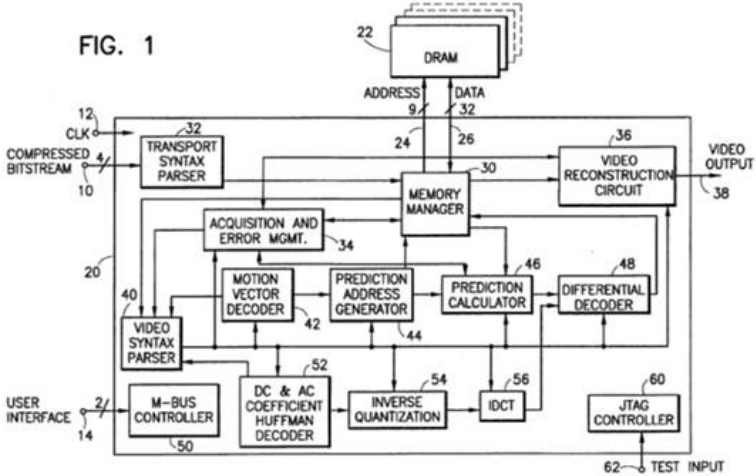
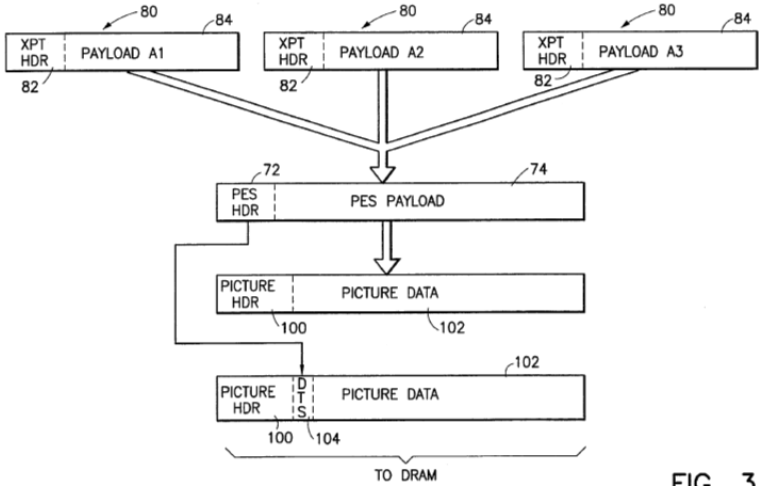
'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p><u>example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals.” <i>Id.</i> at 3:22-37.</u></p> <p><u>“Also, in playback, the data clock 45 used in the MPEG decoder 10 is required to obtain the same frequency as it was compressed in the broadcasting station. To this end, at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly. To this end, in recording, the time stamp 102 is added in the packet control circuit 18. In playback, the respective packets are outputted by the packet control circuit 18 in accordance with the time stamps 102 to maintain the time intervals at which the packets are outputted. To this end, clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18.” <i>Id.</i> at 4:36-50.</u></p> <p><u>“In recording, as shown in FIGS. 7A-7D, the respective broadcasting (BR), video (VI), and audio (AU) packets of the broadcasting stream 41, video stream 42, and</u></p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010)²
	<p>audio stream 43 are multiplexed on a time divisional basis and <u>PMT and PCR are added to the multiplexed packets to constitute a multiplexed stream.</u> <u>In this case, the PAT is already contained in the broadcasting stream 41 (shown by a packet 130 of FIG. 7A), but only contains information on a program contained in the broadcasting stream.</u> <u>Thus, the information should be converted so as to include information on the analog broadcasting.</u> <u>In FIG. 7D, reference numeral 131 denotes a PAT converted by the multiplexer 32.</u> <u>In this case, the packet control circuit 18 uses the data clock 45 produced by the clock recovery unit 13.</u> <u>Thus, the clock changeover switch is set at a contact e, and the video and audio encoders 30 and 31 also use the decoder clock 45.</u> <u>In playback, the clock changeover switch 25 is set at a contact f to use the fixed clock 46.”</u> <i>Id.</i> at 6:28-46; <i>see also id.</i> at 6:3-16.</p> <p>“This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22. <i>See also id.</i> at FIGS. 1-7, 9, 10.</p> <p><u>Ex. 1009</u></p> <p>“<u>Timing information extracted from a PES header is stored together with picture information in a video memory to facilitate the decoding of the picture information.</u> Various techniques are provided for masking and recovering from transmission errors.” Ex. 1009, at 12:8-12.</p> <p>“A decompression processor acquires video data for a desired service from a <u>packetized data stream.</u> The data stream includes transport packets carrying different components of the desired service. Each component is identified by a <u>unique packet identified (PID).</u> One of</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>the components includes a <u>program clock reference (PCR) providing timing information for the desired service</u>. The PIDs of the transport packets are monitored to recover video packets. Header information from the recovered packets is processed to recover packetized elementary stream (PES) packets having a PES header and picture information. <u>Time stamp information obtained from the PES header is appended to the picture information for storage in a video memory.</u>" <i>Id.</i> at Abstract.</p> <p>"Various timing identification information is provided in different portions of the transport stream. These include a packet identifier (PID) found in the transport header of each transport packet to provide a reference number for identifying the transport packets carrying a specific service component." <i>Id.</i> at 2:47-52.</p> <p>"The timing information carried by the transport stream includes a program clock reference (PCR) which effectively represents a sample of the system time clock (STC) time base that underlies the service composed of the PIDs referenced in the service map." <i>Id.</i> at 2:60-64.</p> <p><u>"The timing information carried by the transport stream also includes time stamps for the commencement of decoding and presentation of data for display.</u> The presentation time stamp (PTS) is used for service component acquisition and also for evaluating whether timing and buffer control are operating properly at the decoder. The decoder time stamp (DTS) is used to indicate when the decoder should start to decode the first access unit (e.g., video frame) that starts somewhere in the payload of a packetized elementary stream (PES) packet whose header includes the DTS. A packetized elementary stream is a data stream composed of end-to-end PES packets which have variable length and are typically far longer than a fixed</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>length transport packet. Thus, a PES packet is typically composed of data from a plurality of transport packets with a single PID.” <i>Id.</i> at 3:7-21.</p> <p>“The DTS is required by a video decompression processor in order to properly time the commencement of video decoding. Since the DTS is packaged in a PES header, it has been difficult and complicated for a video decompression processor at the receiver to obtain the DTS at the same time it is receiving the associated video data to be parsed. Prior to parsing, the video data is retrieved from a video memory that temporarily stores the data after having been retrieved from the transport stream. The video data will not be ready for decoding by the video decompression processor until sometime after the PES header containing the necessary DTS has been discarded.” <i>Id.</i> at 3:22-34.</p> <p>“In accordance with the present invention, a method is provided for acquiring video data for a desired service from a packetized data stream. The data stream includes transport packets carrying different components of the service, such as a video component, audio component and control component. The component carried by a particular transport packet is identified by a packet identifier (PID) for that component. One of the components includes a program clock reference (PCR) that provides timing information for the desired service. The method comprises the step of detecting the PCR for the desired service from the component carrying the PCR in the data stream. The recovered PCRs are used to acquire and track a decoder time clock that corresponds to the encoder timing. The PIDs of the transport packets are then monitored to recover those packets carrying a video component of the desired service. Header information from the recovered transport packets is processed to recover packetized elementary stream (PES) packets having a</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>PES header and picture information. Time stamp information is obtained from the PES header of at least one of the PES packets. <u>The time stamp information is buffered and then is appended to the related picture information for storage in a memory.</u> In this manner, the picture information can be read from the memory and decoded using the time stamp information appended thereto without having to reaccess the PES header for the time stamp information.” <i>Id.</i> at 3:64-4:22.</p> <p>“The video decompression processor 20 receives a clock signal via terminal 12. <u>The clock provides timing information that is used, e.g., to enable a transport syntax parser 32 to recover timing information and video information from transport packets contained in a packetized data stream input via terminal 10.</u> An acquisition and error management circuit 34 utilizes a program clock reference (PCR) and decode time stamp (DTS) detected by a video syntax parser 40 to synchronize the start of picture decoding. This circuit sets vertical synchronization and provides global synchronization for all video decode and display functions. The video layer is buffered in an input buffer (FIFO) configured to the external DRAM 22 by memory manager 30.” <i>Id.</i> at 6:23-37.</p> <p>“One of the items contained in the PES header 72 (or inferred from a PTS in the PES header) is the decode time stamp (DTS) 104 which is required by the video syntax parser 40 in order to properly decode the picture data. Thus, in accordance with the present invention, the DTS is extracted from the PES header 72 and reinserted following the picture header 100 in the video information (picture data) 102 stored in the FIFO portion of DRAM 22. The insertion of the DTS in the video information stored in DRAM 22 enables the decompression processor to process the video</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>information without having to retrieve the DTS from a source outside the DRAM. It should be noted that the PTS is also stored in DRAM 22 if it differs from the DTS.” <i>Id.</i> at 9:38-51.</p>  <p>“FIG.3 is a diagrammatic illustration showing how the received transport packets are processed at a decoder to recover picture information and time stamp information for storage in the dynamic random access memory (DRAM) of FIG. 1.” <i>Id.</i> at 5:51-55.</p>  <p>FIG. 3</p> <p>“One of the items contained in the PES header 72 (or inferred from a PTS in the PES header) is the decode time stamp (DTS) 104 which is required by the video syntax parser 40 in order to properly decode the picture</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>data. Thus, in accordance with the present invention, the DTS is extracted from the PES header 72 and reinserted following the picture header 100 in the video information (picture data) 102 stored in the FIFO portion of DRAM 22. The insertion of the DTS in the video information stored in DRAM 22 enables the decompression processor to process the video information without having to retrieve the DTS from a source outside the DRAM. It should be noted that the PTS is also stored in DRAM 22 if it differs from the DTS.” <i>Id.</i> at 9:39-50.</p> <p><u>Ex. 1010</u></p> <p>“This invention relates to digital delivery systems, especially for digital video and digital audio data. More particularly, the invention relates to multiplexors, networks, distribution systems, demultiplexors, and multiplexed bitstreams, and especially to bitstreams carrying a system or transport layer, and one or more data layers of compressed digital video and digital audio data. More particularly, the invention relates to demultiplexing the incoming bitstream to recover video data, audio data, and such system data as program clock references, packet id's, and the like, in real time.” Ex. 1010, at 1:5-15.</p> <p>“FIG. 6 shows the dataflow of the transport demultiplexor of the invention.” Ex. 1010, at 7:34-35.</p> <p>“The <u>front end</u> logic of the transport demultiplexor of the invention includes a packet synchronizer, <u>a packet parser having a packet ID (PID) filter</u>, a clock recovery unit, an optional descrambler, and a packet loader. The <u>back end</u> logic of the transport demultiplexor of our invention includes a buffer control and a data unloader, where the buffer control has a data link to the packet buffer and to the audio and video unloaders and to the data unloader. The buffer control includes an arbiter,</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>packet management, and <u>static RAM control</u>.” Ex. 1010, at 6:61-7:4.</p> <p>“A further need exists for transport demultiplexors to support additional processing and parsing functions to minimize the load on the host processor, such as clock recovery, table filtering, and error detection.” <i>Id.</i> at 6:4-7.</p> <p style="text-align: center;">FIG. 6</p> <p>“The SYNC block determines the start of the transport packet.” Ex. 1010, at 7:66-67.</p> <p>“The MPEG-2 transport bitstream is a set of time division or packet multiplexed bitstreams. Each such time division or packet multiplexed bitstream may contain a plurality of programs, that is, television</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010)²
	<p>channels, digital communications, or the like. Each bitstream contains a systems stream which provides systems layer functions for one or more audio and video elementary streams in the time division or packet multiplexed single stream.” <i>Id.</i> at 7:46-53.</p> <p>“The PACKET PARSER extracts data from the transport packet header and adaptation field. The PID is one of these fields. The PID is compared to active PIDs in the PID filter. If the matches one of the predefined values, the remaining fields are extracted and the packet is forwarded to the descrambler interface which will send filtered but scrambled data to a descrambler, if present.” Ex. 1010, at 8:1-7.</p> <p>“Concurrently, the packet parser sends PCRs from matching PCR packets to the clock recovery unit for reconstructing the System Time Clock (STC).” Ex. 1010, at 8:12-14.</p> <p>“Status indicators representing parsed information are sent along with the complete transport packet to the packet loader to be stored in the packet buffer. The packet buffer holds a plurality, for example up to ten or more, transport packets while they are moved to the decoders and the DRAM or other memory [not shown in Fig. 6].” Ex. 1010, at 8:15-20.</p> <p>“Moreover, since the PCR PID filter is separate from the general PID filters, the STC can be started before the transport begins delivering data to the decoders.” Ex. 1010, at 9:26-28.</p> <p>“Because of real-time processing constraints and system bandwidth requirements, there is a clear need for transport demultiplexors that can extract program clock references (PCRs) from the data stream and filter out unnecessary components through the use of Packet</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>Ids (PIDs). A further need exists for transport demultiplexors to support additional processing and parsing functions to minimize the load on the host processor, such as clock recovery, table filtering, and error detection.” Ex. 1010, at 5:66-7:7.</p> <p>“It is a still further object of the invention to extract program clock references (PCRs) from the data stream, filtering out unnecessary streams through the use of Packet Ids (PIDs). It is a still further object of the invention to support additional processing and parsing functions to minimize the load on the host processor, such as clock recovery, table filtering, and error recovery.” Ex. 1010, at 6:16-23.</p> <p>“Table filtering before memory storage by the transport demultiplexor [to] reduce[] the load on the application processor by filtering table sections before sending them to DRAM or other memory. . . .” Ex. 1010, at 11:57-65.</p> <p><i>See also</i> Ex. 1011, Suppl. Schonfeld Decl., at ¶¶111-131 and 146-158.</p>
<p>[21.e] a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.</p>	<p>“FIG. 1 is a block diagram of a receiving/recording/playing back device for a digital broadcasting signal in a first embodiment of the present invention. In FIG. 1, <u>reference numeral 1 denotes a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD)</u>, 2 a recording/playback device, 3 an encoder, 4 a digital broadcasting signal input terminal, 5 a tuner, 6 a QPSK demodulator, 7 a forward error correction (FEC) unit for correcting an error involved in the transmission of a signal, 8 a playback changeover switch, 9 a demultiplexer, <u>10 a MPEG decoder</u>,” Ex. 1006, at 2:30-50.</p> <p>“When the broadcasting signal is outputted from the present device, the playback changeover switch 8 is set</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p>at a contact to input the output from the FEC 7 to demultiplexer 9, which determines a type of a respective packet, using the PID 57, etc., of the header 50, separates only packets of a video, audio, etc., relating to a specified program, and <u>then outputs these packets to the MPEG decoder 10</u>. The multiplexed signal contains a packet called, for example, a PCR (Program Clock Reference) indicative of time information representing the time when compression took place in a broadcasting station concerned. Thus, the clock recovery unit 13 reproduces a data clock 45 using this PCR. The decoder clock 45 reproduced by the clock recovery unit 13 is controlled so as to have the same frequency as a clock used in a compressor (not shown) which compresses video and audio data information in accordance with the MPEG 2 in the broadcasting station. <u>The MPEG decoder 10 expands the respective video and audio signals compressed in accordance with the MPEG 2, etc., by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals. The video signal is converted by the NTSC encoder 11 to a television analog video signal, which is then output from the video output terminal 15. The audio signal is converted by the D/A converter 14 to an analog audio signal, which is then outputted from the audio output terminal 16.</u> <i>Id.</i> at 3:16-41.</p> <p><u>“In reproduction, a signal 153 reproduced by the rotary head 23 is inputted via the playback amplifier 21 to the recording/playback data processing circuit 19, which detects the sync signal 92, signals ID1 (93), ID2 (94), etc., and corrects errors, using the CIP 101, C2P 76, etc., extracts packet data A 99 and packet data B 100, and then sends those data to the packet control circuit 18. The packet control circuit 18 outputs the respective packets at the same intervals of time as in the recording</u></p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<p><u>in accordance with the time stamp 102 added when the data was recorded</u>, and then sends those packets via the interface 12 to the playback changeover switch 8. When a reproduced picture is to be obtained, the playback changeover switch 8 is set at the contact b to thereby send a reproduced packet to the demultiplexer 9. The demultiplexer 9 automatically selects a broadcasting station on the basis of the packet of program information which was selected and converted by the interface 12 when the data was recorded, and <u>outputs only a packet required for the MPEG decoder 10</u>. Video/audio signals are obtained in a manner similar to that in which an output is obtained from a broadcasting signal.” <i>Id.</i> at 4:16-35.</p> <p>“Also, in playback, <u>the data clock 45 used in the MPEG decoder 10 is required to obtain the same frequency as it was compressed in the broadcasting station</u>. To this end, <u>at least the respective PCR time intervals inputted when recorded are required to be maintained, reproduced and outputted correctly</u>. To this end, in recording, <u>the time stamp 102 is added in the packet control circuit 18</u>. In playback, <u>the respective packets are outputted by the packet control circuit 18 in accordance with the time stamps 102 to maintain the time intervals at which the packets are outputted</u>. To this end, <u>clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13</u>. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18.” <i>Id.</i> at 4:36-50.</p> <p>“<u>In playback</u>, the user selects one of the digital and analog broadcasts, <u>the demultiplexer 9 selects only one of the digital and analog broadcasts on the basis of the PAT converted in the recording</u>, and inputs the selected</p>

'945 Claim Element	Hatanaka (Ex. 1006) and Hoogenboom (Ex. 1009) and Anderson (Ex. 1010) ²
	<u>program packet to the MPEG decoder 10 to obtain the video and audio of the desired program.</u> ” <i>Id.</i> at 6:47-52. “This prior art system is capable of recording/playing back an incoming digital signal as it is” <i>Id.</i> at 1:21-22. <i>See also id.</i> at FIGS. 1-7, 9, 10. <i>See also</i> Ex. 1011, Suppl. Schonfeld Decl., at ¶¶132-139.

VIII. CONCLUSION

Substantial, new, and noncumulative technical teachings have been presented for each of claim 21. For these reasons, and the disclosures identified in the claim charts above, the references above teach and suggest the subject matter of the '945 Patent in such a manner that the Petitioner is likely to prevail in challenging the patentability of claim 21. Accordingly, the Petitioner requests that the Board grant this petition for *inter partes* review on all grounds.

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on this 24th day of July, 2015, a copy of the attached PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,095,945, together with all exhibits, the power of attorney, and all other papers filed therewith was served by UPS on the attorneys of record for the patent owner, with a courtesy copy of the petition by electronic mail to the attorneys of record in IPR2015-00321, at the following addresses:

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