

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

LG ELECTRONICS, INC.  
Petitioner,

v.

ATI TECHNOLOGIES ULC,  
Patent Owner.

---

Case IPR2015-00321  
Patent 7,095,945 B1

---

Before BRIAN J. McNAMARA, RAMA G. ELLURU, and  
JAMES B. ARPIN, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## BACKGROUND

LG Electronics, Inc. (“Petitioner”) filed a petition, Paper 2 (“Pet.”), to institute an *inter partes* review of claims 18 and 21 (the “challenged claims”) of U.S. Patent No. 7,095,945 B1 (Ex. 1001, “the ’945 Patent”). 35 U.S.C. § 311. Petitioner identifies LG Electronics U.S.A., Inc. and LG Electronics MobileComm U.S.A. as real parties-in-interest with Petitioner. Pet. 1. ATI Technologies ULC (“Patent Owner”) filed a Preliminary Response, Paper 19 (“Prelim. Resp.”) contending that the petition should be denied as to all challenged claims. We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we institute *inter partes* review. Specifically, we institute a trial of challenged claim 18 on the grounds specified with particularity herein. We decline to institute a trial of challenged claim 21.

## PENDING LITIGATION

The ’945 Patent is the subject of a patent infringement lawsuit brought by Advanced Micro Devices, Inc. in the Northern District of California: *Advanced Micro Devices, Inc., et al., v. LG Electronics, Inc., et al.*, Case No. 3:14-cv-01012.

## THE ’945 PATENT (EXHIBIT 1001)

The ’945 Patent explains that a transport stream (TS) consists of fixed length packets based on a four byte header and 184 bytes of data payload

obtained from larger data blocks. Ex. 1001, col. 1, ll. 61–64. Elementary Streams are packetized into fixed or variable length packetized elementary stream (PES) packets and PES packets are merged to create a program with its own system time clock (STC). *Id.* at col. 1, l. 65–col. 2, l. 9. Elementary streams (ES) within one program have periodic time stamps corresponding to the STC counter to indicate proper timing for each ES. *Id.* at col. 2, ll. 10–12. Figures 1–4 illustrate conventional signal structures. *Id.* at col. 2, ll. 49–50.

The '945 Patent discloses a system and method for displaying multimedia programs in real time and/or storing them for subsequent display, including as a time shifted display in which the stored portion of the program is played back while new portions of the program are being stored. Ex. 1001, Abstract. The '945 Patent discloses three modes of operation: (1) a receive only mode, i.e., the Transparent Mode, in which a digital transport stream receiver (DTSR) receives a live broadcast, which is accessed immediately and not saved, *id.* at col. 3, 45–53; (2) a Continuous Time Shifting Mode, in which a received program is stored in the form of full transport stream packets or packetized elementary stream (PES) packets; and (3) a Part-Time Shifting Mode, in which a time shifted program is played at a user defined speed, e.g., fast forward, while the host central processing unit (CPU) receives and stores a real time event. *Id.* at col. 4, ll. 1–8.

Figure 6 is a block diagram of a system using two digital transport stream receivers. *Id.* at col. 2, ll. 54–56. The '945 Patent discloses several programmed embodiments of the Part-Time Shifting mode using this system. *Id.* at col. 6, l. 13–col. 7, l. 48.

### ILLUSTRATIVE CLAIMS

Claims 18 and 21, which are the only claims at issue in this proceeding are reproduced below:

**18.** A method comprising:  
determining a mode of operation;  
during a first mode of operation:  
    receiving a multiplexed packetized data stream at a first demultiplexer;  
    selecting a first program from the multiplexed packetized data stream;  
    decoding a video portion of the first program for display;  
during a second mode of operation:  
    receiving the multiplexed packetized data stream at the first demultiplexer;  
    selecting the first program from the multiplexed packetized data stream;  
    storing the first program;  
during a third mode of operation:  
    receiving the multiplexed packetized data stream at the first demultiplexer;  
    selecting the first program from the multiplexed packetized data stream;  
    storing a first program portion of the first program;  
    providing the first program portion to a second demultiplexer;  
    selecting at the second demultiplexer a video portion of the first program portion;  
    decoding the video portion of the first program portion for display; and  
    storing a second program portion of the first program simultaneous to the step of decoding.

- 21.** A system comprising:
- a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;
  - a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;
  - a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;
  - a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and
  - a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data.

ART CITED IN PETITION

Barton	US 6,233,389 B1	May 15, 2001	(Ex. 1005)
Hatanaka	US 6,397,000 B1	May 28, 2002	(Ex. 1006)
O'Connor	US 6,951,058 B1	Jul. 8, 2003	(Ex. 1007)
Fujinami	US 5,521,922	May 28, 1996	(Ex. 1008)

### BASIS OF PETITION

CLAIMS	BASIS	REFERENCES
18, 21	§102(e)	Barton
18	§103(a)	Hatanaka
21	§102(e)	Hatanaka
18	§103(a)	Hatanaka and O'Connor
21	§103(a)	Fujinami

### CLAIM CONSTRUCTION

Petitioner does not propose constructions for any of the claim terms. Petitioner states that in this case, applying the broadest reasonable construction means that the claim terms should be given their plain meaning. Pet. 5–6.

Patent Owner argues that during the third mode of operation the entirety of the first program is not stored and decoded at once, but is processed in portions. Prelim. Resp. 18. For this reason, Patent Owner contends that the term “program portion” should be construed to mean “less than all of a program.” Prelim. Resp. 19. Patent Owner does not specify how much less than all of a program constitutes a portion.

We are not persuaded by Patent Owner’s proposal because the antecedents in claim 18 convey the necessary meaning. In reciting the first mode of operation, claim 18 recites selecting “a first program” from the received multiplexed packetized data stream. In reciting the second and third modes, claim 18 recites selecting the first program, i.e., the same first program in the recitation of the first mode. In the third mode, claim 18 recites that a first program portion of the first program is stored and a video

portion of that first program portion is decoded for display. Claim 18 further recites that a second program portion of the first program is stored at the same time the video portion of the first program portion is being decoded. Thus, claim 18 recites no limits on the first and second portions, other than each being a portion, i.e., some or all, of the first program.

## ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

### *Challenge To Claim 18 As Anticipated By Barton*

Barton discloses a multimedia time warping system that allows a user to view a television program, with the option of instantly reviewing previous scenes within the program, or to store selected television broadcast programs while simultaneously watching or reviewing another program. Ex. 1005, col. 1, l. 64–col. 2, l. 3, col. 3, ll. 19–26. TV streams are converted to Moving Pictures Experts Group (MPEG) formatted strings and sent to a media switch, e.g., media switch 102. The media switch buffers the MPEG stream into memory and sends the stream to an output section, where it is “written simultaneously to the hard disk or storage device” and, if the user is watching real time TV the stream is sent to the Output Section, which produces a TV signal for display. *Id.* at col. 3, l. 62–col. 4, l. 2. Barton also discloses the use of multiple tuners and decoders so that the media switch can be used “to record one program while the user is watching another,” which “means that a stream can be extracted off the disk while another stream is being stored onto the disk.” *Id.* at col. 4, ll. 14– 22. Features such as a picture-in-picture displays, are implemented with the multiple decoders. *Id.* at col 4, ll. 17–19.

To facilitate searching, each stream is stored as a sequence of fixed size segments with monotonically increasing time stamps. *Id.* at col. 4,

ll. 34–54. A parser identifies a video, audio or private data segment, routes it to the corresponding direct memory access (DMA) engine and simultaneously directs an event to an event DMA engine, which generates an event in an event buffer, where the event type, time stamp and an offset are stored. *Id.* at col. 5, ll. 3–24. The program logic, which knows where the audio, video and private data buffers start, adds the offset to find the event in the stream. *Id.* at col. 5, ll. 24–31. The program logic reads events accumulated in the event buffer when it is interrupted by the media switch, generates a sequence of logical segments that correspond to the parsed MPEG segments, and converts the offset into the actual address of each segment. *Id.* at col. 5, ll. 34–40. The program logic collects logical segments until it reaches a fixed buffer size, when it generates a new buffer (the PES buffer), which is passed on to other logic for decoding or writing to storage media. *Id.* at col. 5, ll. 51–60. If a PES buffer is written to storage, the logical segments are written to the medium in the order in which they appear, thereby gathering the components of the stream into a single linear buffer of stream data that can be read back from the storage medium in a single transfer. *Id.* at col. 6, ll. 2–9.

User control commands affect the flow of the MPEG stream and allow the user to view stored programs in a variety of ways, e.g., fast forward, reverse, play, pause, fast/slow play. *Id.* at col. 2, ll. 33–38.

Petitioner contends that Barton discloses each of the modes recited in claim 18. Pet. 8–18. Petitioner argues that Barton’s description of MPEG streams being received at a first demultiplexer MPEG2 Transport Demultiplexer, and a video program being extracted out and decoded by the MPEG decoder discloses the claimed first mode. Pet. 9. Petitioner further



argues that Barton discloses the second mode because it describes storing the program in a memory device. *Id.* Noting that Barton describes a second demultiplexer, parser 401 and simultaneous storing and decoding, Petitioner argues that Barton discloses the third mode recited in claim 18. *Id.*

Patent Owner counters that Barton's general description of user control commands (including fast forward, play, reverse, etc.) does not disclose explicitly the claimed step of determining the mode of operation, nor does Petitioner advance any argument that determining the mode of operation is inherent. Prelim. Resp. 24–25. We are not persuaded by Patent Owner's argument because Barton specifically states that it allows a user to view a television program, with the option of instantly reviewing previous scenes within the program, or to store selected television broadcast programs while simultaneously watching or reviewing another program. Ex. 1005, col. 1, l. 64–col. 2, l. 3, col. 3, ll. 19–26. In order to perform these functions, we are persuaded that the system in Barton determines its mode of operation.

Patent Owner next argues that Petitioner fails to establish that Barton discloses storing a second program portion of the first program simultaneous to the step of decoding. Prelim. Resp. 25–28. According to Patent Owner, Barton's disclosure of parsing an MPEG stream, storing its video and audio components in temporary buffers and then on a storage device, extracting the components from the storage device, and reassembling the components into an MPEG stream, indicates that Barton always stores an entire program prior to displaying any portion of the program. *Id.* at 26. Patent Owner does not explain why such a sequence precludes storing and retrieving portions of a program in progress. Patent Owner references Figure 2 of Barton in which a media switch is connected to several input and output modules as evidence

that Barton only allows a user to store a selected television program while viewing another, different program. *Id.* at 26–27. However, Patent Owner does not explain how this feature of Barton precludes viewing a first portion of a program and storing a second portion of the program. As discussed above, Barton purports to “allow[s] the user to view a television program broadcast program with the option of instantly reviewing previous scenes within the program.” Ex. 1005, col. 1, ll. 65–67.

Patent Owner further contends that claim 18 recites that the decoding of the first program portion occurs simultaneously with the storing of the second program portion, while in Barton the decoding occurs *after* the stream is received by the Output Section and written to the storage device. Prelim. Resp. 28. Petitioner notes that Barton discloses a media switch that buffers the MPEG stream into memory and “performs two operations if the user is watching real time TV: the stream is sent to an output section 103 and it is written simultaneously to the hard disk or storage device 105. The Output Section 103 takes the MPEG streams as input and produces an analog TV signal . . . as required by TV standards” Pet. 17, (citing Ex. 1005, col. 3, l. 62–col. 4, l. 2). There is a finite amount of time for the stream to be received by both the storage device and the output section and a finite amount of time for the storage device to store the stream and the output section to decode it. For purposes of this Decision, we are persuaded that Barton’s simultaneous transmission of the stream to the output section for decoding and writing it to the storage device meets the limitation that the decoding of the first program portion occurs simultaneously.

This disclosure cited by Petitioner, however, concerns how Barton stores the first program portion of the first program. Petitioner does not

establish where Barton discloses storing a second program portion of the first program. Petitioner's references to Figure 2 concern how the media switch can be used record one program while watching another, rather than storing a second program portion of the first program, as recited in claim 18. Pet. 17 (citing Ex. 1005, col. 4, ll. 14–23, 34–44). Petitioner also cites Barton's disclosure of the media switch taking in 8 bit data and sending it to the disk while simultaneously extracting another stream of data off the disk and sending it to the decoder, with all of the DMA engines being capable of working at the same time. *Id.* at 18 (citing Ex. 1005, col. 7, ll. 5–9). However, neither the Petition nor the Declaration of Dan Schonfeld (Ex. 1004, "Schonfeld Decl.") describes how Barton describes storing a second program portion of the first program. Pet. 18 (citing Schonfeld Decl. ¶¶ 115–116). Thus, we agree with Patent Owner that Petitioner has not demonstrated that Barton anticipates storing a second portion of the first program. We therefore decline to institute a trial based on Petitioner's challenge to claim 18 as anticipated by Barton under 35 U.S.C. § 102.

*Challenge to Claim 21 As Anticipated by Barton*

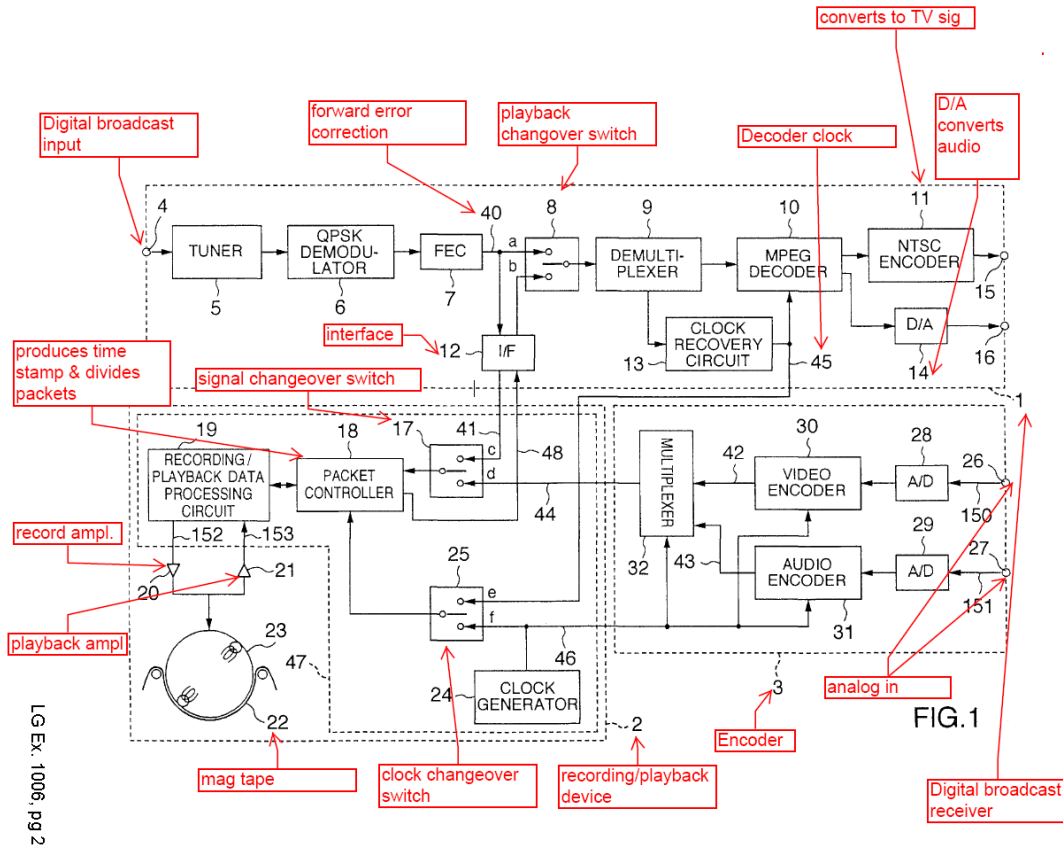
Turning to claim 21, we note that it is unclear whether the phrase "before the select packets are stored in the storage device" means that the received timing information is transmitted in the packets before they are stored, or that the clock recovery module generates a clock before the select packets are stored in the storage device. Petitioner assumes the latter meaning, arguing that Barton "discloses generating a clock prior to storage because time stamps are associated with each segment at the media switch 102 prior to storage in the memory device 104." Pet. 9. Petitioner also

contends that real-time applications in Barton inherently disclose extracting timing information prior to storage. *Id.*

Patent Owner notes that claim 21 requires a first clock recovery module that generates a clock “***based upon received timing information transmitted in packets of multiplexed packetized data stream*** before the selected packets are stored in the storage device.” Prelim Resp. 30. Patent Owner contrasts this received timing information with Barton, which enables the program logic to associate time sequence information with each segment, for example by embedding it into the stream based on the time the system boots up. Prelim Resp. 30–31. Although the Schonfeld Declaration referenced in the Petition includes several paragraphs arguing that the clock generation approach in the ’945 Patent and Barton are similar, these arguments are not advanced in the Petition. Each petition . . . must include . . . [a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.” 37 C.F. R. §42.22(a)(2). In this case, the Petition omits any adequate explanation of how Barton supports Petitioner's challenges. Instead, the Petition includes claim charts that merely cite portions of the references, together with citations to the Schonfeld Declaration. Therefore, we decline to institute a trial on Petitioner’s challenge to claim 21 as anticipated by Barton because the information presented in the Petition fails to show there is a reasonable likelihood Petitioner would prevail on this challenge. *See, ZTE (USA), Inc., and Huawei Device USA, Inc. v. Electronics and Telecommunications Research Institute*, Case IPR2015-00028 (PTAB Apr. 30, 2015)(Paper 14).

*Challenge to Claim 21As Anticipated By Hatanaka*

Petitioner challenges claim 21 as anticipated by Hatanaka and claim 18 as obvious over Hatanaka. Below is an annotated version of Figure 1 of Hatanaka:



Annotated version of Figure 1 of Hatanaka

As shown in Figure 1, Hatanaka discloses a system with digital broadcast receiver 1 that provides an NTSC encoded television video output and an analog audio output, analog receiver/encoder 3, and recording/playback device 2. Ex. 1006, col. 2, ll. 30–50, Fig. 1. The status of playback changeover switch 8, signal changeover switch 17, and clock changeover switch 25 control signal routing. *Id.* Fig. 1. For example, when

playback changeover switch 8 is set to “a” the digital broadcast received at input 4 is routed to the MPEG decoder 10, and the clock recovery circuit 13 is controlled to have the same frequency as a clock (the program reference clock (“PRC”)) used in compressing the video at the broadcast station. *Id.* at col. 3, ll. 7–41. If the received signal is recorded, changeover switch 17 is set at “c” and packet control circuit 18 divides received 188 byte packet data into a ninety-two byte packet and a ninety-six byte packet, and adds a time stamp. *Id.* at col. 3, ll. 42–63. Clock changeover switch 25 is set to “e,” so that decoder clock 45 is input to packet control circuit 18. *Id.* at col. 4, ll. 48–50. In playback the respective packets are output by packet control circuit 18 in accordance with the time stamps. *Id.* at col. 4, ll. 43–45.

During reproduction, packet control circuit 18 cannot use decoder clock 45, so clock changeover switch 25 is set to “f,” so that clock generator 24 provides fixed clock 46 to packet control circuit 18 and a packet is output at time generated by fixed clock 46, allowing clock recovery circuit 13 to generate a stable clock. *Id.* at col. 4, ll. 51–64. When an analog video and audio are received, encoders 30 and 31 and multiplexer 32, which adds signals to comply with MPEG2 standards, deliver multiplexed stream 44, similar to that of the output of interface 12 of digital broadcast receiver 1, to packet control circuit 18 by setting signal changeover switch 17 to “d”. *Id.* at col. 5, ll. 1–67. During recording and playback of the received analog audio and video, clock changeover switch 25 is set to “f” so that packet control circuit 18 uses fixed clock 46. *Id.* at col. 6, ll. 8–15.

Petitioner contends that Hatanaka discloses each and every element of claim 21 of the ’945 Patent. Pet. 38–49. Petitioner specifically argues that Hatanaka discloses a predefined packet identifier (“PID”) 57 and clock

recovery prior to storage and that the program clock reference (“PCR”) intervals input when recorded are maintained by adding time stamp 102 in packet control circuit 18. Pet. 39–39. Petitioner further argues that Hatanaka also discloses real time applications, which inherently discloses extracting timing information prior to storage. *Id.* at 39. Petitioner cites paragraphs 200–204 and 211–217 of the Schonfeld Declaration, but does not include these arguments in the Petition. *Id.* at 38–39. Aside from quoting passages of Hatanaka in its claim charts, the Petition provides no further explanation of how Hatanaka anticipates claim 21.

Patent Owner contends that Hatanaka fails to disclose the limitation in claim 21 “wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device.” Prelim. Resp. 31. With respect to this limitation Petitioner references the Schonfeld Declaration, which states that the generation of a clock based upon received timing information transmitted in packets of the multiplexed data packet stream occurs before the packets are stored in the storage device. Pet. 39 (citing Ex. 1004 ¶214). Patent Owner argues that it is possible in Hatanaka to store the packets prior to performing operations on the packets, including generating a clock (Prelim. Resp. 32), and that Hatanaka never expressly discloses any timing order between its generation of a clock and the storage of select packets by either the annotated storage unit portion of Fig. 1, demultiplexer 9, or multiplexer 32 (*id.* at 34).

The clock recovery module recited in claim 21 is coupled to the input node and generates a clock at an output based upon received timing

information in packets of the data stream before the select packets are stored in the storage device. As discussed above, Hatanaka discloses that when a digital broadcast is being recorded, i.e., signal changeover switch 17 set to “c,” packet control circuit 18 splits the received 188 byte stream into ninety-two byte packet data A 99 and ninety-six byte packet data B 100. Packet control circuit 18 adds to ninety-two byte packet data A 99, a four byte packet header 98, which includes time stamp 102 indicating a time when the packet is received. Ex. 1006, col. 3, ll. 50–63, Fig. 3A. During recording, in which the clock changeover switch 25 is set to “e,” decoder clock 45, produced by clock recovery circuit 13, is provided to packet changeover circuit 18 for use in producing time stamp 102. *Id.* at col. 4, ll. 45–50.

Petitioner contends that clock recovery unit 13 of Hatanaka is the claimed clock recovery module. Pet. 45–46. The Petition does not explain how the production of a time stamp prior to storing the packets teaches generation of a clock, as claimed. Hatanaka discloses that in playback, the time stamps maintain time intervals at which the packets are output, *id.* at col. 4, ll. 43–45, but, in reproduction, the digital broadcasting receiver is operated by a timing signal from packet control circuit 18, to produce decoder clock 45, *id.* at col. 4, ll. 51–54. Because packet control circuit 18 cannot use decoder clock 45, clock changeover switch 25 is set to “f,” so that clock generator 24 provides fixed clock 46 to packet control circuit 18. *Id.* at 51–59. Packets are output at a timing generated by fixed clock 46 and clock recovery unit 13 generates a stable clock based on fixed clock 46. *Id.* at col. 4, ll. 59–60. The Petition does not address how the generation of a stable clock by clock recovery module from clock 46 constitutes the limitations recited in claim 21 of the ’945 Patent. Thus, we are not



persuaded that Petitioner has demonstrated it is reasonable likely to prevail in its challenge to claim 2 as anticipated by Hatanaka, and we decline to institute a trial on this ground.

*Challenge to Claim 18 As Obvious Over Hatanaka*

Petitioner contends that claim 18 is unpatentable under 35 U.S. § 103 over Hatanaka. According to Petitioner, “simultaneous storing and decoding would have been obvious to one of ordinary skill in the art in view of Hatanaka because Hatanaka discloses a system that allows one to simultaneously record different portions of a program.” Pet. 26. Petitioner cites paragraphs 188–191 of the Schonfeld declaration in support of this proposition. *Id.* The Schonfeld Declaration quotes from substantially the same portions of Hatanaka that Petitioner cites in its claim charts, (Ex. 1004 ¶¶ 189–190, Pet. 37–38), and without further analysis states would have been obvious to one of ordinary skill (Ex. 1004, ¶¶188, 191).

In response, Patent Owner first contends that Hatanaka does not disclose “determining a mode of operation.” Prelim. Resp. 38–39. We were not persuaded by a similar argument made by Patent Owner concerning Barton, as discussed above. Patent Owner contends that Hatanaka discloses only determining a respective type of packet (video, audio, etc.) but does not disclose determining the mode of operation. *Id.* However, Hatanaka discloses operating based on the state of various switches, including playback changeover switch 8. Thus, we are not persuaded it would not have been obvious to determine the mode of operation in Hatanaka.

Patent Owner next contends that Petitioner’s declarant’s assertion is conclusory and not supported by Hatanaka because Hatanaka never discloses simultaneous storing and decoding of program portions. Prelim. Resp. 41.

Patent Owner emphasizes that Hatanaka, therefore, does not disclose the claim limitation of “storing a second program portion of the first program simultaneous to the step of decoding.” *Id.* at 41–42. Patent Owner argues that Hatanaka “never disclosed when storage of its packets of video and audio information occurs in relation to decoding of any data at its MPEG decoder” and that, at most, Hatanaka discloses storing audio and video components prior to decoding. *Id.* at 41. However, Patent Owner does not identify any disclosure in Hatanaka that precludes storing a second program portion of the first program simultaneous to the step of decoding. The portions of Hatanaka that Petitioner cites in its claim charts and the Schonfeld Declaration describe the recording and playback of broadcasts in Hatanaka and indicate that playback can occur during recording. Hatanaka is silent about what information is being retrieved from the storage medium and played back at the same time that a program is being recorded.

Although Hatanaka does not explicitly state a first portion of a first program can be decoded at the same time a second portion of the first program is being recorded, the current record does not indicate that Hatanaka excludes this mode of operation or that it would not be obvious to one of ordinary skill in the art. Thus, on the current record, for purposes of this Decision, we are persuaded that Petitioner has demonstrated a reasonable likelihood of succeeding in its challenge to claim 18 as obvious over Hatanaka and we institute a trial on that ground.

*Challenge to Claim 18 As Obvious Over Hatanaka and O’Connor*

Petitioner further contends the combination of Hatanaka and O’Connor discloses “storing a second program portion of the first program simultaneous to the step of decoding” because O’Connor specifically

describes the benefits of a user watching a show, pausing it, and resuming viewing after an interruption. Pet. 49–50 (citing Ex. 1007, col. 11, l. 58–col. 12, l. 10). Patent Owner responds that O’Connor does not disclose the actual operation of its decoding and that, even if O’Connor’s playback includes decoding, Hatanaka does not disclose anything about the timing of decoding operations in relation to storage. Prelim. Resp. 43. Patent Owner further argues that Petitioner’s declarant provides only conclusory statements as a rational for the proposed modification or combination of the prior art, without identifying how the techniques taught in O’Connor might have been used by one of ordinary skill to improve video streaming devices or the video streaming device of Hatanaka. *Id.* at 45–46.

The relevance of O’Connor to the subject matter at issue in this matter, however, is evidenced in its title: “Time Shifting By Concurrently Recording And Playing A Data Stream.” O’Connor discloses a system in which a video stream is recorded simultaneously and retrieved from the storage unit for immediate playback or delayed playback. Ex. 1007, col. 3, ll. 23–28, 33–40; col. 3, l. 62–col. 4, l. 4. In describing a “catch-up” mode, in which a retrieved video is played at higher speed until it catches up with a live broadcast, O’Connor also discloses a bypass in which, upon catch up, recording can be terminated and the incoming video stream can be provided to the video output directly. *Id.* at col. 5, ll. 49–67. Petitioner’s declarant, Dr. Schonfeld cites to similar disclosures in O’Connor. Ex. 1004 ¶ 247 (citing Ex. 1007, col. 5 ll. 19–33).

In view of the disclosures in O’Connor, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its

challenge to claim 18 as obvious over the combination of Hatanaka and O'Connor and we institute a trial on this challenge.

*Challenge to Claim 21 As Obvious over Fujinama*

Petitioner contends that claim 21 is obvious under 35 U.S.C. § 103 over Fujinama. Petitioner notes that in Fujinama, packetized multiplex data streams containing a packet header are supplied to data demultiplexer 5 and extracted video and audio data are stored in video and audio buffers 6 and 8, respectively. Pet. 54. According to Petitioner, the stored video and audio data are next supplied to video and audio decoders 7 and 9, respectively, along with a start signal generated by comparators 23 and 25. *Id.* (citing Ex. 1008, col. 2, ll. 6–15; Schonfeld Decl. ¶254). Petitioner then asserts that it would have been obvious to a person of ordinary skill to use stored timing information as the clock generated at the output. *Id.* (citing Ex. 1008, col. 2, ll. 28–41, 53–59, Schonfeld Decl. ¶¶ 271–281, 284). Petitioner contends that the system time clock is generated based on received timing information in the packetized data stream before the packets are stored in the storage device. *Id.* at 54–55 (citing Ex. 1008, col. 9, ll. 40–55; Schonfeld Decl. ¶¶ 285–86).

Patent Owner contends that Fujinama does not relate to real-time applications, but instead is directed to a data demultiplexer adapted for reproducing time-division multiplex data recorded on an optical disk. Prelim. Resp. (citing Ex. 1008, col. 1, ll. 4–7). Patent Owner further argues that in Fijunami, audio and video data are stored prior to generation of a clock because storage is the first operation performed by the system. *Id.* at 50 (citing Ex. 1008, col. 7, ll. 39–42). Thus, Patent Owner maintains that Fujunami does not disclose the claimed feature “wherein the first clock

recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device,” as required by claim 21. *Id.* at 48.

Fujinama discloses a data demultiplexer in which video and audio data are input fast in order to enhance responsiveness at the start of reproduction. Ex. 1008, Abstract. Fujinama’s demultiplexer separates multiplexed data, including video and audio encoded data and timing data indicative of a video and audio decoding start time, and a system clock reference time, into component data. *Id.* Comparators compare the input timing data with reference timing data and, when the timing data indicative of a video and an audio decoding start time are input, the video and audio data are written to a video code buffer and an audio code buffer, respectively, at a maximum transfer rate. *Id.* During this time period the reference timing data indicative of the current time is monitored. *Id.* Video and audio decoding begins when the reference timing data equals the video and audio timing data. *Id.* Comparing itself with the operation of a conventional system, Fujinama states that in a conventional system the period from a received system clock reference (SCR) to a received decode time stamp (DTS) is calculated by counting clock pulses of a fixed frequency and the data is written to the video code buffer during this period. *Id.* at col. 9, ll. 40–45. However, in Fujinama, the data is written to the video code buffer at the maximum transfer rate when the DTS of a desired picture is input, then the SCR of the data stored in the buffer is compared with the DTS successively, so that a decision can be made about whether a required amount of data for decoding the relevant picture has been written.

*Id.* at col. 9, ll. 46–55. Thus, Fujinama uses the clocks to store information quickly and determine whether sufficient information has been stored to generate a picture. Although Petitioner asserts that this description in Fujinama discloses that the system time clock is generated based on received timing information in the packetized data stream before the packets are stored in the storage device, Petitioner does not explain this contention. Pet. 54–55. Thus, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of succeeding in its challenge to claim 21 as obvious over Fujinama.

#### SUMMARY

We institute a trial as to the following grounds asserted under 35 U.S.C. § 103:

Claim 18 as obvious of Hatanaka;

Claim 18 as obvious over the combination of Hatanaka and O'Connor.

We do not institute a trial on any other claims or grounds.

#### ORDER

In consideration of the foregoing, it is hereby:

**ORDERED** that *inter partes* review is instituted as to the following grounds asserted under 35 U.S.C. § 103:

Claim 18 as obvious of Hatanaka; and

Claim 18 as obvious over the combination of Hatanaka and O'Connor;

**FURTHER ORDERED** that pursuant to 35 U.S.C. § 314(a) an *inter partes* review of the '945 Patent is hereby instituted, commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

**FURTHER ORDERED** that the trial is limited to the grounds identified in the above ORDER, and no other grounds are authorized.

**FURTHER ORDERED** that an initial conference call with the Board is scheduled for the date and time in the accompanying Scheduling Order. The parties are directed to the Office Trial Practice Guide, 77 Fed. Reg. 48756, 48765-66 (Aug. 14, 2012) for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the scheduling order entered herewith and any motions the parties anticipate filing during the trial.

IPR2015-00321  
Patent 7,095,945 B1

PETITIONER:

Robert G. Pluta  
Amanda Streff  
MAYER BROWN LLP  
rpluta@mayerbrown.com  
astreff@mayerbrown.com

PATENT OWNER:

Michael B. Ray  
Lestin Kenton  
Michael D. Specht  
STERNE KESSLER GOLDSTEIN & FOX, PLLC  
mray@skgf.com  
lkenton@skgf.com  
mspecht@skgf.com