UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.
Petitioner,

v.

ATI TECHNOLOGIES ULC
Patent Owner.

Case IPR2015-01620
Patent 7,095,945 B1

PATENT OWNER PRELIMINARY RESPONSE

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Exhibit List

Exhibit Number	Document Description
2001	Invalidity Contentions served by Counsel for LG Electronics, Inc. *et al.*, dated October 2, 2014, Case No. 3:14-cv-1012-SI
2002	Exhibit I-01 (945) US5517250 - Hoogenboom Service Chart
2003	IPR2015-00321, Institution Decision, Paper No. 20
2004	"A consumer digital VCR for digital broadcasting" by Hatanaka et al. (1998)
2005	"A consumer digital VCR for advanced television" by Okamoto et al. (1993)
2006	"A consumer digital VCR for digital broadcasting" by Okamoto et al. (1995)

I. INTRODUCTION

Patent Owner, ATI Technologies ULC (hereafter "Patent Owner"), hereby respectfully submits this Patent Owner Preliminary Response. This filing is timely under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.120, because it was filed by November 6, 2015.

This is the second of two IPR petitions that Petitioner LG Electronics, Inc. (hereafter "LG") has filed against Patent Owner's U.S. Patent 7,095,945 ("the ''945 patent"[1]). The Board should deny institution, because: (i) this Petition is time-barred; (ii) this Petition is redundant; and (iii) LG still has not shown a reasonable likelihood that it would prevail with respect to claim 21.

First, the Board should exercise its discretion and deny LG's second Petition against the '945 patent, because LG is time-barred from bringing this Petition under 35 U.S.C. § 315(b). This Petition was filed more than a year after LG was served with a complaint alleging infringement of the '945 Patent. On July 24, 2015, more than sixteen months after Patent Owner served LG with the complaint (and after previously failing in its challenge of claim 21 in IPR2015-00321), LG filed this second Petition for *inter partes* review of the '945 Patent. Paper 2. LG also filed a motion to join this proceeding with IPR2015-00321. Paper 3. Patent Owner opposed that motion. Paper 7. LG seeks joinder in an effort to circumvent

[1] IPR2015-00321 was filed on December 10, 2014.

the § 315(b) one-year statutory bar.

The Board should exercise its discretion and deny this second Petition. The Board has repeatedly denied joinder where a petitioner attempts, as is the case here, to use a prior institution decision as a roadmap to remedy unsuccessful challenges advanced in a first petition. The Board has been especially critical of such tactics by petitioners when the follow up petition would be time-barred under § 315(b), absent joinder. *See, e.g., Medtronic, Inc. et al. v. Endotach LLC*, IPR2014-00695, Paper 18, pp. 3-4 (P.T.A.B. Sept. 25, 2014).

Second, LG's second Petition and first Petition are redundant. LG has already failed to get trial instituted on three grounds of rejection against claim 21 in its first Petition. LG now proposes two more grounds of rejection without explaining how this second Petition is not an improper circumvention of the IPR rules. Hence, consistent with previous Board rulings, the Board should also find this second Petition redundant.

Finally, after failing in its initial challenge of claim 21, LG still has not established a reasonable likelihood of prevailing with any of its new proposed grounds against claim 21. LG has not shown how Hatanaka in combination with either Hoogenboom or Anderson renders claim 21 obvious. Although LG has advanced Hoogenboom and Anderson specifically to address the shortcomings identified in its first Petition against the '945 patent, Hatanaka still suffers from

several deficiencies which are not cured by either Hoogenboom or Anderson. For example, Hatanaka does not teach (i) "a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets," (ii) "a decoder having … a second input coupled to the dataport of the storage device to receive the select packets..." or (iii) "a first clock recovery module … wherein the first clock recovery module is to generate a clock … before the select packets are stored in the storage device," as required by claim 21.

Regarding, the first two features, Hatanaka's system is structurally different from claim 21. FIG.1 of Hatanaka demonstrates that Hatanaka's storage device: (i) does not have a data port coupled to the output of demultiplexer 9—the alleged first transport stream demultiplexer; and (ii) does not receive the select packets selected by Hatanaka's alleged first transport stream demultiplexer. Additionally, Hatanaka's MPEG decoder 10 does not have a second input coupled to the data port of the storage device to receive the select packets. LG does not and cannot rely on Hoogenboom or Anderson to teach these features, because Hoogenboom and Anderson, similar to Hatanaka, also disclose systems that are structurally different from claim 21.

Regarding the third feature, on one hand, LG appears to maintain that Hatanaka discloses "a first clock recovery module … wherein the first clock

recovery module is to generate a clock … before the select packets are stored in the storage device"— an argument that failed in its first Petition. And, on the other hand, LG advances two new obviousness grounds, alleging that Hoogenboom and Anderson cure the previously identified deficiencies of Hatanaka. But Hoogenboom and Anderson fail to remedy Hatanaka's deficiencies.

LG fails to address the shortcomings of Hatanaka's disclosure. A careful reading and proper analysis of Hatanaka reveals that Hatanaka is a severely limited system. Hatanaka discloses a digital VCR, and its structural arrangement would have presented significant challenges to anyone attempting to modify Hatanaka to include different functionality, such as Hoogenboom's video decompressor. A system resulting from the combination of Hatanaka and Hoogenboom could not have been arranged in the manner of claim 21 without making extensive non-obvious modifications—modifications that would have only been realized by looking at the teachings of the '945 patent.

Moreover, Anderson does not disclose generating a clock at the output before the select packets are stored in the storage device. So, in an attempt to reconstruct the invention of claim 21, LG points to an irrelevant operation performed by Anderson's system—table filtering—and alleges that it would have been obvious to perform clock recovery in the same manner. LG's reasoning, however, is nonsensical, because: (i) Anderson does not provide any link between

table filtering and clock recovery, and (ii) LG's rationale for obviousness is filled with improper hindsight—relying on the '945 patent as a guide to pick and choose disparate teachings of Anderson and Hatanaka in an attempt to arrive at the claimed system. Accordingly, the Board should deny institution.

II. BACKGROUND

A. '945 patent overview

The '945 patent provides a novel approach to time-shifting, employing multiplexed packetized data streams carrying real-time multimedia programs. '945 patent at Abstract. The '945 patent teaches a system for video program time-shifting using reduced storage and CPU resource requirements as compared to the prior art.

A problem addressed by the '945 patent is that time-shifting a digital signal typically required the capture and storage of large data files. A few minutes of a stored digital signal "require[d] a large amount of storage space. . . . The digital signal … [could] be compressed to reduce the amount of storage space required. However, compressing a video signal require[d] additional processing power, resulting in additional costs." '945 patent, Ex. 1001, 1:22-27. The '945 patent teaches an innovative and efficient approach for time-shifting digital video data.

B. Claim 21

Claim 21 of the '945 patent is reproduced below:

A system comprising:

a first input node to receive a multiplexed packetized data stream that carries real-time multimedia programs;

a first transport stream demultiplexer having an input coupled to the first input node to select packets of data having a predefined packet identifier and an output to provide the select packets of data;

a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets;

a first clock recovery module having an input coupled to the first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of the multiplexed packetized data stream before the select packets are stored in the storage device; and

a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data. '945 patent, 10:15-38.

Claim 21 recites a system with various components arranged in a particular manner. The specific claimed arrangement between the first input node, first transport steam demultiplexer, storage device, first clock recovery module, and decoder allows for an efficient approach to time-shifting digital video data.

III. A PERSON OF ORDINARY SKILL IN THE ART ("POSA")

Based on the technology disclosed in the '945 patent, one of ordinary skill in the art would have an undergraduate degree in electrical or computer engineering

or a closely related field. Furthermore, such a person would typically have two years of industry experience related to the design and development of multimedia computer systems.

IV. LG'S PETITION IS PROCEDURALLY BARRED

A. LG's second Petition is time barred and LG does not deserve a second bite at the apple.

The Board should deny institution of LG's second Petition, because LG seeks nothing more than "a second bite at the apple"—a second chance to challenge the same claim that was previously challenged and denied by the Board. As previously stated in Patent Owner's Opposition Motion for Joinder, LG is not entitled to use the prior Institution Decision as a roadmap for its second Petition. In arguing that joinder should be granted, LG relies on cases where follow up Petitions were either filed by another party challenging the same claims, or filed by the same party challenging different claims but using the same art advanced in the first proceeding. Neither situation is applicable here. LG is not a different party, and this second Petition advances new art against a claim challenged but not instituted in the IPR2015-00321 trial. Paper 7, at 4-6. Moreover, unlike the cases cited by LG in its Joinder Motion, LG fails to provide a good reason to warrant a "second bite at the apple." Paper 7, at 6-8. Lastly, LG also fails to provide any explanation why it could not have presented Hoogenboom and Anderson in its first Petition. Paper 7, at 8-10. Granting LG's second Petition will therefore run

contrary to 37 C.F.R. § 42.1(b), because it does not promote the "just, speedy, and inexpensive resolution of every proceeding." So institution should be denied.

Further, LG's Response to Patent Owner's Opposition misconstrues the law and fails to address Patent Owner's "second bite at the apple" argument. Contrary to LG's assertions, the cases cited by Patent Owner are not on the "opposite sides of the split regarding joinder of issues under § 315(c)." Paper 8, at 2. Rather, the cases relied upon by LG in support of joinder are misplaced—not one Board decision cited by LG allowed joinder of issues where the petitioner relied on additional references absent good cause.

For example, in *Samsung v. Virginia*, Samsung did not rely on any additional references; all of the references were previously cited in the original petition. *See* IPR2014-00557, Paper 10, at 17-18 (P.T.A.B. Jun. 13, 2014). Moreover, in that proceeding, the additional challenged dependent claims only added one new limitation that was already addressed in a corresponding IPR proceeding. *See Samsung,* Paper 10, at 17-18. Similarly, in *Oxford Nanopore Tech. Ltd. v. Univ. of Washington,* the two proceedings involved the same claim and the same reference, not a different claim and different references as in this proceeding (claim 18 is the only claim left in IPR2015-00321). *See* IPR2015-00057, Paper 10, p. 23 (P.T.A.B. Apr. 27, 2015). Thus, in Samsung and Oxford, petitioners either relied on the same references or challenged the same claims in their subsequent

petitions, unlike LG's second Petition here, which relies on two new references to challenge a claim not currently in the IPR2015-00321 trial.

Further, good cause was provided in *Sony Corp. v. Yissum*, where Sony filed its second petition challenging newly asserted claims (prior to the first institution decision) when patent owner asserted these claims in a concurrent district court litigation after the first petition was filed. *See* IPR2013-00327, Paper 4, at 1-2, 5 (P.T.A.B. Jul. 3, 2013). "Good cause" was also present in *Microsoft Corp. v. Proxyconn,* where the Board granted joinder when the petitioner "proceeded expeditiously in filing a second Petition after learning that additional claims were being asserted" in a corresponding litigation. *See* IPR2013-00109, Paper 15, at 3 (P.T.A.B. Feb. 25, 2013).

No similar good cause was provided by LG to allow a do-over or "second bite at the apple" despite the § 315(b) bar. Nor does any good cause exist. Here, no new claims were asserted against LG after the first Petition, nor was a new threat of infringement present. Accordingly, the Board should deny the second Petition, because LG fails to apprise the Board of any justifiable "reason that merits a second chance." *See Samsung v. Rembrandt*, IPR2015-00555, Paper 20, p. 8 (P.T.A.B. Jun. 19, 2015).

B. The second Petition and LG's first Petition are entirely redundant.

The trial rules are construed "to secure the just, speedy, and inexpensive

resolution of every proceeding." 37 C.F.R. § 42.1(b). LG has an affirmative burden to demonstrate that it is entitled to the relief requested. 37 C.F.R. § 42.20(c). LG has failed to meet its burden here.

The Board has discretion to deny one or more grounds as being redundant with grounds already presented. *Liberty Mut. Ins. Co. v. Progressive Cas. Inc. Co.*, CBM2012-00003, Paper No. 7, p. 2 (P.T.A.B., Oct. 25, 2012). To show that trial should be instituted as to a claim on more than one ground of unpatentability, LG's petition must "articulate [] a meaningful distinction in terms of relative strengths and weaknesses with respect to the application of the prior art disclosures to one or more claim limitations." *Ultratec, Inc. v. Sorenson Commc'ns, Inc.*, IPR2013-00288, Paper No. 23, p. 4 (P.T.A.B., Jan. 10, 2014).

As an expanded panel of nine judges explained, "multiple grounds, which are presented in a redundant manner by a petitioner who makes no meaningful distinction between them, are contrary to the regulatory and statutory mandates, and therefore are not all entitled to consideration." *Liberty Mut. Ins. Co. v. Progressive Cas. Inc. Co.*, CBM2012-00003, Paper No. 7, p. 2 (P.T.A.B. Oct. 25, 2012). This is so because considering multiple redundant grounds "unnecessarily consume[s] the time and resources of all parties involved" and subverts the Board's ability to conduct proceedings in a timely manner. *Illumina, Inc. v. Trs. of Columbia Univ. in the City of New York*, IPR2012-00006, Paper No. 43, p. 12

(P.T.A.B. May 10, 2013).

Indeed, the Board has noted that "35 U.S.C. § 316(b) . . . recognizes, among other things, that *inter partes* review proceedings must be conducted to ensure the ability of the Office to complete timely the proceedings." *Schrader-Bridgeport Int'l, Inc. v. Cont'l Auto. Sys. US, Inc.*, IPR2013-00014, Paper No. 15, p. 4 (P.T.A.B. Apr. 10, 2013). Ultimately, it is LG's burden to explain why its new proposed grounds are not redundant to those presented in LG's first IPR Petition.

This burden includes LG demonstrating why it is entitled to file two petitions challenging the same claim. LG has not met its burden here. The instant Petition is LG's second Petition against the '945 patent. Both petitions challenged claim 21—the first challenge to claim 21 proving to be unsuccessful. And LG has failed to provide a sufficient reason as to why it is now entitled to a second Petition.

LG also fails to identify a single appreciable difference among the references presented in the second Petition versus its first Petition. LG only alleges that the Board did not previously consider the Hoogenboom and Anderson references. However, LG glosses over the fact that its first Petition presented three grounds of rejection against claim 21—based on both anticipation and obvious. Now, LG relies on the Board's decision for the first Petition as a guide, and asks the Board to review two more grounds of rejection based on its first failed attempt—nothing

else. Indeed, LG's second Petition is nothing more than a veiled attempt to circumvent the time-bar, circumvent strict page-limit requirements for IPR proceedings, and also get a second-bite at the apple. Accordingly, for at least these reasons, the Board should find this second Petition redundant with the first Petition and deny institution.

V. LG STILL FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD THAT IT WILL PREVAIL

A. Overview of Hatanaka.

Claim 21 was distinguished over Hatanaka in LG's first Petition. LG now attempts to rely on the Board's non-institution decision for claim 21 as a guide to cure Hatanaka's identified deficiencies with Hoogenboom and Anderson. In order to understand Hatanaka's deficiencies, it is important to delineate the differences between Hatanaka's different modes of operation and recognize how each component plays a role in each mode of operation. An explanation of Hatanaka's different modes of operation and its components is provided below.

Hatanaka describes a digital signal recording and playback device that includes three sub-systems: a digital broadcasting receiving device (Integrated Receiver & Decoder: IRD), a recording and playback device, and an encoder. Hatanaka, Ex. 1006, 2:32-35. Hatanaka's digital signal recording and playback device is illustrated at FIG. 1, reproduced and annotated below:

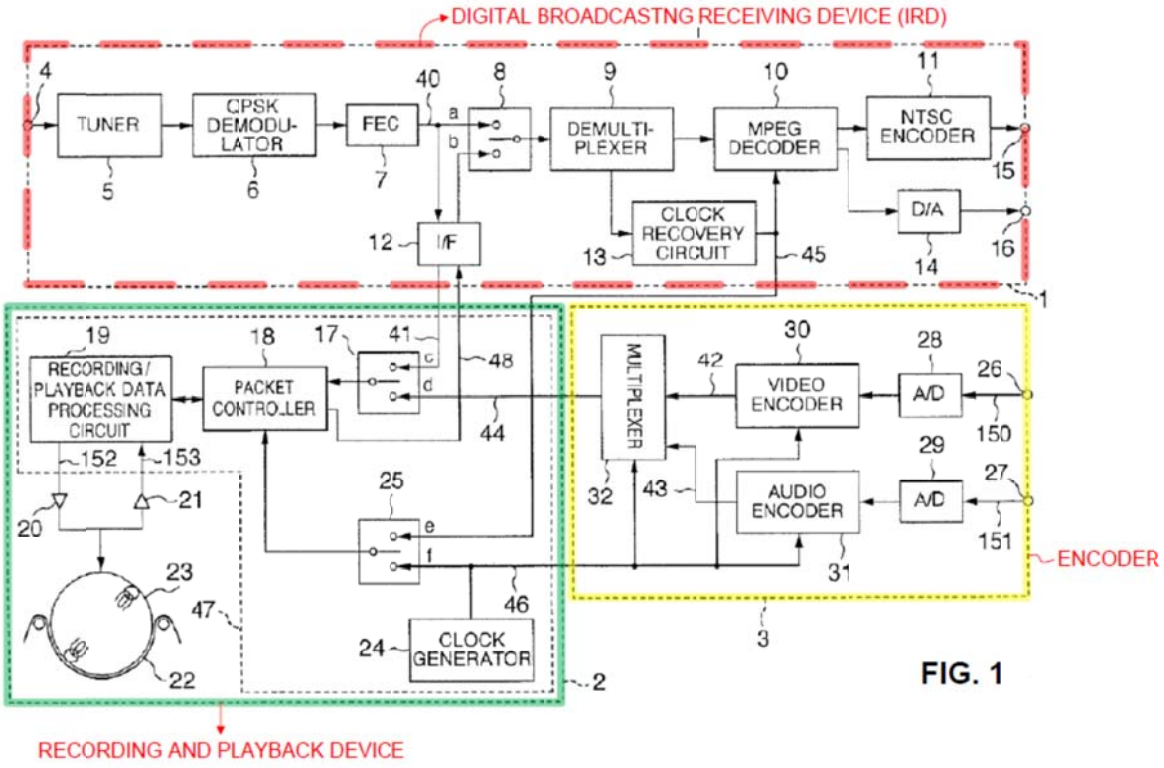


FIG. 1

Hatanaka's IRD and play operation: Hatanaka's IRD—denoted by the red-dashed box in FIG. 1 above—performs Hatanaka's play operation. During Hatanaka's play operation, Hatanaka's IRD receives a digital broadcast stream and displays it without storing the stream. Specifically, Hatanaka's IRD receives a broadcasting signal at tuner 4 and passes the signal to an MPEG decoder 10 (after being processed by QPSK Demodulator 6, FEC 7, Switch 8, and Demultiplexer 9). Hatanaka, 3:7-22.

Demultiplexer 9 "determines a type of a respective packet…, separates only packets of a video, audio, etc., relating to a specified program, and then outputs these packets to the MPEG decoder 10." Hatanaka, 3:19-22. Once MPEG decoder

10 receives the packets of video, audio, etc., MPEG decoder 10 "expands the respective video and audio signals … by using the received separating signal and the data clock 45 reproduced by the clock reproducing unit 13, and provides decoded video/audio signals." Hatanaka, 3:22-41. Next, the video and audio signals are output by Hatanaka's device from respective audio and video terminals. Hatanaka, 3:37-41.

In Hatanaka's FIG. 1, while interface 12 is part of Hatanaka's IRD, it has no role in Hatanaka's play operation. The processing of the digital broadcast stream along the processing path between tuner 5 and the outputs of NTSC encoder 11 and D/A 14 is not influenced in any way by interface 12. The processing path used by Hatanaka's IRD during the play operation is highlighted below.

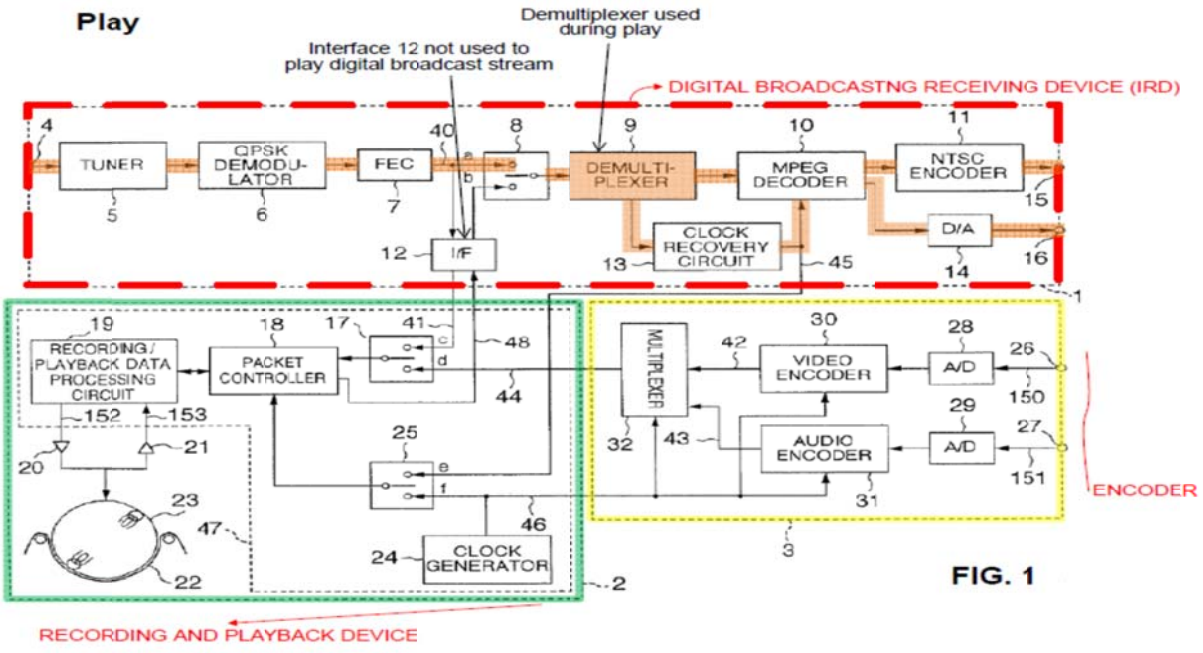
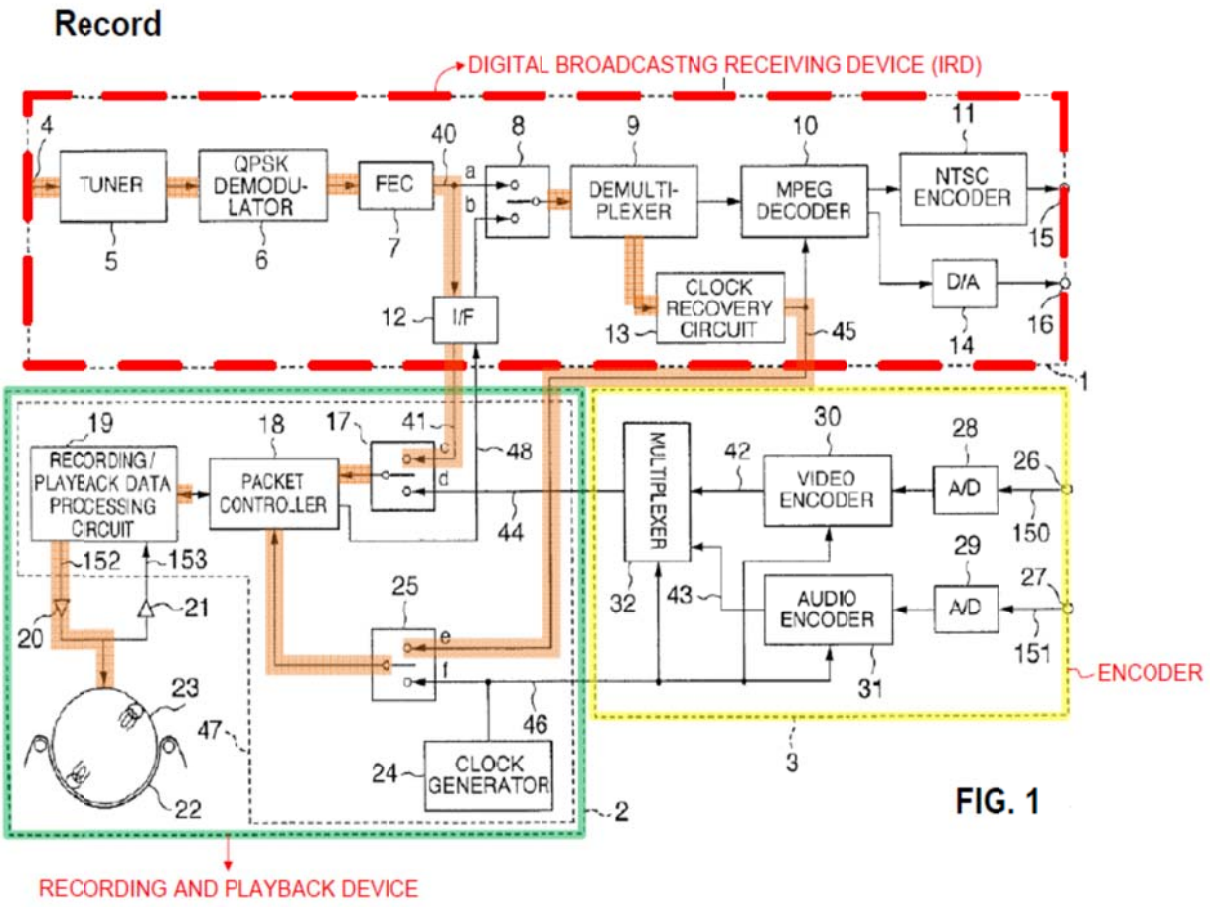


FIG. 1

Hatanaka's Recording and Playback device and record operation: Hatanaka's Recording and Playback device—denoted by the green box in FIG. 1 above—performs Hatanaka's record operation (i.e. storing a program). During Hatanaka's record operation, a digital broadcast signal is received at tuner 5 and the signal is passed to interface 12. Hatanaka, 3:42-54. The information to be recorded is then passed through switch 17, processed by packet controller 18, processed by recording playback data processing circuit 19, and stored in a magnetic tape 22. Hatanaka, 3:42-4:16.

During Hatanaka's record operation, clock changeover switch 25 is set to contact "e", so that decoder clock 45 is passed to the packet control circuit 18. Hatanaka, 4:48-50. Packet controller 18 uses the decoder clock 45 to produce a time stamp for each data packet. Hatanaka, 4:37-49. The time stamp corresponds to the time when the packet is received by Hatanaka's system. Hatanaka, 3:61-63. The processing path used during Hatanaka's record operation is shown highlighted below:



Hatanaka's Recording and Playback device and playback operation:

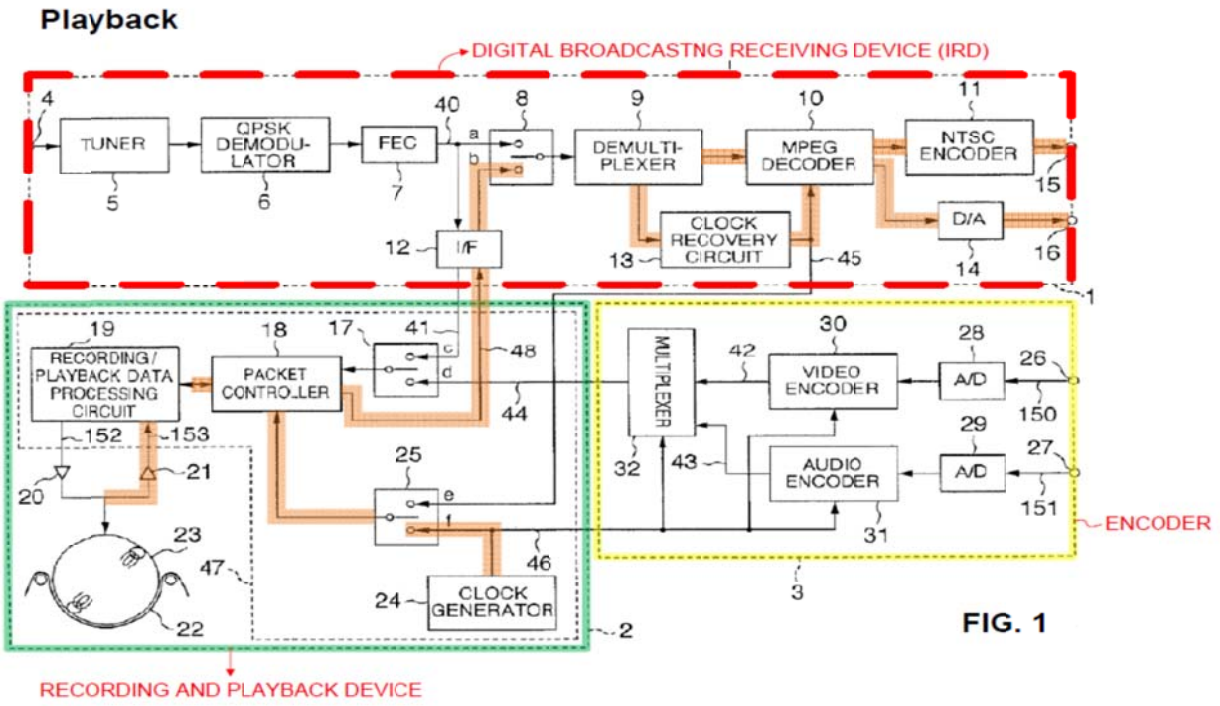
Hatanaka's recording and playback device is also responsible for playback of a digital broadcasting signal. Hatanaka, 4:16-64. Hatanaka's playback is the process of retrieving a previously stored program from the magnetic tape and decoding the retrieved program for display. Hatanaka uses the terms playback and reproduction interchangeably. *See* generally Hatanaka, 4:16-64. Hatanaka's playback operation is different from Hatanaka's play operation, discussed above. While, Hatanaka's play operation does not require storing programs from a transport stream, Hatanaka's playback operation requires prior storage of a program. It first

requires storing a program and then retrieving the stored program for subsequent decoding and displaying.

Hatanaka's playback operation operates as follows: "a signal 153 reproduced by the rotary head 23 is inputted via the playback amplifier 21 to the recording/playback data processing circuit 19" which extracts packets of data and "sends those data to the packet control circuit 18." Hatanaka, 4:16-22. Once the retrieved packets of data are received by packet control circuit 18, "[t]he packet control circuit 18 outputs the respective packets at the same intervals of time as in the recording in accordance with the time stamp 102 added when the data was recorded, and then sends those packets via the interface 12 to the playback changeover switch 8." Hatanaka, 4:22-35. Thereafter, the packets are sent to MPEG decoder 10 for decoding and display. Hatanaka, 4:30-36.

Hatanaka explains that, during playback, its packet controller circuit 18 cannot use the decoder clock produced by the clock recovery circuit 13. Hatanaka, 4:51-64. Instead, packet controller 18 uses a fixed clock generated by clock generator 24. Hatanaka, 4:51-64. Specifically, during Hatanaka's playback operation, switch 25 is set to contact "f", so that a fixed clock 46 is passed to the packet control circuit 18. Hatanaka, 4:51-64. This is in contrast to Hatanaka's record operation, where switch 25 is set to contact "e" and decoder clock 45 is passed to packet controller 18. Hatanaka, 4:48-50.

The processing path used during Hatanaka's playback operation is shown highlighted below:



Hatanaka discloses a digital VCR: A POSA reading the disclosure of Hatanaka would have understood that Hatanaka discloses a digital videocassette recorder (VCR). Hatanaka's figures and disclosure continually refer to a magnetic tape and a rotary head, which are standard components used in a VCR. *See* Hatanaka, FIG. 1, FIG. 6, 4:1-11. This understanding is corroborated by publications from the Hatanaka patent's named inventors during the time period of 1993 to 1998, showing the progression of their digital VCR (coinciding with timeframe when the Hatanaka patent was filed). Ex. 2004-2006. For example, a 1998 publication co-authored by the Hatanaka patent's inventors—Hatanaka and Okamoto—is

substantially similar to the disclosure in the Hatanaka patent. *See* Hatanaka 1998, Ex. 2004 generally.

The publications by the inventors of the Hatanaka patent are helpful in understanding why LG's interpretation of Hatanka is incorrect, including three important aspects that affect any obviousness analysis with respect to Hatanaka and claim 21: (i) the state of the art at the time of filing of the '945 patent; (ii) what the Hatanaka patent discloses, as would have been understood by a POSA; and (iii) what a POSA would have found obvious in view of the Hatanaka patent.

The digital VCR produced by Hatanaka and Okamoto used magnetic tapes for storage, such as VCR cassette tape. The use of magnetic tapes allows a user to record a program, stop the recording, and then playback the recorded program, but a POSA at the time of the '945 patent would have recognized that such storage mechanisms had limited capabilities. A POSA at the time of the '945 patent would have understood that only a single portion of the magnetic tape can reside in the region of the read and write heads at one time and the process of positioning the tape is too slow to allow simultaneous reading and writing to different portions of a tape. This delay due to physical positioning makes tape systems unsuitable for many data storage applications where information is spread over the storage media and any possible location is equally likely to be desired to be available in the near future. In other words, simultaneous storing and retrieval (as described in the '945

patent) to/from a magnetic tape would not have been possible with Hatanaka's system. Thus, Hatanaka's inventors could not have described a system which was capable of simultaneous playback and recording since the main disclosed recording medium (i.e., magnetic tape) was incapable of supporting such functionality.

Hatanaka discloses that its system can use other storage mechanisms (e.g., a magnetic disk, optical disk, semiconductor memory). Hatanaka, 9:6-8. But, Hatanaka's disclosure of alternative storage mechanisms was nothing more than a recognition that other technologies were known for storing digital data, as would have been understood by a POSA. Even with the use of other storage mechanisms, a POSA would have understood that Hatanaka's system still suffers from deficiencies that prevent the arrangement and features of claim 21, as will be demonstrated below.

B. All of LG's obviousness grounds against claim 21 are deficient.

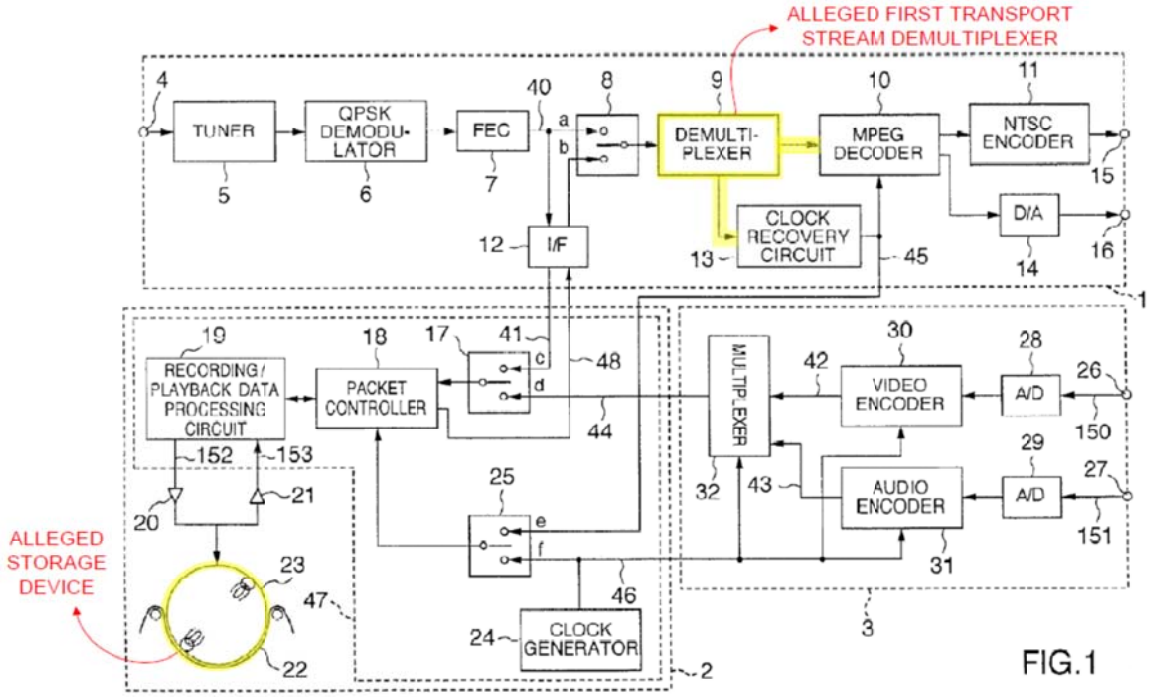
LG argues that claim 21 is obvious over: (i) Hatanaka in view of Hoogenboom; and (ii) Hatanaka in view of Anderson. *See* Petition, Paper 2, p. 8. However, for at least the reasons set forth below, there is no basis to conclude that claim 21 of the '945 patent is obvious under any of these theories.

1. Deficiencies of Hatanaka.

(a) Hatanaka does not teach "a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets."

Claim 21 requires "a storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets"— a feature not disclosed by Hatanaka, because Hatanaka's storage device: (i) does not have a data port coupled to the output of a first transport stream demultiplexer; and (ii) does not receive or store the select packets.

LG attempts to map Hatanaka to claim 21 by alleging "in Hatanaka, the first transport stream demultiplexer is demultiplexer 9." Petition, p. 12. However, this mapping is flawed. FIG. 1 (reproduced below) illustrates Hatanaka's system, including demultiplexer 9 (the alleged first transport stream demultiplexer) and a magnetic tape 22 (the alleged storage device).



Hatanaka's FIG. 1 demonstrates that demultiplexer 9 has two outputs—a first output coupled to MPEG decoder 10 and a second output coupled to clock recovery circuit 13. *See* Hatanaka, FIG. 1 (above). Regarding the first output, demultiplexer 9 "determines a type of a respective packet, … separates only packets of a video, audio, etc., relating to the specified program, and then outputs these packets to the MPEG 10." Hatanaka, 3:18-22. Regarding the second output, demultiplexer 9 outputs a Program Clock Reference (PCR) to clock recovery unit 13 to produce a data clock. The PCR represents the time when compression took place in a broadcasting station. Hatanaka, 3:22-27. Thus, neither of the two outputs of demultiplexer 9 is coupled to a data port of Hatanaka's magnetic tape 22. Instead, the only data port of Hatanaka's magnetic tape 22 is coupled to

recording/playback data processing circuit 19 and packet controller 18. Meaning, at most, it can be alleged that Hatanaka's magnetic tape 22 is indirectly coupled to an input node of demultiplexer 9—not any of demultiplexer 9's outputs. Thus, given Hatanaka's configuration, there is no way that Hatanaka's magnetic tape 22 is coupled to an output of demultiplexer 9, and such a configuration would not have been obvious.

Since Hatanaka's magnetic tape 22 is incapable of receiving information that is output by demultiplexer 9, Hatanaka's alleged storage device also cannot receive select packets from the alleged first transport stream demultiplexer, as claimed. Claim 21 requires that the first transport stream demultiplexer: (i)"**select[s] packets of data** having a predefined packet identifier" and (ii) has an "output to provide the select packets of data" to the storage device. '945 patent, 10:19-24. However, Hatanaka's demultiplexer 9 (the alleged first transport stream demultiplexer) sends its select packets ***only*** to MPEG decoder 10, ***not*** Hatanaka's magnetic tape 22 (i.e., the alleged storage device). *See* Hatanaka, 3:18-22. Hatanaka never discloses an embodiment where the packets selected by demultiplexer 9 are received by magnetic tape 22. Nor can Hatanaka disclose such an embodiment since there is no communicative link between the output ports of demultiplexer 9 and the data port of magnetic tape 22.

Thus, for the foregoing reasons, Hatanaka does not teach the claimed

"storage device having a data port coupled to the output of the first transport stream demultiplexer to receive the select packets, wherein the storage device is to store the select packets." And LG does not and cannot allege that any of its secondary references—Hoogenboom or Anderson—teaches or renders this feature obvious. *See* Petition, pp. 13-14. Accordingly, claim 21 is not rendered obvious over either proposed combination—Hatanaka/Hoogenboom or Hatanaka/Anderson.

(b) Hatanaka does not teach "a decoder having … a second input coupled [to] the data port of the storage device to receive the select packets..."

Hatanaka also fails to disclose or render obvious a "decoder having … a second input coupled [to] the data port of the storage device to receive the select packets..." Hatanaka's MPEG decoder 10 does not have a second input coupled to the data port of Hatanaka's magnetic tape 22 to receive select packets.

As illustrated in FIG. 1 of Hatanaka, MPEG decoder 10 has two inputs: a first input to receive select packets of data from demultiplexer 9, and a second input to receive a data clock from clock recovery circuit 13. *See* Hatanaka, 3:18-27. Thus, MPEG decoder 10 only receives select packets from Hatanaka's demultiplexer 9, ***not*** Hatanaka's magnetic tape 22.

Thus, Hatanaka does not teach this claimed feature. Similar to the first missing feature discussed above, LG does not and cannot allege that any of its

secondary references—Hoogenboom or Anderson—teaches or renders this feature obvious. Therefore, neither combination—Hatanaka/Hoogenboom or Hatanaka/Anderson—renders claim 21 obvious.

(c) Hatanaka does not teach "a first clock recovery module … wherein the first clock recovery module is to generate a clock … before the select packets are stored in the storage device."

LG fails to cite to any portion of Hatanaka that expressly teaches generating a clock at the output before the select packets are stored, as required by claim 21. *See* Petition, pp. 15-17. Although LG introduces Hoogenboom and Anderson in an attempt to meet this claim feature, LG still maintains that Hatanaka teaches this feature as well. *See* Petition, p. 16. Essentially, LG is advancing the same failed anticipation ground presented in its first Petition, while also advancing two new obviousness grounds in this proceeding.

Regarding, LG's re-hashed anticipation argument: Similar to its first Petition, LG alleges that Hatanaka's time stamp generation meets this claimed feature. Petition, p. 16. However, as the Board already concluded in its prior decision not to institute trial against claim 21:

> Hatanaka discloses that in playback, the time stamps maintain time intervals at which the packets are output, *id.* at col. 4, ll. 43–45, but, in reproduction, the digital broadcasting receiver is operated by a timing signal from packet control circuit 18, to produce decoder clock 45, *id.* at col. 4, ll. 51–54. Because packet control circuit 18 cannot use

> decoder clock 45, clock changeover switch 25 is set to "f," so that clock generator 24 provides fixed clock 46 to packet control circuit 18. *Id.* at 51–59. Packets are output at a timing generated by fixed clock 46 and clock recovery unit 13 generates a stable clock based on fixed clock 46. *Id.* at col. 4, ll. 59–60. The Petition does not address how the generation of a stable clock by clock recovery module from clock 46 constitutes the limitations recited in claim 21 of the '945 Patent. IPR2015-00321, Institution Decision, Ex. 2003, Paper No. 20, p. 16.

Accordingly, LG's repeated arguments regarding Hatanaka and this claim feature are flawed and should be disregarded.

Moreover, LG also alleges that "clock recovery unit 13 and packet controller 18 [together] are the claimed "clock recovery module. Petition, p. 15. Here, LG is conflating two of Hatanaka's components, without explaining why this is appropriate. *Id*. Hatanaka's clock recovery circuit 13 and packet controller 18 are separate components with their own respective functionalities. Nowhere does Hatanaka treat these components as a single component, as LG is attempting to do here. Hatanaka's clock recovery circuit 13 generates a decoder clock 45, while packet controller 18 is responsible for generating time stamps—two separate and distinct operations. LG has not provided any evidence that demonstrates why a POSA would have interpreted that Hatanaka's packet controller 18 and clock recovery circuit 13, together, are the claimed first clock recovery module. Thus,

LG's arguments here are flawed, repetitive, already deemed unpersuasive, and should be disregarded.

(d) The system of claim 21 is significantly different from Hatanaka.

The structural differences between claim 21 and Hatanaka are significant and impact functionality. For example, the structure recited in claim 21 supports a system that provides "pause" functionality involving simultaneous recording of a first portion of a program and playback of a second portion of the program from storage. This functionality is referred to in the '945 specification as a "part-time time-shifting mode." *See* '945 patent, 4:1-14. Hatanaka's system is incapable of supporting such functionality.

The Hatanaka system includes a series of changeover switches—playback changeover switch 8, recorded signal changeover switch 17, and clock changeover switch 25. *See* Hatanaka, 2:30-50. Hatanaka's changeover switches control which of Hatanaka's three operations is performed (either play, record, or playback). For example, playback changeover switch 8 controls whether Hatanaka performs its play operation (switch set to "a") or playback operation (switch set to "b"). FIG. 1, reproduced below, highlights each of Hatanaka's changeover switches.

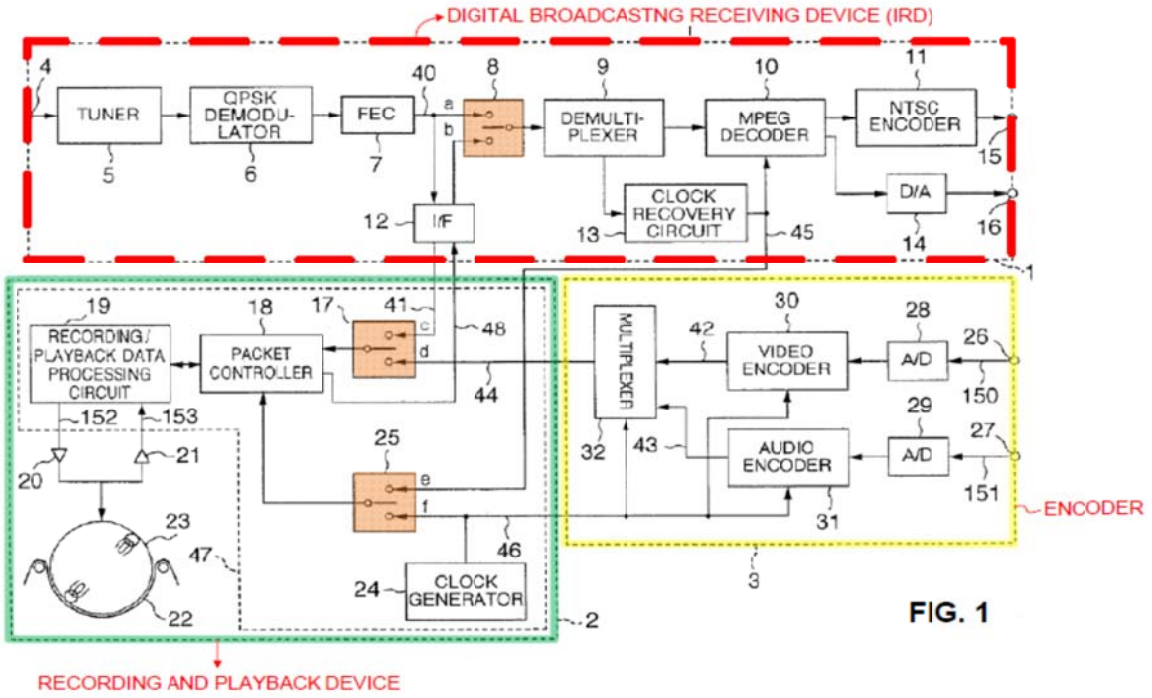


FIG. 1

Each of Hatanaka's changeover switches can select only one contact at a time:

Hatanaka Switch	Contact
playback changeover switch 8	"a" or "b"
recorded signal changeover switch 17	"c" or "d"
Clock changeover switch 25	"e" or "f"

Hatanaka's system cannot simultaneous record and playback different portions of the same program, because clock changeover switch 25 prevents such an operation. Clock changeover switch 25 provides different clocks to packet controller 18 based on whether contact "e" or "f" is selected. Contact "e" is selected for Hatanaka's record operation and contact "f" is selected for Hatanaka's playback operation. *See* Hatanaka, 4:46-50, 3:51-64. Specifically, during Hatanaka's record operation,

clock changeover switch 25 is set to contact e, so that decoder clock 45 generated by clock recovery circuit 13 is used by packet controller 18 to generate time stamp information: "To this end, clocks used for producing the time stamp 102 in the recording should be decoder clock 45 reproduced by the clock recovery unit 13. In recording, the clock changeover switch 25 is set at a contact e so that the decoder clock 45 is inputted to the packet control circuit 18." Hatanaka, 4:46-50.

In contrast, during Hatanaka's playback operation, clock changeover switch 25 is set to contact f, so that a fixed clock 46 from clock generator 24 is inputted to packet controller 18 to assist in retrieving packets of data from the magnetic tape:

> "***[i]n reproduction***, the clock recovery unit 13 of the digital broadcasting receiver 1 is operated by a timing signal outputted from the packet control circuit 18 to produce decoder clock 45. ***Thus, the packet control circuit 18 <u>cannot use</u> the decoder clock 45. In order to avoid-this, the clock generator 24 which generates a fixed clock 46 is provided so that when the clock changeover switch 25 is set at a contact f***, the fixed clock 46 is inputted to the packet control circuit 18 and a packet is outputted at a timing generated by the fixed clock 46. Hatanaka, 3:51-64, emphasis added.

Hence, Hatanaka explicitly discloses that clock changeover switch 25 must be set to different contacts ("e" or "f") to perform its respective record and playback operations. Hatanaka, 3:51-64; 4:48-50. Since clock changeover switch

25 only allows packet controller 18 to receive an individual input from either decoder clock 45 (contact "e") or clock generator 24 (contact "f"), ***not*** both simultaneously, Hatanaka's device simply cannot record and playback simultaneously.

This example, illustrating differences in functionality between the structure recited in claim 21 and the structure disclosed by Hatanaka, shows that the structural differences between claim 21 and Hatanka are significant, and that claim 21 is patentable over Hatanaka and any combination raised by LG.

2. It would not have been obvious to combine Hatanaka and Hoogenboom to arrive at claim 21, because the combination would have required significant reconstruction

LG relies on Hoogenboom in an attempt to remedy the deficiencies of Hatanaka identified in its first Petition. However, LG fails to explain: (i) why a POSA would have been motivated to combine the structurally different systems of Hatanaka and Hoogenboom; and (ii) how a POSA would have successfully overcome the challenges that would have arisen when trying to modify Hatanaka's system to incorporate Hoogenboom's teachings. LG's entire argument relies solely on unsupported and conclusory statements by its expert, which are nothing more than a mischaracterization of what would have been obvious at the time of the '945 patent.

Even if the proffered combination of Hatanaka/Hoogenboom separately

taught the individual elements of the claims—which Patent Owner does not concede—a POSA would not have combined the teachings of Hatanka and Hoogenboom, as alleged. LG contends that adding Hoogenboom's video decompressor to Hatanaka's system amounts to use of a known technique to improve similar devices in the same way. Petition, p. 29. But "[f]ocusing on the obviousness of substitutions and differences, instead of on the invention as a whole, is a legally improper way to simplify the often difficult determination of obviousness." *Gillette Co. v. S.C. Johnson & Son, Inc.*, 919 F.2d 720, 724 (Fed. Cir. 1990). Given all of Hatanaka's deficiencies, and the structural and functional limitations discussed above, significant modifications to Hatanaka's system would have been required to meet claim 21 and would have presented a myriad of challenges. However, the modifications needed to Hatanaka's system and the solutions to those challenges would have only been realized by looking at the teachings of the '945 patent—a classic case of impermissible hindsight. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

LG ignores Hatanaka's structure and alleges that a POSA would have been motivated to combine Hatanaka and Hoogenboom to more efficiently acquire desired video data from storage. Petition, p. 29. However, any attempt at modifying Hatanaka would have required a significant reconstruction due to Hatanaka rigid system of multiple switches and multiple clocking mechanisms. As

evidenced by the iterations of Hatanaka's digital VCR over several years, changes to the system were incremental over time and required a significant amount of research, experimentation, and cost. *See* Ex. 2004-2006. Thus, before a POSA could have looked to the teachings of Hoogenboom for any substantive guidance, a POSA would have needed to reconstruct Hatanaka's system in a significant way. But the necessary changes to Hatanaka's system would not have been obvious nor practical to a POSA.

The necessary reconstruction of Hatanaka's device would have included, at least: (i) determining how to allow packet controller 18 to manage and distinguish between its current clocking mechanisms and the clocking mechanisms that would have been introduced with the addition of Hoogenboom's video decompression processor; (ii) removing Hatanaka's changeover switches; and (iii) duplicating or modifying several of Hatanaka's components: packet controller 18, clock recovery circuit 13, clock generator 24, recording/playback data processing circuit interface 12, and demultiplexer 9. Regarding the duplication or modifications of Hatanaka's components, the extensive modifications would have included a complete rewiring of Hatanaka's circuit and at least the following:

- **Modify the clock recovery system:** Hatanaka's clock recovery system would need to be redesigned to support a clock produced by the analog subsystem during recording, the digital program stream during recording,

and the newly generated clock during playback (provided by Hoogenboom's video decompression processor). Additionally, an algorithm would need to be created to determine which clock would be used for each of the many different combinations and then a controller would need to be constructed to implement this new algorithm.

- **Modification to the demultiplexer**: Hatanaka's demultiplexer 9 would need to be modified in order to provide clock signals from the digital program stream during recording in order to operate with the newly designed and expanded clocking system.

Hence, the reconstruction of Hatanaka's system would not have been routine and would have been difficult given the lack of guidance. And LG has not provided any evidence explaining why a POSA would have been motivated to make such modifications. In fact, a POSA desiring to build a system according to claim 21 would more likely have been motivated to create a system from scratch than to have started with the system of Hatanka and attempted to modify it to provide Hoogenboom's video decompressor.

Here, a piecemeal reconstruction, such as the one conducted by LG and supported by Dr. Schonfeld, is not permissible: "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This

court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'" *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (quoting *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988)).

3. Anderson does not teach "a first clock recovery module ... wherein the first clock recovery module is to generate a clock at the output … before the select packets are stored in the storage device."

(a) Overview of Anderson

Anderson discloses a transport demultiplexer for demultiplexing an MPEG-2 compliant transport stream into a system data stream, a video data stream, and an audio data stream. Anderson, Ex. 1010, Abstract. Anderson's demultiplexer has frontend logic that receives transport stream input packets and delivers the transport stream packets to a packet buffer. *Id*. Thereafter, the packet buffer delivers system data to system data, audio data, and video data unloaders. *Id*. Andersons's FIG. 6 (reproduced below) illustrates the dataflow through its transport demultiplexer. *See also* 7:65 et seq.

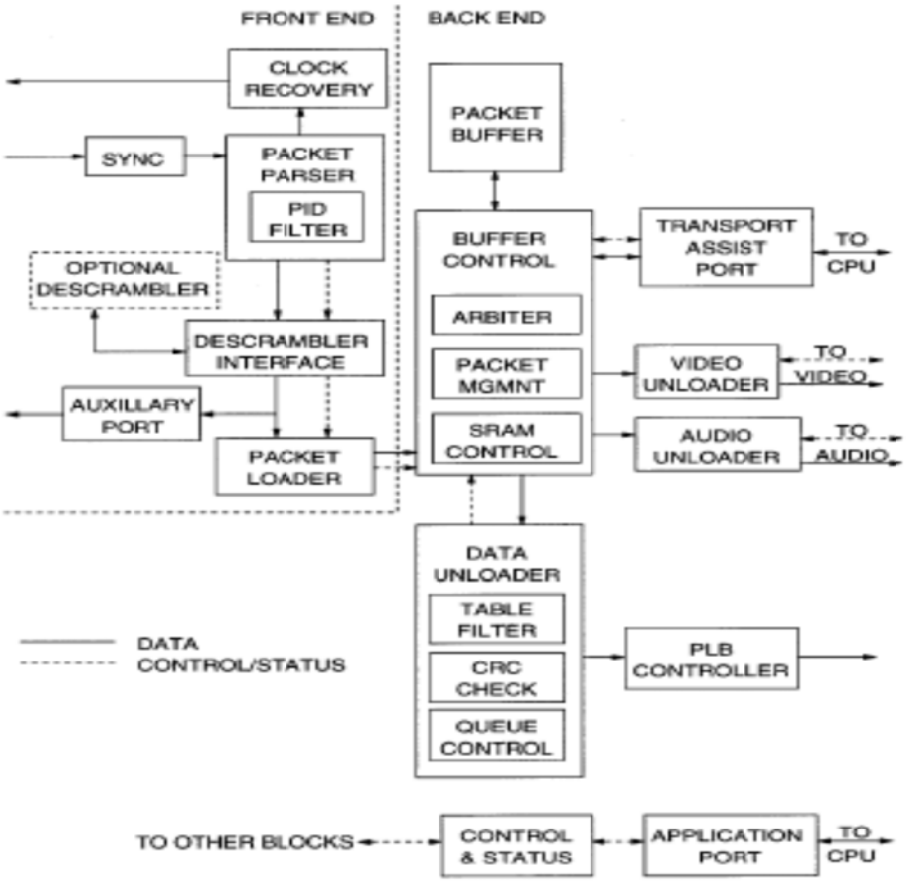


FIG. 6

Anderson's front end logic includes a clock recovery component. However, other than a brief statement that "the packet parser sends PCRs from matching PCR packets to the clock recovery unit for reconstructing the System Time Clock (STC)," Anderson does not provide any indication of when clocks are generated by its system. *See* Anderson, 8:12-14.

(b) LG's reliance on Anderson's table filtering operation to render obvious the claimed feature is a stretching of Anderson's teachings and improper hindsight reconstruction.

Anderson's discussion about its clock generation mechanisms is scant;

Anderson never discloses "generat[ing] a clock at the output …before the select packets are stored in the storage device." Anderson's deficiencies are acknowledged by LG, as LG points to a completely different operation—table filtering—for its obviousness analysis. *See* Petition, pp. 33-34. But, LG's allegations are conclusory and represent nothing more than a case of impermissible hindsight reconstruction—relying on the '945 patent as a guide to pick and choose disparate teachings to arrive at the claimed system. *See* Petition, pp. 33-34.

First, LG curiously points to Anderson's table filtering discussion, which is not linked to Anderson's clock recovery mechanisms. *See* Petition, pp. 30-37. Anderson discusses its clocking mechanisms and table filtering mechanisms separately—indicating that these operations are different. Any allegation that these two operations are somehow similar runs counter to Anderson's disclosure. Anderson's table filtering mechanism occurs before memory storage. *See* Anderson, 11:57-65. And based on this alone, LG makes a bald assertion that "filtering table sections before sending them to DRAM or other memory [] would apply equally to clock recovery" and "the motivation to perform clock recovery before sending the transport packets to DRAM or other memory would be … the desire to 'reduce [] the application processor work load .. and the required size of working areas in DRAM or other memory." Petition, pp. 34.-35. However, LG never explains *how or why* performing clock recovery in a manner similar to

Anderson's table filtering would reduce the application processor work load and the required size of working areas in DRAM or other memory. Anderson's brief disclosure regarding its clock recovery mechanisms simply does not provide enough guidance to support LG's huge leap. LG fails to show that the art teaches or suggests the claim elements, and does not articulate a persuasive reason with a rational underpinning to support a legal conclusion of obviousness. *KSR Int'l Co.,* 550 U.S. at 418; *Heart Failure Tech. v. Cardiokinetix*, IPR2013-00183, Paper 12, p. 9 (P.T.A.B. March 11, 2013) ("*Heart Failure*") ("Petitioner must show some *reason* why a person of ordinary skill in the art would have thought to combine *particular* available elements of knowledge, as evidenced by the prior art, to reach the claimed invention" (emphasis in original)).

Since Anderson does not support LG's conclusions, it is evident that LG's conclusions are solely based on impermissible hindsight reconstruction. At all times, impermissible hindsight must be avoided and the legal conclusion of obviousness must be reached on the basis of facts gleaned from the prior art—and not from the patent owner's disclosure. *KSR Int'l Co.*, 550 U.S. at 421; s*ee also Application of McLaughlin*, 443 F.2d 1392, 1395 (C.C.P.A 1971). Without an articulated reason as to *how or why* the prior art elements would be combined to produce the claimed invention, the combination of prior art elements is viewed as a hindsight reconstruction effort to reach the claimed invention. *Innogenetics, N.V. v.*

Abbott Laboratories, 512 F.3d 1363, 1374 n. 3 (Fed. Cir. 2008). This case is no different. Here, LG does not explain the link between Anderson's table filtering operations and clock recovery mechanisms—a link that cannot be established since Anderson does not connect the disparate operations of table filtering and clock recovery in any manner. LG, nor the references, provide any guidance as to how or why a POSA would have modified Anderson's system such that its clock recovery component generates a clock at the output before the select packets are stored in the storage device, as required by claim 21.

The Fed. Circuit has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'" *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (quoting *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988)). Here, LG has performed a piecemeal reconstruction—using the '945 patent as a guide—in order to choose disparate pieces of Anderson's disclosure along with Hatanaka to arrive at claim 21. This tactic is improper and expressly prohibited. *See Grain Processing Corp. v. Am. MaizeProds. Co*., 840 F.2d 902, 907 (Fed. Cir. 1988) ("Care must be taken to avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.").

VI. CONCLUSION

LG is time barred from bring this Petition and should not be allowed to circumvent the IPR rules. Additionally, LG still has not met its burden of showing a reasonable likelihood of prevailing with respect to claim 21. Patent Owner has carefully catalogued LG's repeated failures to meet its burden, showing that LG has not established that the cited references render obvious claim 21 of the '945 patent. Accordingly, the Board should deny institution.

Respectfully submitted,

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CERTIFICATION OF SERVICE

The undersigned hereby certifies that the foregoing **Patent Owner Preliminary Response and all associated exhibits** were served electronically via e-mail on November 6th, 2015, in their entirety on the following:

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