

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ARM, Ltd.
Petitioner,

v.

GODO KAISHA IP BRIDGE 1
Patent Owner.

Case IPR2016-00825
Patent RE43, 729

Before TRENTON A. WARD, GEORGIANNA W. BRADEN, and
MONICA S. ULLAGADDI, *Administrative Patent Judges*.

ULLAGADDI, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

ARM, Ltd. and ARM, Inc. (collectively, “Petitioner”)¹ filed a Petition (Paper 1, “Pet.”) for *inter partes* review of claims 21 and 22 of U.S. Patent No. RE43,729 (Ex. 1001, “the ’729 patent”). Godo Kaisha IP Bridge 1 (“Patent Owner”)² timely filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Thereafter, on September 7, 2016, a conference call was held among the parties and the Board.³

Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Upon consideration of the Petition, the Petitioner’s supporting evidence, as well as Patent Owner’s Preliminary Response and supporting evidence, and for the purposes of this decision, we are persuaded Petitioner has established a reasonable likelihood it would prevail with respect to at least one of the challenged claims. Accordingly, for the reasons that follow, we institute an *inter partes* review of the ’729 patent as to challenged claims 21 and 22.

¹ Petitioner identifies ARM, Ltd. and ARM, Inc. as the real parties-in-interest. Pet. 57–58.

² In its Mandatory Notices, Patent Owner identifies “IP Bridge” as the real party in interest (Paper 5, 1) and patent owner (Paper 7, 1).

³ During the conference call, Petitioner requested leave to file a reply to Patent Owner’s Preliminary Response, as well as a certified English translation of JP 8-320423, the Japanese patent application designated as “Foreign Application Priority Data” on the face of the ’729 patent. (Paper 11, 2). We denied both requests. *Id.* at 4.

B. Related Proceedings

Patent Owner informs us that the '729 patent is at issue in the following proceeding: *Godo Kaisha IP Bridge 1 v. Broadcom Limited et al.*, Case No. 2-16-cv- 00134 (E.D. Tex.), filed February 15, 2016. Paper 5, 2.

C. The '729 Patent

The '729 patent is a reissue of U.S. Patent No. 6,237,084 (“the '084 patent”). Ex. 1001, [64]. The '729 patent discloses a positive conversion saturation calculation circuit that operates on a sum-product result of matrix multiplication. *Id.* at 13:23–40. The value of the sum-product result is stored in a sum-product result register. *Id.* at 14:8–10. Figure 4, reproduced below, shows positive conversion saturation calculation circuit 3 that operates on the value stored in sum-product result register 6 and includes constant generator 21, comparator 22, polarity judging unit 23, multiplexer 24, and zero generator 25. *Id.* at 13:46–49.

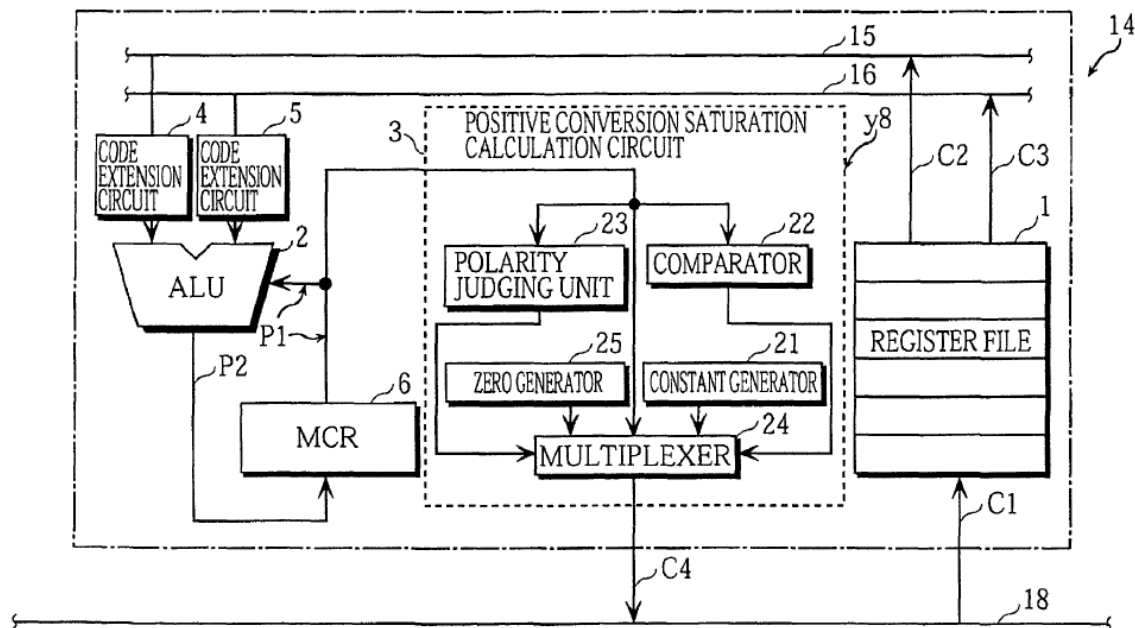


Figure 4 of the '729 patent

When a positive conversion saturation calculation instruction (MCSST) is fetched and decoded, “the constant generator 21 generates a maximum positive value” (e.g., 0x0000_00FF) that is uncoded and has a width specified by a width field of the instruction, and zero generator 25 generates the integer 0x0000_0000. *See* Ex. 1001, 13:35–14:7, 15:4–6.

Comparator 22 compares the magnitude of the sum-product value stored by sum-product result register 6 with the maximum positive value output by constant generator 21 and outputs “1” to multiplexer 24 when the sum-product value exceeds the maximum positive value and outputs “0” in all other cases. *Id.* at 14:29–35. Polarity judging unit 23 outputs “1” to multiplexer 24 when it determines the sum-product value is negative and outputs “0” in all other cases. *Id.* at 14:60–15:3.

In accordance with the values shown in Figure 9, reproduced below, based on the inputs received from comparator 22 and polarity judging unit 23 (respectively, logic values x and y in Figure 9), multiplexer 24 selects one of the 0x0000_0000 value generated by zero generator 25, the maximum positive value 0x0000_00FF generated by constant generator 21, and the sum-product value stored by sum-product result register 6. Ex. 1001, 15:14–37.

LOGIC VALUE X	LOGIC VALUE Y	SELECTED INPUT VALUE
1	0	0x0000_00FF
1	1	0x0000_0000
0	1	0x0000_0000
0	0	STORED VALUE OF SUM-PRODUCT RESULT REGISTER

Figure 9 of '729 patent

Figure 12B, reproduced below, depicts pipelined execution of a matrix multiplication subroutine including the positive saturation conversion instruction, MCSST.

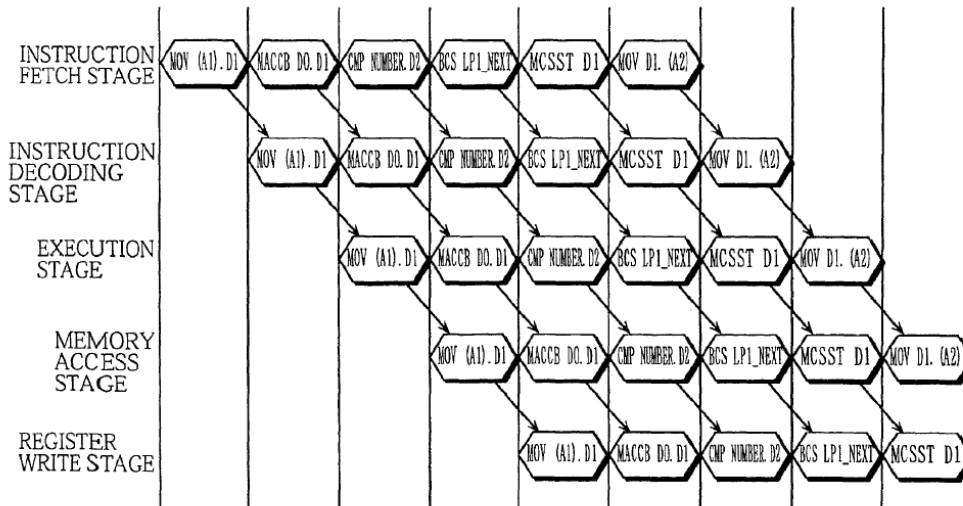


Figure 12B of the '729 patent

Figure 12B was cited by Patent Owner during prosecution of applications in the priority chain⁴ leading to the '729 patent. During prosecution of the '920 priority chain application (now “the '145 patent”), the Examiner issued rejections under 35 U.S.C. §§ 112, 251 of claims specifying that the plural arithmetic operations executed by the positive conversion saturation calculation circuit (discussed above) are performed “within one cycle” or “in a single cycle.” Ex. 1013, Response to Non-Final Office Action dated December 8, 2009, 20–21. According to Patent

⁴Application No. 09/399,577 (“the '577 application”), the application underlying the '084 patent, is a divisional application of Application No. 11/016,920 (“the '920 application”), which was filed on Dec. 21, 2004 and is now U.S. Patent No. RE43,145 (“the '145 patent”), which is a divisional application of Application No. 10/366,502 (“the '502 application”), which was filed on Feb. 13, 2003 and is now U.S. Patent No. RE39,121 (“the '121 patent”), which is a divisional application of Application No. 08/980,676 (“the '676 application”), which was filed on Dec. 1, 1997 and is now U.S. Patent No. 5,974,540 (“the '540 patent”).

Owner, Figure 12B “would have been understood by those of skill in the art that the recited operations are executed in a single cycle,” as recited in the claims, because “each interval in the horizontal direction represents one cycle.” *Id.* at 22.

D. Illustrative Claims

As noted above, Petitioner challenges claims 21 and 22 of the '729 patent, of which claim 21 is independent. Both claims are reproduced herein below.

21. A processor that decodes and executes instructions, the processor comprising:
- a detecting unit for detecting whether an instruction to be decoded is a predetermined instruction; and
 - a rounding unit for rounding, when the detecting unit is detecting that the instruction is the predetermined instruction, a signed m-bit integer stored at an operand designated by the predetermined instruction to a value expressed as an unsigned s-bit integer, wherein
 - s is less than m and the rounding of the rounding unit includes the following plural arithmetic operations which are performed within one cycle:
 - (a) testing whether the signed m-bit integer is a negative number or not,
 - (b) testing whether the signed m-bit integer exceeds a predetermined positive number or not, and
 - (c) defining the value expressed as the unsigned s-bit integer in accordance with the testing results of (a) and (b).

Ex. 1001, 28:19–36.

22. The processor of claim 21, wherein the value of s is specified by the predetermined instruction.

Id. at 28:37–38.

E. The Evidence of Record

Petitioner relies upon the following references, as well as the Declaration of Dr. V. Thomas Rhyne (Ex. 1021):

Reference	Patent/Printed Publication	Date	Exhibit
Van Hook	US Patent No. 5,734,879	Apr. 29, 1994 (filed)	1002
Dulong	U.S. Patent No. 5,822,232	Mar. 1, 1996 (filed)	1003
Intel MMX 1	Intel MMX™ Technology Developers Guide	Mar. 1996	1004
Intel MMX 2	Intel Architecture MMX™ Technology Programmer's Reference Manual	Mar. 1996	1005
Peleg	MMX Technology Extension to the Intel Architecture	Aug. 1996	1006
Patterson	Computer Organization and Design, The Hardware / Software Interface	1994	1007

F. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 21 and 22 of the '729 patent based on the following grounds:

Reference(s)	Basis	Claims Challenged
Van Hook	§ 102(e)	21 and 22
Van Hook	§ 103(a)	21 and 22
Van Hook in view of the Knowledge of One Skilled in the Art, as Described in Patterson	§ 103(a)	21 and 22
Dulong, Intel MMX 1, Intel MMX 2, and Peleg	§ 103(a)	21 and 22

Reference(s)	Basis	Claims Challenged
(collectively, “the MMX references”)		

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable construction standard). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Claim terms need only be interpreted to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. “one cycle”

The term “one cycle” appears once in the ’729 patent, in claim 21. According to Petitioner, the term “one cycle” recited in claim 21 “should be construed to mean that the cited operations are performed within *a single processor stage.*” Pet. 16 (emphasis added). Petitioner’s bases for the proposed construction are Patent Owner’s reference to Figure 12B in connection with issues related to new matter, during prosecution, and knowledge of one skilled in the art. *Id.* at 16–18 (citing Ex. 1013, 22).

Petitioner argues “the ’729 specification might be said to teach that elements 21(a) through (c) occur in the execution stage” but concedes “the ’729 patent does

not have any linkage between execution occurring in an execution stage and the claimed requirement that the operations in elements 21(a) through (c) be performed in one cycle.” *Id.* at 17 (quotations omitted). Petitioner contends that, because Patent Owner filled in this missing link during prosecution by relying on knowledge of one skilled in the art, that same knowledge can be used to construe the term “one cycle.” *See id.* at 17–18.

Petitioner’s contention is unpersuasive. Patent Owner’s arguments during prosecution of applications in the priority chain leading to the ’729 patent that establish a link between the claimed “one cycle” and the “execution stage” depicted in Figure 12B are an insufficient basis to persuade us that the term “one cycle” should be construed as an “execution stage.” Furthermore, Patent Owner did not argue that the “one cycle” *is* the “execution stage.” Rather, during prosecution of the related ’920 application (*see supra* n.4 for priority chain of the ’729 patent), Patent Owner argued

Diagrams for illustrating pipelined execution, such as FIG. 12B of this application, were used extensively in the art, and accordingly FIG. 12B would have been understood by those of skill in the art that the recited operations are executed in a single cycle, as recited in claims 53 and 54. *One of skill in the art would have understood that each interval in the horizontal direction represents one cycle, and that along the vertical axis the instructions are passing through the illustrated 5 pipeline stages Thus, one of ordinary skill in the art would have understood that the original specification clearly discloses that the positive conversion saturation calculation processing is performed within one cycle in an execution stage of the instruction “MCSST D 1.”*

Ex. 1013, Response to Non-final Office Action dated December 8, 2009, 22 (emphasis added). That is, Patent Owner argued how one of ordinary skill in the art would have understood Figure 12B to provide support for the term “one cycle,”

not necessarily how one of ordinary skill in the art would have construed “one cycle.” *See id.*

Patent Owner contends Petitioner’s proposed construction for “one cycle” is “neither supported by the plain and ordinary meaning nor the intrinsic evidence.” Prelim. Resp. 5. Patent Owner further contends that “the plain and ordinary meaning of ‘performed within one cycle’ is a measure of time, not the occurrence of a particular processor stage” and sets forth several definitions from technical dictionaries for this term. *Id.* at 5–6 (citing Ex. 2001, 3; Ex. 2002, 3; Ex. 2003, 3; Ex. 2004, 3–4). We agree with Patent Owner’s contention, which is supported by Petitioner’s own Declarant’s testimony regarding the prosecution of the ’920 application. Ex. 1021 ¶¶ 21–30. Dr. Rhyme testifies that “[t]ypically, one of skill in the art would understand the RISC [Reduced Instruction Set Computer] pipeline in Figure 12B to describe a system where each stage corresponded to a single clock cycle.” *Id.* ¶ 29.

Accordingly, for the purposes of this decision and on the record before us currently, we construe the term “one cycle” to encompass one oscillation of a CPU clock, consistent with Patent Owner’s proffered dictionary definitions. *See* Prelim. Resp. 5–6.

2. “value of *s* is specified”

According to Petitioner, the limitation “‘value of *s* is specified by the predetermined instruction’ means, at a minimum, that the predetermined instruction mentions or states in detail the value of *s*.” Pet. 18–19.

For the purposes of this decision and on the record before us, it is not necessary to explicitly construe this term at this time.

B. Principles of Law

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re*

Magnum Oil Tools Int'l, Ltd., No. 2015-1300, slip op. at 25 (Fed. Cir. July 25, 2016).

Thus, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that one of the challenged claims would have been obvious over the proposed combinations of prior art.

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner’s Declarant, Dr. Rhyne, testifies that a person of ordinary skill in the art relevant to the ’729 patent “would have a Bachelor’s of Science degree in Electrical Engineering, Computer Engineering or a closely related field, and at least three years of professional experience in the development of computer processors.” Ex. 1021 ¶ 31. Patent Owner does not offer any contrary explanation at this time regarding who would qualify as a person of ordinary skill in the art relevant to the ’729 patent. *See generally* Prelim. Resp.

Based on our review of the ’729 patent, the types of problems and solutions described in the ’729 patent and cited prior art, and the testimony of Petitioner’s

Declarant, we adopt and apply Petitioner’s definition of a person of ordinary skill in the art at the time of the claimed invention. We note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Alleged Anticipation Based on Van Hook

Petitioner contends claims 21 and 22 of the ’729 patent are anticipated under 35 U.S.C. § 102(e) by Van Hook. Pet. 20–36. Patent Owner disputes Petitioner’s contention. Prelim. Resp. 9–13. For the reasons that follow, we determine Petitioner has not demonstrated a reasonable likelihood of prevailing as to this ground.

1. Overview of Van Hook

Van Hook describes a CPU provided with a graphics execution unit (GRU) for executing graphics operations in accordance with the disclosed graphics data formats. Ex. 1002, Abstract. The GRU executes arithmetic operations on graphics data including “addition, subtraction, rounding, expansion, merge, alignment, multiplication, logical, compare, and pixel distance operations.” *Id.* Specifically, Van Hook describes FPACK16, FPACK32, and FPACKFIX instructions along with the corresponding circuitry. *Id.* at 10:5–8. Van Hook describes the FPACK16 instruction 106a as shifting four 16-bit fixed values in accordance with a scale factor and determining whether an extracted value is negative. *Id.* at 9:36–41. “If the extracted value is negative (i.e., msb is set), zero is delivered as the clipped value. If the extracted value is greater than 255, 255 is delivered. Otherwise, the extracted value is the final result.” *Id.* at 9:41–46; *see also id.* at 10:9–21 (“The circuitry 248 for executing the FPACK16 instruction comprises four identical portions 240a-240d, one for each of the four corresponding 16-bit fixed

values . . . [t]he shifter . . . shifts the corresponding 16-bit fixed value . . . [t]he sign bit and the logical OR of bits [29:15] of each of the shift results are used to control the corresponding multiplexor . . . Either bits [14:7] of the shift result, the value 0xFF or the value 0x00 are output.”).

2. Analysis

Claim 21 of the '729 patent requires that each of the operations recited in limitations (a) through (c) are “performed within one cycle.” Specifically, claim 21 recites, *inter alia*,

- s is less than m and the rounding of the rounding unit includes the following plural arithmetic operations which are performed within one cycle:
- (a) testing whether the signed m-bit integer is a negative number or not,
 - (b) testing whether the signed m-bit integer exceeds a predetermined positive number or not, and
 - (c) defining the value expressed as the unsigned s-bit integer in accordance with the testing results of (a) and (b).

Ex. 1001, 28:28–36.

First, Petitioner argues “the operations shown in Figure 8e of Van Hook occur within one cycle” because there are no intermediate registers depicted between rs2 and rsd, which “means that the operations occurring between rs2 and rd are performed in one cycle.” Pet. 24 (citing Ex. 1021 ¶¶ 56–61). Petitioner asserts Figure 5 of Van Hook also supports this argument because “Figure 5 shows input registers 55a and 55b, the FPACK function block 59, which executes the entire FPACK16 instruction, and destination register 55c, with no intermediate registers between the input registers 55a and 55b and the destination register 55c.”

Id.

Patent Owner responds that even if Figure 8e of Van Hook showed every required component required to carry out the FPACK16 instruction, Petitioner's argument is flawed because the underlying premise "assumes (without *any* support) that the underlying system of Van Hook already performs *FPACK16* 'within one cycle.'" Prelim. Resp. 10–11.

We are persuaded by Patent Owner's argument. If a prior art reference does not expressly set forth a particular element of the claim, the reference still may anticipate only if that element is "inherent" in its disclosure. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002). Our reviewing court has held that

[t]o establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations and internal quotations omitted) (emphasis added).

Dr. Rhyne testifies that "the logic described in Figure[] 8e will operate and the functions will be performed virtually immediately (within the bounds of the limitations of the specific hardware that implements these logic elements)." Ex. 1021 ¶ 56. Dr. Rhyne, however, does not testify as to what these bounds and limitations are, nor persuade us that that Van Hook's logic and circuitry *necessarily* satisfies these bounds and limitations so as to inherently disclose the "within one cycle" limitation required by claim 21. *Id.* Stated differently, Dr. Rhyne does not testify what CPU clock speeds were known or achievable during the relevant timeframe, and does not testify as to how fast Van Hook's circuitry would have been understood to perform the operations.

Dr. Rhyne also testifies that Van Hook’s “circuitry for the two functions is operating independently and without any restriction on the timing (such as clocked registers) largely simultaneous[ly], one of skill in the art would understand the operations, including the functionality described in elements 21(a) through 21(c), to be performed within a single cycle.” *Id.* ¶ 57. We are not persuaded by this testimony for two reasons: (1) because of the relative nature of Dr. Rhyne’s observations (i.e., circuitry operating independently and simultaneously) that are not linked in any way to an oscillation of a CPU clock; and (2) because Dr. Rhyne does not disclose the underlying facts or data forming the basis of his opinion that the operations are performed simultaneously. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”)

Second, Petitioner contends that “the ‘729 patent’s use of the same logical circuit as Van Hook to perform the operations in elements 21(a) through (c) confirms that Van Hook’s operations are performed in one cycle” and that “[t]he prior art need only disclose as much as the ‘729 patent to be invalidating.” Pet. 25 (citing *SRI Int’l, Inc. v. Internet Sec. Sys.*, 511 F.3d 1186, 1194 (Fed. Cir. 2008)). Patent Owner contends Petitioner mischaracterizes the holding in *SRI International* and asserts “Petitioner cannot establish inherent disclosure of the ‘one cycle’ limitation merely by arguing that a disclosure is enabling.” Prelim. Resp. 12, 15.

Here, again, we agree with Patent Owner. The facts of *SRI International* are distinguishable from the facts of the present proceeding and its holding is not applicable to our determination—SRI did not argue that a reference “fails to disclose each of the limitations of the asserted claims,” but rather argued the reference could not anticipate because “it does not provide an enabling disclosure of the claimed invention.” *SRI Int’l*, 511 F.3d at 1192 (citations and internal

quotations omitted). The requirement that a reference is “at least at the same level of technical detail as the disclosure” of the challenged patent is relevant to whether the reference can be considered enabled as an anticipating reference. *Id.* at 1194. We are not persuaded by Petitioner’s second contention because Petitioner relies on the holding in *SRI International* to cure a deficiency of Van Hook—that it does not disclose that the operations recited in limitations (a) through (c) are performed within one cycle, as required by claim 21.

3. Summary

We determine Petitioner does not establish that the claim 21 requirement that each of the operations recited in limitations (a) through (c) are “performed within one cycle” is disclosed, either expressly or inherently, in Van Hook. Accordingly, Petitioner also does not establish that the limitation of claim 22 is disclosed, either expressly or inherently, in Van Hook.

Therefore, we determine Petitioner fails to establish a reasonable likelihood it would prevail in showing that claims 21 and 22 are anticipated under 35 U.S.C. § 102 by Van Hook.

E. Alleged Obviousness Based on Van Hook Alone

Petitioner contends claims 21 and 22 of the ’729 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Van Hook. Pet. 36–38; *see id.* at 20–35. Patent Owner disputes Petitioner’s contention. Prelim. Resp. 13–15. For the reasons that follow, we determine Petitioner has not demonstrated a reasonable likelihood of prevailing as to this ground.

1. Overview of Van Hook

See Section II.D.1.

2. Analysis

Petitioner argues “Van Hook describ[es] the same logical circuit (in greater detail) to do saturation as is described in the ‘729 patent; and the knowledge of one skill[ed] in the art relied upon during prosecution for support of the ‘one cycle’ limitation (as discussed above).” Pet. 38.

At the outset, we note that during prosecution of applications in the priority chain leading to the ‘729 patent, the knowledge of one of ordinary skill in the art was argued in connection with how the ordinarily skilled artisan would understand the pipeline stage diagram in Figure 12B to provide support for the claim term “one cycle.” Ex. 1013, Response to Non-final Office Action dated December 8, 2009, 22. What the ordinarily skilled artisan would have understood Figure 12B of the ‘729 patent to disclose is not dispositive of how the skilled artisan would have viewed Van Hook’s disclosure because Van Hook does not include the same or similar figure. In fact, Petitioner does not point to any teaching or suggestion in Van Hook as to the amount of time it takes the circuitry shown in Figure 8e to produce the desired output of executing the FPACK16 instruction. *See generally* Pet. 36–38.

Moreover, Petitioner’s argument is unsupported by a citation to the Rhyne Declaration and as such, we determine that it is unpersuasive attorney argument. *See In re Geisler*, 116 F.3d 1465, 1471 (Fed. Cir. 1997) (attorney argument cannot take the place of evidence). Thus, arguments made during prosecution of applications in the priority chain leading to the ‘729 patent are not persuasive to support Petitioner’s conclusion that it would have been obvious for Van Hook’s circuitry to perform the operations recited in limitations (a), (b), and (c) of claim 21 “within one cycle.”

3. Summary

We determine Petitioner’s arguments and supporting evidence do not establish sufficiently that the claim 21 requirement that the operations recited in limitations (a) through (c) are “performed within one cycle” is taught or suggested by Van Hook alone. Accordingly, Petitioner also does not establish that the limitation of claim 22 is taught or suggested by Van Hook alone.

Therefore, we determine Petitioner fails to establish a reasonable likelihood it would prevail in showing that claims 21 and 22 are unpatentable under 35 U.S.C. § 103 over Van Hook alone.

F. Alleged Obviousness Based On Van Hook In View Of the Knowledge of One Skilled in the Art, As Described in Patterson

Petitioner contends claims 21 and 22 of the ’729 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Van Hook in view the knowledge of one skilled in the art, as described in Patterson. Pet. 38–43. Patent Owner disputes Petitioner’s contention. Prelim. Resp. 15–17. For the reasons that follow, we determine Petitioner has demonstrated a reasonable likelihood of prevailing as to this ground.

1. Overview of Van Hook

See Section II.D.1.

2. Overview of Patterson

Patterson compares pipelined instruction processing to single-cycle instruction processing and describes performance improvement due to “increasing instruction throughput, as opposed to decreasing the execution time of an individual instruction.” Ex. 1007, 367. In an exemplary five-stage pipeline, Patterson describes executing five instructions at a time, with one instruction in

each pipeline stage. *Id.* at 366. Patterson further teaches that “[a]ll the stages take a single clock cycle, so the clock cycle must be long enough to accommodate the slowest operation” and “[t]he length of a clock cycle is determined by the time required for the slowest pipe stage, because all stages must proceed at the same rate.” *Id.* at 364, 366. According to Patterson, the stages of instruction execution include: instruction fetch (IF), instruction decode and register fetch (ID), execution and effective address calculation (EX), memory access (MEM), and write back (WB). *Id.* at 367. Figure 6.15 of Patterson, which depicts a traditional multiple clock cycle pipeline diagram for two instructions, is reproduced below.

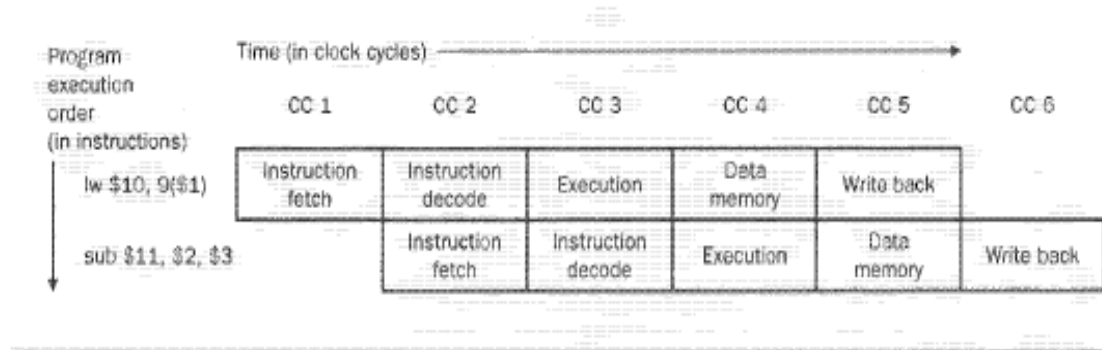


FIGURE 6.15 Traditional multiple-clock-cycle pipeline diagram of two instructions in Figure 6.14.

Figure 6.15 of Patterson

Figure 6.15 of Patterson illustrates the first instruction being executed in one clock cycle (CC3) and second instruction being executed in one clock cycle (CC4).

3. Analysis

Petitioner asserts that Van Hook discloses the saturation processing as discussed above with respect to the ground for challenge based on anticipation by Van Hook (*supra* Section II.D), and cites Patterson for showing that it would have been well known by one of ordinary skill in the art that execution of an instruction in a pipeline stage occurs within one CPU clock cycle. *See* Pet. 41; *see generally*

id. at 17–18. Petitioner contends that both references relate to SPARC (Scalable Processor Architecture) computers because Patterson developed RISC that “became the foundation of the SPARC architecture currently used by . . . Sun” and Van Hook is assigned to Sun Microsystems. *Id.* at 42. Petitioner further asserts:

including the processing of checking for underflow and overflow in the same pipeline stage using circuitry that operates largely at the same time would have the efficiency of not requiring additional circuitry, such as pipeline registers, as well as operating faster. It is common sense that a faster computer is generally better, and thus, one of skill would be motivated for the additional reason to yield a faster processing speed.

Id. (citing Ex. 1021 ¶ 86).

Patent Owner disputes Petitioner’s position. First, Patent Owner argues that the “FPACK16 instruction is not implemented on conventional CPU components but, instead, on a specific ‘graphics execution unit (GRU)’” and asserts “Petitioner fails to provide any evidence that it would have been obvious to implement the specialized ‘graphics execution unit’ (GRU) of Van Hook on the imagined ‘ideal’ pipeline described in the Patterson textbook.” Prelim. Resp. 16. Second, Patent Owner argues there is no link between Van Hook and Patterson because neither suggest implementation (of the FPACK instruction) on a SPARC architecture. *Id.* Third, Patent Owner argues “Petitioner provides no explanation of why one of ordinary skill in the art would look to Patterson to, e.g., decrease the execution time of Van Hook’s FPACK16 instruction when Patterson expressly teaches that such performance is not what its pipelining improves.” *Id.* at 16–17. Lastly, Patent Owner reiterates the argument that enablement cannot show inherent disclosure. *Id.*

Patent Owner’s first argument mischaracterizes Van Hook’s GRU and is contrary to Van Hook’s express disclosure that:

[E]xcept for the incorporated teachings of the present invention, these elements [prefetch and dispatch unit] 46, [integer execution unit] 30, [floating point unit] 26, [integer register file] 36, [floating point register file] 38, [memory management units] 44a–44b, and [load and store unit] 48 are intended to represent a broad category of PDUs, IEUs, FPUs, integer 60 and floating point register files, MMUs, and LSUs, *found in many graphics and nongraphics CPUs*” and “[t]heir constitutions and functions are well known and will not be otherwise described further.

Pet. 42 (citing Ex. 1002, 3:57–64) (emphasis added). Thus, Van Hook’s FPACK16 instruction is implemented by the GRU, which is part of a conventional CPU. *Id.* Moreover, “the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references . . . [r]ather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.” *In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

Although Van Hook’s FPACK instruction is executed on the GRU, the GRU is incorporated into a conventional graphics or non-graphics CPU. *See* Ex. 1002, 3:57–64. Petitioner relies on Patterson as evidence that, during the relevant timeframe, a person of ordinary skill in the art would have known that conventional CPUs employ pipelined instruction processing. *See* Pet. 42–43. Patterson also teaches that pipelined instruction processing includes pipeline stages that each take a single clock cycle. Ex. 1007, 366. In the very same column cited by Petitioner, Van Hook describes the elements found in the graphics and non-graphics CPUs and discloses how these elements, “[t]ogether, . . . fetch, dispatch, execute, and save execution results of the instructions, including graphics instructions, in a pipelined manner.” Ex. 1002, 3:30–32. For these reasons, we

disagree with Patent Owner's second argument that there is no link between Van Hook and Patterson.

Patent Owner's third argument mischaracterizes Petitioner's position— Petitioner relies on Patterson as *evidence*⁵ that conventional CPUs, such as those described in Van Hook, would have implemented pipelined instruction processing. Moreover, Petitioner also does not rely on Patterson specifically for improving the execution time of Van Hook's FPACK16 instruction. *See* Pet. 43. We understand Petitioner's position to be that Van Hook describes implementing the FPACK16 instruction on conventional CPUs, which were known by ordinarily skilled artisans to implement pipelined processing, which Patterson describes and teaches can occur in a single clock cycle, because pipelining was known to increase processing throughput as compared with single cycle processing. *See* Pet. 42 (citing Ex. 1002, 3:57–64); *see* Ex. 1007, 367. We determine that Petitioner's position is supported by Van Hook's disclosure of pipelined instruction processing, as discussed above. *See* Ex. 1002, 3:30–32.

Patent Owner's fourth argument that enablement cannot show inherent disclosure is not persuasive because Petitioner relies on the express disclosure in Patterson to demonstrate that pipelined processing executes an instruction “within one cycle” instead of solely relying on an inherent disclosure in Van Hook. *See* Pet. 42–43; *see* Ex. 1007, 366.

4. Summary

For purposes of this decision, we determine Petitioner sufficiently establishes that each of the limitations recited in claims 21 are taught or suggested

⁵ The Petition challenges claims 21 and 22 based on “Van Hook in View of the Knowledge of One Skilled in the Art, as Described in Patterson.” Pet. 39; *but see id.* at 42 (discussing the combination of Van Hook and Patterson).

by Van Hook in view of the knowledge of one of ordinary skill in the art, as described in Patterson. *See* Pet. 20–36, 38–43. We determine the record supports sufficiently Petitioner’s contentions as summarized above, for purposes of this decision.

On this record and for purposes of this decision, we are satisfied that Petitioner establishes a reasonable likelihood it would prevail in showing that claims 21 and 22 are unpatentable under 35 U.S.C. § 103 over Van Hook in view of the knowledge of one of ordinary skill in the art, as described in Patterson.

G. Alleged Obviousness Based on the MMX References

Petitioner contends claims 21 and 22 of the ’729 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the MMX References. Pet. 43–55. Patent Owner disputes Petitioner’s contention. Prelim. Resp. 17–28. For the reasons that follow, we determine Petitioner has not demonstrated a reasonable likelihood of prevailing as to this ground.

1. Overview of Dulong

Dulong describes executing instructions from a packed instruction set on a processor. Dulong’s packed instruction set 140 includes

instructions for executing Pack with Unsigned Saturation (PACKUS) 141, an Unpack Low Packed data (PUNPCKL) 142, a packed shift right logical (PSRL) 143, a packed shift left logical (PSLL) 144, a packed add (ADD) 145, a packed bit-wise logical OR (POR) 146, a packed bit-wise logical AND (PAND) 147, and a MOVQ operation 148.

Ex. 1003, 3:54–60. Dulong’s packed instruction set 140 can be included in a standard microprocessor instructions set, such as Pentium, PowerPC, and Alpha processor instruction sets. *Id.* at 3:42–50. The PACKUS 141 instruction “converts . . . signed packed words into unsigned packed bytes by packing the low-order

bytes of each signed packed word element from registers 510 and 520 into respective unsigned packed bytes of register 510.” *Id.* at 5:43–47. When the values of the signed packed word elements are negative, the resulting output is clamped to 0x00. *Id.* at 5:48–50. When the values of the signed packed word elements are too large to be represented as an unsigned byte, the resulting output is also clamped to 0x00. *Id.* at 5:50–54.

2. *Overview of Intel MMX 1*

Intel MMX 1 is a Developer’s Guide that describes Intel’s MMX technology including packed byte, packed word, and packed double-word data types. Ex. 1004, 158. Intel MMX 1 further describes the Pentium processor as “an advanced superscalar processor” that includes two general-purpose integer pipelines and a pipelined floating-point unit, which allow the processor to execute two integer instructions simultaneously. *Id.* at 160. Intel MMX 1 describes pack instructions operating on signed input values as well as saturation operations. *Id.* at 189–91.

3. *Overview of Intel MMX 2*

Intel MMX 2 describes packed byte, packed word, packed doubleword, and quadword data types. Ex. 1005, 2-1. Intel MMX 2 further describes the “PACKUS (Packed with Unsigned Saturation) instruction [that] converts signed words into unsigned bytes, in unsigned saturation mode.” *Id.* at 2-6. Intel MMX 2 also describes the PACKUSWB instruction that “packs and saturates four signed words of the source operand and four signed words of the destination operand into eight unsigned bytes.” *Id.* at 5-16. In connection with the PACKUSWB instruction, Intel MMX 2 describes saturating the output value to 0x00 in case of underflow (i.e., when the signed value of the word is smaller than the range of an

unsigned byte) and 0xFF in case of overflow (i.e., when the signed value of the word is larger than the range of an unsigned byte). *Id.*

4. *Overview of Peleg*

Peleg relates to the MMX technology that extends Intel's microprocessor architecture and describes the technology's performance enhancement capability. Ex. 1006, 42. Peleg discloses that "[o]n the first implementation, a Pentium processor, all MMX instructions with the exception of the multiply instructions execute in one cycle." *Id.* at 43.

5. *Analysis*

Petitioner argues one of ordinary skill in the art would have combined Dulong, Intel MMX 1, Intel MMX 2, and Peleg because "[a]ll four references refer to, and describe, the exact same instruction (PACKUS) in the same instruction set (MMX) which executes on the same company's (Intel's) processors." Pet. 44–45.

Patent Owner contends that Dulong discloses a PACKUS instruction that operates differently from the PACKUSWB instruction disclosed in Intel MMX 2. Prelim. Resp. 24. Specifically, Patent Owner argues that Dulong's PACKUS instruction clamps to 0x00 irrespective of whether the signed value is smaller or larger than the range of an unsigned byte. *Id.* (citing Ex. 1003, 5:43–54). Patent Owner further argues Intel MMX 2 describes the PACKUSWB instruction clamping to either 0x00 or 0xFF, depending on whether the signed value is smaller or larger than the range of an unsigned byte. *Id.* at 24–25.

We are persuaded by Patent Owner's argument. When the value of signed input exceeds the range representable by the unsigned output, the PACKUS instruction in Dulong cited by Petitioner outputs a value that is different from the value outputted by the PACKUSWB instruction taught by Intel MMX 2. *Compare*

Ex. 1003, 5:50–54 (“If the signed values . . . are too large to be represented in an unsigned byte, the result elements . . . are clamped to 0x00.”), *with* Ex. 1005, 2-4 (“For example, when the result exceeds the data range limit for signed bytes, it is saturated to . . . 0xFF for unsigned bytes.”). Accordingly, we are not persuaded that Dulong and Intel MMX 2 “refer to, and describe, the exact same instruction (PACKUS).” *See* Pet. 45. For this reason, we determine that Petitioner’s rationale for combining the references is not supported by sufficient evidence of record.

6. *Summary*

For the foregoing reason, we determine Petitioner does not establish sufficiently that the ordinarily skilled artisan would have combined the MMX references. Therefore, we determine Petitioner fails to establish a reasonable likelihood it would prevail in showing that claims 21 and 22 are unpatentable under 35 U.S.C. § 103 over the MMX references.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated there is a reasonable likelihood it would prevail in establishing the unpatentability of claims 21 and 22 of the ’729 patent. At this stage of the proceeding, the Board has not made a final determination as to the patentability of any challenged claim.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 21 and 22 of the ’729 patent on the following asserted ground:

IPR2016-00825
RE43,729

Claims 21 and 22 under 35 U.S.C. § 103(a) as unpatentable over Van Hook in view of the knowledge of one of ordinary skill in the art, as described in Patterson;

FURTHER ORDERED that the trial is limited to the ground identified above, and no other grounds set forth in the Petition are authorized; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, *inter partes* review of the '729 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

FOR PETITIONER:

Kevin P. Anderson
Floyd B. Chapman
Scott A. Felder
WILEY REIN LLP
kanderson@wileyrein.com
fchapman@wileyrein.com
sfelder@wileyrein.com

FOR PATENT OWNER:

Andrew N. Thomases
J. Steven Baughman
ROPES & GRAY LLP
andrew.thomases@ropesgray.com
steven.baughman@ropesgray.com
ipbridgearmptabservice@ropesgray.com