

Paper No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Sony Corporation

Petitioner

v.

Collabo Innovations, Inc.

(record) Patent Owner

Patent No. 5,952,714

DECLARATION OF R. MICHAEL GUIDASH

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1. I, R. Michael Guidash hereby declare as follows:

I. Engagement and compensation

2. I have been retained by Sony Corporation to serve as an expert in the *inter partes* review proceeding described above. I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the grounds of unpatentability set forth in the Petition for *inter partes* review of US 5,952,714 (the '714 Patent). For this service, my billing rate is an hourly consulting fee of \$400/hour, and I am reimbursed for actual expenses. My compensation in no way depends on the outcome of this matter.

II. Summary of opinions

3. It is my opinion that claim 1 is anticipated by Japanese Pat. App. Pub. No. S61-131690 ("Yoshino").

4. It is further my opinion that claim 6 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. S63-221667 ("Izumi").

5. It is further my opinion that claim 7 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. H06-029507 ("Nagano"), in further view of Japanese Pat. App. Pub. No. H07-045803 ("Wakabayashi").

6. It is further my opinion that claim 8 is obvious over Yoshino in view of Izumi or Nagano, in further view of Japanese Pat. App. Pub. No. S60-74880 ("Hirosawa") and Japanese Pat. App. Pub. No. H07-78951 ("Nita").

7. It is further my opinion that claim 9 is obvious over Yoshino in view of Izumi or Nagano.

8. It is further my opinion that claim 10 is obvious over Yoshino in view of Izumi or Nagano, in further view of Wakabayashi.

9. It is further my opinion that claim 11 is obvious over Yoshino in view of Izumi or Nagano, in further view of Japanese Pat. App. Pub. No. H05-006989 (“Onishi”).

10. It is further my opinion that claim 12 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. H05-275611 (“Tobase”).

11. It is further my opinion that claim 13 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. S59-225560 (“Hikosaka”).

12. It is further my opinion that claim 15 is obvious over Yoshino in view of Izumi and Nagano, in further view of Hikosaka.

13. It is further my opinion that claim 16 is obvious over Yoshino in view of Tobase, in further view of Hikosaka.

14. It is further my opinion that claim 1 is obvious over Wakabayashi.

15. It is further my opinion that claims 2-4 are obvious over Wakabayashi, in view of Japanese Pat. App. Pub. No. H06-85221 (“Fujii”).

16. It is further my opinion that claim 5 is obvious over Wakabayashi in view of Fujii, in further view of Onishi.

17. It is further my opinion that claim 13 is obvious over Wakabayashi in view of Hikosaka.

III. Qualifications

18. I started my career with Eastman Kodak as a product engineer for Photometer ASIC's for Kodak film cameras after graduating with a Bachelor of Science in Electrical Engineering from the University of Delaware in 1981. In 1986, I transferred to the Kodak Research Laboratories and CCD wafer fabrication facility. During my time with the Kodak Research Laboratories and CCD wafer fabrication facility, I developed 2um and 1um CMOS processes, and a 30V 4um BiCMOS process. These processes were used for gate arrays for many Kodak products and output driver ASICs for all of Kodak's copiers. During this time, I was also awarded entrance into the Special Opportunity Graduate Program that allowed me to obtain a Master's of Science in Electrical Engineering from the Rochester Institute of Technology.

19. In 1989, I transferred to the Smart Sensor Group which developed BiCMOS-CCD processes to provide fully integrated CCD systems on a chip. I also served as product engineer and yield enhancement engineer for Kodak's high volume CCD's. During this time, I led product delivery and technology development of all ASIC and smart sensor products. I developed a number of products during this time to include an interline CCD integrated with 2um CMOS

on the same chip, the world's 1st pinned photodiode Active Pixel CMOS Sensor, and linear CCD image sensor with on-chip timing and control. I also led & directed the CCD dark current and point defect reduction team.

20. In 1996, I formally started the CMOS Image Sensor group at Kodak. From 1996 to 2009, I managed the R&D and product development of CMOS Image Sensor (CIS) programs. As is further shown in my curriculum vitae, I was the inventor or co-inventor of many key patents in the field of CMOS Image sensors including Pinned Photodiode Pixels, Camera-on-a-Chip architecture, and shared amplifier pixel architectures. During this time, I led the development of the world's 1st pinned photodiode CIS, Megapixel CIS device, and Shared amplifier CIS pixel product and the world's first ½ inch optical format 1.3 megapixel CMOS image sensor into mass production, providing successful delivery to several compact digital camera products. I also led the development of the 1st 3D hybrid stacked BSI CIS architecture. This led to demonstration of very high performance, low dark current BSI prototype sensors with pixel sizes ranging from 0.9um to 5.0um.

21. In 2009, when Kodak closed its CMOS Image Sensor Business, I transitioned into a role as an intellectual property technologist and coordinator. This role included managing remaining image sensor patent applications and office actions, managing broad electronic components patent applications and office

actions, and providing technical support for intellectual property sales and licensing teams.

22. I have since left Kodak and transitioned into a role of providing technical consulting services for CMOS image sensors. In this role I provide consulting services for process, pixels, circuits, sensor architectures, systems and intellectual property to companies and clients.

23. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex. 1026.

IV. My understanding of the relevant law

A. Claim construction

24. I understand that, when a patent is expired, a claim term in an *inter partes* review is to be interpreted in the following manner: First, the language of the claims themselves is of primary importance in the effort to determine precisely what it is that is patented. The terms used in a claim are generally given the ordinary and customary meaning that the terms would have to a person of ordinary skill in the art in question at the time of the alleged invention, unless the term is expressly defined in the patent. The person of ordinary skill in the art reads the claim in the context of the entire patent, including the specification. Next to the language of the claims, the specification is the single best source for interpreting the claim terms. The claims may also be interpreted using the record of

correspondence between the patent applicant and the Patent Office, and also with reference to other sources of evidence that can help to define the meaning of terms to a person of ordinary skill in the relevant time frame. I define the relevant time frame in ¶ 61, below.

B. Anticipation

25. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means that there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim.

26. I understand that an anticipating prior art reference must disclose each of the claim elements expressly or inherently. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure”.

C. Obviousness

27. I understand that a claim in an issued patent can be invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim

elements to be described in different prior art references, so long as there is motivation or sufficient reasoning to combine the references.

28. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the alleged invention was made to a person having ordinary skill in the art to which said subject matter pertains.

29. I understand, therefore, that when evaluating obviousness, one must consider obviousness of the claim “as a whole”. This consideration must be from the perspective of the person of ordinary skill in the relevant art, and that such perspective must be considered as of the “time the invention was made”.

30. The level of ordinary skill in the art is discussed in ¶¶ 52-59 below.

31. The relevant time frame for obviousness, the “time the invention was made”, is discussed in ¶ 61, below.

32. I understand that in considering the obviousness of a claim, one must consider four things. These include the scope and content of the prior art, the level of ordinary skill in the art at the relevant time, the differences between the prior art and the claim, and any “secondary considerations”.

33. I understand that “secondary considerations” include real-world evidence that can tend to make a conclusion of obviousness either more probable

or less probable. For example, the commercial success of a product embodying a claim of the patent could provide evidence tending to show that the claimed invention is not obvious. In order to understand the strength of the evidence, one would want to know whether the commercial success is traceable to a certain aspect of the claim not disclosed in a single prior art reference (i.e., whether there is a causal “nexus” to the claim language). One would also want to know how the market reacted to disclosure of the invention, and whether commercial success might be traceable to things other than innovation, for example the market power of the seller, an advertising campaign, or the existence of a complex system having many features beyond the claims that might be desirable to a consumer. One would also want to know how the product compared to similar products not embodying the claim. I understand that commercial success evidence should be reasonably commensurate with the scope of the claim, but that it is not necessary for a commercial product to embody the full scope of the claim.

34. Other kinds of secondary considerations are possible. For example, evidence that the relevant field had a long-established, unsolved problem or need that was later provided by the claimed invention could be indicative of non-obviousness. Evidence that others had tried, but failed to make an aspect of the claim might indicate that the art lacked the requisite skill to do so. Evidence of copying of the patent owner’s products before the patent was published might also

indicate that its approach to solving a particular problem was not obvious.

Evidence that the art recognized the value of products embodying a claim, for example, by praising the named inventors' work, might tend to show that the claim was non-obvious.

35. I further understand that prior art references can be combined where there is an express or implied rationale to do so. Such a rationale might include an expected advantage to be obtained, or might be implied under the circumstances. For example, a claim is likely obvious if design needs or market pressures existing in the prior art make it natural for one or more known components to be combined, where each component continues to function in the expected manner when combined (i.e., when there are no unpredictable results). A claim is also likely invalid where it is the combination of a known base system with a known technique that can be applied to the base system without an unpredictable result. In these cases, the combination must be within the capabilities of a person of ordinary skill in the art.

36. I understand that when considering obviousness, one must not refer to teachings in the specification of the patent itself. One can, however, refer to portions of the specification admitted to be prior art, including the "BACKGROUND" section. Furthermore, a lack of discussion in the patent specification concerning how to implement a disclosed technique can support an

inference that the ability to implement the technique was within the ordinary skill in the prior art.

V. Technical introduction

A. Background

37. The following is a brief technical background covering some concepts relevant to the '714 patent specification and its claims.

38. The '714 patent has the title “SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF”. It concerns a package for a semiconductor image sensor. An image sensor is a component, used in image capture and optical devices, that converts light into an electrical signal. The electrical signal is generated by semiconductor elements that make up the image sensor, and may be used to generate an image. Image sensors are used in various different types of image capture and optical devices, such as digital cameras, digital scanners, and copiers.

39. Semiconductor devices (sometimes referred to as “chips”), including image sensors, are contained in a housing referred to as a “package”. A package provides protection for the semiconductor device, and also provides electrical connections to circuits external to the device.

40. There are many different types of packages. Some are designed according to industry standards; others are particular to a manufacturer. Some

packages include features appropriate for the type of chip the package houses. For example, an image sensor's package must have an opening to allow light to strike the image sensor. The package's opening is typically covered with a transparent window.

41. The light that enters into the opening of an image sensor's package must strike the photosensitive portions of the image sensor without being obstructed. It must also be aligned with the optical system of the image capture device so that image capture of the scene associated with the light striking the image sensor is accurate.

42. Therefore, an image sensor must be positioned within its package within certain tolerances. Positioning is often performed using optical inspection of the image sensor and package, using measurements taken by an optical device, for example, a video camera.

43. "Mounting" refers to the process of aligning and securing a chip (such as an image sensor) in a package. One method is described in the Admitted Prior Art of the '714 patent:

"FIG. 9 and FIG. 10 depict a conventional solid-state image sensing apparatus. FIG. 9 is a cross section of a solid-state image sensing apparatus in a ceramic package which was once a mainstream. A ceramic package 1, on which metallized conductor 2 is formed, has a concave part 3 in the center thereof. On the concave part 3, a CCD

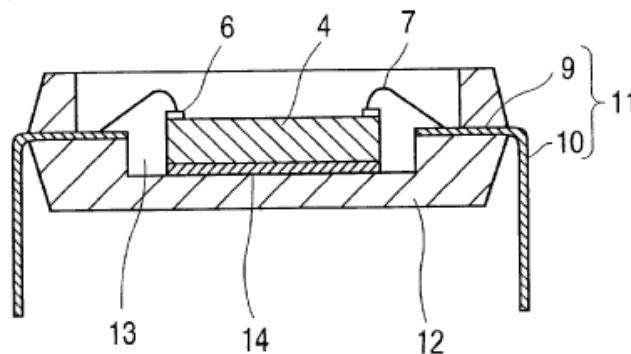
chip 4 is mounted by die bonding, and an electrode pad 6 of CCD chip 4 is wire-bonded to the metallized conductor 2 by a metal lead 7. A lead terminal 8 is deposited to an end face of metallized conductor 2 exposing itself from the side of ceramic package 1.

FIG. 10 is a cross section of a solid-state image sensing apparatus in a plastic package. A lead frame 11 comprising an inner lead 9 and an outer lead 10 is inmolded in a plastic package 12. At a center of the plastic package, a concave portion 13 is situated. The CCD chip 4 is di-bonded [sic.: die-bonded] by conductive paste 14 to the concave portion 13, and the electrode pad 6 on the CCD chip 4 is wire-bonded to the inner lead 9 by the metal lead 7 as same as the case of the ceramic package shown in FIG. 9.” (Ex. 1001, 1:42-61, *see also* Figs. 9 and 10).

44. The above passage from the Admitted Prior Art of the ’714 patent describes an image sensor mounted by “die bonding”. A semiconductor chip is sometimes referred to as a “die” because in fabrication, integrated circuits are typically formed in large batches on a single semiconductor wafer, which is then “diced” into many pieces, each containing a copy of the circuit. Each piece is referred to as a “die”. “Die bonding” refers to affixing the back side of a chip (a “die”) to substrate, for example, the base of a package. This leaves the upper (or front side) surface of the chip exposed. The chip’s upper/front side surface has metal interconnections along its edges with “pads”, which are electrical contacts.

45. Prior art Fig. 10 of the '714 patent (reproduced below and described in the passage described in ¶ 43 above) shows an apparatus constructed in the above-described fashion. Fig. 10 shows an image sensor chip (4) having pads (6). The pads (6) are connected, using wires (7), to flat metallic strips (9 and 10), called “leads”. The leads are divided into two parts: inner leads (9) and outer leads (10). The inner leads are located inside the package and connect to the chip’s pads. The inner leads run into outer leads. The outer leads project out of the package to facilitate connection of the image sensor to external circuitry. (Ex. 1001, 1:53-61).

FIG. 10
PRIOR ART



46. The package of Fig. 10 uses wire bonding (wires 7). This has several problems. Wire bonding limits how small a package can be, since the wires require vertical and horizontal space to make the connections between the pads and the leads. Also, the wires must be carefully placed and bonded to pads (6) and leads (9), which is costly and complex. The materials used and processing time required add to the cost. The requirements that wires be carefully placed and

bonded to the pads adds processing time. Also, wire bonds can cause unwanted reflections of light onto the image sensor.

47. To address these problems, the prior art developed another mounting method. In this method, the inner leads are extended and coated with an amount of a conductive material, referred to as a “bump”. The bumps are press bonded or melted directly onto the contact pads of the chip. This process eliminates the need for intermediate wires (7) and thus leads to space saving and fabrication time.

48. The '714 patent describes a similar, already known optical positioning and bonding process for a package for an image sensor. Figs. 1 (cutaway) and 2 (cross-section) of the '714 patent show the '714 patent's “solid-state image sensing apparatus”, or image sensor package. These figures are reproduced below, and their structure is described in the below passage from the '714 patent's specification. They show a solid-state image sensor (27) mounted in a package (21).

“An exemplary embodiment of the present invention is stated here by referring to FIG. 1, which is a cutaway perspective view of an exemplary embodiment according to the present invention. A lead frame 24 comprising an inner lead 22 and an outer lead 23 is inmolded in a package 21. As FIG. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a smaller opening area is situated, and another opening 26 (hereinafter called ‘inlet’ which has a

wider opening area is situated at the back side thereof. The area of opening 25 is smaller than that of CCD chip 27. An inner lead 22 is exposed from the back side of a step between the opening 25 and the inlet 26, and the inner lead 22 is electrically connected to a bump 29 disposed on an electrode 28 of CCD chip 27.” (Ex. 1001, 4:49-63).

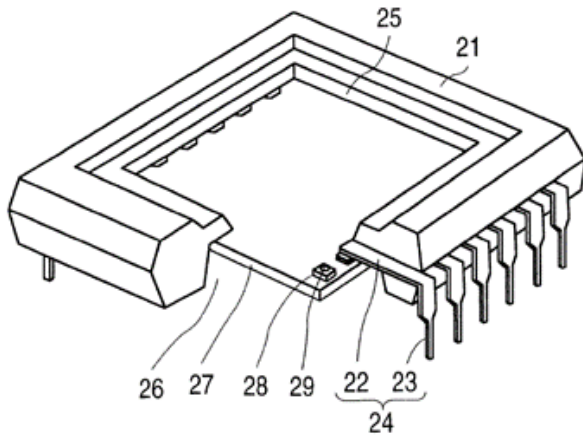


Fig. 1

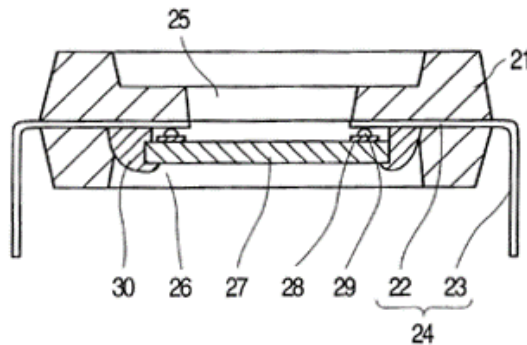


Fig. 2

49. As expected for an image sensor package, package 21 allows light to reach the light-detecting upper/front side surface (not numbered) of image sensor 27, via an opening (25). The opening extends through the package’s center, creating a through hole:

“As FIG. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a smaller opening area is situated, and another opening 26 (hereinafter called ‘inlet’ which has a wider opening area is situated at the back side thereof.” (Ex. 1001, 4:53-58).

As described above, the back of this through hole is indicated by “inlet 26” in Fig.

1. It is the access point for inserting the image sensor into the package. After

being inserted, the image sensor (“CCD chip 27”) is electrically connected to inner leads 22 (which are part of “lead frame (24)”). The image sensor is then secured with an adhesive (30):

“[T]he CCD chip 27 is inserted into the package 21 from the [inlet] 26. Then, the bump 29 is press-fitted and connected to the inner lead 22 which is exposed from a back side of the step situated between the opening 25 and the net 26. During this press-fit operation, a position signal is feedbacked from a optical position adjusting device(not shown) disposed in front of the CCD chip 27 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 27 and disposing the CCD chip 27 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the package 21, and finally, the CCD chip 27 is accurately mounted to the package 21.”
(Ex. 1001, 5:9-22).

50. This arrangement allows light to enter from the top of the package (via opening 25) and reach the light-receiving upper (or front side) surface of the image sensor. That light enters from the top of the package (and that light-receiving surface of the image sensor is its upper surface in the figures) is indicated in the following passages and Figs. 7 and 8 of the ’714 patent (reproduced below). These passages and figures describe minor variations on the ’714 patent’s package

that feature a transparent “glass substrate 49” or “protection panel 56” at the top of the package so as to allow light to reach the upper surface of the image sensor:

“Since the surface on which the circuit elements 43 are formed is situated upward, a shading film 48 is required; however, when defects are found in the CCD chip 41 or the peripheral circuit elements 43, the defective parts can be easily replaced and the other parts also can be used again. In FIG. 7, a glass substrate 49 is made from the shading film by being deposited with metal or by sputtering.” (Ex. 1001, 7:26-32).

FIG. 7

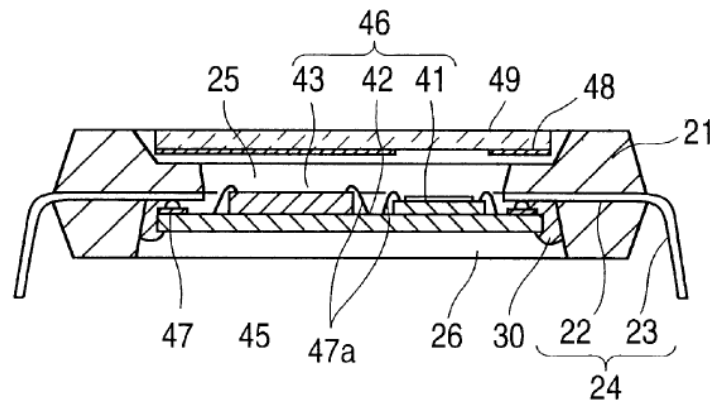
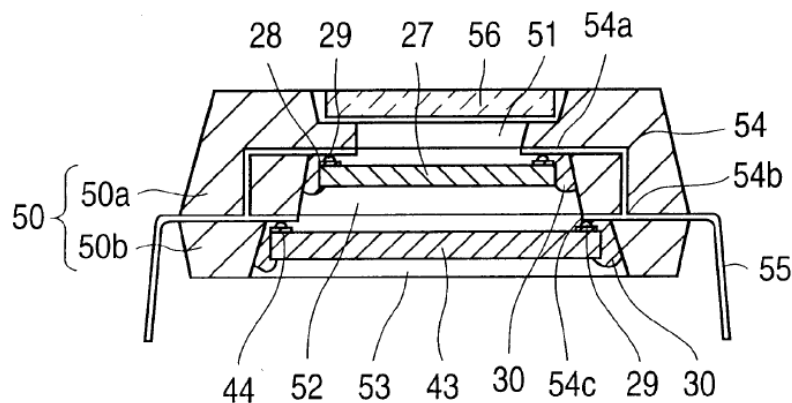


Figure 8, shown below, is described relative to the arrangement as follows:

“A protection panel 56, made of transparent material such as glass, is shown in FIG. 8. The protection panel 56 protects the inside of solid-state image sensing apparatus” (Ex. 1001, 8:43-45).

FIG. 8



51. The '714 patent uses the term “package” somewhat differently from the common understanding of that term. The term “package” in common usage ordinarily refers to the whole apparatus to which the chip is mounted (including, *e.g.*, the lead frame, the transparent lid, etc.). The '714 patent uses the term to refer to just a part of the apparatus—the body part, made, *e.g.*, of “plastic, ceramic or glass”, to which the other components are mounted—which one of ordinary skill would typically have referred to as the package body or substrate. (Ex. 1001, 1:8-9). This usage is shown in the embodiments and figures that consistently label this body part of the assembly as simply the “package”. For example, the following passage describes “package 21” (as seen in Fig. 1) as a separate component from “lead frame 24”. The term is used the same way in the other embodiments. Throughout this declaration, I have adopted the '714 patent’s understanding of the

term “package”, so as to be able to clearly and consistently distinguish between the various elements recited in the ’714 patent and the prior art.

“An exemplary embodiment of the present invention is stated here by referring to FIG. 1, which is a cutaway perspective view of an exemplary embodiment according to the present invention. A lead frame 24 comprising an inner lead 22 and an outer lead 23 is inmolded in a package 21.” (Ex. 1001, 4:49-53; *see also* Fig. 1).

VI. Level of ordinary skill in the art

52. I have considered what the level of ordinary skill in the art of the ’714 patent was in the relevant time frame. In considering the level of ordinary skill, I have taken into account the levels of education and experience of persons working in the field, the types of problems encountered in the field; and the sophistication of the technology. I understand that a person of ordinary skill in the art is a hypothetical person that is deemed to be aware of the content of all analogous prior art.

53. In the relevant time frame, one of ordinary skill in the art of the patent in my opinion would have had a Bachelor’s degree in electrical engineering, physics, or material science and approximately 3-5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience. The levels of education, experience and knowledge can trade off

against one another. I believe that I have at least that level of skill and that I can opine as to the perspective of a person of ordinary skill in the art in the relevant time frame.

54. Examples of particular skills possessed by the person of ordinary skill in the art are visible from the prior art and the specification of the '714 patent.

55. The person of ordinary skill in the relevant time frame would have been familiar with solid-state image sensing devices, including CCD type solid-state image sensing devices. The person of ordinary skill would have been familiar with packages for semiconductor devices, including for solid-state image sensors. The person of ordinary skill would also have been able to employ various standard techniques for mounting a chip (such as a solid-state image sensor) in a package, including mounting a chip face up to the package's base by "die bonding" (Ex. 1001, 1:40-61), and mounting a chip by bonding the chip's pads to the package's leads, as described below.

56. The person of ordinary skill would have known that a package serves to electrically connect the chip housed in the package to external circuits, and would have been familiar with packages that use a lead frame (including inner leads located in the package's interior and outer leads that project outside the package), and would have been able to connect the leads to pads on the chip to make this electrical connection. The person of ordinary skill would also have been

familiar with various methods of connecting a chip's pads to the package's leads, including using wire bonds, bump bonds, or a conductive adhesive such as an anisotropic conductor.

57. The person of ordinary skill would have been familiar with a variety of the different shapes and structures semiconductor packages can take, in particular packages for solid-state image sensors. For example, the person of ordinary skill would have been familiar with multi-chip packages, and would have known that an image sensor may be housed within a single package with a peripheral circuit chip such as an image signal processor. The person of ordinary skill would have been familiar with various different methods of combining multiple chips into a single package, including packages in which chips are mounted on a common substrate inside the package, and packages in which chips are formed on a common semiconductor substrate inside the package, and packages in which multiple chips are mounted separately inside the package.

58. The person of ordinary skill would have known the process steps used in the fabrication of a semiconductor package, including: forming the package itself (*e.g.*, by a molding process) with a lead frame sealed in it such that the inner leads project inside and the outer leads project outside the package; mounting a chip (*i.e.*, a solid-state image sensor or a peripheral chip) on a substrate or forming a chip on a semiconductor substrate; inserting a chip (or substrate on which

multiple chips are formed and/or mounted) into the package; connecting the chip's or substrate's pads to the package's leads via standard bonding methods (*e.g.*, wire bonds, bumps, or an anisotropic conductor); and using an adhesive to secure the chip or substrate to the package.

59. The person of ordinary skill would also have been familiar with the need to precisely adjust the optical positioning of an image sensor (*e.g.*, for use within a lens system). The person of ordinary would be familiar with various methods for performing the optical positioning, such as using reference marks on the image sensor, the package, or a separate positioning element, and using measurements obtained via an optical device to perform an accurate positioning.

VII. Predictability of the art

60. In my opinion, the field of the '714 patent was predictable in the relevant time frame. In particular, the fabrication of a solid-state image sensing apparatus consisting of a package having a through hole in which a solid-state image sensor (or an image sensor and a peripheral circuit chip) are mounted, connected to the inner leads of the package's lead frame, precisely optically positioned, and secured via an adhesive, could be predictably implemented using solid-state image sensor and semiconductor package fabrication techniques readily available to most engineers in the field at the time the '714 patent was filed.

VIII. Relevant time frame for determining obviousness

61. I understand that obviousness must be evaluated at the time the alleged invention was made. From the front page of the '714 patent (left column, field "[30] Foreign Application Priority data"), I understand that the first patent application was filed on Aug. 2, 1995. I will assume for the purpose of this report that Aug. 2, 1995 is the date the purported invention was made, with the understanding that my testimony will also be applicable to some time prior to Aug. 2, 1995, approximately the early 1990s. I may refer to this time period as the "relevant time frame", and my testimony concerning obviousness is directed to this time frame, even if I occasionally do not explicitly use a past tense.

IX. Overview of the claims

62. The '714 patent contains 16 claims. Nine of these claims, 1, 2, 6, 7, 12, 13, 14, 15, and 16, are independent claims, because they do not recite dependencies from any other claims in their preambles.

63. Independent claim 1 of the '714 patent reflects the package described in ¶¶ 48-49 above:

"1. A solid-state image sensing apparatus comprising:
a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,
a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and
a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and

thereby sealing said through hole,
said solid-state image sensing device being secured to said package
via an adhesive.” (Ex. 1001, Claim 1).

64. Claim 1 recites an image sensor mounted in a package. The package has a lead frame consisting of inner leads and outer leads. The package also has a through hole with two openings. One opening is wider than the other. The wider of the openings (which, as shown in Fig. 1, reproduced for ¶ 48 above, is the bottom opening) is used to insert the image sensor into the package. This seals the through hole. The image sensor is the secured to the package using an adhesive—in other words, the image sensor is glued to the package. The remaining claims add various minor features that are addressed below.

X. Overview of the primary prior art references

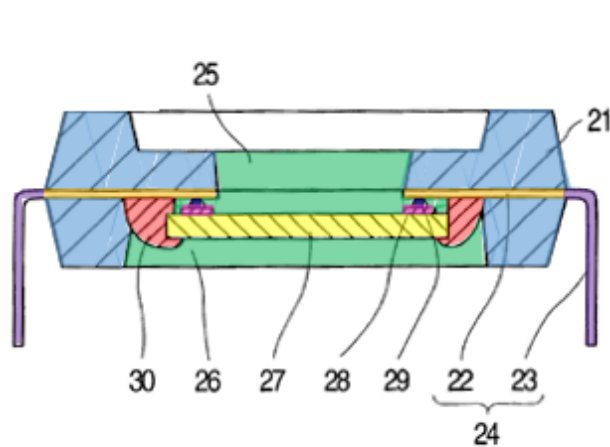
65. Japanese Pat. App. Pub. No. S61-131690 (“Yoshino”) (Ex. 1006, certified translation as Ex. 1003) and Japanese Pat. App. Pub. No. H07-045803 (“Wakabayashi”) (Ex. 1007, certified translation as Ex. 1004), disclose the concepts of claim 1. Yoshino is the base reference applied in Grounds 1-11, for claims 1, 6-13, and 15-16. Wakabayashi is the base reference applied in Grounds 12-15, for claims 1-5 and 13.

A. Overview of Yoshino

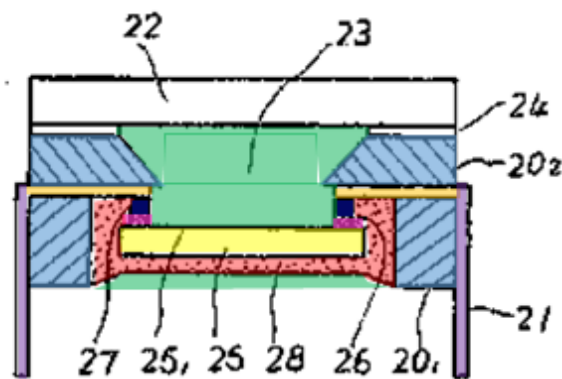
66. Yoshino discloses a package for a solid-state image sensing device, in which the image sensor is mounted in a through hole and bonded to the inner leads, like the '714 patent, as described in the following passage:

“(1) A solid-state image pickup device characterized by comprising a solid-state image sensor, a packaging substrate supporting said solid-state image sensor and having an opening tapered so as to expand the edge as it becomes more distant from said solid-state image sensor’s photoreceptive surface, a light transmitting glass plate adhesive bonded to said packaging substrate so as to cover said opening, and electrode leads connected to said solid-state image sensor’s bonding pads via a conductive bonding material.” (Ex. 1003, p. 1).

67. Petitioner has accurately illustrated similarities between the teachings of Yoshino and the '714 patent in the in the following versions of the '714 patent’s Fig. 2 (left side) and Yoshino’s Fig. 1 (right side). In these figures, Petitioner has accurately highlighted the like elements.



'714 patent Fig. 2



Yoshino Fig. 1

68. For example, Yoshino describes an apparatus like that of claim 1 of the '714 patent. Yoshino's package has a solid-state image sensing apparatus comprising a package ("packaging substrate (20)", highlighted light blue in the above figures) with a through hole ("opening (23)", highlighted green) itself having openings at the top and bottom ends having different areas. Yoshino also discloses a lead frame ("electrode leads (21)"). The inner leads are highlighted orange in the figures above; the outer leads are highlighted purple. Yoshino states:

"FIG. 1 is a cross-sectional view of one example of the invention. In this solid-state image pickup device, the packaging substrate (20), for example, a black ceramic substrate, is constructed by stacking ceramic molded frames (20₁) and (20₂), and the electrode leads (21) are provided in a pin-socket format disposed so as to penetrate the packaging substrate (20) above the ceramic molded frame (20₁). The light transmitting glass plate (22) is hermetically secured to the ceramic molded frame (20₂) using black fritted glass beforehand so as to cover the tapered opening (23) of the packaging substrate (20)."
(Ex. 1003, p. 2).

69. As indicated in the following passage, Yoshino also discloses a solid-state image sensing device ("image sensor (25)", highlighted yellow in the above figures) mounted in the package and secured via an adhesive ("molded resin (28)", highlighted red). Molded resin is a material sometimes used for fabricating a package body or package substrate. When used in the manner taught in Yoshino—

for “supporting the solid-state image sensor (25) in the packaging substrate”—it functions as an adhesive: *i.e.*, it adheres the image sensor to the package body. (Ex. 1003, p. 2).

70. Furthermore, Yoshino discloses elements of other claims. For example, Yoshino discloses connecting an electrode pad (“bonding pads (26)”, highlighted pink in the above figures) of the image sensor to the inner lead via a bump (“conductive bonding material (27)”, highlighted dark blue).

“The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21) aligned therewith are connected via a conductive bonding material (27), for example, indium. The electrode leads (21) are coated with the conductive bonding material (27) by means of plating, brazing, or the like. By supporting the solid-state image sensor (25) in the packaging substrate (20) via a molded resin (28), a desired solid-state image pickup device is obtained.” (Ex. 1003, p. 2).

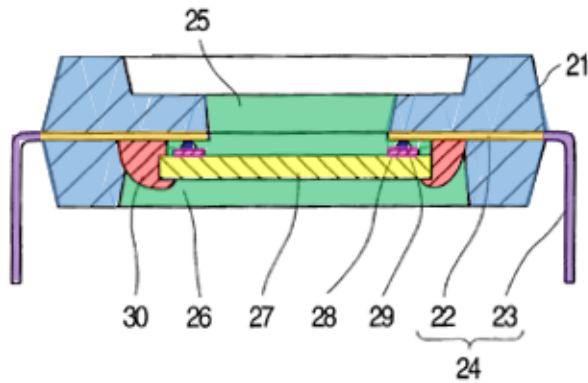
B. Overview of Wakabayashi

71. Wakabayashi discloses the basic embodiments of the ’714 patent. As taught in the following passage and shown in Figs. 1 and 2 of Wakabayashi, Wakabayashi discloses a package in which a solid-state image sensing device is mounted in the through hole of a package, bonded directly to the inner leads, and secured to the package with an adhesive, like claim 1 of the ’714 patent:

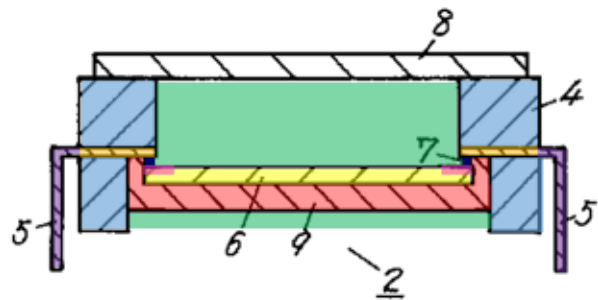
“(Construction) The solid-state image pickup device is comprised of a package 4 made of a transparent resin, leads 5, a CCD chip 6, and bumps 7 which join the inner leads to the CCD chip 4 [sic.: CCD chip 6]. A microlens is formed at the light-receiving face of the CCD chip 6. A space is provided between the microlens face provided at the light receiving face of the CCD chip 6 and the inner face of the light receiving section of the package 4. The spacing can be suitably selected. The package 4 and the leads 5 are produced by transfer molding, or the like, by clamping the lead frame with a pair of dies forming a prescribed cavity.” (Ex. 1004, Abstract).

72. The above passage describes “clamping the lead frame with a pair of dies”. Although a “die” may refer to a semiconductor wafer, this is not what Wakabayashi is referring to here. Rather, the “die” Wakabayashi refers to here is a manufacturing die, which is a specialized manufacturing tool used to cut or shape material such as sheet metal or plastic.

73. Petitioner has accurately illustrated similarities between the teachings of Wakabayashi and the '714 patent in the following versions of the '714 patent's Fig. 2 (left side) and Wakabayashi's Fig. 2 (right side). In these figures, Petitioner has accurately highlighted the like elements. The highlighting indicates the same elements as in the figures (from Yoshino and the '714 patent) discussed in ¶¶ 67-69 above.



'714 patent Fig. 2



Wakabayashi Fig. 2

74. As shown in Fig. 2 and described in the above passage (and also in the passages below), Wakabayashi discloses a package (“package 4”, highlighted light blue in the above figures) having a through hole with different opening areas at its top and bottom end faces. Wakabayashi discloses a lead frame (“lead frame” or “leads 5”) having an inner lead (highlighted orange in the above figures) and outer lead (highlighted purple). Wakabayashi also discloses mounting a solid-state image sensing device (“CCD chip 6”, highlighted yellow in the above passage), in the package, sealing the through hole, using an adhesive (“adhesive resin 7 [sic.: adhesive resin 9]”, highlighted red, labeled “9” in Fig. 2).

“(Claim 1) A solid-state image pickup device characterized by comprising a CCD chip joined via bumps to the inner lead sections of a package made of a transparent resin comprising a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, a space for disposing a CDD [sic.: CCD] chip, the inner lead sections of said lead frame being exposed to the space, and the face opposite to the light-receiving face

being open.” (Ex. 1004, Claim 1).

“(Means for Solving the Problems) The solid-state image pickup device according to the invention has the basic construction of comprising a CCD chip joined via bumps to the inner lead sections of a package made of a transparent resin comprising a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, a space for disposing a CDD [sic.: CCD] chip, the inner lead sections of the lead frame being exposed to the space, and the face opposite to the light-receiving face being open.” (Ex. 1004, ¶ 0005).

“In another aspect, it is constructed by sealing the back face side of the chip with an adhesive resin.” (Ex. 1004, ¶ 0007).

“In FIG. 1, reference numeral 1 is a cross section of the basic construction of the solid-state image pickup device, which includes a package 4 formed with a transparent resin, leads 5, a CCD chip 6, bumps 7 which join the inner lead sections to the CCD chip 4 [sic.: CCD chip 6]. A microlens is formed on the light-receiving face of the CCD chip 6.” (Ex. 1004, ¶ 0010).

“FIG. 2 is a cross section of a solid-state image pickup device in which, in addition to the basic structure discussed above, the back face side of the chip is further sealed with an adhesive resin 7 [sic.: adhesive resin 9]. By constructing the device in this way, the bump joints are reinforced, and at the same time, the penetration of dust from the outside can be prevented.” (Ex. 1004, ¶ 0015).

XI. Construction of the claims

75. My understanding of the legal requirements for claim construction is provided beginning at ¶ 24, above.

76. I have reviewed the claim constructions applied in the petition for *inter partes* review that this declaration supports, and I find that the constructions would have been reasonable to a person of ordinary skill in art in the relevant time frame. I have applied these claim constructions in my analysis in this declaration.

A. Claims 2—“solid-state image apparatus”

77. Claim 1 and 3-16 recite the phrase “solid-state image sensing apparatus”. Claim 2 recites the phrase “solid-state image apparatus”. The ’714 patent—although it does not expressly define the phrase—indicates that a “solid-state image sensing apparatus” may comprise the “solid-state image sensing device”, the package, a lead frame, adhesive, and various other components such as a “substrate ... and a peripheral circuit chip”. For example:

“1. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and

a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and

thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.” (Ex. 1001, 9:20-30).

“6. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,

a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted” (Ex. 1001, 9:59-66).

78. The ’714 does not teach that the entire “solid-state image sensing apparatus” must be solid-state (meaning made of semiconductor material or containing no empty space). Rather, the ’714 patent treats this phrase to mean an apparatus that features a solid-state image sensor. For example, some elements are not necessarily a semiconductor (*e.g.*, the package may be plastic, ceramic, or glass), as indicated in the passage below:

“The present invention relates to a solid-state image sensing apparatus using a solid-state image sensing device (hereinafter called CCD chip) in a package made of plastic, ceramic or glass” (Ex. 1001, 1:6-9).

79. In my opinion, the omission of the word “sensing” in claim 2 does not change the meaning of the phrase.

80. Therefore, I conclude that the term “solid-state image apparatus” should be interpreted interchangeably with the term “solid-state image sensing apparatus”.

B. Claims 2-7, 9-11, 13-16—“electrode pad(s)”

81. The ’714 patent does not expressly define this phrase. The specification also refers to “electrode pad(s)” in one place (as follows) as an “electrode”, but in my opinion this does not have any impact on the meaning of the term:

“An inner lead 22 is exposed from the back side of a step between the opening 25 and the inlet 26, and the inner lead 22 is electrically connected to a bump 29 disposed on an electrode 28 of CCD chip 27.” (Ex. 1001, 4:59-63).

82. The ’714 patent indicates (in the claims and the following passages from the specification) that an “electrode pad” is an electrical connection point on a “solid-state image sensing device”, “peripheral circuit chip”, or “substrate”. For example:

“The bump 29 is formed on the electrode pad 28 of the CCD chip 27” (Ex. 1001, 5:6-8).

“A bump 29 disposed on an electrode pad 44 of the peripheral circuit elements is connected to an electrode pad 45 of the group of wirings on the substrate 42” (Ex. 1001, 6:7-9).

“connecting an electrode pad of the solid-state image sensing device” (Ex. 1001, 10:64-65).

83. The '714 patent also indicates that the “electrode pad(s)” electrically connect the device or substrate to conductive elements in the package: to the inner lead of the “lead frame” or, in the Admitted Prior Art, a “metallized conductor”.

For example:

“The electrode pad of solid-state image sensing apparatus is coupled to the inner lead via a bump or an anisotropic conductor having only vertical conductivity so that optical positioning as well as electrical connecting is completed.” (Ex. 1001, 3:6-10).

“The electrode pad disposed around the upper surface of the substrate is connected to the inner lead via the bump or anisotropic conductor so that the optical positioning as well as electrical connection is completed.” (Ex. 1001, 3:23-26).

“The CCD chip is loaded into the through hole of the package from the opening which has the wider opening area, and the electrode pad is connected to the first inner lead via the bump or the anisotropic conductor so that optical positioning as well as electrical connection is completed.” (Ex. 1001, 3:53-63).

“connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity” (Ex. 1001, 10:64-66).

84. Therefore, I conclude that “electrode pad(s)” should be construed as “an electrical connection point on a substrate or semiconductor device.”

C. Claims 3, 9, 13-16—“bump”

85. The ’714 patent does not expressly define “bump”. The ’714 patent teaches that a “bump” is a means by which the pads (of the image sensor, peripheral chip, or substrate) electrically connected to a lead. This is shown, for example, in the passages from the ’714 patent cited in ¶ 83 above. (*E.g.*, Ex. 1001, 3:6-10; 3:23-26; 3:53-63; 10:64-66). Thus, one of ordinary skill would have understood the term to mean an amount of conductive material used for electrically connecting the device using a number of different methods. This agrees with the definition of the term found in Charles A. Harper & Martin B. Miller, *Electronic Packaging, Microelectronics, and Interconnection Dictionary* (1993) (“Harper”)(Ex. 1012):

“A small metal mound or hump that is formed on the chip or the substrate bonding pad and is used as a contact in face-bonding. It is a means of providing connections to terminal areas of a device.” (Ex. 1012, p. 23).

86. Therefore, I conclude that “bump” should be construed as “an amount of conductive material used for an electrical connection.”

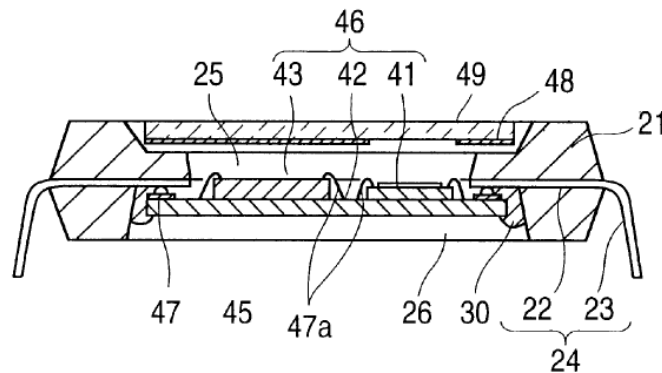
D. Claim 8—“covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device”

87. This phrase in claim 8 does not require that the shading film be located *on* the substrate. Instead, it means that the shading film “covers” in the sense of “provides shade for” an entire upper surface of said substrate except an upper surface of the solid-state image sensing device. This is to protect the peripheral circuit elements on the substrate from light, which can interfere with the function of those elements.

88. Thus, this phrase means that the shading film could be on the substrate itself, or it could be *above* the substrate, as shown in the '714 patent's Fig. 7. Fig. 7 shows the only embodiment in the specification that features a shading film. As seen in Fig. 7 (and described in the below passage), this embodiment places “shading film 48” above the substrate (42), on the package's glass cover (“glass substrate 49”):

“Since the surface on which the circuit elements 43 are formed is situated upward, a shading film 48 is required In FIG. 7, a glass substrate 49 is made from the shading film by being deposited with metal or by sputtering.” (Ex. 1001, 7:26-32).

FIG. 7



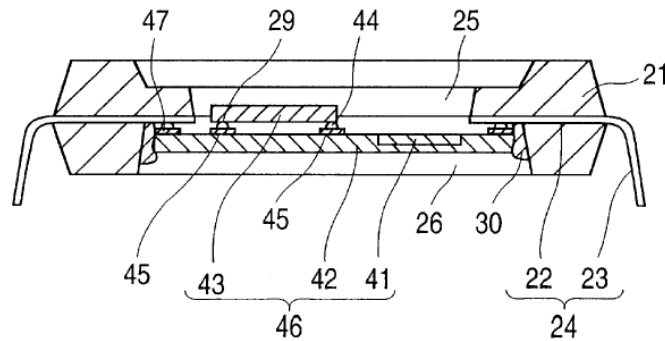
89. Also, claim 8 is multiply dependent from claim 6 or claim 7. Claim 6 discloses a solid-state image sensing device and a peripheral circuit chip “mounted” on the substrate. (Ex. 1001, 9:65-66). If “covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device” required that the shading film actually be on the surface of the substrate, then in this case (because the peripheral chip is *mounted* on the substrate’s surface), the shading film would not provide shade for the peripheral circuit chip. *I.e.*, the film would be *on* the substrate, underneath the mounted peripheral chip, rather than above the peripheral chip. Thus, the shading film would not fulfill its function of protecting the peripheral chip from light.

90. Thus, it is my opinion that this phrase should be construed to require that the shading film is located on or above the entire upper surface of the substrate except for the portion of the substrate on which the solid-state image sensing device is disposed.

E. Claim 7—“plastic package”

91. Although claim 7 recites both a “package” and a “plastic package”, there is no embodiment of the ’714 patent with two packages. Claim 7 corresponds to Fig. 5 (reproduced below), which depicts only one package.

FIG. 5



92. Thus, it is my opinion that the term “plastic package” refers back to the earlier recitation of the term “package”. It is further my opinion that the term “plastic package” in claim 7 should be construed to refer to the earlier use of the term “package”, which is a shorthand reference for “plastic package”.

F. Claim 15—“substrate”/“semiconductor substrate”

93. Claim 15 recites mounting an image sensor and peripheral chip on “a substrate”, then “inserting the semiconductor substrate”, then connecting “the substrate”, then securing “the semiconductor substrate”. In particular, Claim 15 recites:

“mounting said solid-state image sensing device and said peripheral circuit chip on a substrate where a group of wirings is disposed in

order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings,
inserting the semiconductor substrate into the through hole,
connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, and
securing the semiconductor substrate” (Ex. 1001, 11:36-12:9).

94. It is my opinion that claim 15 discloses only one substrate, and that “semiconductor substrate” here refers back to the “substrate”. This is shown by Figs. 6 and 7 of the ’714 patent (reproduced below), which correspond to claim 15, and supported by the following passages from the specification which describe those figures.

“FIG. 6 is a cross section of the solid-state image sensing apparatus used in Embodiment 5 of the present invention. This embodiment is one of variations of Embodiment 4 described above. The method of accurately mounting the CCD chip 41 to the package 21 is the same as that of the Embodiment 4 from the standpoints of structure and manufacturing, namely, the CCD module 46 on which the CCD chip, peripheral circuit elements and the group of wirings are formed, is inserted from the inlet 26, and the CCD module 46 is fixed to the package 21, while the optical position of CCD chip 41 is fine adjusted. A different point from the Embodiment 4 is this: in

Embodiment 4, the CCD chip is formed directly on the semiconductor substrate, which is to be the substrate 42 of the CCD module 46, through a circuit-chip-forming-process such as a direct diffusion process, on the other hand in Embodiment 5, the CCD chip 41 as well as peripheral circuit elements 43 was already produced in a separate process, and the CCD chip 41 and peripheral circuit elements 43 are disposed on the substrate 42 on which the group of wirings have been formed, and thereby they are electrically connected to form the CCD module 46.

Accordingly, the substrate 42 used in this embodiment may be made of a material other than semiconductor. As shown in FIG. 6, when the CCD chip 41 produced in the separate process is mounted on the substrate 42, the electrode of CCD chip 41 is wire-bonded to the electrode terminal of the group of wirings by using a metal wire 47a.

FIG. 7 is a cross section of the solid-state image sensing apparatus used in Embodiment 6. This embodiment is also one of variations of Embodiment 5 above mentioned. A different point from Embodiment 5 is this: in Embodiment 5, the peripheral circuit elements 43 are connected to the substrate 42 via the bump 29 in the face-down way same as that in Embodiment 4; however, in this Embodiment 6, the peripheral circuit elements 43 are disposed on the substrate 42 in the face-up way(the face on which a circuit is formed is situated upward) as the CCD chip 41 is in Embodiment 5, and the electrode of peripheral circuit elements is wire-bonded to the electrode terminal of the group of wiring by using the metal wire 47a.” (Ex. 1001, 6:29-7:2).

A cross-sectional diagram of a cable assembly. The outer jacket (21) contains several internal layers. From top to bottom, there are conductive layers (25, 46), an insulating layer (48), another conductive layer (49), and a braided shield (47). Inside the shield, there are twisted pairs (45, 47a) and other conductive elements (26, 30). A central core (22) is surrounded by a braid (23) which is part of a larger assembly (24).

XII. Claim 1 is anticipated by Yoshino.

96. It is my opinion that Claim 1 is anticipated by Japanese Pat. App. Pub. No. S61-131690 (“Yoshino”) (Ex. 1006, certified translation as Ex. 1003).

B. Yoshino is prior art

C. Summary of Yoshino

99. Yoshino is summarized in ¶¶ 66-69 above.

D. Element-by-element analysis of claim 1 over Yoshino

1. Claim 1

[1a]. “A solid-state image sensing apparatus comprising:”

100. In the following passage, Yoshino discloses a solid-state image sensing apparatus (an apparatus comprising a “solid-state” image sensing device):

“A solid-state image pickup device characterized by comprising a solid-state image sensor, a packaging substrate supporting said solid-state image sensor” (Ex. 1003, p. 1, Claim 1).

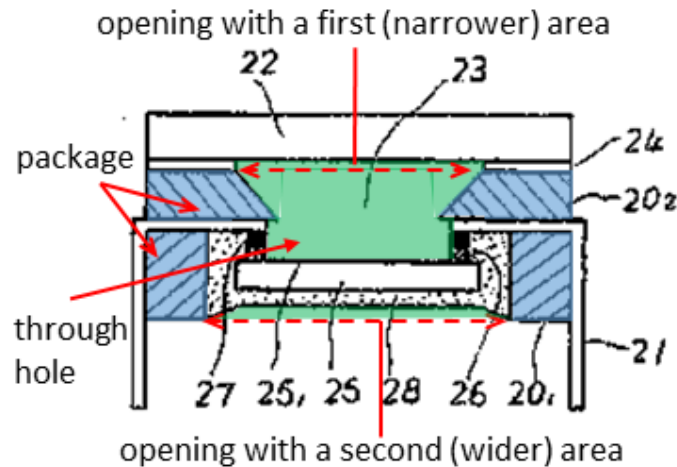
“[1b]. a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,”

101. In the following passage, Yoshino teaches a package having a through hole therein:

“a packaging substrate supporting said solid-state image sensor and having an opening tapered so as to expand the edge” (Ex. 1003, p. 1, Claim 1).

102. Below is a version of Yoshino’s Fig. 1 that Petitioner has annotated to accurately show the through hole, and that the package has openings on both end faces thereof, and different opening areas of said openings. The package (“packaging substrate (20)”) is highlighted in light blue and the through hole

(“tapered opening (23)”) is highlighted in green. (Ex. 1003, p. 2). The openings on both end faces, having different opening areas, are indicated with red arrows.



103. Yoshino’s Fig. 1 shows the apparatus after one end is covered by “glass plate (22)” and the through hole is sealed by an adhesive (“molded resin 28”). (Ex. 1003, p. 2). Yoshino’s openings are nevertheless essentially the same as those of the ’714 patent. With regard to Yoshino’s top opening, the ’714 patent also teaches that one opening may be covered by glass “protection panel 56 [which] protects the inside of solid-state image sensing apparatus”:

“A protection panel 56, made of transparent material such as glass, is shown in FIG. 8. The protection panel 56 protects the inside of solid-state image sensing apparatus; however, whether using of this protection panel 56 or not does not change the functions as well as effects of the present invention described in the above embodiments.” (Ex. 1001, 8:43-48).

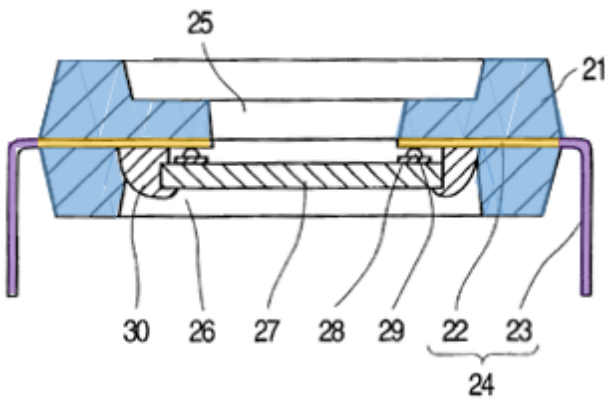
With regard to Yoshino's bottom opening, the '714 patent also requires that this opening be sealed with an image sensor, followed by application of an adhesive, as discussed with regard to claim element [1d] in ¶¶ 106-113 below.

“[1c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and”

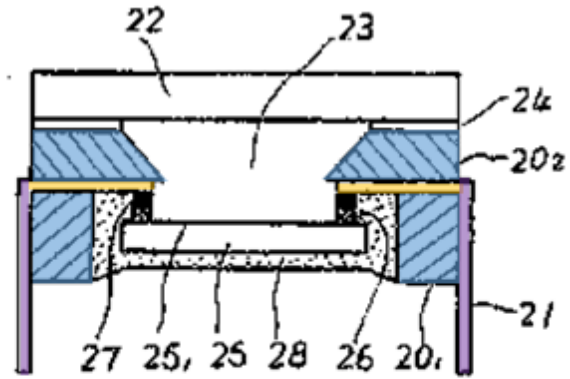
104. Yoshino discloses “electrode leads (21)”, which is a lead frame comprising inner leads and outer leads, in the following passage:

“The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21) aligned therewith are connected via a conductive bonding material (27), for example, indium.” (Ex. 1003, p. 2).

105. Petitioner has accurately highlighted the '714 patent's Fig. 2 (reproduced below on the left side) and Yoshino's Fig. 1 (below on the right side), to show that Yoshino's lead frame is nearly identical to that of the '714 patent. For reference, the '714 patent labels its lead frame as “inner lead 22” and “outer lead 23” of “lead frame 24”. (Ex. 1001, 4:52-53). In both figures, Petitioner has highlighted the inner leads orange. The outer leads are highlighted purple. The figures also show that Yoshino's lead frame is sealed in said package (highlighted blue), just as the lead frame of the '714 patent is.



'714 patent Fig. 2



Yoshino Fig. 1

“[1d]. a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.”

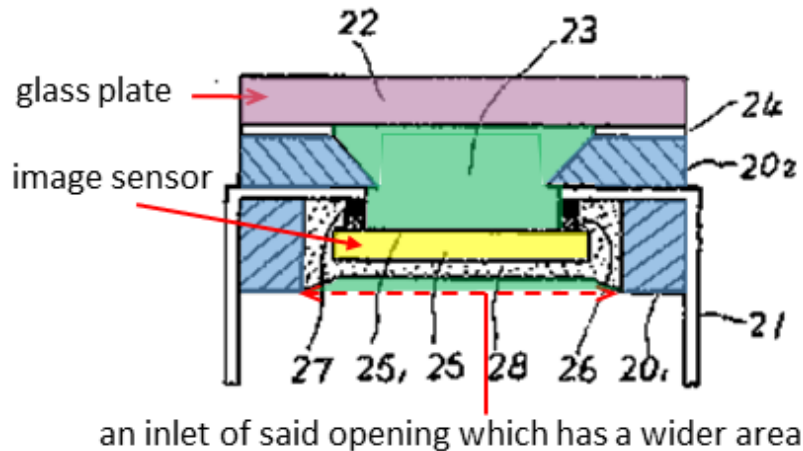
106. Yoshino teaches that the image sensor is mounted in the package by being inserted from an inlet of said opening which has a wider area. As indicated in the below passages, Yoshino teaches that the package is assembled and “light transmitting glass plate (22)” is affixed to it, and *then* the image sensor is placed onto the inner lead of the lead frame.

“FIG. 1 is a cross-sectional view of one example of the invention. In this solid-state image pickup device, the packaging substrate (20), for example, a black ceramic substrate, is constructed by stacking ceramic molded frames (201) and (202), and the electrode leads (21) are provided in a pin-socket format disposed so as to penetrate the packaging substrate (20) above the ceramic molded frame (201). The light transmitting glass plate (22) is hermetically secured to the

ceramic molded frame (202) using black fritted glass beforehand so as to cover the tapered opening (23) of the packaging substrate (20). The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21) aligned therewith are connected via a conductive bonding material (27), for example, indium.” (Ex. 1003, p. 2).

“[N]o heating is required in the step of incorporating the solid-state image sensor (25) into the packaging substrate (20) to which the light transmitting glass plate (22) has already been hermetically bonded.” (Ex. 1003, p. 2).

107. Below is a version of Yoshino’s Fig. 1 that Petitioner has accurately annotated and highlighted to show that “light transmitting glass plate (22)” covers the narrower opening. Thus, since Yoshino teaches that the image sensor is inserted (“placed” or “incorporate[ed]”), there are only two openings, and the narrower opening is covered at the time the image sensing device is inserted, Yoshino teaches that the image sensing device is inserted into the wider opening. In the below version of Fig. 1, Petitioner has highlighted the glass plate purple. The image sensor, highlighted yellow, is inserted into the wider opening of the through hole (highlighted green) of the package (highlighted blue).



108. Fig. 1 shows the bottom (wider) opening sealed by “molded resin (28)”. (Ex. 1003, p. 2). As discussed in ¶ 69 above, molded resin is a material sometimes used in the fabrication of package bodies that functions here as an adhesive. It serves here to secure the image sensor to the package, just as in the ’714 patent. It does not prevent the image sensor from being inserted into the wider opening, since it would not be applied until after the image sensor was inserted. It would make no sense to apply the adhesive (as it is shown in Fig. 1, on the back side of the image sensor) before the image sensor was inserted.

109. Fig. 1 shows a cross-section of the package disclosed by Yoshino. As shown by the hatching on the cross-sectional faces of the package, such a package would extend all the way around or enclose the image sensor. This is typically the case for this type of package, in order to protect the chip. In an image sensor package, also, the packaging substrate would extend all the way around the package so that only wanted light, received through the light receiving window on

the top of the package, would strike the image sensor. If the package were open along the sides or periphery, unwanted light would strike the image sensor. This would interfere with accurate image capture.

110. Also, the passage cited in ¶ 106 above describes the “light transmitting glass plate (22)” as “hermetically secured”. In order for the glass plate (22) to be “hermetically secured” the packaging substrate 202 would have to extend all the way around the package.

111. Thus, there would have been no side openings through which the image sensor could be inserted. Since the narrower (top) opening is covered by the glass plate, the image sensor could only have been inserted through the wider opening, shown as the bottom opening in Fig. 1. This is inherent in Yoshino’s disclosure. If it is not inherent, it is my opinion that it is at least obvious.

112. Yoshino teaches the image sensor sealing the through hole, since Yoshino’s Fig. 1 shows the image sensor blocking the through hole in the same manner as the ’714 patent.

113. Finally, Yoshino discloses the image sensor being secured to said package via “molded resin (28)”, as recited in the passage below. As discussed in ¶ 69 above, molded resin is a material sometimes used in the fabrication of package bodies that functions here as an adhesive.

"By supporting the solid-state image sensor (25) in the packaging

substrate (20) via a molded resin (28), a desired solid-state image pickup device is obtained." (Ex. 1003, p. 2).

114. Thus, for the foregoing reasons, I conclude that claim 1 was anticipated by Yoshino.

XIII. Claim 6 is obvious over Yoshino in view of Izumi.

A. Summary of opinion

115. It is my opinion that Claim 6 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. S63-221667 ("Izumi") (Ex. 1017, certified translation as Ex. 1016).

B. Izumi is prior art

116. I understand that Izumi is prior art to the '714 patent, because it was published on September 14, 1988.

C. Summary of Izumi

117. Izumi discloses a package in which a solid-state image sensor and a peripheral circuit chip are mounted on a common substrate ("sealing base substrate 1C"), as disclosed in claim 6 (and also in claim 15, as discussed in ¶¶ 232-240 below). (Ex. 1016, p. 336; Fig. 2).

D. Element-by-element analysis of claim 6 over Yoshino in view of Izumi

1. Claim 6

"[6a]. A solid-state image sensing apparatus comprising:"

118. As discussed for claim element [1a] in ¶ 100 above, Yoshino discloses a solid-state image sensing apparatus.

“[6b]. a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,”

119. As discussed for claim element [1b] in ¶¶ 101-103 above, Yoshino discloses a package having a through hole, openings on both end faces thereof, and different opening areas of said openings.

“[6c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,”

120. As discussed for claim element [1c] in ¶¶ 104-105 above, Yoshino discloses a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package.

“[6d]. a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted being inserted into the package from a wider opening thereof, and”

121. As discussed for claim element [1d] in ¶¶ 106-111 above, Yoshino discloses a solid-state image sensing device mounted by being inserted into the package from a wider opening thereof. As discussed below, it would have been obvious to use a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted, such as that taught in Izumi, in place of Yoshino’s single solid-state image sensing device.

122. Izumi teaches a package for a solid-state image sensing device and a peripheral circuit chip that are mounted on a common substrate, in a similar context as the '714 patent. This is disclosed in the following passages from Izumi, with reference to Fig. 2 (reproduced below). Fig. 2 depicts the arrangement of components mentioned in the passages below as the second embodiment. In both embodiments, a solid-state image sensing device (“solid state imaging element chip 2”) and a peripheral circuit chip (*e.g.*, “peripheral circuit chips 4A to 4D”) are both mounted on a common substrate (“sealing base substrate 1C” in embodiment II, which is part of the “package member 1” described in embodiment I):

“Embodiment I is an embodiment of the present invention wherein the present invention is applied to a solid state imaging device which has a package part formed of a ceramic material. ...

As shown in Figure 1, the solid state imaging device is principally constructed of package member 1, first cavity part 1A, second cavity part 1B, solid state imaging element chip 2, peripheral circuit chip 3, peripheral circuit chips 4A to 4D, leads 5, glass cap 6 and resin sealing material 7. ...

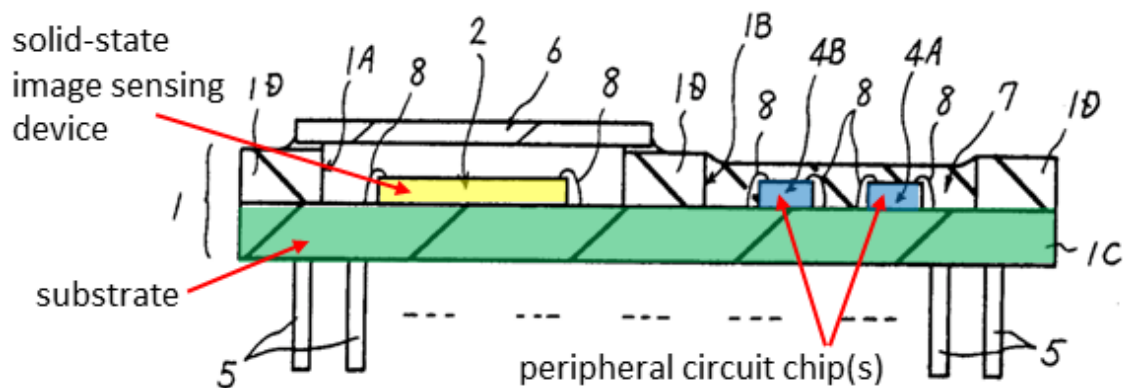
First cavity part 1A and second cavity part 1B are respectively constructed to form package member 1 in a concave shape. Solid state imaging element chip 2 is furnished within first cavity part 1A. Second cavity part 1B is furnished in a different position from and independently to first cavity part 1A, and peripheral circuit chips 3 and 4A to 4D are furnished within it.” (Ex. 1016, p. 335).

“Embodiment II is an another embodiment of the present invention wherein the present invention is applied to a solid state imaging device with a package member that is formed of a resin material. ...

As shown in Figure 2, the solid state imaging device is formed such that package member 1 is comprised of sealing base substrate 1C, and frame member 1D which forms each of first cavity part 1A and second cavity part 1B. Each of sealing base substrate 1C and frame member 1D is formed of a resin material such as glass epoxy resin.

In addition to the effects described in the aforementioned Embodiment I, a solid state imaging device constructed in this manner is able to be formed in a low cost manner as a result of package member 1 being formed of a resin material.” (Ex. 1016, p. 336, *see also* Fig. 2).

123. Below is a version of Fig. 2 that Petitioner has accurately highlighted to show “base substrate 1C” (green), on which “solid state imaging element chip 2” (yellow) and “peripheral circuit chips 4A to 4D” (blue) are mounted.



124. In describing Fig. 2, Izumi's specification notes the "internalization" (moving into the package) of the peripheral chips, and one advantage of doing so (noise reduction):

"[N]oise in the output signal of solid state imaging element chip 2 is reduced through the internalization of peripheral circuit chips 4A to 4D As shown in Figure 2, the solid state imaging device is formed such that package member 1 is comprised of sealing base substrate 1C, and frame member 1D" (Ex. 1016, p. 336).

125. In the above passages (and as shown in Fig. 2), Izumi recites mounting the image sensor and peripheral circuit chip in separate "cavity parts". However, Izumi recognizes a prior art device that mounts the image sensor and peripheral circuit chip (a "pre-amp") in a single chamber, as in the '714 patent. Izumi states:

"The inventors have developer [sic.] a solid state imaging device with an internal pre-amp in order to increase the S/N ratio of the output signal of the aforementioned solid state imaging device. A construction is adopted such that by packaging a pre-amp in the same package as the solid state imaging element chip, the output signal may be amplified while minimizing the generated noise, and this amplified output signal output to an external amp. The pre-amp is comprised so as to be hermetically sealed within the same cavity part as the solid state imaging element chip." (Ex. 1016, p. 334, Problems to be Solved...).

Furthermore, claim 6 does not require the solid-state image sensing device and a peripheral circuit chip to be in the same cavity of a package. The claim only requires that the image sensor and peripheral chip be in the same package.

126. One of ordinary skill would have been motivated to use the substrate (and package divider with two cavity parts) disclosed in Izumi with Yoshino's package. Doing so would provide several advantages. First, putting a peripheral circuit chip and image sensor on a common substrate provides a reduction in noise, as noted in the passage cited in ¶ 124 above. Doing so also provides a shorter signal path. This lowers power consumption and increases speed, features which are commercially valuable. Putting a peripheral circuit chip and image sensor on a common substrate also protects the peripheral circuit chip and takes up less space overall than if the chip were mounted outside the package. Placing Izumi's substrate in Yoshino's package provides the advantage of reduced size over a package that uses wire bonds to connect the substrate. Also, Izumi's use of a substrate on which to mount chips (such as an image sensor and a peripheral circuit chip) was a known variation to Yoshino's base system which would have had no unexpected results.

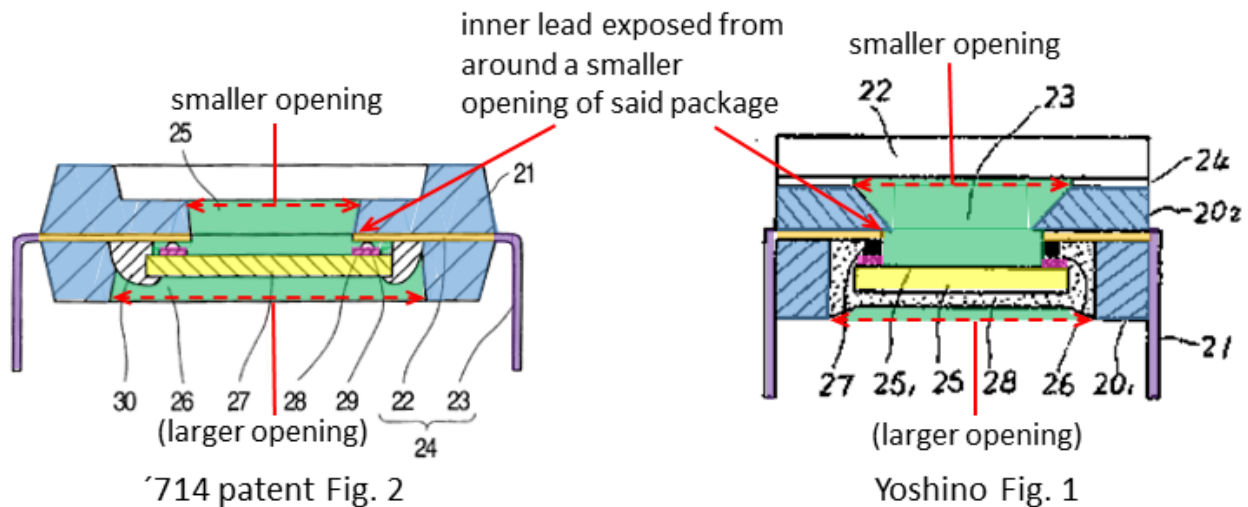
“[6e]. an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,”

127. Yoshino discloses an electrode pad of an image sensor being connected to said inner lead. (Ex. 1003, p. 2). Yoshino refers to its image sensor's electrode pads as "bonding pads (26)", as follows:

"The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21) aligned therewith are connected" (Ex. 1003, p. 2).

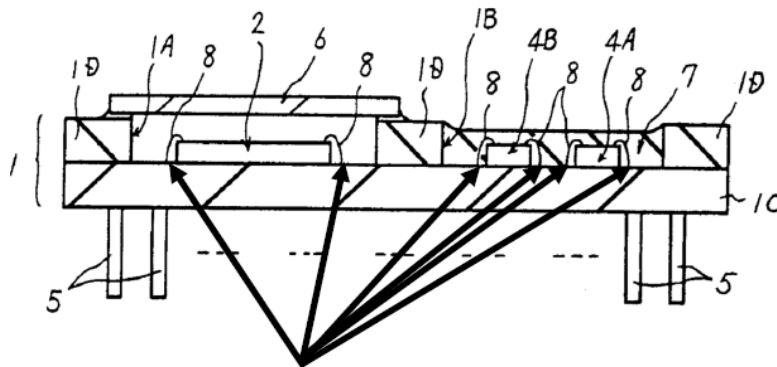
128. As the above passage makes clear, "bonding pads (26)" electrically connect "solid-state image sensor (25)" to the leads. Thus, "bonding pads (26)" are electrical connection points on a semiconductor device, *i.e.*, electrode pads.

129. Yoshino also discloses said inner lead exposed from around a smaller opening of said package. This is shown in the version of Yoshino's Fig. 1 below, which Petitioner has accurately highlighted to show the inner lead (highlighted orange) exposed from around a smaller opening of said package. This is the same arrangement as in the '714 patent. The '714 patent's Fig. 2 is also reproduced, similarly annotated by Petitioner to illustrate the arrangement. The highlighting in the below comparison indicates the like elements of the two figures, as discussed in ¶¶ 67-70 above.



130. As discussed for claim element [6d] in ¶¶ 121-126 above, it would have been obvious to one of ordinary skill to use Izumi's substrate in place of Yoshino's image sensor.

131. Izumi also discloses a connection to its substrate that would obviously have involved an electrode pad (*i.e.*, a contact pad). Izumi teaches that its image sensor and peripheral chips have upward facing contacts that are wire-bonded to the substrate, as shown in Izumi's Fig. 2 (shown below with annotations by Petitioner that indicate the locations of the pads). The connection to the substrate would obviously have involved a contact pad, because the wire bond must connect to a conductive electrode on the surface of the semiconductor substrate in order for an electrical circuit to be maintained.



Location of contact pads

132. Izumi also teaches that the contacts on each of its chips are eventually electrically connected to the package's leads, by means of the wire bond connections from the chip, in the following passage:

"In the same manner as solid state imaging element chip 2, this peripheral circuit chip 3 is connected to leads 5 and solid state imaging element chip 2 through interposed bonding wires 8 and wiring". (Ex. 1016, p. 335, middle).

133. It would have been obvious in Izumi to connect bonding pads on the surface of the semiconductor substrate to inner leads of Yoshino, because the bonding pads serve the same purpose as those of Yoshino. A person of ordinary skill would have known to use the existing wiring of Izumi's substrate to route electrical connections to points where they connect to the leads of Yoshino's package (rather than routing the connections to points where they connect to Izumi's leads (5)).

"[6f]. said substrate being secured to said package via an adhesive."

134. As discussed for claim element [1d] in ¶ 113 above, Yoshino discloses the solid-state image sensing device being secured to said package via an adhesive. As discussed for claim element [6d] in ¶¶ 121-126 above, it would have been obvious to one of ordinary skill to use Izumi's substrate in place of Yoshino's image sensor.

135. Thus, for the foregoing reasons, I conclude that claim 6 was obvious over Yoshino in view of Izumi.

XIV. Claim 7 is obvious over Yoshino in view of Nagano, in further view of Wakabayashi.

A. Summary of opinion

136. It is my opinion that Claim 7 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. H06-029507 ("Nagano") (Ex. 1019, certified translation as Ex. 1018), in further view of Japanese Pat. App. Pub. No. H07-045803 ("Wakabayashi") (Ex. 1007, certified translation as Ex. 1004).

B. Nagano is prior art

137. I understand that Nagano is prior art to the '714 patent, because it was published on February 4, 1994.

C. Summary of Nagano

138. Nagano discloses a "photodiode with a computing function"—*i.e.*, a device in which: (1) a solid-state image sensor ("light receiving part [2] for converting an optical signal into an electrical signal") is formed on a

semiconductor substrate (“chip 1”) and (2) a peripheral circuit chip (“chip 4” having “computing part 5”) is mounted onto the same substrate. (Ex. 1018, Claim 1, ¶¶ 0007-0010, Fig. 1(b)). Thus, Nagano teaches a semiconductor substrate with an image sensor and a peripheral circuit chip disposed on it, as disclosed in claim 7. (Ex. 1018, Claim 1, ¶¶ 0007-0010, Fig. 1(b)).

D. Wakabayashi is prior art

139. I understand that Wakabayashi is prior art to the ’714 patent, because it was published on February 14, 1995.

E. Summary of Wakabayashi

140. Wakabayashi is summarized in ¶¶ 71-74 above.

F. Element-by-element analysis of claim 7 over Yoshino in view of Nagano, in further view of Wakabayashi

1. Claim 7

“[7a]. A solid-state image sensing apparatus comprising:”

141. As discussed for claim element [1a] in ¶ 100 above, Yoshino discloses a solid-state image sensing apparatus.

“[7b]. a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,”

142. As discussed for claim element [1b] in ¶¶ 101-103 above, Yoshino discloses a package having a through hole, openings on both end faces thereof, and different opening areas of said openings.

“[7c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,”

143. As discussed for claim element [1c] in ¶¶ 104-105 above, Yoshino discloses a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package.

“[7d]. a semiconductor substrate having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof, said semiconductor substrate being inserted into a plastic package via the larger of two openings formed in said package, and”

144. As discussed for claim element [1d] in ¶¶ 106-111 above, Yoshino discloses a solid-state image sensing device mounted by being inserted into the package via the larger of two openings formed in said package. As discussed in ¶ 91 above, “package” and “plastic package” in claim 7 indicate the same thing: a single plastic package.

145. Yoshino does not expressly teach that its package is made of plastic. It was well-known in the relevant timeframe to make semiconductor packages out of plastic. Thus, plastic was a known equivalent for other package materials (such as ceramic, as taught in one embodiment of Yoshino). (Ex. 1006, Claim 2). In a very similar context (a similar package for a solid-state image sensing device), Wakabayashi teaches using plastic as a package material, as indicated in the passage below.

“(Object) Provide a solid-state image pickup device comprised of a small plastic package without degrading the CCD microlens effects.”
(Ex. 1004, Abstract).

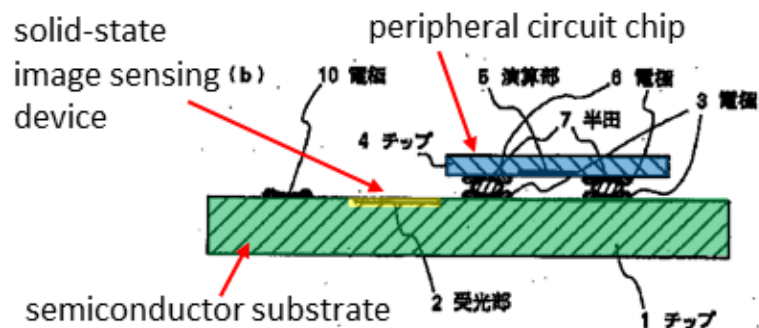
Wakabayashi’s plastic could have been used for Yoshino’s package with only ordinary skill. There would have been no unpredictable results. Thus, a plastic package would have been obvious.

146. A semiconductor image sensor—like the one disclosed in Yoshino—is actually a semiconductor substrate that has an image sensor formed on it. Thus, Yoshino discloses a semiconductor substrate. But Yoshino does not expressly disclose a peripheral circuit chip disposed on an upper surface thereof.

147. Nagano discloses a semiconductor substrate having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof. This is shown in the following passage from Nagano, which describes the apparatus depicted in Nagano’s Fig. 1(b):

“[A] photodiode with a computing function characterized in that a light-receiving part for converting an optical signal into an electrical signal and a computing part for operating upon the electrical signal are formed on different semiconductor chips; on the semiconductor chip on which the computing part is formed there are provided electrodes in the same disposition as a number of electrodes of the semiconductor chip on which the light-receiving part is formed; and these chips have their electrodes connected....” (Ex. 1018, Claim 1).

148. Below is a version of Nagano's Fig. 1(b) that Petitioner has accurately annotated to show that Nagano discloses having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof, per the above passage. As shown in the figure, and described with further specificity in the passage below, Nagano discloses a semiconductor substrate ("chip 1", highlighted green) having a solid-state image sensing device ("light-receiving part 2", highlighted yellow) and a peripheral circuit chip ("chip 4 having a computing part 5", highlighted blue) disposed on an upper surface thereof:



“A photodiode with a computing function according to this embodiment example has electrodes 3 of a chip 1 having a light-receiving part 2 and electrodes 6 of a chip 4 having a computing part 5 fixed together with solder 7 with the electrodes facing each other. An optical signal picked up by the light-receiving part 2 of the chip 1 is converted into an electrical signal, passes through the solder 7, is operated upon in the computing part 5 of the chip 4, and passes through the solder 7 again and returns to the chip 1. And, a photodiode with a computing function according to this embodiment example is connected to another circuit by electrodes 10.” (Ex. 1018,

¶ 0008).

149. For the same reasons and with the same result discussed in ¶¶ 121-126 above for Ground 4, element [6d] with regard to Izumi, one of ordinary skill would have been motivated to use the semiconductor substrate disclosed in Nagano with Yoshino's package. Having the peripheral circuit chip and image sensor on a common substrate provides a reduction in noise and a shorter signal path. This lowers power consumption and increases speed, features that are commercially valuable. Putting a peripheral circuit chip and image sensor on a common substrate also protects the peripheral circuit chip and takes up less space overall than if the chip were mounted outside the package. An apparatus in which an image sensor is formed on the substrate as in Nagano provides even more space-saving advantage than one in which the image sensor is mounted on the substrate. The arrangement—including forming the image sensor, mounting the peripheral chip, and making the substrate larger to accommodate the peripheral chip—would have been a variation to Yoshino's base system that could have been accomplished using only ordinary skill, and there would have been no unpredictable results.

“[7e]. an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around the smaller opening of said package,”

150. As discussed in ¶¶ 127-132 above for claim element [6e], Yoshino discloses an electrode pad of a solid-state image sensing device being connected to the inner lead exposed from around the smaller opening of said package. As discussed in ¶¶ 144-149 above for claim element [7d], it would have been obvious to use Nagano's semiconductor substrate in place of Yoshino's image sensor.

151. As stated in the following passage, Nagano's semiconductor substrate features "electrodes 10", which are contact (*i.e.*, electrode) pads that serve the same function as the pads in Yoshino, and so it would have been obvious to connect them to the inner leads of Yoshino.

"a photodiode with a computing function according to this embodiment example is connected to another circuit by electrodes 10". (Ex. 1018, ¶ 0008).

"[7f]. said semiconductor substrate being secured to said package via an adhesive."

152. As discussed for claim element [1d] in ¶ 113 above, Yoshino discloses the solid-state image sensing device being secured to said package via an adhesive. As discussed above for claim element [7d] (¶¶ 144-149 above), it would have been obvious to one of ordinary skill to use Nagano's semiconductor substrate in place of Yoshino's image sensor.

153. Thus, for the foregoing reasons, I conclude that claim 7 was obvious over Yoshino in view of Nagano, in further view of Wakabayashi.

XV. Claim 8 is obvious over Yoshino in view of Izumi or Nagano, in further view of Hirosawa and Nita.

A. Summary of opinion

154. It is my opinion that Claim 8—which is multiply dependent from claims 6 and 7—is obvious over Yoshino in view of Izumi (if dependent from claim 6) or Nagano (if dependent from claim 7), in further view of Japanese Pat. App. Pub. No. S60-74880 (“Hirosawa”) (Ex. 1021, certified translation as Ex. 1020) and Japanese Pat. App. Pub. No. H07-78951 (“Nita”) (Ex. 1023, certified translation as Ex. 1011). The obviousness analysis is the same no matter whether claim 6 or claim 7 is the base claim.

B. Hirosawa is prior art

155. I understand that Hirosawa is prior art to the ’714 patent, because it was published on April 27, 1985.

C. Summary of Hirosawa

156. Hirosawa discloses a package for a semiconductor substrate (“semiconductor chip 2”) on which a solid-state image sensor (“a light detection semiconductor element ... such as a CCD”) and a peripheral circuit chip (“a signal processing circuit element”) are formed. (Ex. 1020, p. 480; Fig. 1). Hirosawa teaches use of a shading film (“light-shielding film ... 8”) to protect the peripheral circuit elements from light. (Ex. 1020, p. 480, film “8” erroneously shown as “3” in Fig. 1).

D. Nita is prior art

157. I understand that Nita is prior art to the '714 patent, because it was published on March 20, 1995.

E. Summary of Nita

158. Nita also discloses a package for a semiconductor substrate (“chip 1”) on which a solid-state image sensor (“light receiving section” of a “CCD”) and peripheral circuit elements (“storage section”) are disposed. (Ex. 1011, p. 5; Figs. 3 and 4). Nita teaches use of a shading film (“light shielding section”) to protect the peripheral circuit elements from light. (Ex. 1011, p. 5; Figs. 3 and 4).

F. Element-by-element analysis of claim 8 over Yoshino in view of Izumi or Nagano, in further view of Hirose and Nita

1. Claim 8

“8. The solid state image sensing apparatus of claim 6 or claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device.”

159. The combinations of Yoshino and Izumi (if dependent from claim 6) or Yoshino and Nagano (if dependent from claim 7) do not expressly disclose a shading film. Applying a shading film was a well-known technique that would have been an obvious step in a package for an image sensor that features peripheral circuit elements. Hirose and Nita both teach using a shading film to protect peripheral circuit elements of an image sensing apparatus from light (since light

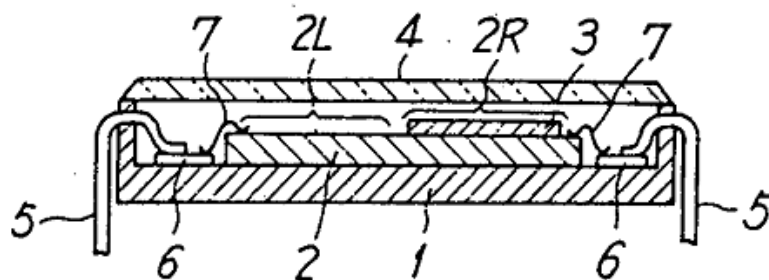
can interfere with the function of those peripheral circuit elements), and leaving the image sensor unshaded. One of ordinary skill in the relevant timeframe could have envisioned a variety of different applications of this technique. This is illustrated by the minor differences between the disclosures of Hirose and Nita. Namely, Hirose places the shading film directly *on* the substrate (on which the image sensor and peripheral circuit elements are disposed), while Nita places the shading film *above* the substrate, on the package's transparent lid.

160. In the following passage, Hirose discloses a semiconductor substrate ("semiconductor chip 2") on which an image sensor ("a light detection semiconductor element") and a peripheral circuit chip ("a signal processing circuit element") are formed, which is mounted in a package having a shading film ("light-shielding film"):

"[A] single semiconductor chip 2 is provided on a ceramic substrate 1 that constitutes a package, a light detection semiconductor element such as a charge transfer element such as a CCD or a BBD, MOS transistor, a photodiode, a phototransistor, a static induction transistor, or the like being formed in a left-side section 2L, and a signal processing circuit element ... being formed in a right-side section 2R. The light-shielding film or a light-shielding plate 8 is provided to the section 2R where the signal processing circuit element is formed, preventing ... light irradiated through a transparent glass cap 4 from affecting the signal processing circuit." (Ex. 1020, p. 480, *see also* Fig. 1).

161. As shown in Hirosawa's Fig. 1 (below), Hirosawa discloses the shading film *on* the substrate, and shows the shading film covering the entire upper surface of the substrate except an upper surface of the solid-state image sensing device (section 2L). (Ex. 1020, p. 480, Fig. 1). Figure 1 erroneously indicates the shading film using the numeral "3" rather than "8", as indicated in the passage above.

FIG. 1



162. Nita discloses a similar solid-state image sensing apparatus in which the shading film is *above* the substrate, on the package's lid. As described in the following passages (and shown in Nita's Figs. 3 and 4, below), Nita refers to the substrate as "chip 1" (a semiconductor substrate which includes a solid-state image sensor). Nita refers to its lid as "transparent glass lid 4" of "package 2", its shading film as a "light shielding section", its image sensor as a "light receiving section", and its peripheral circuit elements as a "storage section".

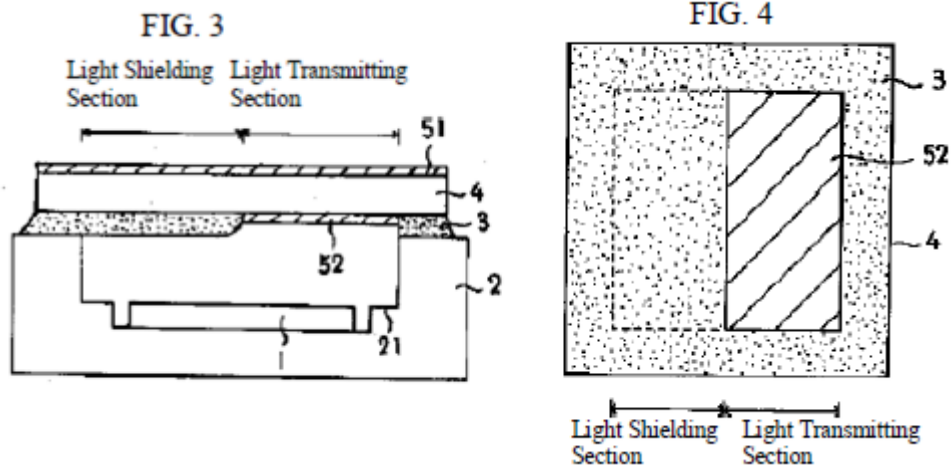
"Next, the second example will be explained with reference to FIGS.

3 and 4. FIG. 3 is a sectional view of the solid-state image pickup device, and FIG. 4 is a plan view of the back face of the lid used in the solid-state image pickup device. The bonding wires for connecting the electrode pins for external circuit connection and the wiring of the package's stepped section to the chip are the same as in the case of FIG. 1, and thus the description will be omitted. This solid-state image pickup device0 [sic.] has a charge transfer device, such as a CCD, as the solid-state image sensor sealed in the package 2. The package 2 is made of ceramic, and its opening is hermetically sealed with a glass lid 4. This section is referred to as a light transmitting window 4 as it allows the light from the outside to transmit therethrough. A solid-state image sensor 1 is placed on the bottom face of the interior of the package 2. The chip 1 is secured to the bottom face of the package using an adhesive. The package 2 has a stepped section 21 along the inner side walls, and the connection wiring is formed to be partially exposed at the flat part of the stepped section 21. The connection wiring is embedded in the package 2, and internally connected to the electrode pins projecting from the bottom face. The solid-state image pickup device is mounted on a circuit board or the like, the electrode pins are connected to the circuit board to electrically connect the external circuit formed on the circuit board to the solid-state image pickup device, and the connection electrodes (not shown) formed on the chip 1 and the aforementioned connection wiring of the package 2 are electrically connected.

This is achieved by connecting the connection wiring exposed at the flat part of the stepped section 21 and the connection electrodes of the

chip 1 using bonding wires. In order to prevent light reflection, an antireflective film 51 is formed on the front face of the transparent lid 4. Besides the front face facing the outside air, an antireflective film 52 is formed on the back face of the lid 4 facing the interior of the package 2 to prevent imaging problems attributable to unnecessary reflection. The antireflective film 51 is deposited across the entire glass surface by vacuum deposition or the like. On the other hand, the antireflective film 52 is not applied across the entire back face of the lid, i.e., the antireflective film is not deposited in the region where the adhesive layer 3 will be applied to secure the lid to the package 2. The adhesive is directly applied to the back face of the lid 4 so as not to overlap with the antireflective film 52. In this example, the region for the adhesive layer 3 is expanded, and the expanded region is used as a light shielding section. The solid-state image sensor is an integrated circuit which satisfies the three basic functions: photoelectric conversion, accumulation, and scanning. For signal extraction, for example, a charge transfer method having a functional device, such as a CCD, is used. Broadly categorized, there are two modes for the CCDs used as two-dimensional imaging sensors that have been put to practical use: frame transfer (FT) and interline transfer (ILT). The frame transfer mode requires a light receiving section and a storage section that are equal in area on one chip, but the structure of the clock circuit is relatively simple as compared to interline transfer. Light enters the light receiving section, and the signal charges are accumulated. The charges are then transferred to the light shielded storage section at high speed and read out sequentially per line at a relatively low speed. While the charges are being read out, charge

accumulation is performed for the subsequent light entry. As such, the frame transfer mode requires that the storage section be light shielded. In cases where the frame transfer mode is applied to the invention, the adhesive layer of this example is appropriately concurrently used as the light shielding section.” (Ex. 1011, ¶¶ 0015-0016).

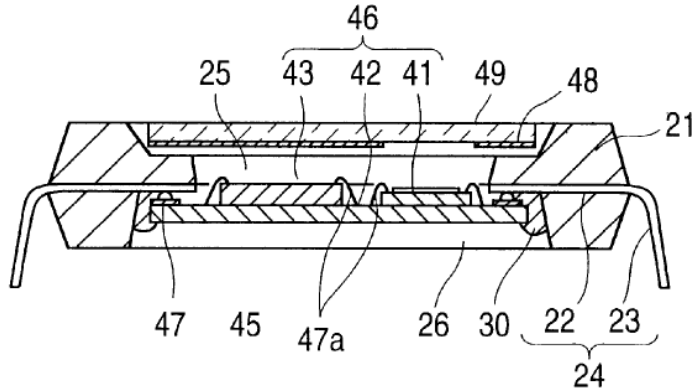


163. This arrangement (with the shading film *above* the substrate, on the package’s transparent lid) is the arrangement shown in the ’714 patent’s Fig. 7 (below). Fig. 7, as described in the passage below, depicts the only shading film embodiment and shows shading film 48 above the substrate on the package’s lid (glass substrate 49).

“Since the surface on which the circuit elements 43 are formed is situated upward, a shading film 48 is required; however, when defects are found in the CCD chip 41 or the peripheral circuit elements 43, the defective parts can be easily replaced and the other parts also can be used again. In FIG. 7, a glass substrate 49 is made from the shading film by being deposited with metal or by sputtering.” (Ex. 1001,

7:26-32).

FIG. 7



164. It would have been obvious to use the shading film of Hirosawa or Nita in the solid-state image sensing apparatus of the combinations of Yoshino/Izumi or Yoshino/Nagano, to cover the entire upper surface of the substrate except an upper surface of the solid-state image sensing device. Doing so would have the predictable advantage of protecting the peripheral chip from light, or of minimizing light reaching the peripheral chip that might obtain with partial coverage. Using such a shading film in the package of Yoshino/Izumi or Yoshino/Nagano is also a known improvement for this type of base system that could have been accomplished using only ordinary skill, and there would have been no unpredictable results.

165. With respect to base claim 6 (the Yoshino/Izumi combination), Izumi also already potentially blocks light to the peripheral chips by covering the

peripheral chip section with resin sealing material 7, as described in the following passage:

“Each of peripheral circuit chip 3 and peripheral circuit chips 4A to 4D which are furnished inside the aforementioned second cavity part 1B are hermetically sealed by resin sealing material 7. Resin sealing material 7 uses for instance polyimide resin or silicon rubber, and is applied through a potting process.” (Ex. 1016, p. 335).

This demonstrates that the function of blocking light to the peripheral chip was common and obvious. A person of ordinary skill in the relevant timeframe would have known that—when combined with Yoshino—a shading film (*i.e.*, a light-shielding layer) was an additional or equivalent method for preventing light from reaching the peripheral circuit elements. The substitution or additional use of light-shading layer would have been obvious.

166. Thus, for the foregoing reasons, I conclude that claim 8 was obvious over Yoshino in view of Izumi or Nagano, in further view of Hirose and Nita.

XVI. Claim 9 is obvious over Yoshino in view of Izumi or Nagano.

A. Summary of opinion

167. It is my opinion that claim 9—which is multiply dependent from claims 6 and 7—is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Izumi (if from claim 6) (Ex. 1016 and Ex. 1017) or Nagano (if from claim 7) (Ex.

1018 and Ex. 1019). The obviousness analysis is the same no matter whether claim 6 or claim 7 is the base claim.

B. Element-by-element analysis of claim 9 over Yoshino in view of Izumi or Nagano

1. Claim 9

“9. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via a bump.”

168. As discussed in ¶¶ 127-133 above for claim element [6e] (with reference to Izumi) and in ¶¶ 150-151 for claim element [7e] (with reference to Nagano), an electrode pad formed on the substrate connected to the inner lead is obvious from Yoshino in combination with Izumi or Nagano.

169. Yoshino discloses that the electrode pads of its image sensor are connected to the inner lead (the inner part “of electrode leads (21)”) via a bump (“conductive bonding material (27)”) in the following passage:

“The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21) aligned therewith are connected via a conductive bonding material (27), for example, indium. The electrode leads (21) are coated with the conductive bonding material (27) by means of plating, brazing, or the like.” (Ex. 1003, p. 2).

170. Indium is a metal used in press fit bump-bonding. For example, in the relevant timeframe, bumps made from Indium (or a composite including Indium) were commonly used to bond an infrared image sensor to a readout circuit. This was referred to as “Indium bump bonding”. Thus, one of ordinary skill would have understood Yoshino’s “conductive bonding material (27), for example, indium” to be a bump.

171. Yoshino discloses that the bump is formed on the inner lead. A bump is often formed on a chip’s pads, but it may also be formed on the inner lead with essentially the same effect. This was known to persons of ordinary skill and in fact the ’714 patent discloses that the bump may be formed on the inner lead in its specification:

“Further, in the above Embodiments 1 and 2, the case is described that the bump 29 is disposed on the electrode pad 28 of CCD chip 27; however, the bump 29 can be disposed at the tip of inner lead 22 and connected with the electrode pad 47 of CCD module 46.” (Ex. 1001, 8:54-58).

172. Therefore, Yoshino discloses that its image sensor’s electrode pads are electrically connected via a bump, *i.e.*, an amount of conductive metal material.

173. As discussed in ¶¶ 121-126 above for claim element [6d] (with reference to Izumi) and in ¶¶ 144-149 for claim element [7d] (with reference to Nagano), it would have been obvious to use a substrate with an image sensor and

peripheral chip in Yoshino's package. For the same reasons discussed there, it would have been obvious to use the connector disclosed in Yoshino—bumps—to connect the substrate. In particular, using Yoshino's bump bonding would have the predictable advantage of providing a smaller package. Bump bonding was a known technique for bonding of image sensors (and for bonding of substrates with chips mounted/formed on them, as described here). It would have been well within ordinary skill in the relevant timeframe to use bumps to make the connection in such a situation, and the results would have been predictable.

174. Thus, for the foregoing reasons, I conclude that claim 9 was obvious over Yoshino in view of Izumi or Nagano.

XVII. Claim 10 is obvious over Yoshino in view of Izumi or Nagano, in further view of Wakabayashi

A. Summary of opinion

175. It is my opinion that claim 10—which is multiply dependent from claims 6 and 7—is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Izumi (if from claim 6) (Ex. 1016 and Ex. 1017) or Nagano (if from claim 7) (Ex. 1018 and Ex. 1019), in further view of Wakabayashi (Ex. 1004 and Ex. 1007). The obviousness analysis is the same no matter whether claim 6 or claim 7 is the base claim.

B. Element-by-element analysis of claim 10 over Yoshino in view of Izumi or Nagano, in further view of Wakabayashi

1. Claim 10

“10. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity.”

176. As discussed in ¶¶ 127-133 above for claim element [6e] (with reference to Izumi) and in ¶¶ 150-151 for claim element [7e] (with reference to Nagano), an electrode pad formed on the substrate connected to the inner lead is obvious from Yoshino in combination with Izumi or Nagano.

177. In the following passages, Wakabayashi discloses connecting the electrode pads (of the image sensor) to the inner lead via an anisotropic conductor:

“[T]he joining of the chip to the inner leads via the bumps is performed via the conductive adhesive layer formed on the surfaces of the bumps disposed on the bonding pads of the CCD chip.” (Ex. 1004, ¶ 0006).

“For the conductive layer, ... a resin-based anisotropic conductive adhesive can be suitably used.” (Ex. 1004, ¶ 0014).

178. An anisotropic conductor is conductive in only one direction. For example, if it is conductive in the Z-axis, it would not be conductive in the X- and Y-axis. One of ordinary skill would have understood Wakabayashi’s anisotropic conductor to be one that has only vertical conductivity. This is obvious because Wakabayashi’s Fig. 2 (reproduced for ¶ 73 above) shows that the connection

between the image sensor's electrode pads and the inner lead is made in the vertical plane.

179. Use of an anisotropic conductor allows the connection points on a chip to be close together, allowing for more connections points and/or a reduced footprint. This closeness of connection points is referred to as connector "pitch". One of ordinary skill would have been motivated to use Wakabayashi's anisotropic conductor in Yoshino's package and Nagano's substrate because an anisotropic conductor allows for a fine connector pitch. Also, Wakabayashi's anisotropic conductor was a known substitute for other methods of electrically connecting a chip such as an image sensor—for example, the bump bonding taught in Yoshino—and there would have been no unexpected results from its use.

180. Thus, for the foregoing reasons, I conclude that claim 10 was obvious over Yoshino in view of Izumi or Nagano in further view of Wakabayashi.

XVIII. Claim 11 is obvious over Yoshino in view of Izumi or Nagano, in further view of Onishi.

A. Summary of opinion

181. It is my opinion that claim 11—which is multiply dependent from claims 6 and 7—is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Izumi (if from claim 6) (Ex. 1016 and Ex. 1017) or Nagano (if from claim 7) (Ex 1018 and Ex. 1019), in further view of Japanese Pat. App. Pub. No. H05-006989

(“Onishi”) (Ex. 1015, certified translation as Ex. 1014). The obviousness analysis is the same no matter whether claim 6 or claim 7 is the base claim.

B. Onishi is prior art

182. I understand that Onishi is prior art to the ’714 patent, because it was published on January 14, 1993.

C. Summary of Onishi

183. Onishi discloses a package in which an image sensor is bump-bonded in a through hole to the inner lead and secured with an adhesive. (Ex. 1014, ¶¶ 0016-0020, Figs. 3 and 4). Onishi teaches the tip of the inner lead projecting into the center of the through hole, as disclosed in claim 5 (and also as in claim 11, as discussed in ¶¶ 181-188 below). (Ex. 1014, ¶¶ 0016, 0020, inner tip of “leads (8)” in Figs. 3 and 4).

D. Element-by-element analysis of claim 11 over Yoshino in view of Izumi or Nagano, in further view of Onishi.

1. Claim 11

“11. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead at an outer portion of said lead, said outer portion of said lead extending into the openings of the package.”

184. As discussed in ¶¶ 127-133 above for claim element [6e] (with reference to Izumi) and in ¶¶ 150-151 for claim element [7e] (with reference to

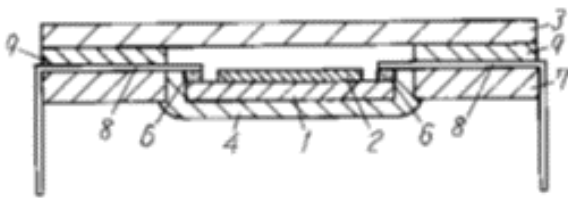
Nagano), an electrode pad formed on the substrate connected to the inner lead is obvious from Yoshino in combination with Izumi or Nagano.

185. Onishi discloses an outer portion of said lead extending into the openings of the package, in a very similar context. Onishi discloses a package for an image sensor. The image sensor is bonded via bumps in a through hole to the inner part of “leads (8)”, which is the inner lead of the lead frame. The image sensor is then secured with an adhesive (“sealing resin (4)”). This is indicated in the following passages from Onishi and in Onishi’s Figs. 3 and 4 (reproduced below):

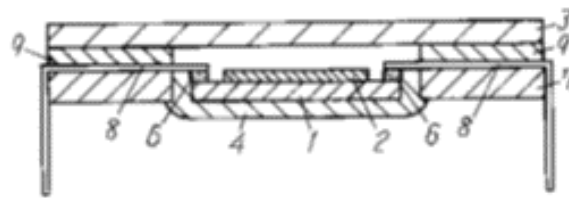
“[0016] Figure 3 is a cross-section of the imaging equipment in a working example of the second invention. In the figure, (7) is the base, (8) are the leads, and (9) is the adhesive. The base (7), which is made of a one-layer ceramic, has in its middle portion a rectangular window of a size that can contain the imaging element (1), and multiple leads (8) are formed on one surface. The leads (8) are formed from conductors of an iron alloy, for example, and the inner edge of each one protrudes into the window of the base (7). In order to increase the bondability of the protruding portion with the bump electrodes (6), for example, if the bump electrodes (6) are metal then it is preferable to perform tin plating of the surfaces of the leads (8). The other edges of the leads (8) extend outside the base (7) and bend downward along the side surfaces of the base (7) to become external leads. The imaging element (1) is electrically connected to the inner edges of the leads (8) by the bump electrodes (6), and its light-

receiving surface is fixed within the window of the base (7) so as to face the transparent plate (3). ...

[0020] Figure 4 is a cross-section of imaging equipment of a working example of the third invention. In the figure, (10) is the flare-prevention layer. The base (7), which is made of a one-layer ceramic, has a window in the center of it, and multiple leads (8) are formed on one surface. The inner edge of each lead (8) protrudes into the window of the base (7). The imaging element (1) is electrically connected to the inner edges of the leads (8) by the bump electrodes (6), and its light-receiving surface is fixed within the window of the base (7) so as to face the transparent plate (3). ...” (Ex. 1014, ¶¶ 0016-0020).



Onishi Fig. 3



Onishi Fig. 4

186. Onishi discloses that a tip of the inner lead (“the inner edges of the leads (8)”) to which the electrode pad (“bump electrodes (6)”) is connected extends into the center of the through hole. This is shown in the following passage, and is seen in Onishi’s Figs. 3 and 4 (reproduced above).

“The imaging element (1) is electrically connected to the inner edges of the leads (8) by the bump electrodes (6) [In one embodiment], the imaging element (1) is connected to the inner edges of the leads (8) that protrude into a hollow space within the window of the base

(7), so the stress during the hardening of the sealing resin (4) can be absorbed by the flexibility of the leads (8)”. (Ex. 1014, ¶¶ 0016-0017, see also Figs. 3 and 4).

187. It would have been obvious to one of ordinary skill to use Onishi’s inwardly extended inner lead with Yoshino’s package, or the package for an image sensor/peripheral chip substrate as rendered obvious by the combination of Yoshino/Izumi or Yoshino/Nagano. This would have allowed the inner lead to be detached from the ledge so that the lead could flex, which would relieve stress during the hardening of the adhesive. Also, it would have allowed for accuracy in positioning of the image sensor and of bonding of the inner lead to the sensor’s pads. Furthermore, it was a known variation on Yoshino’s base system, and its use would have had no unpredictable results.

188. Thus, for the foregoing reasons, I conclude that claim 11 was obvious over Yoshino in view of Izumi or Nagano in further view of Onishi.

XIX. Claim 12 is obvious over Yoshino in view of Tobase.

A. Summary of opinion

189. It is my opinion that claim 12 is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Japanese Unexamined Patent Application Publication No. H05-275611 (“Tobase”) (Ex. 1013, certified translation as Ex. 1022).

B. Tobase is prior art

190. I understand that Tobase is prior art to the '714 patent, because it was published on October 22, 1993.

C. Summary of Tobase

191. Tobase discloses a package in which a number of semiconductor chips (not expressly including an image sensor) are mounted via bumps to multiple step surfaces on the interior of the package, similar to the package disclosed in claims 12 and 16. (Ex. 1022, Abstract, Fig. 1).

D. Element-by-element analysis of claim 12 over Yoshino in view of Tobase

1. Claim 12

“[12a]. A solid-state image sensing apparatus comprising:”

192. As discussed for claim element [1a] in ¶ 100 above, Yoshino discloses a solid-state image sensing apparatus.

“[12b]. a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,”

193. As discussed for claim element [1b] in ¶¶ 101-103 above, Yoshino discloses a package having a through hole, openings on both end faces thereof, and different opening areas of said openings.

“[12c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and”

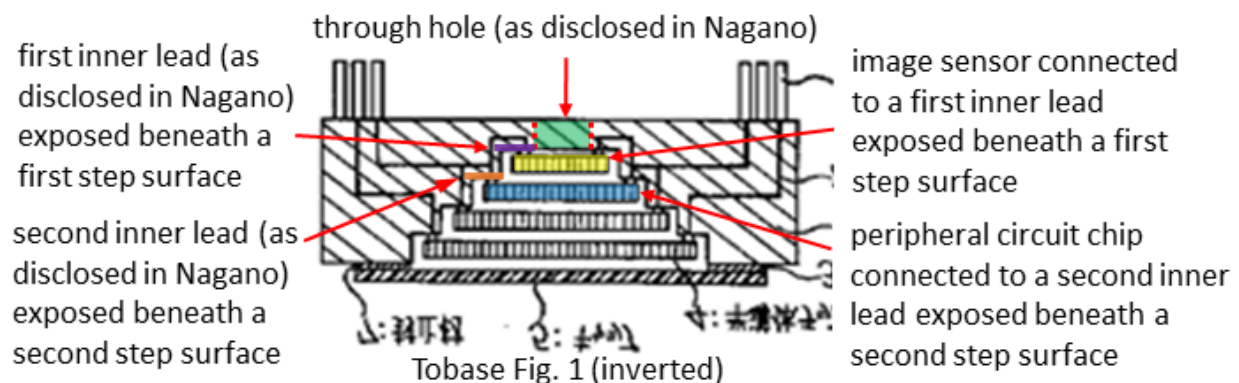
194. As discussed for claim element [1c] in ¶¶ 104-105 above, Yoshino discloses a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package.

“[12d]. a solid-state image sensing device and a peripheral circuit chip both mounted in said package, said solid-state image sensing device being connected to a first inner lead exposed beneath a first step surface formed in said package, said solid-state image sensing device being secured to said package via an adhesive, and said peripheral circuit chip being connected to a second inner lead exposed beneath a second step surface formed in said package, said peripheral circuit chip being secured to said package via an adhesive.”

195. As discussed in ¶¶ 100-114 above for claim elements [1a]-[1d], Yoshino discloses a solid-state image sensing device mounted in a package. As discussed in ¶¶ 127-128 above for claim element [6e], Yoshino discloses that the solid-state image sensing device is connected to the inner lead. Tobase discloses or renders obvious the remaining limitations of claim element 12d.

196. Tobase teaches a package housing multiple semiconductor chips. The chips are mounted on multiple step surfaces. This is shown in Tobase’s Fig. 1, reproduced below with highlighting and annotations by Petitioner in order to illustrate the combination with Yoshino. It is appropriate to invert Fig. 1 in order to compare it to the disclosure of the ’714 patent because the relevant orientation is

of the chip with regard to the package. The '714 patents figures show the image sensor bonded *face up* in the package, such that the image sensor's pads are joined (*e.g.*, via bumps) to the bottom side of the inner leads. Tobase's figures, on the other hand, show chips bonded *face down* in the package, such that the chips' pads are bonded via bumps to the upper side of the leads. Since claim element [12d] discusses orientation with regard to the direction the image sensor is bonded to the inner lead ("connected to a ... inner lead exposed beneath a ... step surface"), Tobase's Fig. 1 must be inverted to properly compare it to the disclosure of the '714 patent.

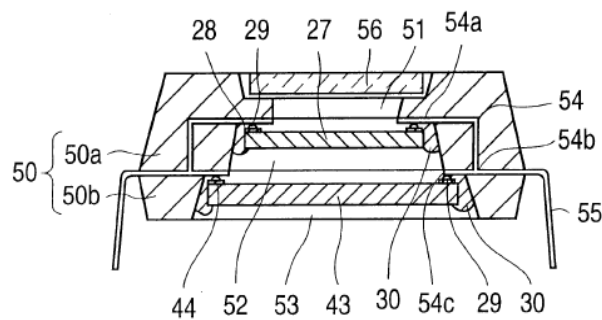


197. Tobase describes Fig. 1 in the following passage:

“As shown in Fig. 1, semiconductor chips 4 are severally received multi-step-wise in the vertical direction, apart from and parallel with each other, in multiple steps of recess provided in an electrically insulating substrate 1 having an electrical interconnector pattern 2. Bumps 3 are formed on the steps where the semiconductor chips 4 are disposed. The semiconductor chips 4 are disposed on these bumps 3, and the semiconductor chips are connected as necessary to each other

or to external leads 6 by the electrical interconnector pattern 2.” (Ex. 1022, ¶ 0009).

198. The structure of the package disclosed in Tobase is very similar to the embodiment shown in the '714 patent's Fig. 8, reproduced below. Fig. 8 depicts chips connected to progressively inwardly-recessed step structures, with the larger chip deeper in the package.



199. It would have been obvious for one of ordinary skill to use the step structure disclosed in Tobase within the package of Yoshino. This would have produced additional space savings, which is important in small optical and image capture devices. Tobase explains that

“mounting density can be increased and the interconnector path lengths of the electrical interconnectors can be shortened and the signal propagation time thereby shortened, and high-speed operation of the multi-chip module thereby made possible.” (Ex. 1022, ¶0018).

200. Using the step structure disclosed in Tobase within the package of Yoshino would also aid in protecting the peripheral circuit chip from light

exposure. This would reduce or eliminate the need for a shading film, and therefore lead to fabrication cost and time savings.

201. The step structure of Tobase is a simple, mechanical variation on Yoshino's package. It would have been well within ordinary skill in the relevant timeframe to use the step structure disclosed in Tobase within the package of Yoshino. Doing so would have produced no unexpected results.

202. One of ordinary skill would have known to package a peripheral circuit chip, such as an image signal processor, with an image sensor in a multi-chip package. Thus, when combined with Yoshino's package for a solid-state image sensing device, it would be obvious for one of Tobase's other chips to be a peripheral circuit chip. It also would have been obvious to have first and second inner leads in a package for multiple chips, because each chip must be connected. This is suggested by Tobase's multiple connection points.

203. As shown in the annotated Fig. 1 reproduced at ¶ 196 above, if Yoshino were modified by using a stepped structure like Tobase's Fig. 1, the first and second inner leads would be exposed beneath a first and a second step surface formed in said package.

204. As discussed for claim element [1d] in ¶ 113 above, Yoshino discloses the solid-state image sensing device being secured to said package via an adhesive. Using different securing methods for the image sensor and the peripheral circuit

chip would have been unnecessarily complex and costly. Thus, it would have been obvious to use Yoshino's adhesive for the peripheral chip as well.

205. Thus, for the foregoing reasons, I conclude that claim 12 was obvious over Yoshino in view of Tobase.

XX. Claim 13 is obvious over Yoshino in view of Hikosaka.

A. Summary of opinion

206. It is my opinion that claim 13 is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Japanese Pat. App. Pub. No. S59-225560 (“Hikosaka”) (Ex. 1008, certified translation as Ex. 1005). Yoshino discloses elements of claim 13 that are also found in claim 1, as discussed in ¶¶ 96-114 above. Claim 13 adds the limitation “simultaneously adjusting the optical positioning of said solid-state image sensing device”, which is taught by Hikosaka. As described below, it would have been obvious to use Hikosaka’s simultaneous optical positioning to improve the positioning of the image sensor within Yoshino’s package.

B. Hikosaka is prior art

207. I understand that Hikosaka is prior art to the ’714 patent, because it was published on Dec. 8, 1984.

C. Summary of Hikosaka

208. Hikosaka discloses a process for producing a solid-state image sensing apparatus in which an image sensor is mounted in a through hole via face

bonding of the image sensor via bumps, much like that of the '714 patent. (Ex. 1005, p. 2). As part of this process, Hikosaka teaches adjusting the optical positioning of the image sensor at the same time the image sensor is being connected, via a process that uses a video display showing an image of a positioning reference mark captured by the image sensor that is aligned with another reference mark on the screen of the video display. (Ex. 1005, p. 3-4).

D. Element-by-element analysis of claim 13 over Yoshino in view of Hikosaka

1. Claim 13

“[13a]. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package, said manufacturing method comprising the steps of:”

209. As discussed in ¶¶ 91-101 above for claim elements [1a]-[1d], Yoshino discloses a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package.

210. Yoshino also discloses a manufacturing method—steps by which the apparatus is “constructed”—for example, in the following passage:

“In this solid-state image pickup device, the packaging substrate (20), for example, a black ceramic substrate, is constructed by stacking ceramic molded frames (201) and (202)” (Ex. 1003, p. 2).

“[13b]. inserting said solid-state image sensing device into said through hole,”

211. As discussed for claim element [1d] in ¶¶ 106-111 above, Yoshino discloses inserting said solid-state image sensing device into said through hole.

“[13c]. connecting an electrode pad of the solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device, and”

212. As discussed for claim element [6e] in ¶¶ 127-128 above, Yoshino discloses connecting an electrode pad of the solid-state image sensing device to the inner lead. As discussed in ¶¶ 169-172 above for claim 9, Yoshino discloses connecting an electrode pad to the inner lead via a bump. Claim element [13c] only requires connecting via a bump *or* an anisotropic conductor having only vertical conductivity.

213. Although Yoshino does not expressly disclose the remaining limitation of claim element [13c]—simultaneously adjusting the optical positioning of said solid-state image sensing device—Hikosaka discloses this limitation in a essentially the same context as that of Yoshino. Both Yoshino and Hikosaka

disclose a solid-state image sensing apparatus for use in a lens system. Hikosaka teaches that its apparatus is used in a “lens system”:

“Since the solid-state image pickup device is used in combination with a lens system, the semiconductor chip 1 must be highly accurately aligned with the housing 2.” (Ex. 1005, p. 2).

Yoshino teaches that its apparatus is used in a “camera” (a type of lens system):

“For this [prior art] solid-state image pickup device, however, space constraints are unavoidable because extraction from the solid image sensor (3) to the electrodes is achieved via metal wires (7) by a bonding step performed for regular semiconductor devices. Therefore, the needs for more compact devices in the electronic camera field, or the like, cannot be fully addressed. ... The present invention was created in order to solve the shortcomings described above” (Ex. 1003, pp. 1-2).

214. Hikosaka discloses optical positioning, both in the sense of adjusting the position of the image sensor to obtain the correct position for use in an optical system, and in the sense of making the adjustment using optical information/measurements (*i.e.*, making the adjustment “optically”).

215. In the following passage, Hikosaka discloses adjusting the position of the image sensor to obtain the correct position for use in an optical system:

“Since the solid-state image pickup device is used in combination with a lens system, the semiconductor chip 1 must be highly accurately aligned with the housing 2.” (Ex. 1005, p. 2).

216. Hikosaka also discloses that positioning of the image sensor is done using optical information, and that this process takes place simultaneously with connecting an electrode pad of the image sensor to the lead. This process is described in full in the following passage from Hikosaka:

“The production steps of the solid-state image pickup device constructed as above will be explained next. First, a housing 7 is positioned and secured on the pair of mounting racks 18 by placing the housing 7 on the pair of mounting racks 18, pressing it against the stops 19 using the pressing means 20, and squeezing it between the pair of mounting racks 18.

Next, a semiconductor chip 12 held by a vacuum suction holding means (not shown) is placed on the solder bumps 11 in the recess 7a of the housing 7 placed at the prescribed position described above so that its electrodes 12a come into contact with the solder bumps 11.

Then, the semiconductor chip 12 is operated by the drive circuit 16 via the leads (not shown) disposed on the housing 7 to display the image captured by the semiconductor chip 12 on the CRT screen of the display device 15. One example of a CRT screen of the display device 15 is shown in FIG. 6(a).

As shown in FIG. 6(a), reference numeral 15a denotes a reference marking on the CRT screen of the display device 15 which has been preset in relation to the housing 7 positioned and secured on the pair of mounting racks 18, and 26 denotes the image of the marking 24a displayed on the CRT screen. The semiconductor chip 12 placed on

the solder bumps 11 is moved so that the image 26 is aligned with the reference marking 15a (see FIG. 5(b)). At this time, any dust or dirt present on the semiconductor chip 12 will be displayed on the CRT screen of the display device 15. If this occurs, the semiconductor chip 12 is replaced.

Then, the electrodes 12a of the semiconductor chip 12 and the metalized pattern 10 are facedown bonded using the heating means for facedown bonding to secure the semiconductor chip 12 to the housing 7.” (Ex. 1005, pp. 3-4).

217. Thus, Hikosaka first teaches that the package “housing 7” is “secured on the pair of mounting racks 18”. (Ex. 1005, p. 3). A solid-state image sensor (“semiconductor chip 12”), which is being held by a “vacuum suction holding means”, has electrode pads (“electrodes 12a”), which are connected via “bumps 11” to conductive elements in the package. (Ex. 1005, p. 3). The image sensor is then powered on. (Ex. 1005, p. 3). A “lamp 25” projects a beam of light toward the image sensor’s front side surface. (Ex. 1005, p. 3). Before it strikes the image sensor’s surface, the light beam passes through “lens 23” and a transparent “marking plate 24” on which “a cross-shaped marking 24a is provided.” (Ex. 1005, p. 3; *see also* Fig. 4). The “cross-shaped marking 24a” thus produces a cross-shaped shadow on the image sensor’s surface. (Ex. 1005, p. 3).

218. Then, Hikosaka explains, the image sensor captures an image of the cross-shaped shadow, which is displayed on a monitor (“CRT”). (Ex. 1005, p. 3).

On the monitor, there is another cross-shaped “reference marking [15a]”, which has been pre-positioned relative to the package. (Ex. 1005, p. 3). The image sensor is then moved (still inside the package) until the image of “cross-shaped marking 24a” that is displayed on the monitor aligns with cross-shaped “reference marking [15a]”. (Ex. 1005, p. 3). Once the marks are aligned, positioning is complete, and the image sensor’s connection to the leads is mechanically fixed, *i.e.*, for normal use. (Ex. 1005, p. 4).

219. To summarize, as described above, Hikosaka, discloses that the image sensor is inserted, then electrically connected to the leads, then positioned using optical information, and then electrically/mechanically connected in a more durable, lasting manner, suitable for normal use. Thus, Hikosaka teaches that the image sensor is positioned as part of the connection process—*i.e.*, Hikosaka teaches “connecting ... while simultaneously adjusting the optical positioning of said solid-state image sensing device.”

220. It would have been obvious to one of ordinary skill in the relevant timeframe to use Hikosaka’s “connecting ... while simultaneously adjusting the optical positioning of said solid-state image sensing device” with the package of Yoshino. One of ordinary skill would have known that optical positioning was necessary for an image sensor package. The need for accurate optical positioning is admitted in the ’714 patent, as follows:

“When this conventional solid-state image sensing apparatus having the above structure is mounted to the three-eye video camera and is accurately positioned in optical manner, the base of concave part 3 or 13 of ceramic package 1 or plastic package 12 to which the CCD chip 4 is die-bonded should be processed in high accuracy.” (Ex. 1001, 1:66-2:5).

221. Yoshino and Hikosaka both teach that the image sensor package apparatus will be used in an optical system with a lens, so one of ordinary skill would have known that it was necessary to accurately optically position the image sensor.

222. Furthermore, Yoshino’s through hole, face-bonded package structure with a light transmitting glass cover would have suggested to one of ordinary skill to do optical positioning while mounting and connecting the image sensor (*e.g.*, using the techniques of Hikosaka). This makes sense because Yoshino’s through hole layout and bump bonding techniques allow the sensor to be positioned when the sensor is connected in the package, rather than in a first step when the sensor is mounted or bonded but not electrically connected, as was done in a traditional, wire-bonded package. In a package in which an image sensor is first die-bonded to the package then electrically connected to the leads via wire bonds, positioning must be complete before the electrical connection step, since the sensor cannot be moved after it is die bonded. In Yoshino’s package, the electrical connection is

made via bumps, which—as taught in Hikosaka—allow for adjustment of the position while the connection is being made.

223. Yoshino recites an embodiment in which bonding is done via press-fitted bumps, whereas Hikosaka recites an embodiment in which bonding is done via heating bumps (*e.g.*, heating solder bumps). (*Compare* Ex. 1003, p. 2 to Ex. 1005, p. 4). Hikosaka’s simultaneous optical positioning technique is nevertheless compatible with Yoshino’s package: there is nothing about Hikosaka’s technique that requires heated solder bumps. In both cases, the image sensor may be electrically connected for the positioning process (for example, using Hikosaka’s “vacuum suction holding means” to hold the image sensor in place sufficiently to enable electrical connection) before being fixed for normal use.

224. Also, Yoshino’s through hole means that the surface of the image sensor is visible while it is being placed and connected, allowing its precise position to be determined.

225. Thus, one of ordinary skill would have known that the most logical time to position the image sensor is during the connection to the leads.

226. Hikosaka discloses an image sensor package very similar to that of Yoshino. (*Compare* Ex. 1005, Fig. 4 to Ex. 1003, Fig. 1). I note that Hikosaka depicts its package inverted relative to that of Yoshino.

227. One of ordinary skill would have been motivated to use Hikosaka's simultaneous optical positioning technique with Yoshino's package because it would provide the predictable advantage of reduced fabrication time and cost over methods that involve more steps, such as a traditional approach in which the image sensor is first positioned, then wire bonded. As Hikosaka recognizes, using its simultaneous optical positioning technique "enables high precision alignment of the semiconductor chip with the housing". (Ex. 1005, p. 2). Furthermore, the combination would allow the image sensor to be active while positioning, providing feedback enabling high precision. This was an advantage because precision in image sensor placement was important for the development of higher quality optical devices.

228. The combination of Yoshino with Hikosaka also represents a known improvement on a known base system. It could have been implemented using ordinary skill without unexpected results. For example, one of ordinary skill would have been able to position and secure Yoshino's package in Hikosaka's "mounting racks 18", insert the image sensor and hold it in place using "vacuum suction holding means", place Hikosaka's "transparent marking plate 24", "lens 23", and "lamp 25" under the secured apparatus such that the lamp projected a light beam that struck the image sensor's surface, and perform Hikosaka's optical

positioning/connecting process on Yoshino's image sensor as described in ¶¶ 217-219 above.

“[13d]. securing said solid-state image sensing device to the package with an adhesive.”

229. As discussed for claim element [1d] in ¶ 113 above, Yoshino discloses the solid-state image sensing device being secured to said package via an adhesive.

230. Thus, for the foregoing reasons, I conclude that claim 13 was obvious over Yoshino in view Hikosaka.

XXI. Claim 15 is obvious over Yoshino in view of Izumi and Nagano, in further view of Hikosaka.

A. Summary of opinion

231. It is my opinion that claim 15 is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Izumi (Ex. 1016 and Ex. 1017) and Nagano (Ex 1018 and Ex. 1019), in further view of Hikosaka (Ex. 1005 and Ex. 1008).

B. Element-by-element analysis of claim 15 over Yoshino in view of Izumi, in further view of Hikosaka

1. Claim 15

“[15a]. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:”

232. As discussed in ¶¶ 209-210 above for claim element [13a], Yoshino discloses all of the limitations of claim element [15a] except for a peripheral circuit chip. As discussed in ¶¶ 121-126 above for claim element [6d], Izumi discloses a peripheral circuit chip, which would have been obvious to use in Yoshino's package.

“[15b]. mounting said solid-state image sensing device and said peripheral circuit chip on a substrate where a group of wirings is disposed in order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings,”

233. As discussed for claim element [6d] in ¶¶ 121-126 above, Izumi discloses mounting said solid-state image sensing device and said peripheral circuit chip on a substrate.

234. Izumi further discloses that a group of wirings is disposed on the substrate in order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings, as indicated by the following passage. The wirings are obviously on the substrate (“base substrate 1c”), because that is where the image sensor and chip (to which they are connected) are mounted. This is shown in Figs. 1-3 of Izumi, *e.g.*, in the version of the Izumi's Fig. 2 reproduced with Petitioner's accurate annotations in ¶ 130 above for claim element [6e], which shows that wire bonds 8 extend from the contacts on the chips to contacts on the substrate.

“The bonding pads of the solid state imaging element chip 2, not shown in the drawing, are connected to the wiring of package member 1 Peripheral circuit chips 4A to 4D are connected to leads 5 and solid state imaging element chip 2 through interposed bonding wires 8 and wiring.” (Ex. 1016, p. 335).

“[15c]. inserting the semiconductor substrate into the through hole,”

235. As discussed in ¶ 121-126 above for claim element [6d], inserting the substrate into the through hole is obvious over a combination of Yoshino and Izumi.

236. As discussed in ¶¶ 93-95 above, claim 15 uses both “substrate” and “semiconductor substrate” to mean a single semiconductor substrate. Izumi does not explicitly disclose that its substrate is a semiconductor substrate. It was well-known in the relevant timeframe to use a semiconductor material as a substrate for an image sensor and peripheral circuit elements. Semiconductor was, in this case, a functionally equivalent material to the ceramic substrate used in at least one embodiment of Izumi. (See Ex. 1016, p. 335). Of course, a semiconductor material has different properties from a ceramic material. However, either substrate material could be used here—as a base on which a solid-state image sensor and a peripheral circuit chip are mounted and connected to wirings on the base—and there would be no change in the overall function of the apparatus. In a

very similar context (a substrate with an image sensor and peripheral chip disposed on its surface), Nagano discloses use of a semiconductor substrate, as discussed in ¶¶ 144-149 above for claim element [7d]. Using only ordinary skill, Nagano's semiconductor substrate could have been substituted in the Yoshino/Izumi combination described here, and there would have been no unpredictable results. Thus, a semiconductor substrate would have been obvious.

“[15d]. connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, and”

237. As discussed in ¶¶ 212-228 above for claim element [13c], Yoshino in combination with Hikosaka renders obvious connecting an electrode pad of a *solid-state image sensing device* inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device. In other words, Yoshino in combination with Hikosaka renders obvious this claim element as to connecting an electrode pad of an image sensor. For the reasons and with the same results as discussed in ¶¶ 127-133 above for claim elements [6d]-[6e], one of ordinary skill would have been motivated to use Izumi's substrate in place of Yoshino's image sensor in claim 15.

238. It would also have been obvious for one of ordinary skill to place the electrode pads on the periphery of the substrate. This would allow them to align with Yoshino's inner leads. Also, the center of the substrate would typically be occupied by the image sensor and peripheral circuit chip. To do so would have been well within ordinary skill and would have had no unpredictable results.

“[15e]. securing the semiconductor substrate on which said solid-state image sensing device and said peripheral circuit chip are mounted to the package via an adhesive.”

239. As discussed in ¶¶ 134-135 above for claim element [6f], Yoshino in combination with Izumi renders obvious securing the semiconductor substrate on which said solid-state image sensing device and said peripheral circuit chip are mounted to the package via an adhesive.

240. Thus, for the foregoing reasons, I conclude that claim 15 was obvious over Yoshino in view of Izumi, in further view Hikosaka.

XXII. Claim 16 is obvious over Yoshino in view of Tobase, in further view of Hikosaka.

A. Summary of opinion

241. It is my opinion that claim 16 is obvious over Yoshino (Ex. 1003 and Ex. 1006) in view of Tobase (Ex. 1013 and Ex. 1022), in further view of Hikosaka (Ex. 1005 and Ex. 1008).

B. Element-by-element analysis of claim 16 over Yoshino in view of Tobase, in further view of Hikosaka

1. Claim 16

“[16a]. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in the package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:”

242. As discussed in ¶¶ 209-210 above for claim element [13a], Yoshino discloses all of the limitations of claim element [16a] except for a peripheral circuit chip. As discussed in ¶¶ 195-205 above for claim element [12d], Yoshino in combination with Tobase renders obvious a peripheral circuit chip.

“[16b]. inserting said solid-state image sensing device into the through hole,”

243. As discussed for claim element [1d] in ¶¶ 104-109 above, Yoshino discloses inserting said solid-state image sensing device into the through hole.

“[16c]. connecting an electrode pad of the solid-state image sensing device to a first inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, said first inner lead being disposed beneath a first step surface formed in said package,”

244. As discussed in ¶¶ 195-205 above for claim element [12d], Yoshino in combination with Tobase renders obvious connecting the image sensor to a first inner lead disposed beneath a first step surface formed in said package.

245. As discussed in ¶ 212 above for claim element [13c], Yoshino discloses that the image sensor's electrode pad is thus connected, and also discloses making the connection via a bump.

246. As discussed in ¶¶ 212-228 above for claim element [13c], Yoshino in combination with Hikosaka renders obvious “connecting ... while simultaneously adjusting the optical positioning of the solid-state image sensing device.” For the same reasons (and with the same results) as discussed there, one of ordinary skill would have been motivated to combine Hikosaka with Yoshino and Tobase.

“[16d]. securing the solid-state image sensing device to the package via an adhesive,”

247. As discussed for claim element [1d] in ¶ 113 above, Yoshino discloses securing the solid-state image sensing device to the package via an adhesive.

“[16e]. inserting the peripheral circuit chip into the through hole,”

248. As discussed in ¶¶ 195-205 above for claim element [12d], Yoshino in combination with Tobase renders obvious a peripheral circuit chip. It would have been obvious for one of ordinary skill to insert the peripheral circuit chip into the through hole, as Yoshino discloses for the image sensing device (*see* claim element

[1d] in ¶¶ 104-109 above). For the same reasons discussed there, there would have been no other way to place the peripheral circuit chip into the package.

“[16f]. connecting an electrode pad of the peripheral circuit chip to a second inner lead via a bump or an anisotropic conductor having only vertical conductivity, to complete an electrical connection, said second inner lead being disposed beneath a second step surface formed in said package, and”

249. As discussed in ¶¶ 195-205 above for claim element [12d], Yoshino in combination with Tobase renders obvious connecting the peripheral circuit chip to a second inner lead disposed beneath a second step surface formed in said package. Yoshino and Tobase both disclose bump bonding. (Ex. 1003, p. 2; Ex. 1022, ¶ 0009). Thus, it was obvious that the connection point of the peripheral circuit chip should be an electrode pad. This is a standard feature of bump-bonded chips. As discussed in ¶ 212 above for claim element [13c], Yoshino discloses an electrode pad.

“[16g]. securing the peripheral circuit chip to the package via an adhesive.”

250. As discussed in ¶ 204 above for claim element [12d], securing the peripheral circuit chip to the package via an adhesive would have been obvious.

251. Thus, for the foregoing reasons, I conclude that claim 16 was obvious over Yoshino in view of Tobase, in further view Hikosaka.

XXIII. Claim 1 is obvious over Wakabayashi.

A. Summary of opinion

252. It is my opinion that Claims 1 is obvious over Wakabayashi (Ex. 1004 and Ex. 1007). Wakabayashi teaches a package essentially like that of claim 1. Wakabayashi does not expressly recite inserting the solid-state image sensing device into an inlet of the package's opening which has a wider area. However, this would have been obvious, for the reasons described below.

B. Element-by-element analysis of claim 1 over Wakabayashi

1. Claim 1

[1a]. “A solid-state image sensing apparatus comprising:”

253. Wakabayashi discloses a solid-state image sensing apparatus, *i.e.*, an apparatus comprising a solid-state image sensing device. Wakabayashi refers to its solid-state image sensing device as a “CCD chip”. A CCD chip is a type of semiconductor image sensor, and is therefore solid-state (since semiconductor chips are solid state). Wakabayashi refers to the entire solid-state image sensing apparatus as a “solid-state image pickup device”. Wakabayashi states:

“The present invention relates to a solid-state image pickup device using a CCD chip, and is particularly one having a package” (Ex. 1004, ¶ 0001).

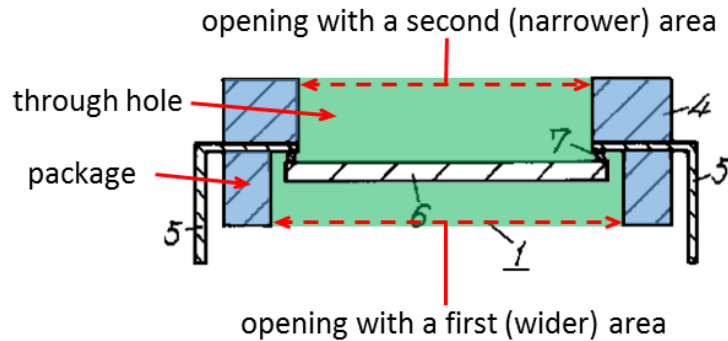
“[1b]. a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,”

254. In the following passages, Wakabayashi discloses a package having a through hole therein, which Wakabayashi describes as “a space for disposing a CDD chip”:

“The solid-state image pickup device is comprised of a package 4 made of a transparent resin, leads 5, a CCD chip 6, and bumps 7 which join the inner leads to the CCD chip 4 [sic.: CCD chip 6].” (Ex. 1004, Abstract).

““[The] package ... compris[es] a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, a space for disposing a CDD [sic.: CCD] chip, the inner lead sections of the lead frame being exposed to the space, and the face opposite to the light-receiving face being open.” (Ex. 1004, ¶ 0005).

255. The below version of Wakabayashi’s Fig. 1 has been accurately annotated and highlighted by Petitioner to show that Wakabayashi’s package (4) has a through hole, openings on both end faces thereof, and different opening areas of said openings. The through hole is highlighted green, and the package body is highlighted blue.



“[1c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and”

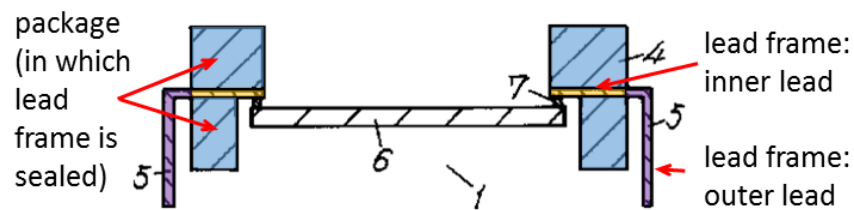
256. Wakabayashi discloses a lead frame comprising inner leads and outer leads. The first below passage discloses the lead frame comprising inner leads, and also discloses said lead frame being sealed in said package (“package ... interposing a lead frame”). The second below passage refers to the lead frame as “leads 5”.

“The solid-state image pickup device according the invention has the basic construction of comprising a CCD chip joined via bumps to the inner lead sections of a package made of a transparent resin comprising a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, a space for disposing a CDD chip, the inner lead sections of the lead frame being exposed to the space, and the face opposite to the light-receiving face being open.” (Ex. 1004, ¶ 0005).

“In FIG. 1, reference numeral 1 is a cross section of the basic construction of the solid-state image pickup device, which includes a package 4 formed with a transparent resin, leads 5, a CCD chip 6,

bumps 7 which join the inner lead sections to the CCD chip 4.” (Ex. 1004, ¶ 0010).

257. The above passage does not explicitly describe outer leads. However, Wakabayashi’s lead frame also has outer leads. This is shown in Wakabayashi’s Fig. 1, a version of which is reproduced below with accurate annotations and highlighting by Petitioner that show the lead frame with the inner lead (orange), the outer lead (purple), and the package (blue).



“[1d]. a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.”

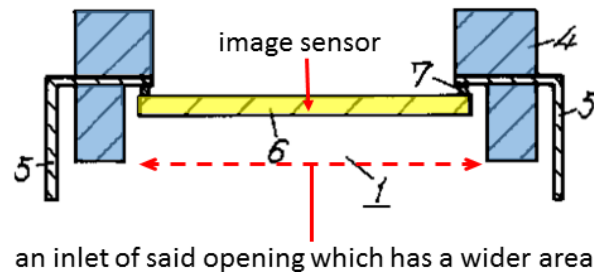
258. As noted above, Wakabayashi describes its solid-state image sensing device as a “CCD chip”. In the following passage, Wakabayashi discloses that its solid-state image sensing device is mounted in said package.

“The solid-state image pickup device according the invention has the basic construction of comprising a CCD chip joined via bumps to the inner lead sections of a package” (Ex. 1004, ¶ 0005).

259. Wakabayashi does not expressly teach that the image sensor is mounted by being inserted from an inlet of said opening which has a wider area. It would have been obvious to one of ordinary skill to insert the image sensor this way. Wakabayashi discloses that the image sensor is bonded to the inner leads, as disclosed in the following passage:

“In FIG. 1, reference numeral 1 is a cross section of the basic construction of the solid-state image pickup device, which includes a package 4 formed with a transparent resin, leads 5, a CCD chip 6, bumps 7 which join the inner lead sections to the CCD chip 4.” (Ex. 1004, ¶ 0010).

260. Wakabayashi's Fig. 1 shows that the image sensor's connection to the inner lead is from the bottom side of the package—the side with the wider opening. Therefore, this is the opening that would be natural for one of ordinary skill to use. Below is a version of Fig. 1 which Petitioner has annotated to accurately illustrate this. Also, Fig. 1 shows that the image sensor fits into the wider opening, but would not fit (or at least, would not easily fit) through the narrower, top opening. Also, there were only two ways to insert the image sensor, the top opening and bottom opening. One of ordinary skill would easily have been able to visualize both possibilities. There would have been no unpredictable results.

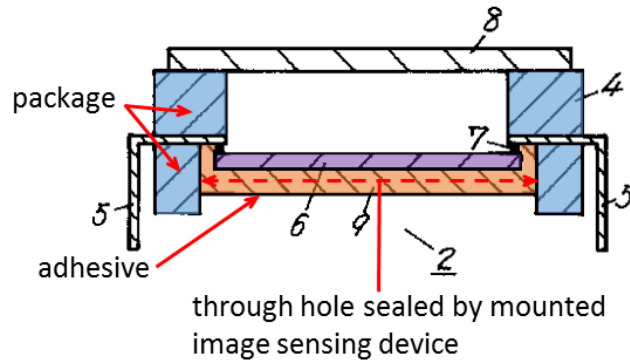


261. Wakabayashi also teaches that mounting the solid-state image sensing device thereby seals the through hole and that the solid-state image sensing device is secured to said package via an adhesive, “adhesive resin”, in the same way that the image sensor of the ’714 patent seals the through hole and is mounted in the package. This is described in the following passage and shown in Wakabayashi’s Fig. 2.

“FIG. 2 is a cross section of a solid-state image pickup device in which, in addition to the basic structure discussed above, the back face side of the chip is further sealed with an adhesive resin 7 [sic: adhesive resin 9]. By constructing the device in this way, the bump joints are reinforced....

For the adhesive resin, epoxy-based potting resins known as the sealing materials for TAB, for example, can be suitably used.” (Ex. 1004, ¶¶ 0015-0016)

262. Below is a version of Wakabayashi’s Fig. 2 that Petitioner has accurately annotated to show that the solid-state image sensing device seals the through hole and that the solid-state image sensing device is secured to the package via an adhesive.



The adhesive (highlighted orange) is labeled “9”. The above passage refers to “adhesive resin 7”. This is an error. Wakabayashi indicates that “7” indicates the “bump section” or “bumps 7”, as in the below passages:

“The solid-state image pickup device is comprised of a package 4 made of a transparent resin, leads 5, a CCD chip 6, and bumps 7”
(Ex. 1004, Abstract).

“1 cross section of a solid-state image pick up device

4 package

5 lead

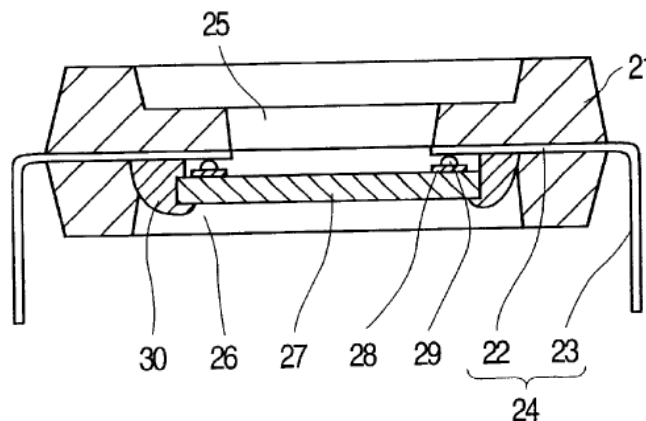
6 CCD chip

7 bump section”. (Ex. 1004, Explanation of Reference Numerals).

263. Also, the passage cited in ¶ 261 above explains that the “adhesive resin” resin seals “the back face side of [CCD] chip [6]”. Thus, it corresponds to the element indicated by the numeral “9” in Fig. 2.

264. The passage cited in ¶ 261 above indicates that the adhesive “reinforce[s]” the connection, indicating that Wakabayashi’s adhesive serves to secure the image sensor to the package. This is also apparent from the fact that the “adhesive resin” is an adhesive that is in contact with the sensor and with the inner walls of the package (as shown in Fig. 2).

265. For comparison, the ’714 patent’s Fig. 2 (reproduced below) shows the image sensor sealing the through hole and secured with adhesive in the same way.



266. Thus, for the foregoing reasons, I conclude that claim 1 was obvious over Wakabayashi.

XXIV. Claims 2-4 are obvious over Wakabayashi in view of Fujii.

A. Summary of opinion

267. It is my opinion that claims 2-4 are anticipated by Wakabayashi (Ex. 1004 and Ex. 1007) in view of Japanese Pat. App. Pub. No. H06-85221 (“Fujii”) (Ex. 1025, certified translation as Ex. 1024).

B. Fujii is prior art

268. I understand that Fujii is prior art to the '714 patent, because it was published on March 25, 1994.

C. Summary of Fujii

269. Fujii discloses a package for a solid-state image sensing device. (Ex. 1024, Abstract). The package features a horizontal ledge projecting into its interior space that serves to hold the package's transparent lid. (Ex. 1024, Fig. 1). This is much like the ledge disclosed in the '714 patent, as seen in Figs. 7 and 8 of the '714 patent. (Ex. 1001, 7:29-31; 8:42-42). Fujii does not disclose that the hole of its package goes all the way through the bottom side of the package. However, it would have been obvious to use Fujii's ledge in a package that did feature a through hole, such as that of Wakabayashi, as described below.

D. Element-by-element analysis of claims 2-4 over Wakabayashi in view of Fujii.

1. Claim 2

“[2a]. A solid-state image apparatus comprising:”

270. As discussed above in ¶ 253 for claim element [1a], Wakabayashi discloses a solid-state image sensing apparatus. As discussed in ¶ 77 above, the omission of the term “sensing” in claim element [2a] appears to have no impact on the meaning of the term.

“[2b]. a package comprising a main body having a through hole

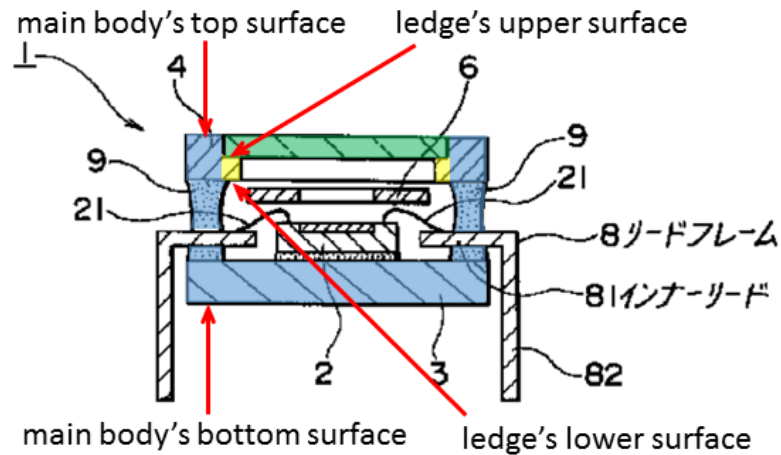
therein, said main body having a top surface and a bottom surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward the center of said through hole, said ledge comprising an upper surface and a lower surface;”

271. Wakabayashi teaches a package with a through hole, as discussed in ¶¶ 254-255 above for claim element [1a]. However, Wakabayashi’s package does not explicitly feature a separate “main body” and “ledge”.

272. Fujii discloses a package with separate main body and ledge portions. Fujii discloses a package (“lid 4” and “base 3” joined by “adhesive 9”) for a “solid-state image sensor 2”, as described in the following passage:

“As shown in the sectional side view in FIG. 4, a lead frame 8 is interposed between the base 3 and the lid 4 of the solid-state image pickup device 1 via an adhesive 9, and the solid-state image sensor 2 and the inner leads 81 of the lead frame 8 are wired using bonding wires 21 under the light shielding plate 6.” (Ex. 1024, ¶ 0013).

273. Below is a version of Fujii’s Fig. 4 that Petitioner has accurately annotated to show that Fujii’s package (which is highlighted blue) comprises a main body having a top surface and a bottom surface and a ledge (highlighted yellow) formed on said main body so as to extend inwardly toward the center of the package.



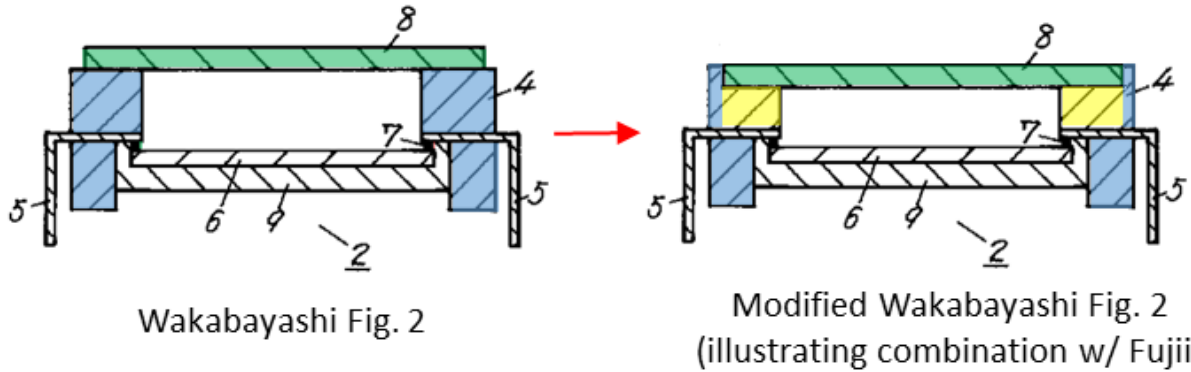
274. As seen in the figure, the “ledge” portion (highlighted yellow), holds “cap 5” (highlighted green), which is the transparent lid of Fujii’s package, as described in the following passage:

“Moreover, as shown in the plan view, FIG. 2, the light shielding plate 6 disposed under the cap 5 of the solid-state image pickup device 1 is attached to four supports 7, for example, and the effective pixel region (hatched section in the figure) of the solid-state image sensor 2 not covered by the light shielding plate 6 is visible from the top of the solid-state image pickup device 1. Accordingly, light from above the solid-state image pickup device 1 reaches the effective pixel region of the solid-state image sensor 2 through the cap 5 made of, for example, substantially transparent glass.” (Ex. 1024, ¶ 0010).

275. Although the numeral “5” was omitted from Fujii’s Fig. 4, it is clear that this is the transparent “cap 5”. It would need to be transparent in order to allow light to strike the surface of the image sensor. Furthermore, the equivalent element is labeled “5” in other of Fujii’s figures, such as Fig. 1, Fig. 2, and Fig. 7.

276. It would have been obvious for one of ordinary skill to use Fujii's ledge in Wakabayashi's package, so that the ledge extends inwardly toward the center of said through hole. For example, one of ordinary skill would have known to extend the edge of Wakabayashi's package upward in order to hold Wakabayashi's transparent lid ("sealing glass" 8). (Ex. 1004, ¶ 0002). This would create the ledge portion of the package disclosed in Fujii. A package with a transparent lid located on a ledge inside the package was a known substitute for a package in which the transparent lid sits *on top* of the package, as shown in Wakabayashi's figures. There would have been no unpredictable results from the substitution.

277. Below are versions of Wakayashi's Fig. 2 that Petitioner has modified in order to accurately illustrate the combination with Fujii. On the left, Petitioner has highlighted Wakabayashi's Fig. 2 to show the main body portion of the package blue, the ledge yellow, and the transparent lid green. On the right, Petitioner has maintained this highlighting, but has modified Fig. 2 to move the transparent lid so that it rests not on top of the package, but inside the package on a ledge formed on said main body so as to extend inwardly toward the center of said through hole, as disclosed in Fujii.



278. Wakabayashi does not expressly indicate what the “8” in its Fig. 2 indicates. It is clear that this is a transparent lid, which Wakabayashi refers to as a “sealing glass” in the passage below. It would need to be transparent (*e.g.*, glass) in order to allow light to strike the surface of the image sensor. It is also shown “sealing” the package.

“(Prior Art) A conventional solid-state image pickup device is constructed by placing and adhering a CCD chip in a ceramic package, being joined to the inner leads by wire bonding and sealed using sealing glass. Since a conventional ceramic package is expensive, a less expensive and more compact plastic package has been desired.” (Ex. 1004, ¶ 0002).

“[2c]. a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and”

279. As discussed in ¶¶ 256-257 above for claim element [1c], Wakabayashi discloses a lead frame comprising inner leads and outer leads, said

lead frame being sealed in said package. Wakabayashi's Fig. 2—as reproduced at ¶ 277 above with highlighting and modifications by Petitioner that illustrate Wakabayashi's combination with Fujii—accurately shows that, when combined with Fujii's ledge, Wakabayashi's lead frame (“lead frame” or “leads 5” (Ex. 1004, ¶ 0005; ¶ 0010)) is sealed in the package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge.

“[2d]. a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;”

280. As discussed in ¶ 258 above for claim element [1d], Wakabayashi discloses a solid-state image sensing device, which Wakabayashi refers to as a “CCD chip”. Wakabayashi's Fig. 2—as reproduced at ¶ 277 above with highlighting and modifications by Petitioner—illustrates that Wakabayashi's solid-state image sensing device has an upper surface and a lower surface.

281. In the following passage, Wakabayashi discloses a plurality of electrical connection points on the solid-state image sensing device (*i.e.*, electrode pads, which Wakabayashi refers to a “bonding pads”), and that each one is coupled to one of the inner leads:

“In another aspect, the joining of the chip to the inner leads via the bumps is performed via the conductive adhesive layer formed on the

surfaces of the bumps disposed on the bonding pads of the CCD chip.” (Ex. 1004, ¶ 0006).

282. Wakabayashi’s Fig. 2 does not label the electrode pads. However, it illustrates that they are on the upper surface of the image sensor. This is because it is the image sensor’s upper surface that is joined to the inner leads (5) via bumps (7). Since the above passage indicates that the joining is accomplished via “bumps disposed on the bonding pads of the [image sensor]”, the bonding pads (electrode pads) must also be on the upper surface of the image sensor.

“[2e]. said solid-state image sensing device being secured to said main body of said package via an adhesive.”

283. As discuss in ¶¶ 261-265 above for claim element [1d], Wakabayashi discloses said solid-state image sensing device being secured to said package via an adhesive. Wakabayashi’s Fig. 2—as reproduced at ¶ 277 above with highlighting and modifications by Petitioner that illustrate Wakabayashi’s combination with Fujii—accurately shows that the solid-state image sensing device is secured to the *main body* portion of the package, when combined with Fujii’s ledge.

284. Thus, for the foregoing reasons, I conclude that claim 2 was obvious over Wakabayashi in view of Fujii.

2. Claim 3

“3. The solid-state image sensing apparatus of claim 2, wherein

each of the electrode pads is connected to the inner lead via a bump.”

285. In the following passage, Wakabayashi discloses that each of the electrode pads of the solid-state image sensing device is connected to the inner lead via a bump. Wakabayashi refers to the solid-state image sensing device as “the CCD chip” and to the electrode pads as “bonding pads”.

“In another aspect, the joining of the chip to the inner leads via the bumps is performed via the conductive adhesive layer formed on the surfaces of the bumps disposed on the bonding pads of the CCD chip.” (Ex. 1004, ¶ 0006).

286. Thus, for the foregoing reasons, I conclude that claim 3 was obvious over Wakabayashi in view of Fujii.

3. Claim 4

“4. The solid-state image sensing apparatus of claim 2, wherein each of the electrode pads is connected to the inner lead via an anisotropic conductor having only vertical conductivity.”

287. As discussed in ¶¶ 177-178 above for claim 10, Wakabayashi discloses that each of the electrode pads is connected to the inner lead via an anisotropic conductor. As also discussed there, it is obvious that Wakabayashi’s anisotropic conductor is one having only vertical conductivity.

288. Thus, for the foregoing reasons, I conclude that claim 4 was obvious over Wakabayashi in view of Fujii.

XXV. Claim 5 is obvious over Wakabayashi in view of Fujii, in further in view of Onishi.

A. Summary of opinion

289. It is my opinion that claim 5 is obvious over Wakabayashi (Ex. 1004 and Ex. 1007) in view of Fujii (Ex. 1024 and Ex. 1025), in further view of Onishi (Ex. 1014 and Ex. 1015).

B. Element-by-element analysis of claim 5 over Wakabayashi in view of Fujii, in further view of Onishi.

1. Claim 5

“5. The solid-state image sensing apparatus of claim 2, wherein a tip of the inner lead to which the electrode pad is connected extends beyond said ledge.”

290. Wakabayashi does not expressly disclose an inner lead with an inwardly extending tip. Fujii does disclose such an inwardly extending tip, as can be seen in Fujii’s Fig. 4, reproduced for ¶ 273 above with annotations by Petitioner. Onishi also discloses an inner lead with an inwardly extending tip, as discussed in ¶¶ 185-186 above for claim 11. Onishi discloses this in a package very similar to that of Wakabayashi’s.

291. It would have been obvious for one of ordinary skill to use Onishi’s or Fujii’s extended inner lead with Wakabayashi’s package, so that the tip of the inner

lead extends beyond said ledge. As discussed in ¶ 187 above for claim 11, this would have provided the advantages of allowing the inner lead to be detached from the ledge so that the lead could flex, which would relieve stress during the hardening of the adhesive. Also, it would have allowed for accuracy in positioning of the image sensor and of bonding of the inner lead to the sensor's pads. Furthermore, it was a known variation on Yoshino's base system, and its use would have had no unpredictable results.

292. Thus, for the foregoing reasons, I conclude that claim 5 was obvious over Wakabayshi in view of Fujii, in further view of Onishi.

XXVI. Claim 13 is obvious over Wakabayashi in view of Hikosaka.

A. Summary of opinion

293. It is my opinion that Claims 13 is obvious over Wakabayashi (Ex. 1004 and Ex. 1007) in view of Hikosaka (Ex. 1005 and Ex. 1008).

B. Element-by-element analysis of claim 13 over Wakabayashi in view of Hikosaka

1. Claim 13

“[13a]. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package, said manufacturing method comprising the steps of:”

294. As discussed in ¶¶ 253-266 above for claim elements [1a]-[1d], Wakabayashi discloses a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package.

295. Wakabayashi also discloses steps for “construct[ing]” a solid-state image sensing apparatus—*i.e.*, a manufacturing method. For example, Wakabayashi states:

“The solid-state image pickup device according the invention has the basic construction of comprising a CCD chip joined via bumps to the inner lead sections of a package made of a transparent resin comprising a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, a space for disposing a CDD [sic.: CCD] chip, the inner lead sections of the lead frame being exposed to the space, and the face opposite to the light-receiving face being open.

In another aspect, the joining of the chip to the inner leads via the bumps is performed via the conductive adhesive layer formed on the surfaces of the bumps disposed on the bonding pads of the CCD chip.

In another aspect, it is constructed by sealing the back face side of the chip with an adhesive resin.” (Ex. 1004, ¶¶ 0005-007).

“[13b]. inserting said solid-state image sensing device into said through hole,”

296. As discussed in ¶ 259 above for claim element [1d], inserting said solid-state image sensing device into said through hole is obvious from Wakabayashi.

“[13c]. connecting an electrode pad of the solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device, and”

297. As recited in the following passage, Wakabayashi discloses an electrode pad of the solid-state image sensing device, “bonding pads of the CCD chip”. Wakabayashi also discloses connecting an electrode pad of the solid-state image sensing device to the inner lead via a bump. Wakabayashi states:

“The bumps are formed on the bonding pads of the CCD chip 6 by stud bumping or plating beforehand, and the chip is bonded to the inner leads 5 within the package via the conductive layer disposed on the bump surfaces by thermosetting or photosetting.” (Ex. 1004, ¶ 0013).

298. As discussed in ¶¶ 177-178 above for claim 10, Wakabayashi also discloses that the connection may be made with an anisotropic conductor. As also discussed there, it is obvious that Wakabayashi’s anisotropic conductor is one having only vertical conductivity.

299. Wakabayashi does not expressly disclose simultaneously adjusting the optical positioning of said solid-state image sensing device. This would have been obvious, for the same reasons discussed in ¶¶ 212-228 above for claim element [13c] with regard to Yoshino. As with Yoshino (which discloses a very similar package), Wakabayashi's solid-state image sensing apparatus would have suggested simultaneously adjusting the optical positioning to one of ordinary skill. For the same reasons discussed in ¶¶ 220-228 (with regard to Yoshino), one of ordinary skill would have been motivated to combine Wakabayashi with Hikosaka, with the same predictable, advantageous results.

300. As discussed in ¶ 228 (with regard to Yoshino), the combination would have been well within ordinary skill, with predictable results. For example, one of ordinary skill would have been able to position and secure Wakabayashi's package in Hikosaka's "mounting racks 18", insert the image sensor and hold it in place using "vacuum suction holding means", place Hikosaka's "transparent marking plate 24", "lens 23", and "lamp 25" under the secured apparatus such that the lamp projected a light beam that struck the image sensor's surface, and perform Hikosaka's optical positioning/connecting process on Wakabayashi's image sensor as described in ¶¶ 217-219 above.

“[13d]. securing said solid-state image sensing device to the package with an adhesive.”

301. As discussed in ¶ 261-265 above for claim element [1d], Wakabayashi discloses securing said solid-state image sensing device to the package with an adhesive.

302. Thus, for the foregoing reasons, I conclude that claim 13 was obvious over Wakabayashi in view Hikosaka.

XXVII. Oath

303. This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare under penalty of perjury under the laws of the United States of America that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

4/13/2006

Date

R. Michael Guidash

R. Michael Guidash