



PATENT
ATTORNEY DOCKET NO. 43890-225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yoshikazu Sano et al.

Serial No.: 08/809,845

Group Art Unit: 2814

Filed: June 16, 1997

Examiner: N. NGO

For: SOLID-STATE IMAGE SENSING APPARATUS AND
MANUFACTURING METHOD THEREOF

AMENDMENT TRANSMITTAL

Honorable Commissioner of Patents
and Trademarks,
Washington, D.C. 20231

Sir:

1. ☒ Transmitted herewith is an amendment for the above-identified application.

STATUS

2. ☒ Applicant is ☐ is small entity - verified statement:
☐ attached ☐ already filed.
☒ other than a small entity.

EXTENSION OF TIME

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. §1.136 apply.

- (a) ☒ Applicant petitions for an extension of time for the total number of months checked below:

EXTENSION (months)	FEE FOR SMALL ENTITY	FEE FOR OTHER THAN SMALL ENTITY
<input type="checkbox"/> one month	\$ 55.00	\$ 110.00
<input checked="" type="checkbox"/> two months	190.00	380.00
<input type="checkbox"/> three months	435.00	870.00
<input type="checkbox"/> four months	680.00	1,360.00

Fee \$380.00

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for ☐ months has already been secured and the fee paid therefor of ☐ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this Request \$

- (b) ☐ Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

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4. X The fee for claims has been calculated as shown below:

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	:	:	:	:	:
Claims	: 16	: 20	: 0	: x \$ 18.00 =	: 0
Independent	:	:	:	:	:
Claims	: 9	: 9	: 0	: x \$ 78.00 =	: 0
Multiple Dependent Claims (first presentation)	:	:	:	: \$260.00 =	: 0
Total	:	:	:	:	: 0
			Reduction by 1/4 for small entity	:	: 0
TOTAL FEE	:	:	:	:	: 0

- (a) X No additional fee for claims is required.

-OR-

- (b) The total additional fee for claims required \$

FEE PAYMENT

5. Attached is a check in the amount of \$.

- X Charge Deposit Account No. 13-0203 the amount of \$380.00. A duplicate copy of this Transmittal is enclosed for accounting purposes.

FEE DEFICIENCY

- X If any additional extension and/or fee is required, this is the request therefor and to charge Deposit Account No. 13-0203.

AND/OR

- X If any additional fee for claims is required, charge Deposit Account No. 13-0203. A duplicate copy of this Transmittal is enclosed for accounting purposes.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date:

12/21/98

By:



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Yoshikazu SANO et al.

Serial No.: 08/809,845

Filed: June 16, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF



Group Art Unit: 2814

Examiner: N. NGO

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AMENDMENT UNDER 37 C.F.R. § 1.115

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 20, 1998, having
a shortened statutory period for response set to expire on
October 20, 1998, a two month extension of time up to and
including December 20, 1998 being filed concurrently herewith,
please amend the above-identified application as follows:

IN THE DRAWINGS:

Please amend Figs. 9 and 10 to include the legend "Prior
Art" as shown on the marked up copies thereof, which are
enclosed herewith.

IN THE CLAIMS:

Please cancel claim 2, add new claim 17 and amend claim 1
and 3-16 as follows:

1. (Amended) A solid-state image sensing apparatus

comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole], and

[(c)] a solid-state image sensing device [element (CCD chip)] mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.

3. (Amended) The solid-state image sensing apparatus of Claim [2] ^{2^v} ~~1~~, wherein each of the electrode pads [pad of the CCD chip] is connected [via the bump] to the inner lead via a bump.

4. (Amended) The solid-state image sensing apparatus of Claim [2] ^{2^v} ~~1~~, wherein each of the electrode pads [pad of the CCD chip] is connected to the inner lead via an anisotropic conductor having only vertical conductivity.

5. (Amended) The solid-state image sensing apparatus of Claim [2] ^{2^v} ~~1~~, wherein a tip of the inner lead to which the electrode pad [of the CCD chip] is connected [is protruded from around the opening] extends beyond said ledge.

6. (Amended) A solid-state image sensing apparatus comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole],

[(c)] a substrate on which a [CCD chip] solid-state image sensing device and a peripheral circuit [element] chip are mounted being inserted into the package from a wider opening thereof, and

[(d)] an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,

said substrate being secured to said package via an adhesive.

7. (Amended) A solid-state image sensing apparatus comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole],

[(c)] a semiconductor substrate [on which, except a]

having a solid-state image sensing device [place a CCD chip is formed,] and a peripheral circuit chip [element is] disposed on an upper surface thereof, said semiconductor substrate being inserted into a plastic package[,] via the larger of two [which has a plurality of] openings [having different opening areas, from a wider opening of] formed in said package, and

[(d)] an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around [a] the smaller opening of said package,

said semiconductor substrate being secured to said package via an adhesive.

8. (Amended) The solid state image sensing apparatus of Claim 6 or Claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the [CCD chip] solid-state image sensing device.

9. (Amended) The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad [of] formed on the substrate is connected to the inner lead via a bump.

10. (Amended) The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad [of] formed on the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity.

11. (Amended) The solid-state image sensing apparatus of

Claim 6 or Claim 7, wherein an electrode pad [of] formed on the
substrate is connected to the inner lead at an outer portion of
said lead, said outer portion of said lead extending into the
openings [of which tip is protruded from around the opening] of
the package.

12. (Amended) A solid-state image sensing apparatus
comprising:

[(a)] a package having a through hole therein, openings
on both end faces thereof, and different opening areas of said
openings,

[(b)] a lead frame comprising [the] inner leads and
outer leads, said lead frame being sealed in said package [which
has a through hole], and

[(c)] a solid-state image sensing [element (CCD chip)]
device and a peripheral circuit chip [element] both mounted in
said package, said [CCD chip] solid-state image sensing device
being connected to a first inner lead exposed [from] beneath a
first step surface [situated to] formed in said package, said
solid-state image sensing device being secured to said package
via an adhesive, and said peripheral circuit [element] chip being
connected to a second inner lead exposed [from] beneath a second
step surface [situated to] formed in said package, said
peripheral circuit chip being secured to said package via an
adhesive.

13. (Amended) A manufacturing method of a solid-state image

sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device mounted in said package, said manufacturing method comprising the steps of:

[(a)] [insert] inserting said [CCD chip] solid-state image sensing device into said through hole [from a wider opening area of the package],

[(b)] [connect] connecting an electrode pad of the [CCD chip] solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning of said solid-state image sensing device [as well as electrical connection], and

[(c)] [fix a back side of the] securing said solid-state image sensing device [CCD chip] to the package with [glue] an adhesive.

14. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising the steps of:

[(a) form] forming said [CCD chip] solid-state image

sensing device and a group of wirings on a semiconductor substrate,

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^
[(b) mount] mounting said peripheral circuit [element] chip on [a surface except the preoccupied place by the ~~the~~ CCD chip] solid-state image sensing device to connect with said group of wiring ^{on} said semiconductor surface,

OC 3/15/99
[(c) insert] inserting said semiconductor substrate into the through hole [from a wider opening of the package],

ALW
[(d) connect] connecting an electrode pad disposed on [around] the semiconductor substrate to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning of said solid-state image sensing device [and electrical connection], and.

[(e)] [fix a back side of] securing the semiconductor substrate on which the [CCD chip] solid-state image sensing device and the peripheral circuit [element] chip are mounted to the package [with glue] via an adhesive.

15. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising steps of:

[(a) mount] mounting said [CCD chip] solid-state image

sensing device and said peripheral circuit [element] chip on a substrate where a group of wirings is disposed in order to connect the [CCD chip] solid-state image sensing device and the peripheral circuit chip to the group of wirings,

[(b) insert] inserting the semiconductor substrate into the through hole [from a wider opening of the package],

[(c) connect] connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning [and electrical connection] of the solid-state image sensing device, and

[(d) fix a back side of] securing the semiconductor substrate [where] on which said [CCD chip] solid-state image sensing device and said peripheral circuit [element] chip are mounted to the package [with glue] via an adhesive.

16. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in the package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising steps of:

[(a) insert] inserting said [CCD chip] solid-state image sensing device into the through hole [from a wider opening of the package],

[(b) connect] connecting an electrode pad of the [CCD chip] solid-state image sensing device to a first inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning [and electrical connection] of the solid-state image sensing device, said first inner lead being disposed beneath a first step surface formed in said package,

[(c) fix a back side of] securing the [CCD chip] solid-state image sensing device to the package [with glue] via an adhesive,

[(d) insert] inserting the peripheral circuit [element] chip into the through hole [from the wider opening of the package],

[(e) connect] connecting an electrode pad of the peripheral circuit [element] chip to a second inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, to complete an electrical connection, said second inner lead being disposed beneath a second step surface formed in said package, and

[(f) fix a back side of] securing the peripheral circuit [element] chip to the package [with glue] via an adhesive.

Please add new claim 17 as follows:

17. A solid-state image apparatus comprising:
a package comprising a main body having a through hole therein, said main body having a top surface and a bottom

surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward the center of said through hole, said ledge comprising an upper surface and a lower surface;

Added
a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and

a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;

said solid-state image sensing device being secured to said main body of said package via an adhesive.--

R E M A R K S

I. Introduction

In response to the Office Action, Applicants have amended Figs. 9 and 10 to include the legend "Prior Art." In addition, claims 1, 3-7 and 9-16 have been amended to clearly distinguish the present invention over the cited art. Claim 2, which is now cancelled, has been rewritten as new claim 17. No new matter has been added. In addition, in an effort to utilize consistent terms throughout the claims, the phrases "solid-state imaging element" and "CCD chip" and been amended to "solid-state imaging

device. Further, the phrase "peripheral circuit element" has been changed to "peripheral circuit chip."

In addition, Applicants wish to verify that the Examiner has received the Supplemental Information Disclosure Statement (IDS) filed on December 15, 1997. An acknowledgement of review of the IDS by initialing and returning the PTO-1449 form is respectfully requested.

II. The Rejection Of Claims 1-6, 13 And 15 Under 35 U.S.C. § 103, As Being Unpatentable Over Takashi et al. Is Overcome By Applicants' Amendments To The Claims

Claims 1-6, 13 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over Takashi et al. (JP 07-45803). For the following reasons Applicants respectfully submit that the rejection is overcome by Applicants' amendments to the claims.

A. The Prior Art Cited By The Examiner Does Not Disclose Or Suggest Applicants' Novel Design As Recited By The Pending Claims

As set forth in the pending claims, the present invention discloses an apparatus which allows for the accurate positioning and mounting of a CCD chip (i.e., solid-state image sensing device). The image sensing apparatus of the present invention comprises a package to which a CCD chip is mounted. The package has leads sealed therein, which are coupled to the CCD chip. The package also has a through hole which allows an optical positioning adjusting device to view the CCD chip during the mounting process so that the CCD chip can be properly positioned.

The CCD chip further comprises electrodes which are coupled to the inner portion of the leads sealed in the package. The electrodes, which are bumps, are pressed into contact with the leads during the mounting process and allow for adjustment of the position of the CCD chip. When the CCD chip is positioned in the desired location, an adhesive is utilized to secure the CCD chip to inner sidewalls of the package, thereby securing the CCD chip in the proper location. It is noted that all of the independent claims have been amended to recite that the CCD chip or the substrate holding the chip are secured to the package via an adhesive.

Moreover, amended claim 5 recites that the inner lead extends beyond the ledge formed in the package. This advantageously makes the lead more flexible, which facilitates the optical positioning of the CCD chip as well as the coupling between the lead and the bump electrode (see, page 10, lines 2-7).

Clearly, Takashi fails to disclose or suggest the present invention as recited by the amended claims. Most importantly, Takashi does not disclose the use of an adhesive for securing the CCD chip to the package. Takashi appears to simply disclose that the CCD chip is coupled to the leads via bumps 7, which can be accomplished, for example, by a reflow solder process. However, by utilizing such a bonding process to couple the CCD chip to the leads, the precise position of the chip cannot be controlled to the accuracy the present invention provides. Thus, it is clear that Takashi fails to disclose the present invention. Moreover,

as Takashi neither discusses nor addresses the need for precise placement of the CCD chip, it is clear that the present invention is not obvious in view of Takashi.

For the same reasons, Applicants respectfully submit that new claim 17 is patentable over Takashi.

III. The Rejection Of Claims 7-12, 14 And 16 Under 35 U.S.C. § 103, As Being Unpatentable Over Takashi et al. In View Of Nicewarner Is Overcome By Applicants' Amendments To The Claims

Claims 7-12, 14 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Takashi et al. (JP 07-45803) in view of Nicewarner (USP No. 5,327,325). For the following reasons Applicants respectfully submit that the rejection is overcome by Applicants' amendments to the claims.

For the reasons set forth above, it is clear that Takashi fails to disclose or suggest the present invention. Nicewarner does not cure the deficiencies of Takashi.

Nicewarner relates to a flip-chip bonding method utilized to position a plurality of chips with a given package. As with Takashi, Nicewarner utilizes a reflow solder process to couple the electrode bumps on the chips to one another and wire bond connections to couple the chips to leads.

More importantly, however, is that contrary to the assertion in the pending rejection, Nicewarner does not provide a through hole. Referring to Figs. 1 and 3 of Nicewarner, Nicewarner discloses a package have a center portion (highlighted in red on the enclosed copy of Fig. 1) that extends across the entire

package. Thus, Nicewarner does not have a through hole.

As such, it is clear that Nicewarner cannot be combined with Takashi to render the present invention obvious. The apparatus of the present invention requires that the CCD chip be mounted through the bottom opening of the package so as to allow the optical positioning adjusting device to view the surface of the CCD chip through the top opening during the mounting process. Clearly, this cannot be done in Nicewarner, because Nicewarner has no through hole. As such, it is respectfully submitted that Nicewarner teaches away from the present invention. For essentially the same reasons, Nicewarner is also incompatible with the device of Takashi.

The Court of Appeals for the Federal Circuit repeatedly has ruled that there must be some teaching or suggestion supporting the combination used in making the rejection. For example, In re Newell, 891 F.2d 899, 901 (Fed. Cir. 1989), the court held "[i]n deciding that a novel combination would have been obvious, there must be supporting teaching in the prior art." In Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), in finding obviousness, the court held "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combination; there must be some teaching suggestion, or incentive to make the combination made by the inventor." Finally, in In re Mills, 916 F.2d 680, 682 (Fed. Cir. 1990), the court held that although a prior art device "may be capable of being modified to run the way [the patent Applicants'] apparatus is claimed, there must be a

suggestion or motivation in the reference to do so" in order to establish obviousness.

Clearly, neither Takashi nor Nicewarner provide the necessary teaching to substantiate an obviousness rejection of the amended claims.

For all of the foregoing reasons, Applicants respectfully submit the present invention as recited by the amended claims is patentable over the combination of Takashi and Nicewarner.

IV. Summary

Having fully and completely responded to the Office Action, Applicants respectfully submit that the claims are in condition for allowance, an indication of which is respectfully solicited.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date:

12/21/98

By:



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Approved
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N/A

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Fig.9

PRIOR ART

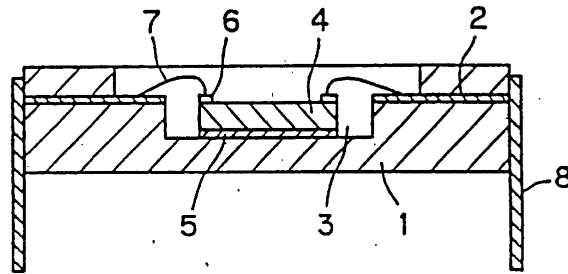


Fig.10

PRIOR ART

