



CERTIFICATION OF TRANSLATION

I, Matthew Francis, hereby declare:

1. I am a Japanese language translator.
2. I have over 10 years experience translating various document types from Japanese to English.
3. I certify that the English translation of the document identified below was translated by me and is a true and correct translation, to the best of my knowledge and ability, of the original Japanese content.

- H63-221667

I hereby certify under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this February 16th, 2016.

By: _____

A handwritten signature in black ink that reads 'M Francis'.

Matthew Francis

LANGUAGE AND TECHNOLOGY SOLUTIONS FOR GLOBAL BUSINESS

THREE PARK AVENUE, 39TH FLOOR, NEW YORK, NY 10016 | T 212.689.5555 | F 212.689.1059 | WWW.TRANSPERFECT.COM
OFFICES IN 90 CITIES WORLDWIDE

(19) Japanese Patent Office (JP)
(12) Unexamined Patent Application
(A)

(11) Publication No.
63-221667

(51) Int. Cl.⁴
H 01 L 27/14
H 04 N 5/335

Identification
Symbol(s)
JPO File Number(s)
D-7525-5F
V-8420-5C

(43) Date of Publication of Application:
September 14, 1988

Request for Examination: Not Requested Number of Inventions: 1 (Total 6 Pages)

(54) Title of Invention: Solid state imaging device

(21) Application No.: 62-54055
(22) Application: March 11, 1987

(72) Inventor: Akiya Izumi, C/O Hitachi, Ltd. Mobara Factory, 3300 Hayano, Mobara, Chiba Prefecture

(72) Inventor: Hisao Nakano, C/O Hitachi, Ltd. Mobara Factory, 3300 Hayano, Mobara, Chiba Prefecture

(72) Inventor: Masahiko Kadowaki, C/O Hitachi, Ltd. Mobara Factory, 3300 Hayano, Mobara, Chiba Prefecture

(71) Applicant: Hitachi, Ltd., 4-6 Surugadai, Chiyoda-ku, Tokyo

(71) Applicant: Hitachi Device Engineering Co., Ltd., 3681 Hayano, Mobara, Chiba Prefecture

(73) Representative: Patent Attorney Katsuo Ogawa and one other

Continued on final page

Specification

1. Title of Invention

Solid state imaging device

2. Claims

1. In the context of a solid state imaging device wherein a solid state imaging element chip is hermetically sealed within the cavity part of a package member, a solid state imaging device characterized in that a solid state imaging element chip is furnished in a hermetically sealed manner within a first cavity part formed by the aforementioned package member, and a peripheral circuit chip which forms the peripheral circuits of the aforementioned solid state imaging element chip is furnished sealed with a sealing material within a second cavity part formed independently of the first cavity part within the aforementioned package member.

2. The solid state imaging device described in Claim 1 characterized in that the aforementioned solid state imaging element chip is hermetically sealed within the first cavity part by a transparent glass cap.

3. The solid state imaging device described in Claim 1 or Claim 2 characterized in that the aforementioned peripheral circuit chip possesses a pre-amp circuit or a driver circuit, etc., and is sealed within the second cavity part by a resin sealing material

4. The solid state imaging device described in Claim 1 to Claim 3 respectively characterized in that the aforementioned package member is formed of ceramic or glass epoxy, etc.

3. Detailed Description of the Invention

[Field of Industrial Use]

The present invention relates to solid state imaging devices, and more particularly relates to a technique which may be usefully applied to solid state imaging devices wherein a solid state imaging element chip is hermetically sealed within the cavity part of a package member.

[Prior Art]

A solid state imaging device is formed through the hermetic sealing of a solid state imaging element chip within the cavity part of a package member.

A ceramic substrates (or resin substrate) is used for the package member. A solid state imaging element chip comprises a one dimensional or two dimensional photosensor.

A solid state imaging element chip is hermetically sealed within the aforementioned cavity part by a glass cap formed of a transparent glass substrate. This hermetically sealed solid state imaging element chip is connected to the leads of the package member through bonding wires.

In addition, solid state imaging devices are, for instance, described in "Image Information INDUSTRIAL," May 1986, published by Industrial Development Organization Ltd., p. 19 to 66, "Special Feature: Latest trends in solid state imaging elements and solid state cameras."

[Problems to be Solved by the Invention]

The inventors have developed a solid state imaging device with an internal pre-amp in order to increase the S/N ratio of the output signal of the aforementioned solid state imaging device. A construction is adopted such that by packaging a pre-amp in the same package as the solid state imaging element chip, the output signal may be amplified while minimizing the generated noise, and this amplified output signal output to an external amp. The pre-amp is comprised so as to be hermetically sealed within the same cavity part as the solid state imaging element chip.

However, it became clear to the inventors that this solid state imaging device would cause the following problems.

(1) Because the surface area inside the cavity part would increase, the mounting of a plurality of chips within the same cavity part would increase the probability that atmospheric debris and other contaminants that obstruct light would adhere within the cavity part. As a result, the aforementioned contaminants would be hermetically sealed together with the solid state imaging element chip, and the adherence of contaminants to the light receptive part of the solid state imaging element chip would cause that part to become substantially faulty, leading to a decrease in the yield of solid state imaging devices.

(2) Mounting a plurality of chips inside the same cavity part increases the number of bondings, which increases the probability that metal materials, coatings and other contaminants that obstruct light and which arise from the bonding process would be hermetically sealed together with the solid state imaging element chip. That is to say, in the same manner as the aforementioned (1), the yield of solid state imaging devices would decrease.

(3) Mounting a plurality of chips inside the same cavity part increases the sealed surface area of the cavity part, which increases the surface area of the glass cap. The glass cap is ordinarily formed of a high quality material in which there are no foreign objects larger than around 5 [μm], and so the cost of the solid state imaging devices would increase.

(4) In the case that a defect occurs in the peripheral circuit chip after the solid state imaging element chip and peripheral circuit chip are sealed inside the same cavity part, repair would be extremely difficult, and so it is essentially not possible to repair or replace the peripheral circuit chip. The cost of the solid state imaging element chip is 5 to 10 times higher in comparison with that of the peripheral circuit chip. As a result, the cost of the solid state imaging device would increase.

The purpose of the present invention is to provide a technique which allows the sensitivity of a solid state imaging device to be increased while reducing the noise of its output signal, and at the same time increasing the manufacturing yield of solid state imaging devices.

The aforementioned and other purposes of the present invention, together with its novel characteristics, will become clear from the text of the specification and the attached drawings.

[Means for Solving the Problems]

An outline of a representative example of the inventions disclosed within the present application is simply explained as follows.

In a solid state imaging device, a solid state imaging element chip is furnished in a hermetically sealed manner inside a first cavity part of a package member, and a peripheral circuit chip is furnished sealed with a sealing material inside a second cavity part which is formed independently of the first cavity part of the aforementioned package member.

[Operation of the Invention]

Through the above stated means, the probability that contaminants which obstruct light are hermetically sealed inside the first cavity part is able to be reduced, and thus the occurrence of defects in the light receiving part of the solid state imaging element chip is able to be reduced, and by internalizing the peripheral circuit chip, the noise in the output signal of the solid state imaging element chip is able to be reduced.

Below, an explanation of the construction of the present invention is given alongside embodiments wherein the present invention has been applied to a solid state imaging device which possesses a solid state imaging element chip with a two dimensional CCD photosensor.

In addition, within all drawings used to explain the embodiments, parts which have the same function are given the same reference numeral, and repeated explanation is omitted.

[Embodiment of the Invention I]

Embodiment I is an embodiment of the present invention wherein the present invention is applied to a solid state imaging device which has a package part formed of a ceramic material.

The schematic structure of the solid state imaging device which is Embodiment I of the present invention is shown in Figure 1 (a partially cut away perspective view).

As shown in Figure 1, the solid state imaging device is principally constructed of package member 1, first cavity part 1A, second cavity part 1B, solid state imaging element chip 2, peripheral circuit chip 3, peripheral circuit chips 4A to 4D, leads 5, glass cap 6 and resin sealing material 7.

The aforementioned package member 1 is comprised of a multi-layer ceramic substrate, and possesses a two layer wiring layer which is not shown in the drawing for this embodiment.

First cavity part 1A and second cavity part 1B are respectively constructed to form package member 1 in a concave shape. Solid state imaging element chip 2 is furnished within first cavity part 1A. Second cavity part 1B is furnished in a different position from and independently to first cavity part 1A, and peripheral circuit chips 3 and 4A to 4D are furnished within it.

Solid state imaging element chip 2 comprises a two dimensional photo sensor. That is to say, solid state imaging element chip 2 is principally comprised of light receiving part 2A wherein a plurality of photodiodes are arranged in a matrix form, horizontal shift register 2B and vertical shift register 2C. The bonding pads of the solid state imaging element chip 2, not shown in the drawing, are connected to the wiring of package member 1 through interposed bonding wires 8. This wiring is connected to leads 5 which are plurally arranged in DIP form on the sides of package member 1.

Solid state imaging element chip 2 is positioned within first cavity part 1A, and is hermetically sealed by the aforementioned glass cap 6. Glass cap 6 is formed for instance of transparent borosilicate glass. Glass cap 6 is bonded to package member 1 by for instance a bonding layer of epoxy resin adhesive, etc.

The aforementioned peripheral circuit chip 3 possesses a drive circuit which drives solid state imaging element chip 2. In the same manner as solid state imaging element chip 2, this peripheral circuit chip 3 is connected to leads 5 and solid state imaging element chip 2 through interposed bonding wires 8 and wiring.

Each of peripheral circuit chips 4A to 4D possesses a pre-amp circuit. The pre-amp circuits are constructed to amplify the output signal of solid state imaging element chip 2 to an appropriate degree, then output this amplified output signal to an external amp through leads 5. Peripheral circuit chips 4A to 4D are connected to leads 5 and solid state imaging element chip 2 through interposed bonding wires 8 and wiring.

Each of peripheral circuit chip 3 and peripheral circuit chips 4A to 4D which are furnished inside the aforementioned second cavity part 1B are hermetically sealed by resin sealing material 7. Resin sealing material 7 uses for instance polyimide resin or silicon rubber, and is applied through a potting process.

In this manner, solid state imaging element chip 2 is furnished in an air tight manner within first cavity part 1A of package member 1 of the solid state imaging device, and peripheral circuit chips 3 and 4A to 4D are furnished within second cavity part 1B which is formed independently of first cavity part 1A of the aforementioned package member 1 and are sealed by resin sealing material 7, such that the surface area of the inner surface of first cavity part 1A is able to be reduced, and the probability that contaminants (for instance, atmospheric debris) which obstruct light will be hermetically sealed within first cavity part 1A is able to be reduced, and thereby the occurrence of defects caused by the adhesion of the aforementioned contaminants to light receiving part 2A of solid state imaging element chip 2 is able to be reduced. Through this decrease in the occurrence of defects, the manufacturing yield of solid state imaging devices is able to be increased.

In addition, in the same manner, by positioning only solid state imaging element chip 2 within first cavity part 1A, the number of bondings is able to be decreased, and thereby the probability that metal materials, coatings and other contaminants that obstruct light and which arise from the bonding process are hermetically sealed together with solid state imaging element chip 2 is able to be decreased. Thus, in the same manner, the manufacturing yield of solid state imaging devices is able to be increased.

In addition, by reducing the sealed surface area of first cavity part 1A, the surface area of glass cap 6 is able to be decreased, and its cost is able to be decreased, and thus the cost of the solid state imaging device is able to be decreased.

Each of these effects is able to be achieved at the same time that noise in the output signal of solid state imaging element chip 2 is reduced through the internalization of peripheral circuit chips 4A to 4D.

In addition, as each of peripheral circuit chip 3 and peripheral circuit chips 4A to 4D are furnished within second cavity part 1B which is independent from first cavity part 1A, they are able to be repaired and replaced without decreasing the airtightness of first cavity part 1A. As a result, the cost of the solid state imaging device is able to be reduced.

[Embodiment of the Invention II]

Embodiment II is an another embodiment of the present invention wherein the present invention is applied to a solid state imaging device with a package member that is formed of a resin material.

The schematic structure of the solid state imaging device which is Embodiment II of the present invention is shown in Figure 2 (a sectional view).

As shown in Figure 2, the solid state imaging device is formed such that package member 1 is comprised of sealing base substrate 1C, and frame member 1D which forms each of first cavity part 1A and second cavity part 1B. Each of sealing base substrate 1C and frame member 1D is formed of a resin material such as glass epoxy resin.

In addition to the effects described in the aforementioned Embodiment I, a solid state imaging device constructed in this manner is able to be formed in a low cost manner as a result of package member 1 being formed of a resin material.

In addition, because sealed member 1 is formed of a resin material, the mechanical strength and degree of freedom of processing of package member 1 are increased, increasing the mounting area, and allowing the modularization of the solid state imaging device to be more readily achieved.

[Embodiment of the Invention III]

Embodiment III is another embodiment of the present invention which allows a lens mount to be attached to a solid state imaging device.

The schematic structure of the solid state imaging device which is Embodiment III is shown in Figure 3 (a sectional view).

As shown in Figure 3, the solid state imaging device is comprised such that lens mount 9 is able to be mounted on package member 1 on the upper part of solid state imaging element chip 2. Lens mount 9 is comprised of optical signal concentrating lenses 9A and 9B, support frame 9C which supports lenses 9A and 9B, positioning member 9D and mounting member 9E.

Support frame 9C is comprised such that positioning member 9D fits together with positioning hole 1E which is furnished to package member 1, and comprised such that it is attached to sealing member 1 by mounting member 9E at the position at which this fitting occurs. Mounting member 9E is comprised of, for instance, a bolt and nut.

The prescribed parts of sealing member 1 are furnished with leads 5A, and are comprised such that connector 10 may be attached. Connector 10 allows the connection of the solid state imaging device and an external device.

The above invention by the inventors has been specifically explained based on the aforementioned embodiments, but the present invention is not limited to the aforementioned embodiments, and it may naturally be changed in various manners to the extent that it does not deviate from its essence.

For instance, the present invention may also be comprised such that the solid state imaging element chip of the solid state imaging device is a one dimensional photosensor.

In addition, the present invention may also be furnished with a plurality of solid state image element chips in the solid state imaging device, with each of the solid state imaging element chips positioned in a separate cavity part.

In addition, the present invention may also internalize chips which contain volatile or non-volatile memory, or microchips, etc. within the solid state imaging device.

[Effects of the Invention]

A simple explanation of the effects yielded by a representative example of the inventions disclosed in the present application is given below.

Noise in the output signal of a solid state imaging device is able to be reduced and its sensitivity increased, while manufacturing yield is able to be increased.

In addition, the miniaturization of an imaging camera through modularization is also able to be readily achieved.

4. Brief Description of the Drawings

Figure 1 is a partially cut away perspective view which shows the schematic structure of a solid state imaging device which is Embodiment I of the present invention.

Figure 2 is a sectional view which shows the schematic structure of a solid state imaging device which is Embodiment II of the present invention.

Figure 3 is a sectional view which shows the schematic structure of a solid state imaging device which is Embodiment III of the present invention.

Within the drawings, reference numeral 1 ... package member; 1A ... first cavity part; 1B ... second cavity part; 2 ... solid state imaging element chip; 3, 4A to 4D ... peripheral circuit chips; 5 ... lead; 6 ... glass cap; 7 ... resin sealing material; 9 ... lens mount.

Representative Patent Attorney Katsuo Ogawa [seal: illegible]

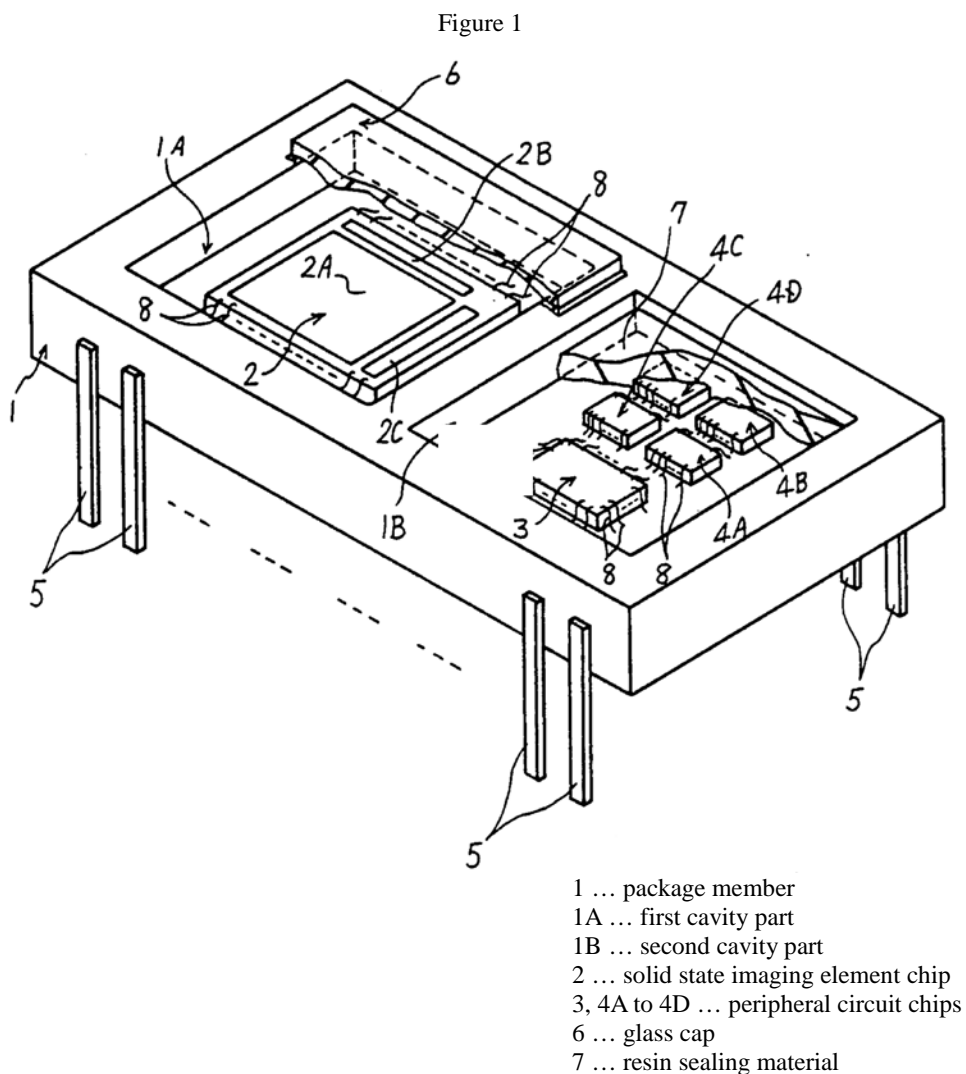


Figure 2

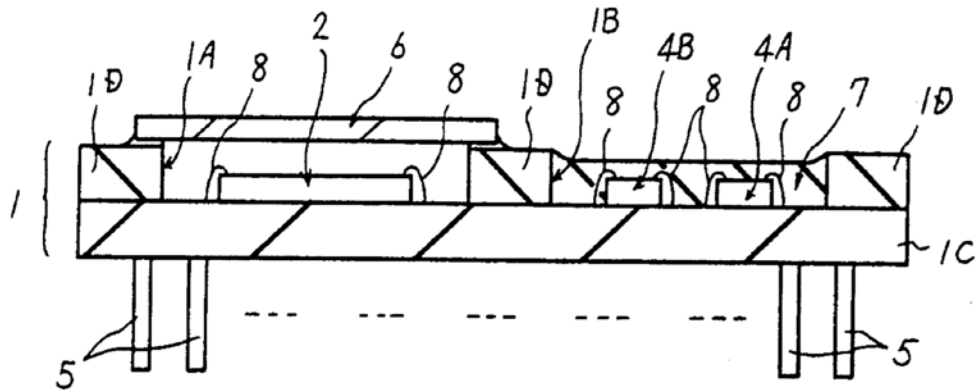
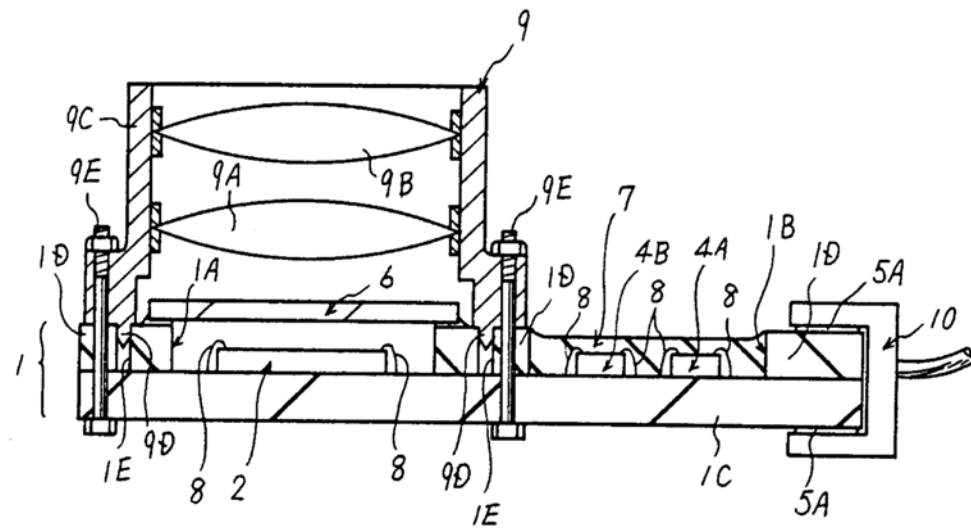


Figure 3



Continued from Page 1

(72) Inventor: Hideaki Abe, C/O Hitachi Device Engineering Co., Ltd., 3681 Hayano, Mohara, Chiba Prefecture

(72) Inventor: Minori Komota, C/O Hitachi, Ltd. Mobara Factory, 3300 Hayano, Mobara, Chiba Prefecture