



CERTIFICATION OF TRANSLATION

I, James Thornton, hereby declare:

1. I am a Japanese language translator.
2. I have over 15 years' experience translating various document types from Japanese to English.
3. I certify that the English translation of the document identified below was translated by me and is a true and correct translation, to the best of my knowledge and ability, of the original Japanese content.

- H5-275611

I hereby certify under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this 16th February 2016.

By: _____

A handwritten signature in black ink, appearing to read 'J. Thornton', written over a horizontal line.

James Thornton

LANGUAGE AND TECHNOLOGY SOLUTIONS FOR GLOBAL BUSINESS

THREE PARK AVENUE, 39TH FLOOR, NEW YORK, NY 10016 | T 212.689.5555 | F 212.689.1059 | WWW.TRANSPERFECT.COM

OFFICES IN 90 CITIES WORLDWIDE

(19) Japan Patent Office (JP)

(12) **Japanese Unexamined Patent
Application Publication** (A)

(11) Japanese Unexamined Patent
Application Publication Number

H5-275611

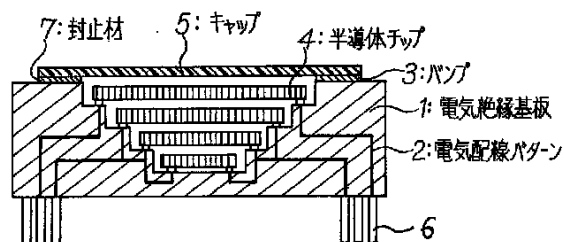
(43) Publication date October 22nd 1993

(51) Int. Cl.-	Identification codes	JPO file number	FI	Technical indications
H01L 25/065 25/07 25/18 21/60	311 S	6918-4M	H01L 25/ 08	Z
Request for examination Not yet requested Number of claims 2 (Total of 4 pages)				
(21) Application number	Japanese Patent Application H4- 74085	(71) Applicant	000004237 NEC CORPORATION SHIBA 5-7-1, MINATO-KU, TOKYO	
(22) Date of application	MARCH 30TH 1992	(72) Inventor	KOJI TOBASE % NEC CORPORATION SHIBA 5-7-1, MINATO-KU, TOKYO	
		(74) Agent	Patent attorney YOSUKE GOTO (and 2 others)	

(54) [TITLE OF THE INVENTION] MULTI-CHIP MODULE

(57) [ABSTRACT]

[PURPOSE] In a for example flip-chip-connected multi-chip module, to achieve high-speed operation of the multi-chip by increasing mounting density and shortening electrical interconnector path lengths to shorten signal propagation time.
[CONFIGURATION] In a multi-chip module wherein multiple semiconductor chips 4 are received and the semiconductor chips are electrically connected by bumps 3 to an electrically insulating substrate 1 having a predetermined electrical interconnector pattern 2, multiple steps of recess are formed in the electrically insulating substrate 1 and the semiconductor chips 4 are accommodated apart from each other in the vertical direction in the recesses.



[Scope of Patent Claims]

[Claim 1] In a multi-chip module wherein multiple semiconductor chips are received and the semiconductor chips are electrically connected by bumps to an electrically insulating substrate having a predetermined electrical interconnector pattern, a multi-chip module characterized in that multiple steps of recess are formed in the electrically insulating substrate and the semiconductor chips are accommodated apart from each other in the vertical direction in the recesses.

[Claim 2] A multi-chip module according to Claim 1, characterized in that in a recess formed in the electrically insulating substrate, a plurality of single-step and/or multiple-step recesses are formed in the horizontal direction to form multiple steps of recess, and the semiconductor chips are accommodated in these recesses.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Use] This invention relates to a semiconductor device and in particular relates to a structure of a multi-chip module in which are received multiple semiconductor chips.

[0002]

[Prior Art] In a multi-chip module of prior art, as shown in sectional view in Fig. 5, multiple semiconductor chips 4 are received on the same face of an electrically insulating substrate having an electrical interconnector pattern (not shown in the figure), the electrically insulating substrate 1 and the semiconductor chips 4 are electrically connected by fine metal wires 10, and the electrical interconnector pattern of the electrically insulating substrate 1 is electrically connected by external leads 6.

[0003] With this prior art construction, for example if it is a multi-chip module comprising one CPU (Central Processing Unit), one FPU (Floating Processing Unit), one BIU (Bus Interface Unit), and six cache memories, or nine semiconductor chips in total, the size of the electrically insulating substrate is about 85mm square.

[Problems the Invention Seeks to Solve] Now, in this multi-chip module of prior art, because the semiconductor chips 4 are only received on the same face of the electrically insulating substrate 1, as the number of semiconductor chips received increases, the size of the electrically insulating substrate must also increase, and consequently the path length of the electrical interconnectors becomes long.

[0005] When the path length of the electrical interconnectors becomes long like this, the capacitance that the interconnectors have becomes large, and the signal propagation delay time becomes large. Consequently, there has been the problem that when the multi-chip module is operated at high speed, the signal ceases to return within a single clock time, and the multi-chip module will not operate at high speed.

[0006] This problem is an extremely serious problem, and there has been the problem that whereas the faster the device operates the more the signal processing speed increases, high-speed operation has not been possible.

[0007] This invention has been proposed in view of this kind of problem with the prior art, and has the purpose of, in for example a flip-chip-connected multi-chip module, increasing

the mounting density and shortening the path length of the electrical interconnectors, and thereby eliminating the shortcomings of the prior art described above.

[0008]

[Means for Solving the Problem] With this invention there can be obtained, in a multi-chip module wherein multiple semiconductor chips are received and the semiconductor chips are electrically connected by bumps to an electrically insulating substrate having a predetermined electrical interconnector pattern, a multi-chip module characterized in that multiple steps of recess are formed in the electrically insulating substrate and the semiconductor chips are accommodated apart from each other in the vertical direction in the recesses.

[0009]

[Embodiment Example] First, a multi-chip module of a first embodiment example of the invention will be described. As shown in Fig. 1, semiconductor chips 4 are severally received multi-step-wise in the vertical direction, apart from and parallel with each other, in multiple steps of recess provided in an electrically insulating substrate 1 having an electrical interconnector pattern 2. Bumps 3 are formed on the steps where the semiconductor chips 4 are disposed. The semiconductor chips 4 are disposed on these bumps 3, and the semiconductor chips are connected as necessary to each other or to external leads 6 by the electrical interconnector pattern 2.

[0010] In this case, as the semiconductor chips 4, the mounting of chip capacitors or the like is possible. In the figures, 5 is a cap and 7 is a seal.

[0011] Next, a multi-chip module of a second embodiment example of the invention will be described. The multi-chip module of the second embodiment example, as shown in Fig. 2, is one in which semiconductor chip mounting recesses are formed so as to line up semiconductor chips 4 in the horizontal direction as well. Needless to say, the disposition of the semiconductor chips 4 and their number in not only the vertical direction but also in the horizontal direction is not limited to what is shown in the figure.

[0012] Whereas with the disposition of semiconductor chips 4 of the first embodiment example the sizes of the semiconductor chips must increase with progress upward and it is not possible to mount semiconductor chips 4 of the same size on the same substrate, when the arrangement of this second embodiment example is adopted it becomes possible to accommodate semiconductor chips 4 of various sizes.

[0013] Next, some cases of mounting a heat sink to a multi-chip module of the invention will be described. Fig. 3 is a sectional view of a case where a heat sink 9 has been mounted on the multi-chip module of the first embodiment example. Here, a highly heat-producing semiconductor chip is connected at the top, and the semiconductor chip and the heat sink 9 are bonded together with a high-conductivity adhesive 8.

[0014] Fig. 4 is a sectional view of a case where a heat sink 9 has been mounted on the multi-chip module of the second embodiment example. When multiple highly heat-producing semiconductor chips are to be accommodated, by connecting these multiple semiconductor chips in the uppermost recesses in an electrically insulating substrate as shown in this

embodiment example, it becomes possible to bond heat sinks to multiple semiconductor chips.

[0015] Now, as the material of the electrically insulating substrate 1, although an alumina substrate or a glass-epoxy substrate or the like has conventionally been used, from the point of view of the reliability of the flip chip mounting, the use of a substrate with the trade name Ceracom Substrate, marketed by Ibiden Co., Ltd., which has been made compatible in thermal expansivity with the semiconductor chip, is preferable.

[0016] As a flip chip mounting evaluation result obtained with Ceracom Substrate, the result has been obtained that no connection breakage occurs for 1000 cycles in a 125° ~ -65° thermal cycle test.

[0017] With the embodiment examples of the invention described above, an electrically insulating substrate which in the prior art needs to have a size of about 85mm square can be reduced in size to about 50mm square.

[0018]

[Effect of the Invention] As described above, with this invention there is the effect that by semiconductor chips being received and connected apart from and parallel with each other in the vertical direction in multiple steps of recess provided in an electrically insulating substrate having an electrical interconnector pattern, without any limitation due to the sizes or the number of the mounted semiconductor chips being suffered, the electrically insulating substrate can be made

small, the mounting density can be increased and the interconnector path lengths of the electrical interconnectors can be shortened and the signal propagation time thereby shortened, and high-speed operation of the multi-chip module thereby made possible.

[Brief Description of the Drawings]

[Fig. 1] A sectional view showing a first embodiment example of the invention.

[Fig. 2] A sectional view showing a second embodiment example of the invention.

[Fig. 3] A sectional view of a case where a heat sink has been mounted on the first embodiment example of the invention.

[Fig. 4] A sectional view of a case where a heat sink has been mounted on the second embodiment example of the invention.

[Fig. 5] A sectional view showing a multi-chip module with a heat sink, of prior art.

[Explanation of the Symbols]

1 electrically insulating substrate

2 electrical interconnector pattern

3 bump

4 semiconductor chip

5 cap

6 external leads

7 seal

8 high-conductivity adhesive

9 heat sink

10 fine metal wire

Fig. 1

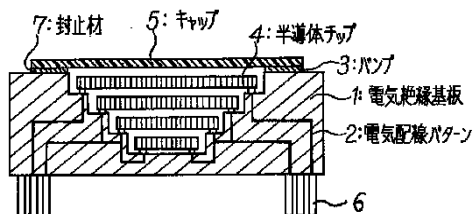


Fig. 2

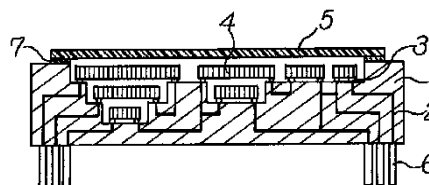


Fig. 3

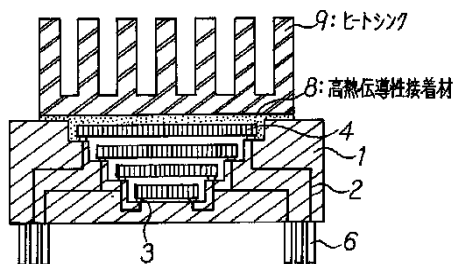


Fig. 4

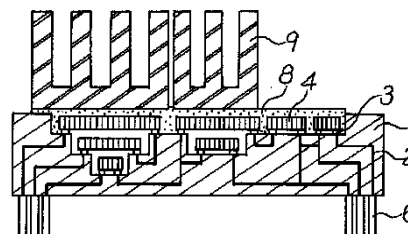


Fig. 5

