Paper No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

Sony Corporation

Petitioner
v.

Collabo Innovations, Inc.

(record) Patent Owner

Patent No. 5,952,714

PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 ET. SEQ

TABLE OF CONTENTS

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 5,952,714 ("the '714 patent").
1002	Declaration of R. Michael Guidash.
1003	Certified translation of Japanese Unexamined Patent Application Publication No. S61-131690 ("Yoshino").
1004	Certified translation of Japanese Unexamined Patent Application Publication No. H07-045803 ("Wakabayashi").
1005	Certified translation of Japanese Unexamined Patent Application Publication No. S59-225560 ("Hikosaka").
1006	Japanese Unexamined Patent Application Publication No. S61-131690, published June 19, 1986.
1007	Japanese Unexamined Patent Application Publication No. H07-045803, published Feb. 14, 1995.
1008	Japanese Unexamined Patent Application Publication No. S59-225560, published December 18, 1984.
1009	Non-Final Office Action dated July 20, 1998, in file history of U.S. Pat. App. No. 08/809,845.
1010	Amendment dated December 21, 1998, in file history of U.S. Pat. App. No. 08/809,845.
1011	Certified translation of Japanese Unexamined Patent Application Publication No. H07-78951 ("Nita").
1012	Excerpt from Charles A. Harper & Martin B. Miller, Electronic Packaging, Microelectronics, and Interconnection Dictionary (1993).
1013	Japanese Unexamined Patent Application Publication No. H05-

	275611, published Oct. 22, 1993.
1014	Certified translation of Japanese Unexamined Patent Application Publication No. H05-006989 (“Onishi”).
1015	Japanese Unexamined Patent Application Publication No. H05-006989, published Jan. 14, 1993.
1016	Certified translation of Japanese Unexamined Patent Application Publication No. S63-221667 (“Izumi”).
1017	Japanese Unexamined Patent Application Publication No. S63-221667, published Sept. 14, 1998.
1018	Certified translation of Japanese Unexamined Patent Application Publication No. H06-029507 (“Nagano”).
1019	Japanese Unexamined Patent Application Publication No. H06-029507, published Feb. 4, 1994.
1020	Certified translation of Japanese Unexamined Patent Application Publication No. S60-74880 (“Hirosawa”).
1021	Japanese Unexamined Patent Application Publication No. S60-74880, published April 25, 1985.
1022	Certified translation of Japanese Unexamined Patent Application Publication No. H05-275611 (“Tobase”).
1023	Japanese Unexamined Patent Application Publication No. H07-78951.
1024	Certified translation of Japanese Unexamined Patent Application Publication No. H06-85221 (“Fujii”).
1025	Japanese Unexamined Patent Application Publication No. H06-85221, published March 25, 1994.
1026	CV of R. Michael Guidash.

NOTICE OF LEAD AND BACKUP COUNSEL

Lead Counsel: Matthew A. Smith (Reg. No. 49,003); Tel: 650.265.6109

Backup Counsel: Zhuanjia Gu (Reg. No. 51,758); Tel: 650.529.4752

Address of lead counsel: Turner Boyd LLP, 702 Marshall St., Ste. 640

Redwood City, CA 94063. FAX: 650.521.5931.

NOTICE OF THE REAL-PARTIES-IN-INTEREST

The real-parties-in-interest for this petition are Sony Corporation, Sony Corporation of America, and Sony Electronics Inc.

NOTICE OF RELATED MATTERS

U.S. Patent No. 5,952,714 ("the '714 patent") has been asserted in *Collabo Innovations, Inc. v. Sony Corporation, et al.*, Case No. 1-15-cv-01094 (D. Del.), which was filed on November 25, 2015, and first served (on Sony Electronics Inc.) on February 22, 2016.

NOTICE OF SERVICE INFORMATION

Please address all correspondence to the lead counsel at the addresses shown above. Petitioners consent to electronic service by email at: smith@turnerboyd.com, docketing@turnerboyd.com, and gu@turnerboyd.com, zweig@turnerboyd.com

GROUNDS FOR STANDING

Petitioner hereby certifies that the patent for which review is sought is available for *inter partes* review, and that the Petitioner is not barred or estopped from

requesting an *inter partes* review on the grounds identified in the petition.

STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner respectfully requests that claims 1-13 and 15-16 of U.S. Patent No. 5,952,714 ("the '714 patent")(Ex. 1001) be canceled based on the grounds below. Grounds 1-11, directed to claims 1, 6-13, and 15-16, are based on the Yoshino reference. Grounds 12-15, directed to claims 1-5 and 13, relate to the Wakabayashi reference. These are the two base references. Fifteen grounds are necessary because the '714 patent claims numerous combinations of secondary features to its primary apparatus (claim 1) and primary method (claim 13).

Ground 1: Claim 1 is anticipated by Japanese Pat. App. Pub. No. S61-131690 ("Yoshino").

Ground 2: Claim 6 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. S63-221667 ("Izumi").

Ground 3: Claim 7 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. H06-029507 ("Nagano"), in further view of Japanese Pat. App. Pub. No. H07-045803 ("Wakabayashi").

Ground 4: Claim 8 is obvious over Yoshino in view of Izumi or Nagano, in further view of Japanese Pat. App. Pub. No. S60-74880 ("Hirosawa") and Japanese Pat. App. Pub. No. H07-78951 ("Nita").

Ground 5: Claim 9 is obvious over Yoshino in view of Izumi or Nagano.

Ground 6: Claim 10 is obvious over Yoshino in view of Izumi or Nagano, in further view of Wakabayashi.

Ground 7: Claim 11 is obvious over Yoshino in view of Izumi or Nagano, in further view of Japanese Pat. App. Pub. No. H05-006989 ("Onishi").

Ground 8: Claim 12 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. H05-275611 ("Tobase").

Ground 9: Claim 13 is obvious over Yoshino in view of Japanese Pat. App. Pub. No. S59-225560 ("Hikosaka").

Ground 10: Claim 15 is obvious over Yoshino in view of Izumi and Nagano, in further view of Hikosaka.

Ground 11: Claim 16 is obvious over Yoshino in view of Tobase, in further view of Hikosaka.

Ground 12: Claim 1 is obvious over Wakabayashi.

Ground 13: Claims 2-4 are obvious over Wakabayashi, in view of Japanese Pat. App. Pub. No. H06-85221 ("Fujii").

Ground 14: Claim 5 is obvious over Wakabayashi in view of Fujii, in further view of Onishi.

Ground 15: Claim 13 is obvious over Wakabayashi in view of Hikosaka.

THRESHOLD REQUIREMENT FOR INTER PARTES REVIEW

This petition presents "a reasonable likelihood that the Petitioners would prevail

with respect to at least one of the claims challenged in the petition", 35 U.S.C. § 314(a), as shown in the Grounds explained below.

I. INTRODUCTION TO THE SUBJECT MATTER

The '714 patent relates to a package for a semiconductor image sensor. An image sensor is a component that converts light into an electric signal. The electric signal is generated by semiconductor elements that make up the image sensor. Image sensors are used in a variety of optical and image capture devices, such as digital cameras, digital scanners, and copiers. (Ex. 1002, ¶38).

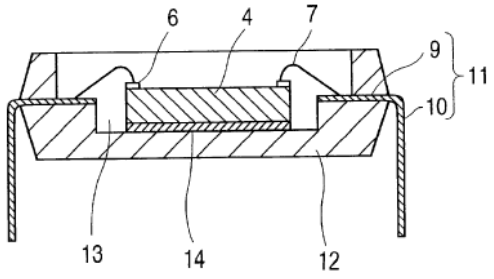
An image sensor, like other semiconductor devices ("chips"), is often contained in a housing. This housing is called a "package". The package protects the chip and provides electrical connections to external circuits. (Ex. 1002, ¶39).

Packages come in many varieties. Some include special features appropriate for the type of chip. A package for an image sensor, for example, must have an opening (typically covered with a transparent window) to allow light to strike the image sensor chip. The light should strike the photosensitive portions of the chip in an unobstructed manner and be aligned with the optical system of the image capture device so that accurate image capture of the scene associated with the light incident on the chip is accomplished. This requirement means that an image sensor must be positioned in its package within certain tolerances. Positioning is often accomplished optically, *i.e.*, using measurements taken by an optical device,

such as a video camera. (Ex. 1002, ¶¶40-42).

The process of aligning and securing a chip in a package is called "mounting". One method of mounting an image sensor is described in the Admitted Prior Art of the '714 patent. (Figs. 9-10)(Ex. 1001, 1:42-61). The Admitted Prior Art describes how an image sensor is mounted by "die bonding". "Die bonding" refers to the act of affixing the back side of a semiconductor chip (a "die") to a substrate (*e.g.*, the base of a package). When a chip is die-bonded with its backside down, the chip's upper surface or front side is exposed. This upper or front-side surface is designed to have metal interconnections along its edges with "pads" (electrical contacts). These pads are shown in Fig. 10 of the '714 patent (at right), where chip (4) has pads (6). These pads (6) are connected, using wires (7), to flat metallic strips (9 and 10), called "leads".

FIG. 10
PRIOR ART



The leads have two parts: inner leads (9) and outer leads (10). "Inner leads" connect to the pads of the sensor and are located inside of the package. The inner leads run into "outer leads", which in turn project out of the package to allow connection to external circuitry. (Ex. 1001, 1:53-61)(Ex. 1002, ¶¶43-45).

The use of wire bonding (wires 7) in the package of Fig. 10 has several problems. First, wire bonding limits how small the package can be, because the

wires require both horizontal and vertical space to make the connection between the pad (6) and inner lead (9). Second, wire bonds are costly, due to the materials used and the processing time required, and are complex, because wires have to be carefully placed and bonded to pads (6) and leads (9). Third, wire bonds can cause unwanted reflections of light onto the image sensor. (Ex. 1002, ¶46).

To alleviate the problems of wire bonding, another mounting method was developed. In this method, the inner leads are extended and coated with an amount of conductive material, called a "bump". Such bumps are then press bonded or melted directly onto the contact pads of the chip, skipping the intermediate wires (7) and saving space and manufacturing time. (Ex. 1002, ¶47).

The '714 patent describes similar, known bonding and optical positioning processes for mounting an image sensor. The '714 patent's package is shown below. In Fig. 1 (cutaway) and Fig. 2 (cross-section), a solid-state image sensor (27) is mounted in a package (21). (Ex. 1001, 4:49-63)(Ex. 1002, ¶48).

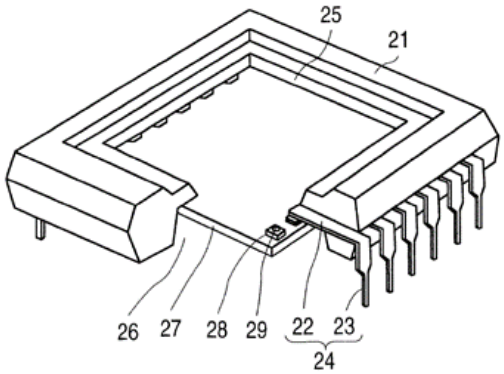


Fig. 1

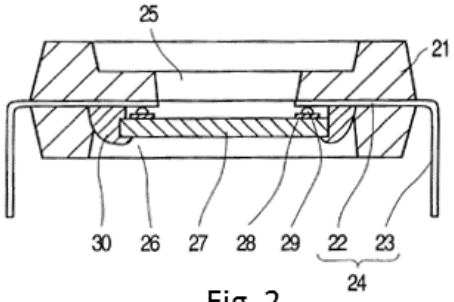


Fig. 2

As one would expect, the package 21 allows light to reach the light-detecting

upper or front-side surface of the image sensor, by providing an opening (25). The opening extends through the package's center, creating a "through hole". (Ex. 1001, 4:53-58). The back side of this through-hole (specifically "inlet 26" in Fig. 1) is the access point for inserting the sensor into the package. Once inserted, the sensor is electrically connected to the leads 22 (part of "lead frame (24)"), and secured with adhesive (30). (Ex. 1001, 5:9-22). This overall arrangement allows light to enter from the top through opening 25 and reach the sensor's upper surface. (*See* Ex. 1001, 7:26-32, 8:43-45, Figs. 7 and 8)(Ex. 1002, ¶¶49-51).

II. CLAIMS OF THE '714 PATENT

Such a package is reflected in independent claim 1 of the '714 patent, below:

> "1. A solid-state image sensing apparatus comprising:
>
> a package having a **through hole** therein, openings on both end faces thereof, and different opening areas of said openings,
>
> a lead frame comprising **inner leads and outer leads**, said lead frame being sealed in said package, and
>
> a **solid-state image sensing device** mounted in said package by being **inserted from an inlet of said opening which has a wider area**, and thereby sealing said through hole,
>
> said solid-state image sensing device being secured to said package via an **adhesive**."

Thus, in claim 1, there is an image sensor mounted in a package. The package has inner and outer leads, and a through hole with two openings. The wider of the

two openings (in Fig. 1, the bottom opening) is used to insert the sensor into the package, thus sealing the through hole. The sensor is then secured by an adhesive (*i.e.* glued) into the package. (Ex. 1002, ¶¶63-64).

The remaining claims add various minor features that will be addressed below.

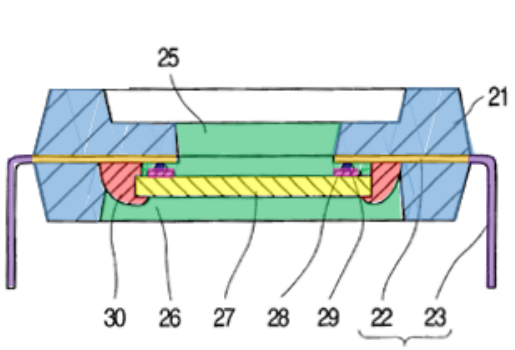
III. INTRODUCTION TO THE PRIOR ART

The concepts of claim 1 are disclosed in Japanese Pat. App. Pub. No. S61-131690 ("**Yoshino**") (Ex. 1003 and Ex. 1006), and Japanese Pat. App. Pub. No. H07-045803 ("**Wakabayashi**") (Ex. 1004 and Ex. 1007). **Yoshino** is the basic reference in Grounds 1-11 against claims 1, 6-13, and 15-16. **Wakabayashi** is asserted in Grounds 12-15 against claims 1-5 and 13. Fifteen grounds are necessary because the '714 patent claims numerous combinations of secondary features, so this petition refers back to common analyses where appropriate to avoid repetition.

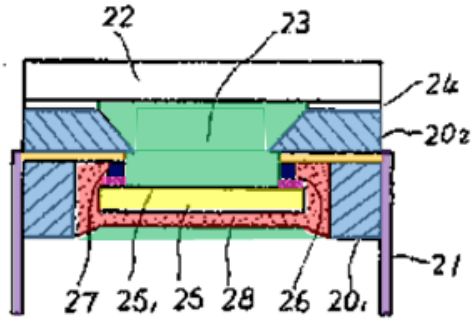
A. Overview of Yoshino

Like the '714 patent, Yoshino discloses a package for a solid-state image sensing device, where the device is mounted in a through hole and bonded to inner leads. (Ex. 1003, p. 002). To illustrate this, Petitioner has highlighted like elements of the '714 patent's Fig. 2 (left side) and Yoshino's Fig. 1 (right side) below. Like claim 1 of the '714 patent, Yoshino teaches a package ("packaging substrate (20)", highlighted light blue) with a through hole ("opening (23)", green),

itself having openings at the top and bottom ends having different areas. (Ex. 1003, p. 003).



'714 patent Fig. 2



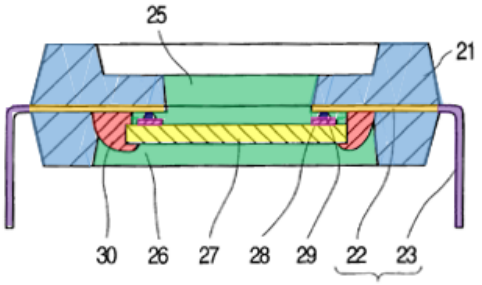
Yoshino Fig. 1

Sealed in the package is a lead frame ("electrode leads (21)") comprising an inner lead (orange) and outer lead (purple). (Ex. 1003, p. 003). A solid-state image sensing device ("image sensor (25)", yellow) is mounted and secured using an adhesive ("molded resin (28)", red). (Ex. 1003, p. 003). Yoshino also discloses elements of other claims, *e.g.*, connecting an electrode pad ("bonding pads (26)", pink) of the image sensor to the inner lead via a bump ("conductive bonding material (27)", dark blue). (Ex. 1003, p. 003)(Ex. 1002, ¶¶66-70).

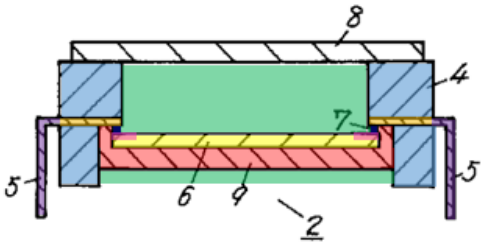
B. Overview of Wakabayashi

Wakabayashi also discloses the basic elements of the '714 patent. Like claim 1, Wakabayashi discloses a package in which a solid-state image sensing device is mounted in the package's through hole, directly bonded to the inner lead, and secured with an adhesive. (Ex. 1004, Abstract, Figs. 1 and 2). Below, Petitioner has highlighted like elements of the '714 patent's Fig. 2 (left) and Wakabayashi's

Fig. 2 (right). Wakabayashi discloses "package 4" (highlighted light blue) having a through hole (green) with different opening areas at its top and bottom end faces. (Ex. 1004, Abstract, ¶0005, ¶0010). Wakabayashi discloses a lead frame ("lead frame" or "leads 5") having an inner lead (orange) and outer lead (purple). (Ex. 1004, Abstract, Claim 1, ¶0010, Fig. 2). Wakabayashi discloses mounting a solid-state image sensor ("CCD chip 6", yellow), in the package, sealing the hole, using an adhesive ("adhesive resin 7", red, labeled "9" in Fig. 2). (Ex. 1004, ¶0007; ¶0010; ¶0015, Fig. 2)(Ex. 1002, ¶¶71-74).



'714 patent Fig. 2



Wakabayashi Fig. 2

C. Relevant Prosecution History of the '714 patent

During prosecution, the Examiner rejected all the original claims under § 103(a) as obvious over Wakabayashi (which the examiner called "Takashi"), or over Wakabayashi in view of U.S. Pat. No. 5,327,325. (Ex. 1009, p. 003). These rejections were withdrawn after the applicants amended the claims to require that the image sensor is secured via an adhesive, and (for certain claims) "simultaneously adjusting the optical positioning of said solid-state image sensing device". (Ex. 1010, pp. 1-10). The applicants argued (incorrectly) that

Wakabayashi did not disclose an adhesive, and that Wakabayashi's connection of the image sensor via "bumps ... for example, by a reflow solder process" did not allow for precise positioning. (*Id.*, p. 12). The Examiner allowed the claims, apparently accepting these arguments.

The applicants' arguments for patentability were, however, incorrect. First, Wakabayashi *does* disclose securing the image sensor with an adhesive. (Ex. 1004, ¶0015; *see also* Fig. 2). Second, Wakabayashi does not require a "solder reflow process", nor do the claims exclude one. Third, those claims requiring simultaneous positioning would have been obvious. Simultaneous optical positioning was a commonly used process for manufacturing image sensors, as explained in Grounds 9 and 15, below. (Ex. 1002, ¶¶212-228; ¶¶299-300).

IV. CLAIM CONSTRUCTION

The '714 patent will expire on July 30, 2016. For an expired patent, the PTAB gives claims "their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record". *See Cisco Systems, Inc. v. AIP Acquisition, LLC*, Case No. IPR2014-00247, Paper 20 at pp. 2-3 (PTAB July 10, 2014).

A. Claim 2—"solid-state image apparatus"

All the claims disclose a "solid-state image sensing apparatus" other than claim

2, which discloses a "solid-state image apparatus". The omission of the word "sensing" in claim 2 has no apparent impact on the meaning of the term. (Ex. 1002, ¶¶77-80).

B. Claims 2-7, 9-11, 13-16—"electrode pad(s)"

The '714 patent does not expressly define "electrode pad(s)", which the specification also refers to as an "electrode". (Ex. 1001, 4:62-63). The specification and claims of the '714 patent indicate that an "electrode pad" is an electrical connection point on a "solid-state image sensing device", "peripheral circuit chip", or "substrate". (*E.g.*, Ex. 1001, 5:6-7; 6:7-9; 10:64-65). The "electrode pad(s)" electrically connect the device or substrate to conductive elements in the package—*i.e.*, the inner lead of the "lead frame" or, in the Admitted Prior Art, a "metallized conductor". (*E.g.*, Ex. 1001, 3:6-10; 3:23-26; 3:53-63; 10:64-66). Thus, "electrode pad(s)" should be construed as "an electrical connection point on a substrate or semiconductor device." (Ex. 1002, ¶¶81-84).

C. Claims 3, 9, 13-16—"bump"

The '714 patent does not expressly define the term "bump". It does, however, indicate that a "bump" is a means by which the pads of the image sensor, peripheral chip, or substrate are electrically connected to a lead. (*E.g.*, Ex. 1001, 3:6-10; 3:23-26; 3:53-63; 10:64-66). One of ordinary skill would thus have understood a "bump" to indicate an amount of conductive material used for

electrically connecting the device, using a number of different methods. (Ex. 1002, ¶85). This is consistent with Harper's definition:

> Bump: "A small metal mound or hump that is formed on the chip or the substrate bonding pad and is used as a contact in face-bonding. It is a means of providing connections to terminal areas of a device." (Ex. 1012, p. 23)(Ex. 1002, ¶85).

Thus, "bump" should be construed as "an amount of conductive material used for an electrical connection." (Ex. 1002, ¶86).

D. Claim 8—"covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device"

When properly interpreted, the term "covers" in claim 8 does not require that the shading film is located *on* the substrate. Rather, it indicates that the film *provides shade* for "an entire upper surface of said substrate except an upper surface of the solid-state image sensing device". This is to protect peripheral circuit elements located on the shaded portion from light. (Ex. 1002, ¶87).

Thus, the shading film could be *on* the substrate, or it could be *above* the substrate. This is made clear by the only embodiment (depicted in Fig. 7) that features such a film, in which "shading film 48" is not *on* but *above* the "substrate 42", on the package's glass cover ("glass substrate 49"). (Ex. 1001, 6:57-62; 7:26-32; *see also* Fig. 7). Furthermore claim 8 (the only claim reciting a shading film) is multiply dependent from claim 6 or 7. Claim 6 features an image sensor and

peripheral chip mounted on a substrate. (Ex. 1001, 9:65-66). If the term "covers" required that the shading film be *on* the substrate, then in this case the film would not actually cover the peripheral chip. Thus, this phrase should be construed as requiring that the shading film is located on or above the entire upper surface of the substrate except for the portion of the substrate on which the solid-state image sensing device is disposed. (Ex. 1002, ¶88-90).

E. Claim 7—"plastic package"

Claim 7 recites both a "package", and (later) a "plastic package". Because there is no embodiment with two packages, Petitioners submit that the term "plastic package" refers back to the earlier recitation of the term "package". (*See, e.g.*, Ex. 1001, Fig. 5). Thus, "plastic package" in claim 7 should be construed to refer to the earlier use of the term "package", which is a shorthand reference for "plastic package". (Ex. 1002, ¶¶91-92).

F. Claim 15—"substrate"/"semiconductor substrate"

Claim 15 recites mounting an image sensor and peripheral chip on "a substrate", then "inserting the **semiconductor** substrate". (Ex. 1001, 11:36-12:9). As with "package" and "plastic package" in claim 7, Petitioner submits that "semiconductor substrate" refers back to "substrate", which is a reference for "semiconductor substrate". (*See* Ex. 1001, 6:29-7:2, Figs. 6 and 7)(Ex. 1002, ¶¶93-95).

V. DETAILED EXPLANATION OF THE REASONS FOR UNPATENTABILITY

Ground 1. Claim 1 is anticipated by Yoshino.

Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 102(b) over Japanese Pat. App. Pub. No. S61-131690 ("Yoshino") (Ex. 1003 and Ex. 1006)(Ex. 1002, ¶96). Yoshino was published on June 19, 1986, and is prior art under pre-AIA § 102(b). (Ex. 1006, cert. trans. as Ex. 1003). Yoshino is summarized in §III.A above.

As described above, Yoshino teaches a package with a through hole. (Ex. 1002, ¶97). The through hole allows an image sensor to be mounted from the back side of the package and bonded directly to inner leads, just like the '714 patent. (*Id.*). The following sections map claim limitations to the teachings of Yoshino, citing to the certified translation in Ex. 1003.

Claim 1. [1a]. "A solid-state image sensing apparatus comprising:"

Yoshino discloses an apparatus comprising a "solid-state" image sensing device—*i.e.*, **a solid-state image sensing apparatus**. Yoshino describes:

> "A solid-state image pickup device characterized by comprising a solid-state image sensor, a packaging substrate supporting said solid-state image sensor …." (Ex. 1003, p. 002, Claim 1)(Ex. 1002, ¶100).

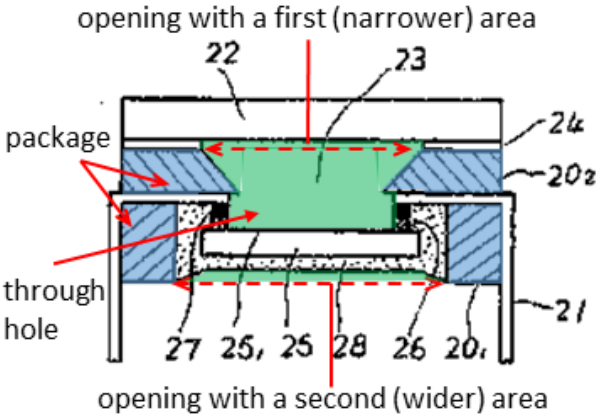
[1b] "a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,"

Yoshino discloses a **package having a through hole therein**. Yoshino states:

> "a **packaging substrate** supporting said solid-state image sensor and

> **having an opening** tapered so as to expand the edge ….” (Ex. 1003, p. 002, Claim 1)(emph. add.)(Ex. 1002, ¶101).

As shown in Yoshino’s Fig. 1 (at right with annotations by Petitioner), the through hole has **openings on both end faces thereof, and different opening areas of said opening**s. (Ex. 1002, ¶102).



The **openings** are essentially the same as those of the ’714 patent, even though Yoshino’s figure depicts the apparatus after one end is covered by “glass plate (22)” and the through hole is sealed by “molded resin (28)” (an adhesive, as disclosed in element [1d]). (Ex. 1003, p. 003)(Ex. 1002, ¶103). Specifically, the ’714 patent also describes that one opening may be covered by glass “protection panel 56”. (Ex. 1001, 8:43-48)(Ex. 1002, ¶103). The ’714 patent also requires that the second opening is sealed with an image sensor, followed by adhesive application. (*See* element [1d] below)(Ex. 1002, ¶103).

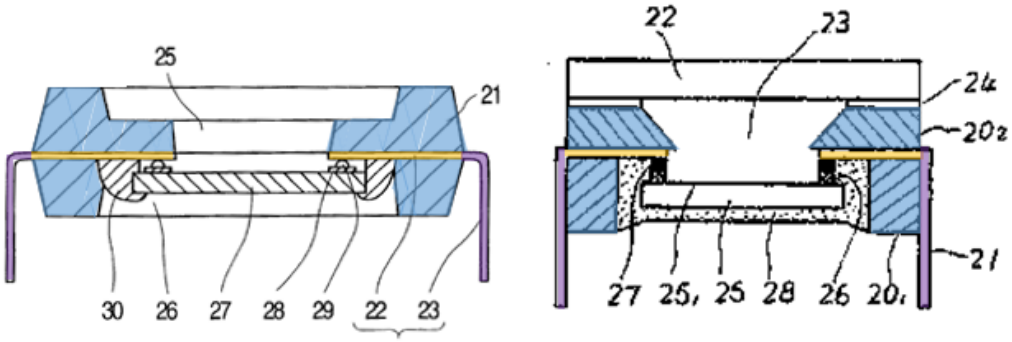
> ***[1c] “a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and”***

Yoshino discloses a **lead frame** (“electrode leads (21)”). Yoshino states:

> “The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and the bonding pads (26) and the electrode leads (21)

aligned therewith are connected…." (Ex. 1003, p. 003)(Ex. 1002, ¶104).

Yoshino's lead frame is nearly identical to that of the '714 patent. Below, Petitioner has highlighted the '714 patent's Fig. 2 (left side) and Yoshino's Fig. 1 (right side), to show that Yoshino teaches the same lead frame **comprising inner leads** (orange) **and outer leads** (purple), described in the '714 patent as "inner lead 22" and "outer lead 23" of "lead frame 24". (Ex. 1001, 4:52-53)(Ex. 1002, ¶105). Fig. 1 of Yoshino also shows that Yoshino's lead frame is **sealed in said package** (blue) in the same way as the '714 patent. (Ex. 1002, ¶105).



'714 patent Fig. 2 Yoshino Fig. 1

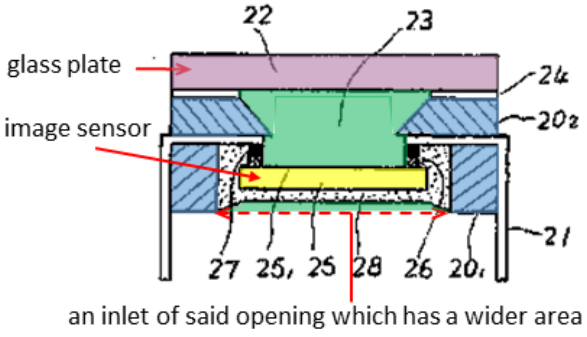
[1d] "a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive."

Yoshino discloses **a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area**. (Ex. 1002, ¶106). In the following passages, Yoshino recites that its image sensor is inserted *after* "light transmitting glass plate (22)" has been affixed to the

package. (Ex. 1002, ¶106). As shown in the Yoshino's Fig. 1 (annotated below), "light transmitting glass plate (22)" covers the narrower opening, so the image sensor must be inserted into the wider opening. (Ex. 1002, ¶107).

> "In this solid-state image pickup device, the packaging substrate (20) … is constructed … and the electrode leads (21) are provided …. The **light transmitting glass plate (22) is hermetically secured** to the ceramic molded frame (202) using black fritted glass **beforehand so as to cover the tapered opening (23) of the packaging substrate (20)**. The **solid-state image sensor (25) is placed** so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21) ….
>
> [N]o heating is required in the step **of incorporating the solid-state image sensor (25) into the packaging substrate (20)** to which the **light transmitting glass plate (22) has already been hermetically bonded**." (Ex. 1003, p. 003)(emph. add.)(Ex. 1002, ¶107).

Petitioner has annotated Yoshino's Fig. 1 below to show the glass plate (highlighted purple) and the image sensor (yellow) inserted into the wider opening of the through hole (green) of the package (blue). (Ex. 1002, ¶107). Fig. 1 depicts the bottom opening sealed by an adhesive ("molded resin (28)"). (Ex. 1003, p. 003)(Ex. 1002, ¶108). As described below, this is as in the '714 patent; it



does not prevent the sensor from being inserted, since the adhesive is not applied until after insertion (a different order would be nonsensical). (Ex. 1002, ¶108).

Fig. 1 depicts a cross-section of Yoshino's package. (Ex. 1002, ¶109). As explained by Mr. Guidash, a person of skill would understand that the package extends all the way around the image sensor. (*Id.*). Also, the above passage describes the "light transmitting glass plate (22)" as "hermetically secured", indicating that the package extends all the way around it. (Ex. 1002, ¶110). Thus, there would have been no back or front opening through which to insert the sensor, only the wider opening depicted at the bottom of Fig. 1, through which it must pass. (Ex. 1002, ¶111). If this is not inherent in Yoshino, it is also at least obvious. (*Id.*).

Fig. 1 also shows the sensor **sealing said through hole**, blocking it in exactly the same manner as the '714 patent. (Ex. 1002, ¶112). Then, as indicated below, Yoshino discloses **the solid-state image sensing device being secured to said package via** "molded resin (28)". (Ex. 1002, ¶113). As explained by Mr. Guidash, "molded resin (28)" functions here as **an adhesive**. (*Id.*).

> "By supporting the solid-state image sensor (25) in the packaging substrate (20) via a molded resin (28), a desired solid-state image pickup device is obtained." (Ex. 1003, p. 003)(Ex. 1002, ¶113).

Ground 2. Claim 6 is obvious over Yoshino in view of Izumi.

Claim 6 is obvious under pre-AIA § 103(a) over Yoshino in view of Japanese Pat. App. Pub. No. S63-221667 ("Izumi") (Ex. 1016 and Ex. 1017). (Ex. 1002, ¶115). Izumi was published on Sept. 14, 1988, and is pre-AIA § 102(b) prior art.

The level of ordinary skill is discussed by Mr. Guidash. (Ex. 1002, ¶¶52-59). The level of ordinary skill applies to every ground of obviousness. The rationale for obviousness under § 103 is provided where applicable, in this and every other ground of obviousness.

<u>Claim 6.</u> [6a] "A solid-state image sensing apparatus comprising:"

Yoshino discloses element 6a. *See* Ground 1, element [1a]. (Ex. 1002, ¶118).

[6b] "a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,"

Yoshino discloses element 6b. *See* Ground 1, element [1b]. (Ex. 1002, ¶119).

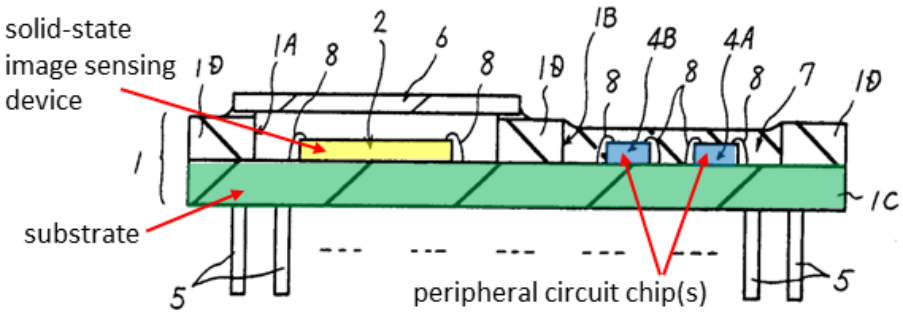
[6c] "a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,"

Yoshino discloses element 6c. *See* Ground 1, element [1c]. (Ex. 1002, ¶120).

[6d] "a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted being inserted into the package from a wider opening thereof, and"

As discussed for Ground 1, element [1d], Yoshino discloses an image sensor **being inserted into the package from a wider opening thereof**. (Ex. 1002, ¶121). It would have been obvious to use, in place of the image sensor alone, **a substrate on which a solid-state image sensing device and a peripheral circuit**

chip are mounted. (*Id.*). In a similar context, Izumi discloses a package in which an image sensor and peripheral circuit chip are mounted on a common substrate. (Ex. 1016, p. 004-005, Fig. 2)(Ex. 1002, ¶122). Petitioner has highlighted Izumi's Fig. 2 at right to show "base substrate 1C" (green), on which "solid state imaging element chip 2" (yellow) and "peripheral circuit chips 4A to 4D" (blue) are mounted. (Ex. 1002, ¶123).



Izumi describes Fig. 2 as follows, noting the "internalization" (moving into the package) of the peripheral chips:

> "[N]oise in the output signal of solid state imaging element chip 2 is reduced through the internalization of peripheral circuit chips 4A to 4D …. As shown in Figure 2, the solid state imaging device is formed such that package member 1 is comprised of sealing base substrate 1C, and frame member 1D …." (Ex. 1016, p. 005)(Ex. 1002, ¶124).

In Izumi Fig. 2, the image sensor and peripheral chip are in separate "cavity part(s)" of the package. (Ex. 1016, p. 005)(Ex. 1002, ¶125). Izumi also teaches a prior art device that mounts them in one chamber. (Ex. 1016, p. 003, Problems to be Solved…)(Ex. 1002, ¶125). Claim 6, in any case, does not require them to be in the same cavity of a package, but only in the same package. (Ex. 1002, ¶125).

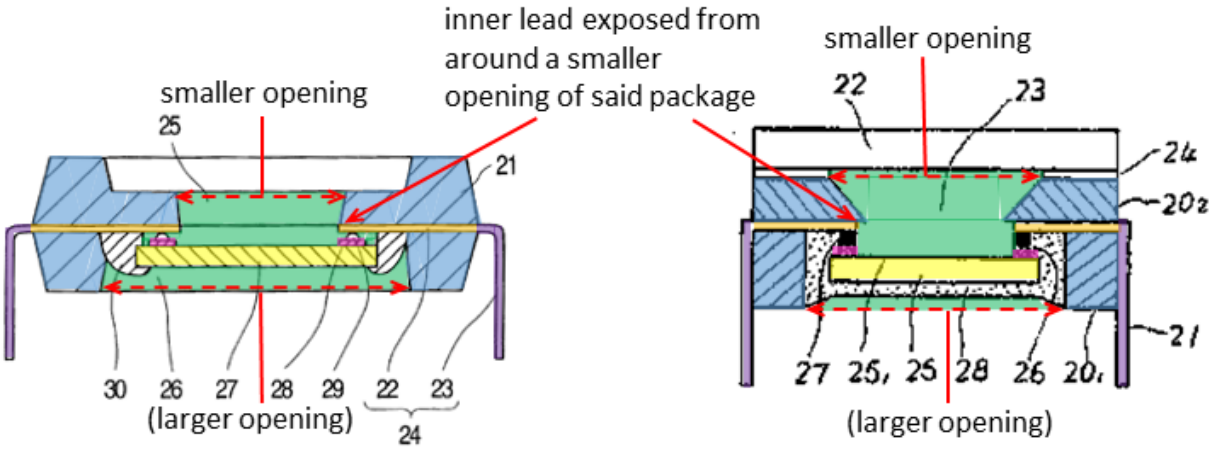
One of ordinary skill would have been motivated to use the substrate (and package divider) disclosed in Izumi with Yoshino's package. (Ex. 1002, ¶126). Having a peripheral chip and image sensor on a common substrate provides a reduction in noise (see quote above) and shorter signal path, which lowers power requirements and increases speed (commercially desirable features), protects the peripheral chip, and takes up less space overall than if the chip were mounted outside the package. (*Id.*). Placing the substrate in Yoshino's package provides the advantage of reduced size over a package using wire bonds. (*Id.*). Furthermore, Izumi's use of a substrate on which to mount chips was a known variation to a base system (Yoshino) with no unexpected results, and is thus obvious under *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 402-03 (2007). (Ex. 1002, ¶126).

[6e] "an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,"

Yoshino discloses **an electrode pad** ("bonding pads 26") of a solid-state image sensing device **connected to said inner lead** (inner part of "electrode leads (21)"):

> "The **solid-state image sensor (25)** is placed so that **the bonding pads (26) of the solid-state image sensor (25)** are aligned with the electrode leads (21), and the **bonding pads (26) and the electrode leads (21)** aligned therewith **are connected** …." (Ex. 1003, p. 003)(emph. add.)(Ex. 1002, ¶127).

Yoshino's "bonding pads (26)" electrically connect "solid-state image sensor (25)" to the leads, thus they are electrical connection points on a semiconductor device, *i.e.*, electrode pads. (Ex. 1002, ¶128).

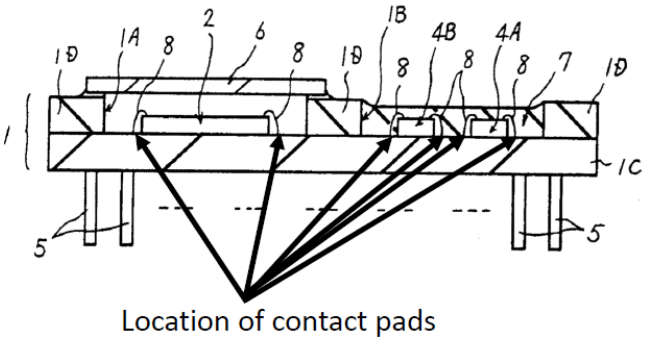


'714 patent Fig. 2 Yoshino Fig. 1

That Yoshino's inner lead is **exposed from around a smaller opening of said package** in the same way as in the '714 patent is shown in the above comparison of Yoshino's Fig. 1 and the '714 patent's Fig. 2, with annotations by Petitioner, and highlighting showing the like elements as described in § III.A. (Ex. 1002, ¶129).

As discussed above for element [6d], **it would have been obvious to use Izumi's substrate** in place of Yoshino's image sensor. (Ex. 1002, ¶130). Moreover, Izumi discloses that its chips (image sensor and peripheral chips) have upward-facing contacts that are wire-bonded to the substrate. (Ex. 1002, ¶131). The connection to the substrate would have involved an electrode pad, because the wire bond must connect to a conductive electrode on the surface of the

semiconductor substrate in order to maintain an electrical circuit. (*Id.*). This is shown at right in Fig. 2 of Izumi, where the Petitioner has drawn arrows to show where wire bonds 8 meet bonding pads on the substrate. (*Id.*). Izumi further notes that, by means of the wire bond connections from the chip, the contacts on each chip are electrically connected to Izumi's package leads:



> "In the same manner as solid state imaging element chip 2, this peripheral circuit chip 3 is connected to leads 5 and solid state imaging element chip 2 through interposed bonding wires 8 and wiring". (Ex. 1016, p. 004, middle)(Ex. 1002, ¶132).

Thus, it would have been obvious in Izumi to connect bonding pads on the surface of the semiconductor substrate to the inner leads of Yoshino, because the bonding pads serve the same purpose as those of Yoshino. (Ex. 1002, ¶133). A person of ordinary skill would simply have used the existing wiring of the substrate of Izumi (see quote above) to route the electrical connections to electrode pads where they could connect to the leads of Yoshino's package, instead of routing the connections to points where they connect to Izumi's leads (5). (*Id.*).

[6f] "said substrate being secured to said package via an adhesive."

As discussed for Ground 1, element [1d], Yoshino discloses an image sensor

being secured to said package via an adhesive. As discussed above for element [6d], **it would have been obvious to use Izumi's substrate** in place of Yoshino's image sensor. (Ex. 1002, ¶134).

Ground 3. Claim 7 is obvious over Yoshino in view of Nagano, in further view of Wakabayashi.

Claim 7 is obvious under pre-AIA § 103(a) over Yoshino in view of Japanese Pat. App. Pub. No. H06-029507 ("Nagano") (Ex. 1018 and Ex. 1019), in further view of Japanese Pat. App. Pub. No. H07-045803 ("Wakabayashi") (Ex. 1004 and Ex. 1007)(Ex. 1002, ¶136). Nagano was published on Feb. 4, 1994 and Wakabayashi was published on Feb. 14, 1995; both are pre-AIA § 102(b) prior art.

Claim 7. ***[7a] "A solid-state image sensing apparatus comprising:"***

Yoshino discloses element 7a. *See* Ground 1, element [1a]. (Ex. 1002, ¶141).

[7b] "a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,"

Yoshino discloses element 7b. *See* Ground 1, element [1b]. (Ex. 1002, ¶142).

[7c] "a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,"

Yoshino discloses element 7c. *See* Ground 1, element [1c]. (Ex. 1002, ¶143).

[7d] "a semiconductor substrate having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof, said semiconductor substrate being inserted into a plastic package via the larger of two openings formed in said package, and"

As discussed for Ground 1, element [1d], Yoshino discloses an image sensor

being inserted into a package via the larger of two openings formed in said package. (Ex. 1002, ¶144). As discussed in § IV.E, "package" and "plastic package" should be construed here to indicate the same (plastic) package. (Ex. 1002, ¶144). Yoshino does not expressly disclose a plastic package. (Ex. 1002, ¶145). However, plastic was a known equivalent for other package materials. (*Id.*). Wakabayashi discloses using plastic as a package material in a similar context. (Ex. 1004, Abstract)(Ex. 1002, ¶145). Wakabayashi's plastic could have been used in Yoshino's package with ordinary skill and predictable results. (Ex. 1002, ¶145). Thus, a plastic package was obvious under *KSR v. Teleflex.* (*Id.*).

While Yoshino discloses a semiconductor image sensor (which is a semiconductor substrate having an image sensor), Yoshino does not expressly disclose **a peripheral circuit chip disposed on an upper surface thereof**. (Ex. 1002, ¶146). Nagano discloses this, as shown in

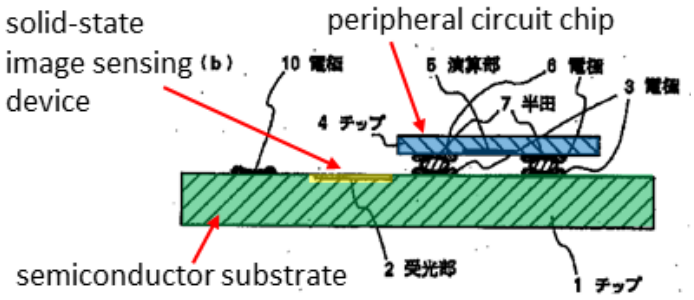


Fig. 1(b) of Nagano, annotated here. (Ex. 1002, ¶¶147-148). As shown in the figure, Nagano discloses a **semiconductor substrate** ("chip 1", highlighted green) **having a solid-state image sensing device** ("light-receiving part 2", yellow) **and a peripheral circuit chip** ("chip 4 having a computing part 5", blue) **disposed on an upper surface thereof**. (Ex. 1018, ¶0008)(Ex. 1002, ¶148). Nagano recites:

> "[A] photodiode with a computing function characterized in that a **light-receiving part for converting an optical signal into an electrical signal** and a **computing part** for operating upon the electrical signal are **formed on different semiconductor chips**; on the semiconductor chip on which the computing part is formed there are provided electrodes in the same disposition as a number of electrodes of the semiconductor chip on which the light-receiving part is formed; and **these chips have their electrodes connected**." (Ex. 1018, Claim 1)(emph. add.)(Ex. 1002, ¶147).

One of ordinary skill would have been motivated to use the semiconductor substrate disclosed in Nagano with Yoshino's package for the same reasons and with the same results as described for Ground 2, element [6d] with regard to Izumi (namely, to reduce the length of electrical connections, reduce noise, and reduce size). (Ex. 1002, ¶149). Having the image sensor *formed* on the substrate as in Nagano provides a further motive of additional space savings. (*Id.*). Furthermore, mounting a peripheral chip on a substrate (including making the substrate somewhat larger to accommodate the peripheral chip) was a known variation to a base system (Yoshino) with no unpredictable results, and therefore obvious under *KSR v. Teleflex.* (*Id.*).

> ***[7e] "an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around the smaller opening of said package,"***

As discussed above for Ground 2, element [6e], Yoshino discloses **an electrode**

pad of an image sensor **being connected to the inner lead exposed from around the smaller opening of said package**. (Ex. 1002, ¶150). As discussed above for element [7d], **it would have been obvious to use Nagano's semiconductor substrate** in place of Yoshino's image sensor. (*Id.*). Furthermore, Nagano's substrate is provided with contact pads ("electrodes 10"). (Ex. 1019, ¶0008)(Ex. 1002, ¶151). Thus, electrodes (pads) 10 in Nagano serve the same function as the pads in Yoshino, and it would have been obvious to connect them to the inner leads of Yoshino. (Ex. 1002, ¶151).

[7f] "said semiconductor substrate being secured to said package via an adhesive."

As discussed for Ground 1, element [1d], Yoshino discloses an image sensor **being secured to said package via an adhesive**. As in element [7d], it would have been obvious to use Nagano's **semiconductor substrate**. (Ex. 1002, ¶152).

Ground 4. Claim 8 is obvious over Yoshino in view Izumi or Nagano, in further view of Hirosawa and Nita.

Claim 8 is obvious under pre-AIA § 103(a) over Yoshino in view of Izumi (if from claim 6) or Nagano (if from claim 7), in further view of Japanese Pat. App. Pub. No. S60-74880 ("Hirosawa") (Ex. 1020 and Ex. 1021) and Japanese Pat. App. Pub. No. H07-78951 ("Nita") (Ex. 1011 and Ex. 1023). (Ex. 1002, ¶154). Hirosawa was published on April 27, 1985, and so is pre-AIA § 102(b) prior art. Nita was published on March 20, 1995, and so is pre-AIA § 102(b) prior art.

> ***Claim 8.*** ***"The solid state image sensing apparatus of claim 6 or claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device."***

Claim 8 is multiply dependent from claims 6 and 7. Whether claim 6 or claim 7 is the base claim, claim 8 is obvious. (Ex. 1002, ¶154). The combinations of Yoshino and Izumi (claim 6) or Yoshino and Nagano (claim 7) do not expressly disclose a **shading film**. (Ex. 1002, ¶159). However, applying a shading film was a well-known technique that would have been an obvious step in an image-sensing package. (*Id.*). For example, Hirosawa and Nita both teach using a shading film to protect the peripheral circuit elements of an image sensing apparatus from light, while leaving the image sensor unshaded. (Ex. 1020, p. 480; Ex. 1011, p. 5)(Ex. 1002, ¶159). One of ordinary skill could have envisioned a variety of applications of this technique, as illustrated by the differences in application between Hirosawa and Nita. (Ex. 1002, ¶159).

Specifically, Hirosawa discloses a semiconductor substrate ("semiconductor chip 2") on which an image sensor ("a light detection semiconductor element") and a peripheral circuit chip ("a signal processing circuit element") are formed, which is mounted in a package having **a shading film** ("light-shielding film"). (Ex. 1020, p. 003; Fig. 1)(Ex. 1002, ¶160). Hirosawa's Fig. 1 depicts the shading film (labeled "3", though the specification erroneously refers to it as "8") ***on*** **the entire**

upper surface of the substrate except an upper surface of the solid-state image sensing device, section 2L. (Ex. 1020, p. 003, Fig. 1)(Ex. 1002, ¶¶160-161).

Nita, on the other hand, discloses a similar package in which an image sensor ("light receiving section") and peripheral circuit elements ("storage section") are mounted on a substrate ("chip 1"), and a shading film ("the light shielding section") is located ***above* the substrate**, on the "transparent glass lid 4" of "package 2". (Ex. 1011, ¶¶0015-0016; *see also* Figs. 3 and 4)(Ex. 1002, ¶162). This is as shown in the '714 patent's Fig. 7. (Ex. 1002, ¶163).

Using a light-shading film, such as that of Hirosawa or Nita, over the entire area of the substrate not having the image sensor would have the predictable advantage of protecting the peripheral chip from light (or of minimizing light reaching the peripheral chip that might obtain with partial coverage). (Ex. 1002, ¶164). It is furthermore a known improvement providing predictable results for systems such as these, and obvious under *KSR v. Teleflex*. (*Id.*).

With respect to base claim 6, Petitioner notes that Izumi itself describes blocking light to the peripheral chips by covering the peripheral chip section with resin sealing material 7, thus demonstrating that the function of blocking light to the peripheral chip was common and obvious. (Ex. 1016, p. 004)(Ex. 1002, ¶165). When combined with Yoshino a person of ordinary skill would have known that a light-shading layer was an equivalent—or additional—way to block light from

reaching the peripheral circuitry, and the substitution or additional use of light-shading layer would have been obvious. (Ex. 1002, ¶165).

Ground 5. Claim 9 is obvious over Yoshino in view of Izumi or Nagano.

Claim 9 is obvious under pre-AIA § 103(a) over Yoshino in view of Izumi (if from claim 6) or Nagano (from claim 7). (Ex. 1002, ¶167). Claim 9 is multiply dependent from claims 6 and 7, but is obvious whether claim 6 or claim 7 is the base claim, as discussed below. (Ex. 1002, ¶167).

> ***Claim 9.*** ***"The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via a bump."***

As discussed for Ground 2, element [6e] and Ground 3, element [7e] above, Yoshino in combination with Izumi or Nagano renders obvious **an electrode pad formed on the substrate connected to the inner lead**. (Ex. 1002, ¶168). In the passage below, Yoshino discloses that **the electrode pads** of its image sensor are **connected to the inner lead** (the inner part "of electrode leads (21)") **via a bump**. (Ex. 1002, ¶169). The bump is made from Indium, which is an additional amount of conductive material. (Ex. 1002, ¶169). Yoshino states:

> "The solid-state image sensor (25) is placed so that the bonding pads (26) of the solid-state image sensor (25) are aligned with the electrode leads (21), and **the bonding pads (26) and the electrode leads (21)** aligned therewith **are connected via a conductive bonding material (27), for example, indium**. The electrode leads (21) are coated with

> the conductive bonding material (27) by means of plating, brazing, or the like." (Ex. 1003, p. 003)(emph. add.)(Ex. 1002, ¶169).

As explained by Mr. Guidash, Indium is a metal used in press fit bump-bonding. (Ex. 1002, ¶170). Thus, Yoshino discloses that its image sensor's electrode pads are electrically connected via an amount of conductive (metal) material, *i.e.*, a **bump**. (Ex. 1002, ¶¶171-172).

For the reasons discussed for Ground 2, element [6d] and Ground 3, element [7d] that it would have been obvious to use a substrate with an image sensor and peripheral chip in Yoshino's package, it would have been obvious to use the connector Yoshino discloses (bumps) to connect the substrate. (Ex. 1002, ¶173). To do so would have the predictable advantage of providing a smaller package. (*Id.*). Furthermore, bump bonding was a known technique for this sort of bonding and could be applied with ordinary skill and with predictable results. It is thus obvious under *KSR v. Teleflex*. (*Id.*).

Ground 6. Claim 10 is obvious over Yoshino in view of Izumi or Nagano, in further view of Wakabayashi.

Claim 10 is obvious under pre-AIA § 103(a) over Yoshino in view of Izumi (claim 6) or Nagano (claim 7), in further view of Wakabayashi. (Ex. 1002, ¶175). Claim 10 is multiply dependent from claims 6 and 7. Claim 10 is obvious regardless of whether claim 6 or 7 is the base claim. (Ex. 1002, ¶175).

Claim 10. ***"The solid-state image sensing apparatus of claim 6 or***

claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity."

As discussed for Ground 2, element [6e] and Ground 3, element [7e], Yoshino in combination with Izumi or Nagano renders obvious **an electrode pad formed on the substrate connected to the inner lead**. (Ex. 1002, ¶176). Wakabayashi discloses making such a connection **via an anisotropic conductor**:

> "[T]he **joining of the chip to the inner leads** via the bumps **is performed via the conductive adhesive layer** formed on the surfaces of the bumps disposed **on the bonding pads of the CCD chip**." (Ex. 1004, ¶0006)(emph. add.)(Ex. 1002, ¶177).

> "For the conductive layer, … a resin-based **anisotropic conductive adhesive** can be suitably used." (Ex. 1004, ¶0014)(emph. add.)(Ex. 1002, ¶177).

An anisotropic conductor is one which is conductive only in one direction. (Ex. 1002, ¶178). It is obvious that Wakabayashi's conductor has **only vertical conductivity**, because Wakabayashi's Fig. 2 shows the connection between the sensor and the inner lead made in vertical plane. (Ex. 1004, Fig. 2)(Ex. 1002, ¶178). One of ordinary skill would have been motivated to combine Yoshino and Izumi or Nagano with Wakabayashi because an anisotropic conductor allows for a fine pitch—*i.e.*, the connection points on the sensor can be close together, allowing for more connection points and/or a reduced footprint. (Ex. 1002, ¶179).

Wakabayashi's anisotropic conductor was also a known substitute for other electrical connection methods (*e.g.* the bump bonding of Yoshino), with no unexpected results, and is thus obvious under *KSR v. Teleflex*. (*Id.*).

Ground 7. Claim 11 is obvious over Yoshino in view of Izumi or Nagano, in further view of Onishi.

Claim 11 is obvious under pre-AIA § 103(a) over Yoshino in view of Izumi (claim 6) or Nagano (claim 7), in further view of Japanese Pat. App. Pub. No. 05-006989 ("Onishi")(Ex. 1014 and Ex. 1015). (Ex. 1002, ¶181). Claim 11 is multiply dependent from claims 6 and 7. Claim 11 is obvious regardless of whether claim 6 or 7 is the base claim. (Ex. 1002, ¶181).

> ***Claim 11.*** ***"The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead at an outer portion of said lead, said outer portion of said lead extending into the openings of the package."***

As discussed for Ground 2, element [6e] and Ground 3, element [7e], above, Yoshino in combination with Izumi or Nagano discloses **an electrode pad formed on the substrate connected to the inner lead**. (Ex. 1002, ¶184). In a very similar context, Onishi discloses **an outer portion of said lead extending into the openings of the package**, as follows:

> "The imaging element (1) is electrically connected to the inner edges of the leads (8) by the bump electrodes (6) …. [In one embodiment], the imaging element (1) is connected to **the inner edges of the leads**

> **(8) that protrude into a hollow space** within the window of the base (7), so the stress during the hardening of the sealing resin (4) can be absorbed by the flexibility of the leads (8)." (Ex. 1014, ¶¶0016-0017, *see also* Figs. 3 and 4)(emph. add.)(Ex. 1002, ¶¶185-186).

It would have been obvious to use Onishi's extended inner lead with Yoshino's package, or the package for an image sensor/peripheral chip substrate as rendered obvious by the combination of Yoshino/Izumi or Yoshino/Nagano. (Ex. 1002, ¶187). To do so would have detached the inner lead of Yoshino from the package, which would have allowed the lead to flex, thus relieving stress during hardening of the adhesive. (*Id.*). It would also have provided for accuracy in positioning of the image sensor and of bonding of the inner lead to the substrate's pads. (*Id.*). It is also a known variation on a base system (Yoshino) that would have led to no unpredictable results, and thus obvious under *KSR v. Teleflex*. (*Id.*).

Ground 8. Claim 12 is obvious over Yoshino in view of Tobase.

Claim 12 is obvious under pre-AIA § 103(a) over Yoshino in view of Japanese Pat. App. Pub. No. H05-275611 ("Tobase") (Ex. 1022 and Ex. 1013)(Ex. 1002, ¶189). Tobase was published on Oct. 22, 1993, and is pre-AIA § 102(b) prior art.

Claim 12. ***[12a] "A solid-state image sensing apparatus comprising:***

Yoshino discloses this. *See* Ground 1, element [1a]. (Ex. 1002, ¶192).

[12b] "a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,"

Yoshino discloses this. *See* Ground 1, element [1b]. (Ex. 1002, ¶193).

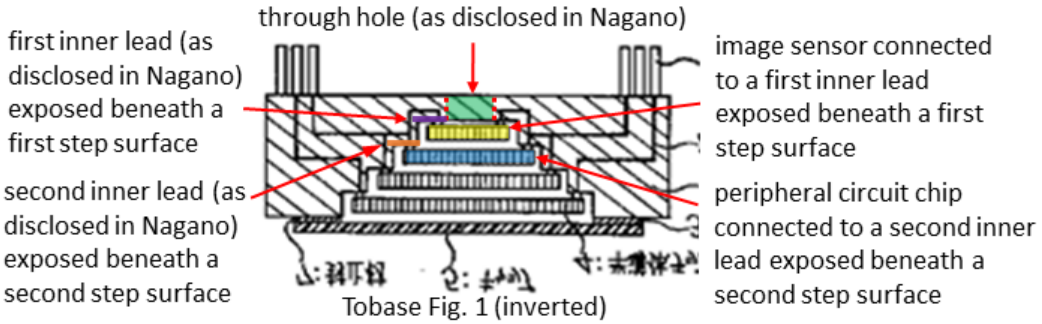
[12c] "a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and"

Yoshino discloses this. *See* Ground 1, element [1c]. (Ex. 1002, ¶194).

[12d] "a solid-state image sensing device and a peripheral circuit chip both mounted in said package, said solid-state image sensing device being connected to a first inner lead exposed beneath a first step surface formed in said package, said solid-state image sensing device being secured to said package via an adhesive, and said peripheral circuit chip being connected to a second inner lead exposed beneath a second step surface formed in said package, said peripheral circuit chip being secured to said package via an adhesive."

Yoshino discloses **a solid-state image sensing device mounted in a package,** as discussed for Ground 1, elements [1a]-[1d], and that the image sensor is **connected to an inner lead**, as in Ground 2, element [6e]. (Ex. 1002, ¶195). Tobase discloses or renders obvious the remaining limitations. (*Id.*).

Tobase discloses multiple "semiconductor chips" mounted in a package with multiple **step surfaces**, as shown in Fig. 1 of Tobase, below. (Ex. 1002, ¶196).



Tobase Fig. 1 (inverted)

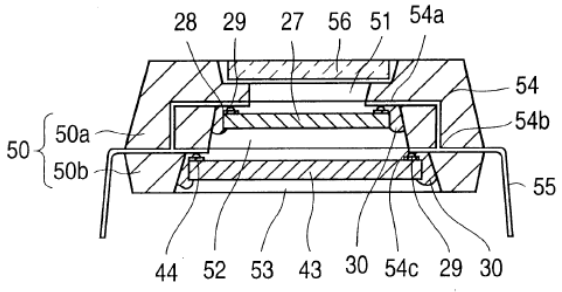
The Petitioner has inverted the figure to match the orientation of the '714

patent, and added highlighting and English text annotations. (*Id.*). As Mr. Guidash explains, inverting Fig. 1 is appropriate since the relevant factor in both cases is the orientation of the chip with regard to the package. (*Id.*).

Tobase describes Fig. 1 as follows:

> "As shown in Fig. 1, **semiconductor chips** 4 are severally received multi-step-wise in the vertical direction, apart from and parallel with each other, **in multiple steps of recess** provided in an electrically insulating substrate 1 having an electrical interconnector pattern 2. Bumps 3 are formed on the steps where the semiconductor chips 4 are disposed. The semiconductor chips 4 are disposed on these bumps 3, and the **semiconductor chips are connected** as necessary to each other or **to external leads 6 by the electrical interconnector pattern 2**." (Ex. 1022, ¶0009)(emph. add.)(Ex. 1002, ¶197).

Tobase's structure is very similar to that of Fig. 8 of the '714 patent, reproduced at right. (Ex. 1002, ¶198). Like Tobase, Fig. 8 shows chips connected to inward-progressing steps, with the smaller chip deeper into the package. (*Id.*).



It would have been obvious to use Tobase's step structure in Yoshino's package. (Ex. 1002, ¶199). Tobase's step structure would provide an additional space saving benefit (important in small devices). (*Id.*). Tobase reports the result that "mounting density can be increased and the interconnector path lengths of the

electrical interconnnectors can be shortened and the signal propagation time thereby shortened, and high-speed operation of the multi-chip module thereby made possible." (Ex. 1022, ¶0018)(Ex. 1002, ¶199). Also, it would help protect the peripheral chip from light exposure, reducing or eliminating the need for a shading film, leading to fabrication cost and time savings. (Ex. 1002, ¶200). Tobase's step structure is a simple, mechanical variation on Yoshino's package that was well within ordinary skill, and has no unexpected results. (Ex. 1002, ¶201). The combination is thus obvious under *KSR v. Teleflex*. (*Id.*).

When combined with Yoshino's package for a **solid-state image sensor**, it would be obvious for one of Tobase's other chips to be a **peripheral circuit chip**, as this is the type of chip one of ordinary skill would know to package with an image sensor. (Ex. 1002, ¶202). Furthermore, as suggested by Tobase's multiple connection points, it would have been obvious to have **first** and **second inner leads** in a package for multiple chips, because each chip must be connected. (*Id.*). If Yoshino were modified by using a stepped structure like Tobase's Fig. 1, the **first** and **second inner leads** would be **exposed beneath a first** and a **second step surface formed in said package**. (Ex. 1002, ¶203).

Finally, as discussed for Ground 1, element [1d], Yoshino discloses **securing the image sensor via an adhesive**. (Ex. 1002, ¶204). It would be obvious to use Yoshino's adhesive for the peripheral chip as well, since using two different

securing methods would be unnecessarily complex and costly. (*Id.*).

Ground 9. Claim 13 is obvious over Yoshino in view of Hikosaka.

Claim 13 is obvious under pre-AIA § 103(a) over Yoshino in view of Japanese Pat. App. Pub. No. S59-225560 ("Hikosaka") (Ex. 1005 and Ex. 1008)(Ex. 1002, ¶206). Hikosaka was published on Dec. 8, 1984, and is pre-AIA § 102(b) prior art.

Yoshino discloses the elements of claim 13 that are common to claim 1, as described in Ground 1 above. Claim 13, however, adds the requirement of "simultaneously adjusting the optical positioning of said solid-state image sensing device." This step is taught by Hikosaka. It would have been obvious to use Hikosaka's simultaneous optical positioning to improve the positioning of the image sensor within Yoshino's package, as described below. (Ex. 1002, ¶206).

> ***Claim 13.*** ***[13a] "A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package, said manufacturing method comprising the steps of:"***

As discussed above for claim 1 elements, [1a]-[1d], Yoshino discloses the **solid-state image sensing apparatus** of element [13a]. (Ex. 1002, ¶209). Yoshino also describes steps by which the apparatus is "constructed"—*i.e.*, a **manufacturing method**. (Ex. 1003, p. 003)(Ex. 1002, ¶210).

> ***[13b] "inserting said solid-state image sensing device into said through hole,"***

Yoshino discloses this. *See* Ground 1, element [1d]. (Ex. 1002, ¶211).

[13c] "connecting an electrode pad of the solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device, and"

As discussed for Ground 2, element [6e], Yoshino discloses **connecting an electrode pad of the image sensor to the inner lead**. (Ex. 1002, ¶212). As discussed for Ground 5, claim 9, Yoshino discloses connecting via a **bump** (and element [13c] only requires a bump *or* anisotropic conductor). (*Id.*).

Yoshino does not expressly disclose "**simultaneously adjusting the optical positioning of said solid-state image sensing device**." This element is, however, disclosed by Hikosaka in the same context: a solid-state image-sensing apparatus for use in a lens system (*e.g.*, a camera). (C*ompare* Ex. 1005, p. 002 ("lens system") to Ex. 1003, p. 003 ("camera"))(Ex. 1002, ¶213).

Hikosaka teaches **optical positioning**: both adjusting the position of the image sensor to obtain the correct position for use in an optical ("lens") system, and making the adjustment *optically* (*i.e.*, using optical information/measurements). (Ex. 1002, ¶214). First, Hikosaka describes adjusting the position of the image sensor to obtain the correct position for use in an optical system:

> "Since the solid-state image pickup device is used in combination with a lens system, the semiconductor chip 1 must be highly

> accurately aligned with the housing 2." (Ex. 1005, p. 002)(Ex. 1002, ¶215).

Then, Hikosaka teaches that positioning is done using optical information, and that this process takes place **simultaneously with connecting an electrode pad of the image sensor to the lead**. (Ex. 1002, ¶216). Hikosaka explains its process as follows. (*Id.*). First,

> "**a semiconductor chip 12** held by a vacuum suction holding means (not shown) **is placed on the solder bumps 11 in the recess 7a of the housing 7** placed at the prescribed position described above so that its **electrodes 12a come into contact with the solder bumps 11.**" (Ex. 1005, p. 003)(emph. add.)(Ex. 1002, ¶¶216-217).

Thus, Hikosaka teaches that **electrode pads** ("electrodes 12a") **of the solid-state image sensing device** ("semiconductor chip 12") **are connected via bumps 11.** (Ex. 1005, p. 003)(Ex. 1002, ¶217). Once the image sensor is electrically connected, it is powered on and a light beam is projected from "lamp 25" toward the sensor's surface, through "lens 23" and a transparent "marking plate 24" on which "a cross-shaped marking 24a is provided." (Ex. 1005, p. 003; *see also* Fig. 4)(Ex. 1002, ¶217). This produces a cross-shaped "shadow" on the sensor's surface. (Ex. 1005, p. 003)(Ex. 1002, ¶217). The captured image is displayed on a monitor, on which another cross-shaped "reference marking [15a]… has been preset in relation to the housing 7" (*i.e.*, the package). (Ex. 1005, p. 003)(Ex.

1002, ¶218). The sensor is moved until mark 15a aligns with mark 24a. (Ex. 1005, p. 3)(Ex. 1002, ¶218). Once the marks are aligned, the image sensor's connection to the leads is mechanically fixed for normal use, as described below:

> "Then, the electrodes 12a of the semiconductor chip 12 and the metalized pattern 10 are facedown bonded using the heating means for facedown bonding to secure the semiconductor chip 12 to the housing 7." (Ex. 1005, p. 004)(Ex. 1002, ¶218).

Thus, Hikosaka teaches that the image sensor is first inserted, then electrically connected to the leads, then positioned using optical information, and then electrically/mechanically connected in a more durable manner. (Ex. 1002, ¶219). In other words, Hikosaka teaches that the image sensor is positioned as part of the connection process—*i.e.,* **connecting … while simultaneously adjusting the optical positioning of said solid-state image sensing device**. (*Id.*).

It would have been obvious to use Hikosaka's simultaneous optical positioning with the package of Yoshino. (Ex. 1002, ¶220). First, one of ordinary skill would have known that positioning was necessary for an image sensor package. (*See* Ex. 1001, 1:66-2:5 (admitting need for accurate positioning))(Ex. 1002, ¶220). In particular, Yoshino—like Hikosaka—teaches that its image sensor package is used in an optical system with a lens (*e.g.*, a camera), so one of ordinary skill would have known to optically position the image sensor. (Ex. 1002, ¶221).

Yoshino's through hole, face-bonded package structure with a light transmitting

glass plate would have suggested to one of ordinary skill to do the optical positioning while mounting and connecting the image sensor using the techniques of Hikosaka. (Ex. 1002, ¶222). In a package (such as that described in the admitted prior art) in which an image sensor is first die-bonded to the package, then electrically connected to the leads via wire bonds, positioning must be complete *before* the electrical connection step, since the sensor cannot be moved after it is die bonded. (*Id.*). In Yoshino's package, the electrical connection is made via bumps, which—as taught in Hikosaka—allow for adjustment of the position *while* the connection is being made. (*Id.*). Yoshino and Hikosaka recite different bump bonding techniques (press fitting bumps vs. heating bumps), but both allow for the image sensor to be electrically connected for the positioning process before being fixed for normal use, as explained by Mr. Guidash. (*Compare* Ex. 1003, p. 003 to Ex. 1005, p. 004)(Ex. 1002, ¶223). Also, Yoshino's through hole allows the sensor to be visible (and its precise position ascertained) while it is being connected to the leads. (Ex. 1002, ¶224). Thus, the most logical time to position it is during connection. (Ex. 1002, ¶225).

Hikosaka discloses an image sensor package very similar to that of Yoshino. (*Compare* Ex. 1005, Fig. 4 to Ex. 1003, Fig. 1 (note that Hikosaka depicts its package inverted relative to that of Yoshino)). (Ex. 1002, ¶226). Use of Hikosaka's technique would provide the predictable advantage of reduced

fabrication time/cost over methods that involve more steps, as described above. (Ex. 1002, ¶227). Hikosaka states that its process "enables high precision alignment of the semiconductor chip with the housing". (Ex. 1005, p. 002)(Ex. 1002, ¶227). The combination would also allow the sensor to be active while positioning, providing optical feedback enabling high precision. (Ex. 1002, ¶227). This was an advantage because precision in image sensor placement was crucial in developing higher quality optical devices. (*Id.*). The combination also represents a known improvement on a known base system, that—as explained by Mr. Guidash—could have been implemented using ordinary skill without unexpected results, and is thus also obvious under *KSR v. Teleflex*. (Ex. 1002, ¶228).

[13d] "securing said solid-state image sensing device to the package with an adhesive."

Yoshino discloses this. *See* Ground 1, element [1d]. (Ex. 1002, ¶229).

Ground 10. Claim 15 is obvious over Yoshino in view of Izumi and Nagano, in further view of Hikosaka.

Claim 15 is obvious under pre-AIA 35 U.S.C. § 103(a) over Yoshino in view of Izumi and Nagano, in further view of Hikosaka. (Ex. 1002, ¶231).

<u>Claim 15.</u> [15a] "A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:"

As discussed for Ground 9, element [13a], Yoshino discloses element [15a]

except for a **peripheral circuit chip**; as discussed for Ground 2, element [6d], Izumi discloses one, obvious to use in Yoshino's package. (Ex. 1002, ¶232).

[15b] "mounting said solid-state image sensing device and said peripheral circuit chip on a substrate where a group of wirings is disposed in order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings,"

As discussed for Ground 2, element [6d], Izumi discloses **mounting said solid-state image sensing device and said peripheral circuit chip on a substrate**. (Ex. 1002, ¶233). Izumi also discloses that on the substrate **a group of wirings is disposed in order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings**:

> "**The bonding pads of the solid state imaging element chip 2**, not shown in the drawing, **are connected to the wiring of package member 1** …. **Peripheral circuit chips 4A to 4D are connected** to leads 5 and solid state imaging element chip 2 **through** interposed bonding wires 8 and **wiring**." (Ex. 1016, p. 004)(emph. add.)(Ex. 1002, ¶234).

The wirings are obviously **on the substrate** ("base substrate 1C"), as that is where the sensor and chip (to which they are connected) are mounted. (*See* Ex. 1016, p. 005 and Fig. 2)(Ex. 1002, ¶234). This is visible in Izumi's Figs 1-3, because wire bonds 8 extend from contacts the chips to contacts on the substrate, as shown by the annotated figure under Ground 2, element [6e]. (Ex. 1002, ¶234).

[15c] "inserting the semiconductor substrate into the through

hole,"

As discussed for Ground 2, element [6d], **inserting the substrate into the through hole** is obvious over a combination of Yoshino and Izumi. (Ex. 1002, ¶235). As discussed in § IV.F, claim 15 uses both "substrate" and "semiconductor substrate" to mean a semiconductor substrate. (Ex. 1002, ¶236). Izumi's substrate is not explicitly a **semiconductor substrate**. (*Id.*). However, as explained by Mr. Guidash, semiconductor was a known substrate material that would be functionally equivalent here: *i.e.*, semiconductor or another material could both serve as a base on which to mount and wire chips. (*Id.*). Nagano discloses such a semiconductor substrate, as discussed for Ground 3, element [7d] above. (Ex. 1018, Claim 1)(Ex. 1002, ¶236). Nagano's semiconductor substrate could have been substituted using only ordinary skill, with predictable results, and was thus obvious under *KSR v. Teleflex*. (Ex. 1002, ¶236).

[15d] "connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, and"

As discussed for Ground 9, elements [13c], Yoshino in combination with Hikosaka renders obvious this claim element as to connecting an electrode pad of an image sensor. (Ex. 1002, ¶237). For the same reasons discussed for Ground 2, elements [6d]-[6e], one of ordinary skill would have been motivated to use Izumi's **substrate** in place of Yoshino's image sensor in this claim. (Ex. 1002, ¶237). It

was furthermore obvious to locate the electrode pads on the **periphery** of the substrate, to align with Yoshino's inner leads and because the center of the substrate would typically be occupied by the sensor and peripheral chip. (Ex. 1002, ¶238). This would have required no more than ordinary skill in semiconductor fabrication, with only predictable results. (*Id.*).

> ***[15e] "securing the semiconductor substrate on which said solid-state image sensing device and said peripheral circuit chip are mounted to the package via an adhesive."***

As discussed for Ground 2, element [6f], Yoshino/Izumi render this claim element obvious. (Ex. 1002, ¶239). As discussed for element [15c] above, a semiconductor substrate would have been obvious. (Ex. 1002, ¶236).

Ground 11. Claim 16 is obvious over Yoshino in view of Tobase, in further view of Hikosaka.

Claim 16 is obvious under pre-AIA 35 U.S.C. § 103(a) over Yoshino in view of Tobase, in further view of Hikosaka. (Ex. 1002, ¶241).

> ***<u>Claim 16.</u> [16a] "A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in the package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:"***

As discussed for Ground 9, element [13a], Yoshino discloses element [16a] except for a **peripheral circuit chip**; as discussed for Ground 8, element [12d], Tobase/Yoshino render a **peripheral circuit chip** obvious. (Ex. 1002, ¶242).

[16b] "inserting said solid-state image sensing device into the through hole,"

Yoshino discloses this. *See* Ground 1, element [1d]. (Ex. 1002, ¶243).

[16c] "connecting an electrode pad of the solid-state image sensing device to a first inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, said first inner lead being disposed beneath a first step surface formed in said package,"

As discussed for Ground 8, element [12d], Yoshino/Tobase render obvious **connecting the image sensor to a first inner lead disposed beneath a first step surface formed in said package**. (Ex. 1002, ¶244). As discussed for Ground 9, element [13c], Yoshino discloses that the sensor's **electrode pad** is connected, **via a bump**. (Ex. 1002, ¶245). As discussed for Ground 9, element [13c], Yoshino and Hikosaka render obvious **simultaneously adjusting the optical positioning of the solid-state image sensing device**. (Ex. 1002, ¶246). For the same reasons and with the same results discussed there, one of ordinary skill would have been motivated to combine Yoshino/Tobase with Hikosaka. (*Id.*).

[16d] "securing the solid-state image sensing device to the package via an adhesive,"

Yoshino discloses this. *See* Ground 1, element [1d]. (Ex. 1002, ¶247).

[16e] "inserting the peripheral circuit chip into the through hole,"

As discussed for Ground 1, element [1d], Yoshino teaches **inserting** an image sensor into the through hole. (Ex. 1002, ¶248). As discussed for Ground 8,

element [12d], a **peripheral circuit chip** is obvious from Yoshino/Tobase. (*Id.*). It would have been obvious to place the peripheral chip in the package using the same method disclosed in Yoshino. (*Id.*).

[16f] "connecting an electrode pad of the peripheral circuit chip to a second inner lead via a bump or an anisotropic conductor having only vertical conductivity, to complete an electrical connection, said second inner lead being disposed beneath a second step surface formed in said package, and"

As discussed for Ground 8, element [12d], Yoshino with Tobase render obvious **connecting the peripheral circuit chip to a second inner lead disposed beneath a second step surface formed in said package**. (Ex. 1002, ¶249). Yoshino and Tobase both teach bonding **via a bump** (Ex. 1003, p. 003; Ex. 1022, ¶0009), so it is obvious that the connection point of the peripheral chip is **an electrode pad**, a standard feature of bump-bonded chips. (Ex. 1002, ¶249). As discussed for Ground 9, element [13c], Yoshino discloses an **electrode pad**. (*Id.*).

[16g] "securing the peripheral circuit chip to the package via an adhesive."

As in Ground 8, element [12d,] it would be obvious to use Yoshino's adhesive for **securing the peripheral chip to the package**. (Ex. 1002, ¶250).

Ground 12. Claim 1 is obvious over Wakabayashi

Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 103(a) over Wakabayashi. (Ex. 1002, ¶252). As described in § III.B above, Wakabayashi essentially teaches the package of claim 1. Ground 12 is presented under § 103 because Wakabayashi

does not expressly recite that the image sensor is inserted into package's wider opening. As discussed below, this would have been obvious. (Ex. 1002, ¶252).

<u>Claim 1.</u> [1a] "A solid-state image sensing apparatus comprising:"

Wakabayashi refers to its solid-state image sensing apparatus as a "solid-state image pickup device" with a "CCD chip", as recited in the passage below. (Ex. 1002, ¶253). A "CCD chip" is a semiconductor image sensor and is thus solid-state, as semiconductor chip is solid-state. (*Id.*)

> "The present invention relates to a **solid-state image pickup device using a CCD chip**, and is particularly one having a package …." (Ex. 1004, ¶0001)(emph. add.)(Ex. 1002, ¶253).

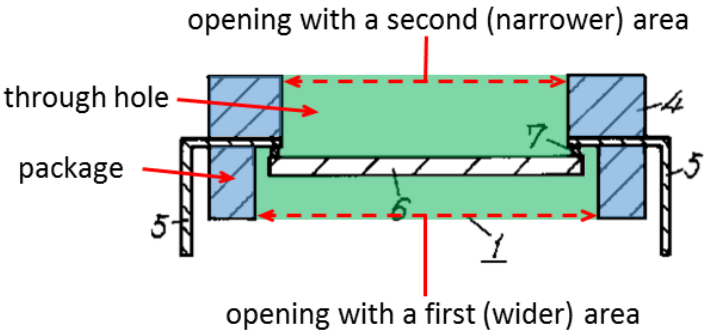
[1b] "a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,"

Wakabayashi teaches a **package having a through hole** (a "space") **therein**. (Ex. 1002, ¶254). Wakabayashi states:

> "The solid-state image pickup device is comprised of a **package 4** …." (Ex. 1004, Abstract)(emph. add.)(Ex. 1002, ¶254).

> "**[The] package … compris[es]** a light-receiving section and side wall sections integrally formed while interposing a lead frame and having, in its interior, **a space** for disposing a CDD chip, the inner lead sections of the lead frame being exposed to the space, …." (Ex. 1004, ¶0005)(emph. add.)(Ex. 1002, ¶254).

As seen in Fig. 1 (annotated below), the package (4) has **openings on both end faces thereof, and different opening areas of said openings**. (Ex. 1002, ¶255). The through hole is shown in green, the package body in blue. (Ex. 1002, ¶255).

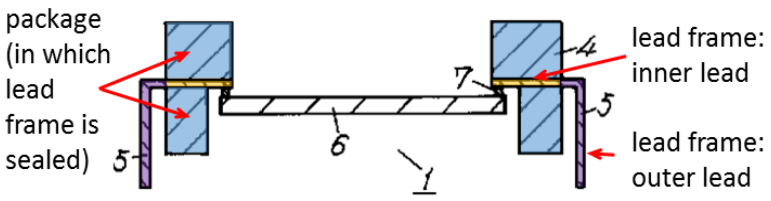


[1c] "a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and"

Wakabayashi discloses **a lead frame comprising inner leads and outer leads** and that the lead frame is **sealed in** ("interpos[ed]" by) **the package** in the same manner as the '714 patent (*compare* '714 patent, Fig. 2), as follows:

> "The solid-state image pickup device according the invention has … a **package** … **interposing a lead frame** and having, in its interior, a space for disposing a CDD chip, the **inner lead sections of the lead frame** being exposed to the space …." (Ex. 1004, ¶0005; *see also* ¶0010 ("leads 5"))(emph. add.)(Ex. 1002, ¶256).

That Wakabayashi also has **outer leads** is made clear by Fig. 1. (Ex. 1002, ¶257). Below, Petitioner has highlighted Fig. 1 to show the inner lead (orange), the outer lead (purple), and the package (blue). (*Id.*).



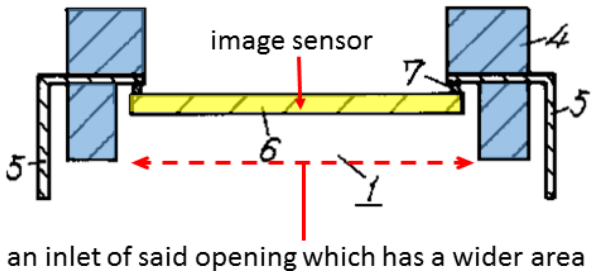
[1d] "a solid-state image sensing device mounted in said package by being inserted

> ***from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive."***

Wakabayashi discloses **a solid-state image sensing device** (a "CCD chip") **mounted in said package**:

> "The solid-state image pickup device according the invention has the basic construction of comprising a **CCD chip joined** via bumps **to the** inner lead sections of a **package** …." (Ex. 1004, ¶0005)(emph. add.)(Ex. 1002, ¶258).

Wakabayashi does not expressly disclose that the image sensor is mounted **by being inserted from an inlet of said opening which has a wider area**. (Ex. 1002, ¶259). However, this would have been obvious. (*Id.*). First, Wakabayashi teaches that the image sensor is bonded to the inner leads. (Ex. 1004, ¶0010). (Ex. 1002, ¶259). As shown in Fig. 1 (annotated below), the inner lead connection is from the (bottom) side of the package with the wider opening, making this the natural opening to use. (Ex. 1002, ¶260).

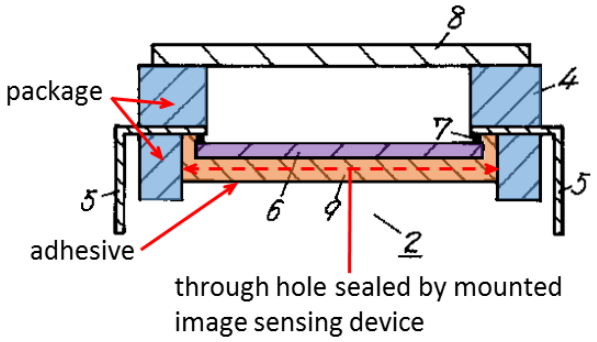


Second, as shown in Fig. 1, the sensor (6) fits into the wider opening, but would not fit (or at best would fit only with difficulty) in the top. (*Id.*). Third, there were only two possibilities for placing the sensor in the package, and one of ordinary skill would have immediately been able to visualize both. (*Id.*). There were no unpredictable results. (*Id.*).

Wakabayashi discloses that mounting **thereby seals the through hole** in the same way as in the '714 patent (*compare* Ex. 1001, Fig. 2) and that the **solid-state image sensing device is secured to said package via an adhesive** ("adhesive resin"), as shown in Wakabayashi's Fig. 2 and in the following passage:

> "FIG. 2 is a cross section of a solid-state image pickup device in which, in addition to the basic structure discussed above, the back face side of the chip is further **sealed with an adhesive resin 7** [sic: 9]. By constructing the device in this way, the bump joints are **reinforced**…." (Ex. 1004, ¶¶0015)(emph. add.)(Ex. 1002, ¶261; ¶¶264-265).

Figure 2 is annotated at right. (Ex. 1002, ¶262). The **adhesive** (highlighted orange) is indicated by the numeral "9". (*Id.*). The above passage refers to "adhesive resin 7" erroneously. (*Id.*). Wakabayashi indicates that "7" indicates the "bump section" or "bumps 7". (Ex. 1004, Explanation of Reference Numerals; Abstract)(Ex. 1002, ¶262). That "9" in Fig. 2 is the adhesive resin is confirmed by the above passage, which states that it seals "the back face side of [CCD] chip [6]". (Ex. 1004, ¶0015)(Ex. 1002, ¶263).



Ground 13. Claims 2-4 are obvious over Wakabayashi in view of Fujii.

Claims 2-4 are unpatentable under pre-AIA 35 U.S.C. § 103(a) over

Wakabayashi in view of Japanese Pat. App. Pub. No. H06-85221 ("Fujii")(Ex. 1024 and Ex. 1025). (Ex. 1002, ¶267).

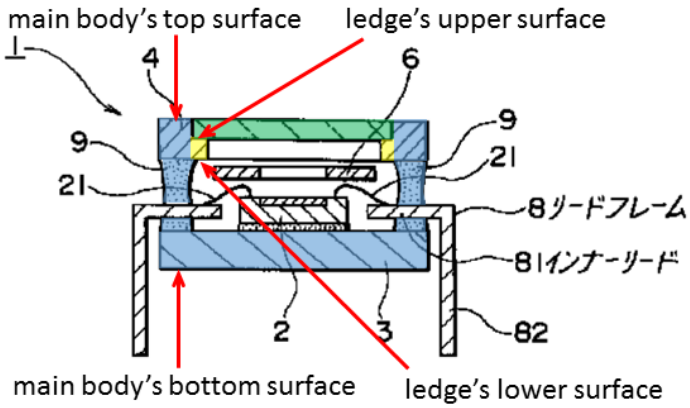
Claim 2. ***[2a] "A solid-state image apparatus comprising:"***

Wakabayashi discloses this. *See* Ground 12, element [1a]. (Ex. 1002, ¶270).

[2b] "a package comprising a main body having a through hole therein, said main body having a top surface and a bottom surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward the center of said through hole, said ledge comprising an upper surface and a lower surface;"

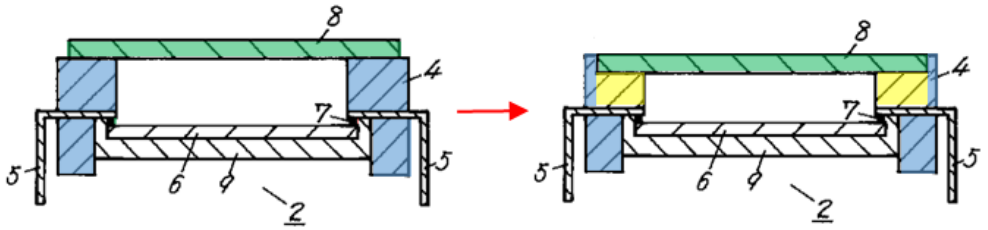
As discussed for Ground 12, element [1a], Wakabayashi discloses a **package having a through hole**. (Ex. 1002, ¶271). Wakabayashi does not explicitly disclose that its package has separate **main body** and **ledge** portions, as recited in element [2a]. (*Id.*). Fujii, however, discloses this. (Ex. 1002, ¶272).

Fujii discloses a package for a "solid-state image sensor 2". (Ex. 1024, ¶0013)(Ex. 1002, ¶272). As shown in Fujii's Fig. 4 (annotated at right), Fujii's **package** (highlighted blue) **comprises a main body having a top surface and a bottom surface** and **a ledge** (yellow) **formed on said main body so as to extend inwardly toward the center** of the package. (Ex. 1002, ¶273). The ledge holds transparent "cap 5" (highlighted green, although the numeral "5" was omitted from



the figure). (Ex. 1024, ¶0010)(Ex. 1002, ¶¶274-275).

It would have been obvious to use Fujii's **ledge** in Wakabayashi's package, such that the ledge **extends inwardly toward the center of said through hole**, as illustrated below using Wakabayashi's Fig. 2. (Ex. 1002, ¶¶276-277).



Wakabayashi Fig. 2

Modified Wakabayashi Fig. 2
(illustrating combination w/ Fujii)

On the right, Petitioner has modified Fig. 2 to show the combination with Fujii, and highlighted the main body portion of the package blue, the ledge yellow, and the transparent lid green. (Ex. 1002, ¶277). Wakabayashi's specification does not indicate what the numeral "8" in Fig. 2 refers to, but, as explained by Mr. Guidash, it is clear that this is a transparent lid, *i.e.*, a "sealing glass", as Wakabayashi recites elsewhere. (Ex. 1004, ¶0002)(Ex. 1002, ¶278).

One of ordinary skill would have known to extend the edge of Wakabayashi's package upward in order to hold Wakabayashi's transparent lid ("sealing glass" 8), creating the ledge disclosed in Fujii. (Ex. 1002, ¶276). This arrangement was a known substitute for a package in which the lid sits on top of the package, with no unpredictable results, and is thus obvious under *KSR v. Teleflex*. (*Id.*).

[2c] "a lead frame comprising inner leads and outer leads, said lead

frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and"

As discussed for Ground 12, element [1c], Wakabayashi discloses **a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package**. (Ex. 1002, ¶279). As shown in the modified version of Wakabayshi's Fig. 2 (shown for element [2b] above), when combined with Fujii's ledge, Wakabayashi's lead frame (5) is sealed in the package such that **said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge**. (*Id.*).

[2d] "a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;"

As discussed for Ground 12, element [1d], Wakabayashi discloses **a solid-state image sensing device** (a "CCD chip"). (Ex. 1002, ¶280). As shown in Fig. 2 (*see* element [2b] above), Wakabayashi's image sensor has **an upper surface and a lower surface**. (Ex. 1002, ¶280). Wakabayashi discloses **a plurality of electrode pads** ("bonding pads", which per the below passage are electrical connection points on the chip) **disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads**:

> "In another aspect, the **joining of the chip to the inner leads** via the bumps **is performed via** the conductive adhesive layer formed on the

> surfaces of the bumps disposed on the **bonding pads of the CCD chip.**" (Ex. 1004, ¶0006)(emph. add.)(Ex. 1002, ¶281).

Fig. 2 (*see* element [2b] above) does not label the bonding pads, but illustrates that the pads are on the **upper surface** of the image sensor, since this is the surface that is joined to the inner leads (5) via bumps (7). (Ex. 1002, ¶282).

> ***[2e] "said solid-state image sensing device being secured to said main body of said package via an adhesive."***

Wakabayashi discloses this. *See* Ground 12, element [1d]. The modified version of Wakabayshi's Fig. 2, shown for element [2b] above, shows that the sensor is secured to the **main body** portion via adhesive (9). (Ex. 1002, ¶283).

> ***Claim 3.*** ***"The solid-state image sensing apparatus of claim 2, wherein each of the electrode pads is connected to the inner lead via a bump."***

Wakabayashi discloses that **each of the electrode pads** ("bonding pads") of the image sensor ("CCD chip") **is connected to the inner lead via a bump**:

> "In another aspect, the **joining of the chip to the inner leads** via the bumps **is performed via** the conductive adhesive layer formed on the surfaces of the **bumps disposed on the bonding pads** of the CCD chip." (Ex. 1004, ¶0006)(emph. add.)(Ex. 1002, ¶285).

> ***Claim 4.*** ***"The solid-state image sensing apparatus of claim 2, wherein each of the electrode pads is connected to the inner lead via an anisotropic conductor having only vertical conductivity."***

As discussed for Ground 6, claim 10, Wakabayashi discloses the connection of **each of the electrode pads to the inner lead** may be made **via an anisotropic**

conductor, obviously **having only vertical conductivity**. (Ex. 1002, ¶287).

Ground 14. Claim 5 is obvious over Wakabayashi in view of Fujii, in further in view of Onishi.

Claim 5 is obvious under pre-AIA § 103(a) over Wakabayshi in view of Fujii, in further view of Onishi. (Ex. 1002, ¶289).

> ***Claim 5.*** ***"The solid-state image sensing apparatus of claim 2, wherein a tip of the inner lead to which the electrode pad is connected extends beyond said ledge."***

Wakabayashi does not expressly disclose that **the tip of the inner lead extends** into the package such that it would extend **beyond said ledge**. (Ex. 1002, ¶290). Fujii, however, does disclose an inwardly extending inner lead, as shown in Fujii's Fig. 4. (*See* Ground 13, element [2b])(Ex. 1002, ¶290). Moreover, as discussed for Ground 7, claim 11, Onishi discloses an inner lead extending into the center of a through hole, in a package very similar to Wakabayashi's. (Ex. 1002, ¶290).

It would have been obvious to use Onishi's or Fujii's extended inner lead with Wakabayashi's package, so that the **tip of the inner lead extends beyond said ledge**. (Ex. 1002, ¶291). This would provide the same advantages discussed for Ground 7, claim 11. (*Id.*). It is also a known variation on a base system (Wakabayashi) that would have led to no unpredictable results, and thus obvious under *KSR v. Teleflex*. (*Id.*).

Ground 15. Claim 13 is obvious over Wakabayashi in view of Hikosaka.

Claim 13 is obvious under pre-AIA 35 U.S.C. § 103(a) over Wakabyashi in

view of Hikosaka. (Ex. 1002, ¶293).

> ***Claim 13. [13a] "A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package, said manufacturing method comprising the steps of:"***

As discussed above for Ground 12, elements [1a]-[1d], Wakabayashi discloses the **solid-state image sensing apparatus** of element [13a]. (Ex. 1002, ¶294). Wakabayashi also describes steps for "construct[ing]" the apparatus—*i.e.*, a **manufacturing method**. (*E.g.*, Ex. 1004, ¶¶0005-007)(Ex. 1002, ¶295).

> ***[13b] "inserting said solid-state image sensing device into said through hole,"***

As discussed for Ground 12, element [1d], this is obvious. (Ex. 1002, ¶296).

> ***[13c] "connecting an electrode pad of the solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device, and"***

Wakabayashi discloses **connecting an electrode pad of the image sensor** ("bonding pads of the CCD chip") **to the inner lead(s) via a bump**:

> "The **bumps are formed on the bonding pads of the CCD chip 6** by stud bumping or plating beforehand, and the **chip is bonded to the inner leads** 5 within the package **via** the conductive layer disposed on **the bump surfaces** by thermosetting or photosetting." (Ex. 1004, ¶0013)(emph. add.)(Ex. 1002, ¶297).

As discussed for Ground 6, claim 10, Wakabayashi also discloses making the connection with **an anisotropic conductor**, obviously one **having only vertical conductivity**. (Ex. 1002, ¶298).

Wakabayashi does not expressly disclose **simultaneously adjusting the optical positioning of said solid-state image sensing device**. (Ex. 1002, ¶299). For the same reasons discussed for Ground 9, element [13c] with regard to Yoshino, this would have been obvious. (*Id.*). For the same reasons discussed there, one of ordinary skill would have understood Wakabayashi's apparatus to suggest **simultaneously adjusting the optical positioning** and would have been motivated to combine Wakabayashi with Hikosaka, with the same predictable, advantageous results. (Ex. 1002, ¶¶299-300). As described by Mr. Guidash, the combination would have been well within ordinary skill. (Ex. 1002, ¶300).

[13d] "securing said solid-state image sensing device to the package with an adhesive."

Wakabayashi discloses this. *See* Ground 14, element [1d]. (Ex. 1002, ¶301).

VI. CONCLUSION

Petitioner respectfully requests that claims 1-13 and 15-16 of the '714 patent be canceled.

Date: April 22, 2016 /Matthew A. Smith/ (RN 49,003)
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing petition for *inter partes* review, together with all exhibits and other documents filed therewith, was served by Federal Express this 22nd day of April 2016, on the Patent Owner's counsel of record at the United States Patent & Trademark Office having the following address:

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON DC 20001

Date: April 22, 2016 /Matthew A. Smith/ (RN 49,003)

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the foregoing petition for inter partes review contains 13,707 words according to the word processing software used to prepare the petition.

Date: April 22, 2016 Signed:/Matthew A. Smith/ R.N. 49,003