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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case IPR2016-00941
U.S. Patent No. 5,952,714

DECLARATION OF MARTIN AFROMOWITZ, PH.D.

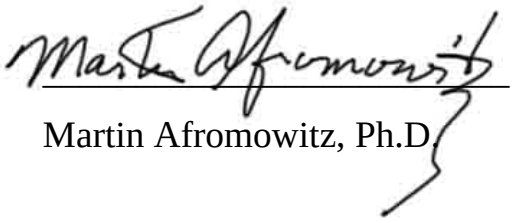
Mail Stop PATENT BOARD
Patent Trial and Appeal Board
U.S. Patent & Trademark Office
P.O. Box 1450

Petition for Inter Partes Review of U.S. Patent No. 5,952,714

Declaration of Martin Afromowitz, Ph.D.

I, Martin Afromowitz, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed January 27, 2017, in Mercer Island, Washington, USA.



Martin Afromowitz, Ph.D.

I. INTRODUCTION

1. The facts set forth below are known to me personally and I have firsthand knowledge of them. I am a United States citizen over eighteen years of age. I am fully competent to testify on the matters in this Declaration. I understand that this Declaration is being submitted along with the Patent Owner's response to the Decision in the Institution of Inter Partes Review ("IPR") by the Patent Trial and Appeal Board ("Board") for U.S. Patent No. 5,952,714 (the "'714 patent") in IPR2016-00941.

A. Engagement

2. I have been hired as a technical expert by counsel for the owner of the '714 patent to study it and certain prior art and provide my opinions on whether that prior art discloses the limitations of the claims of the '714 patent at issue in this IPR proceeding. In particular, I have been asked to review the Declaration of R. Michael Guidash Ex. 1002 ("Guidash Declaration") and provide my opinions about that declaration. Further, I have read the Institution Decision (Paper 6) and understand that the Board has instituted against claims 1–13, 15, and 16 in this IPR on the following fifteen grounds:

(1) claim 1 as anticipated under § 102(b) by Japanese Pat. App. Pub. No. S61-131690 ("Yoshino") (Ex. 1003);

(2) claim 6 as obvious under § 103(a) over Yoshino and Japanese Pat. App. Pub. No. S63-221667 ("Izumi") (Ex. 1016);

(3) claim 7 as obvious under § 103(a) over Yoshino, Japanese Publication No. H06-029507 ("Nagano") (Ex. 1018), and Publication No. H07-045803 ("Wakabayashi") (Ex. 1004);

(4) claim 8 as obvious under § 103(a) over Yoshino, Izumi/Nagano, Publication No. S60-74880 ("Hirosawa") (Ex. 1020), and JP Publication No. H07-78951 ("Nita") (Ex. 1011);

(5) claim 9 as obvious under § 103(a) over Yoshino and Izumi/Nagano;.

(6) claim 10 as obvious under § 103(a) over Yoshino, Izumi/Nagano, and Wakabayashi;

(7) claim 11 as obvious under § 103(a) over Yoshino, Izumi/Nagano, and JP Publication No. H05-006989 ("Onishi");

(8) claim 12 as obvious under § 103(a) over Yoshino and JP Publication No. H05-275611 ("Tobase") (Ex. 1022);

(9) claim 13 as obvious under § 103(a) over Yoshino and JP Publication No. S59-225560 ("Hikosaka") (Ex. 1005);

(10) claim 15 as obvious under § 103(a) over Yoshino, Izumi, Nagano, and Hikosaka;

(11) claim 16 as obvious under § 103(a) over Yoshino, Tobase, and Hikosaka;

(12) claim 1 as obvious under § 103(a) over Wakabayashi;

(13) claims 2–4 as obvious under § 103(a) over Wakabayashi and Fujii;

(14) claim 5 as obvious under § 103(a) over Wakabayashi, JP Publication No. H06-85221 ("Fujii") (Ex. 1014), and JP Publication No. H05-006989 ("Onishi") (Ex. 1014); and

(15) claim 13 as obvious under § 103(a) over Wakabayashi and Hikosaka.

Claims 1, 2, 6, 7, and 12-16 are independent claims.

B. Background and Qualifications

3. In this section, I discuss my educational background, work experience, and other relevant qualifications. A complete list of cases in which I have testified at trial, hearing, or by deposition within the preceding four years is provided in my curriculum vitae, which is attached as Appendix A.

4. At the end of 2015 I retired as the senior professor in the Department of Electrical Engineering at the University of Washington where I had been doing research and teaching since 1974. Prior to my academic career, I was a Member of the Technical Staff at the Murray Hill (NJ) Bell Telephone Laboratories, and worked in the groups developing the first visible light red and green light-emitting diodes (LEDs) and the GaAs heterostructure laser. My work at Bell Labs was primarily involved with materials characterization (optical, thermal, lattice matching, etc.)

5. I have taught both undergraduate and graduate students, including courses in circuits, electricity & magnetism, integrated circuit fabrication, optical fiber theory and applications, semiconductor optical properties and devices, and a

seminar on professional issues (career choices, personal & corporate ethics, and intellectual property.)

6. I hold thirteen patents in the general areas of optical sensors and photolithography. As a consultant to industry, he has worked on optical fiber sensors for acceleration, pressure, temperature, electric field, pH, physical measurements of gases, including flow, thermal conductivity, thermal diffusivity, and viscosity. I also developed an optical fiber sensor for monitoring the curing of thermoset resins. Other research interests include infrared imaging, three-dimensional lithography, microfluidics, and methods for infrared sensing of conditions inside coalfired boilers to improve control and efficiency. As an expert witness, I have supported patent litigation in a range of semiconductor fabrication technologies. For three years, I served as a member of the Board of Directors of Enertechnix, Inc.

7. I have 44 years of experience in microfabrication, sensor systems, and optical devices & applications. I received the NIH Research Career Development Award in 1977 – 1982 and was an inductee into the Space Technology Hall of Fame for my work with an "Accelerometer" in 1999.

C. <u>Compensation</u>

8. I am being compensated for the time I spend on this case at my normal consulting rate of $500 an hour. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this

investigation. My compensation is not contingent upon the outcome of this matter or the substance of my testimony.

D. Summary of Opinions

9. It is my opinion that claims 1-13 and 15-16 are valid. It is of note that the Petitioner had filed fifteen grounds against fifteen claims including separate grounds against most of the dependent claims. Many of the grounds that the Petitioner asserted was using art that provides only one or two cross-sections of a package to highlight a certain feature of that package. Most of these references provide little to no information about the package outside of the description of the cross-section. That is, no information about any other section of the

E. Information Considered and Basis of Opinions Formed

10. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this declaration and those listed in Appendix B.

11. I may rely upon these materials and/or additional materials to respond to arguments raised by the Petitioner. I may also consider additional documents and information in forming any necessary opinions – including documents that may not yet have been provided to me.

12. My analysis of the materials produced in this investigation is ongoing, and I will continue to review any new material as it is provided. This declaration

represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS

13. In expressing my opinions and considering the subject matter of the claims of the ’493 patent, I am relying upon certain basic legal principles that counsel has explained to me.

14. First, I understand that for something to be found patentable, it must be, among other things, new and not obvious from what was known before.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.) that existed before the earliest filing date (the “effective filing date”) of the claim in the patent. I also understand that a patent may be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

16. I set forth my understanding of the anticipation standard as follows: I understand that a claimed invention is not patentable if a prior art reference discloses every element of the claimed invention, either explicitly or inherently and that those elements must be arranged or combined in the same way as the claimed

invention. I further understand that being arranged or combined in the same way does not require an identity of terminology.

17. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art at the time of the invention.

18. I understand that, in this proceeding, Petitioner has the burden of proving that the claims of the '493 patent are rendered obvious in view of the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

19. It is my further understanding that a claimed invention is unpatentable for the reason of obviousness if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

20. I understand that the ultimate conclusion of whether a claim is (non) obvious should be based upon a determination of several factual considerations: (1) Determining the scope and content of the prior art; (2) Ascertaining the differences between the claimed invention and the prior art; and (3) Resolving the level of ordinary skill in the pertinent art. I understand that when considering those factors both the claimed invention and the scope and content of the prior art must be

considered as a whole, including disclosures in the references that diverge from and teach away from the invention at hand. I understand that it is improper to limit the obviousness inquiry to a difference from the prior art and then to show that that difference alone would have been obvious.

21. I understand that the existence of each and every element of the claimed invention in the prior art does not necessarily prove obviousness and that most, if not all, inventions rely on building blocks of prior art. In considering whether a claimed invention is obvious, I understand that one may find obviousness if at the time of the claimed invention there was a reason that would have prompted a person having ordinary skill in the field to combine the known elements in a way the claimed invention does, taking into account such factors as (1) whether the claimed invention was merely the predictable result of using prior art elements according to their known function(s); (2) whether the claimed invention provides an obvious solution to a known problem in the relevant field; (3) whether the prior art teaches or suggests the desirability of combining elements claimed in the invention; (4) whether the prior art teaches away from combining elements in the claimed invention; (5) whether it would have been obvious to try the combinations of elements, such as when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions; and (6) whether the change resulted more from design incentives or other market forces. I understand that to find it rendered the invention obvious, one

must find that the prior art provided a reasonable expectation of success and that each claim must be considered separately.

22. I understand that one should not use hindsight when considering obviousness. I also understand that in assessing obviousness, that one should take into account any objective evidence (sometimes called "secondary considerations") that may have existed at the time of the invention and afterwards that may shed light on the obviousness or not of the claimed invention, such as: (a) Whether the invention was commercially successful as a result of the merits of the claimed invention (rather than the result of design needs or market-pressure advertising or similar activities); (b) Whether the invention satisfied a long-felt need; (c) Whether others had tried and failed to make the invention; (d) Whether others invented the invention at roughly the same time; (e) Whether others copied the invention; (f) Whether there were changes or related technologies or market needs contemporaneous with the invention; (g) Whether the invention achieved unexpected results; (h) Whether others in the field praised the invention; (i) Whether persons having ordinary skill in the art of the invention expressed surprise or disbelief regarding the invention; (j) Whether others sought or obtained rights to the patent from the patent holder; and (k) Whether the inventor proceeded contrary to accepted wisdom in the field.

III. THE ’714 PATENT

A. Effective Filing Date of the ’714 Patent

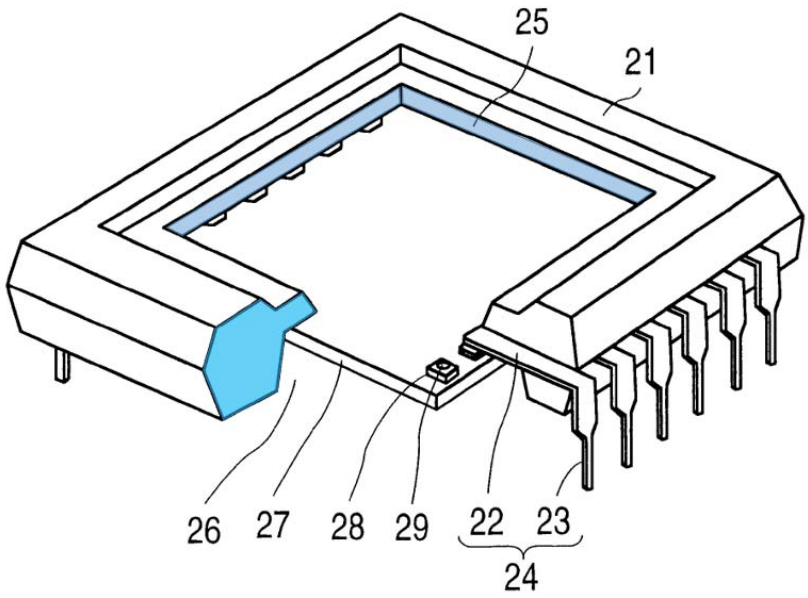
23. I have been told that the ‘714 Patent is currently expired. On its face, the ’714 patent claims priority to (JP) 7-197365 with a priority date of August 2, 1995. For the purpose of this *inter partes* review, I will assume that the priority date for the ’714 patent is its foreign priority date of August 2, 1995.

B. Overview of the ’714 Patent

24. The ’714 patent is drawn to a “solid-state image sensing apparatus” that comprises, among other things, a solid-state image sensor (e.g., a CCD chip). Ex. 1001, Abstract. The package has a through hole with one smaller opening and one wider opening the relative size determined by the *area* of the opening. One novel aspect of the package is the way the image sensor device is precisely positioned into the package via ball bumps to inner leads of the package, the image device is then fixed into place by glue. *Id.* Then a sealant used to fill up the inlet (i.e., wider opening). ’714 Patent, 4:49-63.

25. The process of aligning and securing the chip in a package is called “mount[ing].” *Id.* at 1:42–61. Use of this package allows accurate positioning of the image sensor while permitting a lower profile device than one with conventional wire leads. *Id.* 4:5-12. (“Thus, the present invention can reduce a number of manufacturing processes comparing with the conventional method which requires two bonding processes including the die-bonding of CCD chip and

the wire-bonding of electrode pad. Further, because a loading jig for the CCD chip can be disposed at the back side of CCD chip, the CCD chip can be optically positioned with ease from the front, thus more accurate positioning can be expected.”).



’714 Patent, Fig. 1 (annotated).

C. <u>Claim Construction</u>

26. **Distinction between Molded Resin and Adhesive**

The '714 patent describes the use of both a "molded resin" and an "adhesive" in its embodiments, and uses the term "adhesive" in claims 1, 2, 6, 7, 12, 13, 14, 15, and 16. Claim 7 also uses the term "plastic package." In several locations in the specification, '714 describes how "epoxy resin mixed with inorganic filler is

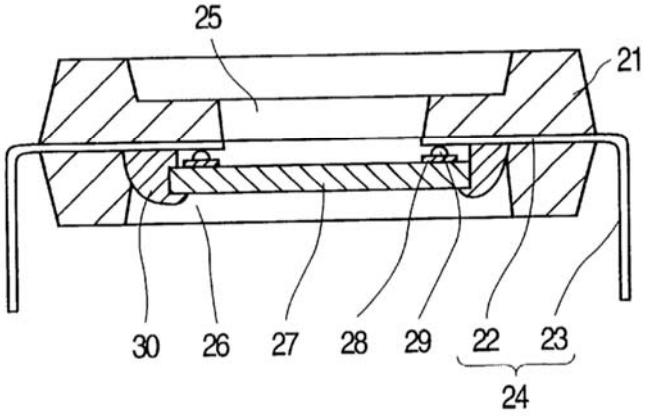
injected into a mold... Then the package ... is taken out from the mold." In addition, the term "adhesive" is found in the specification in the following phrases:

- "a back side of the CCD chip is glued to the package by adhesive."
- "the back side of the substrate... is glued to the package by adhesive."
- "the back side of the peripheral circuit elements is glued to the package by adhesive."
- "ultraviolet hardening adhesive 30 is injected... to glue... the CCD chip... to the package."
- "ultraviolet hardening adhesive 30 is injected... to glue... the peripheral circuit elements... to the package."

Thus, a person of ordinary skill would understand that "molded resin" refers specifically to the material used to fashion the "plastic package," and that "adhesive" is used to glue chips and substrates to the package.

27. A typical application of these materials is shown in FIG. 2 of '714, below, in which the plastic package is labeled 21 and the adhesive is labeled 30.

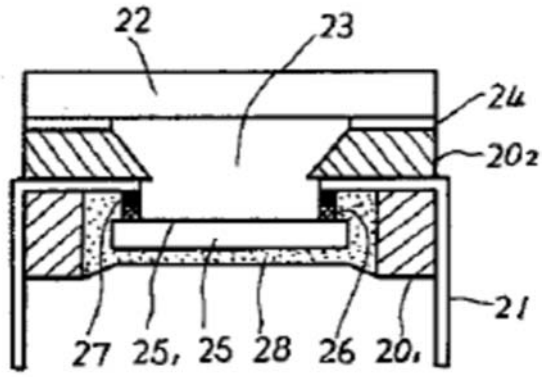
FIG. 2



'714 patent, FIG. 2.

28. Prior art also uses these terms. Yoshino shows FIG. 1, in which "by supporting the solid-state image sensor (25) in the packaging substrate (20) via a molded resin (28), a desired solid- state image pickup device is obtained." (Ex. 1003, page 3)

FIG. 1

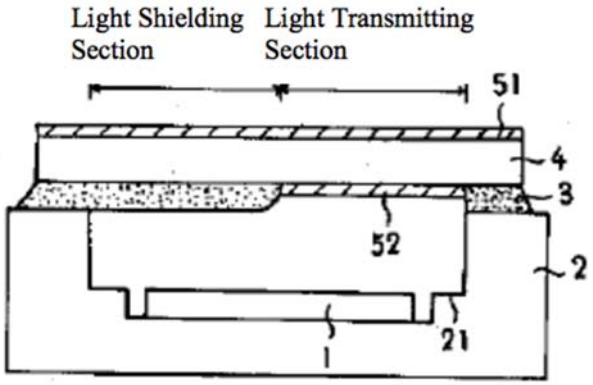


Yoshino, Fig. 1.

29. The bottom of molded resin 28 has inwardly-angled edges and a flat center, which is consistent with its description as a molded structure. This shape contrasts with the rounded, globular shape of the adhesive 30 in the '714 patent.

30. Nita teaches using adhesive in two places in its embodiments. The first is on the back face of the lid, to secure the lid to the package. This is element 3, and this adhesive may also "extend to the section not in contact with the package, and the extended section may be used as a light shielding film." (Ex. 1011, paragraph 0007). In the figure below, Nita also teaches that "chip 1 is secured to the bottom face of the package using an adhesive." (Ex. 1011, paragraph 15). However, this last application may be dispensed with because it is disclosed as prior art (FIG. 10) in '714.

FIG. 3



Nina, Fig. 10.

31. There are significant differences between an adhesive and a molded resin in the manner in which they are applied and in their intended applications. Patent '714 describes the use of adhesive exclusively to glue parts to the package.

"Gluing" is a formless process, in which the adhesive flows under forces of gravity, surface tension, and geometry. On the other hand, a molding process requires that a thermoplastic or thermosetting material be injected into a mold or form and pressed into a desired shape. This injection or pressing operation forces flow of the viscous resin encapsulant, and if used around wire-bonded chips, for example, can cause wire sweep (the displacement and deformation of wire loop during the encapsulant flow), resulting in shorts, and other deformations, including unintended movement of the chip. (Encapsulation Technologies for Electronic Applications by Haleh Ardebili and Michael Pecht, Elsevier, 2009, page 236, and Semiconductor Packaging Assembly Technology, National Semiconductor, August 1999, MS011800, http://focus.ti.com/en/download/qlty/SEMICONDUCTOR_PACKAGING_ASSEMBLY_TECHNOLOGY-MISC.pdf)

32. Adhesive attachment, or gluing, would not include the use of injection molding or any of the other molding methods, such as reaction-injection, compression or transfer molding. A person of ordinary skill in the art would not have understood a molded resin used in this way to constitute an "adhesive." In the 42 years that I have been involved in the semiconductor field, I have never heard a molded resin referred to as an adhesive. Chips are often secured to substrates using materials referred to commonly as die attach adhesives, which are often electrically and/or thermally conductive. The gluing process described in '714 is generally

benign, and permits chips and substrates to be moved about in the package so that electrical contact and optical positioning can be achieved before the adhesive hardens. "During this press-fit operation, a position signal is feedbacked from a optical position adjusting device (not shown) disposed in front of the CCD chip 27 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 27 and disposing the CCD chip 27 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the package 21, and finally, the CCD chip 27 is accurately mounted to the package 21." (Ex. 1001, 5:12-22) All embodiments are similarly positioned and glued. A molding process would not permit that flexibility in positioning, since the mold would necessarily enclose the molding resin and the chips.

IV. Analysis

A. Analysis of First Ground: Claim 1 as anticipated over Yoshino

Claim 1 is reproduced below:

1. A solid-state image sensing apparatus comprising:

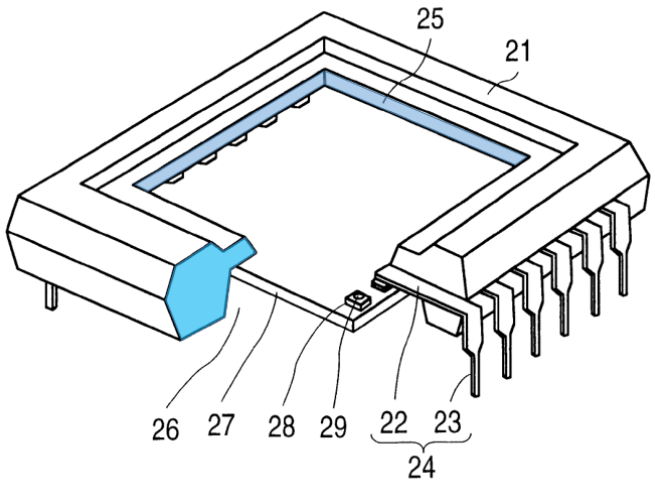
a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and

a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole,

said solid-state image sensing device being secured to said package via an adhesive.

It is my opinion that Yoshino lacks *a package having a through hole therein, openings on both end faces thereof, and <u>different opening areas</u> of said openings*.



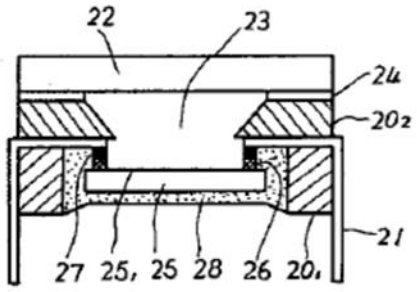
33. The relative areas of the openings are shown in FIG. 1 of '714, reproduced below:

As FIG. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a <u>smaller opening area</u> is situated, and another opening 26 (hereinafter called "inlet" which has a <u>wider opening area</u> is situated at the back side thereof. ('714 Patent at 4:53-58).

34. On the other hand, Yoshino does not address the relative areas of the openings of its package, nor does it provide any information about the length dimensions of its openings or indeed if any other openings exist. Figure 1 of Yoshino, which is used by Petitioner to assert that the lower opening has a wider area, is shown below:

35. Of course, the figure shows only one cross-section of the device. In order for Petitioner, or Mr. Guidash, to assert that the lower opening has a larger *area* than the upper opening, Petitioner must first show that the openings have a particular shape, and that this particular cross-section is representative of a particular feature of that shape. This analysis was not done. For example, if the Petitioner had alleged that the openings were round, then the cross-section might indicate the diameter of the round opening. However, if the openings were alleged to be square, it is not obvious that the cross-section represents the side of the square as opposed to some other cross-sectional view. If the openings were

FIG. 1



rectangular, it is not obvious that the openings represent either the shorter length of the rectangle, the longer length, or some other cross-sectional view. Just as it is

common knowledge that manhole openings and covers are made round so that the cover cannot fall through the hole, so it is true that a square or rectangular opening can accommodate a square or rectangular chip inserted diagonally. The diagonal dimension of a square or rectangular opening, by the Pythagorean Theorem, is larger than the length or width of a square or rectangular chip of the same size, or even of a chip of somewhat larger size. Thus, Petitioner's assertion, that Yoshino discloses a device inserted from an opening which has a wider area, is clearly false. Yoshino FIG. 1 shows only a cross-section, whereas '714 FIG. 1 shows relative area, via an isometric projection. The teachings of these two figures are not the same.

36. It is further my opinion that Yoshino lacks a *solid-state image sensing device being secured to said package via an adhesive*. Yoshino recites "by supporting the solid-state image sensor (25) in the packaging substrate (20) via a molded resin (28), a desired solid- state image pickup device is obtained." (Ex. 1003, page 3). Yoshino does not teach how the imaging device is secured. Yoshino's device is "supported" by a molded resin. Also, as discussed above in the section entitled, Distinction between Molded Resin and Adhesive, a molding operation is not the same as securing with an adhesive. Yoshino shows that a molded resin fills the molded cavity surrounding the chip. One of ordinary skill would not understand the molded resin of Yoshino to disclose the adhesive of '714.

B. Analysis of Second Ground: Claim 6 as obvious over Yoshino and Izumi

Claim 6 is reproduced below:

6. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,

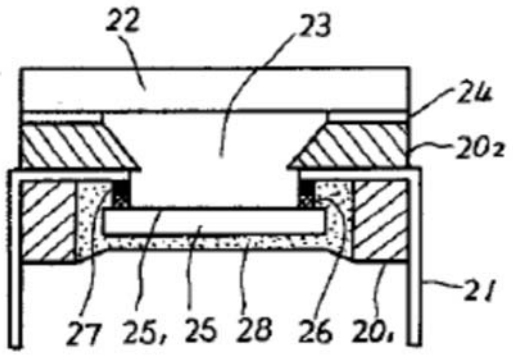
a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted being inserted into the package from a wider opening thereof, and

an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,

said substrate being secured to said package via an adhesive.

37. Figure 1 of Yoshino is shown below:

FIG. 1



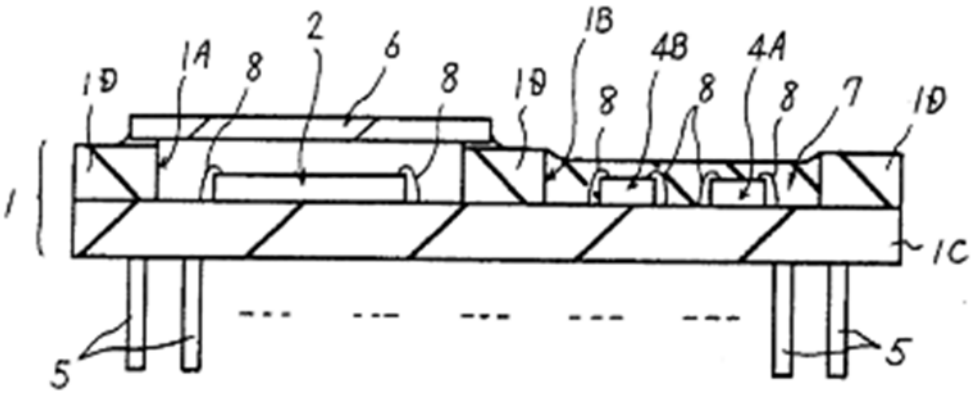
38. Yoshino, as discussed above with regard to claim 1, lacks a package having a through hole therein, openings on both end faces thereof, and *different opening areas of said openings*. My arguments regarding this limitation in claim 1 also apply here.

39. Yoshino further teaches that element 25, a solid state image sensor, is *supported* in the package via a molded resin 28, but does not disclose a substrate being *secured to said package via an adhesive*.

40. Petitioner asserts that claim 6 is rendered obvious by combining Izumi with Yoshino. Specifically, Petitioner concludes that one of ordinary skill "would have been motivated to use the substrate (and package divider) disclosed in Izumi with Yoshino's package." Pet 21-22. Figure 2 of Izumi is reproduced below.

41. It has to be assumed that Petitioner does not intend that *only* the substrate and package divider disclosed in Izumi is to be used, since those elements

do not include the image sensor and peripheral circuit chips. I expand the definition of substrate to include these essential elements.



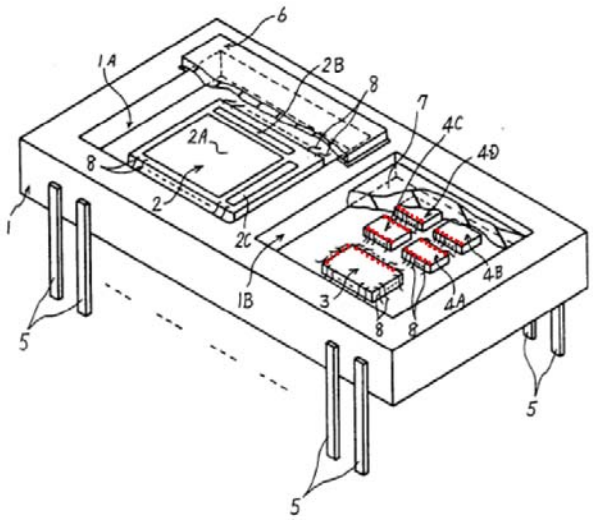
42. Izumi's substrate, 1C consists of solid state imaging element chip 2, positioned so as to be located in the left-hand cavity of the package, and peripheral circuit chips 4A and 4B, positioned so as to be located in the right-hand cavity of the package. The package divider does not appear to be part of the substrate as the diagonal shading in that element 1B matches the shading of the package 1D. The chips are wire-bonded to the top of the substrate. We also note that leads 5 extend from the underside of the substrate 1C and are fixed to the substrate. Izumi's substrate includes all these elements. Furthermore, Izumi's substrate is not "inserted into the package from a wider opening thereof" but is attached under the package, and Izumi's peripheral chips, located in a separate cavity (for which Izumi has several good reasons) provide an additional complication, to be discussed below.

43. Although Izumi teaches a substrate on which a solid-state image sensing device is positioned so as to be located in the left-hand cavity of the package, and peripheral circuit chips are positioned so as to be located in the right-hand cavity of the package, it is my opinion that a person of ordinary skill would not be motivated to use Izumi's substrate with Yoshino. A major difficulty with Izumi is that the image sensing device must be bonded to the substrate prior to wire-bonding the contacts to the chip. The position of the image sensor chip is thus fixed with respect to the position of the pins before one could establish whether its optical position is correct. Izumi's pins locate the package on a circuit board, so the location of the image sensor chip, mounted in this way on a substrate, is fixed with respect to the circuit board. This design goes against a principal advantage of the '714 invention, that is, the image sensor chip can be moved about in its package, while it is actively operating, to secure proper alignment of the chip with respect to its pins, prior to being locked in place with an adhesive. "The electrode pad disposed around the upper surface of the substrate is connected to the inner lead via the 25 bump or anisotropic conductor so that the optical positioning as well as electrical connection is completed." (3:24-27)

44. To counter this defect in the combination of Yoshino and Izumi, Petitioner also suggests that Izumi's substrate could be modified so that the electrical wiring on the top surface of the substrate would connect the chips to

electrode pads instead of to the pins so that the chips could then connect to the inner leads of the lead frame in Yoshino.

45. Izumi's substrate and package structure are so different from the teachings of '714, that I submit that the modifications required of Izumi's substrate are extreme, and the combination of such a modified substrate with the teachings of Yoshino would not be obvious to a person of ordinary skill. Petitioner fails to describe the proposed modifications with any reasonable detail. I am skeptical that such a modification is possible much less obvious to a person having ordinary skill in the art. For instance, referring to Figure 1 below, how would the inner most bond pads connect to the inner leads of Yoshino? Yoshino's inner leads overhang the substrate from the edge of the package. Even if Yoshino's metal inner leads could be formed with a small enough pitch to permit the number of lead frame contacts to match the number of bond pads required from Izumi's peripheral circuit chips 3, 4A-4D, how would Yoshino's inner leads reach Izumi's bond pads (general positions highlighted in red) that are not facing the exterior of the package?



46. Petitioner apparently only considered Izumi's cross-section in Figure 2 in coming to its analysis. The reasons to modify Izumi simply do not exist when considering the actual device. It is therefore my opinion that claim 6 is not obvious over Yoshino and Izumi.

C. Analysis of Third Ground: Claim 7 as obvious over Yoshino, Nagano and Wakabayashi

Claim 7 is reproduced below:

7. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,

a semiconductor substrate having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof, said semiconductor

substrate being inserted into a plastic package via the larger of two openings formed in said package, and

an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around the smaller opening of said package,

said semiconductor substrate being secured to said package via an adhesive.

47. Yoshino has the first two limitations of this claim, viz., a package and a lead frame. However, Yoshino does not have the semiconductor substrate with all its required elements.

48. Petitioner asserts that Nagano and Wakabayashi teach these elements, and that a person of ordinary skill would be motivated to combine all these elements. I disagree. Wakabayashi teaches a device very similar to that of Yoshino, but adds a plastic package. I accept as reasonable that a person of ordinary skill would be motivated to adopt that element. That is the only contribution to obviousness cited by the Petitioner that comes from Wakabayashi.

49. Nagano, on the other hand, is a very different matter, and it is my opinion that a person of ordinary skill would have no reason to even be aware of Nagano. In particular, a person of ordinary skill would have not have reason to combine Nagano with Yoshino and Wakabayashi.

50. In the first place, Nagano does not have anything to do with an image sensor, and the Petitioner, and their expert Guidash, have asserted that Nagano

discloses a solid-state image sensing device (Pet. p. 26, and Ex. 1002 ¶147) when the fact is that Nagano does nothing of the sort.

51. As evidence for the absence of an image sensing device in Nagano, I submit the following:

1. The title of Nagano's invention is "Photodiode with Computing Function."

2. The purpose of the invention (see Abstract) is "to realize a photodiode with a computing function that has the merits that it is compact and resistant to electrical noise, and furthermore which has a low cost of changes to the shape of its light-receiving part.

3. Nagano states, "the light-receiving part 2 may be circular or rhomboidal instead of rectangular" (paragraph 0009). I challenge the Petitioner to come up with an image sensor whose shape is circular or rhomboidal.

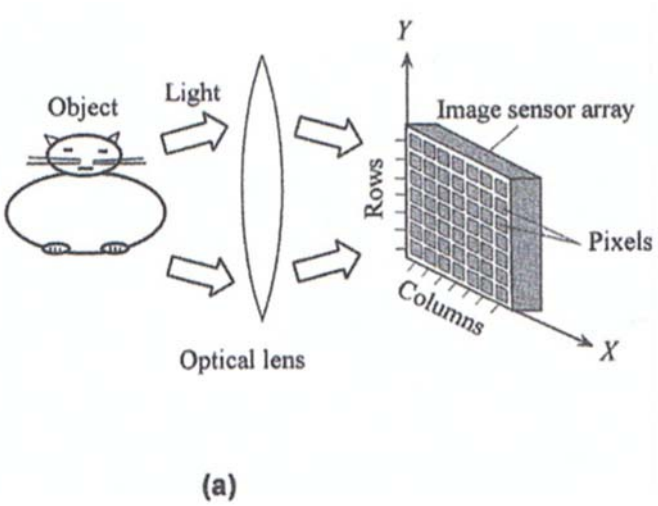
4. Nagano cites a prior art example of a photodiode with a computing function as a "PDIC" (photodiode integrated circuit) article "Thin Optical Pickup with Optical Train Including Semiconductor Laser Mounted on an Actuator." This PDIC is clearly not an image sensor.

5. The word "image" does not appear in Nagano.

52. Guidash asserts in his third deposition rough ASCII p. 61), "I would not agree that in a broad sense that an image sensor would have to contain more than one photodiode or more than one pixel." And on page 63: " A single element of a device that has a single element photo detector, meaning an element that is

used to measure the amount of light incident on that sensor and determine information in a system that is based on the amount of light hitting that sensor incident from the intended thing to be examined, would be -- could be considered an image sensor."

53. It is my opinion that a person of ordinary skill would not agree with Guidash on this point. For example, in the textbook *Optoelectronics and Photonics: Principles and Practices*, by S. O. Kasap, 2nd Edition, published by Pearson, 2013, one finds the following definition of "image sensor" on page 415: "An image sensor, as illustrated in Figure 5.33 (a), is an integrated circuit chip made up of an array of photosensitive elements, that is able to capture an image and provide an output in the form of an electrical signal such as current, charge, or voltage... The sensor usually consists of an array of elements, called **pixels** (*pixel* from "picture element"), in *N* rows and *M* columns, where each element or pixel has a detector and is able to provide an electrical signal that is proportional to the light intensity at the *X,Y* location."



54. Figure 5.33 (a) referred to above is shown below:

55. Although "image sensor" or "image sensing apparatus" has not been construed, its ordinary and customary meaning in the context of the patent and at the time of invention is clear. A person or ordinary skill, according to Guidash (Ex. 1002, ¶¶ 53-54), "would have had a Bachelor’s degree in electrical engineering, physics, or material science and approximately 3-5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience... The person of ordinary skill in the relevant time frame would have been familiar with solid-state image sensing devices, including CCD type solid-state image sensing devices."

56. Technical product brochures describing image sensors of the period give a good idea of what a person of ordinary skill would have understood an

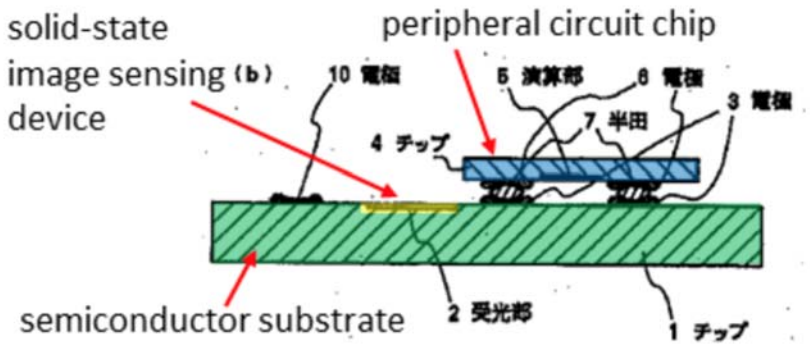
image sensor to be. Sony, for example, released the DSC-F505 Cyber-shot CCD camera in 1999, the issue year of '714. A picture of the camera and Sony's description is reproduced below:

DSC-F505 Cyber-shot
Product Design

57. *The way the large-aperture Carl Zeiss "Vario-Sonnar" lens dominates this camera represents unprecedented, bold design. In fact, the lens barrel can be considered an integral part of the camera design; the CCD image sensor, main circuits, and other primary camera components are actually built into the lens. The shape is unimaginable with conventional film cameras, and it created waves in the digital camera market at launch. Offering a 5x optical zoom and 2 megapixel resolution, this model also heralded the dawn of the megapixel age.*

58. Guidash has presented no evidence that a person of ordinary skill would have agreed with Guidash that an image sensor would *not* have to contain more than one photodiode or more than one pixel.

59. As Nagano is not related to image sensor technology, it is my opinion that a person of ordinary skill in the art of image sensor design and manufacture would not venture to review literature in an entirely distinct and unrelated field. This is my first objection to the obviousness of combining Nagano with Yoshino and Wakabayashi.



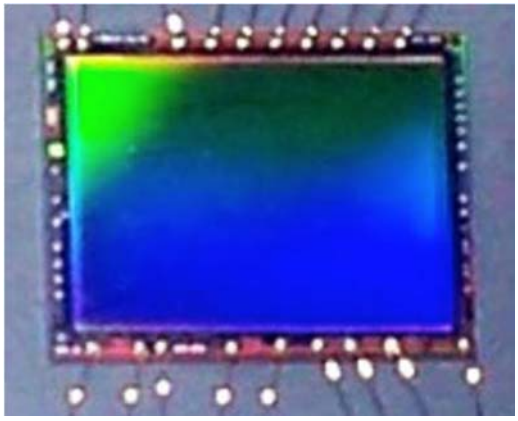
60. Whether or not a person of ordinary skill in the art would consider Nagano required reading, Petitioner asserts that a person of ordinary skill would have been motivated to use the semiconductor substrate disclosed in Nagano with Yoshino's package (Pet p.27). Petitioner selects the following figure from Nagano (to which highlights, red arrows and associated annotations have been added by Petitioner) and quotes Nagano describing this device:

61. “A photodiode with a computing function according to this embodiment example has electrodes 3 of a chip 1 having a light- receiving part 2 and electrodes 6 of a chip 4 having a computing part 5 fixed together with solder 7 with the electrodes facing each other. An optical signal picked up by the light-receiving part 2 of the chip 1 is converted into an electrical signal, passes through the solder 7, is operated upon in the computing part 5 of the chip 4, and passes through the solder 7 again and returns to the chip 1. And, a photodiode with a computing function according to this embodiment example is connected to another circuit by electrodes 10.” (Ex. 1018, ¶ 0008).

62. Clearly, Nagano has not identified the photodiode (also identified by Nagano as the light-receiving part 2) as the claimed image sensor. The annotations of this figure are misleading. None of the other figures shown in Nagano look remotely like an image sensor with a peripheral circuit attached. In particular, the number of leads and contacts shown are small. An image sensor has many contacts around its periphery for timing signals, power and signal extraction. Nothing of the sort is shown in Nagano's figures. There is no mention of CCD or CMOS. Nagano's invention is a simple photodiode integrated circuit that can accommodate photodiode chips of rectangular, circular or rhomboidal shape. Even if the claims of the ’714 patent were amenable to the Broadest Reasonable Interpretation, a person having ordinary skill in the art would not have found the disclosure of a

device having a single photodetecting element to serve as disclosure of an “image” sensor. It would be an unreasonably broad read on the claim limitation.

63. The following figure shows a typical 2 megapixel CCD chip produced by Hewlett Packard at about the same time frame as the '714 patent. The large number of contact pads around the chip is obvious.



HP 2.1 Megapixel CCD

64. Additionally, Petitioner claims its motivation to combine Nagano with Yoshino are identical to the reasons Petitioner had for combining Izumi. “One of ordinary skill would have been motivated to use the semiconductor substrate disclosed in Nagano with Yoshino’s package for the same reasons and with the same results as described for Ground 2, element [6d] with regard to Izumi (namely, to reduce the length of electrical connections, reduce noise, and reduce size).” Pet. at 27. This motivation is nonsensical. Nagano discloses no wire bonds that would make use of Yoshino’s package device advantageous. Furthermore, Petitioner fails to explain why Yoshino would benefit from the simple “computing part” of

Nagano which processes the signal from a single photodiode. In short, Nagano does not disclose the claimed "semiconductor substrate having a solid-state image sensing device." Moreover, even if the single photodiode of Nagano and its rudimentary "computing part" were to be construed as disclosing the claimed "solid-state image sensing device and a peripheral circuit chip," a person having ordinary skill in the art would have had no motivation to combine these disparate references.

65. It is therefore my opinion that a person of ordinary skill in the art of image sensors would not be motivated to use the semiconductor substrate disclosed in Nagano with Yoshino's package.

66. Therefore, it is my opinion that claim 7 is not obvious over Yoshino, Nagano and Wakabayashi.

D. Analysis of Fourth Ground: Claim 8 as obvious over Yoshino, Izumi/Nagano, Hirosawa, and Nita

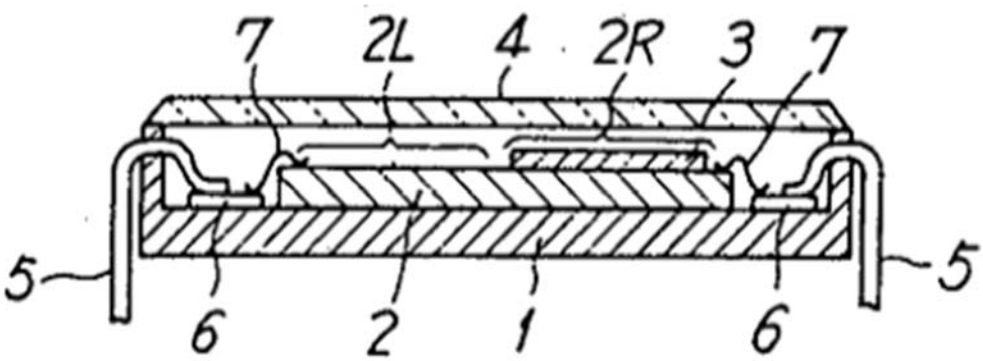
67.

Claim 8 is reproduced below:

8**.** The solid state image sensing apparatus of claim 6 or claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device.

68. The new element in claim 8 is the shading film. Petitioner asserts that Hirosawa and Nita have light shielding films as described in claim 8. I disagree.

69. Hirosawa teaches that a light detection semiconductor element and a signal processing circuit element can be configured either on a single chip or on a plurality of chips. The case of a single chip is relevant here. Hirosawa shows this case in figure 1, below.



70. In this figure, the region 2L denotes a light detection element, and region 2R denotes a signal processing circuit element (Ex 1020, p. 003). On the same page, Hirosawa states, "The light-shielding film or a light-shielding plate 8 is provided to the section 2R where the signal processing circuit element is formed (I agree with the Petitioner that there is an apparent error in the figure, and element 3 should have been written 8.) Further on, Hirosawa states, "Transmission and reception of signals between the light detection semiconductor element and the signal processing circuit element is done via semiconductor regions or conductor patterns." Since the transmission means must extend to the light detection element, they are not part of the signal processing element. They would be in between those two elements. Hirosawa does not indicate that these signal transmission means are

also covered by the light shield. In fact, if they were semiconductor regions, it would be especially important that they be covered. Guidash confirms this in his deposition (Guidash Depo. 38:7-10):

"Q. What kind of circuits would be sensitive to light?

A. So in general, all circuits will be -- that are built in silicon."

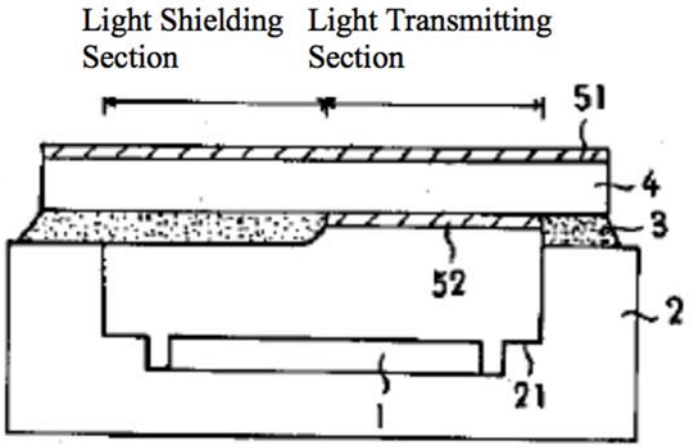
71. Hirosawa also does not indicate that the contact pads around the edges of the device are covered with a light shield. They are not part of the signal processing element either. One can see from the figure above that the contact areas are highly reflective. Guidash specifically notes that it is important to cover these areas with a light shield:

72. "it's important to have shielding over areas that are sensitive to photons. It's important to have shielding over areas that may reflect light that was not intended for being incident on the image array. (These) are two examples of the regions that are desired to be shielded." (rough draft day 3 p. 40) Thus, Hirosawa does not teach that "a shading film covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device." Hirosawa does not make the covered region inclusive enough.

73. Nita teaches an image sensor in a package. "The solid-state image sensor comprises, for example, a silicon semiconductor substrate in which a CCD, including a drive circuit, (chip) is formed" (Ex. 1011, ¶ 0009). Nita refers to an

example image sensor as a frame transfer CCD. "Light enters the light receiving section, and the signal charges are accumulated. The charges are then transferred to the light shielded storage section (Ex. 1011, ¶ 0016). The light shielding of the storage section is accomplished by spreading an adhesive over part of the underside of a cover glass, as shown below:

FIG. 3



74. The adhesive layer (3) on the glass lid is also meant to extend over the lower surface of the cover glass 4 in the stippled area. This light shield does not cover "an entire upper surface of said substrate except an upper surface of the solid-state image sensing device." Because of the open space between the chip and the adhesive layer, light entering at a slight angle away from the vertical can impinge on many parts of the chip that the inventor would have liked to shield from the light. This is a very crude attempt to keep light away from the parts of the chip other than the surface of the image sensing region.

75. Guidash describes a similar problem in his deposition: "The image sensor in that particular package had has *[sic]* end wire disposed in a part of the package that typically sensors of this type were not disposed in. Light would hit the portions of the wire bonds, would be reflected up to the cover glass, reflected back down, reflected off of the wire bond or ball bond in many directions and end up being incident on the imaging array." (Guidash Depo. 43:11-44:6.)

76. These problems would have been eliminated by the teaching of claim 8, whose light shield covers "an entire upper surface of said substrate except an upper surface of the solid-state image sensing device." Neither Hirosawa nor Nita provide the light-shielding solution provided by claim 8.

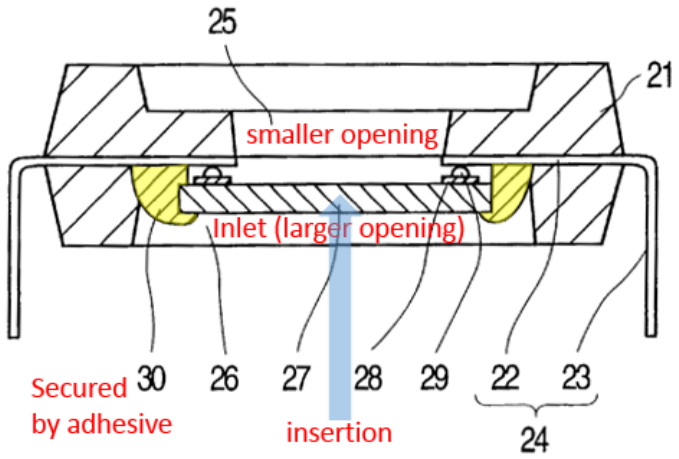
77. Thus, it is my opinion that for these reasons, claim 8 is not obvious over Hirosawa and Nita.

E. <u>Analysis of Twelfth Ground: Claim 1 as obvious over Wakabayashi</u>

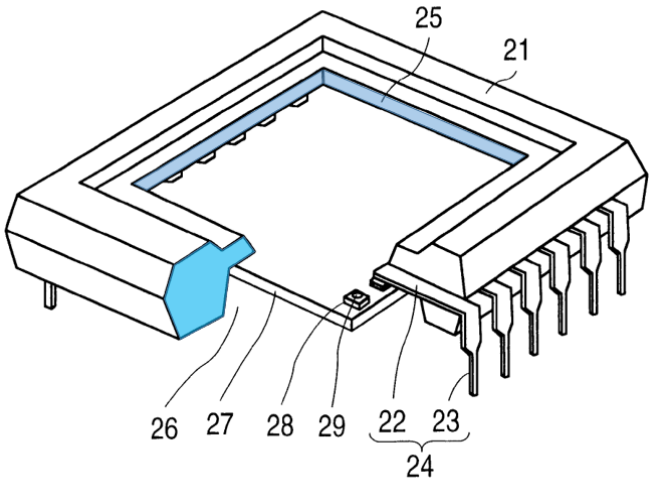
78. Petitioner states that this ground "is presented under § 103 because Wakabayashi does not expressly recite that the image sensor is inserted into package's wider opening." Pet. at 49-50. However, like Yoshino this ground under Wakabayashi fails for the same reasons as Ground 1 with respect to claim 1.

79. Specifically, Wakabayashi does not disclose "a solid-state image sensing *device mounted in said package by being inserted from an inlet of said opening which has a* ***wider area***, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive." '714

Patent at 9:20-30. Claim 1 addresses specifically, that the **area** of the smaller opening is smaller than the **area** of the wider opening. Claim 1 is embodied in at least Figure 2 of the ’714 Patent annotated below:



80. The relative areas of the openings can be seen with respect to Figure 1 of the ’714 Patent:



81. ’714 Patent, Fig. 1 (annotated). As can be readily seen, and as described in the specification, opening 26 has the wider opening area and opening 25 has the smaller opening area.

82. As FIG. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a smaller opening area is situated, and another opening 26 (hereinafter called “inlet” which has a wider opening area is situated at the back side thereof.

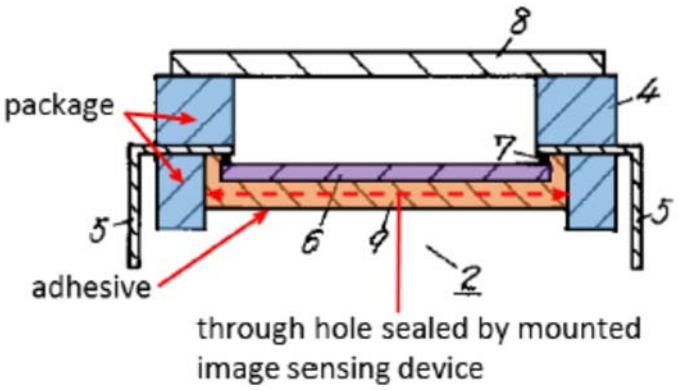
’714 Patent at 4:53-58.

83. Petitioner refers to this element as belonging to limitation [1d]. Pet. at 51-52. Again, Petitioner provides no argument or evidence about the relative area of the openings of its through hole. Again, Petitioner reads too much into the package cross sections provided by the reference. Wakabayashi provides no information about its ends, the structure of its leadframe, e.g., are the leads provided on two sides of the die or all four sides, the pitch between leads, whether the package is designed for multiple substrates, etc. Wakabayashi also indicates that the shape of the openings can change. Wakabayashi at ¶0012 (“In the package 4, the resin thicknesses of the light-receiving section and the side wall sections can be selected to form desirable shapes from the perspective of the optical characteristics and mechanical strength.”). In short, without another view of the device or more information, Wakabayashi provides no information regarding the relative areas of the package through holes.

84. Petitioner's entire treatment of the relative areas of the through-hole openings is the following:

Wakabayashi does not expressly disclose that the image sensor is mounted by being inserted from an inlet of said opening which has a wider area. (Ex. 1002, ¶259). However, this would have been obvious. (Id.). First, Wakabayashi teaches that the image sensor is bonded to the inner leads. (Ex. 1004, ¶0010). (Ex. 1002, ¶259). As shown in Fig. 1 (annotated below), the inner lead connection is from the (bottom) side of the package with the wider opening, making this the natural opening to use. (Ex. 1002, ¶260). Second, as shown in Fig. 1, the sensor (6) fits into the wider opening, but would not fit (or at best would fit only with difficulty) in the top. (Id.). Third, there were only two possibilities for placing the sensor in the package, and one of ordinary skill would have immediately been able to visualize both. (Id.). There were no unpredictable results. (Id.) (Pet. at 52.)

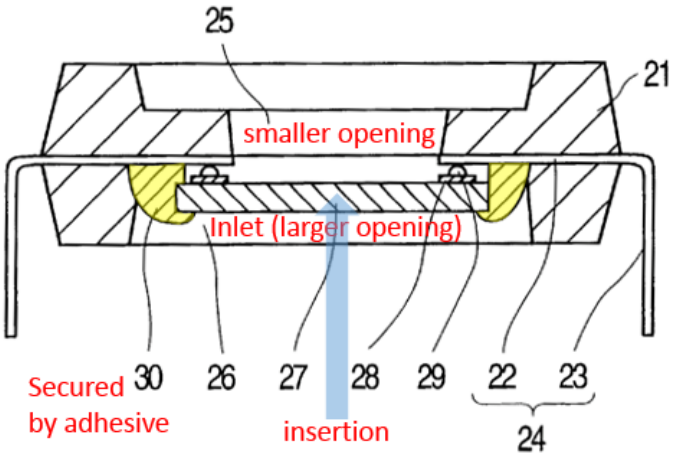
85. From the arguments above and the annotated figure (reproduced below), it appears that Petitioner addresses the width of the opening at the specific cross-section of the device provided by Wakabayashi, and does not address the opening's area at all.



86. Another limitation of claim 1 is underlined below:

a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state *image sensing device being secured to said package via an adhesive*. ('714 Patent at 9:20-30.)

Claim 1 is embodied in at least Figure 2 of the '714 Patent annotated below:

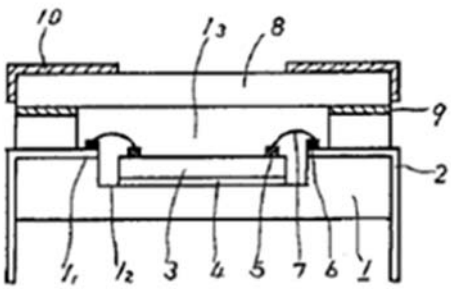


87. The securing of the solid state image sensing device via an adhesive 30 can be seen with respect to Figure 2. As indicated by the adhesive 30 highlighted in Figure 2, the image sensing device is glued into place inside the inlet cavity 26.

88. In contrast, Wakabayashi, does not glue or "secure" the imaging device to the package except in perhaps an unreasonably broad sense. *See* Pet. at 53 (identifying element 9 as the adhesive). One having ordinary skill in the art would understand that the adhesive resin used to fill in the bottom opening e.g., in Wakabayashi's claim 2 is simply a sealant for the back side of the device. However this material is not used to glue or secure the CCD to the package. As Wakabayashi states, it is used to "reinforce" the bump joints and prevent "the penetration of dust from the outside." Wakabayashi at ¶0015. A person having ordinary skill in the art would not have understood the sealant used in this way to constitute "gluing an adhesive."

89. Consistent with this construction, Yoshino (shown below) uses the term "secured . . . via a conductive adhesive" when referring to its background art. Yoshino at 002 ("A solid-state image sensor (3) having a photoelectric conversion function is *secured on the bottom section (1_2) via a conductive adhesive (4)*" (emphasis added)).

FIG. 2



90. Yoshino, Fig. 2. Showing how its imaging device 3 is "secured" via an "adhesive 4" in the prior art.

91. According to Patent Owner's proposed claim construction for "securing to said package via an adhesive" is "gluing with an adhesive." Patent Owner notes that Wakabayashi does not glue the imaging device to the package as Wakabayashi simply fills the molded cavity with resin. Moreover, one having ordinary skill in the art would not understand Wakabayashi resin to disclose the claimed "adhesive."

F. Analysis of Thirteenth Ground: Claims 2 – 4 as obvious over Wakabayashi and Fujii

92.

Claim 2 is reproduced below:

2. A solid-state image apparatus comprising:

a package comprising a main body having a through hole therein, said main body having a top surface and a bottom surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward

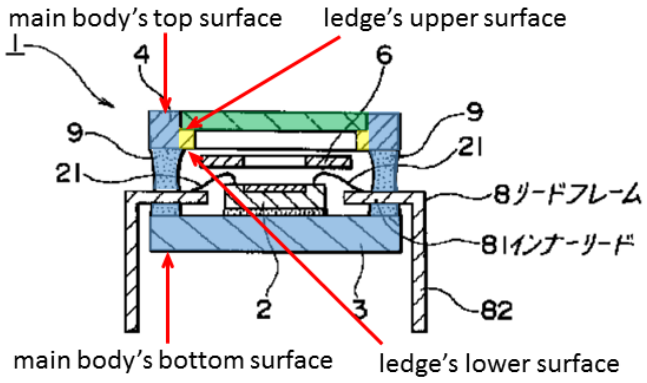
the center of said through hole, said ledge comprising an upper surface and a lower surface;

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and

a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;

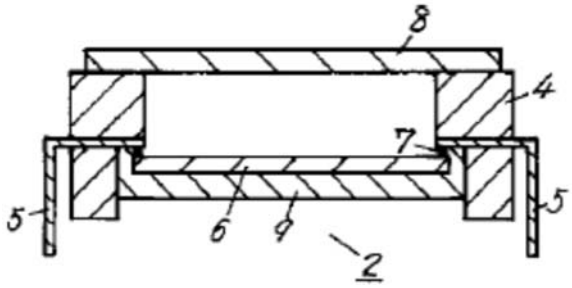
said solid-state image sensing device being secured to said main body of said package via an adhesive.

93. Petitioner cites the following figure from Fujii in support of this ground.



94. Petitioner has modified this figure with annotation and shading. A key element of this figure is the ledge, shaded yellow, having the indicated upper and lower surfaces. Petitioner asserts that this single element could be used in a

modified package taught by Wakabayashi, whose original figure in displayed below:



95. We see that Wakabayashi places a sealing glass 8 on the top surface of the package, whereas Fujii's ledge permits the sealing glass in that design to rest on the upper surface of the ledge. Petitioner gives no reason to combine Fujii's ledge with Wakabayashi's package in this manner. Fujii makes no claim as to an improvement offered by his ledge design, so a person of ordinary skill would not be motivated to combine the ledge element from Fujii with the package of Wakabayashi. It is merely an equivalent alternate design.

Thus, it is my opinion that claim 2 is not obvious over Wakabayashi and Fujii.

96.

G. Analysis of Fifteenth Ground: Claim 13 as obvious over Wakabayashi and Hikosaka

97. Petitioner relies on its analysis of Wakabayashi with respect to claim limitations [1d] in order to show disclosure of limitations [13d]. Therefore, for at

least the reasons provided with respect to claim limitation [1d], it is my opinion that this limitation has not been shown and is therefore non-obvious.

98. I further understand that the scope of claims are not determined solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. Additionally, I understand that the words of the claim must be given their plain meaning, unless the plain meaning is inconsistent with the specification. I understand that the plain meaning of a term means the ordinary and customary meaning given to the term by those of ordinary skill in the art at the time of the invention. I understand that the ordinary and customary meaning of a term may be evidenced by a variety of sources, including the words of the claims themselves, the specification, drawings, and prior art.

99. Given that claim terms are understood by a person of ordinary skill in the art at the time of the invention, a definition of one of ordinary skill in the art must be established to construe the claims of the ’493 patent. I understand that factors such as the education level of those working in the field, the sophistication of the technology, the types of problems encountered in the art, the prior art solutions to those problems, and the speed at which innovations are made may help establish the level of skill in the art.

100. In this declaration, I rely on the following definition of a person of ordinary skill in the art: a person of ordinary skill in the art of the ’493 patent

would hold an undergraduate degree in physics or electrical engineering, and have one or both of the following: (1) three or more years of work experience in a field related to analog integrated circuit design; or (2) a graduate degree in physics or electrical engineering and one or more years of work experience in a field related to analog integrated circuit design.

Thus, it is my opinion that claim 9 is not obvious over Sakurai

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Columbia University 1966 MS
Columbia University 1965 BSEE (Valedictorian)

Biosketch

Dr. Afromowitz was the senior professor in the Department of Electrical Engineering, University of Washington, when he retired at the end of 2015. He had been doing research and teaching there since 1974.

Prior to his academic career, he was a Member of the Technical Staff at the Murray Hill (NJ) Bell Telephone Laboratories, working in the groups developing the first visible light red and green light-emitting diodes (LEDs) and the GaAs heterostructure laser. His work at Bell Labs was primarily involved with materials characterization (optical, thermal, lattice matching, etc.)

Prof. Afromowitz taught both undergraduate and graduate students, including courses in circuits, electricity & magnetism, integrated circuit fabrication, optical fiber theory and applications, semiconductor optical properties and devices, and a seminar on professional issues (career choices, personal & corporate ethics, and intellectual property.)

He holds thirteen patents in the general areas of optical sensors and photolithography. As a consultant to industry, he has worked on optical fiber sensors for acceleration, pressure, temperature, electric field, pH, physical measurements of gases, including flow, thermal conductivity, thermal diffusivity, and viscosity. He also developed an optical fiber sensor for monitoring the curing of thermoset resins. Other research interests include infrared imaging, three-dimensional lithography, microfluidics, and methods for infrared sensing of conditions inside coal-fired boilers to improve control and efficiency. As an expert witness, he has supported patent litigation in a range of semiconductor fabrication technologies.

For three years, he served as a member of the Board of Directors of Enertechnix, Inc.

Specific Areas of Expertise

Electrical Engineering	Lasers, Optics & Devices	Bio/Med Engineering
Sensor Systems	Fiber & Integrated Optics	Bio-medical Devices
IC Chip Fabrication	Photonics Devices	Burn Wounds
Lithography	Imaging & Display Systems	Catheter Devices
Electromagnetics/RF	MEMS Devices	Medical Lasers
Industrial Applications	Laser & LED Applications	Equipment Failure
Patent Litigation Support	Laser Safety / Forensics	Ultrasonics / Phaco

Honors

NIH Research Career Development Award, 1977 – 1982
Inductee, Space Technology Hall of Fame, "Accelerometer", 1999.

Research Interests

Three-dimensional microfabrication technologies, specifically for micro-optic and microfluidic applications; sensors; laser applications; and bio-medical instrumentation, including spectroscopy and ultrasonics.

Publications

Refereed Archival Journal Articles

1. D. Redfield and M. A. Afromowitz, "Direct Absorption Edge in Covalent Solids," Appl. Phys. Letters 11, 138, (1967).

2. D. Redfield and M. A. Afromowitz, "Carrier-Wavelength Effect on Screening in Semiconductors," Phil. Mag. 19, 831, (1969).

3. M. A. Afromowitz and M. DiDomenico, Jr., "Measurement of Free-Carrier Lifetimes in GaP by Photoinduced Modulation of Infrared Absorption," J. Appl. Phys. 42, 3205, (1971).

4. G. A. Rozgonyi and M. A. Afromowitz, "Correlation of Defect-Impurity Interactions in GaP with Local Variations in Photoluminescence," Appl. Phys. Letters 19, 153, (1971).

5. M. A. Afromowitz, "Thermal Conductivity of $Ga_{1-x}Al_xAs$ Alloys," J. Appl. Phys. 44, 1292, (1973).

6. M. A. Afromowitz, "Refractive Index of $Ga_{1-x}Al_xAs$," Solid State Comm. 15, 59, (1974).

7. M. A. Afromowitz and D. L. Rode, "Limitations on Stress compensation in $Al_xGa_{1-x}As_{1-y}P_y$ - GaAs LPE Layers," J. Appl. Phys. 45, 4738, (1974).

8. D. L. Rode, R. L. Brown and M. A. Afromowitz, "Measurement of Lattice Dilitation in LPE GaAs due to Ge Acceptor Doping," J. Crystal Growth 30, 299 (1975).

9. M. A. Afromowitz, P. S. Yeh and S. Yee, "Photoacoustic Measurement of Spatially Varying Optical Absorption in Solids: A Theoretical Treatment," J. Appl. Phys. 48, 209, (1977).

10. M. A. Afromowitz and S. S. Yee, "Fabrication of pH-Sensitive Implantable Electrode by Thick Film Hybrid Technology," J. of Bioengineering 1, 55 (1977).

11. S. D. Campbell, S. S. Yee, and M. A. Afromowitz, "Two Applications of Photoacoustic Spectroscopy to Measurements in Dermatology," J. of Bioengineering 1, 185, (1977).

12. S. D. Campbell, S. S. Yee, and M. A. Afromowitz, "Applications of Photacoustic Spectroscopy to Problems in Dermatology Research ," IEEE Trans. Biomed. Eng'g., BME-26, 220, (1979).

13. J. M. McDavid, K. L. Lee, S. S. Yee, and M. A. Afromowitz, "Photoacoustic Determination of the Optical Absorptance of Highly Transparent Solids." J. Appl. Phys. 49, 6112, (1979).

14. S. Fedel, M. A. Afromowitz and R. A. Sigelmann, "Micropower Pulse Frequency Modulator for Use in an Optically-Isolated Catheter System, "IEEE Trans. Biomed. Eng'g., BME-29, 549 (1982).

15. K.-L. Peng and M. A. Afromowitz, "An Improved Method to Determine MOSFET Channel Lengths," IEEE Electron Device Letters, EDL-3, 360 (1982).

16. D. M. Heimbach, M. A. Afromowitz, L. H. Engrav, J. A. Marvin, and B. Perry, "Burn Depth Estimation --Man or Machine," J. Trauma, 24, 373 (1984).

17. K.-L. Peng, S.-Y. Oh, M. A. Afromowitz, and J. L. Moll, "Basic Parameter Measurement and Channel Broadening Effect in Submicrometer MOSFET," IEEE Electron Device Letters, EDL-5, 473 (1984).

18. M. A. Afromowitz, G. S. Van Liew, and D. M. Heimbach, "Clinical Evaluation of Burn Injuries using an Optical Reflectance Technique," IEEE Trans. Biomed. Eng'g. BME - 34(2), 114 (1987).

19. M. A. Afromowitz, James B. Callis, David M. Heimbach, Larry A. DeSoto, and Mary K. Norton, "Multispectral Imaging of Burn Wounds: A New Clinical Instrument for Evaluating Burn Depth," IEEE Trans. Biomed. Eng'g. 35 (10) , 842 (1988).

20. M. A. Afromowitz, "Fiber Optic Polymer Cure Sensor," J. of Lightwave Tech. 6(10), 1591 (1988).

21. M. A. Afromowitz and K-Y. Lam, "Fiber Optic Method for Monitoring the Curing of Thermoset Composites," Rev. Prog. Quant. NDE, 1988.

22. M. A. Afromowitz and J. E Samaras, "Pinch Field-Flow Fractionation using Flow Injection Techniques," Separation Sci. and Tech. 24(5 & 6), 325 (1989).

23. M. A. Afromowitz and K.-Y. Lam, "Optical Properties of Curing Epoxies and Applications to the Fiber Optic Epoxy Cure Sensor," Sensors and Actuators, A21-A23, 1107-1110 (1990).

24. R. A. Wolthuis, G. L. Mitchell, E. Saaski, J. C. Hartl, and M. A. Afromowitz, "Development of Medical Pressure and Temperature Sensors Employing Optical Spectrum Modulation," IEEE Trans. Biomed. Eng. 38(10), 974-981 (1991).

25. W.-C. Wang, M. Afromowitz, and B. Hannaford, "Technique for Mechanical Measurements Using Optical Scattering from a Micropipette," IEEE Tr. Bio. Eng. 41(3), 298-304 (1994).

26. K-Y. Lam and M. A. Afromowitz, "Fiber-optic Epoxy Cure Sensor, I: Dependence of Refractive Index of an Autocatalytic Reaction Epoxy System at 850 nm on Temperature and Extent of Cure," Appl. Opt. 34(25), 5635-5638 (1995).

27. K-Y. Lam and M. A. Afromowitz, "Fiber-optic Epoxy Cure Sensor, II: Performance Characteristics," Appl. Opt. 34(25), 5639-5644, (1995).

28. C. Wu, M. A. Kenny, M. Huang, M. A. Afromowitz and P.Yager, "Feasibility Study for the Measurement of Oxyhemoglobin Using Whole Blood Without Pretreatment," Clinical Chemistry 42:S283, (1996).

29. Yager, P., Afromowitz, M.A., Bell, D., Forster, F.K., Brody, J.P., Qin, D., Cabrera, C., Holl, M., Kamholz, A., and Weigl, B.H., "Design of microfluidic sample preconditioning systems for detection of biological agents in environmental samples," SPIE Proceedings, 3515, 252-259 (1998).

Fully Refereed and Published Conference Proceedings

1. M. A. Afromowitz and D. Redfield, "Temperature Dependence of the Absorption Edge of GaAs," Proc. Int'l Conf. on the Physics of Semiconductors, Moscow, (1968).

2. D. M. Peter, M. A. Afromowitz and S. S. Yee, "Fabrication of Implantable pH Electrode Utilizing Thin and Thick Film Techniques," Proc. Conf. Int'l. Soc. Hybrid Manufacturers, Vancouver, B. C., Oct. 1976.

3. S. S. Yee and M. A. Afromowitz, "Ion-sensitive Implantable Electrodes Fabricated by Hybrid Technology," Proc. Workshop on Theory, Design, and Biomed. Appl. of Solid State Chemical Sensors, Case Western Reserve Univ., March 1977.

4. M. A. Afromowitz and S. S. Yee, "Fabrication of pH-Sensitive Implantable Electrode by Thick Film Hybrid Technology," Proc. Int'l. Conf. on Thin- and Thick-Film Technology, Augsburg, Sept. 1977.

5. M. A. Afromowitz, K. L. Lee, and S. S. Yee, "Photoacoustic Spectroscopy and its Applications to the Measurement of Surface and Bulk Optical Absorption," Proc. High Power Laser Optical Components and Component Materials, Boulder, Oct. 1977.

6. E. W. Saaski, J. C. Hartl, G. L. Mitchell, R. A. Wolthuis, and M. A. Afromowitz, "A Family of Fiber Optic Sensors using Cavity Resonator Microshifts," Proc. 4th International Conference on Optical Fiber Sensors, Tokyo, October 7-9, 1986.

7. E. W. Saaski, J. C. Hartl, G. L. Mitchell, R. A. Wolthuis, and M. A. Afromowitz, "Multimode Fiber Optic Pressure Sensor with Extended Range," SPIE 838, Fiber Optics and Laser Sensors, Aug. 1987.

8. M. A. Afromowitz, James B. Callis, David M. Heimbach, Larry A. DeSoto, and Mary K. Norton, "Multispectral Imaging of Burn Wounds," SPIE 914, Medical Imaging II, 500-504, February 1988.

9. M. A. Afromowitz and K-Y. Lam, "Fiber Optic Cure Sensor for Thermoset Composites," SPIE 986, Fiber Optic Smart Structures and Skins, 135 (1988).

10. M. A. Afromowitz and K.-Y. Lam, "Optical Properties of Curing Epoxies and Applications to the Fiber Optic Epoxy Cure Sensor," SPIE 1170, Fiber Optic Smart Structures and Skins II, p. 138-142 (1989).

11. L. W. Burgess and M. A. Afromowitz, "Fiber Optic Sensor Programs at the University of Washington," SPIE 1169, Fiber Optic and Laser Sensors VII, p. 16-19 (1989).

12. R. A. Wolthuis, M. A. Afromowitz, G. L. Mitchell, D. Frank, T. Lenihan, and M. Bouchard, "A New Method for Measuring Intra-Arterial Size and Arterial Wall Compliance," FASEB J 8(5) part 2, A866 (1994).

13. F. K. Forster, R. L. Bardell, M. A. Afromowitz, N. R. Sharma and A. Blanchard, "Design, Fabrication and Testing of Fixed-Valve Micro-Pumps," Proc. ASME Fluids Eng'g. Div., FED-234, 39-44 (1995).

14. R. L. Bardell, F. K. Forster, R. J. Penney, N. R. Sharma and M. A. Afromowitz, "Designing High-Performance Micro-pumps based on No-Moving-Parts Valves," DSC-Vol. 62/HTD-Vol. 354, Microelectromechanical Systems (MEMS) ASME 1997, pp. 47-53.

15. M-C. Huang, M. Afromowitz, G. vanden Engh, B. H. Weigl and P. Yager, "Development of a Flow Cytometery Based Miniature Chemical Fluid Analysis System using Fluorescent Microbeads," Proc. of SPIE, Vol. 3256, 178-185 (1998).

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Patents

"Ion-Sensitive Electrode and Processes for Making the Same," M. A. Afromowitz and S. S. Yee; U.S. Patent #4,133,735 issued 1/9/79.

"Inclinometer Having Two Degrees of Freedom," M. A. Afromowitz; U.S. Patent #4,627,172 issued 12/9/86.

"Apparatus and Method for Measuring Electric Field by Electroreflectance," M. A. Afromowitz; U.S. Patent #4,730,109 issued 3/8/88.

"Method of Monitoring Solidification of a Liquid Composition," M. A. Afromowitz; U.S. Patent #4,904,080 issued 2/27/90.

"Method of Monitoring Solidification of a Liquid Composition," M. A. Afromowitz; U.S. Patent #5,009,102 issued 4/ 23/91.

"Apparatus and Method for Determining Physiologic Characteristics of Body Lumens," M. A. Afromowitz, Roger A. Wolthuis, and Gordon Mitchell; U.S. Patent #5,275,169 issued 1/4/94.

"Micropumps with Fixed Valves," F. K. Forster, R. L. Bardell, A. P. Blanchard, M. A. Afromowitz and N. R. Sharma; U.S. Patent #5,876,187 issued 3/2/99.

"Method for Fabricating 3-D Structures with Smoothly-Varying Topographic Features in Photo-Sensitized Epoxy Resists," M. A. Afromowitz; U.S. Patent #6,635,412 issued 10/21/03.

"Sensing System for Detection and Control of Deposition on Pendant Tubes in Recovery and Power Boilers," G. Kychakoff, M. A. Afromowitz and R. E. Hogle; U.S. Patent #6,909,816 issued 6/21/05.

"Fabrication of Molds and Mold Components using a Photolithographic Technique and Structures Made Therefrom," M. A. Afromowitz; U.S. Patent #7,045,089 issued 5/16/06.

"3-D Structures with Smoothly-Varying Topographical Features in Photo-Sensitive Epoxy Resists," M. A. Afromowitz; U.S. Patent #7,303,853 issued 12/4/2007.

"Sensing System for Detection and Control of Deposition on Pendant Tubes in Recovery and Power Boilers," G. Kychakoff, M. A. Afromowitz and R. E. Hogle; U.S. Patent #7,437,025 issued 10/14/08.

"Infrared Imaging Sensor," G. Kychakoff, M. A. Afromowitz and R. E. Hogle; U.S. Patent #7,956,326 issued 6/7/11.

Expert Witness & Consulting (2004 —>)

* indicates recent testifying experience

Consultant to Preston, Gates & Ellis (San Francisco), on patent infringement case involving horizontal directional drilling equipment and methods (Tim Walker and Mike Bettinger, Esq., expert for Digital Control v. Charles Machine Works), 2004.

Consultant to Preston, Gates & Ellis (Seattle), on patent infringement case involving horizontal directional drilling equipment and methods (David Binney, Esq., expert for Digital Control v. Ridge Tool), 2004.

Consultant to Akin Gump Strauss Hauer & Feld (Houston), on patent infringement case involving medical products for refractive surgery (Les Hewitt, Esq. for Bausch & Lomb), 2007.

Consultant to Kirkpatrick & Lockhart Preston Gates Ellis (San Francisco), on patent infringement case No. 3:06-cv-05701-RJB (Western District of Washington), expert for defendant, Wacom Co. Ltd, et al v. Hanvon Corporation et al (Tim Walker and Mike Bettinger, Esq.), 2008.

Consultant to Susman Godfrey (Seattle), on patent infringement case (Civil Action No. 2:07-CV-67, Eastern District of Texas, Marshall Division), expert for plaintiff, Positive Technologies Inc. v. Toshiba America Consumer Products, LLC, et al (Ian Crosby, Esq.), 2010.

Consultant to Collins Edmonds & Pogorzelski (Houston), for evaluation of patents involving micro-electro-mechanical systems (Henry Pogorzelski, Esq.), 2011 and 2012.

Consultant to Rickles Law Firm (Portland, OR), on an insurance matter concerning damage to semiconductor wafers due to faulty installation of processing equipment (Stephen Rickles, Esq.), 2011.

Consultant to Leviton Manufacturing Co., Inc., on claim construction issues pertaining to electrical cable structures (Kathy Milam, Esq.), 2011 and 2012.

*****Testifying witness for Covington & Burling (San Francisco) on ITC patent infringement case Inv. No. 337-TA-798, expert for Complainants, Samsung Electronics, et al v. Osram AG, et al (Ashley Miller, Esq., Jared Frisch, Esq., Michael Markman, Esq.), settled August 2012. Case involved fabrication of LEDs. Claim construction, expert reports, deposition, trial prep.

Consultant to Collins Edmonds & Pogorzelsky (Houston) on a patent infringement case, expert for plaintiff, Semiconductor Technologies LLC v. Micron Technology, Inc., et al (Henry Pogorzelsky, Esq.), settled May 2013. Case involved design and fabrication of MEMS accelerometer.

Consultant to Desmarais, LLP (New York) on a patent infringement case, 3:11-cv-05243-RS, Northern District of California, expert for defendant and counterclaim plaintiff in Sandisk v. Round Rock Research, LLC, settled

in 2013. Case involved packaging of integrated circuits. Provided declaration re summary judgment.

Consultant to Desmarais, LLP (New York) on a patent infringement case, expert for plaintiff, Round Rock Research, LLC, v. Asus (Lauren Nowierski, Esq.), settled May 2014. Participated in claim construction discussions.

*****Testifying witness for Desmarais, LLP (New York) on a patent infringement case, 1:11-CV-792-SLR, District of Delaware, expert for plaintiff, Intellectual Ventures I, LLC, et al v. Canon, Inc., et al (Alan Kellman, Esq.), verdict in favor of Intellectual Ventures on all matters, May 2014. Case involved design of CMOS image sensors. Expert reports, deposition, trial.

Consultant to Desmarais, LLP (New York) on a patent infringement case, expert for plaintiff, Intellectual Ventures, against Nikon, related to CMOS image sensor technology (settled December 2015).

Consultant to Radulescu, LLP (New York) on a patent infringement case, 2:14-cv-09466-ODW(Ex), Central District of California, expert for plaintiff, Seoul Semiconductor v. Curtis International Ltd., involving design and fabrication of LEDs and their use in back-lighting of LCDs, settled in 2015. Claim construction, declaration.

Consultant to Bragalone Conroy PC (Dallas) on one ongoing patent infringement case involving design of CMOS image sensors.

APPENDIX B

INFORMATION CONSIDERED

- Ex. 1001 - U.S. Patent No. 5,952,714 ("the '714 patent").
- Ex. 1002 – Declaration of R. Michael Guidash.
- Ex. 1003 – JP Translation Pub. No. S61-131690 ("Yoshino").
- Ex. 1004 – JP Translation Pub. No. H07-045803 ("Wakabayashi").
- Ex. 1005 – JP Translation Pub. No. S59-225560 ("Hikosaka").
- Ex. 1011 – Publication No. H07-78951 ("Nita").
- Ex. 1014 – Publication No. H05-006989 ("Onishi").
- Ex. 1016 –. Publication No. S63-221667 ("Izumi").
- Ex. 1018 – Publication No. H06-029507 ("Nagano").
- Ex. 1020 – Publication No. S60-74880 ("Hirosawa").
- Ex. 1022 – Publication No. H05-275611 ("Tobase").
- Ex. 1024 – Publication No. H06-85221 ("Fujii").
- Ex. 2002 – S. O. Kasap, Optoelectronics and Photonics: Principles and Practices (2d ed. 2013)
- Ex. 2003 – Prosecution File History of U.S. Pat. No. 5,952,714
- Ex. 2004 – Deposition of R. Michael Guidash, January 11, 2017
- Ex. 3001 – The Am. Heritage Dictionary
- Paper No. 2, Petition
- Paper No. 6, Institution Decision
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