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| UTILITY SERIAL NUMBER | 809845 | PATENT DATE | SEP 14 1998 | PATENT NUMBER | 5952714 |
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TSUJII, KYOTO, JAPAN; MASAJI ASAUMI, KYOTO, JAPAN; YOSHIKAZU CHATANI,
KYOTO, JAPAN.

CONTINUING DATA***

VERIFIED THIS APPLN IS A 371 OF PCT/JP96/02142 07/30/96

FOREIGN APPLICATIONS***

VERIFIED JAPAN 7-197365 08/02/95

CERTIFICATE

SEP 05 2000

OF CORRECTION

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SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

U.S. DEPT. OF COMM./PAT. & TM - PTO-436L (Rev. 12-94)

PARTS OF APPLICATION
FILED SEPARATELY

NOTICE OF ALLOWANCE MAILED

1/11, 99

Assistant Examiner

CLAIMS ALLOWED

Total Claims 16 Print Claim 1

ISSUE FEE

Amount Due

Date Paid

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3-26-98

NGAN V. NGO

PRIMARY EXAMINER
GROUP 2500

DRAWING

Sheets Drwg. 10 Figs. Drwg. 2 Print Fig. 2

ISSUE
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NUMBER

N 72

Label
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PREPARED FOR ISSUE 1/14/99

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ISSUE FEE IN FILE

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PATENT APPLICATION



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| | 1. Application | 8 pgs | papers. | 19 MAY 1997 |
| | 2. | 985 | | |
| | 3. | 2 pgs Dec | | 16 June 97 |
| | 4. | 903 | | 10 July 97 |
| Q-10-98 | 5. | IDS | | 10-10-98 |
| | 6. | CR | | 3 pgs/98 |
| 7-16-98 | 7. | Examination (3 months) | | 7-20-98 |
| 1-4-99 | 8. | Amendment & reply for EPO | | 12-21-98 |
| FS 1-11 | 9. | PTOL-37 | | 1-11-99 |
| | 10. | Duplicate Notice | | 1/11/99 |
| H-19-99 | 11. | Formal Drawings (2 sets) set | | 3-26-99 |
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| 6-23-99-H | 15. | PTOL-271 | | 6/24/99 |
| | 16. | Req. for CIP | | 2-8-2000 |
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| 257 | 680 686 688 689 701 724 725 | 7-15-68 | ✓ |
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| SEARCH NOTES | | |
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PATENT NUMBER

ORIGINAL CLASSIFICATION

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257

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APPLICATION SERIAL NUMBER

08/809845

CROSS REFERENCE(S)

CLASS

SUBCLASS
(ONE SUBCLASS PER BLOCK)

257

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APPLICANT'S NAME (PLEASE PRINT)

SANO ET AL

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION

H 0 1 L

23 / 02

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23 / 48

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GROUP
ART UNIT

2814

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

NGAN V. NG

PTO 270
(REV. 5-91)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

| Claim | | Date | |
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SYMBOLS

✓ Rejected
= Allowed
- (Through numerical) Canceled
+ Restricted
N Non-elected
I Interference
A Appeal
O Objection

(LEFT INSIDE)



US005952714A

United States Patent [19]

Sano et al.

[11] **Patent Number:** **5,952,714**[45] **Date of Patent:** **Sep. 14, 1999**[54] **SOLID-STATE IMAGE SENSING APPARATUS
AND MANUFACTURING METHOD
THEREOF**5,357,056 10/1994 Nagano 174/52.4
5,753,857 5/1998 Choi 174/52.4[75] **Inventors:** Yoshikazu Sano, Osaka; Sumio
Terakawa, Ibaraki; Eiichi Tsujii,
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Osaka, Japan[21] **Appl. No.:** **08/809,845**[22] **PCT Filed:** **Jul. 30, 1996**[86] **PCT No.:** **PCT/JP96/02142**§ 371 Date: **Jun. 16, 1997**§ 102(e) Date: **Jun. 16, 1997**[87] **PCT Pub. No.:** **WO97/05660****PCT Pub. Date:** **Feb. 13, 1997**[30] **Foreign Application Priority Data**

Aug. 2, 1995 [JP] Japan 7-197365

[51] **Int. Cl.⁶** **H01L 23/02; H01L 23/48;**
H01L 23/34[52] **U.S. Cl.** **257/680; 257/686; 257/688;**
257/689; 257/724; 257/725[58] **Field of Search** **257/680, 686,**
257/688, 689, 700, 724, 725[56] **References Cited****U.S. PATENT DOCUMENTS**

5,327,325 7/1994 Nicewarner, Jr. 361/760

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4-235476 8/1992 Japan .
7-45803 2/1995 Japan .
7-99214 4/1995 Japan .*Primary Examiner*—Ngân V. Ngô*Attorney, Agent, or Firm*—McDermott, Will & Emery[57] **ABSTRACT**

A lead frame 24 comprising an inner lead 22 and outer lead 23 is sealingly filled from a through-hole into a package 21. A CCD chip 27 is inserted from an inlet 26 into the package 21. An electrode pad 28 is connected to the inner lead 22 via a bump 29 to complete an optical positioning and an electrical connection, then the positions of these components are fixed by glue. As a result, a solid-state image sensing apparatus can be manufactured at a low cost, and an accurate positioning can be realized. Thus, the solid-state image sensing apparatus can be employed to a video camera of high quality picture to reproduce vivid colors and fine pictures.

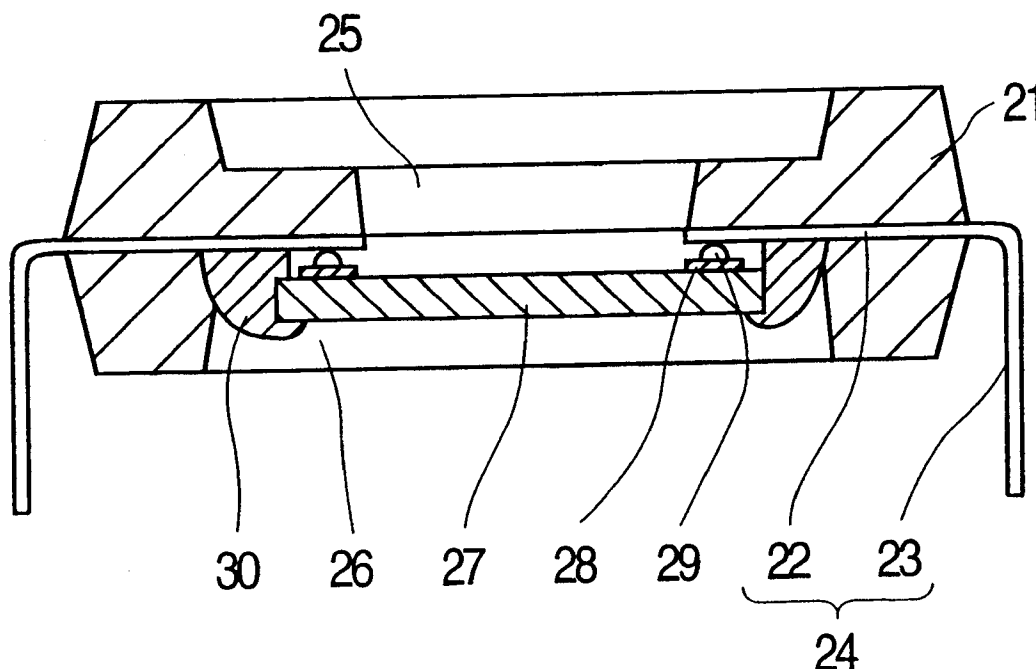
16 Claims, 6 Drawing Sheets

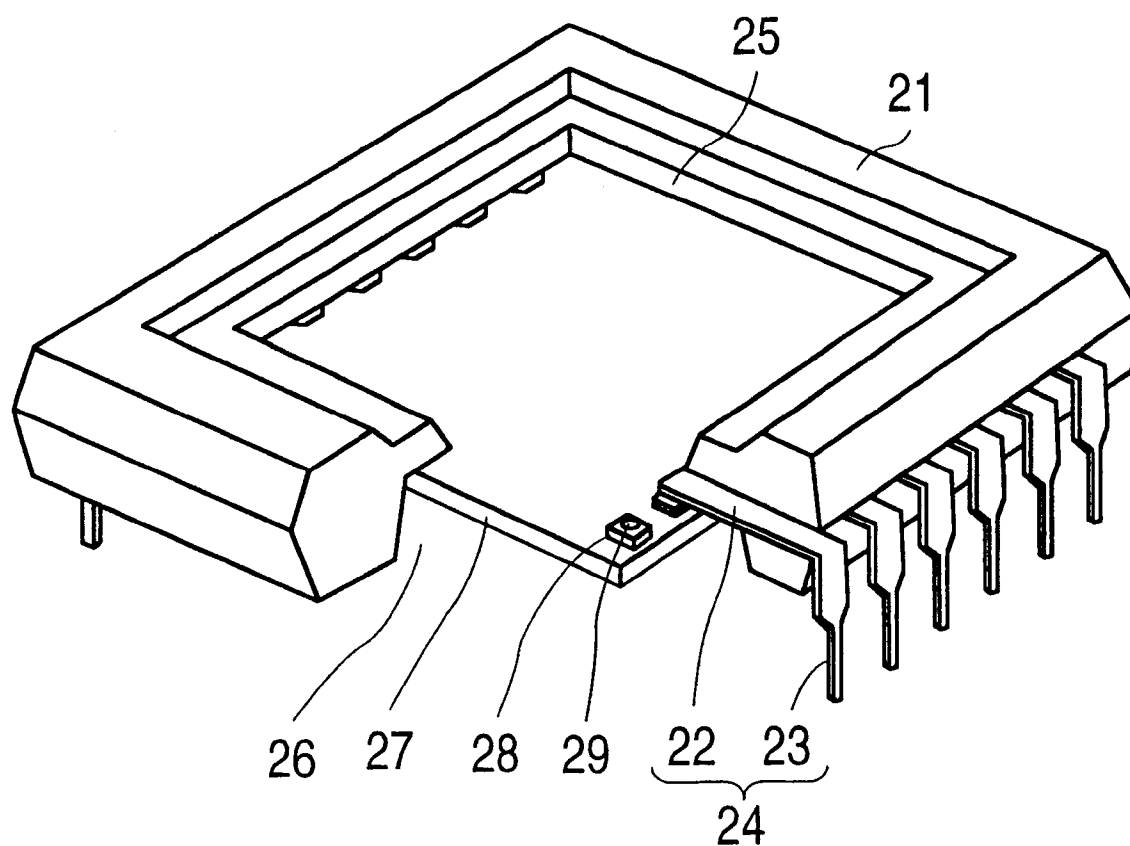
FIG. 1

FIG. 2

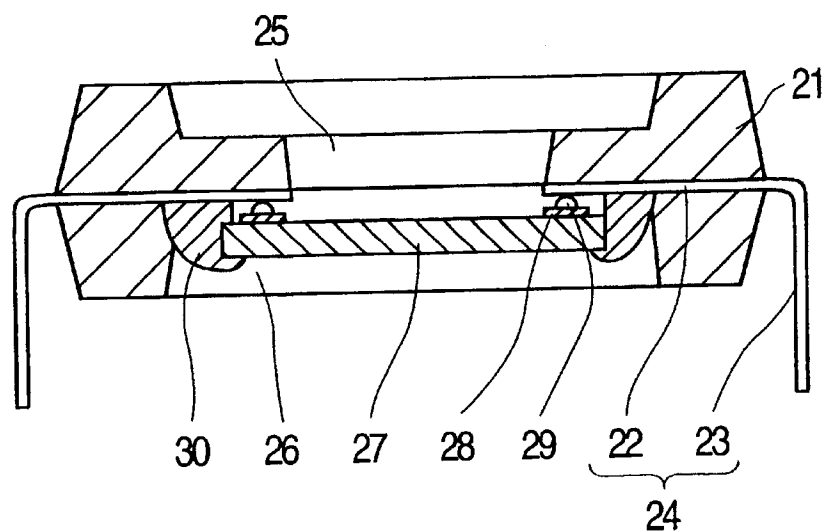


FIG. 3

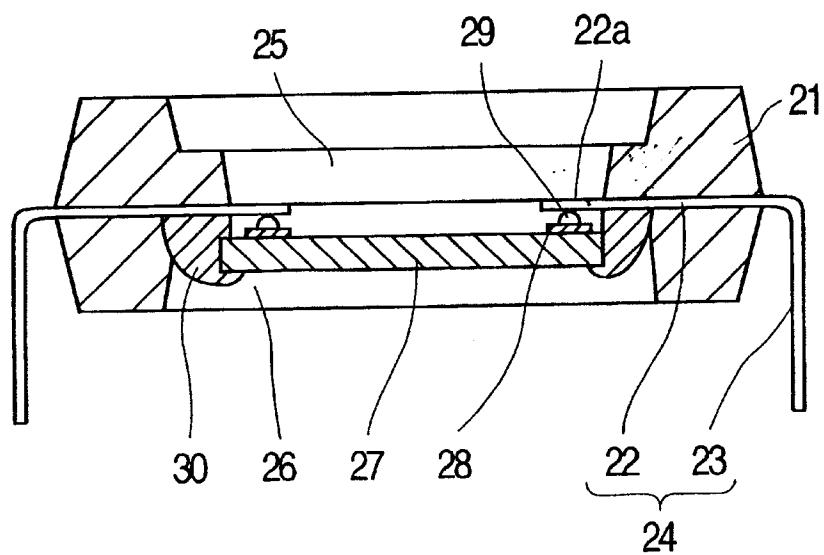


FIG. 4

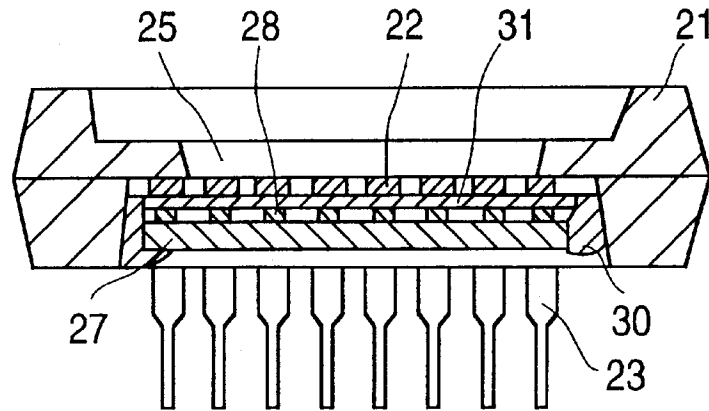


FIG. 5

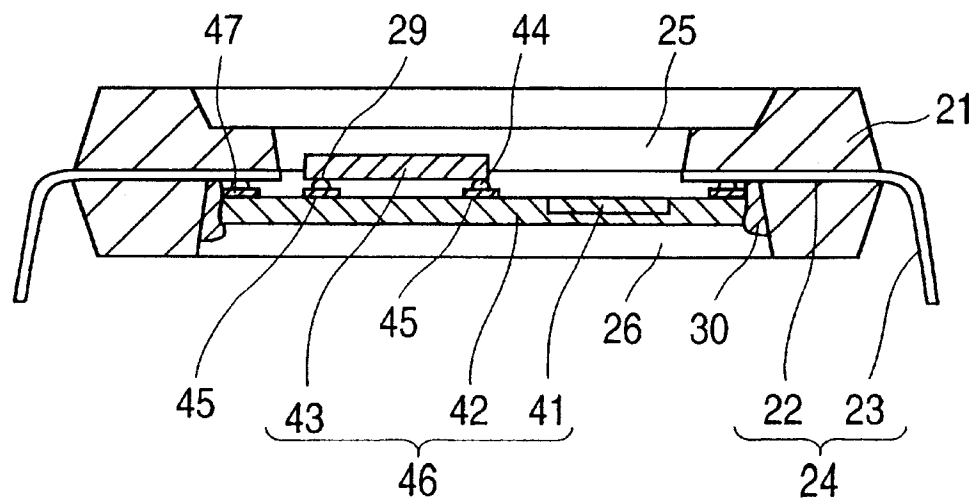


FIG. 6

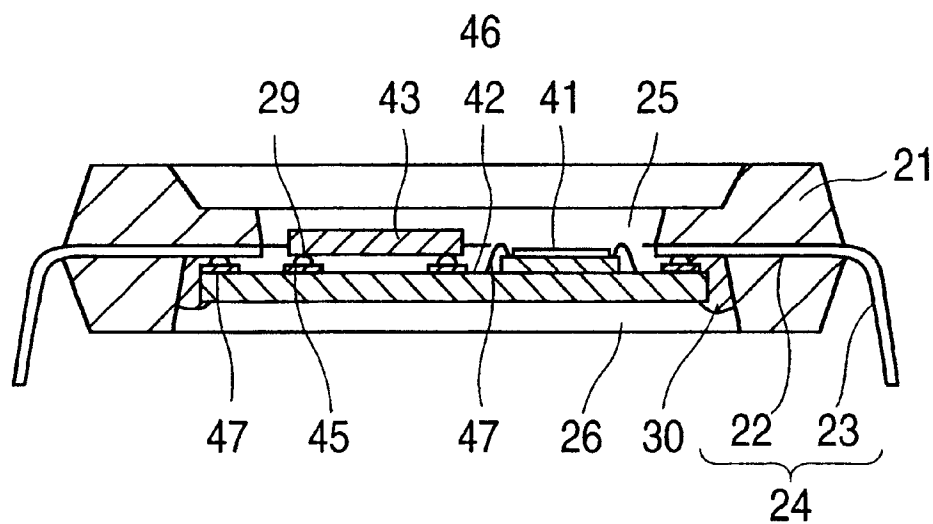


FIG. 7

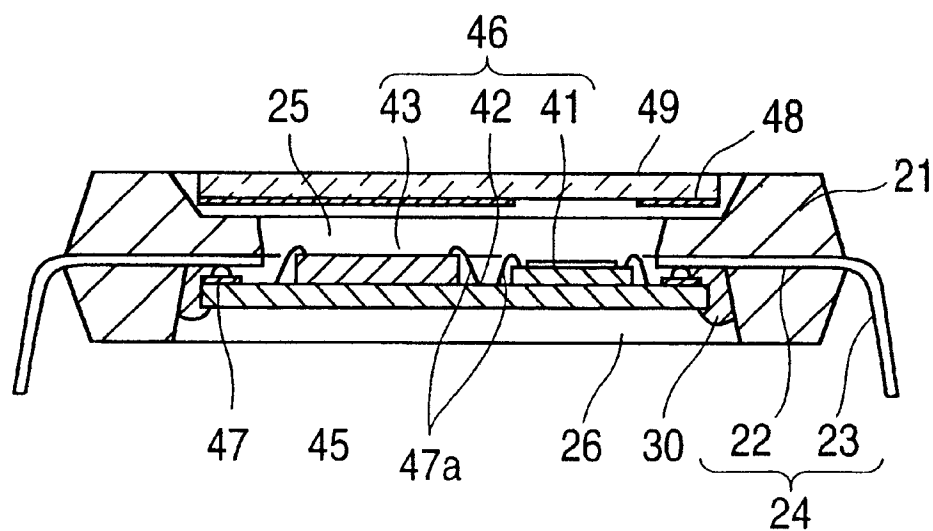


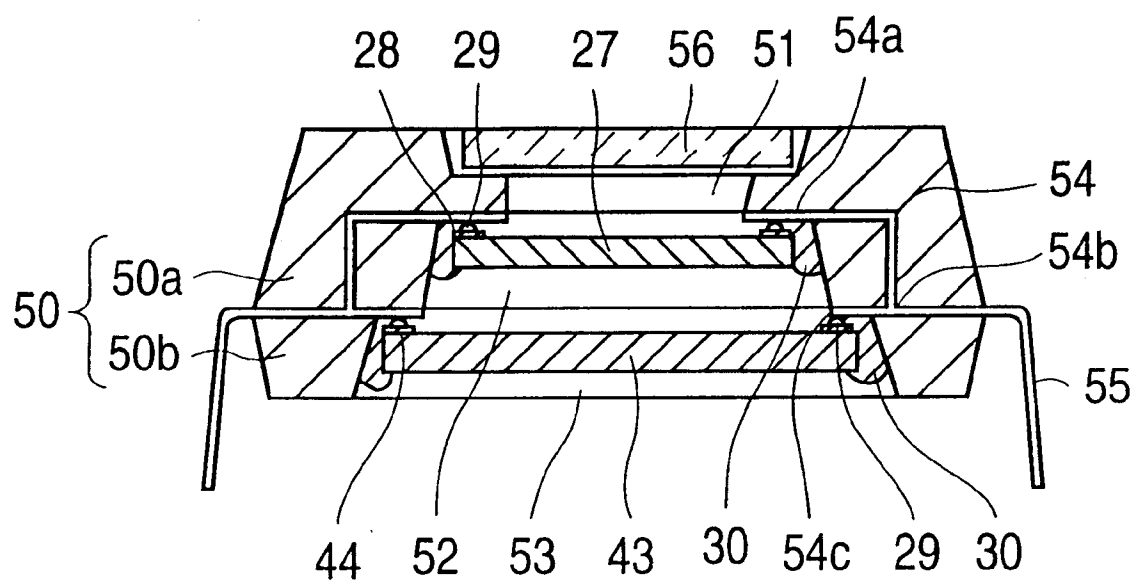
FIG. 8

FIG. 9
PRIOR ART

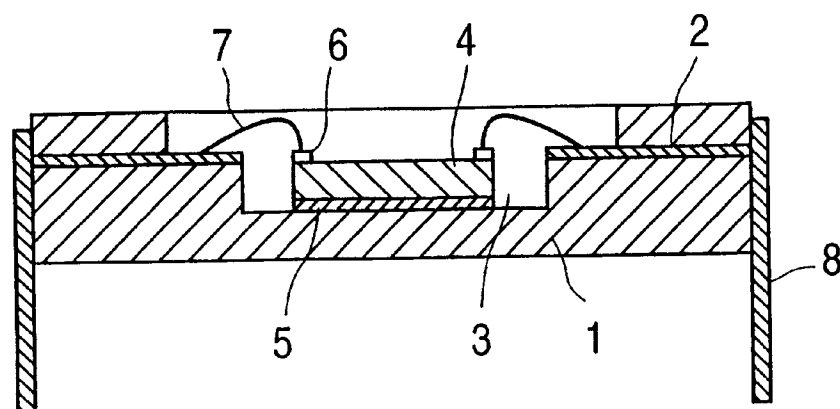
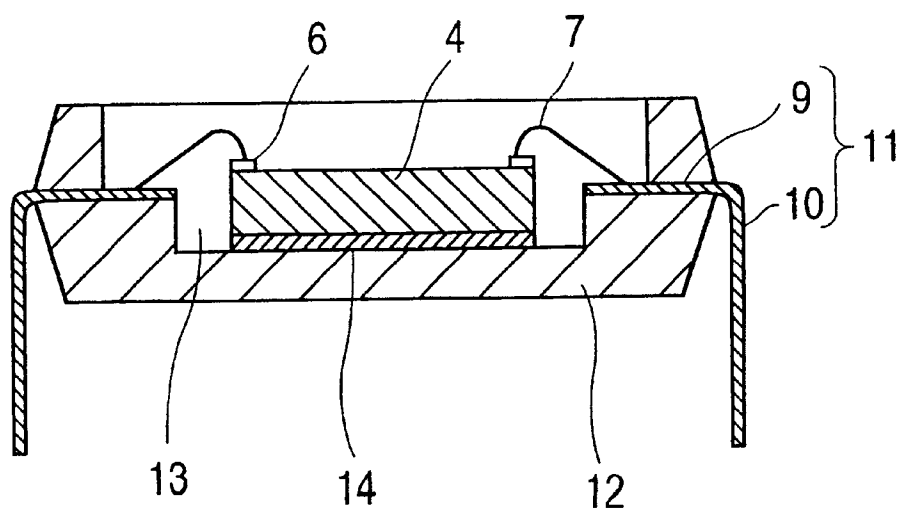


FIG. 10
PRIOR ART



SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

FIELD OF ENGINEERING

The present invention relates to a solid-state image sensing apparatus using a solid-state image sensing device (hereinafter called CCD chip) in a package made of plastic, ceramic or glass (hereinafter called package), more particularly to a solid-state image sensing apparatus using three CCD chips, which is used for a video camera and required severe optical positioning accuracy. The present invention also relates to the manufacturing method of the solid-state image sensing apparatus.

BACKGROUND OF ENGINEERING

Recently, a video camera, a home-use video camera among others, has been equipped with the better functions in addition to its reducing size and weight. Consumers have demanded the better quality picture such as of high color fidelity as well as displaying detail. In order to satisfy this demand, technical levels relating to many components of the video camera have been highly enhanced, and in particular, performance of the CCD chip which is called "a heart of video camera," has been remarkably progressed in increasing a number of pixels. On the other hand, a home-use video camera of which main stream has been one-eye video camera using one CCD chip, starts replacing the one-eye with a three-eye using three CCD chips which has been employed in an expensive professional video camera, namely, three CCD chips correspond to Red, Green, Blue colors. Comparing with the one-eye video camera, the three-eye video camera is required an ultra positioning accuracy because three CCD chips are to be optically disposed at correct positions. Since the home-use video camera has been designed to be portable and smaller in size, many of the components are mounted in an extreme high density. Therefore, the solid-state image sensing apparatus for the home-use video camera is required to change itself in its own structure.

FIG. 9 and FIG. 10 depict a conventional solid-state image sensing apparatus. FIG. 9 is a cross section of a solid-state image sensing apparatus in a ceramic package which was once a mainstream. A ceramic package 1, on which metallized conductor 2 is formed, has a concave part 3 in the center thereof. On the concave part 3, a CCD chip 4 is mounted by die bonding, and an electrode pad 6 of CCD chip 4 is wire-bonded to the metallized conductor 2 by a metal lead 7. A lead terminal 8 is deposited to an end face of metallized conductor 2 exposing itself from the side of ceramic package 1.

FIG. 10 is a cross section of a solid-state image sensing apparatus in a plastic package. A lead frame 11 comprising an inner lead 9 and an outer lead 10 is inmolded in a plastic package 12. At a center of the plastic package, a concave portion 13 is situated. The CCD chip 4 is di-bonded by conductive paste 14 to the concave portion 13, and the electrode pad 6 on the CCD chip 4 is wire-bonded to the inner lead 9 by the metal lead 7 as same as the case of the ceramic package shown in FIG. 9.

However, according to the above conventional solid-state image sensing apparatus and the manufacturing method thereof, the CCD chip in either the ceramic package 1 or plastic package 12, is mounted on the base of either concave part 3 or 13 by die bonding. When this conventional solid-state image sensing apparatus having the above struc-

ture is mounted to the three-eye video camera and is accurately positioned in optical manner, the base of concave part 3 or 13 of ceramic package 1 or plastic package 12 to which the CCD chip 4 is die-bonded should be processed in high accuracy. Also a level of parallelism with regard to the base and an upper face of ceramic package 1 or plastic package 12 should be highly accurate. These factors not only increase a cost of ceramic package 1 or plastic package 12 but also raise a cost of mounting process of CCD chip 4. The wire-bonding method for connecting the electrode pad 6 of CCD chip 4 with the metallized conductor 2 or the inner lead 9 via the metal lead 7 is a classic manufacturing technique expecting a low defect ratio and requiring little effort for replacing chips; however, this method limits the size reduction of solid-state image sensing apparatus, and cannot fully respond to a request of reducing a size thereof from the market of home-use video camera.

DISCLOSURE OF THE INVENTION

The present invention aims to provide a solid-state image sensing apparatus mountable to a video camera of high quality picture, which not only can reproduce vivid colors and fine pictures but also can be manufactured at a low cost. The present invention also aims to provide a manufacturing method of the solid-state image sensing apparatus.

The solid-state image sensing apparatus according to the present invention comprises a package having a through hole therein, a lead frame comprising an inner lead and an outer lead sealed therein, and a CCD chip loaded therein. Both the end faces of the package have different opening areas. The CCD chip can be mounted from the opening having the wider opening area, and thereby shutting the through hole tightly.

Another type of the solid-state image sensing apparatus according to the present invention has the opening of the package. The electrode pad of CCD chip is connected via the inner lead to the opening, and the opening area is smaller than the entire area of CCD chip.

Still another type of the solid-state image sensing apparatus according to the present invention has the package having a through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and a substrate on which the CCD chip and peripheral circuit elements are mounted being loaded into the package from the opening which has the wider opening area, and the electrode pad of substrate connected to the inner lead exposed from a periphery of end face of the opening which has the smaller opening area.

Further another type of the solid-state image sensing apparatus of the present invention has the package having a through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and the peripheral circuit elements mounted on a substrate which is disposed on an upper surface of the substrate excluding the surface where the CCD chip is mounted. The two substrates are loaded into the package from the opening which has the wider opening area. The electrode pad is connected to the inner lead exposed from the periphery end face of the opening which has the smaller opening area.

Another type of the solid-state image sensing apparatus of the present invention has the package having the through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and the CCD chip fixed and coupled to a first inner lead exposed from a first step of the package, and the peripheral circuit elements fixed and connected to a second inner lead exposed from a second step of the package.

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A manufacturing method according to the present invention relates to the solid-state image sensing apparatus which has the package comprising a through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and the CCD chip mounted therein. The CCD chip is loaded into the through hole of the package from the opening which has the wider opening area. The electrode pad of solid-state image sensing apparatus is coupled to the inner lead via a bump or an anisotropic conductor having only vertical conductivity so that optical positioning as well as electrical connecting is completed. Then a back side of the CCD chip is glued to the package by adhesive.

Another manufacturing method according to the present invention relates to the solid-state image sensing apparatus which has the package comprising the through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and the CCD chip as well as the peripheral circuit elements mounted therein. The CCD chip and group of wirings are formed on a semi-conductor substrate, then the periphery circuit elements are disposed on the substrate excluding a preoccupied place by the CCD chip, and connected to the group of wirings. Next, the substrate is loaded into the through hole from the opening which has the wider opening area. The electrode pad disposed around the upper surface of the substrate is connected to the inner lead via the bump or anisotropic conductor so that the optical positioning as well as electrical connection is completed. Then the back side of the substrate having the CCD chip and peripheral circuit elements thereon is glued to the package by adhesive.

Still another manufacturing method according to the present invention relates to the solid-state image sensing apparatus which has the package comprising the through hole therein, and the lead frame comprising the inner lead and outer lead sealingly filled therein, and the CCD chip as well as the peripheral circuit elements loaded therein. The CCD chip and the peripheral circuit elements are mounted on the substrate where the group of wirings were already disposed, and the CCD chip and the peripheral circuit elements are connected to the group of wirings. The substrate is loaded into the through hole from the opening which has the wider opening area. The electrode pad disposed at periphery of the upper surface of the substrate is connected to the inner lead via the bump or anisotropic conductor so that the optical positioning as well as electrical connection is completed. Then the back side of the substrate having the CCD chip and peripheral circuit elements thereon is glued to the package by adhesive.

Further another manufacturing method according to the present invention relates to the solid-state image sensing apparatus which has the package comprising the through hole therein, and the lead frame comprising the inner and outer leads sealed therein, and the CCD chip as well as the peripheral circuit elements mounted therein. The CCD chip is loaded into the through hole of the package from the opening which has the wider opening area, and the electrode pad is connected to the first inner lead via the bump or the anisotropic conductor so that optical positioning as well as electrical connection is completed. Then the back side of the CCD chip is glued to the package by adhesive, and the peripheral circuit elements is loaded into the through hole from the same opening used when the CCD chip loaded. The electrode pad of the peripheral circuit elements is electrically connected to the second inner lead via the bump or the anisotropic conductor, and then the back side of the peripheral circuit elements is glued to the package by adhesive.

According to the present invention, the through hole is provided in the package, and the CCD chip can be loaded

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into the package from the bottom side, namely from the opening which has the wider opening area. The electrode pad of CCD chip is electrically connected to the bump or the anisotropic conductor, and also optically positioned at the same time. Thus, the present invention can reduce a number of manufacturing processes comparing with the conventional method which requires two bonding processes including the die-bonding of CCD chip and the wire-bonding of electrode pad. Further, because a loading jig for the CCD chip can be disposed at the back side of CCD chip, the CCD chip can be optically positioned with ease from the front, thus more accurate positioning can be expected.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cutaway perspective view of the solid-state image sensing apparatus of an exemplary embodiment of the present invention.

FIG. 2 is a cross section of the solid-state image sensing apparatus of the first exemplary embodiment of the present invention.

FIG. 3 is a cross section of the solid-state image sensing apparatus of the second exemplary embodiment of the present invention.

FIG. 4 is a cross section of the solid-state image sensing apparatus of the third exemplary embodiment of the present invention.

FIG. 5 is a cross section of the solid-state image sensing apparatus of the fourth exemplary embodiment of the present invention.

FIG. 6 is a cross section of the solid-state image sensing apparatus of the exemplary embodiment of the present invention.

FIG. 7 is a cross section of the solid-state image sensing apparatus of the sixth exemplary embodiment of the present invention.

FIG. 8 is a cross section of the solid-state image sensing apparatus of the seventh exemplary embodiment of the present invention.

FIG. 9 is a cross section of a conventional solid-state image sensing apparatus.

FIG. 10 is a cross section of another conventional solid-state image sensing apparatus.

THE DESCRIPTION OF PREFERRED EMBODIMENT

An exemplary embodiment of the present invention is stated here by referring to FIG. 1, which is a cutaway perspective view of an exemplary embodiment according to the present invention. A lead frame 24 comprising an inner lead 22 and an outer lead 23 is inmolded in a package 21. As FIG. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a smaller opening area is situated, and another opening 26 (hereinafter called "inlet" which has a wider opening area is situated at the back side thereof. The area of opening 25 is smaller than that of CCD chip 27. An inner lead 22 is exposed from the back side of a step between the opening 25 and the inlet 26, and the inner lead 22 is electrically connected to a bump 29 disposed on an electrode 28 of CCD chip 27.

Next, a manufacturing method according to the present invention is described. FIG. 2 is a cross section of the solid-state image sensing apparatus according to the first exemplary embodiment of the present invention. Epoxy

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resin mixed with inorganic filler is injected into a mold where the lead frame 24 made of phosphor bronze, etc. is disposed, and is inmolded at a high temperature. Then the package 21 is taken out from the mold. A frame body of the lead frame 24 is cut away, and the outer lead 23 is bent toward the inlet 26, thereby forming the package 21. The bump 29 is formed on the electrode pad 28 of the CCD chip 27, whose back side is held by a mounting jig(not shown), and the CCD chip 27 is inserted into the package 21 from the net 26. Then, the bump 29 is press-fitted and connected to the inner lead 22 which is exposed from a back side of the step situated between the opening 25 and the net 26. During this press-fit operation, a position signal is feed-backed from an optical position adjusting device(not shown) disposed in front of the CCD chip 27 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 27 and disposing the CCD chip 27 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the package 21, and finally, the CCD chip 27 is accurately mounted to the package 21.

FIG. 3 is a cross section of the solid-state image sensing apparatus used in a second exemplary embodiment of the present invention. A different point from the first exemplary embodiment is this: a tip 22a of the inner lead 22 slightly protrudes from the opening 25 toward inside. This structure facilitates the optical positioning as well as the bonding between the inner lead and the bump 29 thanks to elasticity of the tip 22a.

In the first and second exemplary embodiments, the bump 29 is disposed on the electrode pad 28; however, the bump 29 may be disposed at the tip of inner lead 22 and coupled with the electrode pad 28 of CCD chip 27.

FIG. 4 is a cross section of the solid-state image sensing apparatus used in Embodiment 3. The inner leads 22 are cut so that they seem to be arranged in parallel from their cross sectional view. In this embodiment, the electrode pad 28 of CCD chip 27 and the inner leads 22 are connected via the anisotropic conductor 31 which has conductivity in only the vertical direction instead of via the bump 29. Thanks to the elasticity of anisotropic conductor 31 made of conductive rubber or the like, the CCD chip 27 can be optically positioned with ease as same as the second embodiment.

According to this exemplary embodiment, an assembly process can be substantially simplified because of the structure as follows: the through hole is provided in the package 21, and the CCD chip 27 is loaded from the inlet 26 which is situated on the back side of package 21, namely, on the side of outer leads, and the exposed inner lead 22 from the back side of the step situated between the opening 25 and the inlet 26 is connected to the electrode pad 28 of CCD chip 27 electrically via the bump or anisotropic conductor, at the same time, an optical positioning between the inner lead 22 and the electrode pad 28 is completed. Further, since the mounting jig of CCD chip 27 can be disposed on the back side of CCD chip 27, the CCD chip 27 can be optically positioned from the front with ease, thus an accurate positioning can be achieved.

FIG. 5 is a cross section of the solid-state image sensing apparatus used in Embodiment 4. Epoxy resin mixed with inorganic filler is injected into a mold where the lead frame 24 made of phosphor bronze, etc. are disposed, and is inmolded at a high temperature. Then the package 21 is taken out from the mold. A frame body of the lead frame 24 is cut away, and the outer lead 23 is bent toward the inlet 26,

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thereby forming the package 21. A substrate 42 comprising a semiconductor substrate such as silicon wafer, on which a group of wirings (not shown) and a CCD chip 41 are formed, and on a part of the substrate surface, a peripheral circuit elements 43 are disposed in a face-down way; the peripheral circuit elements 43 were produced in a separate manufacturing process. A bump 29 disposed on an electrode pad 44 of the peripheral circuit elements is connected to an electrode pad 45 of the group of wirings on the substrate 42, thereby producing a function device 46 (hereinafter called "CCD module"). A back side of the CCD module 46 is held by a mounting jig (not shown), and is inserted from the inlet 26 into the package 21. Then, the bump 29 on an electrode pad 47 disposed around the CCD module 46 is press-fitted to the inner lead 22 exposed from the back side of the step situated between the opening 25 and the inlet 26, thus the bump 29 is electrically connected with the inner lead 22. During this press-fit operation, a position signal is feed-backed from an optical position adjusting device(not shown) disposed in front of the CCD chip 41 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 41 and disposing the CCD module 46 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 41 to the package 21, and finally, the CCD chip 41 is accurately mounted to the package 21.

FIG. 6 is a cross section of the solid-state image sensing apparatus used in Embodiment 5 of the present invention. This embodiment is one of variations of Embodiment 4 described above. The method of accurately mounting the CCD chip 41 to the package 21 is the same as that of the Embodiment 4 from the standpoints of structure and manufacturing, namely, the CCD module 46 on which the CCD chip, peripheral circuit elements and the group of wirings are formed, is inserted from the inlet 26, and the CCD module 46 is fixed to the package 21, while the optical position of CCD chip 41 is fine adjusted. A different point from the Embodiment 4 is this: in Embodiment 4, the CCD chip is formed directly on the semiconductor substrate, which is to be the substrate 42 of the CCD module 46, through a circuit-chip-forming-process such as a direct diffusion process, on the other hand in Embodiment 5, the CCD chip 41 as well as peripheral circuit elements 43 was already produced in a separate process, and the CCD chip 41 and peripheral circuit elements 43 are disposed on the substrate 42 on which the group of wirings have been formed, and thereby they are electrically connected to form the CCD module 46.

Accordingly, the substrate 42 used in this embodiment may be made of a material other than semiconductor. As shown in FIG. 6, when the CCD chip 41 produced in the separate process is mounted on the substrate 42, the electrode of CCD chip 41 is wire-bonded to the electrode terminal of the group of wirings by using a metal wire 47a.

FIG. 7 is a cross section of the solid-state image sensing apparatus used in Embodiment 6. This embodiment is also one of variations of Embodiment 5 above mentioned. A different point from Embodiment 5 is this: in Embodiment 5, the peripheral circuit elements 43 are connected to the substrate 42 via the bump 29 in the face-down way same as that in Embodiment 4; however, in this Embodiment 6, the peripheral circuit elements 43 are disposed on the substrate 42 in the face-up way(the face on which a circuit is formed is situated upward) as the CCD chip 41 is in Embodiment 5, and the electrode of peripheral circuit elements is wire-

bonded to the electrode terminal of the group of wiring by using the metal wire 47a.

Embodiments 4, 5, and 6 have some similarities as well as differences with each other. An advantage of the solid-state image sensing apparatus in these embodiments are as follows.

First, in Embodiment 4, since the CCD chip 41 is formed on the substrate 42 together with other groups of wirings at the same time, the electrode of CCD chip 41 is electrically connected to the electrode terminals of the groups of wirings with ease and reliably. Therefore, Embodiment 4 is effective for reducing the size of the solid-state image sensing apparatus.

Second, in Embodiment 5, since the CCD chip, which has a large number of pixels to be highly accurate and, as a result, an yield ratio generally has to be extraordinarily low, is produced in the separate process, only defect-free CCD chips are put into the assembly process, thereby reducing the total cost.

Third, in Embodiment 6, the electrodes of CCD chip 41 and peripheral circuit elements 43 are connected to the electrode terminal of group of wirings by mounting technique or wire-bonding method, both are classic techniques and have high reliability based on ample experience of mounting engineering and automatic mounting machines. Since the surface on which the circuit elements 43 are formed is situated upward, a shading film 48 is required; however, when defects are found in the CCD chip 41 or the peripheral circuit elements 43, the defective parts can be easily replaced and the other parts also can be used again. In FIG. 7, a glass substrate 49 is made from the shading film by being deposited with metal or by sputtering.

As described above, the solid-state image sensing apparatus in Embodiments 4, 5, or 6 is used depending on a requested performance, price, and application.

FIG. 8 is a cross section of the solid-state image sensing apparatus used in Embodiment 7. A different point from the above embodiments is this: the CCD chip and peripheral circuit elements are mounted in multilayered structure situated in the package, therefore, the package structure of this embodiment is different from those of the above embodiments, namely, the CCD chip and peripheral circuit elements are inserted into the package from the through hole comprising two openings both having wide and different opening areas.

A structure and manufacturing method of Embodiment 7 is described as follows. In FIG. 8, a package 50 having an original structure is employed in Embodiment 7. A first opening 51 having a small opening area is disposed on a first end face, a second opening 52 having a large opening area and a third opening 53 having the larger opening area than that of the opening 52 are disposed on a second end face. Regarding a package 50, its upper frame 50a has the first opening 51 and the second opening 52, and also has a bent inner lead 54 situated therein. A first end of the inner lead 54 forms an exposed terminal 54a of the inner lead from a step situated between the first opening 51 and second opening 52. A second terminal 54b of inner lead 54 bent and extended downward from inside of the upper frame 50a is sealed between a lower frame 50b and the upper frame 50a, and the end of the terminal 54b is connected in the package to a junction point of an inner lead terminal 54c exposed from a step between the second opening 52 and third opening 53 with an outer lead 55 which is bent outside of the package 50.

The manufacturing method shown in FIG. 8 is, first, as same as the Embodiment 1, the epoxy resin mixed with

inorganic filler is injected into a mold where the lead frame comprising the inner lead 54 made of phosphor bronze, etc. and the outer lead 55 is disposed, and is inmolded at a high temperature. Then the package 50 is taken out from the mold. A frame body of the lead frame is cut away, and the outer lead 55 is bent toward the inlet 26, thereby forming the package 50. The bump 29 is formed on the electrode pad 28 of the CCD chip 27, whose back side is held by a mounting jig(not shown), and the CCD chip 27 is inserted into the package 50. Then, the bump 29 is press-fitted and connected to the inner lead terminal 54a which is disposed at a first step situated on the upper frame of the package 50. During this press-fit operation, a position signal is feed backed from an optical position adjusting device(not shown) disposed in front of the CCD chip 27 to the mounting jig, thereby an orientation of the CCD chip 27 is finely adjusted and the CCD chip 27 is positioned at the back side of the step of the package 50. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the package 50, and finally, the CCD chip 27 is accurately mounted to the package 50.

Then, the peripheral circuit elements 43 are also inserted into the lower frame 50b of package 50 from the third opening 53, and the electrode pad 44 of peripheral circuit elements 43 are connected via the bump 29 by press-fit to the second inner lead terminal 54c which is exposed from the step between the second opening 52 and third opening 53. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the peripheral circuit elements 43 to the package 50, and finally, the peripheral circuit elements 43 are accurately mounted to the package 50.

Thus, according to Embodiment 7, the CCD chip 27 and peripheral circuit elements 43 are disposed in multilayered or vertical structure within the package 50, and the driving circuit can be incorporated into the solid-state image sensing apparatus, thereby reducing an area occupied by parts mounted on the substrate. As a result, a high density mounting into a small size video camera can be realized.

A protection panel 56, made of transparent material such as glass, is shown in FIG. 8. The protection panel 56 protects the inside of solid-state image sensing apparatus; however, whether using of this protection panel 56 or not does not change the functions as well as effects of the present invention described in the above embodiments.

In Embodiment 5 through Embodiment 7, the tip of inner lead can be slightly protruded from the opening toward inside of package, as described in Embodiment 3. Thus, the optical positioning and bonding with the bump can be completed with ease thanks to the elasticity of the inner lead tip. Further, in the above Embodiments 1 and 2, the case is described that the bump 29 is disposed on the electrode pad 28 of CCD chip 27; however, the bump 29 can be disposed at the tip of inner lead 22 and connected with the electrode pad 47 of CCD module 46.

In Embodiment 5 through Embodiment 7, the electrode pad 47 of CCD module 46 can be connected to the inner lead terminal via, instead of the bump 29, the anisotropic conductor which has only vertical conductivity, as described in Embodiment 4.

Industrial Applicability

According to the above solid-state image sensing apparatus and the manufacturing method thereof of the present

invention, the invention relates to the solid-state image sensing apparatus comprising a through hole therein, the lead frame comprising the inner and outer leads which are sealed in the package, and the CCD chip as well as peripheral circuit elements mounted in the package, and also relates to the manufacturing method of the same. The package has the openings on both end faces, and the areas of the openings differ with each other. The CCD chip is inserted from the larger opening into the package, thereby sealing the through hole. Since the electrode pads of CCD chip and that of the peripheral circuit elements are connected to the inner leads via the anisotropic conductor, a number of manufacturing processes can be greatly reduced. Further, the mounting jig of CCD chip is disposed behind the CCD chip and the CCD chip is optically positioned from the front, thus highly accurate positioning can be achieved. As a result, the solid-state image sensing apparatus, which enables a video camera to reproduce vivid colors as well as fine pictures, can be manufactured at a low cost.

What is claimed is:

1. A solid-state image sensing apparatus comprising:
 - a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,
 - a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and
 - a solid-state image sensing device mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.
2. A solid-state image apparatus comprising:
 - a package comprising a main body having a through hole therein, said main body having a top surface and a bottom surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward the center of said through hole, said ledge comprising an upper surface and a lower surface;
 - a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and
 - a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;
 said solid-state image sensing device being secured to said main body of said package via an adhesive.
3. The solid-state image sensing apparatus of claim 2, wherein each of the electrode pads is connected to the inner lead via a bump.
4. The solid-state image sensing apparatus of claim 2, wherein each of the electrode pads is connected to the inner lead via an anisotropic conductor having only vertical conductivity.
5. The solid-state image sensing apparatus of claim 2, wherein a tip of the inner lead to which the electrode pad is connected extends beyond said ledge.
6. A solid-state image sensing apparatus comprising:
 - a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,
 - a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,
 - a substrate on which a solid-state image sensing device and a peripheral circuit chip are mounted being inserted into the package from a wider opening thereof, and

an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,

said substrate being secured to said package via an adhesive.

7. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package,

a semiconductor substrate having a solid-state image sensing device and a peripheral circuit chip disposed on an upper surface thereof, said semiconductor substrate being inserted into a plastic package via the larger of two openings formed in said package, and

an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around the smaller opening of said package,

said semiconductor substrate being secured to said package via an adhesive.

8. The solid state image sensing apparatus of claim 6 or claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the solid-state image sensing device.

9. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via a bump.

10. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity.

11. The solid-state image sensing apparatus of claim 6 or claim 7, wherein an electrode pad formed on the substrate is connected to the inner lead at an outer portion of said lead, said outer portion of said lead extending into the openings of the package.

12. A solid-state image sensing apparatus comprising:

a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and

a solid-state image sensing device and a peripheral circuit chip both mounted in said package, said solid-state image sensing device being connected to a first inner lead exposed beneath a first step surface formed in said package, said solid-state image sensing device being secured to said package via an adhesive, and said peripheral circuit chip being connected to a second inner lead exposed beneath a second step surface formed in said package, said peripheral circuit chip being secured to said package via an adhesive.

13. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device mounted in said package, said manufacturing method comprising the steps of:

inserting said solid-state image sensing device into said through hole,

connecting an electrode pad of the solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjust-

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ing the optical positioning of said solid-state image sensing device, and

securing said solid-state image sensing device to the package with an adhesive.

14. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising the steps of:

forming said solid-state image sensing device and a group of wirings on a semiconductor substrate,

mounting said peripheral circuit chip on the solid-state image sensing device to connect with said group of said semiconductor surface,

inserting said semiconductor substrate into the through hole,

connecting an electrode pad disposed on the semiconductor substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of said solid-state image sensing device, and

securing the semiconductor substrate on which the solid-state image sensing device and the peripheral circuit chip are mounted to the package via an adhesive.

15. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:

mounting said solid-state image sensing device and said peripheral circuit chip on a substrate where a group of wirings is disposed in order to connect the solid-state image sensing device and the peripheral circuit chip to the group of wirings,

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inserting the semiconductor substrate into the through hole,

connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, and

securing the semiconductor substrate on which said solid-state image sensing device and said peripheral circuit chip are mounted to the package via an adhesive.

16. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in the package, and a solid-state image sensing device as well as a peripheral circuit chip mounted in said package, said manufacturing method comprising steps of:

inserting said solid-state image sensing device into the through hole,

connecting an electrode pad of the solid-state image sensing device to a first inner lead via a bump or an anisotropic conductor having only vertical conductivity, while simultaneously adjusting the optical positioning of the solid-state image sensing device, said first inner lead being disposed beneath a first step surface formed in said package,

securing the solid-state image sensing device to the package via an adhesive,

inserting the peripheral circuit chip into the through hole, connecting an electrode pad of the peripheral circuit chip to a second inner lead via a bump or an anisotropic conductor having only vertical conductivity, to complete an electrical connection, said second inner lead being disposed beneath a second step surface formed in said package, and

securing the peripheral circuit chip to the package via an adhesive.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,952,714

DATED : September 14, 1999

INVENTOR(S) : Sano et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page:

At the end of the "FOREIGN PATENT DOCUMENTS" section, insert:

--63-274162 11/88 Japan--.

Signed and Sealed this
Fifth Day of September, 2000

Attest:



Q. TODD DICKINSON

Attesting Officer

Director of Patents and Trademarks

PATENT APPLICATION SERIAL NO. 08/809845

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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Abstract of the Disclosure

A lead frame 24 comprising an inner lead 22 and outer lead 23 is sealingly filled from a through-hole into a package 21. A CCD chip 27 is inserted from an inlet 26 into the package 21. An electrode pad 28 is
5 connected to the inner lead 22 via a bump 29 to complete an optical positioning and an electrical connection, then the positions of these components are fixed by glue. As a result, a solid-state image sensing apparatus can be manufactured at a low cost, and an accurate positioning can be realized. Thus, the solid-state image sensing apparatus can be employed
10 to a video camera of high quality picture to reproduce vivid colors and fine pictures.

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Solid-state Image Sensing Apparatus and
Manufacturing Method Thereof

Field of Engineering

5 The present invention relates to a solid-state image sensing apparatus
using a solid-state image sensing device (hereinafter called CCD chip) in a
package made of plastic, ceramic or glass(hereinafter called package), more
particularly to a solid-state image sensing apparatus using three CCD chips,
which is used for a video camera and required severe optical positioning
10 accuracy. The present invention also relates to the manufacturing method of
the solid-state image sensing apparatus.

Background of Engineering

Recently, a video camera, a home-use video camera among others, has
15 been equipped with the better functions in addition to its reducing size and
weight. Consumers have demanded the better quality picture such as of high
color fidelity as well as displaying detail. In order to satisfy this demand,
technical levels relating to many components of the video camera have been
highly enhanced, and in particular, performance of the CCD chip which is
20 called "a heart of video camera," has been remarkably progressed in
increasing a number of pixels. On the other hand, a home-use video camera
of which main stream has been one-eye video camera using one CCD chip,
starts replacing the one-eye with a three-eye using three CCD chips which has
been employed in an expensive professional video camera, namely, three CCD
25 chips correspond to Red, Green, Blue colors. Comparing with the one-eye

video camera, the three-eye video camera is required an ultra positioning accuracy because three CCD chips are to be optically disposed at correct positions. Since the home-use video camera has been designed to be portable and smaller in size, many of the components are mounted in an extreme high density. Therefore, the solid-state image sensing apparatus for the home-use video camera is required to change itself in its own structure.

Fig. 9 and Fig. 10 depict a conventional solid-state image sensing apparatus. Fig. 9 is a cross section of a solid-state image sensing apparatus in a ceramic package which was once a mainstream. A ceramic package 1, on which metallized conductor 2 is formed, has a concave part 3 in the center thereof. On the concave part 3, a CCD chip 4 is mounted by die bonding, and an electrode pad 6 of CCD chip 4 is wire-bonded to the metallized conductor 2 by a metal lead 7. A lead terminal 8 is deposited to an end face of metallized conductor 2 exposing itself from the side of ceramic package 1.

Fig. 10 is a cross section of a solid-state image sensing apparatus in a plastic package. A lead frame 11 comprising an inner lead 9 and an outer lead 10 is inmolded in a plastic package 12. At a center of the plastic package, a concave portion 13 is situated. The CCD chip 4 is di-bonded by conductive paste 14 to the concave portion 13, and the electrode pad 6 on the CCD chip 4 is wire-bonded to the inner lead 9 by the metal lead 7 as same as the case of the ceramic package shown in Fig. 9.

However, according to the above conventional solid-state image sensing apparatus and the manufacturing method thereof, the CCD chip in either the ceramic package 1 or plastic package 12, is mounted on the base of either concave part 3 or 13 by die bonding. When this conventional solid-state

image sensing apparatus having the above structure is mounted to the three-eye video camera and is accurately positioned in optical manner, the base of concave part 3 or 13 of ceramic package 1 or plastic package 12 to which the CCD chip 4 is die-bonded should be processed in high accuracy. Also a level of parallelism with regard to the base and an upper face of ceramic package 1 or plastic package 12 should be highly accurate. These factors not only increase a cost of ceramic package 1 or plastic package 12 but also raise a cost of mounting process of CCD chip 4. The wire-bonding method for connecting the electrode pad 6 of CCD chip 4 with the metallized conductor 2 or the inner lead 9 via the metal lead 7 is a classic manufacturing technique expecting a low defect ratio and requiring little effort for replacing chips; however, this method limits the size reduction of solid-state image sensing apparatus, and cannot fully respond to a request of reducing a size thereof from the market of home-use video camera.

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Disclosure of the Invention

The present invention aims to provide a solid-state image sensing apparatus mountable to a video camera of high quality picture, which not only can reproduce vivid colors and fine pictures but also can be manufactured at a low cost. The present invention also aims to provide a manufacturing method of the solid-state image sensing apparatus.

The solid-state image sensing apparatus according to the present invention comprises a package having a through hole therein, a lead frame comprising an inner lead and an outer lead sealed therein, and a CCD chip loaded therein. Both the end faces of the package have different opening

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areas. The CCD chip can be mounted from the opening having the wider opening area, and thereby shutting the through hole tightly.

Another type of the solid-state image sensing apparatus according to the present invention has the opening of the package. The electrode pad of
5 CCD chip is connected via the inner lead to the opening, and the opening area is smaller than the entire area of CCD chip.

Still another type of the solid-state image sensing apparatus according to the present invention has the package having a through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and a
10 substrate on which the CCD chip and peripheral circuit elements are mounted being loaded into the package from the opening which has the wider opening area, and the electrode pad of substrate connected to the inner lead exposed from a periphery of end face of the opening which has the smaller opening area.

15 Further another type of the solid-state image sensing apparatus of the present invention has the package having a through hole therein, and the lead frame comprising the inner lead and outer lead sealed therein, and the peripheral circuit elements mounted on a substrate which is disposed on an upper surface of the substrate excluding the surface where the CCD chip is
20 mounted. The two substrates are loaded into the package from the opening which has the wider opening area. The electrode pad is connected to the inner lead exposed from the periphery end face of the opening which has the smaller opening area.

Another type of the solid-state image sensing apparatus of the present
25 invention has the package having the through hole therein, and the lead

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positioning as well as electrical connection is completed. Then the back side of the substrate having the CCD chip and peripheral circuit elements thereon is glued to the package by adhesive.

Still another manufacturing method according to the present invention
5 relates to the solid-state image sensing apparatus which has the package comprising the through hole therein, and the lead frame comprising the inner lead and outer lead sealingly filled therein, and the CCD chip as well as the peripheral circuit elements loaded therein. The CCD chip and the peripheral
10 circuit elements are mounted on the substrate where the group of wirings were already disposed, and the CCD chip and the peripheral circuit elements are connected to the group of wirings. The substrate is loaded into the through hole from the opening which has the wider opening area. The electrode pad disposed at periphery of the upper surface of the substrate is connected to the inner lead via the bump or anisotropic conductor so that the
15 optical positioning as well as electrical connection is completed. Then the back side of the substrate having the CCD chip and peripheral circuit elements thereon is glued to the package by adhesive.

Further another manufacturing method according to the present invention relates to the solid-state image sensing apparatus which has the
20 package comprising the through hole therein, and the lead frame comprising the inner and outer leads sealed therein, and the CCD chip as well as the peripheral circuit elements mounted therein. The CCD chip is loaded into the through hole of the package from the opening which has the wider opening area, and the electrode pad is connected to the first inner lead via the bump or
25 the anisotropic conductor so that optical positioning as well as electrical

connection is completed. Then the back side of the CCD chip is glued to the package by adhesive, and the peripheral circuit elements is loaded into the through hole from the same opening used when the CCD chip loaded. The electrode pad of the peripheral circuit elements is electrically connected to the
5 second inner lead via the bump or the anisotropic conductor, and then the back side of the peripheral circuit elements is glued to the package by adhesive.

According to the present invention, the through hole is provided in the package, and the CCD chip can be loaded into the package from the bottom
10 side, namely from the opening which has the wider opening area. The electrode pad of CCD chip is electrically connected to the bump or the anisotropic conductor, and also optically positioned at the same time. Thus, the present invention can reduce a number of manufacturing processes comparing with the conventional method which requires two bonding
15 processes including the die-bonding of CCD chip and the wire-bonding of electrode pad. Further, because a loading jig for the CCD chip can be disposed at the back side of CCD chip, the CCD chip can be optically positioned with ease from the front, thus more accurate positioning can be expected.

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Brief Description of the Drawings

Fig. 1 is a cutaway perspective view of the solid-state image sensing apparatus of an exemplary embodiment of the present invention.

Fig. 2 is a cross section of the solid-state image sensing apparatus of the
25 first exemplary embodiment of the present invention.

Fig. 3 is a cross section of the solid-state image sensing apparatus of the second exemplary embodiment of the present invention.

Fig. 4 is a cross section of the solid-state image sensing apparatus of the third exemplary embodiment of the present invention.

5 Fig. 5 is a cross section of the solid-state image sensing apparatus of the fourth exemplary embodiment of the present invention.

Fig. 6 is a cross section of the solid-state image sensing apparatus of the fifth exemplary embodiment of the present invention.

10 Fig. 7 is a cross section of the solid-state image sensing apparatus of the sixth exemplary embodiment of the present invention.

Fig. 8 is a cross section of the solid-state image sensing apparatus of the seventh exemplary embodiment of the present invention.

Fig. 9 is a cross section of a conventional solid-state image sensing apparatus.

15 Fig. 10 is a cross section of another conventional solid-state image sensing apparatus.

The Description of Preferred Embodiment

An exemplary embodiment of the present invention is stated here by referring to Fig. 1, which is a cutaway perspective view of an exemplary
20 embodiment according to the present invention. A lead frame 24 comprising an inner lead 22 and an outer lead 23 is molded in a package 21. As Fig. 1 depicts, a through hole is provided at the center of the package 21, and in front side of the package 21, an opening 25 which has a smaller opening area
25 is situated, and another opening 26 (hereinafter called "inlet") which has a

wider opening area is situated at the back side thereof. The area of opening 25 is smaller than that of CCD chip 27. An inner lead 22 is exposed from the back side of a step between the opening 25 and the inlet 26, and the inner lead 22 is electrically connected to a bump 29 disposed on an electrode 28 of CCD
5 chip 27.

Next, a manufacturing method according to the present invention is described. Fig. 2 is a cross section of the solid-state image sensing apparatus according to the first exemplary embodiment of the present invention. Epoxy resin mixed with inorganic filler is injected into a mold where the lead frame
10 24 made of phosphor bronze, etc. is disposed, and is inmolded at a high temperature. Then the package 21 is taken out from the mold. A frame body of the lead frame 24 is cut away, and the outer lead 23 is bent toward the inlet 26, thereby forming the package 21. The bump 29 is formed on the electrode pad 28 of the CCD chip 27, whose back side is held by a mounting
15 jig(not shown), and the CCD chip 27 is inserted into the package 21 from the inlet 26. Then, the bump 29 is press-fitted and connected to the inner lead 22 which is exposed from a back side of the step situated between the opening 25 and the inlet 26. During this press-fit operation, a position signal is feedbacked from a optical position adjusting device(not shown) disposed in
20 front of the CCD chip 27 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 27 and disposing the CCD chip 27 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the
25 package 21, and finally, the CCD chip 27 is accurately mounted to the

package 21.

Fig. 3 is a cross section of the solid-state image sensing apparatus used in a second exemplary embodiment of the present invention. A different point from the first exemplary embodiment is this: a tip 22a of the inner lead 5 22 slightly protrudes from the opening 25 toward inside. This structure facilitates the optical positioning as well as the bonding between the inner lead and the bump 29 thanks to elasticity of the tip 22a.

In the first and second exemplary embodiments, the bump 29 is disposed on the electrode pad 28; however, the bump 29 may be disposed at 10 the tip of inner lead 22 and coupled with the electrode pad 28 of CCD chip 27.

Fig. 4 is a cross section of the solid-state image sensing apparatus used in Embodiment 3. The inner leads 22 are cut so that they seem to be arranged in parallel from their cross sectional view. In this embodiment, the electrode pad 28 of CCD chip 27 and the inner leads 22 are connected via 15 the anisotropic conductor 31 which has conductivity in only the vertical direction instead of via the bump 29. Thanks to the elasticity of anisotropic conductor 31 made of conductive rubber or the like, the CCD chip 27 can be optically positioned with ease as same as the second embodiment.

According to this exemplary embodiment, an assembly process can be 20 substantially simplified because of the structure as follows: the through hole is provided in the package 21, and the CCD chip 27 is loaded from the inlet 26 which is situated on the back side of package 21, namely, on the side of outer leads, and the exposed inner lead 22 from the back side of the step situated between the opening 25 and the inlet 26 is connected to the electrode pad 28 of 25 CCD chip 27 electrically via the bump or anisotropic conductor, at the same

time, an optical positioning between the inner lead 22 and the electrode pad 28 is completed. Further, since the mounting jig of CCD chip 27 can be disposed on the back side of CCD chip 27, the CCD chip 27 can be optically positioned from the front with ease, thus an accurate positioning can be
5 achieved.

Fig. 5 is a cross section of the solid-state image sensing apparatus used in Embodiment 4. Epoxy resin mixed with inorganic filler is injected into a mold where the lead frame 24 made of phosphor bronze, etc. are disposed, and is inmolded at a high temperature. Then the package 21 is taken out from
10 the mold. A frame body of the lead frame 24 is cut away, and the outer lead 23 is bent toward the inlet 26, thereby forming the package 21.

A substrate 42 comprising a semiconductor substrate such as silicon wafer, on which a group of wirings (not shown) and a CCD chip 41 are formed, and on a part of the substrate surface, a peripheral circuit elements 43 are disposed in
15 a face-down way; the peripheral circuit elements 43 were produced in a separate manufacturing process. A bump 29 disposed on an electrode pad 44 of the peripheral circuit elements is connected to an electrode pad 45 of the group of wirings on the substrate 42, thereby producing a function device 46 (hereinafter called "CCD module"). A back side of the CCD module 46 is held
20 by a mounting jig (not shown), and is inserted from the inlet 26 into the package 21. Then, the bump 29 on an electrode pad 47 disposed around the CCD module 46 is press-fitted to the inner lead 22 exposed from the back side of the step situated between the opening 25 and the inlet 26, thus the bump 29 is electrically connected with the inner lead 22. During this press-fit
25 operation, a position signal is feedbacked from an optical position adjusting

device(not shown)disposed in front of the CCD chip 41 to the mounting jig, thereby finely adjusting an orientation of the CCD chip 41 and disposing the CCD module 46 on the back side of the step of the package 21. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity
5 from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 41 to the package 21, and finally, the CCD chip 41 is accurately mounted to the package 21.

Fig. 6 is a cross section of the solid-state image sensing apparatus used in Embodiment 5 of the present invention. This embodiment is one of
10 variations of Embodiment 4 described above. The method of accurately mounting the CCD chip 41 to the package21 is the same as that of the Embodiment 4 from the standpoints of structure and manufacturing, namely, the CCD module 46 on which the CCD chip, peripheral circuit elements and the group of wirings are formed, is inserted from the inlet 26, and the CCD
15 module 46is fixed to the package 21, while the optical position of CCD chip41 is fine adjusted. A different point from the Embodiment 4 is this: in Embodiment 4, the CCD chip is formed directly on the semiconductor substrate, which is to be the substrate 42 of the CCD module 46, through a circuit-chip-forming-process such as a direct diffusion process, on the other
20 hand in Embodiment 5, the CCD chip 41 as well as peripheral circuit elements 43 was already produced in a separate process, and the CCD chip 41 and peripheral circuit elements 43 are disposed on the substrate 42 on which the group of wirings have been formed, and thereby they are electrically connected to form the CCD module 46.

Accordingly, the substrate 42 used in this embodiment may be made of a material other than semiconductor. As shown in Fig. 6, when the CCD chip 41 produced in the separate process is mounted on the substrate 42, the electrode of CCD chip 41 is wire-bonded to the electrode terminal of the group of wirings by using a metal wire 47a.

Fig. 7 is a cross section of the solid-state image sensing apparatus used in Embodiment 6. This embodiment is also one of variations of Embodiment 5 above mentioned. A different point from Embodiment 5 is this: in Embodiment 5, the peripheral circuit elements 43 are connected to the substrate 42 via the bump 29 in the face-down way same as that in Embodiment 4; however, in this Embodiment 6, the peripheral circuit elements 43 are disposed on the substrate 42 in the face-up way (the face on which a circuit is formed is situated upward) as the CCD chip 41 is in Embodiment 5, and the electrode of peripheral circuit elements is wire-bonded to the electrode terminal of the group of wiring by using the metal wire 47a.

Embodiments 4, 5, and 6 have some similarities as well as differences with each other. An advantage of the solid-state image sensing apparatus in these embodiments are as follows.

First, in Embodiment 4, since the CCD chip 41 is formed on the substrate 42 together with other groups of wirings at the same time, the electrode of CCD chip 41 is electrically connected to the electrode terminals of the groups of wirings with ease and reliably. Therefore, Embodiment 4 is effective for reducing the size of the solid-state image sensing apparatus.

Second, in Embodiment 5, since the CCD chip, which has a large number of pixels to be highly accurate and, as a result, an yield ratio

generally has to be extraordinarily low, is produced in the separate process, only defect-free CCD chips are put into the assembly process, thereby reducing the total cost.

Third, in Embodiment 6, the electrodes of CCD chip 41 and peripheral
5 circuit elements 43 are connected to the electrode terminal of group of wirings by mounting technique or wire-bonding method, both are classic techniques and have high reliability based on ample experience of mounting engineering and automatic mounting machines. Since the surface on which the circuit
10 elements 43 are formed is situated upward, a shading film 48 is required; however, when defects are found in the CCD chip 41 or the peripheral circuit elements 43, the defective parts can be easily replaced and the other parts also can be used again. In Fig. 7, a glass substrate 49 is made from the shading film by being deposited with metal or by sputtering.

As described above, the solid-state image sensing apparatus in
15 Embodiments 4, 5, or 6 is used depending on a requested performance, price, and application.

Fig. 8 is a cross section of the solid-state image sensing apparatus used in Embodiment 7. A different point from the above embodiments is this: the
20 CCD chip and peripheral circuit elements are mounted in multilayered structure situated in the package, therefore, the package structure of this embodiment is different from those of the above embodiments, namely, the CCD chip and peripheral circuit elements are inserted into the package from the through hole comprising two openings both having wide and different opening areas.

25 A structure and manufacturing method of Embodiment 7 is described

as follows. In Fig. 8, a package 50 having an original structure is employed in Embodiment 7. A first opening 51 having a small opening area is disposed on a first end face, a second opening 52 having a large opening area and a third opening 53 having the larger opening area than that of the opening 52 are disposed on a second end face. Regarding a package 50, its upper frame 50a has the first opening 51 and the second opening 52, and also has a bent inner lead 54 situated therein. A first end of the inner lead 54 forms an exposed terminal 54a of the inner lead from a step situated between the first opening 51 and second opening 52. A second terminal 54b of inner lead 54 bent and extended downward from inside of the upper frame 50a is sealed between a lower frame 50b and the upper frame 50a, and the end of the terminal 54b is connected in the package to a junction point of an inner lead terminal 54c exposed from a step between the second opening 52 and third opening 53 with an outer lead 55 which is bent outside of the package 50.

The manufacturing method shown in Fig. 8 is, first, as same as the Embodiment 1, the epoxy resin mixed with inorganic filler is injected into a mold where the lead frame comprising the inner lead 54 made of phosphor bronze, etc. and the outer lead 55 is disposed, and is inmolded at a high temperature. Then the package 50 is taken out from the mold. A frame body of the lead frame is cut away, and the outer lead 55 is bent toward the inlet 26, thereby forming the package 50. The bump 29 is formed on the electrode pad 28 of the CCD chip 27, whose back side is held by a mounting jig(not shown), and the CCD chip 27 is inserted into the package 50. Then, the bump 29 is press-fitted and connected to the inner lead terminal 54a which is disposed at a first step situated on the upper frame of the package 50.

During this press-fit operation, a position signal is feedbacked from an optical position adjusting device(not shown) disposed in front of the CCD chip 27 to the mounting jig, thereby an orientation of the CCD chip 27 is finely adjusted and the CCD chip 27 is positioned at the back side of the step of the package 50. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the CCD chip 27 to the package 50, and finally, the CCD chip 27 is accurately mounted to the package 50.

Then, the peripheral circuit elements 43 are also inserted into the lower frame 50b of package 50 from the third opening 53, and the electrode pad 44 of peripheral circuit elements 43 are connected via the bump 29 by press-fit to the second inner lead terminal 54c which is exposed from the step between the second opening 52 and third opening 53. At the same time, ultra-violet hardening adhesive 30 is injected in a specified quantity from a dispenser which is situated beside a press-fit jig to glue four sides of the peripheral circuit elements 43 to the package 50, and finally, the peripheral circuit elements 43 are accurately mounted to the package 50.

Thus, according to Embodiment 7, the CCD chip 27 and peripheral circuit elements 43 are disposed in multilayerd or vertical structure within the package 50, and the driving circuit can be incorporated into the solid-state image sensing apparatus, thereby reducing an area occupied by parts mounted on the substrate. As a result, a high density mounting into a small size video camera can be realized.

A protection panel 56, made of transparent material such as glass, is shown in Fig. 8. The protection panel 56 protects the inside of solid-state

image sensing apparatus; however, whether using of this protection panel 56 or not does not change the functions as well as effects of the present invention described in the above embodiments.

In Embodiment 5 through Embodiment 7, the tip of inner lead can be slightly protruded from the opening toward inside of package, as described in Embodiment 3. Thus, the optical positioning and bonding with the bump can be completed with ease thanks to the elasticity of the inner lead tip. Further, in the above Embodiments 1 and 2, the case is described that the bump 29 is disposed on the electrode pad 28 of CCD chip 27; however, the bump 29 can be disposed at the tip of inner lead 22 and connected with the electrode pad 47 of CCD module 46.

In Embodiment 5 through Embodiment 7, the electrode pad 47 of CCD module 46 can be connected to the inner lead terminal via, instead of the bump 29, the anisotropic conductor which has only vertical conductivity, as described in Embodiment 4.

Industrial Applicability

According to the above solid-state image sensing apparatus and the manufacturing method thereof of the present invention, the invention relates to the solid-state image sensing apparatus comprising a through hole therein, the lead frame comprising the inner and outer leads which are sealed in the package, and the CCD chip as well as peripheral circuit elements mounted in the package, and also relates to the manufacturing method of the same. The package has the openings on both end faces, and the areas of the openings differ with each other. The CCD chip is inserted from the larger opening into

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the package, thereby sealing the through hole. Since the electrode pads of CCD chip and that of the peripheral circuit elements are connected to the inner leads via the anisotropic conductor, a number of manufacturing processes can be greatly reduced. Further, the mounting jig of CCD chip is disposed behind the CCD chip and the CCD chip is optically positioned from the front, thus highly accurate positioning can be achieved. As a result, the solid-state image sensing apparatus, which enables a video camera to reproduce vivid colors as well as fine pictures, can be manufactured at a low cost.

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(a) a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings.

(c) a solid-state image sensing element (CCD chip) mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole.

(a) a package having a through hole therein, openings on both end faces thereof.

(c) a solid-state image sensing element (CCD chip) mounted in said package, said CCD chip having an electrode pad which is connected via said inner lead to said opening of which area is smaller than an entire area of said CCD chip.

4. The solid-state image sensing apparatus of Claim 2 wherein the electrode pad of the CCD chip is connected to the inner lead via an anisotropic conductor having only vertical conductivity.

5. The solid-state image sensing apparatus of Claim 2 wherein
25 a tip of the inner lead to which the electrode pad of the CCD chip is connected

[illegible]

an upper surface of the CCD chip.

9. The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad of the substrate is connected to the inner lead via a bump.

5 10. The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad of the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity.

10 11. The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad of the substrate is connected to the inner lead of which tip is protruded from around the opening of the package.

12. A solid-state image sensing apparatus comprising:

(a) a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

15 (b) a lead frame comprising the inner and outer leads, said lead frame being sealed in said package which has a through hole, and

20 (c) a solid-state image sensing element (CCD chip) and a peripheral circuit element both mounted in said package, said CCD chip being connected to a first inner lead exposed from a first step situated to said package, and said peripheral circuit element being connected to a second inner lead exposed from a second step situated to said package.

25 13. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner and outer leads, said lead frame being sealed in said package, and a solid-state image sensing element (CCD chip) mounted in said package, said manufacturing method comprising the steps of:

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(a) insert said CCD chip into said through hole from a wider opening area of the package,

(b) connect an electrode pad of the CCD chip inserted in the through hole to the inner lead via a bump or an anisotropic conductor, which
5 has only vertical conductivity, to complete an optical positioning as well as electrical connection, and

(c) fix a back side of the CCD chip to the package with glue.

14. A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame
10 comprising the inner and outer leads, said lead frame being sealed in said package, and a solid-state image sensing element (CCD chip) as well as a peripheral circuit element mounted in said package, said manufacturing method comprising the steps of:

(a) form said CCD chip and a group of wirings on a semiconductor
15 substrate,

(b) mount said peripheral circuit element on a surface except the preoccupied place by the CCD chip to connect with said group of wiring,

(c) insert said substrate into the through hole from a wider opening of the package,

20 (d) connect an electrode pad disposed on around the substrate to the inner lead via a bump or an anisotropic conductor, which has only vertical conductivity, to complete an optical positioning and electrical connection, and

(e) fix a back side of the substrate on which the CCD chip and the peripheral circuit element are mounted to the package with glue.

[illegible]

(b) connect an electrode pad of the CCD chip to a first inner lead via an anisotropic conductor, which has only vertical conductivity, to an optical positioning and electrical connection,

(c) fix a back side of the CCD chip to the package with glue,

5 (d) insert the peripheral circuit element into the through hole from the wider opening of the package,

(e) connect an electrode pad of the peripheral circuit element to a second inner lead via a bump or an anisotropic conductor, which has only vertical conductivity, to complete an electrical connection, and

10 (f) fix a back side of the peripheral circuit element to the package
with glue.

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List of Reference Symbols in the Drawings

21. package
22. inner lead
- 22a. tip of inner lead
- 5 23. outer lead
24. lead frame
25. opening
26. inlet
27. CCD chip (solid-state image sensing element)
- 10 28. electrode pad
29. bump
30. ultraviolet hardening adhesive
31. anisotropic conductor
41. CCD chip
- 15 42. substrate
43. peripheral circuit element
44. electrode pad
45. electrode pad of a group of wiring
46. CCD module
- 20 47. electrode pad
- 47a. metal wire
48. shading film
49. glass substrate
50. package
- 25 50a. upper frame

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- 50b. lower frame
- 51. first opening
- 52. second opening
- 53. third opening
- 5 54. inner lead terminal
- 54a. first terminal of inner lead
- 54b. another terminal of inner lead
- 54c. second terminal of inner lead-
- 55. outer lead
- 10 56. protection panel
- 1. ceramic package
- 2. metallized conductor
- 3. concave part
- 15 4. CCD chip
- 5. conductive adhesive
- 6. electrode pad
- 7. metal wire
- 8. lead terminal
- 20 9. inner lead
- 10. outer lead
- 11. lead frame
- 12. plastic package
- 13. concave part
- 25 14. conductive paste

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Docket No. 43890/225

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF, the specification of which

(check one)

_____ is attached hereto.

X

_____ was filed on July 30, 1996 as United States Application No. or PCT International Patent Application Number PCT/JP96/02142 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

| Prior Foreign Application(s) | Priority Claimed |
|---|--------------------------------|
| <u>7-197365</u> <u>Japan</u> <u>02/ August /1995</u> | <u>X</u> Yes <u> </u> No |
| (Number) (Country) (Day/Month/Year Filed) | |
| <u> </u> <u> </u> <u> </u> | <u> </u> Yes <u> </u> No |
| (Number) (Country) (Day/Month/Year Filed) | |
| <u> </u> <u> </u> <u> </u> | <u> </u> Yes <u> </u> No |
| (Number) (Country) (Day/Month/Year Filed) | |

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| |
|---|
| <u>PCT/JP96/02142</u> <u>July 30, 1996</u> <u>Pending</u> |
| (Appln. Serial No.) (Filing Date) (Status-patented, pending, abandoned) |
| <u> </u> <u> </u> <u> </u> |
| (Appln. Serial No.) (filing Date) (Status-patented, pending, abandoned) |

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P03

P13943

10- I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); Edward E. Kubasiewicz (Reg. No. 30,020); Paul Devinsky (Reg. No. 28,553); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Kenneth L. Cage, Esq.
MCDERMOTT, WILL & EMERY
1850 K STREET, N.W., SUITE 450
WASHINGTON, D.C. 20006-2296
Telephone: 202-778-8300

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Yoshikazu SANO

1-10 Inventor's signature Yoshikazu Sano Date June 6, 1997
Residence* 3-30-702, Yuhigaoka-cho, Tennoji-ku, Osaka-shi, Osaka 543 Japan JPX
Post Office Address Same as above Citizenship Japanese

2-10 Full name of second inventor Sumio TERAKAWA

Inventor's signature Sumio Terakawa Date June 6, 1997
Residence* 1-20-C403, Minamikasugaoka, Ibaraki-shi, Osaka, 567 Japan JPX
Post Office Address Same as above Citizenship Japanese

3-10 Full name of third inventor Eiichi TSUJII

Inventor's signature Eiichi Tsujii Date June 6, 1997
Residence* 35-23, Teradashoudou, Jouyou-shi, Kyoto, 610-01 Japan JPX
Post Office Address Same as above Citizenship Japanese

4-10 Full name of fourth inventor Masaji ASAUMI

Inventor's signature Masaji Asaumi Date June 6, 1997
Residence* 111-1017, Sanintokiso-cho, Ukyo-ku, Kyoto-shi, Kyoto, 615 Japan JPX
Post Office Address Same as above Citizenship Japanese

5-10 Full name of fifth inventor Yoshikazu CHATANI

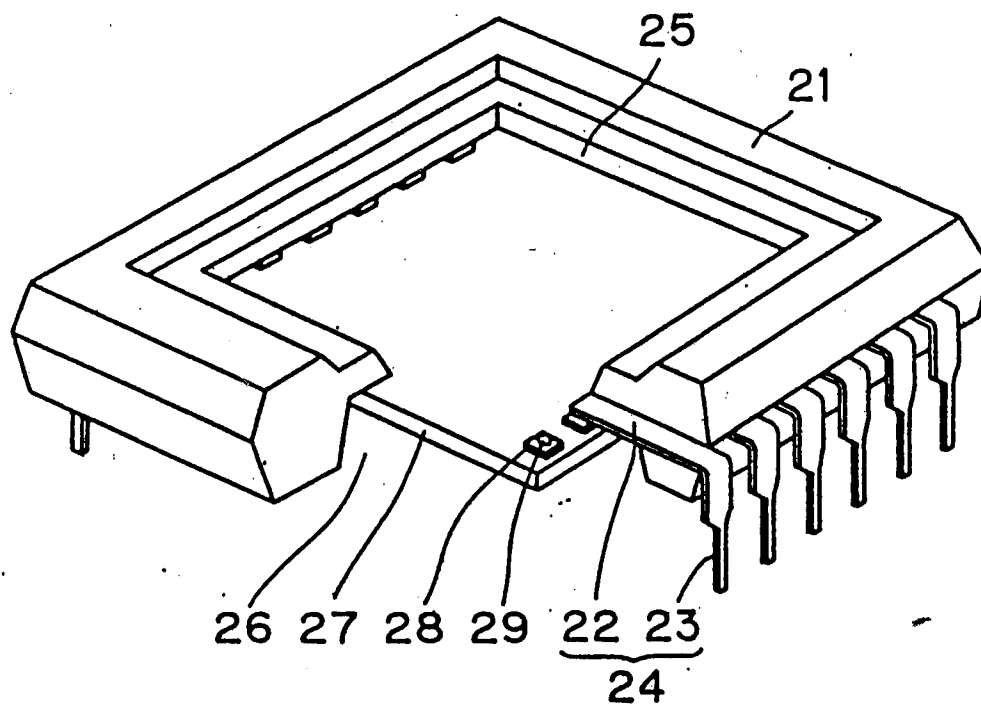
Inventor's signature Yoshikazu Chatani Date June 6, 1997
Residence* 8, Misasaqikamoto-cho, Yamashina-ku, Kyoto-shi, Kyoto, 607 Japan JPX
Post Office Address Same as above Citizenship Japanese

* City and State, or City and Country for foreign inventors

257
222
page

1/8

Fig.1



08/809845-001697

Fig.2

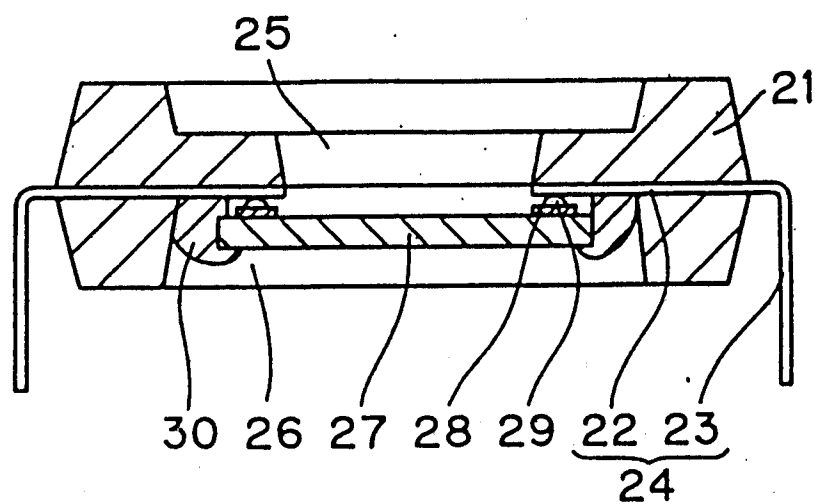
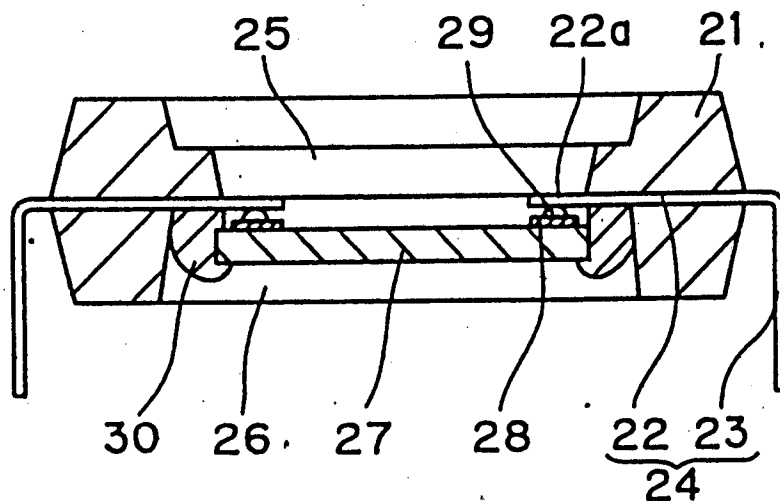


Fig.3



3/8

Fig.4

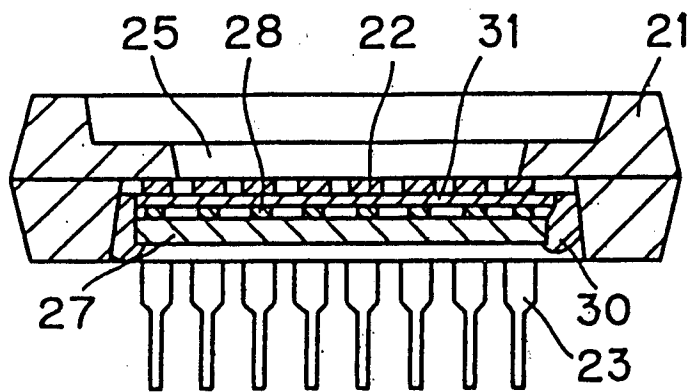


Fig.5

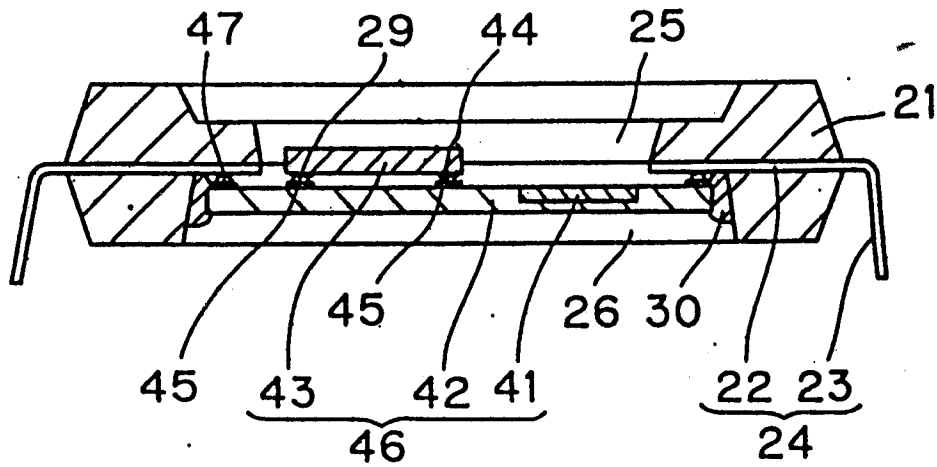


Fig.6

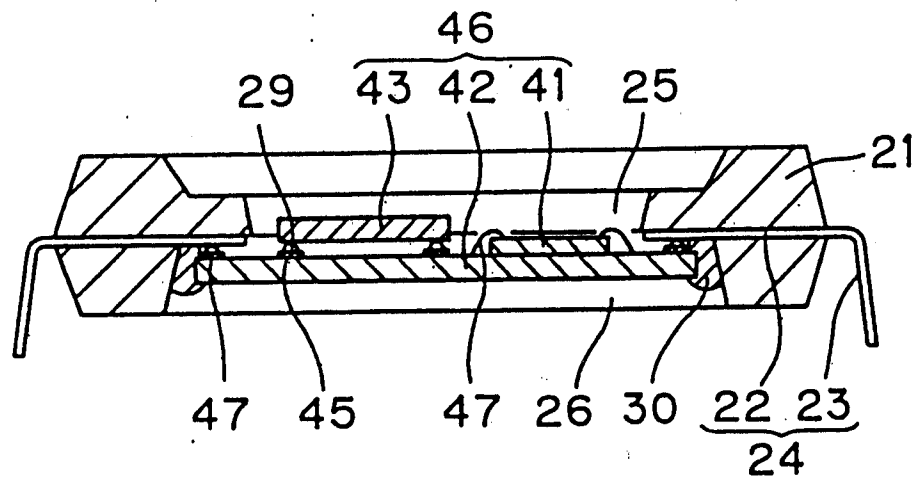


Fig.7

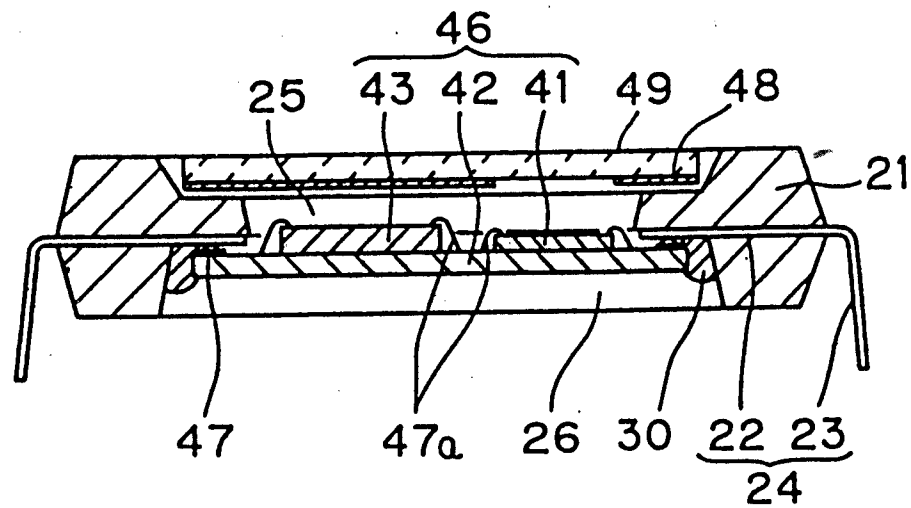


Fig.8

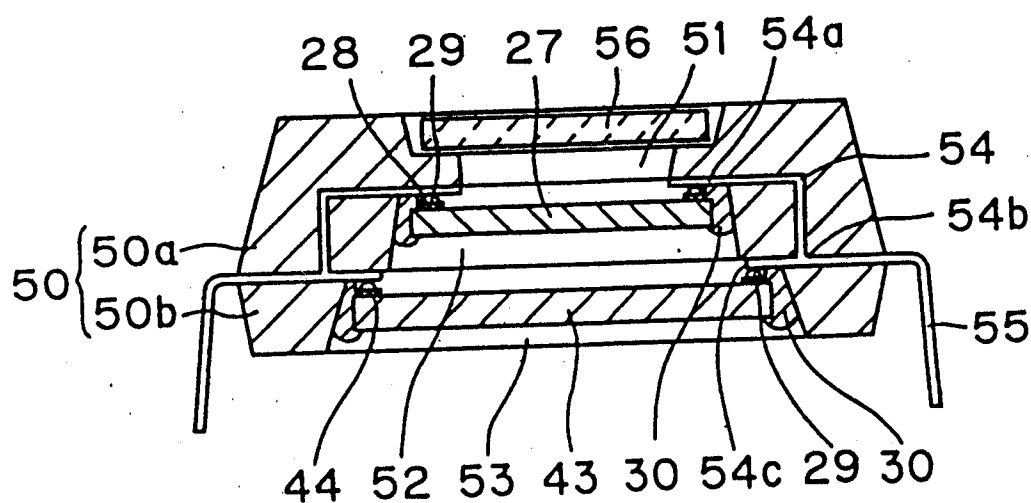


Fig.9

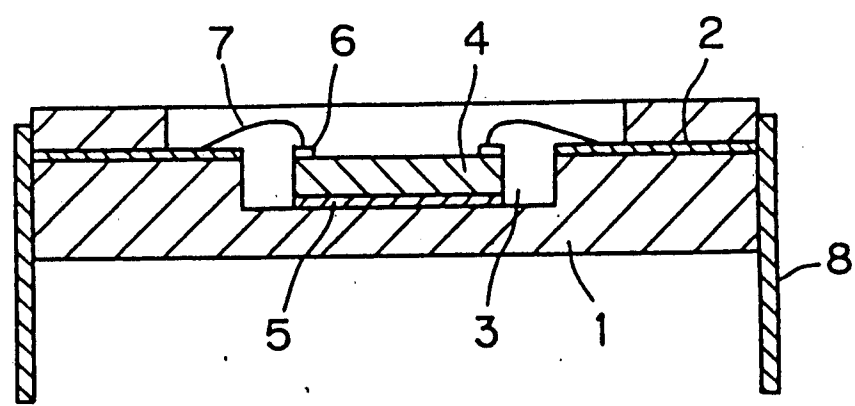


FIG. 9

Fig.10

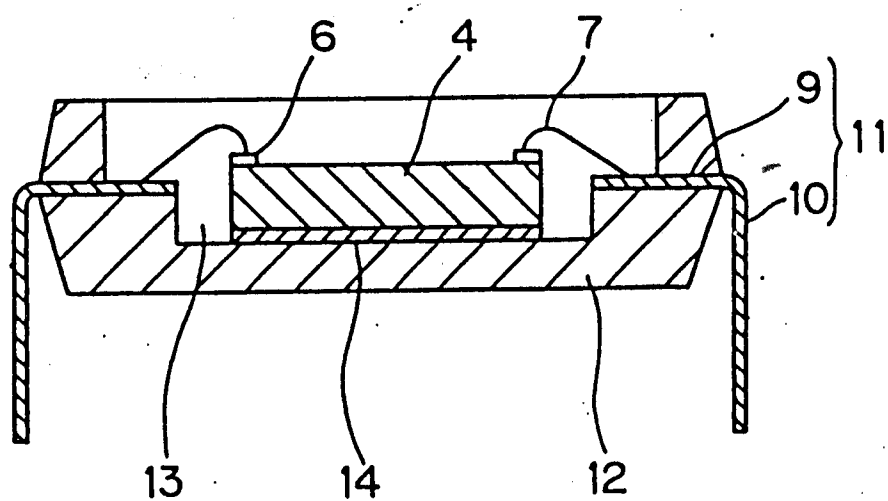


FIG. 10

08/809845-001697

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1995

Application Serial Number

425

CLAIMS AS FILED - PART I

| (Column 1) | | (Column 2) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|--------------|--------------|--------------|---------|----|-------------------------|----------|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE | FEE | | RATE | FEE |
| BASIC FEE | | | | \$85.00 | OR | | \$770.00 |
| TOTAL CLAIMS | | | x\$11= | | OR | x\$22= | |
| INDEPENDENT CLAIMS | | | x\$40= | | OR | x\$80= | \$480 |
| MULTIPLE DEPENDENT CLAIM PRESENT | | | +1\$30= | | OR | +260= | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | OR | TOTAL | \$1340 |

CLAIMS AS AMENDED - PART I

| (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|--|----------------------------------|------------------------------------|---------------|--------------|----------------|-------|-------------------------|----------------|
| AMENDMENT A | CLAIMS REMAINING AFTER AMENDMENT | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
| Total | 16 | Minus | 20 | x\$11= | | OR | x\$22= | |
| Independent | 9 | Minus | | x\$40= | | OR | x\$80= | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | +1\$30= | | OR | +260= | |
| | | | TOTAL | | OR | TOTAL | | |

| (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|--|----------------------------------|------------------------------------|---------------|--------------|----------------|-------|-------------------------|----------------|
| AMENDMENT B | CLAIMS REMAINING AFTER AMENDMENT | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
| Total | | Minus | | x\$11= | | OR | x\$22= | |
| Independent | | Minus | | x\$40= | | OR | x\$80= | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | +1\$30= | | OR | +260= | |
| | | | TOTAL | | OR | TOTAL | | |

| (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|--|----------------------------------|------------------------------------|---------------|--------------|----------------|-------|-------------------------|----------------|
| AMENDMENT C | CLAIMS REMAINING AFTER AMENDMENT | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
| Total | | Minus | | x\$11= | | OR | x\$22= | |
| Independent | | Minus | | x\$40= | | OR | x\$80= | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | +1\$30= | | OR | +260= | |
| | | | TOTAL | | OR | TOTAL | | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" in THIS SPACE is less than 0, enter 0.
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 0, enter 0.
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 3.

8/809845



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: ASSISTANT COMMISSIONER FOR PATENTS
Box PCT
Washington, D.C. 20231

| | | |
|----------------------|-----------------------|------------------|
| U.S. APPLICATION NO. | FIRST NAMED APPLICANT | ATTY. DOCKET NO. |
| 08/809,845 | SANO | Y 43890/225 #2 |

EDWARD E. KUBASIEWICZ
MCDERMOTT, WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006

5611

INTERNATIONAL APPLICATION NO.

PCT/JP96/02142

I.A. FILING DATE

PRIORITY DATE

07/30/96

08/02/95

DATE MAILED:

05/19/97

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

1. The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as

- ☒ a Designated Office (37 CFR 1.494),
☐ an Elected Office (37 CFR 1.495):

☒ U.S. Basic National Fee.

☒ Copy of the international application in:

- ☒ a non-English language.
☐ English.

☒ Translation of the international application into English.

☐ Oath or Declaration of inventor(s) for DO/EO/US.

☐ Copy of Article 19 amendments.

☐ Translation of Article 19 amendments into English.

☐ The International Preliminary Examination Report in English and its Annexes, if any.

☐ Translation of Annexes to the International Preliminary Examination Report into English.

☐ Preliminary amendment(s) filed _____ and _____.

☐ Information Disclosure Statement(s) filed _____ and _____.

☐ Assignment document.

☐ Power of Attorney and/or Change of Address.

☐ Substitute specification filed _____.

☒ Verified Statement Claiming Small Entity Status.

☒ Priority Document.

☒ Copy of the International Search Report ☒ and copies of the references cited therein.

☐ Other:

2. The following items MUST be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- ☐ a. Translation of the application into English. Note a processing fee will be required if submitted later than the appropriate 20 or 30 months from the priority date.

☐ The current translation is defective for the reasons indicated on the attached Notice of Defective Translation.

- ☐ b. Processing fee for providing the translation of the application and/or the Annexes later than the appropriate 20 or 30 months from the priority date (37 CFR 1.492(f)).

- ☒ c. Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date.

☐ The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) for the reasons indicated on the attached PCT/DO/EO/917.

- ☒ d. Surcharge for providing the oath or declaration later than the appropriate 20 or 30 months from the priority date (37 CFR 1.492(e)).

3. Additional claim fees of \$ 282 as a ☒ large entity ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due. See attached PTO-875.

ALL OF THE ITEMS SET FORTH IN 2(a)-2(d) AND 3 ABOVE MUST BE SUBMITTED WITHIN ONE MONTH FROM THE DATE OF THIS NOTICE OR BY ☒ 21 OR ☐ 31 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

4. Translation of the Annexes MUST be submitted no later than the time period set above or the annexes will be cancelled. Note processing fee will be required if submitted later than 30 months from the priority date.

5. ☐ The Article 19 amendments are cancelled since a translation was not provided by the appropriate 20 (37 CFR 1.494(d)) or 30 (37 CFR 1.495(d)) months from the priority date.

Applicant is reminded that any communication to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above. (37 CFR 1.5)

A copy of this notice MUST be returned with this response.

Enclosed: ☐ PCT/DO/EO/917

☐ Notice of Defective Translation

☒ PTO-875

FORM PCT/DO/EO/905 (September 1996)

Paralegal Specialist
Telephone: (703) 305-3656

Paulette Kidwell

P. Kidwell

Rec'd PCT/PTO 16 JUN 1997

ATTORNEY DOCKET NO. 43890/225
PATENT APPLICATION



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of:

Yoshikazu SANO et al.

Based on PCT/JP96/022142

Filed: July 30, 1996

Serial No.: 08/809,845

Filed: April 1, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF

Attention:

PCT Division

Priority Date:
August 2, 1995

**RESPONSE TO NOTICE TO FILE
MISSING REQUIREMENTS UNDER 35 U.S.C. 371**

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In response to the NOTICE TO FILE REQUIREMENTS UNDER 35
U.S.C. 371 dated May 19, 1997 (copy attached), enclosed are:

1. Combined Declaration/Power of Attorney executed by the
inventors: Yoshikazu SANO, Sumio TERAOKAWA, Eiichi TSUJII, Masaii
ASAUMI, and Yoshikazu CHATANI.

2. Recordation Form Cover Sheet submitting an Assignment
executed by the inventors: Yoshikazu SANO, Sumio TERAOKAWA, Eiichi
TSUJII, Masaii ASAUMI, and Yoshikazu CHATANI, along with an
Assignment Recordal Fee of \$40.00.

3. Payment of the Surcharge set forth in 37 C.F.R.
§ 1.16(e) in the amount of \$130.00.

With respect to paragraph No. 3 of the Notice, in a conversation with Paulette Kidwell, paralegal specialist, of the PCT division of the U.S. Patent and Trademark Office, she indicated that the surcharge outlined in this paragraph should be disregarded. Therefore, no surcharge fee is submitted.

Please charge Deposit Account No. 13-0203 in the amount of \$170.00 to cover the above-mentioned fees. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this Response is enclosed for accounting purposes.

Applicants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: June 16, 1997

By: 

Edward E. Kubasiewicz
Registration No. 30,020

1850 K Street, N.W., Suite 450
Washington, D.C. 20006-2296
Telephone: 202-778-8300
Facsimile: 202-778-8335
143890\225\MISPARTS.RES

269190" 54860880

8/809845



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: ASSISTANT COMMISSIONER FOR PATENTS
Box PCT
Washington, D.C. 20231

29 Feb 1997

| | | |
|-------------------------------|-----------------------|-----------------------|
| U.S. APPLICATION NO. | FIRST NAMED APPLICANT | ATTY. DOCKET NO. |
| 08/809,845 | SANO | 16 JUN 1997 43890/225 |
| INTERNATIONAL APPLICATION NO. | | |

EDWARD E. KUBASIEWICZ
MCDERMOTT, WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006

5611

PCT/JP96/02142

| | |
|------------------|---------------|
| I.A. FILING DATE | PRIORITY DATE |
|------------------|---------------|

07/30/96

08/02/95

DATE MAILED

05/19/97

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

1. The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as

- ☒ a Designated Office (37 CFR 1.494),
☐ an Elected Office (37 CFR 1.495);

☒ U.S. Basic National Fee.

☒ Copy of the international application in:

- ☒ a non-English language.
☐ English.

☒ Translation of the international application into English.

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☐ The International Preliminary Examination Report in English and its Annexes, if any.

☐ Translation of Annexes to the International Preliminary Examination Report into English.

☐ Preliminary amendment(s) filed _____ and _____.

☐ Information Disclosure Statement(s) filed _____ and _____.

☐ Assignment document.

☐ Power of Attorney and/or Change of Address.

☐ Substitute specification filed _____.

☒ Verified Statement Claiming Small Entity Status.

☒ Priority Document.

☒ Copy of the International Search Report ☒ and copies of the references cited therein.

☐ Other:

2. The following items MUST be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- ☐ a. Translation of the application into English. Note a processing fee will be required if submitted later than the appropriate 20 or 30 months from the priority date.

☐ The current translation is defective for the reasons indicated on the attached Notice of Defective Translation.

- ☐ b. Processing fee for providing the translation of the application and/or the Annexes later than the appropriate 20 or 30 months from the priority date (37 CFR 1.492(f)).

- ☒ c. Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date.

☐ The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) for the reasons indicated on the attached PCT/DO/EO/917.

- ☒ d. Surcharge for providing the oath or declaration later than the appropriate 20 or 30 months from the priority date (37 CFR 1.492(e)).

3. Additional claim fees of \$ 282 as a ☒ large entity ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due. See attached PTO-875.

ALL OF THE ITEMS SET FORTH IN 2(a)-2(d) AND 3 ABOVE MUST BE SUBMITTED WITHIN ONE MONTH FROM THE DATE OF THIS NOTICE OR BY ☒ 21 OR ☐ 31 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

4. Translation of the Annexes MUST be submitted no later than the time period set above or the annexes will be cancelled. Note processing fee will be required if submitted later than 30 months from the priority date.

5. ☐ The Article 19 amendments are cancelled since a translation was not provided by the appropriate 20 (37 CFR 1.494(d)) or 30 (37 CFR 1.495(d)) months from the priority date.

Applicant is reminded that any communication to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above. (37 CFR 1.5)

A copy of this notice MUST be returned with this response.

Enclosed: ☐ PCT/DO/EO/917

☐ Notice of Defective Translation

☒ PTO-875

FORM PCT/DO/EO/905 (September 1996)

Telephone: (703) 305-2000

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MAY 20 1997

MCDERMOTT, WILL & EMERY

Maulette Kidwell
Paralegal Specialist

1.2
#5
ATTORNEY DOCKET NO. 43890/225
PATENT APPLICATION 2-10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Y. SANO et al.

Serial No.: 08/809,845 DEC 15 1997

Filed: April 1, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF

Group Art Unit: 2503 2602

Examiner: Unassigned

RECEIVED

DEC 19 1997

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

GROUP 2500

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

To further comply with the duty of disclosure under 37 C.F.R. §§ 1.56 and 1.98, Applicants wish to bring to the attention of the U.S. Patent and Trademark Office ("Patent Office") abstracts for each of the references submitted to the Patent Office of April 1, 1997 and listed on the enclosed Form PTO-1449. Copies of the listed abstracts are enclosed.

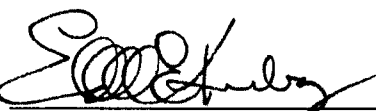
The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: December 15, 1997

By:



Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

ATTORNEY DOCKET NO. 43890/225
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Y. SANO et al.

Serial No.: 08/809,845

Filed: April 1, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF

)
)
) Group Art Unit: 2602

)
) Examiner: Unassigned
)
)

RECEIVED

DEC 19 1997

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

To further comply with the duty of disclosure under 37 C.F.R. §§ 1.56 and 1.98, Applicants wish to bring to the attention of the U.S. Patent and Trademark Office ("Patent Office") abstracts for each of the references submitted to the Patent Office of April 1, 1997 and listed on the enclosed Form PTO-1449. Copies of the listed abstracts are enclosed.

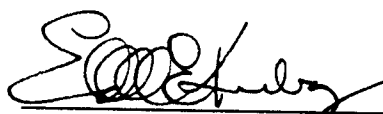
The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: December 15, 1997

By:



Edward E. Kubasiewicz
Registration No. 30,020

600 13th Street, N.W.
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

03/26/98 15:50 202 756 8087

MCDERMOTT

001

DATE & TIME REC'D
IN OFFICE SERVICES

McDermott, Will & Emery
600 13th Street, N.W.
Washington, D.C. 20005-3096

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OUR FACSIMILE NUMBER IS: 202-756-8087
OUR CONFIRMATION NUMBER IS: 202-756-8090

GROUP 2500

DATE: 3/26/98 NO. OF PAGES (INCLUDING COVER SHEET): 5

TO: Ms. Kathy Kirik, OIPE -

COMPANY: U.S. Patent Office CLIENT NUMBER: 43889/534

FACSIMILE NUMBER: 703-308-3840

SENDING PARTY: Dexter Forbes DIRECT PHONE: 202-756-8383

TIMEKEEPER ID: 3343

CONFIRMATION REQUIRED: YES NO XX

IF YES, CONFIRMATION TELEPHONE NUMBER:

COMMENTS: Serial No.: 08/809,845

PLEASE NOTE:

This facsimile originates from the Washington office of McDermott, Will & Emery. If there are any problems regarding the reception of the number of pages listed above, please call our facsimile center at the following number: 202-778-8330 (M-F 8:00 a.m. to 8:00 p.m.), or the sending party at the above listed number.

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TIME CONFIRMED: BY:

AFTER SENDING RETURN THIS FAX TO: D. Forbes

03/26/98 15:51 P 202 756 8087

MCDERMOTT

002

Applicant: SANO, et al. Docket No. 43890-225

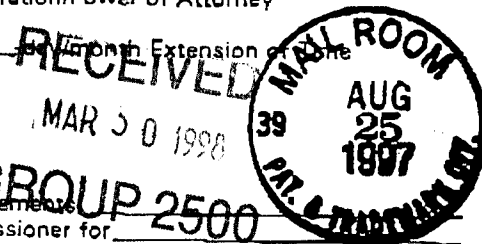
Title/Mark: Solid-State Image... Serial/Reg./Patent No. 08/809,845

Date Sent: 8-25-97 ☐ Hand Carried ☐ 1st-Class Mail ☐ Cert. of Mailing ☐ Express Mail No. _____

- ☐ Transmittal Letter
☐ Utility/Design/Continuation/CIP/FWC/Divisional/PCT
☐ Other: _____
- _____ pages of Specification
_____ pages of Claims
_____ pages of Abstract
_____ pages of Formal/Informal Drawings
- ☐ Information Disclosure Statement
_____ Form PTO 1449
_____ copies of cited references
- ☐ Preliminary Amendment
☐ Response to Missing Parts Notice
☐ Certified Copy of Priority Doc.
☐ Claim for Convention Priority
☐ Verified Statement of Small Entity Status
☐ Transmittal of Issue Fee: Form PTO 85b _____ Form PTO 85C _____
☐ Maintenance Fee for _____ years after grant
☐ Notice of Appeal ☐ Appeal Brief
☐ Recordation of _____ Patent _____ Trademark: Assignments/Security Agreements
☐ Response/Amendment to Office Action of _____ ☐ Petition to Commissioner for _____
- ☐ Trademark/Service Mark/Intent-To-Use Application
☐ Amendment to Allege Use ☐ Statement of Use
☐ Formal/Informal/Substitute Drawing Sheet
_____ (no. of) Substitute/Specimens
☐ Continued Use Affidavit/Declaration (Section 8 & 15)
☐ Notice of Opposition/Answer to _____
☐ Ex Parte Appeal
☐ Petition for Cancellation/ Answer to _____
☐ Renewal of Reg. No. _____
☐ Combined Declaration/Power of Attorney
☐ Letter of Protest
☐ Request for _____

Other: Second Request for Corrected Filing Receipt
or
Check for \$ 0 ☐ Total Deposit Account charge for \$ _____ Attorney: EEK/daf/jm
☐ CHI ☒ WASH

CLO2 Descrip.: _____
THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.



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MCDERMOTT

003

ATTORNEY DOCKET NO. 43890/225
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|--------------------------------|---|---------------------|
| In re Application of: |) | |
| |) | |
| Yoshikazu SANO et al. |) | |
| |) | Attention: |
| |) | APPLICATIONS BRANCH |
| Based on PCT/JP96/022142 |) | |
| Filed: July 30, 1996 |) | |
| |) | |
| Serial No.: 08/809,845 |) | |
| |) | |
| Filed: April 1, 1997 |) | |
| |) | |
| For: SOLID-STATE IMAGE SENSING |) | |
| APPARATUS AND MANUFACTURING |) | |
| METHOD THEREOF |) | |

SECOND REQUEST FOR CORRECTED FILING RECEIPT

Honorable Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

This is a second Request to correct the Official Filing Receipt in the above-identified application. Applicants filed a similar Request on August 19, 1997 requesting that the Official Filing Receipt be corrected to reflect the correct name of fourth inventor listed on the Official Filing Receipt.

Applicants, subsequently, received a "corrected" filing receipt; however, the requested correction was not effectuated. Therefore, Applicants again request that the Official Filing Receipt be corrected to reflect the correct name of the fourth inventor, as is shown on the attached photocopy of the "corrected" filing receipt on which the errors have been noted in red.

- [X] PTO ERROR - Because the error was made by the Patent and Trademark Office, it is believed that no fee is due.
- [] APPLICANT'S ERROR - In accordance with the provisions of 37 C.F.R. 1.19(h), our Check No. _____ in the amount of Twenty Five Dollars (\$___) is attached.

Please grant any extension of time deemed necessary. Please charge any deficient fees, or credit any overpayment of fees, to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: August 25, 1997

By: 

Edward E. Kubasiewicz
Registration No. 30,020

1850 K Street, N.W., Suite 450
Washington, D.C. 20006-2296
Telephone: 202-778-8300
Facsimile: 202-778-8335
\\43890\\225\\OFRCORR2.DOC

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MCDERMOTT

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JUG 2 2 1997

PTO-103X
(Rev. 8-95)

MCDERMOTT, WILL & EMERY

FILING RECEIPT
CORRECTED



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NUMBER | FILING DATE | GRP ART UNIT | FIL FEE REC'D | ATTORNEY DOCKET NO. | DRAWGS | TOT CL | IND CL |
|--------------------|-------------|--------------|---------------|---------------------|--------|--------|--------|
| 08/809,845 | 06/16/97 | 2602 | \$1,520.00 | 43890/225 | 6 | 16 | 9 |

KENNETH L CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006-2296

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

YOSHIKAZU SANO, OSAKA, JAPAN; SUMIO TERAKAWA, OSAKA, JAPAN; EIICHI TSUJII, KYOTO, JAPAN; ~~MASAJI~~ ASAUMI, KYOTO, JAPAN; YOSHIKAZU CHATANI, KYOTO, JAPAN. **MASAJI**

CONTINUING DATA AS CLAIMED BY APPLICANT-

THIS APPLN IS A 371 OF PCT/JP96/02142 07/30/96 **MASAJI**

FOREIGN/PCT APPLICATIONS-JAPAN

7-197365

08/02/95

TITLE

SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

PRELIMINARY CLASS: 348



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|-----------------|-------------|----------------------|---------------------|
|-----------------|-------------|----------------------|---------------------|

08/809,845 06/16/97 SAND Y 43890/225

EXAMINER

MM11/0720

KENNETH L CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006-2296

| NGO, N | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |

2814
DATE MAILED: 07/20/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

08/849845

Applicant(s)

Sam J. Hall

Examiner

Ngan Ngo

Group Art Unit

2814

---The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address---

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☒ Responsive to communication(s) filed on 3-26-98
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1 to 16 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1 to 16 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
 - ☐ received in Application No. (Series Code/Serial Number) _____.
 - ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5
- ☐ Interview Summary, PTO-413
- ☒ Notice of References Cited, PTO-892
- ☐ Notice of Informal Patent Application, PTO-152
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Other _____

Office Action Summary

Serial Number: 08/809,845

Page 2

Art Unit: 2814

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Figures 9 and 10 must be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al(JP-07-45803, cited by Applicants).

Takashi discloses in figures 1 and 2 a solid state image sensing apparatus comprising a package(4) having through hole and different opening areas, a lead frame(5), and a chip(6). It would have been obvious to one of ordinary skill in the art to form the sensing elements and the peripheral circuit elements on the same chip to provide a compact device.

Claims 7-12, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al as applied to claims 1-6, 13, and 15 above, and further in view of Nicewarner, Jr.

Nicewarner discloses in figures 1 and 2 a through-hole package having a stack of circuit chips of different circuit elements formed in the same package. It would have been obvious to one

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Page 3

Art Unit: 2814

of ordinary skill in the art to use the teachings of Takashi and Nicewarner to form different circuit elements such as sensing elements and peripheral circuits in the same package.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (703) 308-4938. The fax phone number for the Art unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



NGAN V. NGO
PRIMARY EXAMINER
GROUP 2500

Ngan Ngo

July 15, 1998

809845

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) 4/1/97 are

A. ☐ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:

Black ink. Color.

☐ Not black solid lines. Fig(s) _____☐ Color drawings are not acceptable until petition is granted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84(b)

☐ Photographs are not acceptable until petition is granted. Fig(s) _____☐ Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____☐ Poor quality (half-tone). Fig(s) _____

3. GRAPHIC FORMS. 37 CFR 1.84(d)

☐ Chemical or mathematical formula not labeled as separate figure. Fig(s) _____☐ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis. Fig(s) _____☐ Individual waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s) _____

4. TYPE OF PAPER. 37 CFR 1.84(e)

☐ Paper not flexible, strong, white, smooth, nonshiny, and durable. Sheet(s) _____☒ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds copy machine marks not accepted. Fig(s) 1-10☐ Mylar, vellum paper is not acceptable (too thin). Fig(s) _____

5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:

21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)

21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)

21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)

21.0 cm. by 29.7 cm. (DIN size A4)

☐ All drawing sheets not the same size. Sheet(s) _____☐ Drawing sheet not an acceptable size. Sheet(s) _____

6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size

| | | | |
|---|---|---|-----------------------------------|
| 21.6 cm. X 35.6 cm. (8 1/2 X 14 inches) | 21.6 cm. X 33.1 cm. (8 1/2 X 13 inches) | 21.6 cm. X 27.9 cm. (8 1/2 X 11 inches) | 21.0 cm. X 29.7 cm. (DIN Size A4) |
| 1.5 cm. (1/2") | 2.5 cm. (1") | 2.5 cm. (1") | 2.5 cm. |
| L .64 cm. (1/4") | .64 cm. (1/4") | .64 cm. (1/4") | 2.5 cm. |
| R .64 cm. (1/4") | .64 cm. (1/4") | .64 cm. (1/4") | 1.5 cm. |
| B .64 cm. (1/4") | .64 cm. (1/4") | .64 cm. (1/4") | 1.0 cm. |

Margins do not conform to chart above.

Sheet(s) _____

☐ Top (T) ☐ Left (L) ☐ Right (R) ☐ Bottom (B)

7. VIEWS. 37 CFR 1.84(h)

REMARK: Specification may require revision to correspond to drawing changes.

☐ All views not grouped together. Fig(s) _____☐ Views connected by projection lines or lead lines. Fig(s) _____

Partial views. 37 CFR 1.84(b) 2

☐ View and enlarged view not labeled separately or properly. Fig(s) _____

Sectional views. 37 CFR 1.84 (h) 3

☐ Hatching not indicated for sectional portions of an object. Fig(s) _____☐ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____☐ Indication such as "actual size" or scale 1/2" not permitted. Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)

☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings). Fig(s) 1-10

11. SHADING. 37 CFR 1.84(m)

☐ Solid black shading areas not permitted. Fig(s) _____☐ Shade lines, pale, rough and blurred. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)

☐ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(1) Fig(s) _____☐ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____☐ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____☐ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3) Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(r)

☐ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Sheet(s) _____

15. NUMBER OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____☐ View numbers not preceded by the abbreviation Fig. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from prior PTO-948. Fig(s) _____

17. DESIGN DRAWING. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____☐ Solid black shading not used for color contrast. Fig(s) _____

COMMENTS:

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ATTORNEY DOCKET NO. 43890-225
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

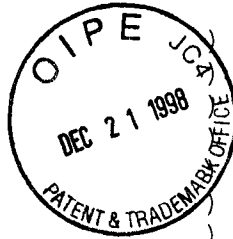
In re Application of:

Yoshikazu SANO et al.

Serial No.: 08/809,845

Filed: June 16, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF



Group Art Unit: 2814

Examiner: N. NGO

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AMENDMENT UNDER 37 C.F.R. § 1.115

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 20, 1998, having a shortened statutory period for response set to expire on October 20, 1998, a two month extension of time up to and including December 20, 1998 being filed concurrently herewith, please amend the above-identified application as follows:

IN THE DRAWINGS:

Please amend Figs. 9 and 10 to include the legend "Prior Art" as shown on the marked up copies thereof, which are enclosed herewith.

IN THE CLAIMS:

Please cancel claim 2, add new claim 17 and amend claim 1 and 3-16 as follows:

1. (Amended) A solid-state image sensing apparatus

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comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole], and

[(c)] a solid-state image sensing device [element (CCD chip)] mounted in said package by being inserted from an inlet of said opening which has a wider area, and thereby sealing said through hole, said solid-state image sensing device being secured to said package via an adhesive.

3. (Amended) The solid-state image sensing apparatus of Claim [2] ²/~~17~~, wherein each of the electrode pads [pad of the CCD chip] is connected [via the bump] to the inner lead via a bump.

4. (Amended) The solid-state image sensing apparatus of Claim [2] ²/~~17~~, wherein each of the electrode pads [pad of the CCD chip] is connected to the inner lead via an anisotropic conductor having only vertical conductivity.

5. (Amended) The solid-state image sensing apparatus of Claim [2] ²/~~17~~, wherein a tip of the inner lead to which the electrode pad [of the CCD chip] is connected [is protruded from around the opening] extends beyond said ledge.

6. (Amended) A solid-state image sensing apparatus comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole],

Alt [(c)] a substrate on which a [CCD chip] solid-state image sensing device and a peripheral circuit [element] chip are mounted being inserted into the package from a wider opening thereof, and

[(d)] an electrode pad of said substrate being connected to said inner lead exposed from around a smaller opening of said package,

said substrate being secured to said package via an adhesive.

7. (Amended) A solid-state image sensing apparatus comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole],

[(c)] a semiconductor substrate [on which, except a]

having a solid-state image sensing device [place a CCD chip is formed,] and a peripheral circuit chip [element is] disposed on an upper surface thereof, said semiconductor substrate being inserted into a plastic package[,] via the larger of two [which has a plurality of] openings [having different opening areas, from a wider opening of] formed in said package, and

[(d)] an electrode pad of said semiconductor substrate being connected to the inner lead exposed from around [a] the smaller opening of said package,

said semiconductor substrate being secured to said package via an adhesive.

8. (Amended) The solid state image sensing apparatus of Claim 6 or Claim 7, wherein a shading film covers an entire upper surface of said substrate except an upper surface of the [CCD chip] solid-state image sensing device.

9. (Amended) The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad [of] formed on the substrate is connected to the inner lead via a bump.

10. (Amended) The solid-state image sensing apparatus of Claim 6 or Claim 7, wherein an electrode pad [of] formed on the substrate is connected to the inner lead via an anisotropic conductor which has only vertical conductivity.

11. (Amended) The solid-state image sensing apparatus of

Claim 6 or Claim 7, wherein an electrode pad [of] formed on the substrate is connected to the inner lead at an outer portion of said lead, said outer portion of said lead extending into the openings [of which tip is protruded from around the opening] of the package.

12. (Amended) A solid-state image sensing apparatus comprising:

[(a)] a package having a through hole therein, openings on both end faces thereof, and different opening areas of said openings,

[(b)] a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package [which has a through hole], and

[(c)] a solid-state image sensing [element (CCD chip)] device and a peripheral circuit chip [element] both mounted in said package, said [CCD chip] solid-state image sensing device being connected to a first inner lead exposed [from] beneath a first step surface [situated to] formed in said package, said solid-state image sensing device being secured to said package via an adhesive, and said peripheral circuit [element] chip being connected to a second inner lead exposed [from] beneath a second step surface [situated to] formed in said package, said peripheral circuit chip being secured to said package via an adhesive.

13. (Amended) A manufacturing method of a solid-state image

sensing apparatus comprising a package having a through hole therein, a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device mounted in said package, said manufacturing method comprising the steps of:

[(a)] [insert] inserting said [CCD chip] solid-state image sensing device into said through hole [from a wider opening area of the package],

[(b)] [connect] connecting an electrode pad of the [CCD chip] solid-state image sensing device inserted in the through hole to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning of said solid-state image sensing device [as well as electrical connection], and

[(c)] [fix a back side of the] securing said solid-state image sensing device [CCD chip] to the package with [glue] an adhesive.

14. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising the steps of:

[(a) form] forming said [CCD chip] solid-state image

sensing device and a group of wirings on a semiconductor substrate,

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^
((b) mount] mounting said peripheral circuit [element] chip on [a surface except the preoccupied place by the ~~/~~CCD chip] solid-state image sensing device to connect with said group of wiring^{on} said semiconductor surface,

OC 3/15/99
((c) insert] inserting said semiconductor substrate into the through hole [from a wider opening of the package],

OC 3/15/99
((d) connect] connecting an electrode pad disposed on [around] the semiconductor substrate to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning of said solid-state image sensing device [and electrical connection], and

OC 3/15/99
((e)] [fix a back side of] securing the semiconductor substrate on which the [CCD chip] solid-state image sensing device and the peripheral circuit [element] chip are mounted to the package [with glue] via an adhesive.

15. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in said package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising steps of:

OC 3/15/99
((a) mount] mounting said [CCD chip] solid-state image

sensing device and said peripheral circuit [element] chip on a substrate where a group of wirings is disposed in order to connect the [CCD chip] solid-state image sensing device and the peripheral circuit chip to the group of wirings,

[(b) insert] inserting the semiconductor substrate into the through hole [from a wider opening of the package],

[(c) connect] connecting an electrode pad disposed on a periphery of the substrate to the inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning [and electrical connection] of the solid-state image sensing device, and

[(d) fix a back side of] securing the semiconductor substrate [where] on which said [CCD chip] solid-state image sensing device and said peripheral circuit [element] chip are mounted to the package [with glue] via an adhesive.

16. (Amended) A manufacturing method of a solid-state image sensing apparatus comprising a package having a through hole therein, a lead frame comprising [the] inner leads and outer leads, said lead frame being sealed in the package, and a solid-state image sensing [element (CCD chip)] device as well as a peripheral circuit [element] chip mounted in said package, said manufacturing method comprising steps of:

[(a) insert] inserting said [CCD chip] solid-state image sensing device into the through hole [from a wider opening of the package],

[(b) connect] connecting an electrode pad of the [CCD chip] solid-state image sensing device to a first inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, [to complete an] while simultaneously adjusting the optical positioning [and electrical connection] of the solid-state image sensing device, said first inner lead being disposed beneath a first step surface formed in said package,

[(c) fix a back side of] securing the [CCD chip] solid-state image sensing device to the package [with glue] via an adhesive,

[(d) insert] inserting the peripheral circuit [element] chip into the through hole [from the wider opening of the package],

[(e) connect] connecting an electrode pad of the peripheral circuit [element] chip to a second inner lead via a bump or an anisotropic conductor[, which has] having only vertical conductivity, to complete an electrical connection, said second inner lead being disposed beneath a second step surface formed in said package, and

[(f) fix a back side of] securing the peripheral circuit [element] chip to the package [with glue] via an adhesive.

Please add new claim 17 as follows:

~~3-17.~~ A solid-state image apparatus comprising:
a package comprising a main body having a through hole therein, said main body having a top surface and a bottom

surface, said package further comprising a ledge formed on said main body so as to extend inwardly toward the center of said through hole, said ledge comprising an upper surface and a lower surface;

Alone
a lead frame comprising inner leads and outer leads, said lead frame being sealed in said package such that said inner leads extend inwardly from said main body so as to be adjacent said lower surface of said ledge; and

a solid-state image sensing device having an upper surface and a lower surface and a plurality of electrode pads disposed on said upper surface, each of said plurality of electrode pads coupled to one of said inner leads;

said solid-state image sensing device being secured to said main body of said package via an adhesive.--

R E M A R K S

I. Introduction

In response to the Office Action, Applicants have amended Figs. 9 and 10 to include the legend "Prior Art." In addition, claims 1, 3-7 and 9-16 have been amended to clearly distinguish the present invention over the cited art. Claim 2, which is now cancelled, has been rewritten as new claim 17. No new matter has been added. In addition, in an effort to utilize consistent terms throughout the claims, the phrases "solid-state imaging element" and "CCD chip" and been amended to "solid-state imaging

device. Further, the phrase "peripheral circuit element" has been changed to "peripheral circuit chip."

In addition, Applicants wish to verify that the Examiner has received the Supplemental Information Disclosure Statement (IDS) filed on December 15, 1997. An acknowledgement of review of the IDS by initialing and returning the PTO-1449 form is respectfully requested.

II. The Rejection Of Claims 1-6, 13 And 15 Under 35 U.S.C. § 103, As Being Unpatentable Over Takashi et al. Is Overcome By Applicants' Amendments To The Claims

Claims 1-6, 13 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over Takashi et al. (JP 07-45803). For the following reasons Applicants respectfully submit that the rejection is overcome by Applicants' amendments to the claims.

A. The Prior Art Cited By The Examiner Does Not Disclose Or Suggest Applicants' Novel Design As Recited By The Pending Claims

As set forth in the pending claims, the present invention discloses an apparatus which allows for the accurate positioning and mounting of a CCD chip (i.e., solid-state image sensing device). The image sensing apparatus of the present invention comprises a package to which a CCD chip is mounted. The package has leads sealed therein, which are coupled to the CCD chip. The package also has a through hole which allows an optical positioning adjusting device to view the CCD chip during the mounting process so that the CCD chip can be properly positioned.

The CCD chip further comprises electrodes which are coupled to the inner portion of the leads sealed in the package. The electrodes, which are bumps, are pressed into contact with the leads during the mounting process and allow for adjustment of the position of the CCD chip. When the CCD chip is positioned in the desired location, an adhesive is utilized to secure the CCD chip to inner sidewalls of the package, thereby securing the CCD chip in the proper location. It is noted that all of the independent claims have been amended to recite that the CCD chip or the substrate holding the chip are secured to the package via an adhesive.

Moreover, amended claim 5 recites that the inner lead extends beyond the ledge formed in the package. This advantageously makes the lead more flexible, which facilitates the optical positioning of the CCD chip as well as the coupling between the lead and the bump electrode (see, page 10, lines 2-7).

Clearly, Takashi fails to disclose or suggest the present invention as recited by the amended claims. Most importantly, Takashi does not disclose the use of an adhesive for securing the CCD chip to the package. Takashi appears to simply disclose that the CCD chip is coupled to the leads via bumps 7, which can be accomplished, for example, by a reflow solder process. However, by utilizing such a bonding process to couple the CCD chip to the leads, the precise position of the chip cannot be controlled to the accuracy the present invention provides. Thus, it is clear that Takashi fails to disclose the present invention. Moreover,

as Takashi neither discusses nor addresses the need for precise placement of the CCD chip, it is clear that the present invention is not obvious in view of Takashi.

For the same reasons, Applicants respectfully submit that new claim 17 is patentable over Takashi.

III. The Rejection Of Claims 7-12, 14 And 16 Under 35 U.S.C. § 103, As Being Unpatentable Over Takashi et al. In View Of Nicewarner Is Overcome By Applicants' Amendments To The Claims

Claims 7-12, 14 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Takashi et al. (JP 07-45803) in view of Nicewarner (USP No. 5,327,325). For the following reasons Applicants respectfully submit that the rejection is overcome by Applicants' amendments to the claims.

For the reasons set forth above, it is clear that Takashi fails to disclose or suggest the present invention. Nicewarner does not cure the deficiencies of Takashi.

Nicewarner relates to a flip-chip bonding method utilized to position a plurality of chips with a given package. As with Takashi, Nicewarner utilizes a reflow solder process to couple the electrode bumps on the chips to one another and wire bond connections to couple the chips to leads.

More importantly, however, is that contrary to the assertion in the pending rejection, Nicewarner does not provide a through hole. Referring to Figs. 1 and 3 of Nicewarner, Nicewarner discloses a package have a center portion (highlighted in red on the enclosed copy of Fig. 1) that extends across the entire

package. Thus, Nicewarner does not have a through hole.

As such, it is clear that Nicewarner cannot be combined with Takashi to render the present invention obvious. The apparatus of the present invention requires that the CCD chip be mounted through the bottom opening of the package so as to allow the optical positioning adjusting device to view the surface of the CCD chip through the top opening during the mounting process. Clearly, this cannot be done in Nicewarner, because Nicewarner has no through hole. As such, it is respectfully submitted that Nicewarner teaches away from the present invention. For essentially the same reasons, Nicewarner is also incompatible with the device of Takashi.

The Court of Appeals for the Federal Circuit repeatedly has ruled that there must be some teaching or suggestion supporting the combination used in making the rejection. For example, In re Newell, 891 F.2d 899, 901 (Fed. Cir. 1989), the court held "[i]n deciding that a novel combination would have been obvious, there must be supporting teaching in the prior art." In Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), in finding obviousness, the court held "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combination; there must be some teaching suggestion, or incentive to make the combination made by the inventor." Finally, in In re Mills, 916 F.2d 680, 682 (Fed. Cir. 1990), the court held that although a prior art device "may be capable of being modified to run the way [the patent Applicants'] apparatus is claimed, there must be a

suggestion or motivation in the reference to do so" in order to establish obviousness.

Clearly, neither Takashi nor Nicewarner provide the necessary teaching to substantiate an obviousness rejection of the amended claims.

For all of the foregoing reasons, Applicants respectfully submit the present invention as recited by the amended claims is patentable over the combination of Takashi and Nicewarner.

IV. Summary

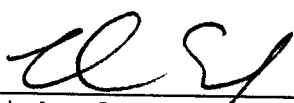
Having fully and completely responded to the Office Action, Applicants respectfully submit that the claims are in condition for allowance, an indication of which is respectfully solicited.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 12/21/98

By:


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087

6/8

Approved
1-7-99
W/m J N/r

Fig.9

PRIOR ART

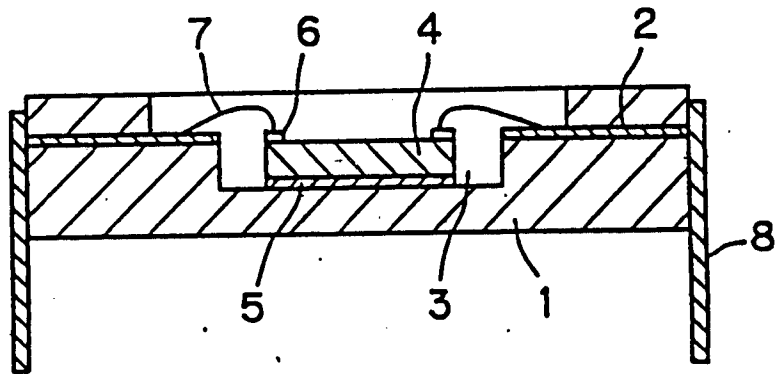
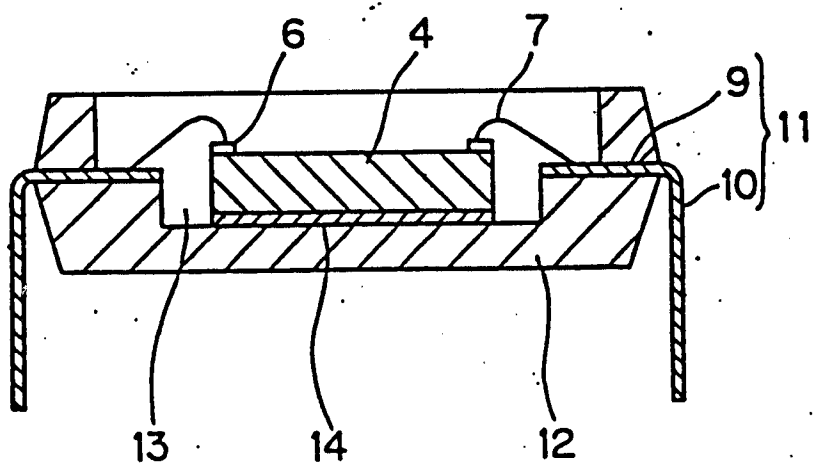


Fig.10

PRIOR ART





PATENT
ATTORNEY DOCKET NO. 43890-225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yoshikazu Sano et al.

Serial No.: 08/809,845

Group Art Unit: 2814

Filed: June 16, 1997

Examiner: N. NGO

For: SOLID-STATE IMAGE SENSING APPARATUS AND
MANUFACTURING METHOD THEREOF

AMENDMENT TRANSMITTAL

Honorable Commissioner of Patents
and Trademarks,
Washington, D.C. 20231

Sir:

1. X Transmitted herewith is an amendment for the above-identified application.

STATUS

2. X Applicant is is small entity - verified statement:
 attached already filed.
X other than a small entity.

EXTENSION OF TIME

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. §1.136 apply.

- (a) X Applicant petitions for an extension of time for the total number of months checked below:

| EXTENSION (months) | FEE FOR SMALL ENTITY | FEE FOR OTHER THAN SMALL ENTITY |
|--------------------------|-------------------------|------------------------------------|
| <u> </u> one month | \$ 55.00 | \$ 110.00 |
| <u>X</u> two months | 190.00 | 380.00 |
| <u> </u> three months | 435.00 | 870.00 |
| <u> </u> four months | 680.00 | 1,360.00 |

Fee \$380.00

If an additional extension of time is required, please consider this a petition therefor.

 An extension for months has already been secured and the fee paid therefor of is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this Request \$

- (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

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TECHNOLOGY CENTER 2800

4. X The fee for claims has been calculated as shown below:

| | Claims Remaining After Amendment | Highest Number Previously Paid For | Present Extra | Rate | Additional Fee |
|--|---|---|------------------|----------------|-------------------|
| Total | : | : | : | : | : |
| Claims | : 16 | : 20 | : 0 | : x \$ 18.00 = | : 0 |
| Independent | : | : | : | : | : |
| Claims | : 9 | : 9 | : 0 | : x \$ 78.00 = | : 0 |
| Multiple Dependent Claims (first presentation) | | | | : \$260.00 = | : 0 |
| Total | | | | = | : 0 |
| Reduction by 1/2 for small entity | | | | : | : - 0 |
| TOTAL FEE | | | | : | : 0 |

- (a) X No additional fee for claims is required.

-OR-

- (b) The total additional fee for claims required \$ _

FEE PAYMENT

5. Attached is a check in the amount of \$ _.

X Charge Deposit Account No. 13-0203 the amount of \$380.00. A duplicate copy of this Transmittal is enclosed for accounting purposes.

FEE DEFICIENCY

X If any additional extension and/or fee is required, this is the request therefor and to charge Deposit Account No. 13-0203.

AND/OR

X If any additional fee for claims is required, charge Deposit Account No. 13-0203. A duplicate copy of this Transmittal is enclosed for accounting purposes.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date:

12/21/98

By:

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
(202) 756-8000



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NUMBER | FILING DATE | FIRST NAMED APPLICANT | ATTORNEY DOCKET NO. |
|--------------------|-------------|-----------------------|---------------------|
|--------------------|-------------|-----------------------|---------------------|

08/809,845 08/16/97 SANDO

Y 43890/225

MM21/0111

KENNETH L. CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006-2296

| EXAMINER |
|----------|
|----------|

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2814

DATE MAILED:

01/11/99

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

- ☒ This communication is responsive to An amendment filed 12-21-98
- ☒ The allowed claim(s) is/are 1 and 3 to 17
- ☐ The drawings filed on _____ are acceptable.
- ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
- ☐ received in Application No. (Series Code/Serial Number) _____
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

- ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- ☒ Applicant MUST submit NEW FORMAL DRAWINGS
- ☐ because the originally filed drawings were declared by applicant to be informal.
- ☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. 7
- ☒ including changes required by the proposed drawing correction filed on 12-21-98, which has been approved by the examiner.
- ☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

- ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

- ☐ Notice of References Cited, PTO-892
- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
- ☐ Notice of Draftperson's Patent Drawing Review, PTO-948
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Interview Summary, PTO-413
- ☐ Examiner's Amendment/Comment
- ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
- ☐ Examiner's Statement of Reasons for Allowance

Ngan Van Ngo
Primary Examiner



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM21/0014

EXAMINER: J. J. J. J.
CLASS: 35/000000
INVENTOR: J. J. J. J.
ATTORNEY: J. J. J. J.
DATE: J. J. J. J.

| APPLICATION NO. | FILING DATE | TOTAL CLAIMS | EXAMINER AND GROUP ART UNIT | DATE MAILED |
|-----------------------|-------------|--------------|-----------------------------|---------------|
| 08/2000, 0000 | 06/16/97 | 016 | NOL, N | 2010 01/11/99 |
| First Named Applicant | YOSHIKAZU | | | |

TITLE OF INVENTION: STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

| ATTY'S DOCKET NO. | CLASS-SUBCLASS | BATCH NO. | APPLN. TYPE | SMALL ENTITY | FEE DUE | DATE DUE |
|-------------------|----------------|-----------|-------------|--------------|-----------|----------|
| 08/2000, 0000 | 25/272.000 | N72 | UTILITY | NO | \$1200.00 | 08/10/99 |

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- Pay FEE DUE shown above, or
- File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM21/0111

APPLICATION NO. 06/004,010
FILING DATE 06/16/97
TOTAL CLAIMS 617
EXAMINER AND GROUP ART UNIT NGO, M
DATE MAILED 2014 01 11 01

| APPLICATION NO. | FILING DATE | TOTAL CLAIMS | EXAMINER AND GROUP ART UNIT | DATE MAILED |
|-----------------------|-----------------------------------|--------------|-----------------------------|---------------|
| 06/004,010 | 06/16/97 | 617 | NGO, M | 2014 01 11 01 |
| First Named Applicant | 35 USC 154(b) term ext. = 0 Days. | | | |

TITLE OF INVENTION: MULTI-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

| ATTY'S DOCKET NO. | CLASS-SUBCLASS | BATCH NO. | APPLN. TYPE | SMALL ENTITY | FEE DUE | DATE DUE |
|-------------------|----------------|-----------|-------------|--------------|-----------|----------|
| 06/004,010 | 237-023,000 | N72 | UTILITY | NO | \$1510.00 | 04/12/14 |

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- Pay FEE DUE shown above, or
- File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

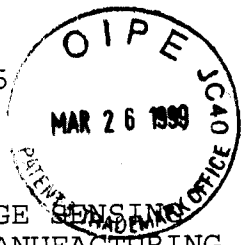
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11 LP

ATTORNEY DOCKET NO. 43890-225
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Yoshikazu SANO et al.)
Serial No.: 08/809,845)
Filed: June 16, 1997)
For: SOLID-STATE IMAGE SENSING)
APPARATUS AND MANUFACTURING)
METHOD THEREOF)



Attn: BOX ISSUE FEE

Notice of Allowance
dated: 1/11/99

BATCH NO.: N72

LETTER SUBMITTING FORMAL DRAWINGS
AFTER NOTICE OF ALLOWANCE

RECEIVED
Publishing Division
MAR 30 1999

Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability mailed January 11, 1999 in which the U.S. Patent and Trademark Office required that formal corrected drawings be filed, it is respectfully requested that the six (6) sheets of formal drawings (Figs. 1-10) be entered in the subject application. These drawings are being submitted concurrently with the payment of the Issue Fee.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any

overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Dated: 3/26/99

By:



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087

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FIG. 1

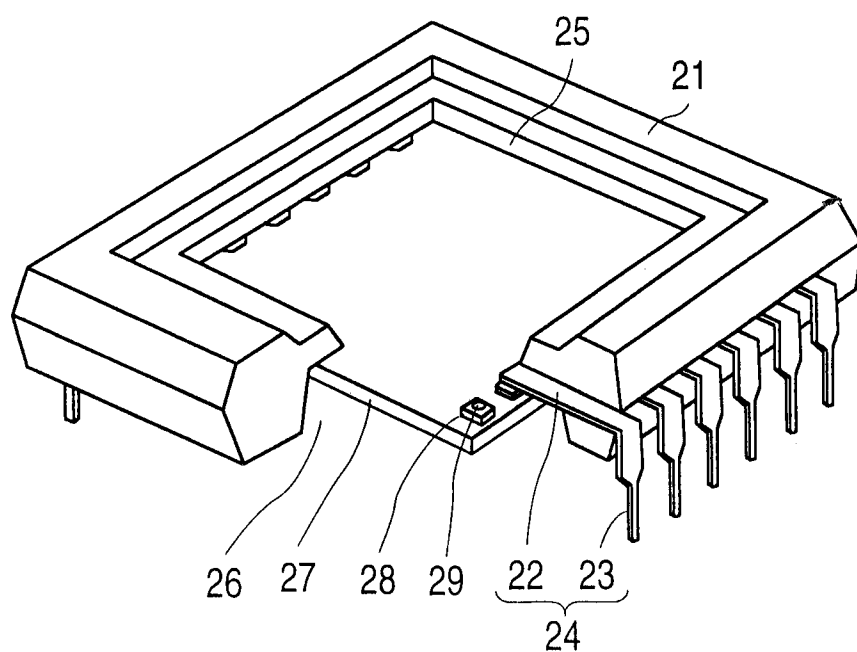


FIG. 2

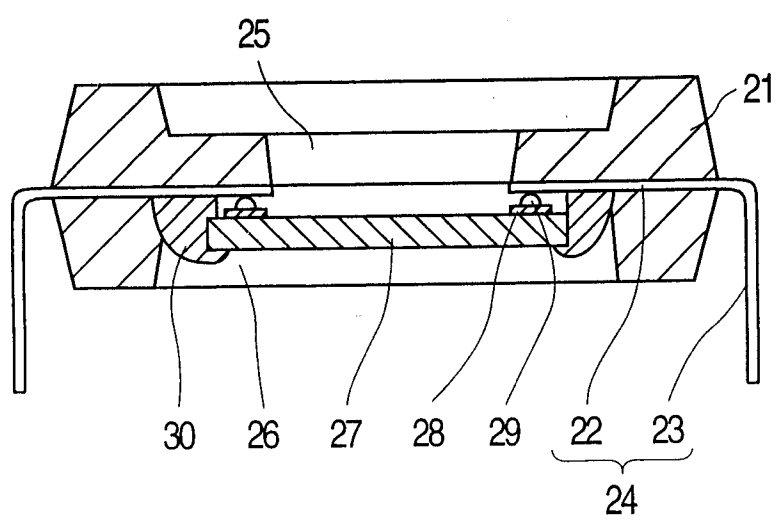


FIG. 3

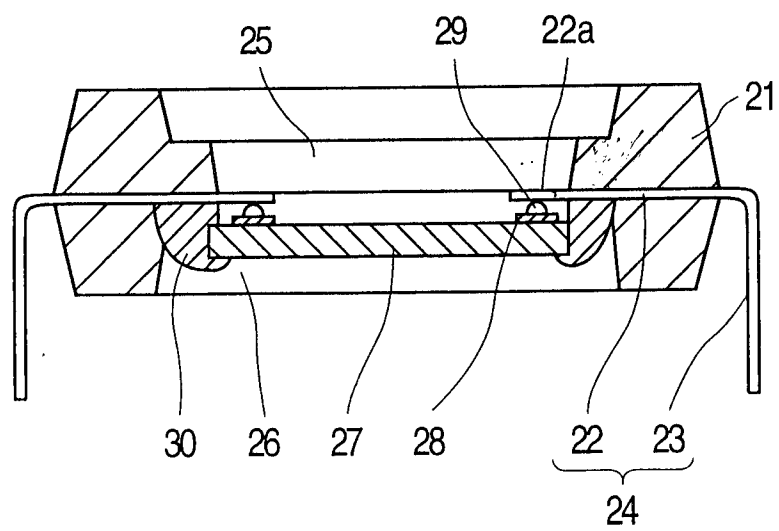


FIG. 4

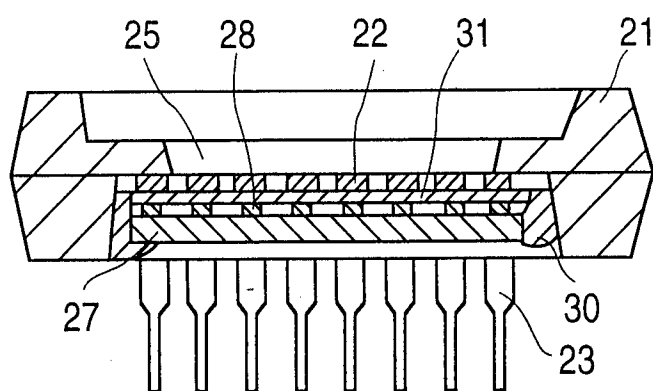


FIG. 5

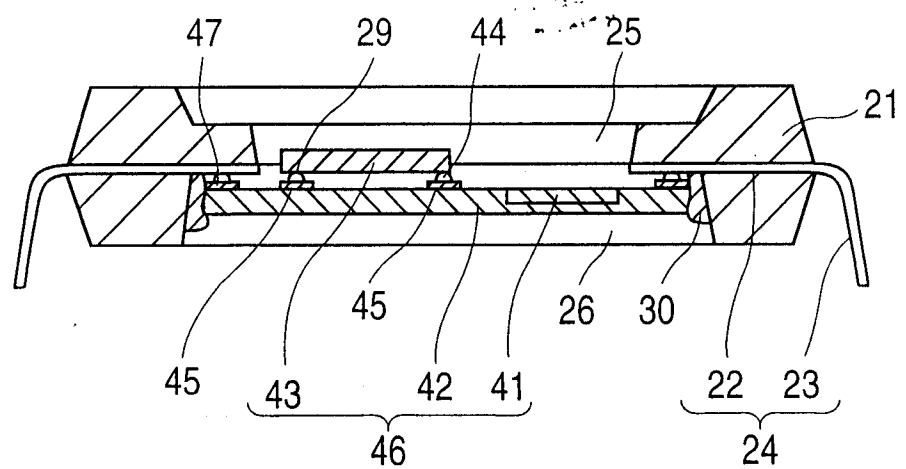


FIG. 6

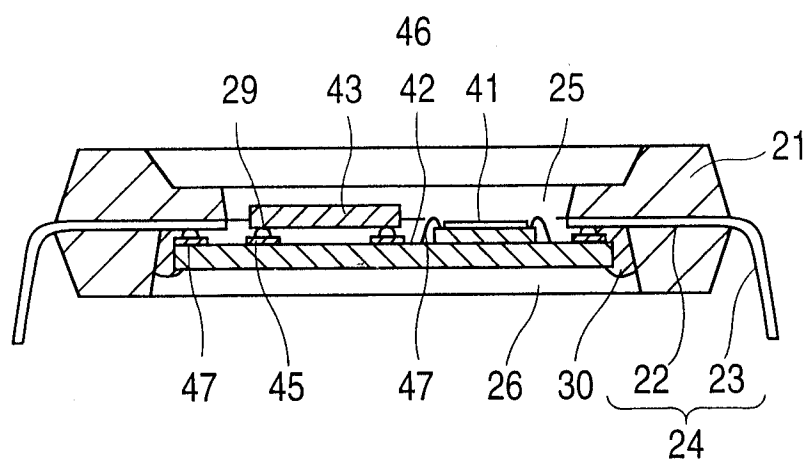


FIG. 7

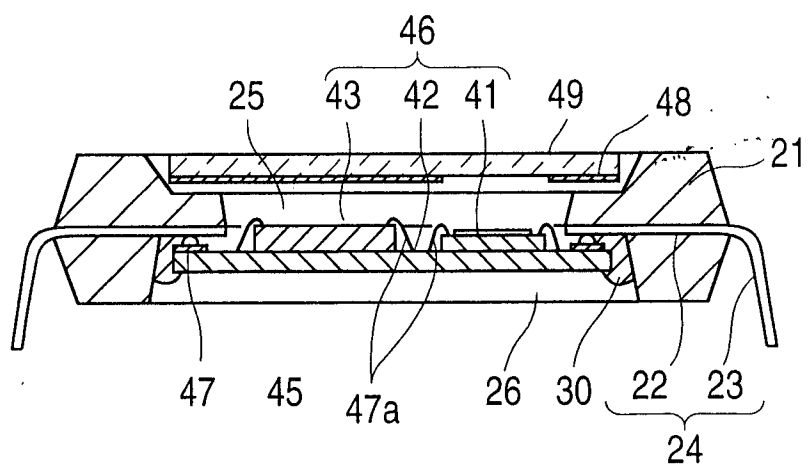


FIG. 8

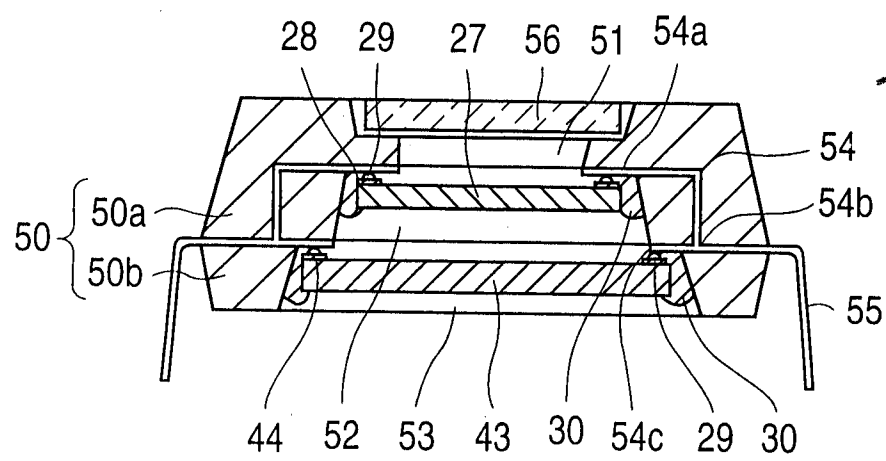


FIG. 9
PRIOR ART

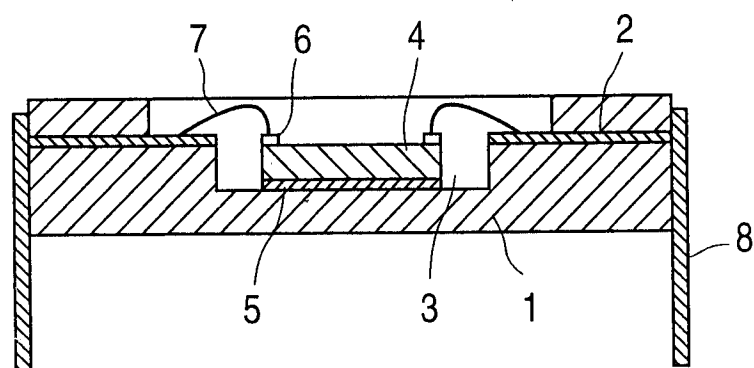
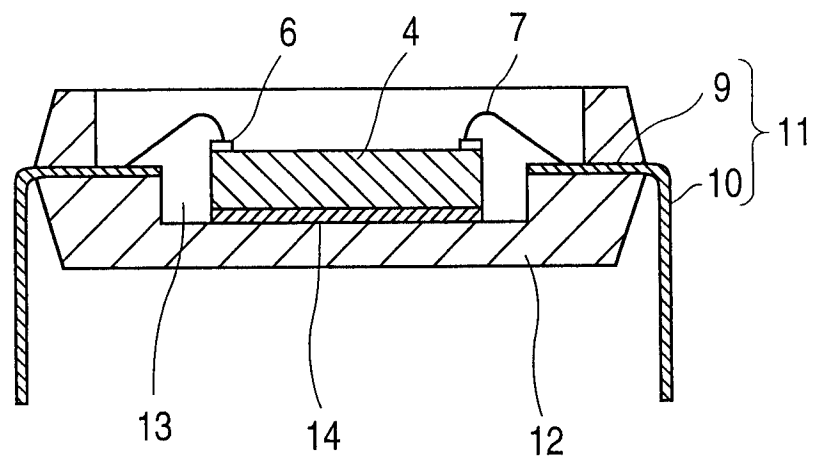


FIG. 10
PRIOR ART



#12 KC
3-26-9
FD

ATTORNEY DOCKET NO. 43890-225
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Yoshikazu SANO et al.

Serial No.: 08/809,845

Filed: June 16, 1997

For: SOLID-STATE IMAGE SENSING
APPARATUS AND MANUFACTURING
METHOD THEREOF



Attn: BOX ISSUE FEE

Notice of Allowance
dated: 1/11/99

BATCH NO.: N72

REQUEST FOR CHANGE OF ADDRESS

Hon. Assistant Commissioner
for Patents
Washington, D.C. 20231

RECEIVED
Publishing Division

MAR 30 1999

Sir:

The undersigned attorney, being of record in the subject application with power of attorney, hereby requests that, for the above-identified application, all future correspondence, facsimiles and telephone calls be addressed to:

McDermott, Will & Emery
600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Dated:

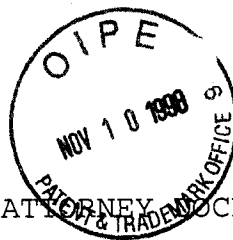
3/26/99

By:

A handwritten signature in cursive script, appearing to read "Michael E. Fogarty".

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087



#13/Religion
Hood
PATENT 5,289,999

ATTORNEY DOCKET NO. 43890-225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re CPA Application of:)
Y. Sano et al.) Group Art Unit: 2814
Serial No.: 08/809,845)
Filed: April 1, 1997) Examiner: N. NGO
For: SOLID-STATE IMAGE SENSING)
APPARATUS AND MANUFACTURING)
METHOD THEREOF)

RECEIVED

NOV 12 1998

GROUP 2000

PETITION REQUESTING CONSIDERATION OF
INFORMATION DISCLOSURE STATEMENT AND
CERTIFICATION UNDER 37 C.F.R. § 1.97(e)(1)
ACCOMPANYING INFORMATION DISCLOSURE STATEMENT

Hon. Assistant Commissioner for Patents
Washington, D.C. 22031

Sir:

Applicants hereby petition for the consideration of the reference cited in the Information Disclosure Statement being filed concurrently herewith. As certified below, the reference came to the attention of the Applicants within the last three months, and before payment of the issue fee.

In accordance with the provisions of 37 C.F.R. § 1.97(e)(1), I hereby certify that, to the best of my knowledge and belief, each item of information contained in the

Information Disclosure Statement being filed concurrently herewith was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of said Statement.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: _____

1/13/98

By: _____

Michael E. Fogarty

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005
Telephone: 202-756-8000
Facsimile: 202-756-8087
43890225\SANOPET.001



ATTORNEY DOCKET NO. 43890-225
PATENT

#14/405
Hood
52899

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re CPA Application of:)
Y. Sano et al.) Group Art Unit: 2814
Serial No.: 08/809,845)
Filed: April 1, 1997) Examiner: N. NGO
For: SOLID-STATE IMAGE SENSING)
APPARATUS AND MANUFACTURING)
METHOD THEREOF)

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97(c)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

RECEIVED

NOV 12 1998

GROUP 2100

Sir:

In accordance with the duty of disclosure, Applicants bring to the attention of the U.S. Patent and Trademark Office a reference cited in a European Search Report, which issued in connection with a European Patent Application corresponding to the above-identified application. The reference cited in the Report is:

Foreign Patent Publications

JP 63 274162A

An English abstract of the foregoing reference and a copy of the Report are enclosed herewith.

06/04/1999 FJONES1 00000001 130203 08809845
01 FC:122 130.00 CH

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 13-0203. A duplicate copy of this communication is enclosed for accounting purposes.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 11/10/92

By: CEY

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, D.C. 20005
Telephone: 202-756-8000
Facsimile: 202-756-8087

143890(225)AN01DS 001



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

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| SERIAL NUMBER | FILING DATE | FIRST NAMED APPLICANT | ATTORNEY DOCKET NO. |
|---------------|-------------|-----------------------|---------------------|
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08/809,845 06/16/97 SAND

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| Y | EXAMINER 433907/225 |
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MM22/0624

MODERMOTT, WILL, & EMERY
600 13TH STREET, N.W.
SUITE 1200
WASHINGTON DC 20005-3096

| | |
|--------------------|--------------------|
| ART UNIT NGO, N | PAPER NUMBER 15 |
|--------------------|--------------------|

DATE MAILED:
2814

06/24/99

- A. ☐ The petition filed _____ under 37 CFR 1.312(b) is granted.
The paper has been forwarded to the examiner for consideration on the merits.

- B. ☒ ^{IDS} The amendment filed 11-10-98 under 37 CFR 1.312 has been considered, and has been:
- ☒ entered and considered.
 - ☐ entered as directed to matters of form not affecting the scope of the invention (0.3311).
 - ☐ disapproved. A report appears below.
 - ☐ entered in part. A report appears below.

Report:

Ngan Van Ngo

**Ngan Van Ngo
Primary Examiner**

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 5,952,714

Issue Date: September 14, 1999

Inventors: Sano et al.

Title: SOLID-STATE IMAGE-SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

Docket No.: 43890-225



Cofc
M.W.

16

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Assistant Commissioner of Patents
Washington, D. C. 20231

APPROVED
JUL 5 2000

Sir:

FOR THE DIRECTOR OF USPTO

In reviewing the above-identified patent, printing errors were discovered therein requiring correction in order to conform the Official Record in the application.

The errors noted are set forth on the two attached copies of form PTO-1050 Rev. 2-93.

As the changes requested herein occurred as a result of errors in the printing the Petters Patent caused by the USPTO, the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, the Applicant requests issuance of the Certificate of Correction.

While it is believed that no fee is necessary, please charge any shortage of fees due in connection with the filing of this paper to Deposit Account 13-0203.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 2/1/00

By:

Michael E. Fogarty
Registration No. 36,139

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Washington, D.C. 20005
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Facsimile: (202) 756-8087

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

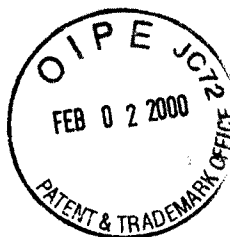
Patent No.: 5,952,714

Issue Date: September 14, 1999

Inventors: Sano et al.

Title: SOLID-STATE IMAGE-SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

Docket No.: 43890-225



REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Assistant Commissioner of Patents
Washington, D. C. 20231

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Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 2/1/00

By: 

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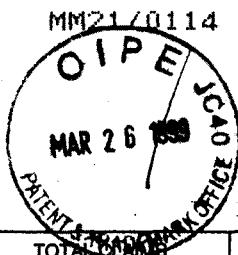
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CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

KENNETH L CAGE
MCDERMOTT WILL & EMERY
1850 K STREET NW
SUITE 450
WASHINGTON DC 20006-2296



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I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

(Depositor's name)

(Signature)

(Date)

| APPLICATION NO. | FILING DATE | TOTAL | EXAMINER AND GROUP ART UNIT | DATE MAILED |
|--|-------------|-------|-----------------------------|-------------|
| 08/809,845 | 06/16/97 | 016 | NGO, N | 2814 |
| First Named Applicant SANDO, YOSHIKAZU | | | | |

TITLE OF INVENTION: SOLID-STATE IMAGE SENSING APPARATUS AND MANUFACTURING METHOD THEREOF

| ATTY'S DOCKET NO. | CLASS-SUBCLASS | BATCH NO. | APPLN. TYPE | SMALL ENTITY | FEE DUE | DATE DUE |
|-------------------|----------------|-------------|-------------|--------------|---------|-----------|
| 2 | 43890/225 | 257-222.000 | N72 | UTILITY | NO | \$1210.00 |
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2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDermott, Will & Emery

2

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE MATSUSHITA ELECTRONICS CORPORATION

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Osaka, JAPAN

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ Corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

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The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature)

(Date)

Michael E. Fogarty

Reg. No. 36,139

26MAR99

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