

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORP.

Petitioner,

v.

NORTH STAR INNOVATIONS INC.

Patent Owner.

Patent No. 6,372,638

Issued: April 16, 2002

Filed: June 22, 2000

Inventors: Robert A. Rodriguez, Heather M. Klesat

Title: METHOD FOR FORMING A CONDUCTIVE PLUG BETWEEN
LAYERS OF AN INTEGRATED CIRCUIT

Inter Partes Review No. 2016-00965

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT LIST

Exhibit No.	Title & Description
1001	U.S. Patent No. 6,372,638 to Rodriguez <i>et al.</i>
1002	Prosecution History of U.S. Patent No. 6,372,638
1003	Declaration of Martin Walker, Ph.D.
1004	U.S. Patent No. 5,580,821 to Mathews <i>et al.</i> (“Mathews”)
1005	U.S. Patent No. 4,939,105 to Langley (“Langley”)
1006	U.S. Patent No. 5,547,892 to Wu <i>et al.</i> (“Wu”)
1007	Excerpts from McGraw-Hill Electronics Dictionary, 6th Ed. (McGraw-Hill, 1997)
1008	Excerpts from Madou, “Fundamentals of Microfabrication” (CRC Press, 1997)
1009	Excerpts from Weste <i>et al.</i> , “Principles of CMOS VLSI Design” (Addison Wesley Longman, 1993)
1010	Excerpts from National Materials Advisory Board, “Plasma Processing of Materials” (National Academy Press, 1985)
1011	Excerpts from Webster’s Third New International Dictionary (1993)

Exhibit No.	Title & Description
1012	U.S. Patent No. 5,327,002 to Motoyoshi (“ <i>Motoyoshi</i> ”)
1013	U.S. Patent No. 5,488,579 to Sharma <i>et al.</i> (“ <i>Sharma</i> ”)
1014	Excerpts from Sharma, “Semiconductor Memories: Technology, Testing, and Reliability” (Wiley, 1997)
1015	U.S. Patent No. 5,801,094 to Yew <i>et al.</i>

I. 37 C.F.R. § 42.8: Mandatory Notices

A. Real Party-In-Interest

The real party in interest of this petition pursuant to § 42.8(b)(1) is Nanya Technology Corp. located at 669 Fusing 3rd Rd., Gueishan Dist., Taoyuan City 333, Taiwan, R.O.C.

B. Related Matters

U.S. Patent No. 6,372,638 (“the ’638 patent”) is the subject of the infringement action styled *North Star Innovations Inc. v. Nanya Tech. Corp. et al.*, Case No. 1:15-CV-01027-GMS (D. Del.), filed on November 5, 2015. In the related district court action, Patent Owner has accused Petitioner and Petitioner’s subsidiary (Nanya Technology Corp. U.S.A.) of infringing the ’638 patent. Patent Owner has not identified any specific claims.

C. Lead And Back-Up Counsel & Service Information

Petitioner provides the following designation of counsel:

Lead Counsel	Back-up Counsel
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II. 37 C.F.R. § 42.15: Fees

Petitioner hereby authorizes the Office to charge to Deposit Account No. 50-1597 (i) \$9,000 for the request fee required by 37. C.F.R. § 42.15(a)(1); and (ii) \$ 14,000 for the Post-Institution fee required by 37 C.F.R. § 42.15(a)(2) for this Petition for *Inter Partes* Review. No excess claim fees are due as Petitioner seeks review of eleven (11) claims. Petitioner further authorizes the Office to charge to the above referenced Deposit Account any additional fees that might be due in connection with this Petition.

Petitioner Nanya Technology Corp. respectfully requests *inter partes* review of Claims 1-11 of U.S. Patent No. 6,372,638 (the “’638 Patent”) in accordance with 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*

III. 37 C.F.R. § 42.104(a): Grounds For Standing

Petitioner hereby certifies that the ’638 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the ’638 patent. Neither Petitioner nor any party in privity with Petitioner has filed a civil action challenging the validity of any claim of the ’638 patent or sought *inter partes* review of any claim of the ’638 patent. Petitioner reserves the right to seek invalidity of any claim of the ’638 patent asserted against Petitioner in the related district court litigation.

Petitioner also certifies that this Petition for *Inter Partes* Review is timely filed. Petitioner’s subsidiary Nanya Technology Corp. U.S.A. was served with the complaint on January 25, 2016. Because this Petition is not more than one year from January 25, 2016, it is timely under 35 U.S.C. § 315(b).

IV. 37 C.F.R. § 42.104(b): Identification Of Challenge

A. Challenged Claims

Petitioner requests *inter partes* review of Claims 1-11 of the ’638 patent.

B. Bases For Challenge

Petitioner requests *inter partes* review in view of the following prior art:

- U.S. 5,580,821 by Mathews *et al.* (“*Mathews*”);
- U.S. 4,939,105 by Langley (“*Langley*”);
- U.S. 5,547,892 by Wu *et al.* (“*Wu*”).

Petitioner requests *inter partes* review based on the following grounds:

- Claims 8-11 are anticipated under 35 U.S.C. § 102(a) by *Mathews*;
- Claims 8-11 are obvious under 35 U.S.C. § 103(a) over *Mathews*;
- Claims 1-7 and 11 are obvious under 35 U.S.C. § 103(a) over *Mathews* in view of *Langley*;
- Claims 1-7 and 11 are obvious under 35 U.S.C. § 103(a) over *Mathews* in view of *Langley* and *Wu*.

C. Claim Construction

See Section V.F below.

D. Unpatentability Of Challenged Claims

See Sections VII-X below.

E. Supporting Evidence

See **Exhibit List** above.

V. **The '638 Patent**

A. **Effective Filing Date**

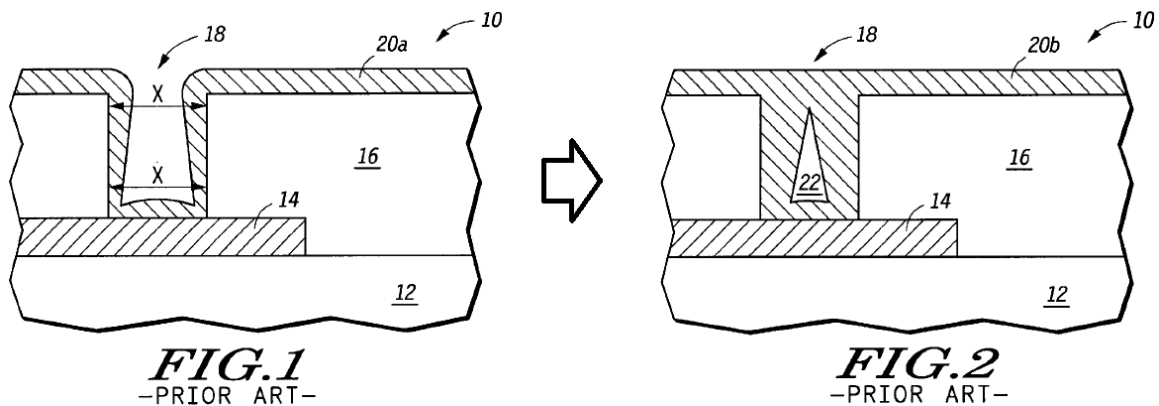
The '638 patent by Robert A. Rodriguez *et al.* issued on April 16, 2002 from Application Ser. No. 09/599,378, filed on June 22, 2000, claiming benefit back to Application Ser. No. 08/802,299, filed on February 18, 1997. Ex. 1001 at Cover Page. For the purpose of this proceeding, Petitioner will treat the effective filing date of the '638 patent as no earlier than February 18, 1997.

B. **Technology Background**

The '638 patent relates to processing of integrated circuits, specifically to the formation of tungsten interconnects, or vias, in a chemical-mechanical polishing (“CMP”) process. Ex. 1001 at 2:28-54; Ex. 1003 at ¶¶ 50-53. CMP was developed in the 1990s. Ex. 1003 at ¶¶ 29-33. It was an advancement over the traditional “conformal” process in that it achieved a more uniform surface and thus allowed process designers to implement complex circuits in multiple layers which were then connected through vias. Ex. 1003 at ¶¶ 29-36.

At the time of the '638 patent invention, vias were often formed using tungsten. Ex. 1001 at 1:17-19. As integrated circuits became smaller and more complex, tungsten vias became narrower and deeper. Ex. 1001 at 1:19-23. This increase in the aspect ratio (depth/radius) of tungsten vias led to manufacturing problems. Ex. 1001 at 1:23-26. Tungsten, due to its “highly nonconformal

deposition characteristics,” accumulates on the top surface of a dielectric layer at a much faster rate than inside a via. Ex. 1001 at 1:29-32; 1:45-48; 1:56-59. The thick layer of tungsten which accumulates on the top surface of the dielectric can block the opening of the via prematurely (*i.e.*, before the vias are completely filled with tungsten) and cause voids (or “keyholes”) to form inside the via, as shown below in FIGS. 1 and 2 of the ’638 patent. Ex. 1001 at 1:54-59; FIGS. 1-2.



Ex. 1001 at FIGS. 1, 2

The voids in the vias caused by the nonconformal deposition of tungsten “create[d] depressed yields, nonfunctional IC die[s] from electrical open circuits, and [caused] electromigration failures over time.” Ex. 1001 at 1:64-67. As tungsten vias became narrower and deeper, such defects became more common. Ex. 1001 at 1:28-34.

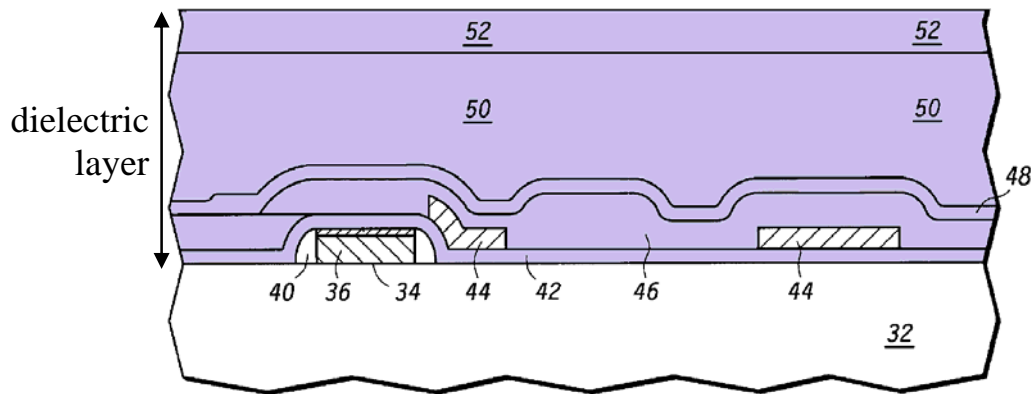
C. Specification

As a proposed solution to this problem, the ’638 patent discloses first

widening the top portion of the openings to allow tungsten to deposit more uniformly inside and subsequently polishing away the widened top portion of the openings to preserve circuit density. Specifically, the proposed method comprises the following steps (figures annotated for illustration purposes):

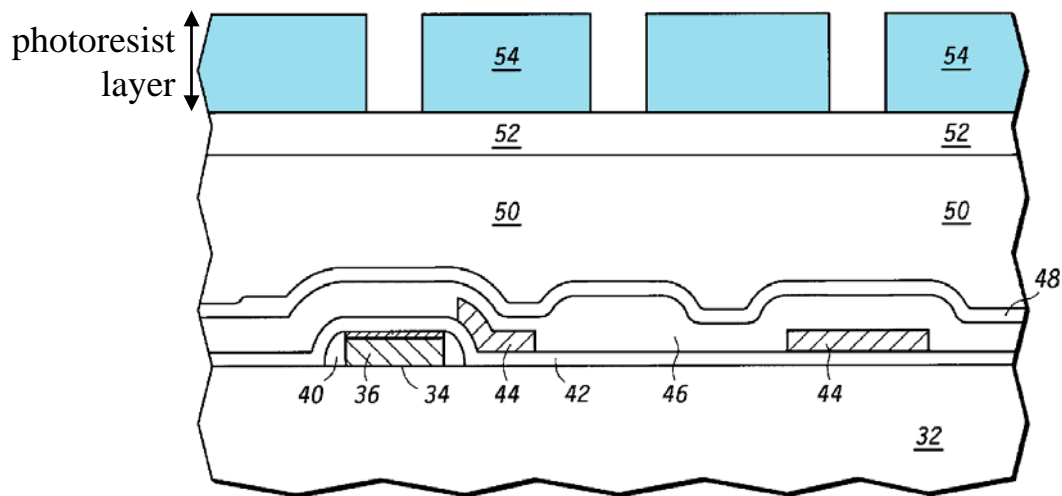
(Step 1) Forming dielectric layers (42-52) over a conductive layer

(36, 44) (Ex. 1001 at 2:57-3:43);

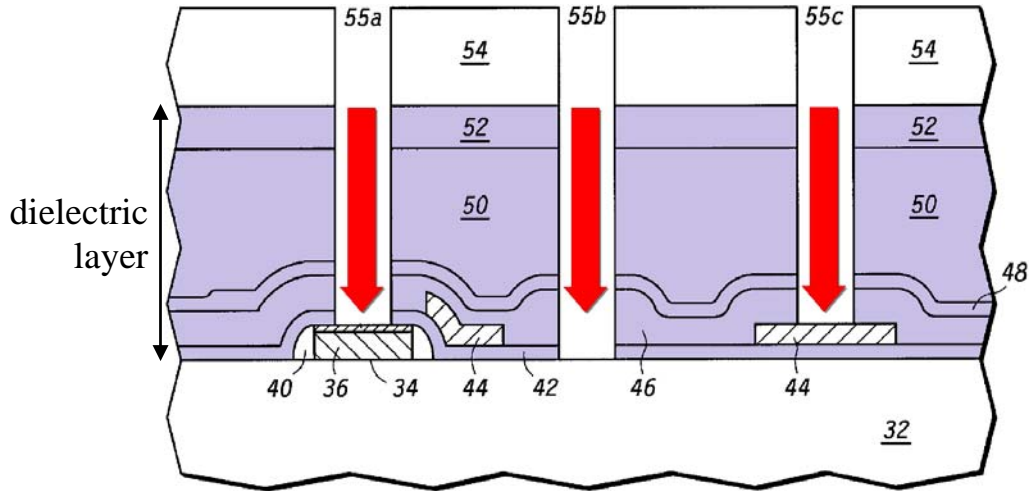


(Step 2) Patterning a photoresist layer (54) over the dielectric

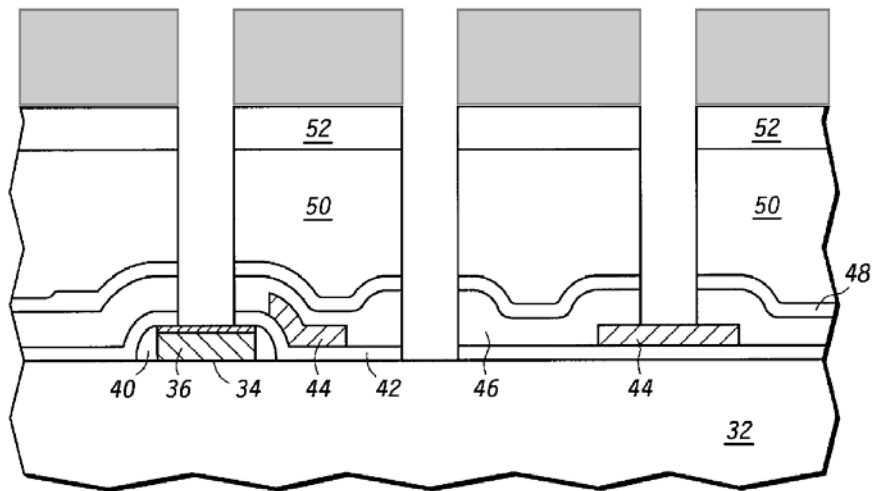
layers (42-52) (Ex. 1001 at 3:44-48);



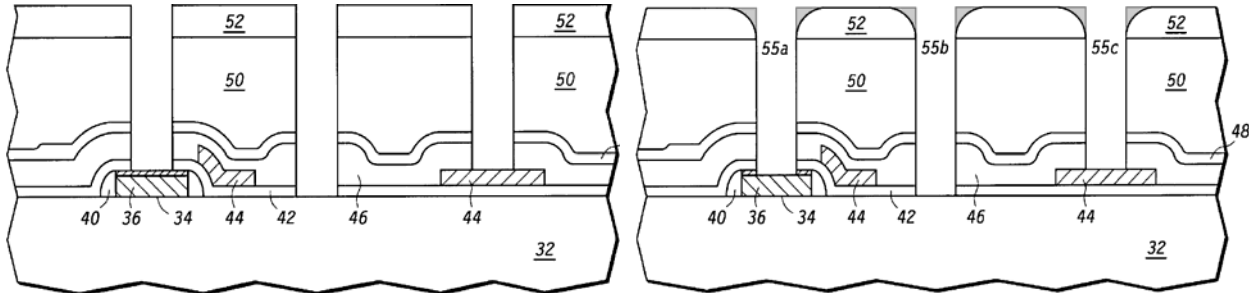
(Step 3) Anisotropically etching the dielectric layers (42-52) to form a vertical contact opening (55a-c) (Ex. 1001 at 3:49-67);



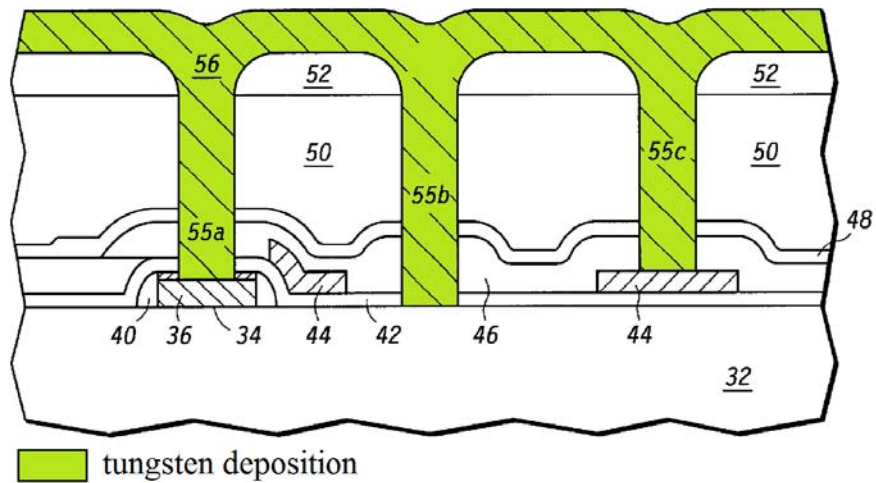
(Step 4) Removing the photoresist layer (54) (Ex. 1001 at 4:1-8, 4:54-5:8);



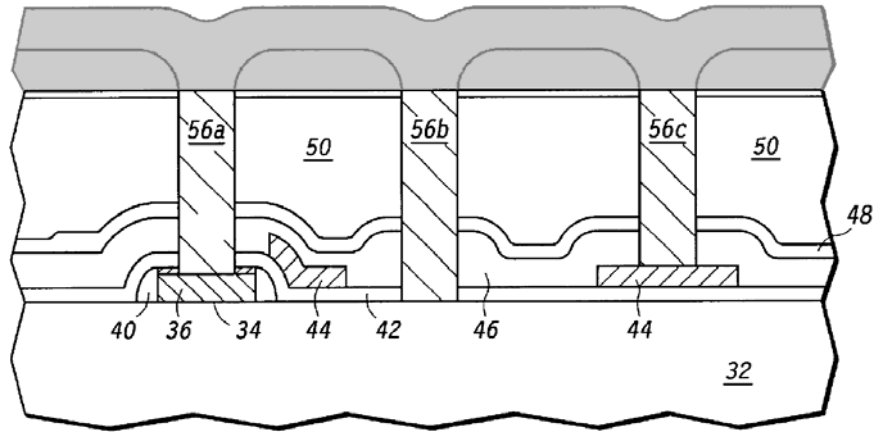
(Step 5) *Anisotropically* etching the dielectric layer (52) to taper the upper portion of the contact opening (55a-c) (Ex. 1001 at 4:9-30, 4:62-5:8).



(Step 6) Depositing tungsten (56) in and above the contact opening (55a-c) (Ex. 1001 at 5:23-54); and



(Step 7) Polishing the bulk tungsten (56) and the tapered upper portion of the contact opening (55a-c) (Ex. 1001 at 5:55-6:12).



The '638 patent further discloses a second embodiment in which the contact opening is: (1) tapered using an *isotropic* etch process and; (2) the photoresist layer is removed *after* the contact opening is tapered. Ex. 1001 at 6:40-7:15, FIGS. 8-11; Ex. 1003 at ¶ 53. The '638 patent states specifically that the above first embodiment utilizes an anisotropic etch to form a “golf tee” shaped taper, while in a second embodiment an isotropic etch is used to form a “wine glass” shaped taper, as shown below. Ex. 1001 at 6:61-65 (comparing FIGS. 5 & 9); Ex. 1003 at ¶ 51.

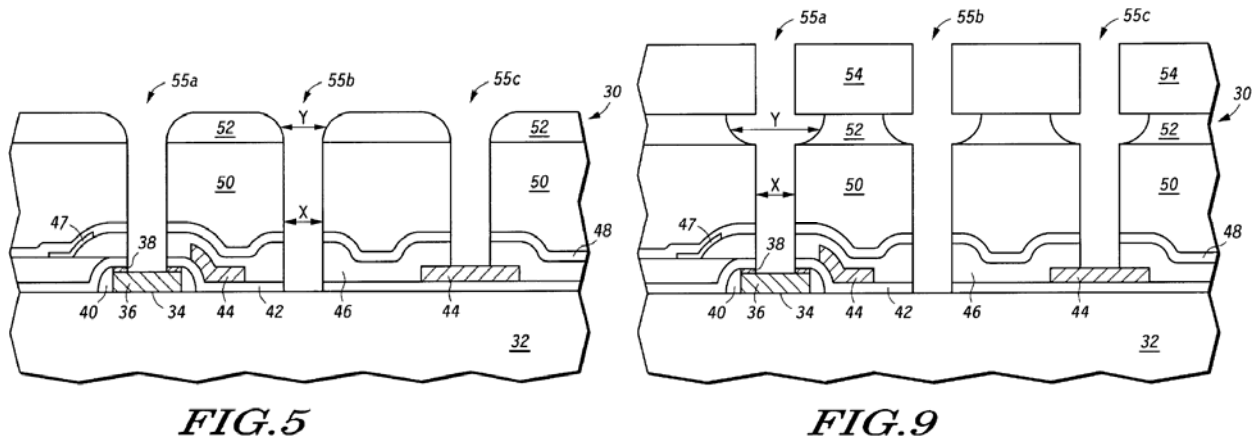


FIG. 5

FIG. 9

Ex. 1001: FIGS. 5 and 9**D. Claims**

The '638 patent recites eleven claims, three independent claims (claims 1, 8 and 11) and eight dependent claims. Claims 8 and 11 generally recite the first embodiment described above, but claim 11 differs from claim 8 in one substantive respect. Whereas claim 8 recites “tapering the top portion of the opening . . . *after* removing of the resist layer,” claim 11 recites “tapering the top portion of the opening . . . *while* removing the resist layer.” Ex. 1001 at Claims 8, 11 (emphasis added). Claim 1 recites additional limitations that are not recited in claim 8 or 11 and is thus narrower.

E. The Person Of Ordinary Skill In The Art

A skilled artisan on February 18, 1997 would have been either a person with a B.S. degree in Electrical Engineering and four or more years of industry experience with semiconductor device fabrication and processing, or a person with

a M.S. in Electrical Engineering and two or more years of industry experience with semiconductor device fabrication and processing. Ex. 1003 at ¶¶ 20-24.

F. Claim Construction

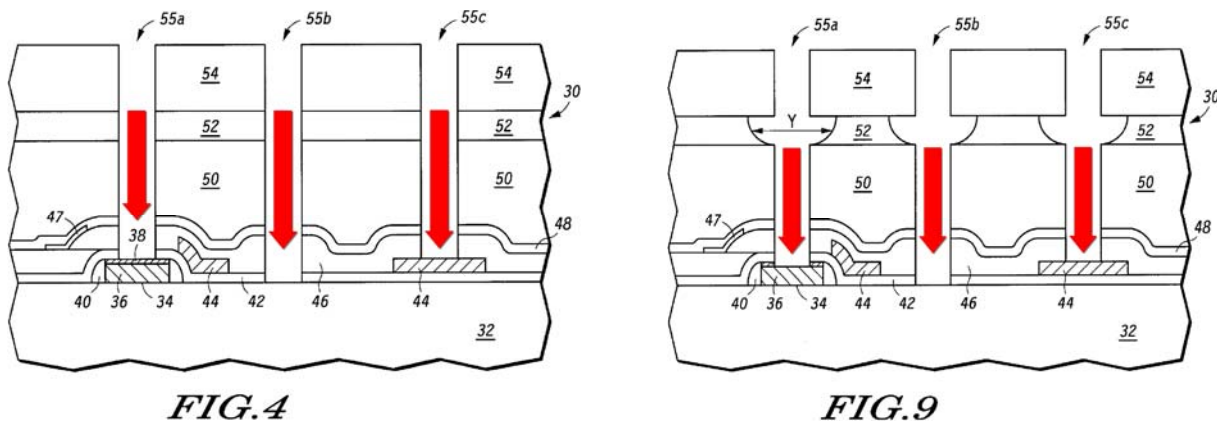
The '638 patent will expire no later than February 18, 2017, which is within 18 months from the filing date of this Petition. Consequently, if *inter partes* review is instituted, the challenged claims should be construed using their ordinary and customary meaning as would be understood by a skilled artisan at the time of the invention in light of the language of the claims, the specification, and the prosecution history of record. IPR2014-00247, Order (Paper 20) at 2-3; *In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012).

Petitioner below construes certain terms that are relevant to the present Petition. Petitioner reserves the right to construe different or additional terms in a different proceeding, including but not limited to the concurrently pending district court litigation.

1. “anisotropically etching” and “anisotropic etch” (claims 8, 11)

The proper construction of the terms “anisotropically etching” and “anisotropic etch” are “non-uniformly etching” and “non-uniform etch,” respectively. Ex. 1003 at ¶ 54. A non-uniform etch is where the etch rate is not uniform in all directions, as opposed to an isotropic etch, which etches material in all directions at substantially the same rate. Ex. 1003 at ¶ 55.

This construction is consistent with the specification and the claim language. The '638 patent discloses at least two examples of anisotropic or non-uniform etching. Ex. 1003 at ¶¶ 56-60. First, the '638 patent discloses forming the vias by etching the dielectric layer in the vertical direction only, which is one form of non-uniform etching. Ex. 1001 at FIG. 4; 3:49-52; FIG. 9; 6:33-7:15; Ex. 1003 at ¶¶ 55, 57.

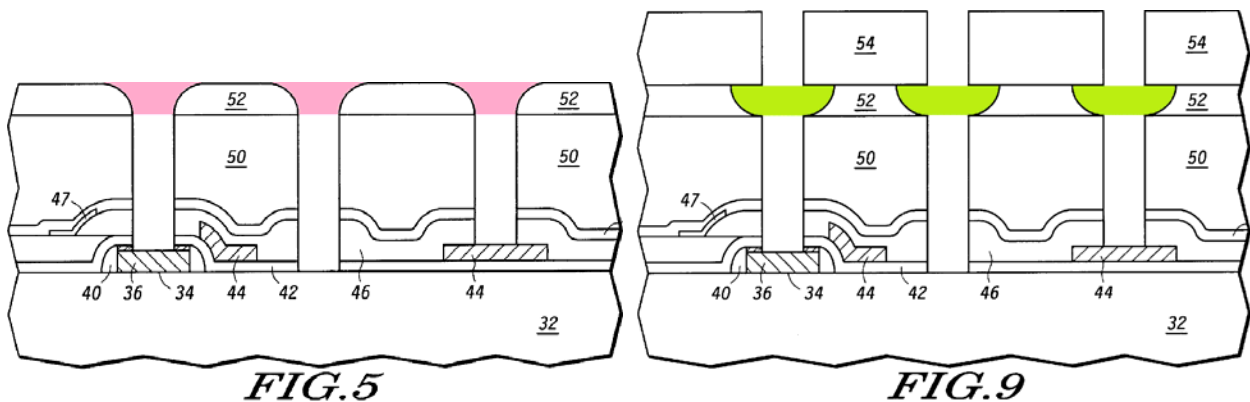


Ex. 1001 at FIGS. 4 & 9 (Annotated)

Claims 8 and 11 of the '638 patent refer to vertical etching the vias as “*anisotropically etching* portions of the dielectric layer . . .” Ex. 1001 at Claims 8, 11 (emphasis added). Since all of the disclosed embodiments etch the vias in the vertical direction only, and the claims refer to such vertical etching as “*anisotropically etching*,” the term “*anisotropically etching*” encompasses vertical etching (which is non-uniform). See e.g., Oatey Co. v. IPS Corp., 514 F.3d 1271, 1277 (Fed. Cir. 2008) (“where claims can reasonably [be] interpreted to include a

specific embodiment, it is incorrect to construe the claims to exclude that embodiment, absent probative evidence on the contrary.”); Ex. 1003 at ¶ 59.

Another example of non-uniform etching, specifically described as “anisotropic” by the ’638 patent, involves etching the top portion of the contact opening to form a “golf tee” shaped contact opening. Ex. 1001 at FIG. 5; 4:9-32. The etch does not uniformly etch the dielectric layer in all directions, as illustrated in FIG. 5, below. The ’638 patent confirms that this “golf tee” profile is created by an anisotropic etch, and distinguishes it from the “wine glass” profile created by an isotropic etch, as shown below. Ex. 1001 at FIGS. 5, 9, 6:61-65 (“Unlike the anisotropic plasma etch taper process illustrated in FIG. 5, the isotropic taper process of FIG. 9 results in a differently-sloped contact profile. The profile of FIG. 4 [sic] is referred to as a ‘golf tee’ profile. Whereas, the profile of FIG. 9 is a ‘wine glass’ profile.”).



Ex. 1001 at FIG. 5 (“Golf Tee”) and FIG. 9 (“Wine Glass”) (Annotated)

Therefore, according to the specification of the '638 patent, the terms “anisotropically etching” and “anisotropic etch” mean “non-uniformly etching” and “non-uniform etch,” respectively, in terms of the direction(s) of the etch. Ex. 1003 at ¶¶ 55-60.

This construction is also consistent with the understanding of a person of ordinary skill in the art at the time of the alleged invention. Ex. 1003 at ¶ 58. A skilled artisan would have defined the term “anisotropic etching” as “non-uniform etching.” Ex. 1003 at ¶¶ 54-57; Ex. 1007¹ at p. 19 (defining “anisotropic etching” as “preferential directional etching of a material,” *i.e.*, not uniform in all directions).

¹ McGraw-Hill Electronics Dictionary, 6th Ed. (Ex. 1007) is a technical dictionary on various terms used in the field of electronics with a copyright date of 1997. Ex. 1007 at Copyright Page. Upon information and belief, Ex. 1007 was first published on or around June 1997, *i.e.*, around the effective filing date of the '638 patent. Petitioner cites to Ex. 1007 merely to describe the state of the relevant technology and the knowledge and understanding of a skilled artisan around the effective filing date of the '638 patent and not as prior art.

For example, “The Fundamentals of Microfabrication”² (Ex. 1008), a contemporaneous treatise, classifies different types of etched features as having been formed in either isotropic or anisotropic etching processes, as shown below.

Ex. 1003 at ¶¶ 38-39, 55; Ex. 1008 at FIGS. 2.2 (p. 56), 4.30 (p. 174).

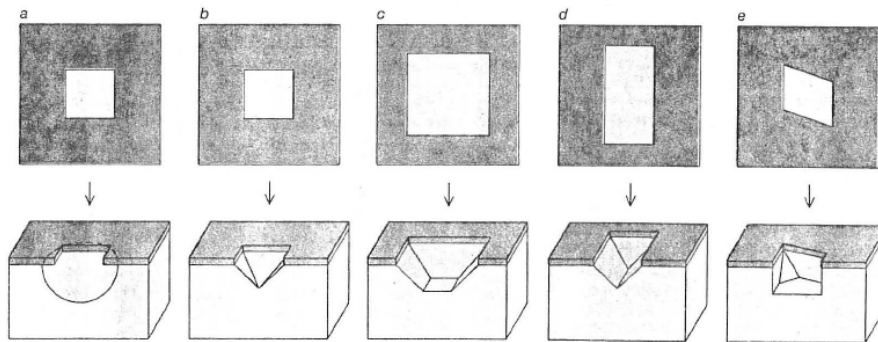


FIGURE 4.30 . Isotropic and anisotropic etched features in $\langle 100 \rangle$ and $\langle 110 \rangle$ wafers. (a) isotropic etch; (b) to (e) anisotropic etch. (a) to (d): $\langle 100 \rangle$ oriented wafers and (e): $\langle 110 \rangle$ oriented wafer.

Ex. 1008 at FIG. 4.30 (p. 174): Wet Etch Profiles (Annotated)

² “Fundamentals of Microfabrication” by Marc J. Madou (Ex. 1008) is a technical treatise on IC fabrication with a copyright date of 1997. Upon information and belief, Ex. 1008 was first published in or around September 1997, *i.e.*, around the effective filing date of the ’638 patent. Petitioner cites to Ex. 1008 merely to describe the state of the relevant technology and the knowledge of a skilled artisan around the effective filing date of the ’638 patent and not as prior art.

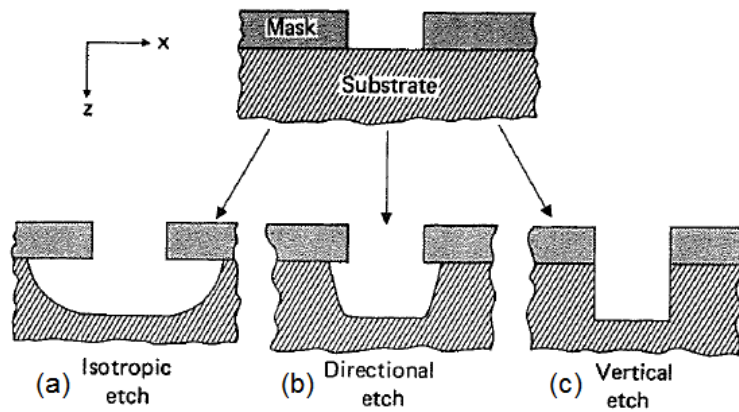


FIGURE 2.2 Directionality of etching processes.

Ex. 1008 at FIG. 2.2 (p. 56): Dry Etch Profiles (Annotated)

An isotropic etch, which etches materials equally in all directions, creates a spherical cavity, the radius of which is dependent upon the opening and etch parameters. Ex. 1003 at ¶¶ 39, 56; Ex. 1008 at FIGS. 2.2(a), 4.30(a). The spherical cavity disclosed in the prior art treatise is created by the same type of isotropic etch as the “wine glass” cavity shown in FIG. 9 of the ’638 patent. Ex. 1003 at ¶ 56; compare Ex. 1008 at FIGS. 2.2(a), 4.30(a) and Ex. 1001 at FIG. 9.

In contrast, non-spherical, and thus non-uniform, cavities are formed in the anisotropic etches in the various examples, above, including FIG. 4.30(b)-(e) and FIG. 2.2(b)-(c). Ex. 1003 at ¶¶ 38-39, 55-57; Ex. 1008 at FIGS. 2.2(b)-(c) (annotated), 4.30 (b)-(e).

Another treatise, “Principles of CMOS VLSI Design” (Ex. 1009)³ discloses a similar understanding. As illustrated in the figure below, the etch rate for isotropic etching is substantially equal in all directions (*i.e.*, “ $x = y$ ”). Ex. 1003 at ¶ 56; Ex. 1009 at FIG. 3.12(a) (p. 129).

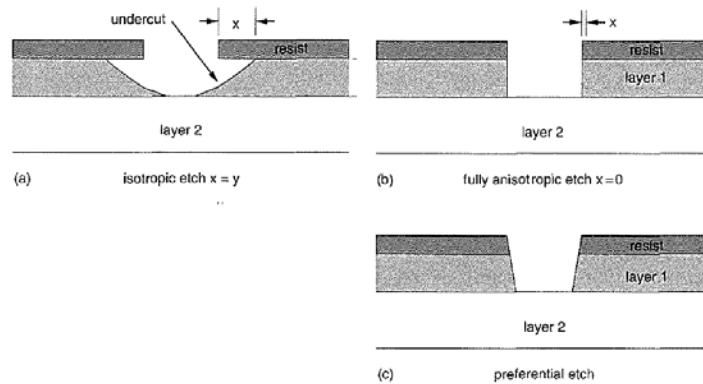


FIGURE 3.12 Classification of etching processes

Ex. 1009 at FIG. 3.12

In contrast, anisotropic etching leads to unidirectional erosion, as illustrated in FIG. 3.12(b), or preferential erosion primarily in one direction, as illustrated in

³ “Principles of CMOS VLSI Design” by Weste *et al.* (Ex. 1009) is a treatise on CMOS IC design with a copyright date of 1994. Ex. 1009 at Copyright Page. Upon information and belief, Ex. 1009 was first published in or around October 1994. Petitioner cites Ex. 1009 merely to describe the state of the relevant technology and the knowledge of a skilled artisan around the effective filing date of the ’638 patent and not as prior art.

FIG. 3.12(c). Ex. 1003 at ¶¶ 39, 44, 55-58; Ex. 1009 at FIG. 3.12(b)-(c) (p. 129).

In summary, both the specification of the '638 patent and the understanding of a skilled artisan support the construction of the terms “anisotropically etching” and “anisotropic etch” as “non-uniformly etching” and “non-uniform etch,” respectively, in terms of the direction of the etch. Ex. 1003 at ¶¶ 54-60.

2. “storage node of an SRAM cell” (claim 6)

The proper construction of the term “storage node of an SRAM cell” is a “node of the storage transistors of an SRAM cell where the data (or its complement) is stored,” where a “node” is a “connection of two or more conductive paths.”

The '638 patent does not define the term “storage node.” However, a person of ordinary skill in the art would have understood that the term “storage node of an SRAM cell” refers to a “node of the storage transistors of an SRAM cell where the data (or its complement) is stored.” Ex. 1003 at ¶¶ 61-66. A skilled artisan would also have understood that the term “node” means “a connection of two or more conductive paths or regions.” Ex. 1003 at ¶ 61; Ex. 1011⁴ at p. 1533 (defining

⁴ “Webster’s 3rd New International Dictionary” (Ex. 1011) has a copyright date of 1993. Ex. 1011 at Copyright Page. Upon information and belief, Ex. 1011 was first published on or around December 1993. Petitioner cites Ex. 1011

“node” as “a point in an electrical network at which several branches come together”).

FIG. 2-4 of “Semiconductor Memories,”⁵ a contemporaneous treatise, discloses two well-known SRAM cell structures. Ex. 1003 at ¶ 62; Ex. 1014 at FIG. 2-4(a)-(b).

merely to describe the knowledge of a skilled artisan around the effective filing date of the ’638 patent and not as prior art.

⁵ “Semiconductor Memories: Technology, Testing, and Reliability” is a treatise on semiconductor memory design with a copyright date of 1997. Ex. 1014 at Copyright Page. Upon information and belief, Ex. 1014 was first published in 1997. Petitioner cites Ex. 1014 merely to describe the state of the relevant technology and the knowledge of a skilled artisan around the effective filing date of the ’638 patent and not as prior art.

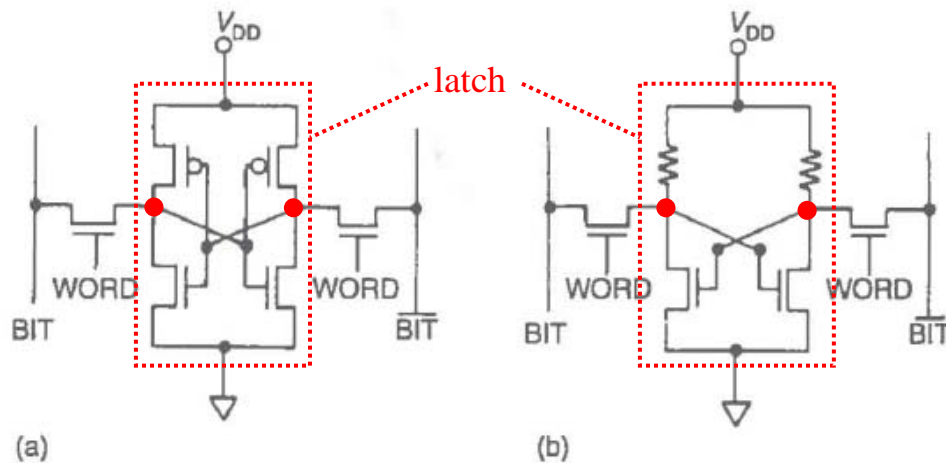
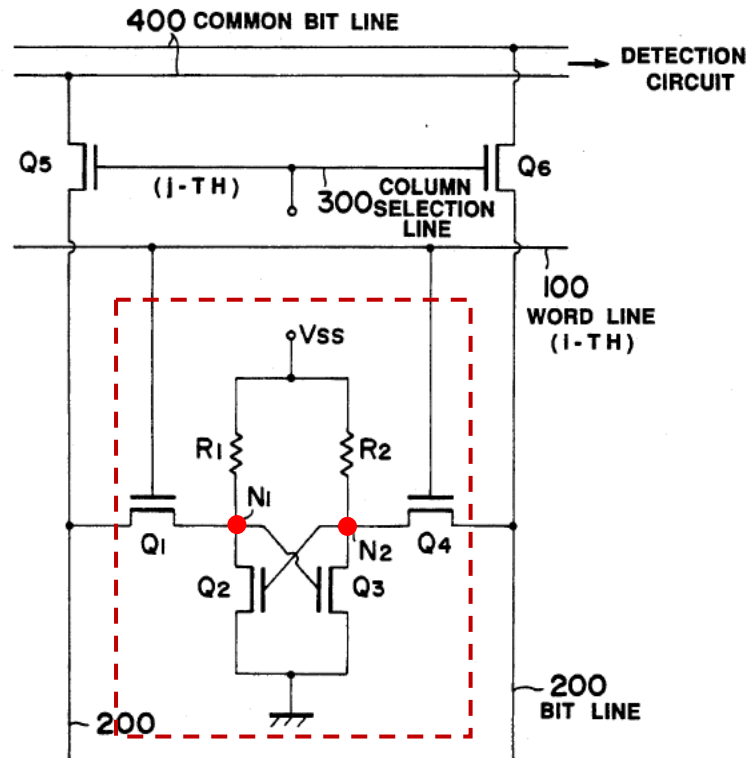


Figure 2-4. Various configurations of CMOS SRAM cells. (a) Six-transistor full CMOS. (b) Four transistors with R-load NMOS.

Ex. 1014 at FIG. 2-4 (p. 13) (Annotated)

Shown in FIG. 2-4(a) is a six-transistor SRAM cell with four transistors forming a latch for storing the SRAM cell data and its complement (“latch transistors” or “storage transistors.”). Ex. 1003 at ¶¶ 62-63; Ex. 1014 at FIG. 2-4(a). FIG. 2-4(b) shows a four-transistor SRAM cell with two storage transistors forming a latch for storing the SRAM cell data and its complement. Ex. 1003 at ¶¶ 62-63; Ex. 1014 at FIG. 2-4(b). In the well-known SRAM cell structures shown above, the SRAM cell data or its complement is stored at the node(s) where the gate of a storage transistor and the drain of an opposing storage transistor are coupled together (in red). Ex. 1003 at ¶¶ 62-63; Ex. 1014 at FIG. 2-4. These nodes correspond to a “storage node.” Ex. 1003 at ¶ 63.

The following references show that a skilled artisan actually defined and used the term “storage node” to mean the “node of the storage transistors of an SRAM cell where the data (or its complement) is stored.” FIG. 11 of U.S. Patent No. 5,327,002 by Motoyoshi (Ex. 1012; “*Motoyoshi*”) discloses the same four-transistor SRAM cell that is disclosed in FIG. 2-4(a) of the “Semiconductor Memories” treatise, as shown below. Ex. 1003 at ¶ 64; Ex. 1012 at FIG. 11.

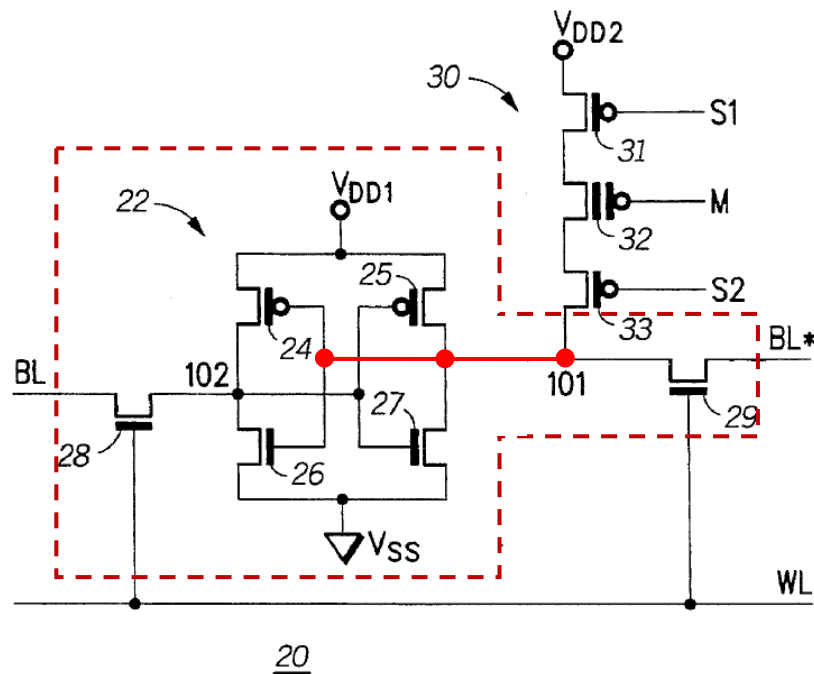


Ex. 1012 at FIG. 11 (Annotated)

As illustrated in FIG. 11 of *Motoyoshi*, nodes N1 and N2 are formed by coupling the drain and gate electrodes of the storage transistors Q2 and Q3 together, and

they maintain the SRAM cell data and its complement. Ex. 1003 at ¶ 64; Ex. 1012 at FIG. 11 (annotated).

FIG. 1 of U.S. Patent No. 5,488,579 by Sharma *et al.* (Ex. 1013; “Sharma”) discloses the same six-transistor SRAM cell that is disclosed in FIG. 2-4(b) of the “Semiconductor Memories” treatise. Ex. 1003 at ¶ 65; Ex. 1013 at FIG. 1 (annotated below).



Ex. 1013 at FIG. 1 (Annotated)

Sharma refers to node 101 in FIG. 1 as a “storage node.” Ex. 1013 at 3:59-61. As illustrated in FIG. 1 of *Sharma*, storage node 101 is formed by coupling the gates of storage transistors 24 and 26 to the drains of storage transistors 25 and 27, and stores the complement of the SRAM cell data (node 102 storing the non-

complement). Ex. 1003 at ¶ 65; Ex. 1013 at FIG. 1.

As exemplified by the two contemporaneous references above, a skilled artisan would have understood that the term “storage node of an SRAM cell” means a “node of the storage transistors of an SRAM cell where the data (or its complement) is stored.” Ex. 1003 at ¶¶ 61-66. Furthermore, a skilled artisan would have understood that the “node of the storage transistors of an SRAM cell where the data (or its complement) is stored” is where the gate(s) and drain(s) of opposing storage transistors are coupled together. Ex. 1003 at ¶¶ 61-66.

3. “*current electrode for a transistor*” (claim 7)

The proper construction of the term “current electrode for a transistor” is “a current conducting electrode in a transistor, such as a source or drain electrode.” The ’638 patent expressly defines the term “current electrode” as one of the “source and drain” electrodes. Ex. 1003 at ¶ 67; Ex. 1001 at 3:25-27 (“The exact current electrodes (source and drain) are not specifically illustrated in FIG. 4.”).

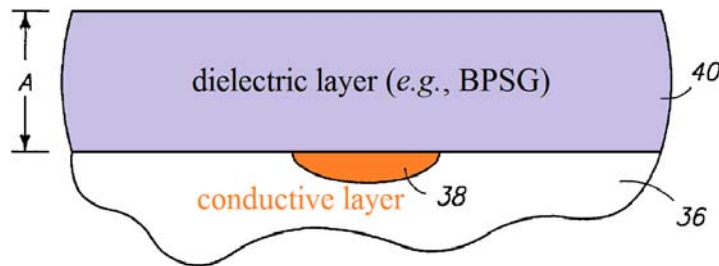
VI. Prior Art And Motivations To Combine

A. U.S. Patent No. 5,580,821 (“*Mathews*”)

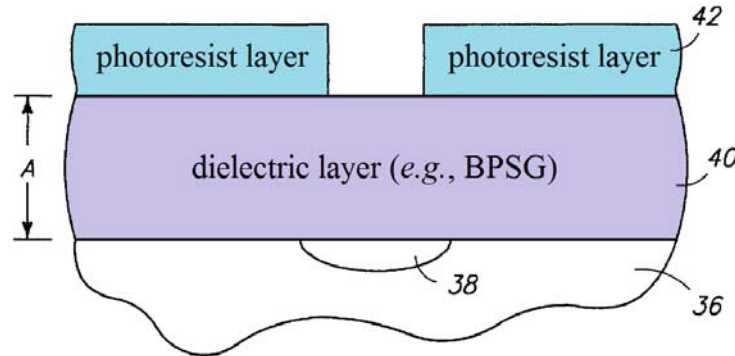
U.S. Patent No. 5,580,821 by Viju K. Mathews *et al.* (Ex. 1004; “*Mathews*”) issued on December 3, 1996 from Application Ser. No. 08/391,719, filed on February 21, 1995. Consequently, *Mathews* is prior art to the ’638 patent under 35 U.S.C. § 102(a).

Mathews is directed to solving the same problem addressed by the '638 patent, *i.e.*, forming void-free tungsten vias in integrated circuits without sacrificing circuit density. Ex. 1004 at 4:15-16; 4:30-32; Ex. 1003 at ¶¶ 50, 69. The solution *Mathews* proposed is identical to the solution proposed by the '638 patent: widening the contact opening to facilitate uniform tungsten depositions (Ex. 1004 at 3:39-42; FIGS. 4, 5; Ex. 1003 at ¶¶ 70-71); and subsequently removing the widened portion to preserve the circuit density of the device (Ex. 1004 at 4:17-42; FIGS. 7-8; Ex. 1003 at ¶ 73). Specifically, *Mathews* discloses a method for forming void-free tungsten vias comprising the following steps (figures annotated for illustration purposes):

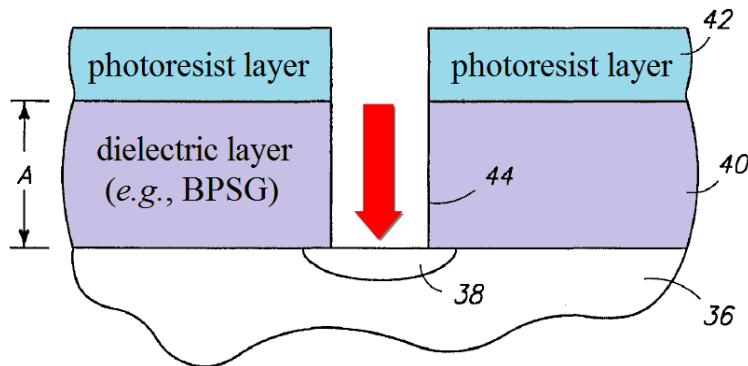
- (Step 1) Forming a dielectric layer (40) over a conductive layer (38)
(Ex. 1004 at 3:21-24);



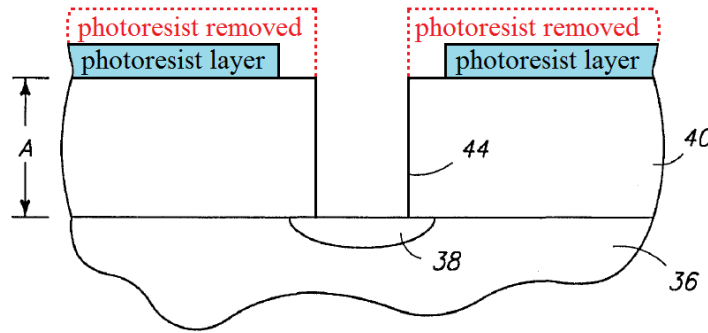
- (Step 2) Forming and patterning a photoresist layer (42) over the dielectric layer (40) (Ex. 1004 at 3:25-29);



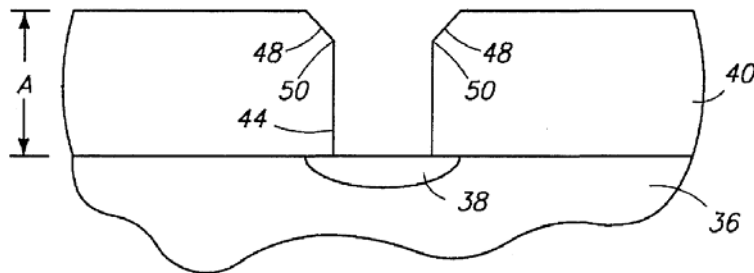
- (Step 3) Anisotropically etching the dielectric layer (40) to form a contact opening (44) (Ex. 1004 at 3:26-32);



(Step 4) Removing some or all of the photoresist layer (42) to expose the dielectric layer near the contact opening (Ex. 1004 at 3:45-49; Ex. 1003 at ¶¶ 71, 110-12)⁶;

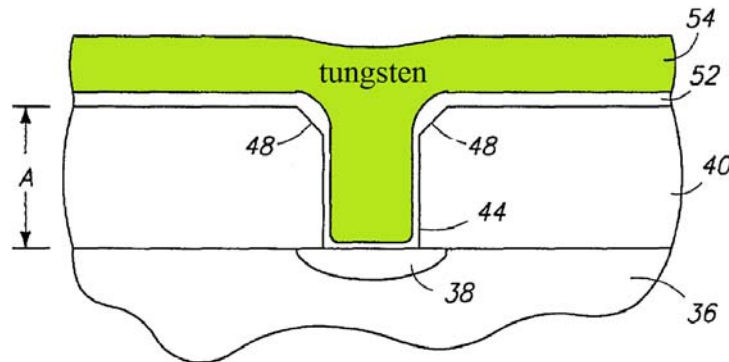


(Step 5) Anisotropically sputter etching the upper portion of the contact opening (44) to form sloped sidewalls (Ex. 1004 at 3:39-44; Ex. 1003 at ¶¶ 71, 96-98);

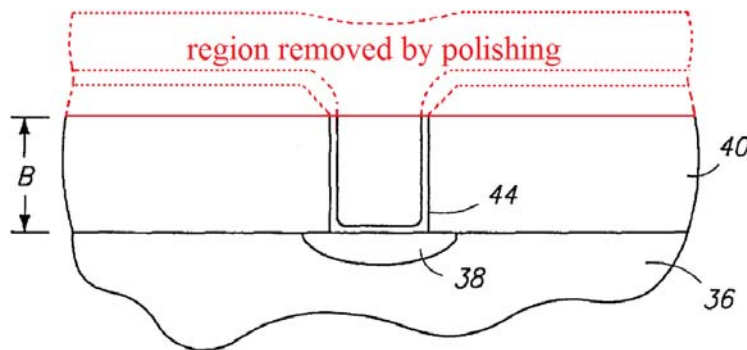


⁶ *Mathews* discloses stripping the photoresist away from the via to expose the dielectric layer adjacent to the via. Ex. 1004 at 3:38-49; Ex. 1003 at ¶¶ 71, 110-12. The figure merely illustrates one of many possibilities embodied in *Mathews*.

(Step 6) Depositing metal (e.g., titanium (48) and/or tungsten (54)) over the wafer and in the contact opening (44) (Ex. 1004 at FIG. 7, 4:1-10); and



(Step 7) Polishing the bulk tungsten (54) and the upper portion of the contact opening (48) (Ex. 1004 at FIG. 8, 4:17-25, 33-42).



Mathews provides the same reason as the '638 patent for widening the top portion of the contact opening and subsequently removing the widened top portion. Ex. 1003 at ¶¶ 59, 60. *Mathews* explains that by widening the top portion of the contact opening, “cusp formation is avoided such that keyholes and fangs are substantially eliminated.” Ex. 1004 at 4:30-31; Ex. 1003 at ¶ 72. *Mathews* further

explains that the widened top portion of the contact opening is removed such that “small-size/maximum density goals are not defeated.” Ex. 1004 at 4:31-32; Ex. 1003 at ¶ 73.

In summary, *Mathews* identifies the same problem as the '638 patent and proposes solving the same problem in the same way as the '638 patent to achieve the same result. Ex. 1003 at ¶¶ 50, 69.

B. U.S. Patent No. 4,939,105 (“*Langley*”)

I. Overview

U.S. Patent No. 4,939,105 by Rod C. Langley (Ex. 1005; “*Langley*”) issued on July 3, 1990 from Application Ser. No. 07/388,841 filed on August 3, 1989. Consequently, *Langley* is prior art to the '638 patent under 35 U.S.C. §§ 102(a) and (b).

Langley is directed to methods for forming void-free vias in integrated circuits in a “conformal” process. Ex. 1005 at 1:6-10; Ex. 1003 at ¶¶ 75, 76. Specifically, *Langley* discloses a method for forming vias in integrated circuits comprising the following steps:

- 1) Forming and patterning a photoresist layer (14) over an oxide layer (13) (Ex. 1005 at 3:4-10);

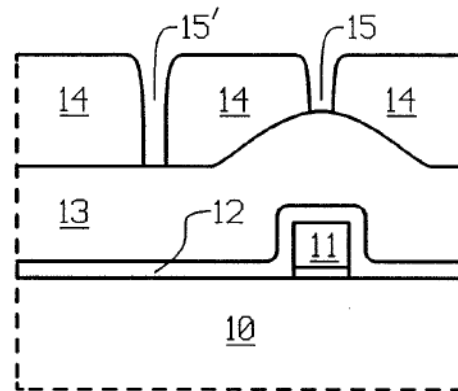


FIG. 4

- 2) Etching portions of the photoresist layer (14) using a mixture of oxygen and fluorocarbon gas to form a slope in the photoresist layer (14) (Ex. 1005 at 3:36-47);

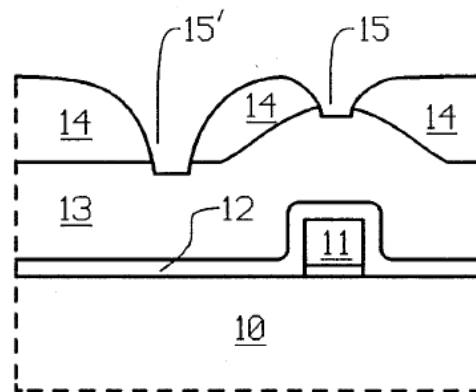


FIG. 5

- 3) Etching the oxide layers (12, 13) and remaining portions of the photoresist layer (14) using a mixture of fluorocarbon gas to form a slope in the oxide layers (12, 13) (Ex. 1005 at 3:48-61); and

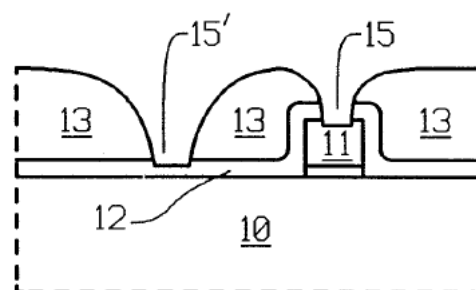


FIG. 6

- 4) Etching remaining oxide in the contact openings (15, 15') (Ex. 1005 at 3:62-4:20).

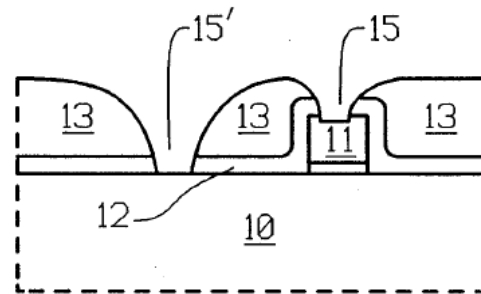


FIG. 7

2. Motivation To Combine Mathews With Langley

Mathews and *Langley* are in the same field of endeavor and propose the same solutions to the same problem. Ex. 1003 at ¶ 127. Both *Mathews* and *Langley* disclose methods for forming void-free vias in integrated circuits. Ex. 1004 at 1:6-8; Ex. 1005 at 1:6-10; Ex. 1003 at ¶ 127. Both identify the formation of voids inside vias as a problem, and both propose widening the top portion of the vias as a solution to this problem. Ex. 1004 at 2:53-3:15; Ex. 1005 at 2:25-46; Ex. 1003 at ¶ 127. Because of the overlap in the field of endeavor, the problems addressed, and the solutions presented, a skilled artisan trying to solve the problem of void formations in vias would have been motivated to consider and combine *Mathews* and *Langley* together. Ex. 1003 at ¶ 127.

Specifically, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Langley* with *Mathews*. Ex. 1003 at ¶ 125. When the semiconductor industry began utilizing CMP for planarization (in the 1990s), process designers combined various etching and metallization techniques

from the conformal process era with CMP. Ex. 1003 at ¶ 126. *Langley* discloses etching techniques for a conformal process. *Id.* Accordingly, it would have been obvious for a person of ordinary skill in the art to combine the etching technologies taught in *Langley* with the CMP process disclosed in *Mathews*. Ex. 1003 at ¶¶ 125-26.

Furthermore, there is a significant overlap between *Mathews* and *Langley* in their etching techniques. Both *Mathews* and *Langley* disclose using dry (plasma) etching to form a contact opening. Ex. 1003 at ¶ 127; Ex. 1004 at 3:33-35; Ex. 1005 at 3:27-30. In particular, both disclose using fluorocarbon gas mixtures to etch the dielectric layer. Ex. 1003 at ¶ 127; Ex. 1004 at 3:33-37; Ex. 1005 at 3:36-4:20. *Mathews* and *Langley* also teach and suggest performing all etching and photoresist removal steps in a single plasma chamber. Ex. 1003 at ¶ 127; Ex. 1004 at 3:56-67; Ex. 1005 at 3:27-30. In light of the overlap in the etch type, chemical, and environment, it would have been simple for a skilled artisan to substitute one or more etching steps disclosed in *Langley* for the etching steps disclosed in *Mathews*. Ex. 1003 at ¶ 127.

C. U.S. Patent No. 5,547,892 (“Wuu”)

1. Overview

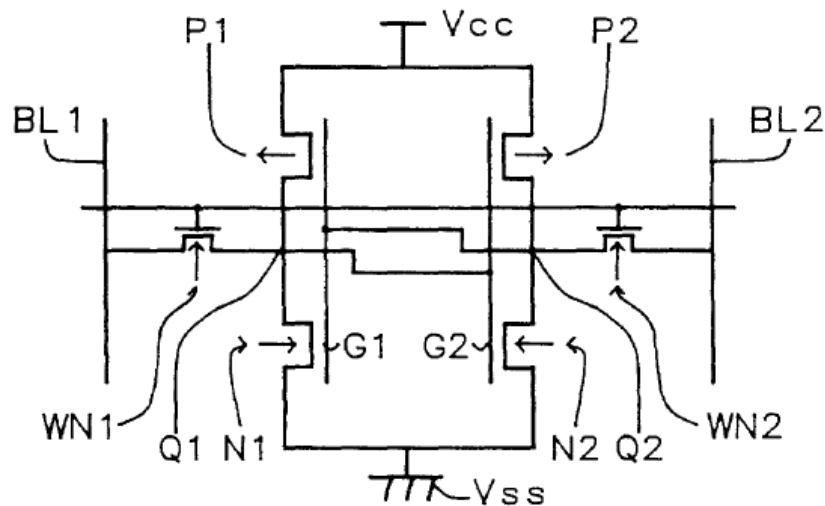
U.S. Patent No. 5,547,892 by Shou-Gwo Wuu *et al.* (Ex. 1006; “Wuu”) issued on August 20, 1996 from application Ser. No. 08/429,725 filed on April 27,

1995. Consequently, *Wuu* is prior art to the '638 patent under 35 U.S.C. § 102(a).

Wuu is directed to methods for forming low-resistance contacts in Static Random Access Memories (“SRAMs”). Ex. 1006 at 2:50-55; Ex. 1003 at ¶¶ 80-82.

FIG. 1 of *Wuu* illustrates a six-transistor SRAM cell (storage transistors P1, P2, N1, N2 and access transistors WN1, WN2). Ex. 1006 at 1:30-35, FIG. 1;

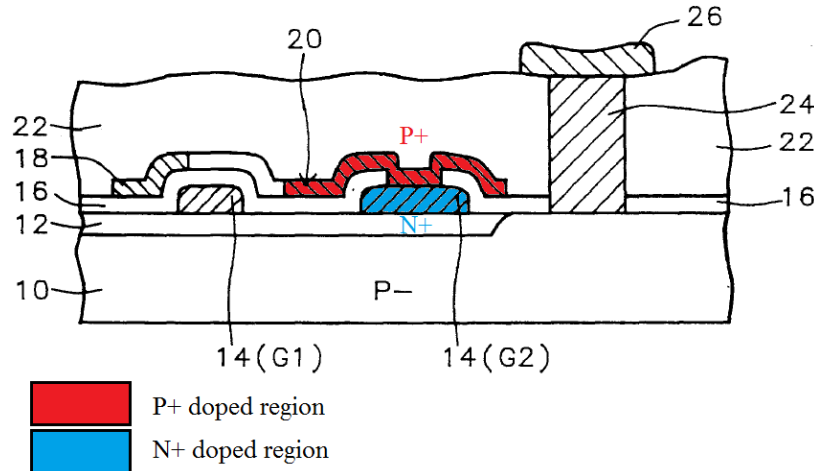
Ex. 1003 at ¶ 80.



Ex. 1006 at FIG. 1

As illustrated in FIG. 1, storage transistors P1, P2, N1, and N2 collectively store the data and its complement at nodes N1 and N2. Ex. 1006 at FIG. 1; Ex. 1003 at ¶ 80. The storage node Q1 is at the connection of the drain of the transistor N1 to the gate G2 of opposing transistor N2. Ex. 1006 at 2:14-18; Ex. 1003 at ¶ 80.

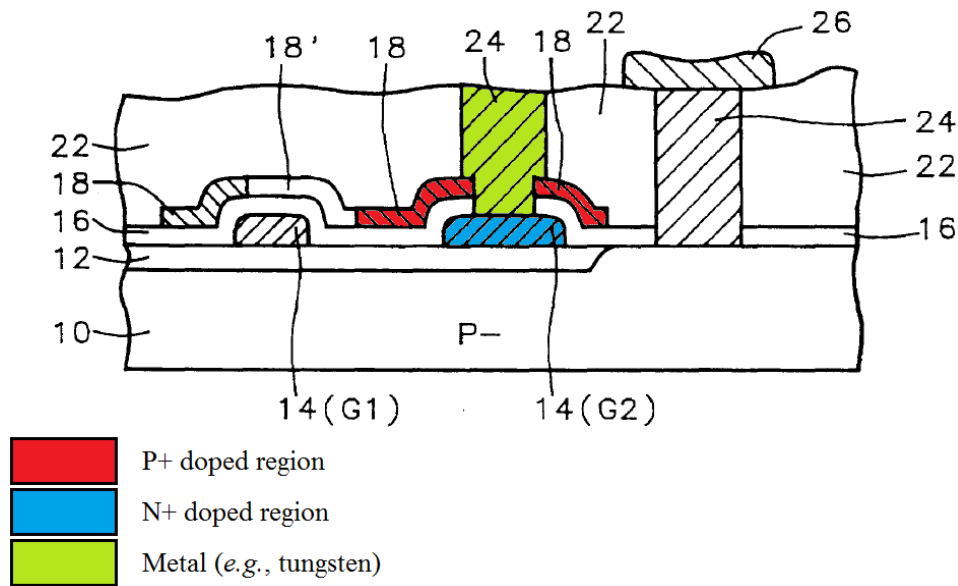
FIG. 5 of *Wuu* illustrates a cross sectional view of a prior art six-transistor SRAM cell. Ex. 1006 at 3:61-64.



Ex. 1006 at FIG. 5 (Annotated)

In FIG. 5 of *Wuu*, the gate electrodes of P2 and N2 (G2) (in blue) come in direct contact with the drain electrodes of P1 and N1 (20) (in red) to form the storage node Q1. Ex. 1006 at FIG. 5. The direct connection between the drain electrode (20) and the gate electrode (G2) creates a P/N-junction, which undesirably increases the resistance of the storage node Q1. Ex. 1006 at 2:34-41; Ex. 1003 at ¶ 81.

Recognizing the need to eliminate the P/N-junction at the storage node Q1, *Wuu* proposes connecting the drain electrode of transistor P1 (20) and the gate electrode (G2) to a contact plug (24), as shown below in FIG. 9. Ex. 1006 at FIG. 9; 7:4-9; Ex. 1003 at ¶¶ 80-81.



Ex. 1006 at FIG. 9 (Annotated)

The contact plug (24), or via, shorts the P/N-junction (G2 and 20 in FIG. 5) and thus forms a low resistance connection for the storage node (Q1). Ex. 1006 at 3:48-51; Ex. 1003 at ¶ 81. *Wuu* further proposed forming the via (24) using tungsten. Ex. 1006 at 7:12-16 (“The conductive plugs 24 are preferably composed of a refractory metal, such as tungsten . . .”); Ex. 1003 at ¶ 82.

2. Motivation To Combine Mathews And Langley With Wuu

As discussed above, *Wuu* expressly discloses and teaches using tungsten to form the contact plugs in an SRAM. Ex. 1003 at ¶ 166. But as *Mathews*, and *Langley*, and the '638 patent explain, voids tend to form inside tungsten vias, especially vias that are not tapered, such as the type illustrated in FIG. 5 of *Wuu*, increasing the resistance of the via and the likelihood of defects in the integrated

circuit. Ex. 1001 at 1:54-62, 64-67; Ex. 1004 at 1:40-44; Ex. 1006 at FIG. 5; Ex. 1003 at ¶ 166.

A person of ordinary skill in the art practicing *Wuu* at the time of the invention would have experienced void formations in the tungsten vias of the SRAM cells and thus would have been motivated to find a solution to the problem. Ex. 1003 at ¶ 168. *Mathews* and *Langley* provides such a solution. Hence, a skilled artisan practicing *Wuu* would have been motivated to combine the specific teachings of *Mathews*, and *Langley* with *Wuu* to solve the problem of void formations inside tungsten plugs. Ex. 1003 at ¶ 168.

VII. Claims 8-11 Are Anticipated By *Mathews*⁷

A. Claim 8 Is Anticipated By *Mathews*

1. Preamble

The preamble of Claim 8 recites “[a] method for forming an integrated circuit.” Ex. 1001 at 8:22. *Mathews* discloses “[a] semiconductor processing method of forming an electrically conductive contact plug relative to a wafer . . .” Ex. 1004 at Abstract, 1:7-9. Therefore, *Mathews* discloses the preamble of Claim

⁷ Independent Claims 8 and 11 are broader than independent Claim 1. Hence, Claims 8-11 are discussed first, followed by Claims 1-7.

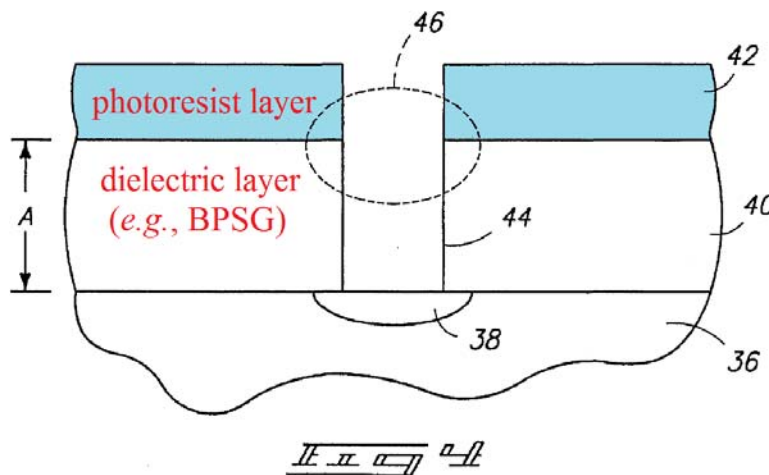
8;⁸ Ex. 1003 at ¶ 91.

2. Claim Element [8a]

Claim element [8a] recites “patterning a resist layer over a dielectric layer.”

Ex. 1001 at 8:24.

As illustrated in FIG. 4, below, *Mathews* discloses forming a dielectric layer (40) using an electrically insulative material, such as borophosphosilicate glass (BPSG). Ex. 1004 at FIG. 4; 3:22-24 (“Preferably, the material layer 40 comprises an electrically insulative material, with BPSG being one of example preferred material.”); Ex. 1003 at ¶ 70.



Ex. 1004 at FIG. 4 (Annotated)

⁸ *Mathews* further discloses the preamble at at disclosures: Ex. 1004 at Abstract; 1:7-9; FIGS. 4-9; and *passim*.

Mathews also discloses forming a photoresist layer (42) over the dielectric layer (40). Ex. 1004 at FIG. 4; 3:21-29 (photoresist layer 42 formed over insulative dielectric layer 40); Ex. 1003 at ¶ 70. Therefore, *Mathews* discloses claim element [8a];⁹ Ex. 1003 at ¶ 92.

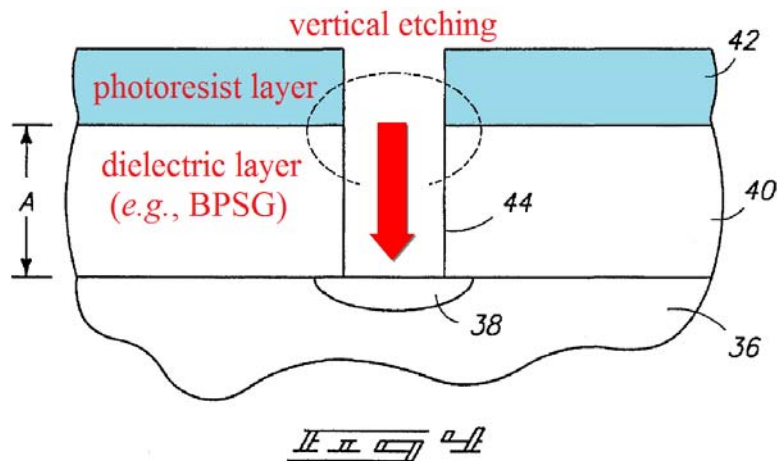
3. Claim Element [8b] – “anisotropically etching portions of the dielectric layer . . .”

Claim element [8b] recites “anisotropically etching portions of the dielectric layer exposed by the resist layer to define an opening in the dielectric layer.”

Ex. 1001 at 8:25-27.

As illustrated in FIG. 4, below, *Mathews* discloses selectively etching the dielectric layer (40) where the photoresist layer (42) is patterned. Ex. 1004 at FIG. 4; 3:26-29 (“[A] layer 42 of photoresist is provided, and then first material layer 40 etched through to form a contact opening 44 for making electrical connection with substrate area 38.”); Ex. 1003 at ¶¶ 70, 93.

⁹ *Mathews* further discloses claim element [8a] at: Ex. 1004 at Abstract; 2:60-63; 3:16-32; 5:1-4; 5:25-26; 6:18-21; FIG. 4.



Mathews (Ex. 1004) at FIG. 4 (Annotated)

In *Mathews*, the dielectric layer (40) is etched in the vertical direction only – a non-uniform etch. Ex. 1004 at FIG. 4; Ex. 1003 at ¶¶ 70, 93. As discussed earlier, vertically etching a via is created by an anisotropic etch. See Section V.F.1; Ex. 1003 at ¶¶ 55-60, 70, 93.

Claims 8 and 11 of the '638 patent both require that vertically etching through the dielectric is the result of an anisotropic etch. Ex. 1001 at Claims 8, 11; Ex. 1003 at ¶ 59. Vertically etching through the dielectric layers are the only disclosed embodiments (Ex. 1001 at FIGS. 4 & 9), which must fall within the claimed “anisotropically etching” step of the claims. Oatey, 514 F.3d at 1277 (Fed.

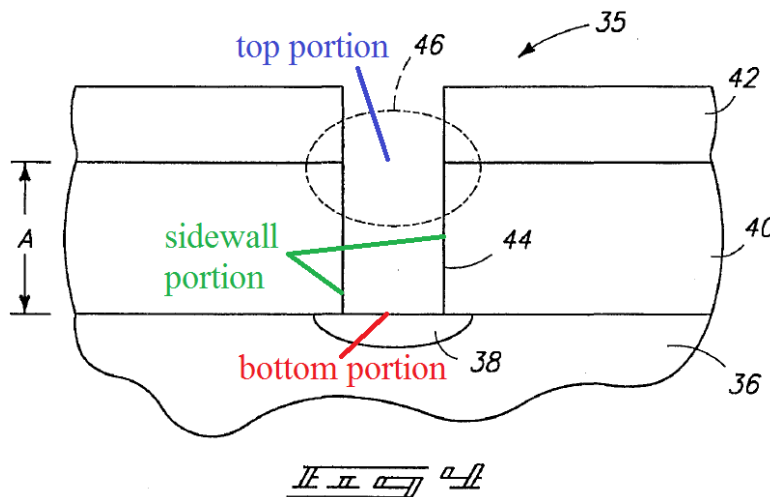
Cir. 2008); Ex. 1003 at ¶ 59. Therefore, *Mathews* discloses claim element [8b].¹⁰

Ex. 1003 at ¶ 93.

4. Claim Element [8c] – “the opening includes . . .”

Claim element [8c] recites “the opening includes a top portion that is adjacent an upper surface of the dielectric layer, a bottom portion that is opposite the top portion, and a sidewall portion that is disposed between the top portion and the bottom portion.” Ex. 1001 at 8:28-32.

As illustrated in FIG. 4, below, *Mathews* discloses (i) a top portion; (ii) a bottom portion; and (iii) a sidewall portion located between the bottom portion and the top portion. Ex. 1004 at FIG. 4; Ex. 1003 at ¶¶ 70, 94.



Ex. 1004 at FIG. 4 (Annotated)

¹⁰ *Mathews* further discloses claim element [8b] at: Ex. 1004 at Abstract; 2:64-67; 3:16-38; 5:5-8; 6:22-25.

Mathews further explains that “contact opening 44 can be considered as having an outermost region, indicated generally by dashed outline 46 [in FIG. 4],” which is adjacent to the upper surface of the dielectric layer (40). Ex. 1004 at 3:29-32. Ex. 1003 at ¶¶ 70, 94. Therefore, *Mathews* discloses claim element [8c].¹¹ Ex. 1003 at ¶ 94.

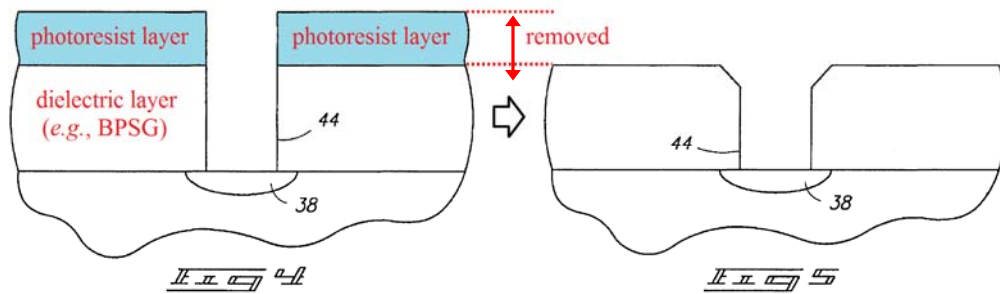
5. Claim Element [8d] – “removing the resist layer”

Claim element [8d] recites “removing the resist layer.” Ex. 1001 at 8:34.

As illustrated in FIGS. 4 and 5, below, *Mathews* discloses removing the photoresist layer (42) after the via (44) is formed. Ex. 1004 at FIGS. 4, 5; 3:39-40 (“Referring to FIG. 5, masking layer 42 is removed after the etching which formed contact opening 44.”). Ex. 1003 at ¶¶ 70, 95. Therefore, *Mathews* discloses claim element [8d].¹² Ex. 1003 at ¶ 95.

¹¹ *Mathews* further discloses claim element [8c] at: Ex. 1004 at Abstract; 3:26-32.

¹² *Mathews* further discloses claim element [8d] at: Ex. 1004 at Abstract; 3:1-2; 3:38-39; 3:43-50; 5:9-10; 6:26-27; FIGS. 4, 5.

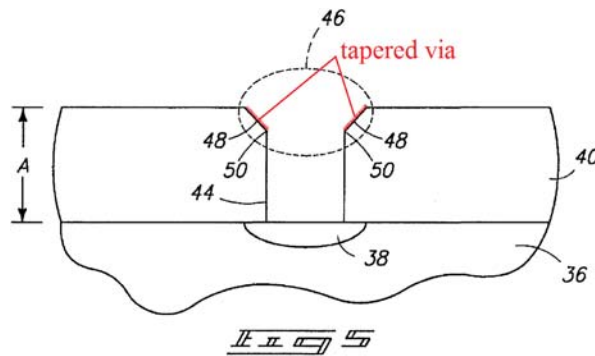


Ex. 1004 at FIGS. 4 and 5 (Annotated)

6. Claim Element [8e] – “tapering the top portion of the opening using an anisotropic etch . . .”

Claim element [8e] recites “tapering the top portion of the opening using an anisotropic etch process after removing of the resist layer.” Ex. 1001 at 8:35-36.

As illustrated in FIG. 5, below, *Mathews* discloses one embodiment in which the outwardly angled sidewalls (48) at the top portion of the via (44). Ex. 1004 at FIG. 5; Ex. 1003 at ¶¶ 71, 96.



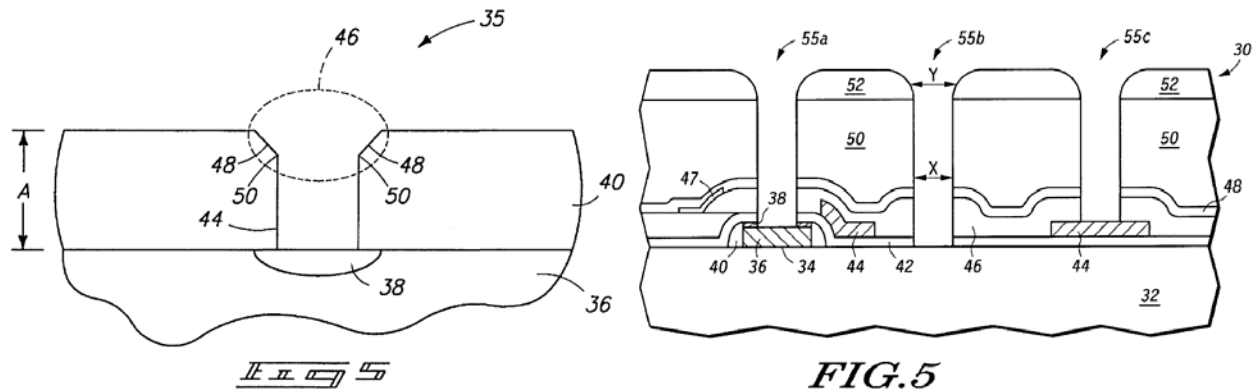
Ex. 1004 at FIG. 5 (Annotated)

The photoresist layer (42) is partially or completely removed before creating the outwardly angled sidewalls. Ex. 1004 at 3:38-60; Ex. 1003 at ¶¶ 71, 118-20.

Mathews further explains that the outwardly angled sidewalls (48) are formed using a “facet sputter etching.” Ex. 1004 at 3:39-43 (“Then, facet sputter etching is conducted into first material layer 40 relative to contact opening 44 to provide outwardly angled sidewalls 48.”). Due to its highly physical nature (as opposed to chemical), sputter etching is highly directional, which, as discussed earlier, is anisotropic. See Section V.F.1; Ex. 1003 at ¶¶ 42-46, 71, 97; Ex. 1008 at p. 63 (“the [sputter etching] method entails directional anisotropy.”); Ex. 1010¹³ at p. 124 (sputter etching is “strongly directional (anisotropic).”).

Furthermore, the outwardly angled sidewalls (48) illustrated in FIG. 5 of *Mathews* are nearly identical to the “golf tee” tapered openings illustrated in FIG. 5 of the ’638 patent. Compare Ex. 1004 at FIG. 5 with Ex. 1001 at FIG. 5; Ex. 1003 at ¶¶ 71, 98, 120-22.

¹³ “Plasma Processing of Materials” (Ex. 1010) is a Governmental report on plasma processing of materials. Upon information and belief, Ex. 1010 was first published on or around February 1985. Ex. 1010 at DD Form 1473 (p. 3). The report indicates that it was approved for public release and distribution. *Id.* Petitioner cites Ex. 1010 merely to describe the state of the relevant technology and the knowledge of a person of ordinary skill in the art on or around the effective filing date of the ’638 patent and not as prior art.



Ex. 1004 at FIG. 5 And '638 patent (Ex. 1001) at FIG. 5

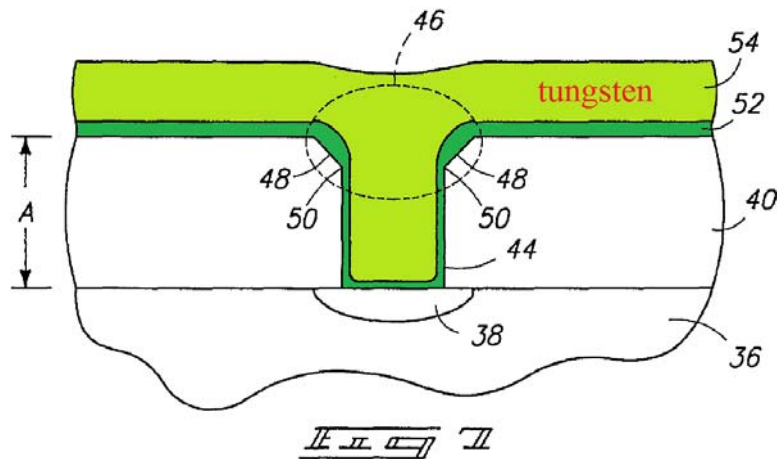
As discussed earlier, a “golf tee” shaped profile is defined by the '638 patent as the result of an anisotropic etch. See Section V.F.1; Ex. 1003 at ¶¶ 71, 98, 120-22. Therefore, *Mathews* discloses claim element [8e].¹⁴ Ex. 1003 at ¶¶ 96-98.

7. Claim Element [8f] – “depositing a material . . .”

Claim element [8f] recites “depositing a material over portions of the upper surface of the dielectric layer and within the opening.” Ex. 1001 at 8:37-38.

As illustrated in FIG. 7, below, *Mathews* discloses depositing one or more layers of conductive material (52, 54) within the via and on the top surface of the dielectric layer (40). Ex. 1004 at FIG. 7; Ex. 1003 at ¶ 99.

¹⁴ *Mathews* further discloses claim element [8e] at: Ex. 1004 at Abstract; 3:39-44; 3:1-8; 3:40-60; 5:11-16; 6:28-33; FIG. 5.



Ex. 1004 at FIG. 7 (Annotated)

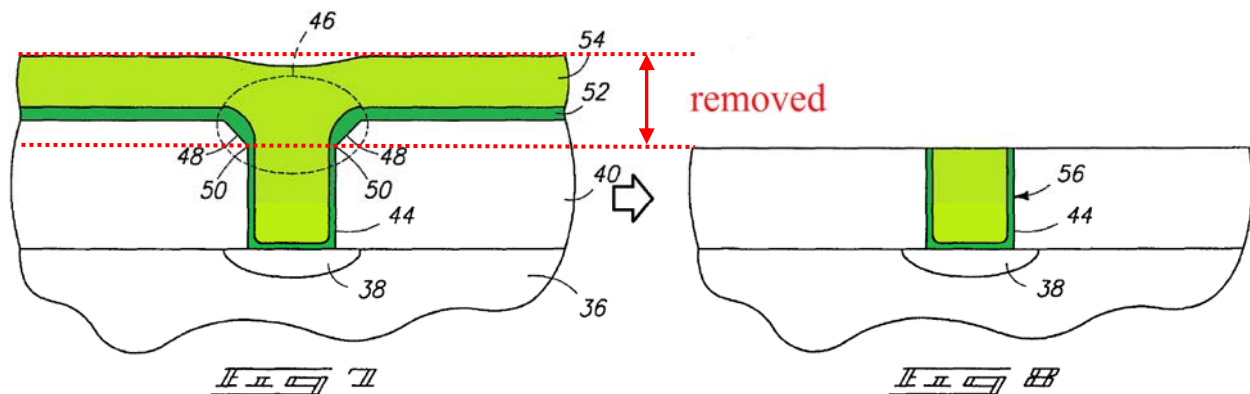
In reference to FIG. 7, *Mathews* states that a thin layer of titanium (52) is deposited within the via and on top of the dielectric layer, followed by a deposition of tungsten (54). Ex. 1004 at 3:60-4:7; Ex. 1003 at ¶ 72. Alternatively, a single layer of metal can be deposited as well. Ex. 1004 at 4:7-10 (Via can “alternately be filled by a single layer deposition.”); Ex. 1003 at ¶ 72. Therefore, *Mathews* discloses claim element [8f].¹⁵ Ex. 1003 at ¶ 99.

¹⁵ *Mathews* further discloses claim element [8f] at: Ex. 1004 at Abstract; 3:9-11; 3:60-4:16; 5:18-20; 6:35-40; FIGS 6, 7.

8. Claim Element [8g] – “polishing to remove . . .”

Claim element [8g] recites “polishing to remove (1) the material over portions of the upper surface of the dielectric layer and (2) the top portion of the opening including the taper and portions of the material contained within the top portion.” Ex. 1001 at 8:40-43.

As illustrated in FIGS. 7 and 8 below, *Mathews* discloses removing the layer of conductive material (52, 54) and the dielectric layer (40) at least down to the point where the outwardly angled sidewalls (48) meet the vertical sidewalls (50). Ex. 1004 at FIGS. 7, 8; 4:17-25; Ex. 1003 at ¶¶ 73, 100.



Ex. 1004 at FIGS. 7 & 8 (Annotated)

The metal layers (52, 54) and the portion of the dielectric layer (40) containing the tapered sidewalls (48) are all removed in this step. Ex. 1004 at FIGS. 7, 8; Ex. 1003 at ¶ 73. *Mathews* further discloses that “[t]he preferred method by which layers 54, 52 and layer 40 are etched is by chemical-mechanical polishing.” Ex.

1004 at 4:33-42; Ex. 1003 at ¶ 73. Therefore, *Mathews* discloses claim element [8g].¹⁶ Ex. 1003 at ¶ 100.

B. Claims 9-10 Are Anticipated By *Mathews*

1. Claim 9 – “. . . wherein the material includes a conductive material”

Claim 9 recites “[t]he method of claim 8, wherein the material includes a conductive material.” Ex. 1001 at 8:44-45. The term “the material” refers to the material that is deposited “over portions of the upper surface of the dielectric layer and within the opening.” Ex. 1001 at 8:38-39; 8:44-45.

Mathews discloses that the material deposited “atop the wafer and [] within facet etched contact opening” is a conductive material, such as titanium or tungsten. Ex. 1004 at 3:60-63 (titanium); 4:1-5 (tungsten); Ex. 1003 at ¶¶ 72, 102. Therefore, *Mathews* discloses Claim 9.¹⁷ Ex. 1003 at ¶ 102.

¹⁶ *Mathews* further discloses claim element [8g] at: Ex. 1004 at Abstract; 1:45-47; 3:23-25; 4:17-50; 5:21-24; 6:41-44; FIGS. 7, 8.

¹⁷ *Mathews* further discloses claim 9 at: Ex. 1004 at Abstract; 1:45-47; 3:23-25; 4:17-50; 5:21-24; 6:41-44; FIGS. 7, 8.

2. Claim 10 – “. . . wherein the conductive material is . . . a tungsten material”

Claim 10 recites “[t]he method of claim 9 wherein the conductive material is further characterized as a tungsten material.” Ex. 1001 at 8:46-47.

Mathews discloses that the preferred material for the conductive layer is tungsten. Ex. 1004 at 4:1-5 (“preferably tungsten.”); Ex. 1003 at ¶¶ 72, 104.

Therefore, *Mathews* discloses claim 10.¹⁸ Ex. 1003 at ¶ 104.

C. Claim 11 Is Anticipated By *Mathews*

Claim 11 substantively recites (Ex. 1001 at 8:48-65):

11. A method for forming an integrated circuit, the method comprising:

[11a] patterning a resist layer over a dielectric layer;

[11b] anisotropically etching portions of the dielectric layer exposed by the resist layer to substantially define

[11c] a top portion . . . , a bottom portion . . . , and a sidewall portion . . . ;

[11d] tapering the top portion of the opening using an anisotropic etch process while removing the resist layer;

[11e] depositing a material over portions of the upper surface of the dielectric layer and within the opening; and

¹⁸ *Mathews* further discloses claim 10 at: Ex. 1004 at 1:12-45; 1:59-2:6; 2:7-14; 4:1-5; 4:17-25; 4:33-42; 6:8-10; FIGS. 6, 7.

[11f] polishing to remove the material over portions of the upper surface of the dielectric layer and the top portion of the opening including the taper and portions of the material contained within the top portion.

Claim 11 differs from claim 8 in one substantive respect. Whereas claim 8 recites “tapering the top portion of the opening . . . *after* removing of the resist layer” (Ex. 1001 at 8:35-36 (Claim Element [8e]) (emphasis added)), claim 11 recites “tapering the top portion of the opening . . . *while* removing the resist layer” (Ex 1001 at 8:57-58 (Claim Element [11d]) (emphasis added)). Hence, for all other elements of claim 11, Petitioner incorporates herein by reference the arguments set forth in Section VII.A.¹⁹

¹⁹ Claim elements [11b] and [11c], while not identical to claim elements [8b] and [8c], respectively, they are the same in scope. The corresponding discussion regarding elements of claim 8 apply to the claim 11 elements as follows:

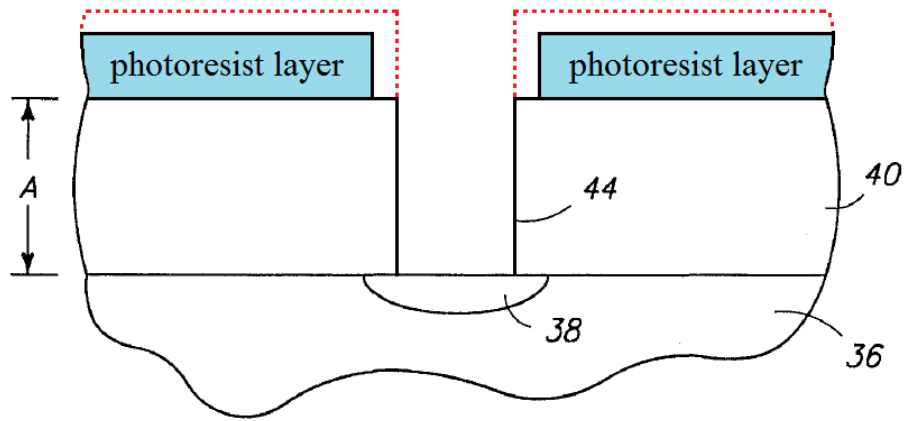
- For Claim 11, preamble: See Section VII.A.1 (Claim 8, preamble)
- For claim element [11a]: See Section VII.A.2 (Claim element [8a])
- For claim element [11b]: See Section VII.A.3 (Claim element [8b])
- For claim element [11c]: See Section VII.A.4 (Claim element [8c])
- For claim element [11e]: See Section VII.A.7 (Claim element [8f])
- For claim element [11f]: See Section VII.A.8 (Claim element [8g])

1. Claim Element [11d]

Claim element [11d] recites “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” Ex. 1001 at 8:57-58.

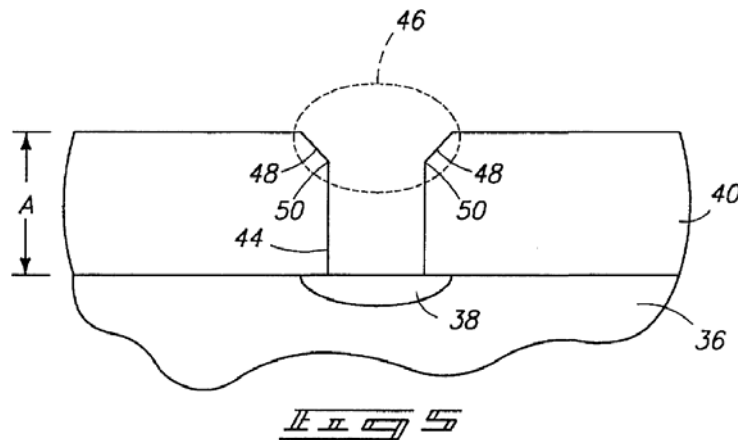
As discussed above, *Mathews* discloses “removing the resist layer.” See Section VII.A.5; Ex. 1003 at ¶¶ 71, 93. *Mathews* discloses removing the photoresist layer before forming outwardly angled sidewalls at the top portion of the via. Ex. 1004 at 3:38-43; Ex. 1003 at ¶¶ 71, 93. *Mathews* discloses that the photoresist removal step may strip only party of the photoresist, particularly the photoresist near the via opening. Ex. 1004 at 3:47-49 (“The desired effect is to move the resist back away from the contact, and not to necessarily fully strip the resist.”); Ex. 1003 at ¶¶ 71, 110. However, some photoresist remains after this step, as shown in the edited figure below.²⁰ Ex. 1003 at ¶¶ 71, 110.

²⁰ The figure is an exemplary illustration of a wafer with a partially removed photoresist layer.



Partial Photoresist Removal According To Mathews

In a subsequent step, *Mathews* discloses “facet sputter etching” to form outwardly angled sidewalls at the top portion of the vias, the result of which is illustrated in FIG. 5. Ex. 1004 at 3:40-44; FIG. 5; Ex. 1003 at ¶¶ 71, 110-12.



Ex. 1004 at FIG. 5

This results in “tapering the top portion of the opening [due to] an anisotropic etch process.” See Section VII.A.6; Ex. 1001 at 8:35-36 (Claim Element [8e]); Ex. 1003 at ¶¶ 71, 110-12.

The “facet sputter etching” step also simultaneously removes some or all of the remaining photoresist, as illustrated in FIG. 5 of *Mathews*. Ex. 1003 at ¶¶ 71, 110-12; Ex. 1004 at FIG. 5 (showing no photoresist remaining after the facet sputter etch). Because sputter etching is a non-selective physical process, it etches different materials at significantly the same rates. Ex. 1003 at ¶¶ 43-45, 111; Ex. 1008 at p. 63 (“Physical etching is inherently material nonselective because the ion energy required to eject material is large compared to differences in chemical bond energy and chemical reactivity.”); Ex. 1010 at p. 124 (“Most importantly, [sputter etching] is not very selective. Because it is a strictly physical process, the etch rates for different materials do not differ by much.”); Ex. 1003 at ¶¶ 45, 111. This means that sputter etching will remove any material the sputter ions collide with, including the remaining photoresist layer, which was well-known and well-documented. See e.g., Ex. 1008 at p. 63 (“As sputter etching is nonselective, it introduces a masking problem.”); id at p. 64 (*detailing how sputter etching can erode the photoresist*); id at p. 65 (“It should be noted, though, that some of the disadvantages of physical etching, such as resist corner faceting, can sometimes be exploited.”). Thus, the (facet) sputter etching *necessarily* removes the photoresist layer as well as the exposed dielectric layer while the taper is being formed. Ex. 1003 at ¶¶ 45-46, 112. Therefore, *Mathews* discloses “tapering the top portion of the opening using an anisotropic etch process *while* removing the resist layer,” as

recited in claim element [11d].²¹ Ex. 1001 at 8:57-58 (emphasis added); Ex. 1003 at ¶¶ 110-12.

VIII. Claims 8-11 Are Obvious Over *Mathews*

A. Claims 8-10 Are Obvious Over *Mathews*

As explained above, *Mathews* discloses each and every element of Claims 8-10. See Sections VII.A, VII.B. To the extent, however, the PTAB determines that *Mathews* does not anticipate Claims 8-10, *Mathews* nevertheless renders Claims 8-10 obvious because they would have been obvious to a skilled artisan in light of *Mathews*. Ex. 1003 at ¶¶ 113-15.

B. Claim 11 Is Obvious Over *Mathews*

As explained above, *Mathews* discloses each and every element of Claim 11, including claim element [11d] (“tapering the top portion of the opening using an anisotropic etch process *while* removing the resist layer.”). Ex. 1001 at 8:57-58 (emphasis added); see Section VII.C; Ex. 1003 at ¶¶ 105-12. To the extent, however, the PTAB determines that *Mathews* does not anticipate Claim 11, *Mathews* nevertheless renders Claim 11 obvious because claim element [11d] would have been obvious to a skilled artisan in light of *Mathews*. Ex. 1003 at ¶¶

²¹ *Mathews* further discloses claim element [11d] at: Ex. 1004 at Abstract; 3:38-49; 3:59-61; 4:1-5; 4:17-25; 4:33-42; FIGS. 4-5; Sections VII.A.5 & 6.

117-23.

1. Claim Element [11d] – “tapering the top portion of the opening . . .”

Claim element [11d] recites “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” Ex. 1001 at 8:57-58.

It would have been obvious to a skilled artisan that leaving a portion of the photoresist on the dielectric layer to be sacrificially etched during the facet sputter etching step would be advantageous. Ex. 1003 at ¶ 120. As discussed earlier, *Mathews* discloses: (1) an anisotropic tapering etch (Section VII.C.1; Ex. 1003 at ¶¶ 71, 97-98); (2) complete or partial removal of the photoresist during the tapering etch (Section VII.C.1; Ex. 1004 at 3:44-50; Ex. 1003 at ¶¶ 71, 95, 110-12); and (3) that the non-selective tapering (sputter etch) removes any remaining photoresist (See Section VII.C.1; Ex. 1003 at ¶¶ 45, 71, 110-12).

Additionally, sputter etching is a slow process requiring significant energy. Ex. 1003 at ¶¶ 43, 121. If the photoresist were completely removed prior to the facet etch, it would take longer to obtain the same amount of tapering since the flat portions of the dielectric would be receding at the same time the edges are being tapered. Ex. 1003 at ¶ 121. Another inherent property of sputter etching is its tendency to form facets or rounded corners at the edges of a layer due to the physical nature of the etch. Ex. 1003 at ¶¶ 46, 97-98. Thus, exposing the edges

would permit the tapering of the via faster since the flat portions of the dielectric are not etched until the remaining photoresist is removed completely. Ex. 1003 at ¶ 121.

Therefore, it would have been obvious for a person of ordinary skill in the art to not remove the photoresist layer completely prior to the sputter etching process, and instead retain portions of the photoresist layer and remove them simultaneously during the facet sputter etching step. Ex. 1003 at ¶¶ 118-22. Therefore, *Mathews* renders claim element [11d] obvious.

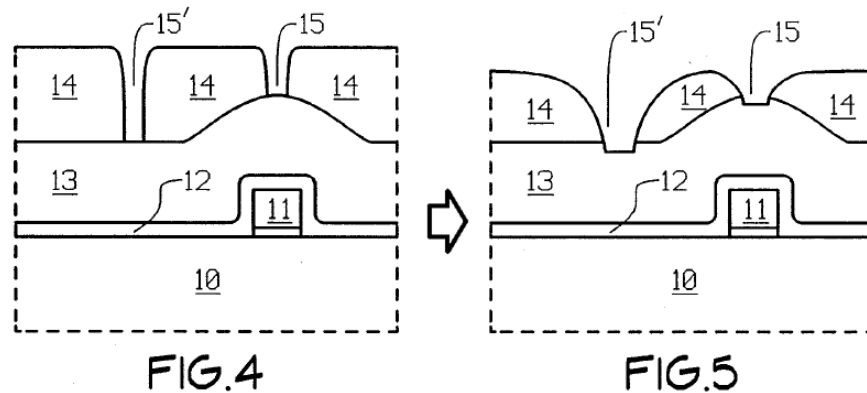
IX. Claims 1-7 And 11 Are Obvious Over *Mathews* In View Of *Langley*

A. Claim 11 Is Obvious Over *Mathews* In View Of *Langley*

As discussed earlier, Claim 11 is anticipated by or rendered obvious by *Mathews*. See Sections VII.C, VIII.B. To the extent, however, the PTAB determines that *Mathews* does not anticipate or render obvious Claim 11, it is nevertheless obvious over *Mathews* in view of *Langley* because *Langley* further discloses “tapering the top portion of the opening . . . while removing the resist layer.” Ex. 1001 at 8:57-58 (Claim Element [11d]); Ex. 1003 at ¶¶ 124-33.

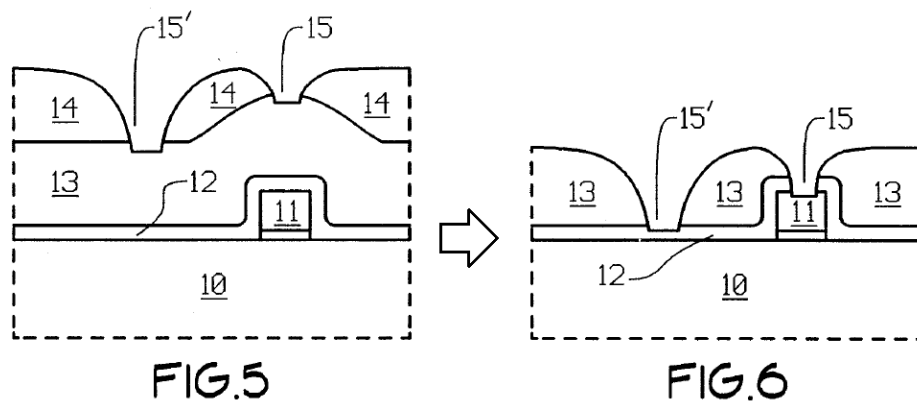
As illustrated in FIGS. 4 and 5 below, *Langley* discloses partially etching a patterned photoresist layer (14) to form a slope on the photoresist layer (14). Ex. 1005 at 3:36-38 (“In the first step, a chamber atmosphere of O₂, He, CHF₃, and CF₄ is provided, widening, or forming slopes in, contacts 15 and 15’ by eroding

resist 14.”); 2:27-29 (“A first etch step is performed, which slopes the resist and begins etching exposed oxide.”); *id.* at FIGS. 4, 5; Ex. 1003 at ¶ 129.



Ex. 1005 at FIGS. 4 & 5: Showing Partial Photoresist Etch

As illustrated in FIGS. 5 and 6 below, *Langley* further discloses subsequently transferring the slope from the photoresist layer (14) to the dielectric layer (13) by further etching away the photoresist layer (14) and the dielectric layer (13) simultaneously. Ex. 1005 at FIGS. 5, 6; 3:48-52 (“After the proper contact slope is obtained, a second etch is performed . . . in order to etch oxides 13 and 12 and remaining resist 14 at a 1:1 etch rate ratio.”). Ex. 1003 at ¶ 129.



Ex. 1005 at FIGS. 5 & 6: Showing Photoresist/Dielectric Etch

The result of this second etching step is a dielectric layer (13) with a tapered top portion, as illustrated in FIG. 6, with all the photoresist removed. Ex. 1005 at FIG. 6; Ex. 1003 at ¶ 129. Therefore, *Langley* discloses tapering the top portion of the opening . . . while removing the resist layer,” as recited in claim element [11d].²² Ex. 1001 at 8:57-58; Ex. 1003 at ¶ 129.

Moreover the resulting slope on the dielectric layer (13) has a “golf tee” profile and is substantially identical to the “golf tee” profile disclosed in the ’638 patent. Compare Ex. 1005 at FIG. 6 with Ex. 1001 at FIG. 5 (see below); Ex. 1003 at ¶¶ 130-33. As discussed earlier, a “golf tee” profile is created by an anisotropic etch. See Section V.F.1; Ex. 1003 at ¶¶ 130-33.

²² *Langley* further discloses claim element [11d] at: Ex. 1005 at Abstract; 1:51-2:5; 2:25-46; 3:48-61; 4:60-65; 6:17-21; FIGS. 5, 6.

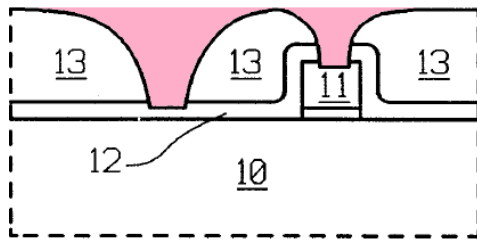


FIG. 6

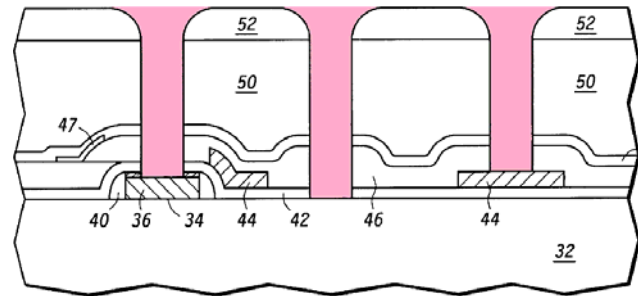


FIG. 5

Ex. 1005 at FIG. 6 and Ex. 1001 at FIG. 5 (Annotated)

Furthermore, as discussed earlier, a skilled artisan would have been motivated to combine the specific teachings of *Langley* (i.e., simultaneously etching the dielectric and the photoresist) with *Mathews*. See Section VI.B.2; Ex. 1003 at ¶¶ 125-27. Therefore, *Mathews* in view of *Langley* renders claim element [11d] obvious. Ex. 1003 at ¶¶ 128-33.

B. Claim 1 Is Obvious Over *Mathews* In View Of *Langley*

1. Preamble

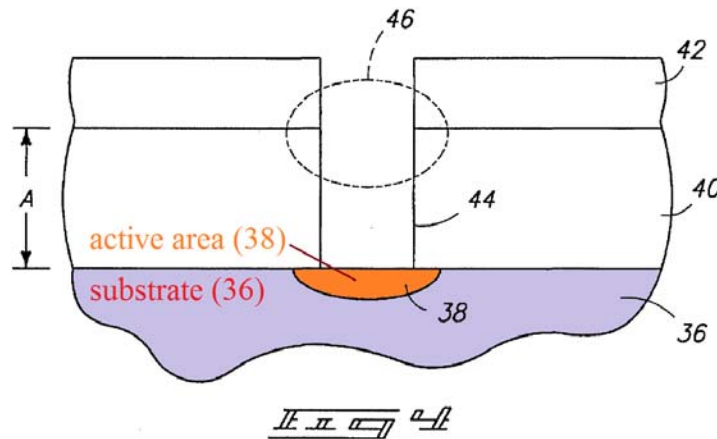
The preamble of Claim 1 recites “[a] method for forming a contact structure.” Ex. 1001 at 7:33. *Mathews* discloses “a method for forming a contact structure” in a semiconductor circuit. Ex. 1004 at Abstract; 1:7-9 (same). Therefore, *Mathews* discloses the preamble of Claim 1.²³ Ex. 1003 at ¶¶ 136.

²³ *Mathews* further discloses the preamble at: Ex. 1004 at Abstract; 1:7-9; FIGS. 4-9; and *passim*.

2. **Claim Element [1a] – “forming a first conductive material . . .”**

Claim element [1a] recites “forming a first conductive material overlying a semiconductor substrate.” Ex. 1001 at 7:35-36.

As illustrated in FIG. 4 below, *Mathews* discloses forming a bulk substrate (36) and an active area (38) to which electrical connection is to be made. Ex. 1004 at FIG. 4; 3:19-21 (“Such comprises a bulk substrate 36 and active area 38 to which electrical connection is to be made.”); Ex. 1003 at ¶ 137.



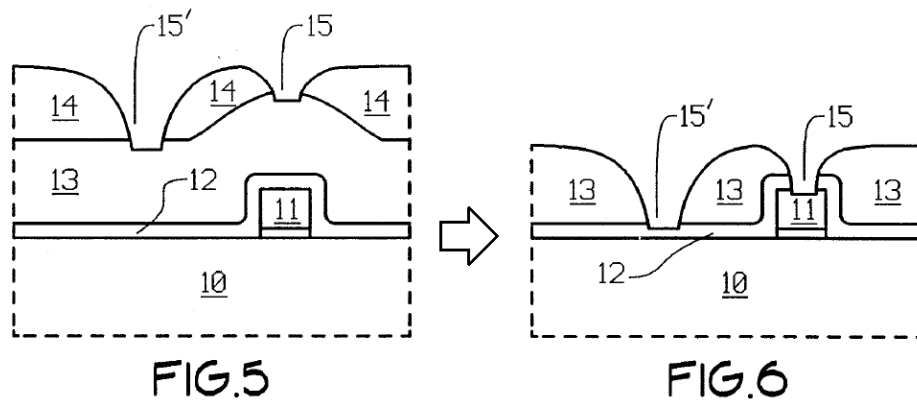
Ex. 1004 at FIG. 4 (Annotated)

As further illustrated in FIG. 4, an active area (38), such as a doped source/drain region, is formed within the top surface of the bulk substrate (36). Ex. 1004 3:19-21 (“[Wafer] comprises a bulk substrate 36 and active area 38 to which electrical connection is to be made.”); *id.* at FIG. 4; *id.* at 1:18-21 (FIGS. 1 and 2 depict prior art “[b]ulk substrate 12 [that] includes a dopant diffusion/active region 16 to which electrical connection is to be made.”); *id.* at FIGS. 1 & 2; Ex. 1003 at ¶¶ 137.

Claim 7 of the '638 patent recites “forming the first conductive layer as a doped current electrode for a transistor within a substrate . . .” Ex. 1001 at 8:18-21. As discussed above, “a doped current electrode” can be the source or drain region, which are doped diffusions formed within the substrate. Ex. 1003 at ¶ 137. Claim 7 is dependent on Claim 1, which means Claim 1 encompasses Claim 7. Hence, the term “overlying a semiconductor substrate” recited in Claim 1 includes being “within a substrate” as recited in Claim 7. Ex. 1001 at 7:35-36, 8:18-21; Ex. 1003 at ¶ 138. Accordingly, the active area (38) in FIG. 4 of *Mathews* overlies (“overlying”) the bulk substrate (36). Ex. 1003 at ¶ 138. Therefore, *Mathews* discloses “forming a first conductive material overlying a semiconductor substrate,” as recited in claim element [1a].²⁴ Ex. 1001 at 7:35-36; Ex. 1003 at ¶¶ 137-38.

Langley also discloses claim element [1a]. *Langley* discloses forming conductive material in the form of polysilicon (11), on which via contacts (15) are formed, overlying a semiconductor substrate, as shown below. Ex. 1004 at 3:4-13; FIGS. 5-6; Ex. 1003 at ¶ 139.

²⁴ *Mathews* further discloses claim element [1a] at: Ex. 1004 at Abstract; 2:57-58; 3:16-21; 4:66-67; 6:15-16.



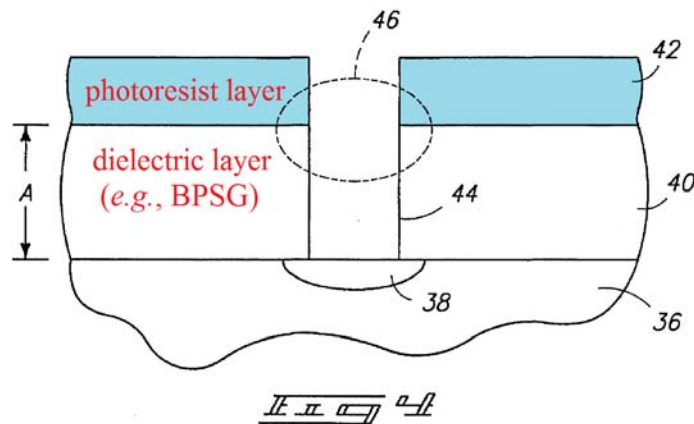
Ex. 1005 at FIGS. 5 & 6: Showing Photoresist/Dielectric Etch

A skilled artisan would have been motivated to consider *Mathews* and *Langley* together. See Section VI.B.2; Ex. 1003 at ¶ 140. Furthermore, with respect to claim element [1a], different parts of a device are used as examples in *Mathews* (*i.e.*, drain and source) and *Langley* (*i.e.*, gate) to show how a via can be fabricated. Ex. 1003 at ¶ 140. Thus, it would have been obvious to a person of ordinary skill in the art that the methods disclosed in *Mathews* and *Langley* are easily applied to all parts of a device. Ex. 1003 at ¶ 140. Therefore, *Mathews* in light of *Langley* renders obvious claim element [1a]. Ex. 1003 at ¶ 140.

3. Claim Element [1b] – “forming a dielectric layer . . .”

Claim element [1b] recites “forming a dielectric layer overlying the first conductive layer.” Ex. 1001 at 7:37-38. As illustrated in FIG. 4 below, *Mathews* discloses forming a dielectric layer (40) using insulative materials, such as BPSG, over the bulk substrate (36) and the active area (38). Ex. 1004 at 2:19-24;

Ex. 1003 at ¶ 136.



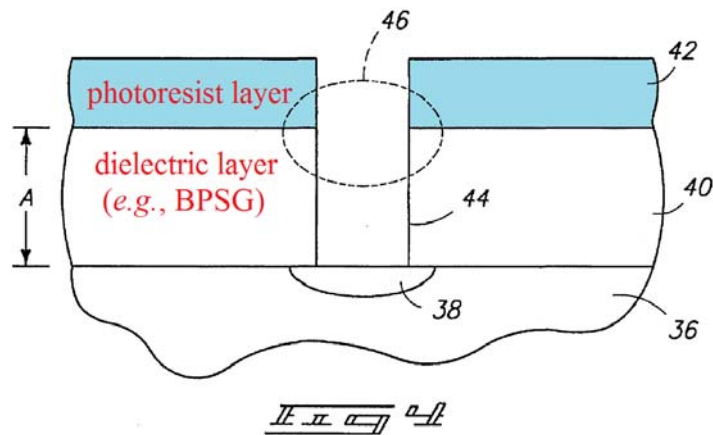
Ex. 1004 at FIG. 4 (Annotated)

Therefore, *Mathews* discloses claim element [1b].²⁵ Ex. 1003 at ¶ 136.

4. Claim Element [1c] – “forming a resist layer . . .”

Claim element [1c] recites “forming a resist layer over the dielectric layer.” Ex. 1001 at 7:39. As discussed in Section VII.A.2, *Mathews* discloses forming and patterning a photoresist layer (14) for forming a desired via. Ex. 1004 at FIG. 4; 3:25-27 (“Layer 40 is patterned/masked for formation of a desired contact opening therethrough. Specifically and preferably, a layer 42 of photoresist is provided . . .”). Ex. 1003 at ¶ 136.

²⁵ *Mathews* further discloses claim element [1b] at: Ex. 1004 at Abstract; 2:59-60; 3:21-24; 5:1-2; 6:18-19; FIG. 4.



Ex. 1004 at FIG. 4 (Annotated)

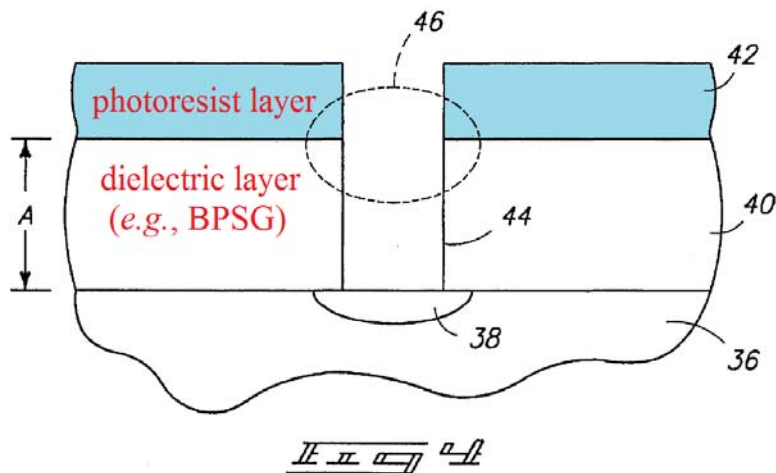
Therefore, *Mathews* discloses claim element [1c].²⁶ Ex. 1003 at ¶ 136.

5. Claim Element [1d] – “patterning the resist . . .”

Claim element [1d] recites “patterning the resist layer to form an opening that exposes portions of the dielectric layer.” Ex. 1001 at 7:40-41.

As discussed in Section VII.A.2, *Mathews* discloses forming and patterning a photoresist layer (14) for forming a desired via. Ex. 1004 at FIG. 4; 3:25-27 (“Layer 40 is patterned/masked for formation of a desired contact opening therethrough. Specifically and preferably, a layer 42 of photoresist is provided . . .”); Ex. 1003 at ¶ 136.

²⁶ *Mathews* further discloses claim element [1c] at: Ex. 1004 at Abstract; 2:60-63; 3:16-32; 5:3-4; 5:25-26; 6:20-21; FIG. 4.



Ex. 1004 at FIG. 4 (Annotated)

Therefore, *Mathews* discloses claim element [1d].²⁷ Ex. 1003 at ¶ 136.

6. Claim Element [1e] – “placing the semiconductor substrate into a reactive ion etching chamber . . .”

Claim element [1e] recites “placing the semiconductor substrate into a reactive ion etching chamber and in-situ processing the semiconductor substrate.”

Ex. 1001 at 7:43-45.

Mathews discloses placing the wafer in a plasma etch chamber and performing all etching steps in the same chamber. Ex. 1003 at ¶ 141; Ex. 1004 at 3:55-57 (“The above processes (mask removal and all etching) are all preferably

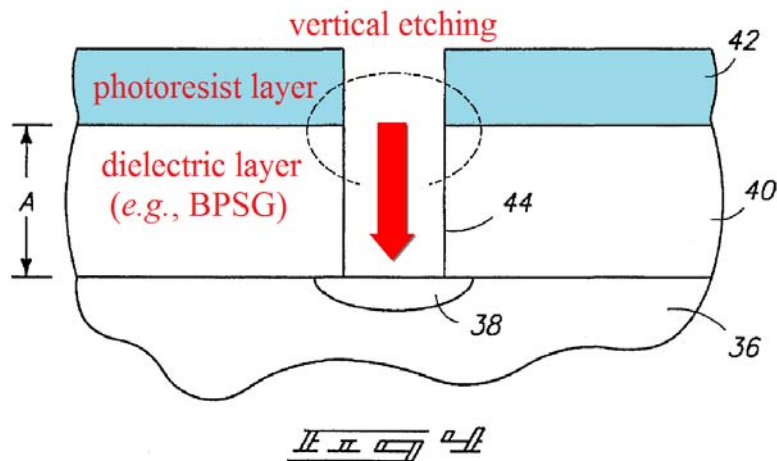
²⁷ *Mathews* further discloses claim element [1d] at: Ex. 1004 at Abstract; 2:60-63; 3:16-32; 5:3-4; 5:25-26; 6:20-21; FIG. 4.

conducted in the same chamber.”). The chamber can be a reactive chamber. Ex. 1003 at ¶ 142; Ex. 1004 at 3:44-46 (“An example facet etching technique to produce sidewalls 48 includes first etching a contact in conventional reactive or non-reactive manner.”). Therefore, *Mathews* discloses “placing the semiconductor substrate into a reactive ion etching chamber and in-situ processing the semiconductor substrate,” as recited in claim element [1e]. Ex. 1001 at 7:43-45; Ex. 1003 at ¶ 141.

Langley also discloses claim element [1e]. Ex. 1003 at ¶ 143. *Langley* states that “[t]he preferred method includes four timed etch steps in a single Lam 790 parallel plate plasma etch reactor . . .” Ex. 1003 at ¶ 143; Ex. 1005 at 3:27-30. This further demonstrates that the etching and photoresist removal steps in *Mathews* and in *Langley* are compatible with the other and interchangeable. Ex. 1003 at ¶ 143.

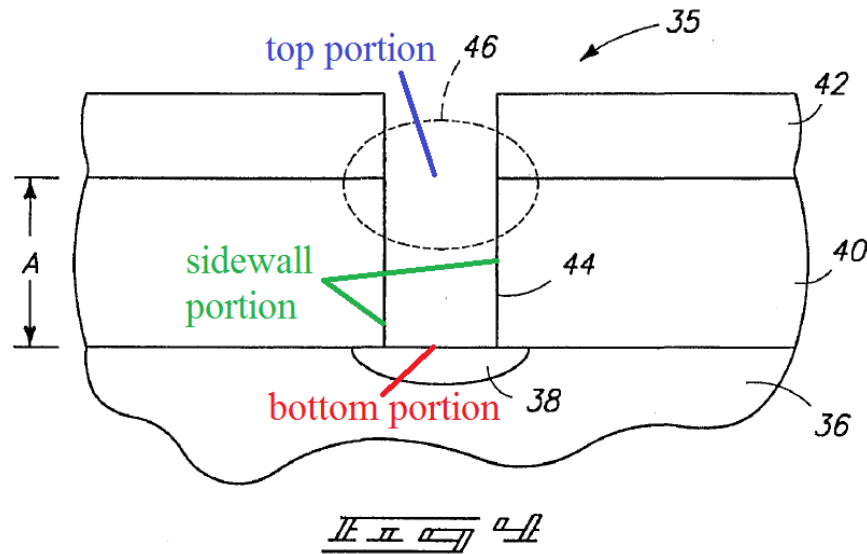
7. Claim Element [1f] – “etching portions of the dielectric layer . . .”

Claim element [1f] recites “etching portions of the dielectric layer using a gas mixture that includes a fluorocarbon source gas to form an opening in the dielectric layer, the opening having a bottom portion and a sidewall portion.” Ex. 1001 at 7:46-49.



Ex. 1004 at FIG. 4 (Annotated)

As illustrated in FIG. 4 above, *Mathews* discloses etching the dielectric layer (42) to form a via (44) that extends down to the substrate (36) and the active region (38). Ex. 1004 at FIG. 4; 3:26-29 (“[A] layer 42 of photoresist is provided, and then first material layer 40 etched through to form a contact opening 44 for making electrical connection with substrate area 38.”). Ex. 1003 at ¶ 145. *Mathews* further discloses that the via is etched using a mixture of CF_4 , CHF_3 and Ar. Ex. 1004 at 3:33-35 (“An example etch of the BPSG oxide to form contact 44 would be a dry etch using a carbon/fluorene based chemistry, e.g., CF_4 , CHF_3 , and Ar.”). Ex. 1003 at ¶ 145. Both CF_4 and CHF_3 contain carbon and fluorine and thus are fluorocarbon compounds. Ex. 1003 at ¶ 145.



Ex. 1004 at FIG. 4 (Annotated)

As further illustrated in FIG. 4 above, *Mathews* discloses a bottom portion, and a sidewall portion. Ex. 1004 at FIG. 4; Ex. 1003 at ¶ 145. Therefore, *Mathews* discloses claim element [1f].²⁸ Ex. 1003 at ¶ 145.

8. Claim Element [1g] – “etching a portion of the resist layer . . .”

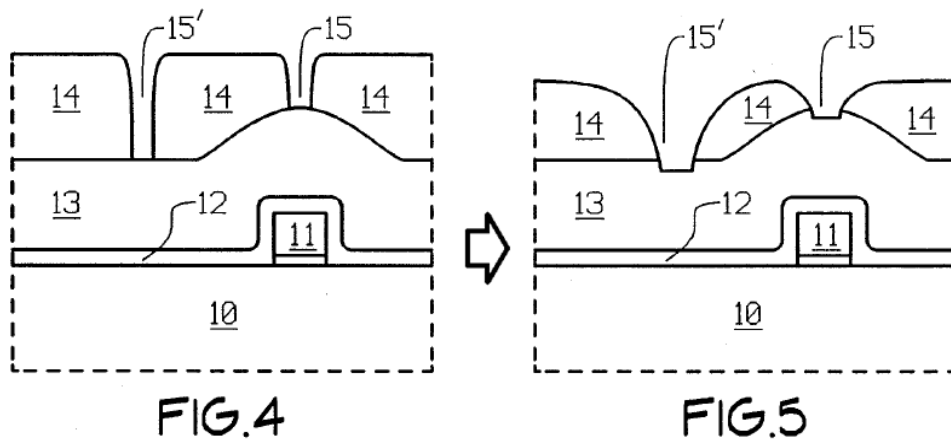
Claim element [1g] recites “etching a portion of the resist layer using a gas mixture that includes a fluorocarbon source gas and an oxygen source gas to remove the portion of the resist layer and expose a top surface portion of the dielectric layer adjacent the sidewall portion.” Ex. 1001 at 7:50-54.

²⁸ *Mathews* further discloses claim element [1f] at: Abstract; 2:64-67; 3:16-38; 5:6-9; 6:22-25; FIG. 4.

Mathews discloses removing the photoresist layer using an oxygen-based etch. Ex. 1004 at 3:46-48 (“Then, an oxygen etch is conducted to strip the resist and pull it away from the edge of the contact.”); Ex. 1003 at ¶ 144. *Mathews* states that the goal is to remove the portion of the photoresist layer adjacent to the via and not to remove the entire layer. Ex. 1004 at 3:48-50 (“The desired effect is to move the resist back away from the contact, and not to necessarily fully strip the resist.”); Ex. 1003 at ¶¶ 71, 119-22. Furthermore, it would have been obvious for a skilled artisan to etch the photoresist layer without completely evacuating the fluorocarbon gas that was used in the previous step (of vertically etching the vias). Ex. 1003 at ¶ 148.

To the extent the PTAB determines that *Mathews* does not expressly disclose “using a gas mixture that includes a fluorocarbon source gas and an oxygen source gas to remove the portion of the resist layer,” *Langley* nevertheless discloses claim element [1g]. Ex. 1001 at 7:50-54; Ex. 1003 at ¶¶ 146-47. As illustrated in FIGS. 4 and 5 of *Langley* below, *Langley* discloses etching a portion of the photoresist layer in “a chamber atmosphere of O₂, He, CHF₃, and CF₄.” Ex. 1005 at 3:36-38 (“In the first step, a chamber atmosphere of O₂, He, CHF₃, and CF₄ is provided, widening, or forming slopes in, contacts 15 and 15’ by eroding resist 14.”); Ex. 1003 at ¶ 146. As further illustrated in FIG. 5 of *Langley*, the surface of a portion of the dielectric layer (13) is exposed where the photoresist

layer (14) is etched back. Ex. 1003 at ¶¶ 76, 129; Ex. 1005 at FIG. 5. Therefore, *Langley* discloses “etching a portion of the resist layer using a gas mixture that includes a fluorocarbon source gas and an oxygen source gas to remove the portion of the resist layer and expose a top surface portion of the dielectric layer adjacent the sidewall portion,” as recited in claim element [1g].²⁹ Ex. 1001 at 7:50-54; Ex. 1003 at ¶ 141.



Ex. 1005 at FIGS. 4 & 5

A skilled artisan would have been motivated to combine the specific teachings of *Langley* (*i.e.*, using a mixture of oxygen and fluorocarbon gas to etch the photoresist layer) with *Mathews*. Ex. 1003 at ¶¶ 147-48. The environment for etching or removing the various layers disclosed in *Mathews* is remarkably similar

²⁹ *Langley* further discloses claim element [1g] at: Ex. 1005 at Abstract; 2:25-46; 3:36-47; 4:54-59; 6:11-16; FIGS. 4, 5.

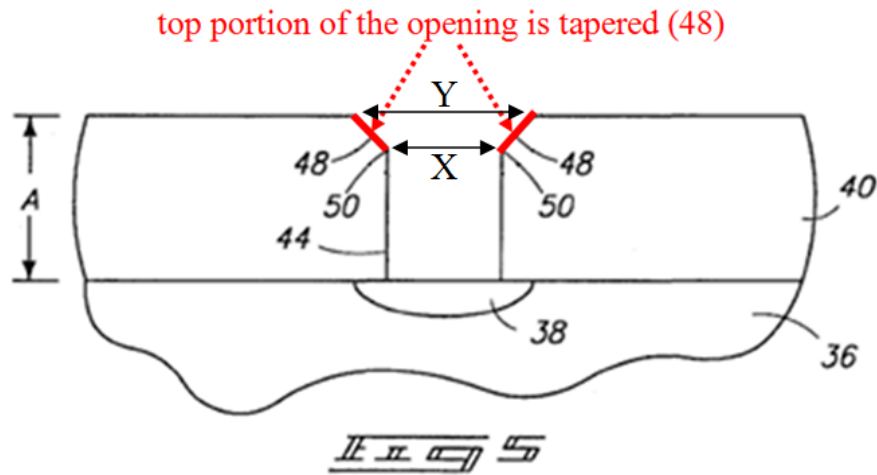
to that of *Langley*. Ex. 1003 at ¶¶ 142-43. For instance, both *Langley* and *Mathews* propose performing all etch and photoresist removal steps in a single plasma chamber. Ex. 1003 at ¶ 144; Ex. 1004 at 3:55-57; Ex. 1005 at 3:27-35. Both *Langley* and *Mathews* propose using CHF_3 and CF_4 as the main plasma ingredients for vertically etching the vias. Ex. 1003 at 142-43; Ex. 1004 at 3:33-37; Ex. 1005 at 3:48-61. Both *Langley* and *Mathews* propose using oxygen (O_2) as one of the plasma ingredients for etching the photoresist layer. Ex. 1003 at ¶¶ 110, 146; Ex. 1004 at 3:45-47, 3:50-51; Ex. 1005 at 3:36-47. Because of the significant overlap in the process environment, it would have been a simple substitution for a person practicing the invention of *Mathews* to use a mixture of CHF_3 , CF_4 , and O_2 (as taught in *Langley*) during the photoresist removal step instead of using just O_2 as *Mathews* suggests. Ex. 1003 at ¶ 148.

As discussed earlier, *Mathews* and *Langley* are directed to the same field of forming vias in integrated circuits. See Section VI.B.2; Ex. 1003 at ¶¶ 50, 69, 127; Ex. 1004 at 1:6-8; Ex. 1005 at 1:6-10. *Mathews* and *Langley* both propose widening the top portion of the vias as a solution. See Section VI.B.2; Ex. 1003 at ¶¶ 51, 72, 127; Ex. 1004 at 2:53-3:15; Ex. 1004 at 2:25-46. When CMP process began to replace conventional, conformal process, process designers often took etching technology for conformal process, such as the four etch steps disclosed in *Langley*, and combined them to CMP process, such as the CMP disclosed in

Mathews. Ex. 1003 at ¶ 126. Therefore, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Langley* (i.e., etching techniques) with *Mathews*. Ex. 1003 at ¶¶ 125-27.

9. Claim Element [1h] – “etching the top surface portion of the dielectric layer . . .”

Claim element [1h] recites “etching the top surface portion of the dielectric layer adjacent the sidewall portion to form a taper that extends between a top surface of the dielectric layer and the sidewall portion, wherein the taper towards the top surface portion has a radius Y and the taper towards the sidewall portion has a radius X wherein $X < Y$.”³⁰ Ex. 1001 at 7:55-61.



Ex. 1004 at FIG. 5 (Annotated)

³⁰ See Ex. 1001 at 4:20-24 and FIG. 5 for an explanation of the X and Y radii.

As discussed in Section VII.A.6, *Mathews* discloses (anisotropically) etching the top surface of the dielectric layer to form an outwardly angled walls, or tapered openings, in the dielectric layer. Ex. 1004 at 3:40-44, 3:57-60, FIG. 5; Ex. 1003 at ¶¶ 96-98. FIG. 5 of *Mathews* above further illustrates that the radius of the via at the top of the dielectric layer (48) is greater than the radius of the via at the bottom of the dielectric layer (50)—*i.e.*, $X < Y$. Ex. 1004 at FIG. 5; Ex. 1003 at ¶ 96. Therefore, *Mathews* discloses claim element [1h].³¹ Ex. 1001 at 7:55-61; Ex. 1003 at ¶¶ 96, 136.

10. Claim Element [1i] – “removing remaining portions of the resist layer”

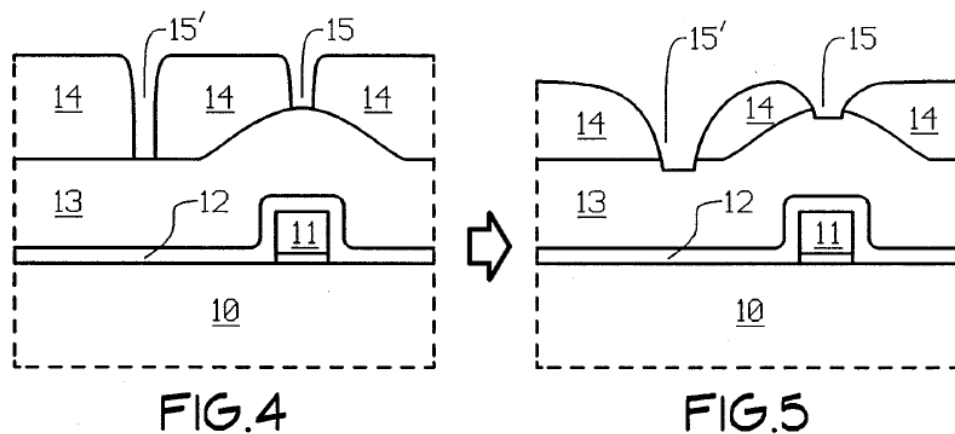
Claim element [1i] recites “removing remaining portions of the resist layer.” Ex. 1001 at 7:62.

As discussed earlier, *Mathews* either discloses or renders obvious removing the remaining portions of the resist layer during the facet sputter etching step. See Sections VII.C.1, VIII.B.1; Ex. 1003 at ¶¶ 71, 110-13.

To the extent, however, the PTAB determines that *Mathews* does not disclose or render obvious claim element [1i], *Langley* nevertheless discloses

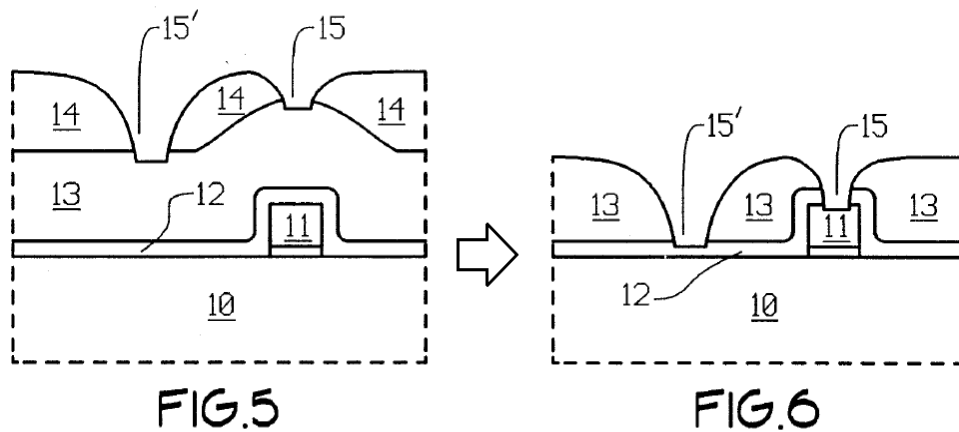
³¹ *Mathews* further discloses claim element [1h] at disclosures: Ex. 1004 at Abstract; 3:39-44; 3:3-8; 3:40-60; 5:11-16; 6:28-33; FIG. 5.

performing such a second photoresist removal step. Ex. 1003 at ¶¶ 129-33. As illustrated in FIGS. 4 and 5 of *Langley* below, *Langley* discloses removing only a portion of the photoresist layer. Ex. 1005 at FIG. 5; 3:36-38 (“In the first step, a chamber atmosphere of O₂, He, CHF₃, and CF₄ is provided, widening, or forming slopes in, contacts 15 and 15’ by eroding resist 14.”). Ex. 1003 at ¶¶ 129-33.



Ex. 1005 at FIGS. 4 & 5: Showing Partial Photoresist Removal

Then in the next step, as illustrated in FIGS. 5 and 6 of *Langley* below, the remaining photoresist layer (14) is removed and the slope is transferred from the photoresist layer (14) to the dielectric layer (15). Ex. 1005 at FIGS. 5, 6; 3:48-52 (“After the proper contact slope is obtained, a second etch is performed, the chamber atmosphere including about 140 sccm He, 15 sccm CHF₃, and 125 sccm CF₄, in order to etch oxides 13 and 12 and remaining resist 14 at a 1:1 etch rate ratio.”). Ex. 1003 at ¶¶ 129-33.



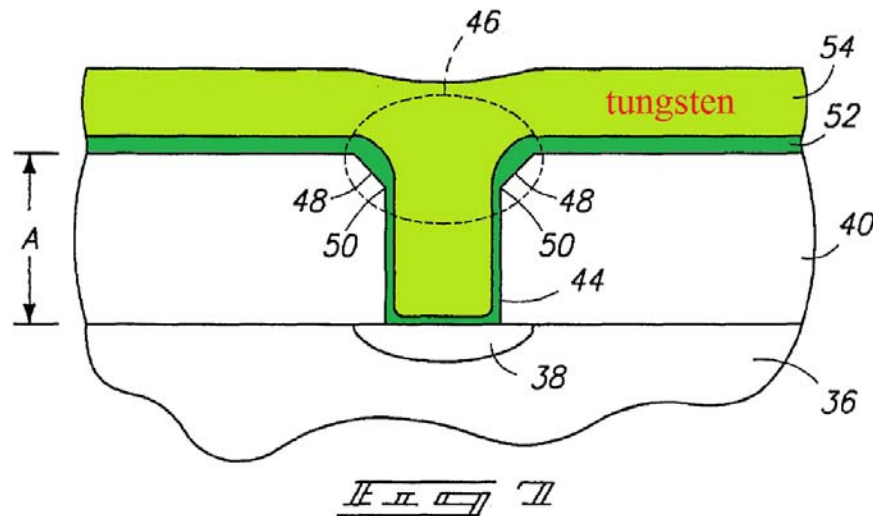
Ex. 1005 at FIGS. 5 & 6: Showing Removal Of Remaining Photoresist

Therefore, *Langley* discloses “removing remaining portions of the resist layer,” as recited in claim element [1i].³² Ex. 1001 at 7:62; Ex. 1003 at ¶¶ 129-33, 135.

11. Claim Element [1j] – “depositing a second conductive material . . .”

Claim element [1j] recites “depositing a second conductive material within the opening.” Ex. 1001 at 7:63-64.

³² *Langley* further discloses claim element [1i] at disclosures: Ex. 1005 at Abstract; 1:51-2:5; 2:25-46; 3:48-61; 4:60-65; 6:17-21; FIGS. 5, 6.



Ex. 1004 at FIG. 7 (Annotated)

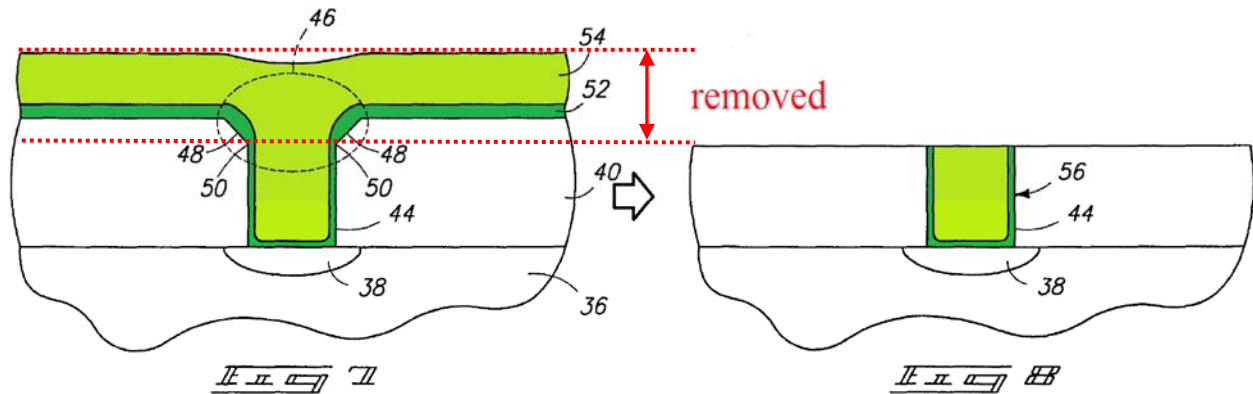
As discussed in Section VII.A.7 (claim element [8f]), *Mathews* discloses depositing one or more layers of conductive material (52, 54) such as titanium or tungsten on the surface of the dielectric (40) and within the vias (44). Ex. 1004 at FIG. 7; 3:61-67, 4:1-7; Ex. 1003 at ¶¶ 72, 99, 136. Therefore, *Mathews* discloses “depositing a second conductive material within the opening,” as recited in claim element [1j].³³ Ex. 1001 at 7:63-64.

12. Claim Element [1k] – “polishing away . . .”

Claim element [1k] recites “polishing away a top portion of the conductive material and a top portion of the dielectric layer to remove the taper.” Ex. 1001 at

³³ *Mathews* further discloses claim element [1j] at: Ex. 1004 at Abstract; 3:9-11; 3:60-4:16; 5:18-20; 6:35-40; FIGS. 6, 7.

7:65-67.



Ex. 1004 at FIGS. 7, 8: Chemical-Mechanical Polishing

As discussed in Section VII.A.8 (claim element [8g]), *Mathews* discloses removing, by chemical-mechanical polishing, the conductive material and the dielectric layer until the tapered portion of the opening is removed and the minimum radius of the contact opening is restored. Ex. 1004 at FIG. 8; 4:17-25, 4:33-42; Ex. 1003 at ¶¶ 73, 100, 136. Therefore, *Mathews* discloses claim element [1k].³⁴ Ex. 1003 at ¶¶ 100, 136.

C. Claims 2-4 Are Obvious Over *Mathews* In View Of *Langley*

1. Claim 2 – “wherein the second conductive material comprises tungsten”

Claim 2 recites “[t]he method of claim 1, wherein the second conductive

³⁴ *Mathews* further discloses claim element [1k] at: Ex. 1004 at Abstract; 1:45-47; 3:23-25; 4:17-50; 5:21-24; 6:41-44; FIGS. 7, 8.

material comprises tungsten.” Ex. 1001 at 8:1-2. Claim 2 recites substantially the same language as Claim 10.

As discussed in Section VII.B.2 (Claim 10), *Mathews* discloses that one of the preferred materials for the conductive layer is tungsten. Ex. 1004 at 4:1-5 (“preferably tungsten”). Ex. 1003 at ¶¶ 72, 103-04. Therefore, *Mathews* discloses Claim 2.³⁵ Ex. 1003 at ¶¶ 103-04, 149.

2. Claim 3 – “wherein removing remaining portions of the resist layer . . .”

Claim 3 recites “[t]he method of claim 1, wherein removing remaining portions of the resist layer is performed as part of in situ-processing in the reactive ion etching chamber.” Ex. 1001 at 8:3-5.

As discussed in Section IX.B.6 regarding claim element [1e], *Mathews* discloses performing all etching and mask removal steps in the same chamber. Ex. 1003 at ¶¶ 141-42, 150; Ex. 1004 at 3:55-57 (“The above processes [i.e. in-situ] (mask removal and all etching) are all preferably conducted in the same chamber.”). Therefore, *Mathews* discloses Claim 3. Ex. 1003 at ¶¶ 142, 150.

Langley also discloses that “[t]he preferred method includes four timed etch

³⁵ *Mathews* further discloses Claim 2 at: Ex. 1004 at 1:12-45; 1:59-2:6; 2:7-14; 4:1-5; 4:17-25; 4:33-42; 6:8-10; FIGS. 6, 7.

steps in a single Lam 790 parallel plate plasma etch reactor . . .” Ex. 1005 at 3:27-28; Ex. 1003 at ¶¶ 143-44. Therefore, both *Mathews* and *Langley* individually disclose and in combination render obvious Claim 3. Ex. 1003 at ¶¶ 143-44. This further demonstrates that the etching and photoresist removal steps disclosed in *Mathews* and *Langley* are compatible with the other and interchangeable. Ex. 1003 at ¶¶ 141-44.

3. Claim 4 – “using the top portion of the opening . . .”

Claim 4 recites “[t]he method of claim 1 further comprising using the top portion of the opening having the radius Y to reduce void formation in the contact structure due to the step of depositing.” Ex. 1001 at 8:6-9.

Mathews discloses that the tapering step is performed to avoid cusp formation in the vias. Ex. 1004 at 4:10-16 (“Regardless, angled sidewalls 48 facilitate elimination of cusp formation. Contact opening 44 as patterned can be designed with the minimum photolithographic feature size at its base such that wafer or real estate widening only occurs at the outermost portion or region 46. Accordingly, circuit density can still be maximized while cusp formation is minimized.”). Ex. 1003 at ¶¶ 69, 151. Therefore, *Mathews* discloses Claim 4.³⁶

³⁶ *Mathews* further discloses Claim 4 at disclosures: Ex. 1004 at 1:37-45; 1:59-2:6; 3:59-4:32; FIGS. 1-3, 7, 8.

Ex. 1003 at ¶ 151.

D. Claims 5-7 Are Obvious Over *Mathews* In View Of *Langley*

Claims 5-7 are directed to applying Claim 1 to various portions of an SRAM cell, that is forming a via over various elements of an SRAM transistor. As discussed below, it would have been obvious for a person of ordinary skill in the art to apply the inventions disclosed in *Mathews* and *Langley* to an SRAM cell. Ex. 1003 at ¶¶ 152-63.

Claims 5 through 7 respectively recite forming a void-free via over: (1) a gate electrode of an SRAM transistor (Claim 5); (2) a polysilicon layer coupled to an SRAM storage node (Claim 6); and (3) a doped current electrode of an SRAM transistor (Claim 7). It was well known to a skilled artisan that an SRAM cell comprises multiple MOS transistors. Ex. 1003 at ¶¶ 62-65, 152-53. Further, it was well known to a skilled artisan that a MOS transistor has a drain, a source, and a gate electrode (Ex. 1003 at ¶¶ 62-65, 81-82, 152-53); that the gate electrode is generally made from polysilicon (Ex. 1003 at ¶¶ 62-65, 81, 154, 157; Ex. 1009 at pp. 113-15); that the source and drain electrodes are doped (Ex. 1003 at ¶¶ 81-82, 153; Ex. 1009 at p. 115, Fig. 3.4(d)); and that the various electrodes are electrically connected to vias (Ex. 1003 at ¶¶ 82, 153-54; Ex. 1009 at Plates 1 and 8). Put differently, Claims 5-7 simply recite characteristics of SRAM cells that were well-known at the time of the alleged invention.

Furthermore, Claims 5-7 do not recite any elements that are particularly suited for or targeted at SRAM cells. In fact, the '638 patent admits that the process disclosed in claim 1 is as applicable to SRAMs as other types of devices. Ex. 1001 at 6:27-32 (“It is important to note that this contact process may also be used in microprocessors, other memory devices (i.e., EEPROM, EPROM, DRAM, ferroelectric devices, flash memories, etc.) or any semiconductor device fabrication process using plug contacts.”); Ex. 1003 at ¶ 154.

In light of the foregoing, Claims 5-7 are obvious over *Mathews* in view of *Langley*. Ex. 1003 at ¶¶ 153-63.

X. Claims 1-7 Are Obvious Over *Mathews* In View Of *Langley* And *Wuu*

A. Claims 1-4 Are Obvious Over *Mathews* In View Of *Langley* And *Wuu*

1. Claim 1

Claim 1 is obvious over *Mathews* in view of *Langley* and *Wuu* for the same reasons as discussed in Section IX.B.

2. Claim 2

As discussed in Section IX.C.1, *Mathews* discloses Claim 2. See also Ex. 1003 at ¶¶ 147, 169. Therefore, Claim 2 is obvious over *Mathews* in view of *Langley* and *Wuu*.

3. Claim 3

As discussed in Section IX.C.2, *Mathews* discloses Claim 3. See also Ex. 1003 at ¶¶ 148, 169. Therefore, Claim 3 is obvious over *Mathews* in view of *Langley* and *Wuu*.

4. Claim 4

As discussed in Section IX.C.3, *Mathews* discloses Claim 4. See also Ex. 1003 at ¶¶ 149, 169. Therefore, Claim 4 is obvious over *Mathews* in view of *Langley* and *Wuu*.

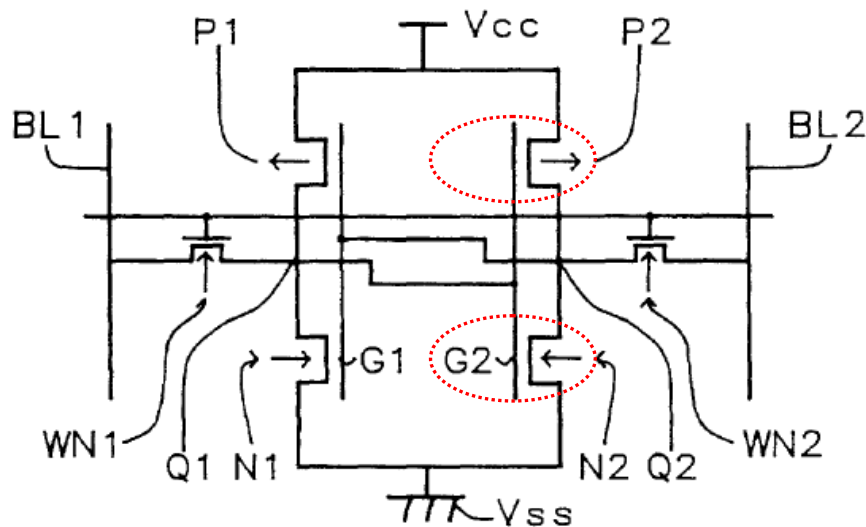
B. Claims 5-7 Are Obvious Over *Mathews* In View Of *Langley* And *Wuu*

As discussed earlier, dependent Claims 5-7 are obvious over *Mathews* in view of *Langley*. See Section IX.D. To the extent, however, the PTAB determines that Claims 5-7 are not obvious over *Mathews* in view of *Langley*, Claims 5-7 are nevertheless obvious over *Mathews* in view of *Langley* and *Wuu* because *Wuu* discloses Claims 5-7 and because skilled artisans would have been motivated to combine the specific teachings of *Mathews* and *Langley* with *Wuu*. See VI.C.2; Ex. 1003 at ¶¶ 64-68.

1. Claim 5 – “. . . forming the first conductive layer as a gate electrode . . .”

Claim 5 recites “[t]he method of claim 1, wherein the step of forming the first conductive layer comprises forming the first conductive layer as a gate

electrode which gates a transistor in an SRAM cell.” Ex. 1001 at 8:10-13.



Ex. 1006 at FIG. 1 (Annotated)

FIG. 1 of *Wuu* (above), which is a circuit diagram of a six-transistor SRAM cell, shows the gate electrode (G2) of storage transistors P2 and N2. Ex. 1006 at FIG. 1; Ex. 1003 at ¶ 171.

FIG. 9 of *Wuu* (below), which is a cross sectional diagram of the same six-transistor SRAM cell, further shows the gate electrode (G2) being buried underneath a dielectric layer (16, 22) and in contact with a contact plug (24). Ex. 1006 at FIG. 9, 3:65-67. Therefore, *Wuu* discloses

“forming the first conductive layer as a gate electrode which gates a transistor in an SRAM cell,” as recited in Claim 5.³⁷ Ex. 1001 at 8:10-13.

³⁷ *Wuu* further discloses claim 5 at at disclosures: Ex. 1006 at Abstract; 2:5-28; 4:58-5:27; 7:24-36; 7:62-67; FIGS. 1, 7-9.

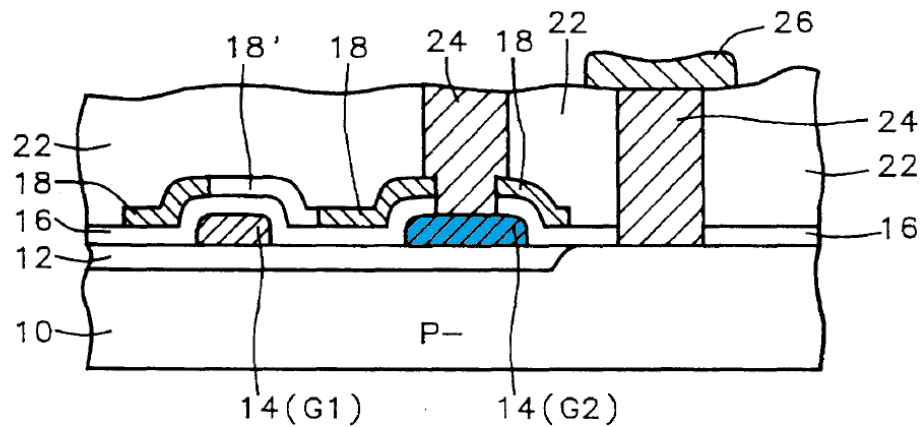


FIG. 9

Ex. 1006 at FIG. 9 (Annotated)

Furthermore, as discussed above, a skilled artisan would have been motivated to combine the specific teachings of *Mathews* and *Langley* with *Wuu* to solve the problem of keyhole formation in vias. See Section VI.C.2; Ex. 1003 at ¶¶ 165-67. Therefore, Claim 5 is obvious over *Mathews* in view of *Langley* and *Wuu*.

2. Claim 6 – “. . . forming a poly-silicon layer which is coupled to a storage node of an SRAM cell”

Claim 6 recites “[t]he method of claim 1, wherein forming the first conductive layer is further characterized as forming a poly-silicon layer which is coupled to a storage node of an SRAM cell.” Ex. 1001 at 8:14-17.

As discussed above, gate electrode (G2) corresponds to “the first conductive layer.” *Wuu* also discloses that the gate electrode (G2) is “patterned from an N⁺ doped third polysilicon layer 14.” Ex. 1006 at 2:5-7, 5:4-8, FIG. 1; Ex. 1003 at

¶ 175. Furthermore, FIG. 1 of *Wuu* further illustrates that the transistors P1, P2, N1, N2 form the latch or the storage portion of an SRAM cell with their drain and gate electrodes coupled to the nodes Q1 and Q2. Ex. 1006 at FIG. 1. As discussed earlier, nodes Q1 and Q2 are “storage nodes of an SRAM cell.” See Section V.F.2; Ex. 1003 at ¶¶ 165-67. Therefore, *Wuu* discloses the gate electrode (G2), which is “a polysilicon layer which is coupled to a storage node of an SRAM cell,” as recited in Claim 6.³⁸ Ex. 1001 at 8:14-17.

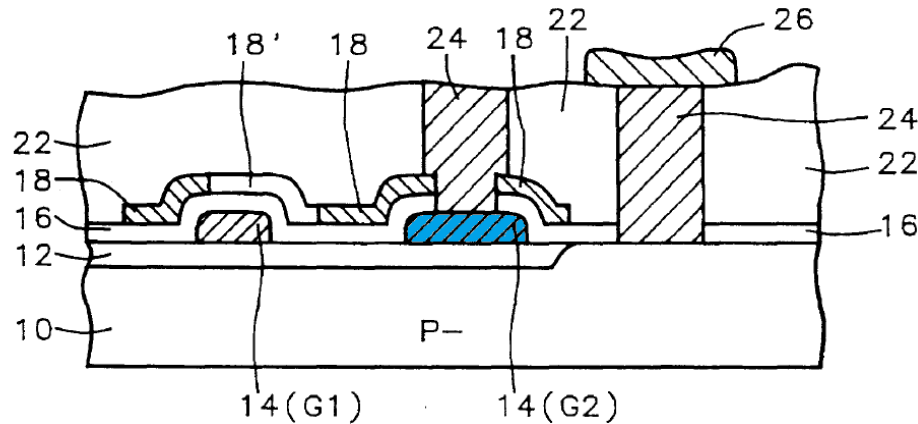


FIG. 9

Ex. 1006 at FIG. 9 (Annotated)

Furthermore, as discussed above, a skilled artisan would have been motivated to combine the specific teachings of *Mathews* and *Langley* with *Wuu* to

³⁸ *Wuu* further discloses claim 6 at at disclosures: Ex. 1006 at Abstract; 2:5-28; 4:58-5:27; 7:24-36; 7:62-67; FIGS. 1, 7-9.

solve the problem of keyhole formation in vias. See Section VI.C.2; Ex. 1003 at ¶¶ 165-67. Therefore, Claim 6 is obvious over *Mathews* in view of *Langley* and *Wuu*.

3. **Claim 7 – “. . . forming the first conductive layer as a doped current electrode . . .”**

Claim 7 recites “[t]he method of claim 1, wherein the step of forming the first conductive layer comprises forming the first conductive layer as a doped current electrode for a transistor within a substrate, the transistor being coupled in an SRAM cell.” Ex. 1001 at 8:18-21.

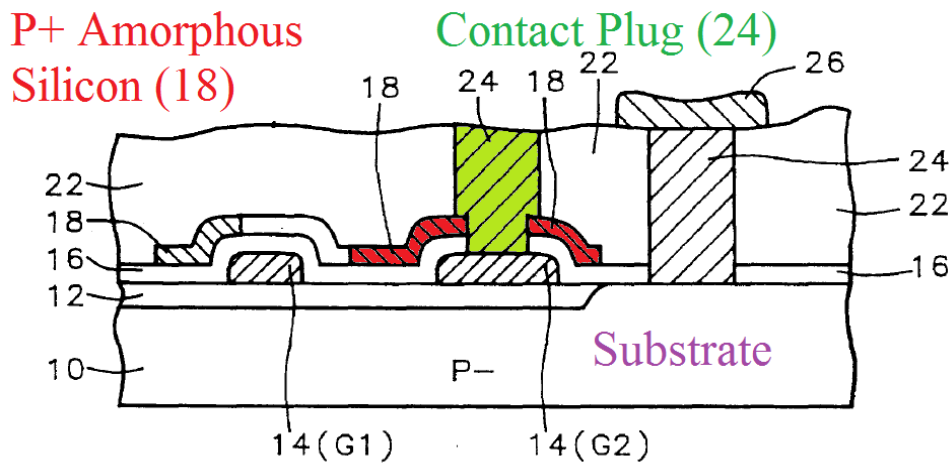


FIG. 9

Ex. 1006 at FIG. 9 (Annotated)

FIG. 9 of *Wuu* shows a silicon layer (18) which is buried underneath a dielectric layer (24) and is in contact with a contact plug (24). Ex. 1006 at FIG. 9. Therefore, the amorphous silicon layer (18) is a “first conductive layer.”

As discussed above, a “current electrode” includes the drain and the source. See Section V.F.3; Ex. 1003 at ¶ 67. *Wuu* states that “[t]he amorphous silicon layer 18 is [] subjected to an ion implantation using a P type dopant, for example, using a boron11 (B¹¹).” Ex. 1006 at 6:3-6; Ex. 1003 at ¶ 180. *Wuu* further states that “[t]his ion implant forms the source/drain doped regions of the P-channel TFTs, and also provide a conducting layer elsewhere on the substrate.” Ex. 1006 at 6:6-8; Ex. 1003 at ¶ 180. Therefore, the amorphous silicon layer (18) is a “conductive layer [which is] a doped current electrode for a transistor . . . coupled in an SRAM cell,” as recited in Claim 7. Ex. 1001 at 8:18-21.

Furthermore, as discussed above, a skilled artisan would have been motivated to combine the specific teachings of *Mathews* and *Langley* with *Wuu* to solve the problem of keyhole formation in vias. See Section VI.C.2; Ex. 1003 at ¶¶ 165-67. Therefore, Claim 7 is obvious over *Mathews* in view of *Langley* and *Wuu*.

XI. Conclusion

The prior art references Petitioner identified in this Petition contain pertinent technological teachings (explicitly or inherently disclosed or otherwise obvious to a person of ordinary skill in the art) that were not previously considered in the manner presented herein or applied during original examination of the ’638 patent.

These references and the arguments Petitioner set forth in this Petition establish a reasonable likelihood that Petitioner will prevail with respect to Claims 1-11 of the '638 patent. Petitioner therefore respectfully requests that the Patent Office institute *inter partes* review of Claims 1-11 of the '638 patent.

Dated: May 6, 2016

Respectfully Submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,372,638, including all Exhibits, has been served on May 6, 2016 by Federal Express on the patent owner at the following correspondence address of record:

North Star Innovations, Inc.
600 Anton Blvd., Suite 1350
Costa Mesa, CA 92626

I further certify that a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,372,638, including all Exhibits, has been served on May 6, 2016 by email on the counsel of record for the patent owner at the following address:

IP LAW LEADERS PLLC
7529 Standish Place, Ste. 103
Rockville, MD 20855

Dated: May 6, 2016

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