

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the *Inter Partes* Review of U.S. Patent No. 6,372,638

Trial No.: Not Yet Assigned

Issued: April 16, 2002

Filed: June 22, 2000

Inventors: Robert A. Rodriguez *et al.*

Assignee: North Star Innovations, Inc.

Title: Method For Forming A Conductive Plug Between Conductive
Layers Of An Integrated Circuit

DECLARATION OF MARTIN WALKER, PH.D. UNDER 38 C.F.R. § 42.100

I, Dr. Martin G. Walker, hereby declare as follows:

1. I am making this declaration at the request of Nanya Technology Corp. (“Nanya”) in the matter of the *Inter Partes* Review of U.S. Patent No. 6,372,638 (“the ’638 patent”).

2. I have been asked to provide my opinion as to whether Claims 1-11 of the ’638 patent are anticipated or would have been obvious to a person of ordinary skill in the art at the time of the alleged invention in view of the prior art.

3. I am being compensated for my work in this matter at my standard hourly rate of \$ 550 for consulting services. My compensation in no way depends on the outcome of this proceeding.

4. In preparing this Declaration, I considered the following materials:

Exhibit No.	Title & Description
1001	U.S. Patent No. 6,372,638 to Rodriguez <i>et al.</i>
1002	Prosecution History of U.S. Patent No. 6,372,638
1004	U.S. Patent No. 5,580,821 to Mathews <i>et al.</i> (“Mathews”)
1005	U.S. Patent No. 4,939,105 to Langley (“Langley”)
1006	U.S. Patent No. 5,547,892 to Wu <i>et al.</i> (“Wu”)
1007	Excerpts from McGraw-Hill Electronics Dictionary, 6th Ed. (McGraw-Hill, 1997)
1008	Excerpts from Madou, “Fundamentals of Microfabrication” (CRC Press, 1997)
1009	Excerpts from Weste <i>et al.</i> , “Principles of CMOS VLSI Design” (Addison Wesley Longman, 1993)
1010	Excerpts from National Materials Advisory Board, “Plasma Processing of Materials” (National Academy Press, 1985)
1011	Excerpts from Webster’s Third New International Dictionary (1993)
1012	U.S. Patent No. 5,327,002 to Motoyoshi (“Motoyoshi”)
1013	U.S. Patent No. 5,488,579 to Sharma <i>et al.</i> (“Sharma”)

Exhibit No.	Title & Description
1014	Excerpts from Sharma, “Semiconductor Memories: Technology, Testing, and Reliability” (Wiley, 1997)
1015	U.S. Patent No. 5,801,094 to Yew <i>et al.</i> (“Yew”)

I. PROFESSIONAL BACKGROUND

A. Educational Background

5. I received my Bachelors of Science degree in Electrical Engineering from the Massachusetts Institute of Technology in 1973. I then received my Masters of Science and Doctor of Philosophy degrees in Electrical Engineering in 1976 and 1979 from Stanford University.

B. Career History

6. I have over 35 years of experience in the design of integrated circuits (“ICs”), including analog, digital, and RF/microwave circuits.

7. I began my professional career designing ICs in 1973. I designed high speed integrated circuits for microwave applications. I received a national award related to the design on integrated circuits in 1976. Beginning in 1981, I developed computer software to aid in the development of integrated circuits. I worked with multiple IC designs and designers using the software products my

company developed. I continued to work in the IC design industry through Jan 2000. Thus, I have more than 25 years of experience in the design industry.

8. During my experience in this field, I worked on the technology at issue relating to the '638 patent. I have personally designed and fabricated integrated circuits beginning in my undergraduate days at MIT. Later in my career, I founded Frequency Technology, whose products focused on the detailed analysis of the electrical interconnect structures of integrated circuits of the type described in the '638 patent. I am named as an inventor on three U.S. patents in this field. At the time of the filing of the application which I understand led to the '638 patent (*i.e.*, February 1997) I was the Chief Scientist at Frequency Technology, and thus directly involved in integrated circuit technology for fabricating interconnects, including the vias (or contacts) described in the specification of the '638 patent.

9. At the time of the invention of the patents at issue, I exceeded the requirements for one of ordinary skill in the art. (See Section III, ¶¶ 20-22).

10. My career in consulting on technology issues in general and litigation in particular began in 2001. Since that time I have been engaged in more than 35 projects in the field of IC design. Many of these projects have involved the design of interconnect structures of memory and logic circuits of the type described in the '638 patent.

C. Publications

11. I have written over fifty articles in the fields of circuit design and design automation, including technical papers in peer-reviewed journals, an invited article in the IEEE Spectrum, and various conference proceedings. I have organized seminars, which were designed to enhance the technical credibility of my companies, and written numerous opinion pieces published in journals such as the EE Times that served to establish and promote our corporate position. Some of my publications are listed in my CV attached as Appendix A.

II. RELEVANT LEGAL STANDARDS

12. I am an engineer by training and profession. The opinions I am expressing in this report involve the application of my engineering knowledge and experience to the evaluation of certain prior art with respect to the '638 patent. My knowledge of patent law is no different than that of any lay person. Therefore, I have requested the attorneys from Sidley Austin LLP, who represent Nanya, to provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patent validity to my analysis.

13. I understand that the terms of the '638 patent are to be construed according to their ordinary and customary meaning as would be understood by a person of ordinary skill in the art at the time of the invention in light of the

language of the claims, the specification, and the prosecution history of record.

For the purposes of this review, I have construed each claim term in accordance with this standard.

14. I have been asked to provide my opinions regarding whether the claims of the '638 patent would have been obvious to a person having ordinary skill in the art at the time of the alleged invention.

15. I have been informed and understand that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time of the presumed invention. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time of the presumed invention.

16. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time of the presumed invention;
- the scope and content of the prior art; and

- what differences, if any, existed between the claimed invention and the prior art.

17. I have been informed and understand that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve a similar device (method, or product) in the same way;
- applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

18. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

19. The analysis in this declaration is in accordance with the above-stated legal principles.

III. PERSON OF ORDINARY SKILL IN THE ART

20. It is my understanding that when interpreting the claims of the '638 patent I must do so based on the perspective of one of ordinary skill in the art at the relevant priority date. My understanding is that the earliest claimed priority date of the '638 patent is February 18, 1997.

21. The '638 patent describes a method of forming a void-free tungsten interconnect, or via an integrated circuit.

22. In my opinion a person of ordinary skill in the art for the '638 patent would have been a person with a Bachelor of Science degree in Electrical Engineering and four or more years of industry experience with semiconductor device fabrication and processing or a person with a Master of Science in Electrical Engineering and two or more years of industry experience with semiconductor device fabrication and processing.

23. As explained above, my own training and experience exceeds that of a person of ordinary skill in the art. Furthermore, I am familiar with the knowledge and capabilities of a person of ordinary skill in the relevant art in the period around 1997 – the period that includes the earliest priority date of the '638 patent. Specifically, my work with engineers practicing in the industry allowed me to become personally familiar with the level of skill of individuals and the general state of the art.

24. Unless otherwise stated, my testimony refers to the knowledge of one of ordinary skill in the art at the time before the earliest priority date of the '638 patent.

IV. BACKGROUND TECHNOLOGY

25. In this section I am providing information regarding relevant technologies that may be useful in understanding the claimed inventions and the prior art.

A. Planarization And Chemical-Mechanical Processing (“CMP”)

26. As is well known, today's integrated circuits based on CMOS technology consist of millions of transistors that perform logic operations. In order to perform useful functions, these transistors are connected together using a metal interconnect technology. Basically, the metal interconnects crisscross the

integrated circuit so as to connect up the various transistors. In order to avoid shorting all of the connections, the interconnects are arranged in stacked layers with insulating dielectric separating the layers and thereby allowing the interconnects to reach their destination. In order for different conductor layers to contact with each other, holes (called “vias”) are introduced into the dielectric insulators at specifically designed points.

27. In the early days of integrated circuit processing (through the early 1990s), the interconnect layers were formed using a process now termed “conformal.” A simple example is shown below:

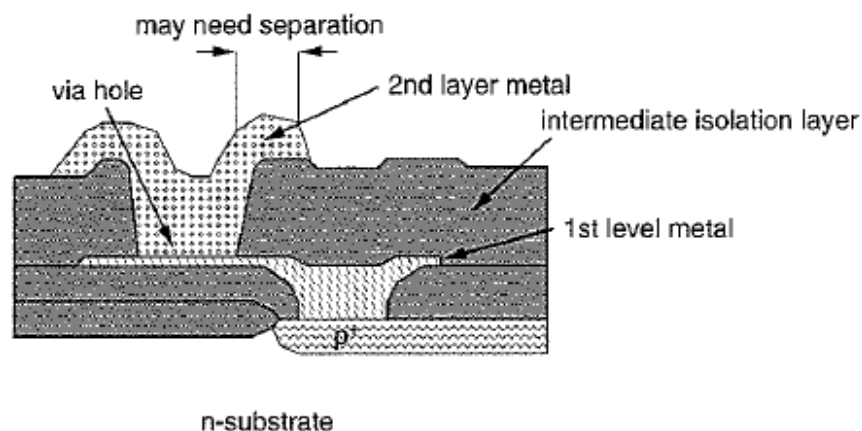


FIGURE 3.13 Two-level metal process cross section

Ex. 1009 at FIG. 3.13 (p. 131)¹

¹ “Principles of CMOS VLSI Design” by Weste *et al.* (Ex. 1009) is a treatise on CMOS IC design. It is my understanding that **Ex. 1009** was published in or around October 1994. I am citing to **Ex. 1009** merely to describe the state of the

Shown in the figure above is part of a transistor (labeled “p+”). The insulating dielectric layers are shown in dark grey. As indicated there is a contact area that connects the first layer metal to the conductive layer. Additionally, there is a second “via hole” that connects the second layer metal to the first layer metal. This process is referred to as “conformal” as the next layer conforms to the topology of the underlying layers.

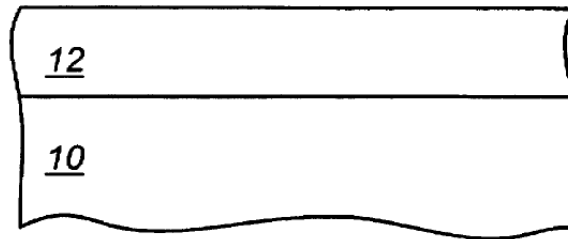
28. The conformal process necessarily results in increased lumpiness as the number of layers increases. As a practical matter, the number of metal layers that were supported by such a process was limited to about two. However, as process technology advanced, there developed a need for an increase in the number of layers. In order to implement more metal layers, process designers realized that each layer should be made as flat (or planar) as possible before beginning the process of fabricating the next layer.

29. Accordingly, process designers in the 1990s developed process technologies that adapted the previous generation conformal metallization and etching technologies but produced planar metallization structures. One such

relevant technology and the knowledge of a person of ordinary skill in the art on or around the effective filing date of the '638 patent. I am not citing to **Ex. 1009** to opine on whether it invalidates the '638 patent.

technology is disclosed as prior art in U.S. Patent No. 5,801,094 to Yew *et al.* (“Yew”; Ex. 1015).²

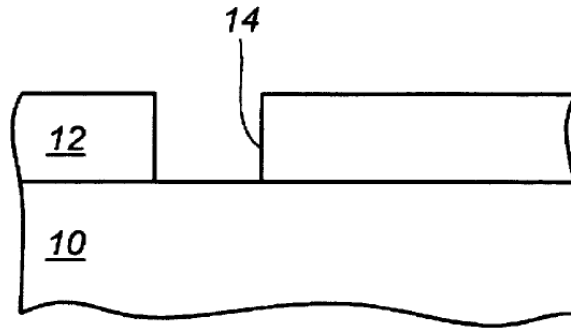
30. This planarization process is illustrated in Figures 1-7 of Yew. The process begins with an oxide layer, (12) created on top of the substrate (10) as shown in the figure below. (Ex. 1015 at FIG. 1, 1:48-52):



Yew (Ex. 1015) at FIG. 1

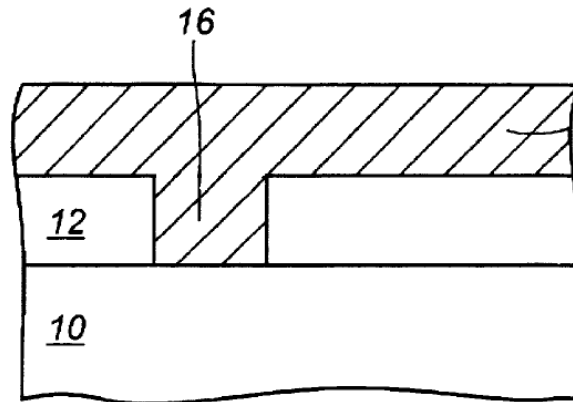
31. Next, as explained in Yew, a dielectric layer is deposited on the substrate, and contact holes are opened in the layer where it is desired to make contact with the MOS transistors in the substrate. (Ex. 1015 at FIG. 2; 1:53-56).

² I am citing to Yew merely to describe the state of the relevant technology on or around the effective filing date of the '638 patent. I am not citing Yew to opine on whether it invalidates the '638 patent.



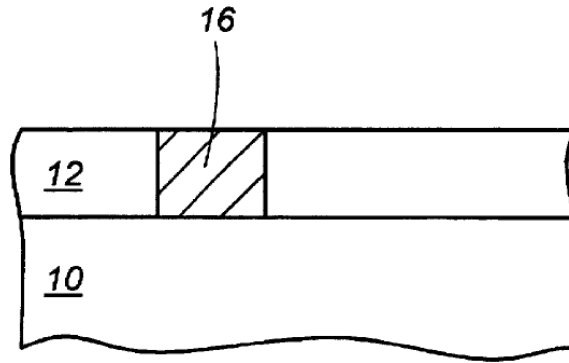
Yew (Ex. 1015) at FIG. 2

32. Next, metal layer (16) is deposited on top of the structure resulting in the figure shown below. (Ex. 1015 at FIG. 4 (Annotated), 1:59-2:2).



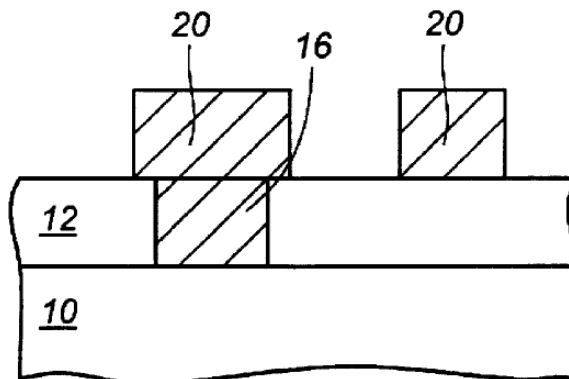
Yew (Ex. 1015) at FIG. 4 (Annotated)

33. Yew then explains that the metal is subjected to a polishing process. This process is “CMP” or chemical-mechanical processing. (Ex. 1015 at 1:66-2:2). The result is that all of the metal above the dielectric layer (12) is removed. The result is shown in the figure below. (Ex. 1015 at FIG. 3, 1:59-2:2).



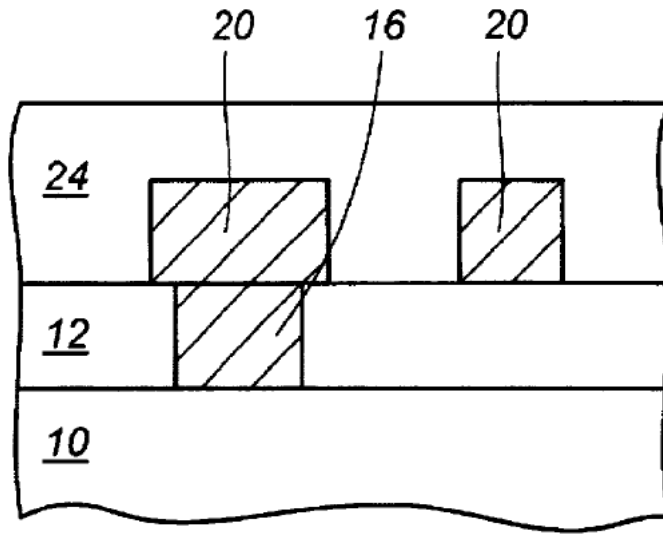
Yew (Ex. 1015) at FIG. 3

34. Next a metal pattern is formed on top of layer 12, using standard photolithographic techniques by providing a resist pattern and etching away metal not protected by the resist. These metal patterns facilitate connection of the various transistors. (Ex. 1015 at FIGS. 4-5, 2:3-18).



Yew (Ex. 1015) at FIG. 5

35. Next a thick dielectric layer is again applied above the metal, and as shown in the figure below, the top of this layer is planarized using CMP as described above. (Ex. 1015 at FIGS. 6-7, 2:18-31).



Yew (Ex. 10105) at FIG. 7

36. This process can be repeated to build a complex multi-layer interconnect system capable of providing connections to millions of transistors in advanced integrated circuits at the time of the filing of the '638 Patent.

B. Dry Etching, Chemical Etching, And Physical (Sputter) Etching

37. Etching refers to processes that are used to define the metal lines and vias discussed in the previous paragraphs. Etching results in the removal of unwanted material from the wafer. For example, the via hole (14) in Figure 2 of Yew is formed by etching the dielectric material (12).

38. Dry etching refers to a family of etching methods by which the surface of a wafer is etched in the gas phase. (Ex. 1008³ at p. 53). Dry etching is

³ “Fundamentals of Microfabrication” by Marc J. Madou (Ex. 1008) is a technical treatise on IC fabrication. It is my understanding that Ex. 1008 was published in

distinguished from wet etching, which uses liquid etchants to etch the surface of a wafer. Dry etching can be physical (by ion bombardment or sputtering), chemical (by a chemical reaction), or both. (*Id.*).

39. There are several considerations in selecting a dry etching process. One such consideration is the desired shape of the etch profile. (Ex. 1008 at pp. 53-54). Generally, isotropic or anisotropic etch profiles can be obtained through dry etching, as shown in the figure below. (Ex. 1008 at FIG. 2.2). As shown, anisotropic dry etching has a preferred direction, and even unidirectional. (Ex. 1008 at pp. 53-54). In contrast, isotropic etching does not have a preferred direction and will etch materials at an equal rate in all directions – *i.e.*, a uniform etch, as shown in the left most image below. (*Id.*). Anisotropic etching would likely be used to create the via hole (14) in Figure 3 of *Yew* above.

or around September 1997, which is around the effective filing date of the '638 patent. I am citing to Ex. 1008 merely to describe the state of the relevant technology and the knowledge of a person of ordinary skill in the art on or around the effective filing date of the '638 patent. I am not citing to Ex. 1008 to opine on whether it invalidates the '638 patent.

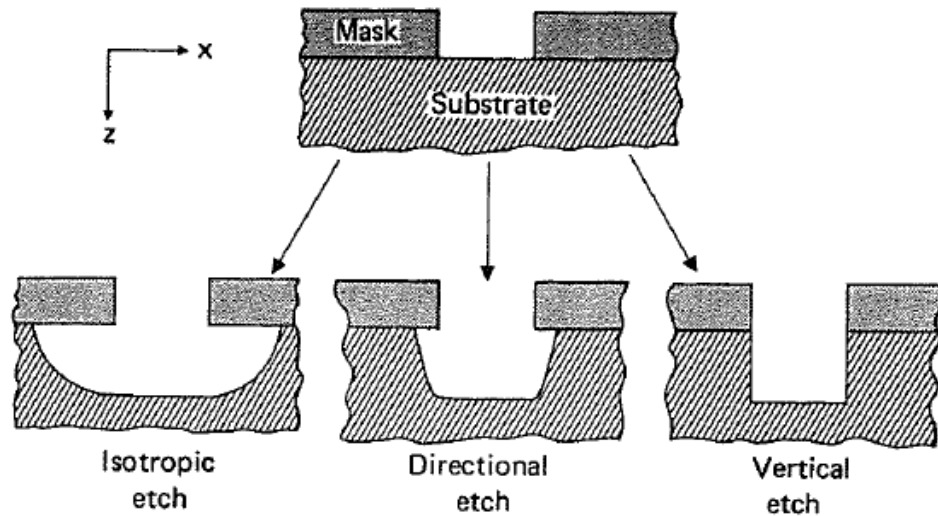


FIGURE 2.2 Directionality of etching processes.

Ex. 1008 at FIG. 2.2 (p. 56)

40. Another consideration is selectivity. Selectivity refers to the difference in etch rate between two materials using a given etchant. (Ex. 1008 at p. 54). High selectivity indicates that one material will be etched at a higher rate than the other, *i.e.*, the etchant is used to selectively etch one material over the other. (*Id.*). Conversely, low selectivity indicates that the etch rate for both materials will be similar. (*Id.*).

41. In dry chemical or reactive etching, reactive chemicals (*i.e.*, etchants) diffuse to the surface of the wafer and selectively react with layers on the wafer surface. (Ex. 1008 at p. 67, FIG. 2.12). In a chemical dry etch, the plasma does not etch the wafer itself but instead allows the etchant (or its components) to diffuse towards the wafer. (*Id.*).

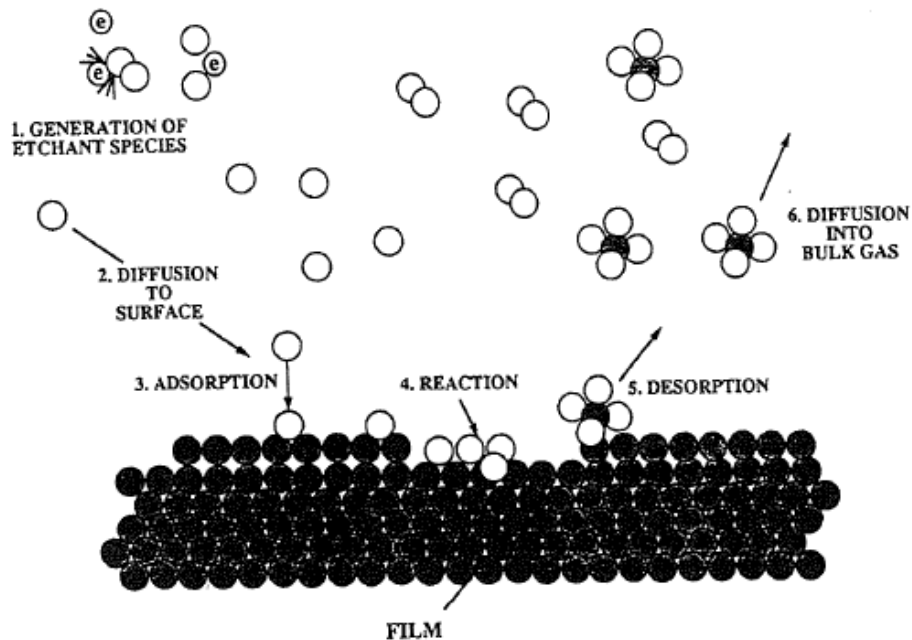


FIGURE 2.12 Primary process occurring in a plasma etch process.

Ex. 1008 at FIG. 2.12 (p. 67)

42. Because materials are etched through a chemical reaction, dry chemical etching tends to be highly selective. (Ex. 1008 at p. 68). Dry chemical etching also tends to be more isotropic than sputter or physical etching. (*Id.*).

43. In physical or sputter etching, an inert gas (e.g., Argon) is energized into an ionized state. (Ex. 1008 at p. 62). A potential across the chamber accelerates the energized gas ions towards the surface of the wafer in a targeted direction relative to the wafer. (Ex. 1008 at p. 55). When the accelerated gas ions collide with the wafer surface, momentum is transferred from the gas ion to the atoms on the wafer surface and the atoms are ejected. (Ex. 1008 at p. 62). Sputter etching is a slow process, relative to other etching techniques, having slow etch

rates and has high energy requirements. (Ex. 1008 at p. 63). Shown in the figure below is an exemplary reactor for sputter etching.

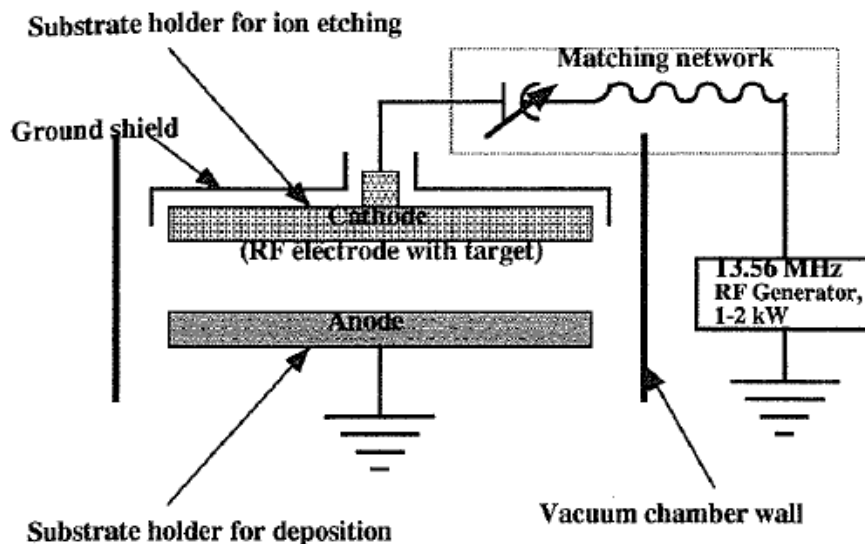


FIGURE 2.8 Two electrode set-up (diode) for RF ion sputtering or sputter deposition. For ion sputtering, the substrates are put on the cathode (target); for sputter deposition, the substrates to be coated are put on the anode.

Ex. 1008 at FIG. 2.8 (p. 60)

44. Because ions are accelerated towards the wafer surface at a uniform angle, the wafer is etched substantially in the direction along the path of the ions. Hence, sputter etching is highly anisotropic. (Ex. 1008 at p. 63).

45. Sputter etching is also highly nonselective because the ion energy required to eject materials is large compared to the differences in chemical bond energy of the various materials on the surface of the wafer. (Id.).

46. Another property of sputter etching is that it tends to develop facets on the edge or corners of a layer, *e.g.*, resist or oxide. Facets at the corners form because the etch rate in sputter etching is highly sensitive to the angle of incidence. (Ex. 1008 at p. 64). The corners of layers such as resist are often rounded even when formed vertically. (*Id.*). The rounded corners create a smaller angle of incidence, and in turn causes the corners to etch faster than the rest, such as flat surface regions. (*Id.*). The faceting of corners in sputter etching is further illustrated in the figure below. (Ex. 1008 at FIG. 2.11).

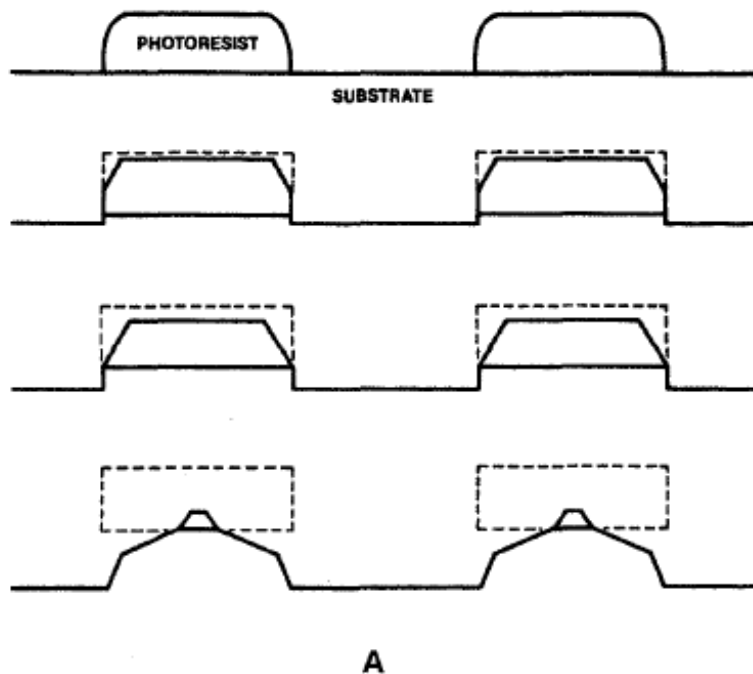


FIGURE 2.11 Limitations of dry physical etching. (A) Faceting. Sputtering creates angled features. An angled facet ($\sim 60^\circ$) in the resist propagates as the mask is eroded away. Sloped walls may also be created in the underlying substrate.

Ex. 1008 at FIG. 2.11(A) (p. 64): Faceting In Sputter Etching

C. Resist Removal (Resist Stripping)

47. After the exposed oxide has been etched away, the remaining resist is removed for further processing. (Ex. 1008 at p. 33). This process is referred to as resist stripping. (Id.). The primary consideration in resist stripping is high selectivity, *i.e.*, removing the resist without damaging the device layers.

48. Resist stripping can be performed wet or dry. (Ex. 1008 at p. 33). In wet resist stripping, the resist is stripped off with chemicals (*e.g.*, H₂SO₄, acetone) which selectively erode the resist but not the oxide or the silicon. (Id.).

49. In dry stripping, oxygen (O₂) plasma is used to remove the resist. (Ex. 1008 at pp. 33-34). This type of plasma stripping belongs to the category of dry chemical etching and is isotropic in nature. (Ex. 1008 at p. 34).

V. THE '638 PATENT

A. Overview

50. The '638 patent relates to forming void-free interlayer contacts (“vias”) in integrated circuits without altering the dimensions or design rules of the vias. (Ex. 1001 at 2:28-54).

51. Specifically, the '638 patent discloses two embodiments. In the first embodiment, a substantially vertical contact hole is created in the dielectric layer via lithography, after which the resist layer is removed. (Ex. 1001 at FIG. 4, 3:44-4:8). Then, the top portion of the contact hole is widened using an anisotropic etch

process. (Ex. 1001 at 4:9-12). The widened contact hole prevents the metal deposition on the surface of the wafer from collapsing and thereby blocking deposition of metal inside the contact hole. (Ex. 1001 at 4:20-32, 5:23-30). This is further illustrated in Figures 4-5. (Ex. 1001 at FIGS. 4-5).

52. Once the metal is deposited inside the contact hole, the bulk metal on the surface of the wafer and a portion of the dielectric layer containing the widened contact hole is removed by CMP (“chemical-mechanical polishing”). (Ex. 1001 at 5:31-54). By removing the widened portion, the original dimension (*e.g.*, radius) of the contact hole is restored. (*Id.*). This is further illustrated in Figures 6-7.

53. The ’638 patent further discloses an alternate embodiment. In the alternate embodiment, the top portion of the contact hole is widened before the resist layer is removed. (Ex. 1001 at 6:33-50). This requires etching a portion of the dielectric layer underneath the resist layer. (Ex. 1001 at 6:40-50, FIG. 8). Hence, an isotropic etch process is utilized. (Ex. 1001 at 6:42-43 (“exposed to an isotropic etch chemistry”)). This alternative embodiment is further illustrated in Figures 8-11.

B. Claim Interpretation

1. “anisotropically etching”; “anisotropic etch” (Claims 8, 11)

54. In my opinion, the terms “anisotropically etching” and “anisotropic etch” as recited in Claims 8 and 11 collectively refer to “non-uniform etching.”

55. The term “anisotropic etch” (and “anisotropically etching”) means a non-isotropic etch. In isotropic etching, materials are etched at substantially equal rates in all directions. That is, isotropic etching is uniform etching. Hence, “anisotropic etching,” which is the opposite of isotropic etching, is non-uniform etching. Anisotropic etching can also be one-directional, *e.g.*, vertical. (See ¶ 38 *infra*, Ex. 1008 at FIG. 4.30 (p. 174).)

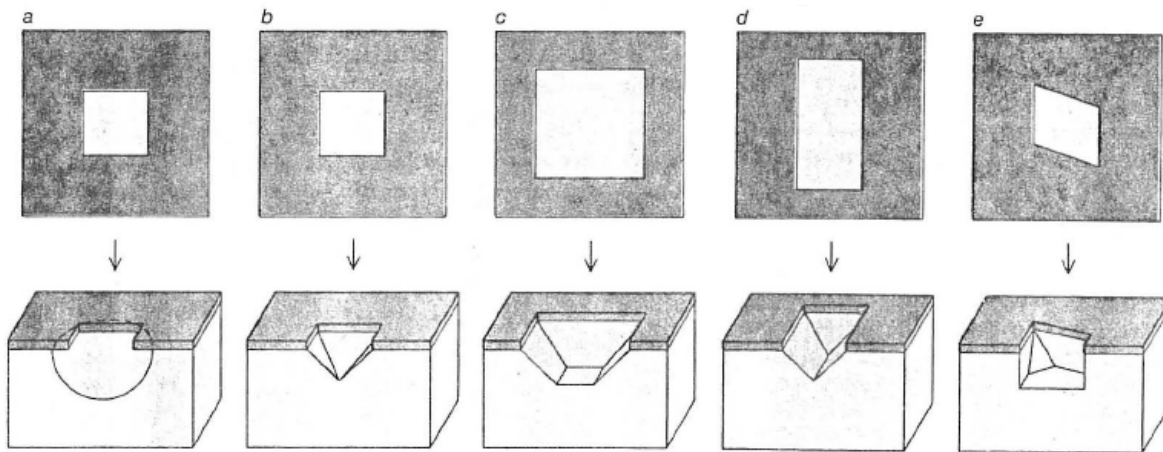


FIGURE 4.30 . Isotropic and anisotropic etched features in $\langle 100 \rangle$ and $\langle 110 \rangle$ wafers. (a) isotropic etch; (b) to (e) anisotropic etch. (a) to (d): $\langle 100 \rangle$ oriented wafers and (e): $\langle 110 \rangle$ oriented wafer.

Ex. 1008 at FIG. 4.30 (p. 174): Wet Etch Profiles

56. This is true for both wet etching and dry etching. The figure above illustrates the etch profiles for various types of wet etching. (Ex. 1008 at FIG. 4.30 (p. 174).) As shown in the figure, isotropic etching results in a semi-spherical etch profile, the shape of which is dependent upon the aperture and etching parameters. (Ex. 1008 at FIG. 4.30(a).) A semi-spherical etch profile indicates that the etching was uniform in all directions, *i.e.*, the same isotropic process used to create the

“wine glass” etch in FIG. 9 of the ‘638 patent. (Ex. 1001 at FIG. 9; 6:61-65; see also Ex. 1009 at FIG. 3.12(a) (p. 129)). In contrast, anisotropic wet etching results in preferential etching along a particular crystallographic direction. (Ex. 1008 at FIGS. 4.30(b)-(e)). Hence, “anisotropic etching,” in the context of wet etching, is etching whose etch rate is not uniform in all crystallographic directions.

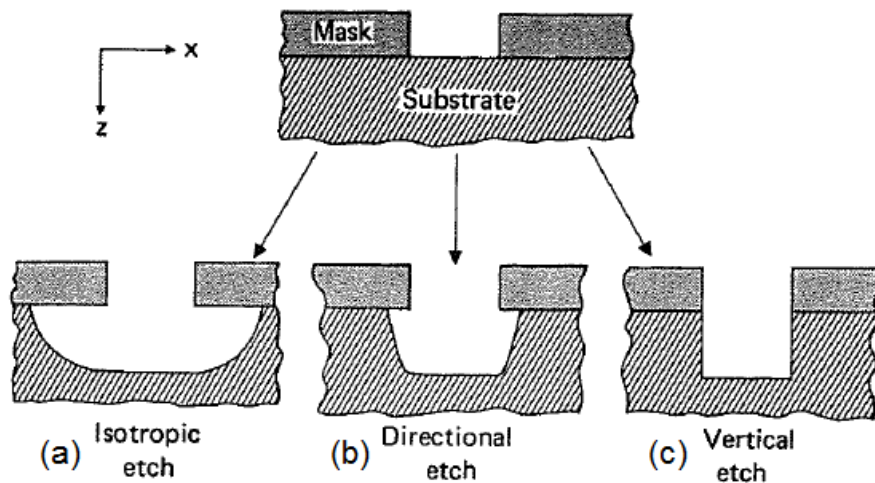


FIGURE 2.2 Directionality of etching processes.

Ex. 1008 at FIG. 2.2 (p.56): Dry Etch Profiles (Annotated)

57. In dry etching, the shape of an etch profile is not determined by the crystallographic direction of the etched material but instead by the plasma conditions, such as plasma pressure, reactivity of etchant to the material, and RF and DC fields applied to the plasma. (Ex. 1008 at p. 54). Despite the difference, isotropic dry etching also results in a semi-spherical, uniform etch profile, the shape of which is dependent upon the aperture and etching parameters. (Ex. 1008 at FIG. 2.2(a)) (*see above*). In contrast, anisotropic dry etching results in

preferential directional or one-directional (*e.g.*, vertical) etch profiles. (Ex. 1008 at FIGS. 2.2(b)-(c)). Hence, “anisotropic etching,” in the context of dry etching, is etching whose etch rate is not uniform in all directions.

58. The ’638 patent’s use of the terms “anisotropically etching” and “anisotropic etch” is consistent with the customary use of those terms by those in the field of semiconductor circuit fabrication, *i.e.*, non-uniform etching.

59. First, the claims of the ’638 patent require “anisotropically etching” a dielectric layer to create a via opening which, I understand, must encompass the vertical etches through the dielectric layer to form the openings because they are the only disclosed embodiment. (Ex. 1001 at Claims 8, 11; FIGS. 4 and 9; 3:44-52; 6:51-54). Also, this etching is substantially vertical and therefore non-uniform. (Ex. 1001 at FIG. 4). Thus, the ’638 patent’s requirement that “anisotropically etching” is a non-uniform vertical etch is consistent with the customary usage of the term “anisotropic etching.”

60. Second, the ’638 patent refers to the tapered top portion of the contact hole as being etched “using an anisotropic etch process.” (Ex. 1001 at FIG. 5). The rounded corners of the dielectric layer, which the ’638 patent describes as a “golf tee” profile, indicates a non-uniform etch. (Ex. 1001 at 6:61-65 (stating that anisotropic plasma taper process results in a “golf tee profile”)). Because the “golf tee” shape indicates a non-uniform etch, the ’638 patent’s characterization of the

“golf tee” etch as an “anisotropic etch process” is also consistent with the customary usage of the term “anisotropic etching.”

2. “storage node of an SRAM cell” (Claim 6)

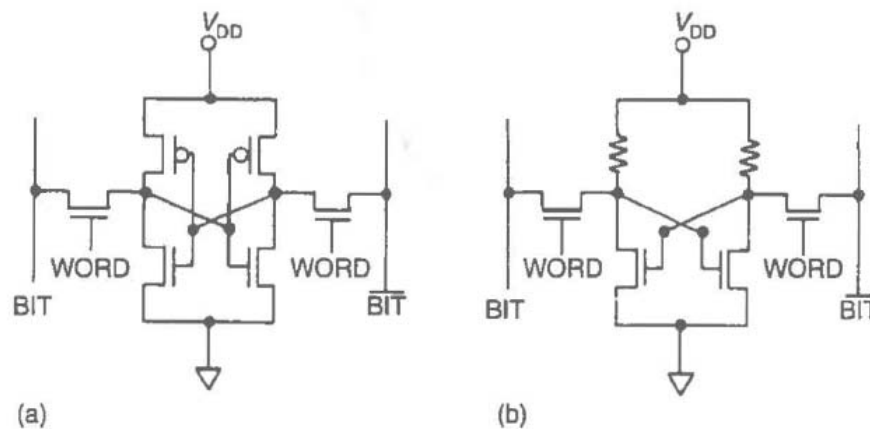
61. Claim 6 of the ’638 patent recites “forming a polysilicon layer which is coupled to a storage node of an SRAM cell.” (Ex. 1001 at 8:14-17). The ’638 patent does not explain what the term “storage node of an SRAM cell” means.

62. A “node” means “a connection of two or more conductive paths or regions.” (Ex. 1011⁴ at p. 1533). The term “storage node,” as used in the context of an SRAM, is commonly referred to as the node of the storage transistors of an SRAM cell where the data (or its complement) is stored. Figure 2-4 of “Semiconductor Memories,” a prior art treatise, shows the schematics of an SRAM cell. (Ex. 1014⁵ at p. 13, FIG. 2-4). As shown in the figure below, a basic SRAM

⁴ “Webster’s 3rd New International Dictionary” (Ex. 1011) has a copyright date of 1993. (Ex. 1011 at Copyright Page). Upon information and belief, Ex. 1011 was first published on or around December 1993. I am citing Ex. 1011 merely to describe the knowledge of a person of ordinary skill in the art around the effective filing date of the ’638 patent and not as prior art.

⁵ “Semiconductor Memories” by Ashok K. Sharma (Ex. 1014) is a technical treatise on semiconductor memory design. It is my understanding that **Ex. 1014**

cell consists of transistors that store the SRAM data (“storage transistors”) and transistors that control the connection between the storage transistors and the bit lines (“access transistors”). (Ex. 1014 at FIG. 2-4). In a CMOS implementation, a basic SRAM cell consists of six transistors. (Ex. 1014 at FIG. 2-4(a)). In an NMOS implementation, a basic SRAM cell consists of four transistors and two resistors. (Ex. 1014 at FIG. 2-4(b)).



Ex. 1014 at FIG. 2-4(a)-(b) (p. 13)

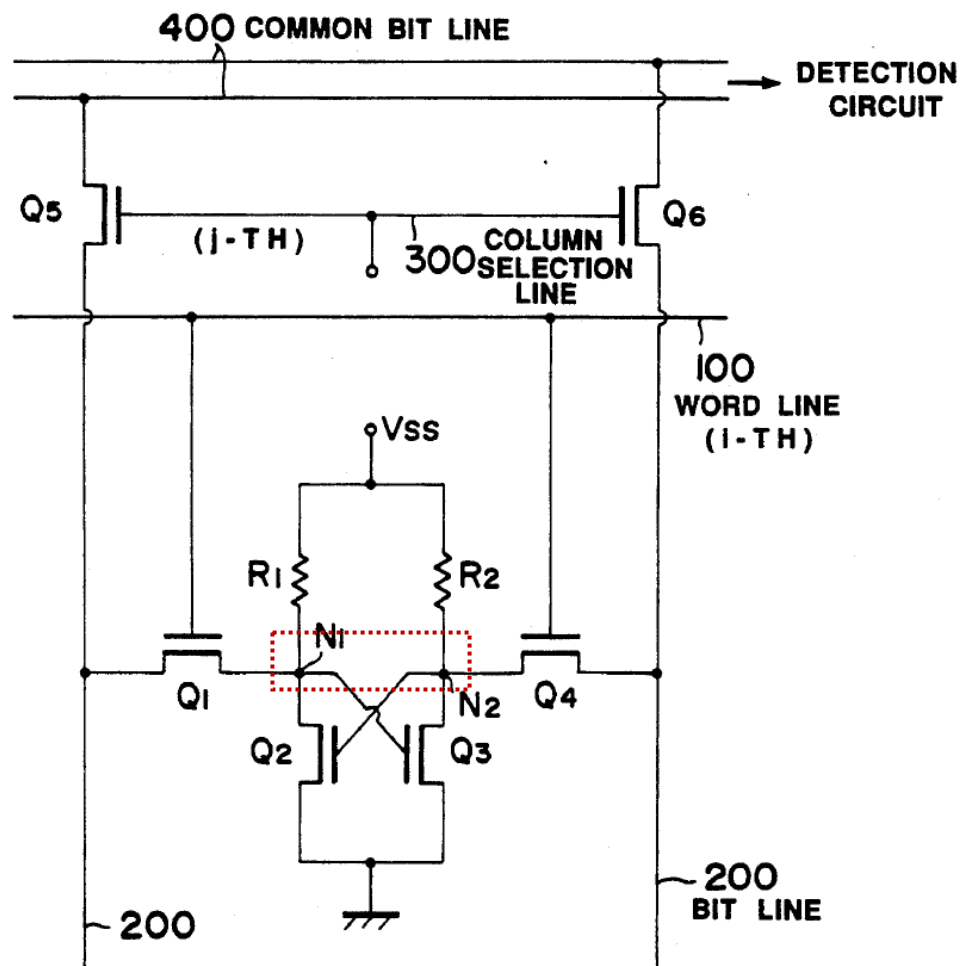
63. In both implementations, the storage transistors form a latch, which stores the SRAM data and its complement. As depicted in the figure above, a latch

was published in or around 1997, which is around the effective filing date of the '638 patent. I am citing to **Ex. 1014** merely to describe the state of the relevant technology and the of a person of ordinary skill in the art on or around the effective filing date of the '638 patent. I am not citing to **Ex. 1014** to opine on whether it invalidates the '638 patent.

is formed by coupling the gate(s) of the storage transistor(s) on the left side to the drain(s) of the storage transistor(s) on the right side, and vice versa. (Ex. 1014 at FIG. 2-4). The SRAM data and its complement is stored at the gate-drain connection, or node. This node is commonly referred to as the “storage node.”

64. A number of references published on or around the time of the effective filing date of the '638 patent use the term “storage node” to refer to the node where the drain(s) and gate(s) of storage transistors intersect in an SRAM cell. U.S. Patent No. 5,327,002 to Motoyoshi (“*Motoyoshi*”; Ex. 1012)⁶ identifies nodes N1 and N2 of Figure 11 as “storage nodes.” (Ex. 1012 at 1:36-42, FIG. 11). As depicted in Figure 11 of *Motoyoshi* (see below), the drain of storage transistor Q2 intersects with the gate of storage transistor Q3 at node N1, while the drain of storage transistor Q3 intersects with the gate of storage transistor Q2 at node N2. (Ex. 1012 at FIG. 11). During a read cycle, the data of the SRAM cell and its

⁶ It is my understanding that *Motoyoshi* (Ex. 1012) was filed on May 8, 1992 and subsequently issued on July 5, 1994. I am citing to *Motoyoshi* merely to describe the state of the relevant technology and the knowledge of a person of ordinary skill in the art at or around the effective filing date of the '638 patent. I am not citing *Motoyoshi* to opine on whether *Motoyoshi* invalidates the '638 patent.



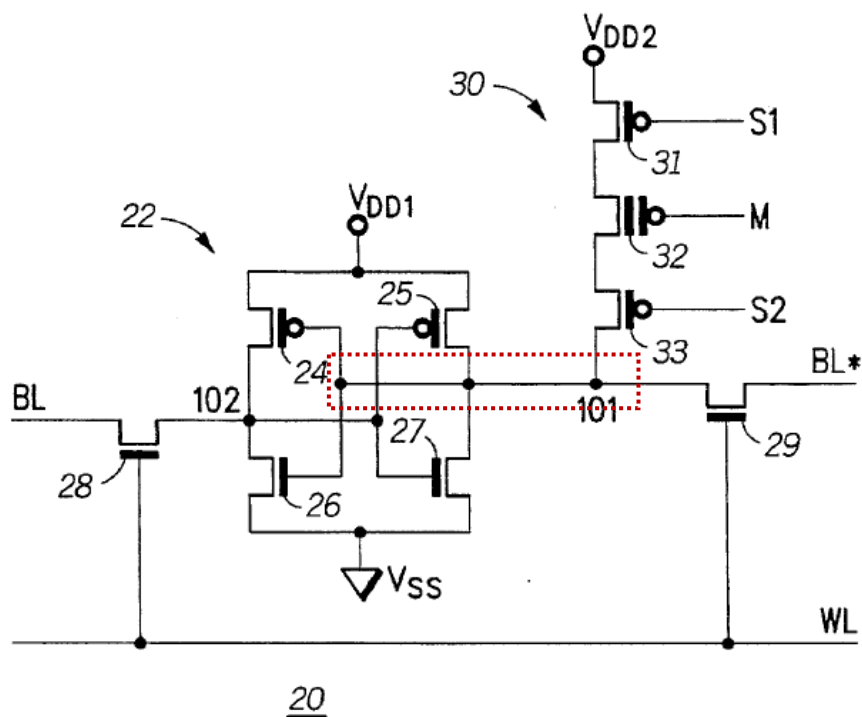
***Motoyoshi* (Ex. 1012) at FIG. 11 (Annotated)**

65. Another contemporaneous reference, U.S. Patent No. 5,488,579 to Sharma *et al.* (“Sharma”; Ex. 1013)⁷ discloses a six-transistor CMOS SRAM cell.

⁷ It is my understanding that *Sharma* (Ex. 1013) was filed on April 29, 1994 and subsequently issued on January 30, 1996. I am citing to *Sharma* merely to

(Ex. 1013 at FIG. 1). *Sharma* identifies node 101 in Figure 1 as a “storage node.”

(Ex. 1013 at 3:59-61). As depicted in Figure 1, the gates of storage transistors 24 and 26 (on the left side) intersect with the storage transistors 25 and 27 (on the right side) at node 101, which stores the complement of the SRAM data. (Ex. 1013 at FIG. 1).



Sharma (Ex. 1013) at FIG. 1 (Annotated)

66. In summary, the term “a storage node of an SRAM cell” is well understood to mean the node of the storage transistors of an SRAM cell where the describe the state of the relevant technology and the knowledge of a person of ordinary skill in the art at or around the effective filing date of the ’638 patent. I am not citing *Sharma* to opine on whether *Sharma* invalidates the ’638 patent.

data (or its complement) is stored, and that, in standard SRAM cells, such nodes are where the drain and gate electrodes of the storage transistors intersect.

3. “current electrode for a transistor” (Claim 7)

67. In my opinion, the term “current electrode for a transistor” means “a current conducting electrode in a transistor, such as a source or drain electrode.” The ‘638 patent states that a “current electrode” includes the source or drain of the transistor. Ex. 1001 at 3:25-27. Additionally, one of skill in the art would have this understanding of the term since the source and drain are the primary electrodes for passing current through a transistor.

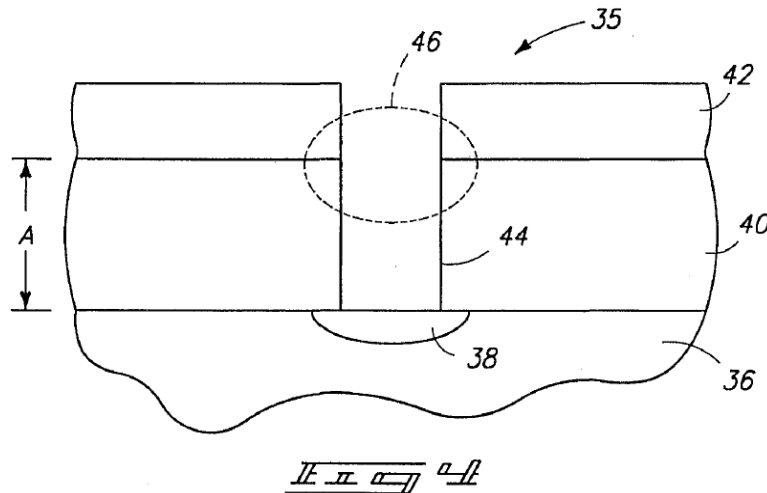
VI. PRIOR ART

A. U.S. Patent No. 5,580,821 (“Mathews”)

68. U.S. Patent No. 5,580,821 by Viju K. Mathews *et al.* (“Mathews”; Ex. 1004) issued on December 3, 1996 from an application filed on February 21, 1995. Hence, it is my understanding that *Mathews* is prior art to the ‘638 patent under 35 U.S.C. § 102(a).

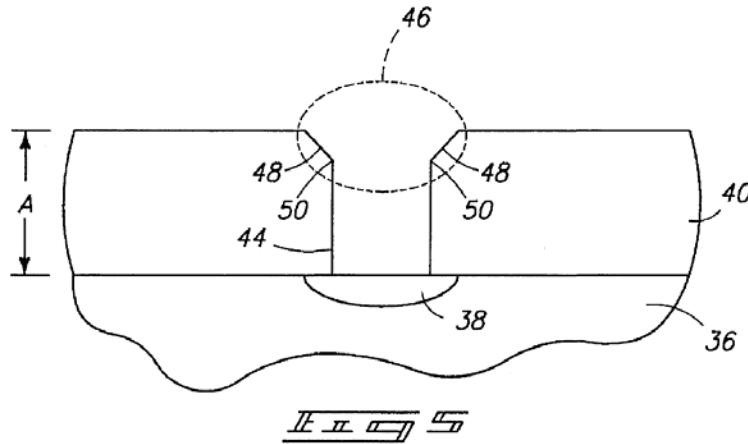
69. *Mathews* discloses methods for forming void-free vias in integrated circuits while maintaining the circuit density – addressing the same problems identified in the ‘638 patent. (Ex. 1004 at Abstract).

70. The method disclosed in *Mathews* is summarized as follows. First, a dielectric layer is formed above the substrate and the active regions and a resist layer is formed above the dielectric layer. (Ex. 1004 at 3:16-24, FIG. 4). The active regions, such as a source or drain region, are formed by doping portions of the substrate. The resist layer is patterned and a contact hole is formed where the resist pattern exposed the dielectric layer by an anisotropic etch. (Ex. 1004 at 3:25-38, FIG. 4). These steps are depicted in Figure 4 of *Mathews*, below.



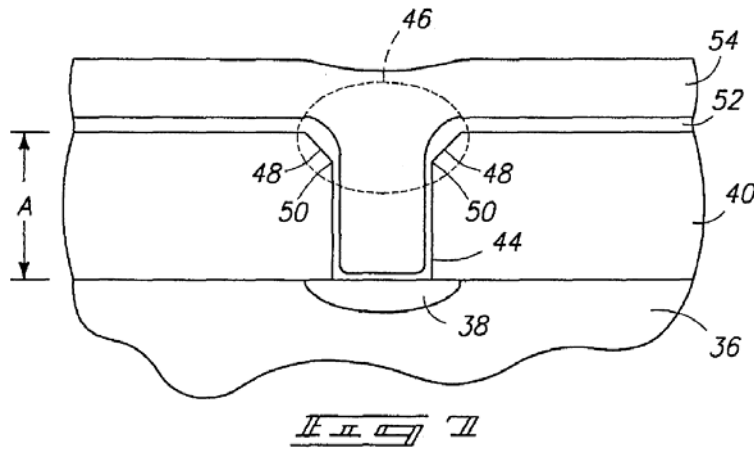
Mathews (Ex. 1004) at FIG. 4

71. After the contact hole is formed, the resist is stripped away from the contact hole to expose the portion of the dielectric layer adjacent to the contact hole. (Ex. 1004 at 3:39-60, FIG. 5). Then an anisotropic facet sputter etching is conducted to create facets or “outwardly angled sidewalls” at the top portion of the contact holes. (Ex. 1004 at 3:39-60, FIG. 5). These steps are depicted in Figure 5 of *Mathews*, below.



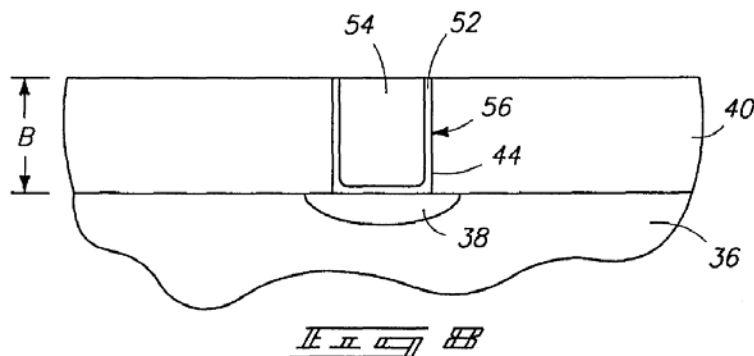
Mathews (Ex. 1004) at FIG. 5

72. Next, one or more metal layers are deposited inside the contact holes and on the surface of the dielectric layer. (Ex. 1004 at 3:61-4:16, FIGS. 6-7). In one embodiment, a thin layer of titanium is first deposited and then tungsten is deposited. (Ex. 1004 at 3:61-4:7; FIGS. 6-7). According to *Mathews*, the tapered opening permits the deposition of the metal materials without the formation of “cusps” or “keyholes.” (Ex. 1004 at FIGS. 2 & 7; 4:30-32. In other embodiments, only one or three or more metal layers are deposited. (Ex. 1004 at 4:8-10). The result of these steps are depicted in Figure 7 of *Mathews*, below.



Mathews (Ex. 1004) at FIG. 7

73. Finally, the metal deposited on the surface of the dielectric layer is removed via chemical-mechanical polishing (“CMP”). (Ex. 1004 at 4:17-42, FIG. 8). In addition, the dielectric layer is polished away until the facet or the “outwardly angled sidewalls” are all removed. (Id.) As a result, the radius of the contact holes are restored to their original size. (Ex. 1004 at FIG. 8; 4:31-32 (“small-size/maximum density goals are not defeated”)). These steps are depicted below in Figure 8 of *Mathews*.



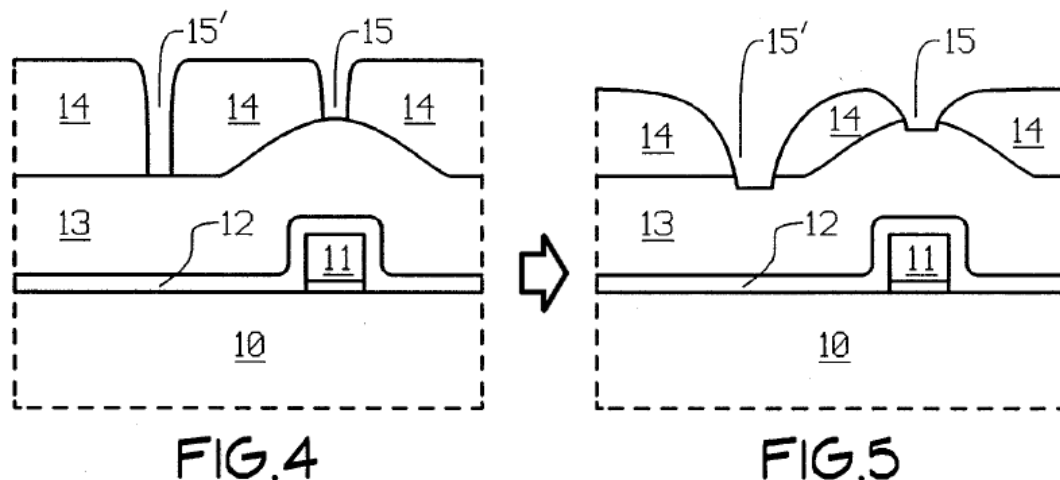
Mathews (Ex. 1004) at FIG. 8

B. Prior Art: U.S. Patent No. 4,939,105 (“Langley”)

74. U.S. Patent No. 4,939,105 by Rod C. Langley (*“Langley”*; Ex. 1005) issued on July 3, 1990 from an application filed on August 3, 1989. Hence, it is my understanding that *Langley* is prior art to the ’638 patent under 35 U.S.C. §§ 102(a) and (b).

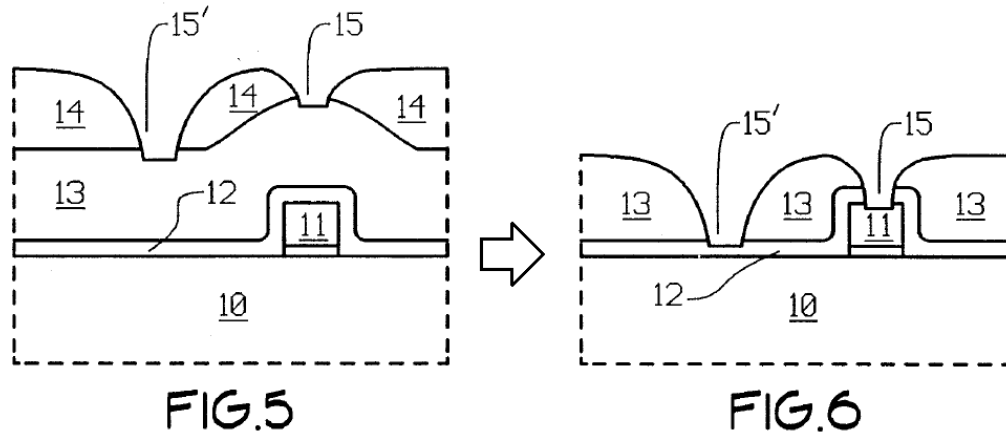
75. Langley discloses methods for forming vias in integrated circuits. (Ex. 1005 at Abstract).

76. The method disclosed in *Langley* consists of four etching steps after conductive, dielectric and photoresist layers have been deposited in a conformal process. (Ex. 1005 at 3:4-13). In the first etch, the resist layer is partially etched to form a slope in the resist layer. (Ex. 1005 at 3:36-47, FIGS. 4-5). The result of the first step is depicted below in Figures 4-5 of *Langley*.



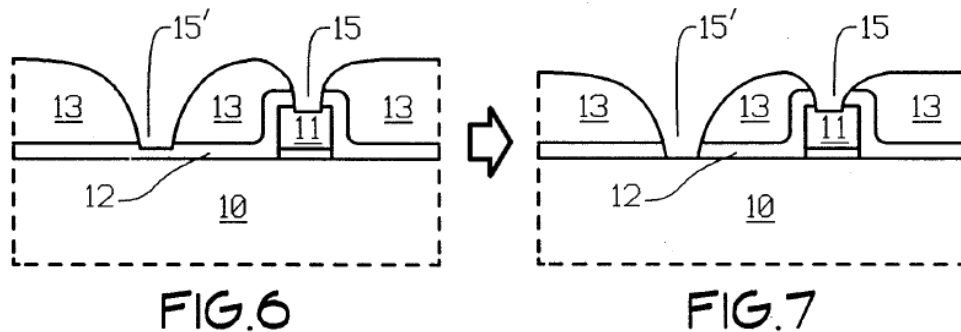
Langley (Ex. 1005) at FIGS. 4-5: Partial Resist Removal & Slope Formation

77. In the second etch, the resist layer and the underlying oxide layer are etched simultaneously and at a 1:1 etch ratio (*i.e.*, non-selective) until all of the remaining resist layer is removed. (Ex. 1005 at 3:48-61, FIGS. 5-6). This creates a sloped oxide layer, as depicted below in Figures 5-6 of *Langley*.



Langley (Ex. 1005) at FIGS. 5-6: Residual Resist Removal & Oxide Removal

78. In the third and fourth steps, any oxide remaining inside the contact hole is etched away to expose the substrate where the contact is to be made. (Ex. 1005 at 3:62-4:20, FIGS. 6-7). The result of the third and fourth steps are depicted below in Figures 6-7 of *Langley*.



Langley (Ex. 1005) at FIGS. 6-7: Residual Oxide Etch

C. Prior Art: U.S. Patent No. 5,547,892 (“Wuu”)

79. U.S. Patent No 5,547,892 by Shou-Gwo Wu *et al.* (“Wuu”; Ex. 1006) issued on August 20, 1996 from an application filed on April 27, 1995. Hence, it is my understanding that *Wuu* is prior art to the ’638 patent under 35 U.S.C. § 102(a).

80. *Wuu* relates to forming improved nodes in SRAMs. (Ex. 1006 at Abstract). FIG. 1 of *Wuu* depicts a circuit schematic for a six-transistor SRAM cell, the operation of which was well understood by persons of ordinary skill in the art. (Ex. 1006 at FIG. 1: 30-49). The “storage nodes” located at Q1 and Q2, which store the data and its complement, respectively. (Ex. 1006 at FIG. 1: 30-49).

81. *Wuu* explains that prior art technology formed the storage nodes Q1 and Q2 in SRAMs by directly coupling doped (poly- or amorphous) silicon regions together, *e.g.*, drain and gate regions. (Ex. 1006 at 2:1-28, FIG. 5). When the two regions in contact are doped with impurities of the opposite types, the contact becomes an PN-junction and exhibits diode-like characteristics. (Ex. 1006 at 2:34-41). This increases the effective resistance of the contact and storage nodes, which is undesirable in SRAMs. (*Id.*).

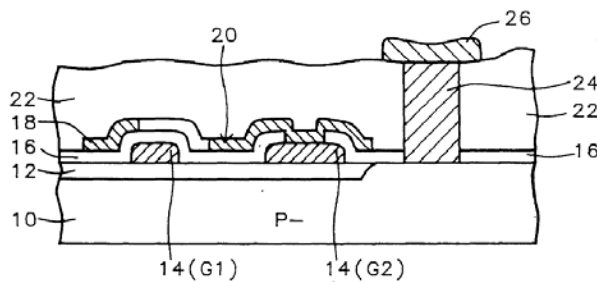


FIG. 5 - Prior Art

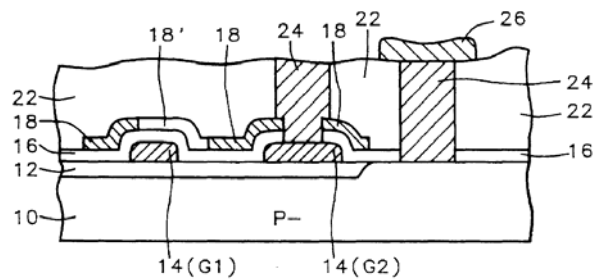


FIG. 9

Wuu (Ex. 1006) at FIG. 5 - Prior Art Versus FIG. 9

82. Wuu thus proposes forming the contacts (and storage nodes) in SRAMs using metal contact plugs, such as tungsten, which is depicted in Figure 9 of Wuu. (Ex. 1006 at FIG. 9; 7:12-16). Wuu explains that by coupling the doped silicon regions through a metal plug, the PN-junction is eliminated and the resistance of the node is lowered. (Ex. 1006 at 3:49-51, FIG. 9).

VII. UNPATENTABILITY BASED ON PRIOR ART IN THE PRESENT PROCEEDINGS

83. As I noted above, it is my understanding that the '638 patent claims priority to the parent application filed on February 18, 1997. It is my understanding that all of the art discussed below qualify as prior art in view of this February 18, 1997 date.

84. I have been informed that a patent claim can be found unpatentable as anticipated when each and every claim limitation is found within a single reference or is a necessary part of a claim limitation.

85. I have been informed that a patent claim can be found unpatentable as obvious where the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art. I understand that an obviousness analysis involves a consideration of: (1) the scope and content of the prior art; (2) the differences between the claimed inventions and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations of non-obviousness.

86. My analysis of these considerations is set forth in the following sections.

A. Mathews Anticipates Claims 8-11 Of The '638 Patent

87. As I noted above, *Mathews* discloses a method for forming a void-free via in integrated circuits by widening the top portion of the via to allow uniform metal deposition and subsequently polishing the widened portion to preserve the circuit density. (See ¶ 69 *infra*; Ex. 1004 at Abstract).

88. In my opinion, *Mathews* anticipates Claims 8-11 because *Mathews* discloses each and every element of Claims 8-11.

1. Claim 8: *Mathews* Anticipates Claim 8

89. Claim 8 (Ex. 1001 at 8:22-43) recites:

8. A method for forming an integrated circuit, the method comprising:

[8a] patterning a resist layer over a dielectric layer;

[8b] anisotropically etching portions of the dielectric layer exposed by the resist layer to define an opening in the dielectric layer, wherein:

[8c] the opening includes a top portion that is adjacent an upper surface of the dielectric layer, a bottom portion that is opposite the top portion, and a sidewall portion that is disposed between the top portion and the bottom portion;

[8d] removing the resist layer;

[8e] tapering the top portion of the opening using an anisotropic etching process after removing of the resist layer;

[8f] depositing a material over portions of the upper surface of the dielectric layer and within the opening; and

[8g] polishing to remove (1) the material over portions of the upper surface of the dielectric layer and (2) the top portion of the opening including the taper and portions of the material contained within the top portion.

90. In my opinion, *Mathews* anticipates Claim 8 because *Mathews* discloses each and every element of Claim 8.

a. Claim 8 Preamble

91. *Mathews* discloses “a method for forming an integrated circuit.” (Ex. 1001 at 8:22-23; Ex. 1004 at Title, Abstract, 1:7-9, FIGS. 4-9).

b. Claim Element [8a]

92. *Mathews* discloses “patterning a resist layer over a dielectric layer.” (Ex. 1001 at 8:24; Ex. 1004 at Abstract, 2:60-63, 3:16-32, 5:1-4, 5:25-26, 6:18-21, FIG. 4; see also ¶ 70, *infra*).

c. Claim Element [8b]

93. *Mathews* discloses “anisotropically etching portions of the dielectric layer to define an opening in the dielectric layer.” (Ex. 1001 at 8:25-27). *Mathews* discloses etching the portion of the oxide that is exposed by the resist pattern. (Ex. 1004 at FIG. 4; see also ¶ 69, *infra*). The etch creates a vertical contact hole in the oxide layer and is thus an anisotropic etch. As I noted, the term “anisotropic etching” means non-uniform etching (*i.e.*, etch rate is not substantially uniform in all directions). (See ¶¶ 54-60, *infra*). Furthermore, anisotropic etching includes vertical etching. (See ¶¶ 57-58, *infra*). As I noted above, this is consistent with the ’638 patent and also the understanding of a person of ordinary skill in the art. (see ¶¶ 53-59, *infra*). Therefore, *Mathews* discloses claim element [8b].

d. Claim Element [8c]

94. *Mathews* discloses that “the opening includes a top portion that is adjacent to the upper surface of the dielectric layer, a bottom portion that is opposite the top portion, and a sidewall portion that is disposed between the top portion and the bottom portion.” (Ex. 1001 at 8:29-33; Ex. 1004 at FIG. 4, 3:29-32).

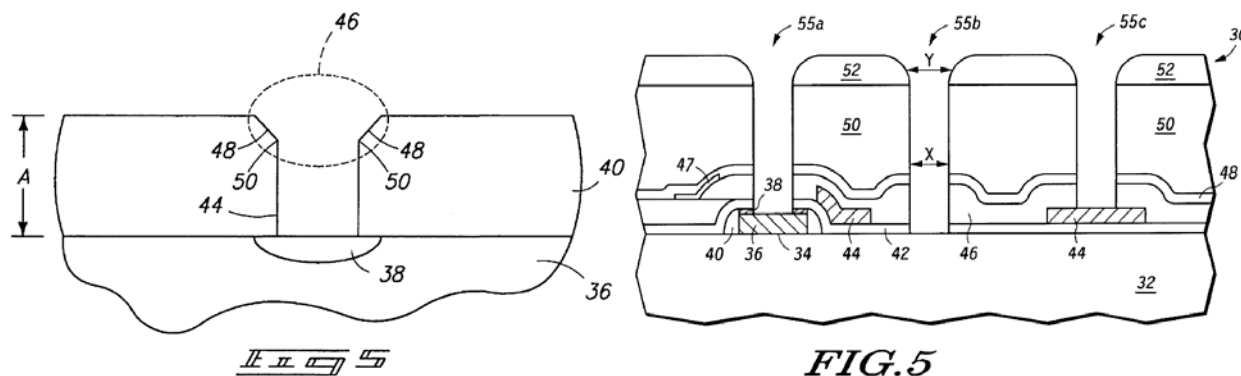
e. Claim Element [8d]

95. *Mathews* discloses “removing the resist layer.” (Ex. 1001 at 8:34; Ex. 1004 at Abstract, 3:1-2, 3:38-39, 3:43-50, 5:9-10, 6:26-27, Figs. 4-5; see also ¶ 71, *infra*).

f. Claim Element [8e]

96. *Mathews* discloses “tapering the top portion of the opening using an anisotropic etch.” (Ex. 1001 at 8:35-36). *Mathews* discloses that sloped sidewalls in the contact holes can be created using “facet sputter etching.” (Ex. 1004 at 3:39-44). The resulting outwardly angled sidewalls correspond to the “taper[ed] top portion of the opening,” as shown in FIG. 5, the tapered portion extending from the top of the dielectric layer to the sidewalls. (Ex. 1004 at FIG. 5). The top of the tapered opening has a radius (Y) greater than the radius of the lower portion of the opening (X). (Ex. 1004 at FIG. 5).

97. Further, “facet sputter etching” corresponds to the term “using an anisotropic etch.” As I noted, because sputter etching removes material by directional bombardment of ions, sputter etching is highly directional (*i.e.*, non-uniform) and therefore anisotropic. (*See* ¶ 43 *infra*).



Ex. 1004 at FIG. 5 versus Ex. 1001 at FIG. 5: “Golf Tee” Profile

98. Also, the shape of the sloped sidewalls are remarkably similar to the “golf tee” shape depicted in Figure 5 of the ’638 patent. The ’638 patent specifically notes that the “golf tee” profile indicates an “anisotropic etch.” (*Ex. 1001 at 6:61-65; see also* ¶ 60, *infra*). Since the sloped sidewalls in *Mathews* also have a “golf tee” shape, they demonstrate that the facet sputter etching in *Mathews* is an anisotropic etch process. Therefore, *Mathews* discloses claim element [8e].

g. Claim Element [8f]

99. *Mathews* discloses “depositing a material over portions of the upper surface of the dielectric layer and within the opening.” (Ex. 1001 at 8:37-38; Ex. 1004 at Abstract, 3:9-11, 3:60-4:16, 5:18-20, 6:35-40, FIGS. 6-7; see also ¶ 72, *infra*).

h. Claim Element [8g]

100. *Mathews* discloses “polishing to remove (1) the material over portions of the upper surface of the dielectric layer and (2) the top portion of the opening including the taper and portions of the material contained within the top portion.” (Ex. 1001 at 8:40-43; Ex. 1004 at Abstract, 1:45-47, 3:23-25, 4:17-50, 5:21-24, 6:41-44, FIGS. 7-8; see also ¶ 73, *infra*).

2. Claim 9

101. Claim 9 additionally recites “[t]he method of claim 8, wherein the material includes a conductive material.” (Ex. 1001 at 8:44-45).

102. In my opinion, *Mathews* anticipates Claim 9 because *Mathews* further discloses that “the material” which is deposited “over portions of the upper surface of the dielectric layer and within the opening” is a “conductive material,” such as titanium or tungsten. (Ex. 1004 at Abstract, 1:45-47, 3:23-25, 4:17-50, 5:21-24, 6:41-44, FIGS. 7, 8).

3. Claim 10

103. Claim 10 additionally recites “[t]he method of claim 9 wherein the conductive material is further characterized as a tungsten material.” (Ex. 1001 at 8:46-47).

104. In my opinion, *Mathews* anticipates Claim 10 because *Mathews* further discloses that “the conductive material” is preferably tungsten. (Ex. 1004 at 1:12-45, 1:59-2:6, 2:7-14, 4:1-5, 4:17-25, 4:33-42, 6:8-10, FIGS. 6, 7).

4. Claim 11

105. Claim 11 (Ex. 1001 at 8:48-65) recites:

A method for forming an integrated circuit, the method comprising:

[11a] patterning a resist layer over a dielectric layer;

[11b] anisotropically etching portions of the dielectric layer exposed by the resist layer

[11c] to substantially define a top portion of the opening that is adjacent an upper surface of the dielectric layer, a bottom portion of the opening that is opposite the top portion, and a sidewall portion of the opening that is disposed between the top portion and the bottom portion;

[11d] tapering the top portion of the opening using an anisotropic etch process while removing the resist layer;

[11e] depositing a material over portions of the upper surface of the dielectric layer and within the opening; and

[11f] polishing to remove the material over portions of the upper surface of the dielectric layer and the top portion of the opening including the taper and portions of the material contained within the top portion.

106. In my opinion, *Mathews* anticipates Claim 11 because it discloses each and every element of Claim 11.

107. The language of Claim 11 differs from Claim 8 in one primary respect. Claim 8 recites “tapering the top portion of the opening using an anisotropic etching process after removing of the resist layer,” but Claim 11 recites “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” (*Compare Ex. 1001 at Claim 8 with Claim 11 (emphasis added)*).

a. Preamble, Claim Elements [11a] – [11c], [11e]-[11f]

108. Claim elements [11a] – [11c] and [11e] – [11f] are identical or substantially identical to claim elements [8a] – [8c] and [8f] – [8g].⁸ For these

⁸ The language of claim element [8b-c] and claim [11c] are not identical. Claim element [8b-c] recites “to define an opening in the dielectric layer, wherein: the opening includes a top portion that is adjacent an upper surface of the dielectric layer . . .” (*Ex. 1001 at 8:25-33*). Claim element [11c] recites “to substantially define a top portion . . .” (*Ex. 1001 at 8:51-56*). In my opinion, the difference in the language does not affect the analysis.

claim elements, I refer to my opinion regarding the corresponding elements of claim 8:

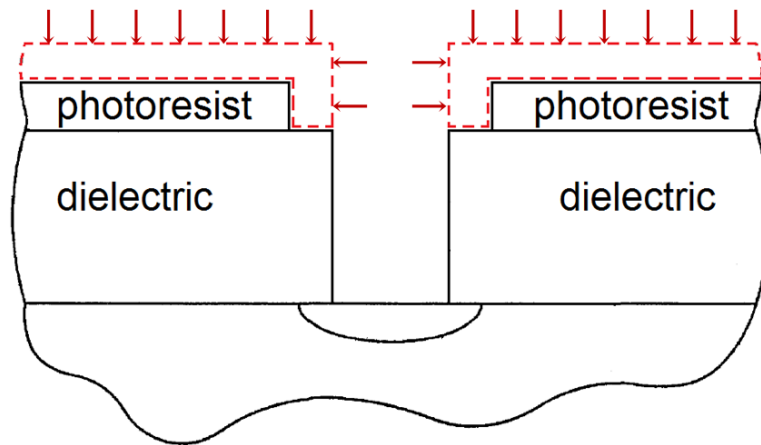
- Claim 11, Preamble: See ¶ 91, *infra* (Claim 8, Preamble)
- Claim Element [11a]: See ¶ 92, *infra* (Claim Element [8a])
- Claim Element [11b]: See ¶ 93, *infra* (Claim Element [8b])
- Claim Element [11c]: See ¶ 94, *infra* (Claim Element [8c])
- Claim Element [11e]: See ¶ 99, *infra* (Claim Element [8f])
- Claim Element [11f]: See ¶ 100, *infra* (Claim Element [8g])

b. *Claim Element [11d]*

109. *Mathews* discloses “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” (Ex. 1001 at 8:57-58 (emphasis added)). As I noted, the facet sputter etching of *Mathews* corresponds to “tapering the top portion of the opening using an anisotropic etch process.” (See ¶ 96, *infra*).

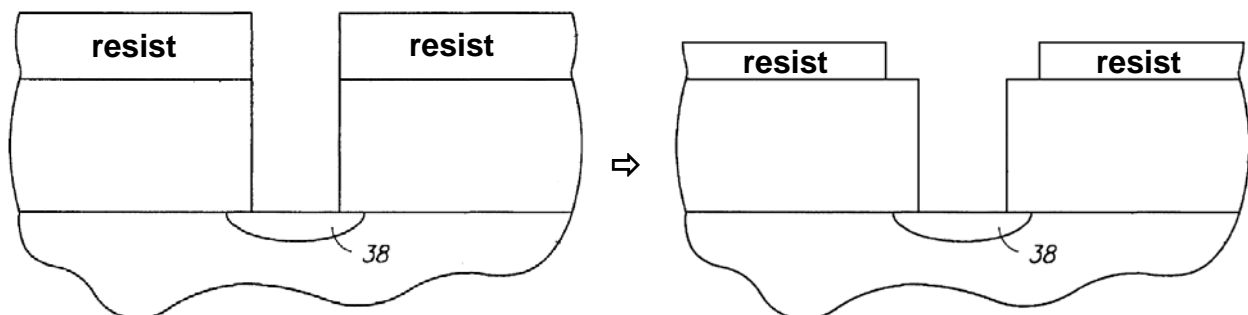
110. The facet sputter etching also simultaneously removes any resist layer on the dielectric layer. As an initial matter, *Mathews* explains that the facet sputter etching can be performed without fully stripping away the resist layer first. (Ex. 1004 at 3:45-49). *Mathews* discloses that an oxygen etch can be used to partially strip away the resist. (*Id.*). This type of resist stripping, *i.e.*, oxygen-based resist stripping, is categorized as a dry chemical etching and is isotropic in

nature. (*See ¶ 48, infra; Ex. 1008 at p. 34*). Because the oxygen-based resist stripping is isotropic, the resist would etch away at substantially uniform rates in both horizontal and vertical directions.



Partial Resist Removal According To An Embodiment Of *Mathews*

Hence, the shape of the remaining resist immediately before and after the facet sputter etch, according to one embodiment of *Mathews*, would look like the following:



Before & After Partial Resist Removal According To An Embodiment Of *Mathews*

111. The facet sputter etching disclosed in *Mathews* is a dry physical etch process. (See ¶ 42, *infra*). As I noted above, physical etching is not only highly anisotropic but also highly non-selective, *i.e.*, the etch rates for different materials do not differ substantially. (See ¶¶ 43-44, *infra*). Due to the low selectivity, dry physical etching etches away resist as well. This inherent property of sputter etching (*i.e.*, resist erosion) is well-known and well-documented. (Ex. 1008 at p. 63 (“As sputter etching is nonselective, it introduces a masking problem.”); *id.* at pp. 64-65 (discussing resist eroding property of sputter etching)).

112. Since the “facet sputter etching” disclosed in *Mathews* is a dry physical (or sputter) etch process, it would necessarily erode some or all of the resist that is present on the wafer surface. *Mathews* uses the partial removal of the resist beneficially to perform the facet etch while removing the remainder of the resist in a single anisotropic etch. (Ex. 1004 at 3:48-52 (“... move the resist back away from the contact, and not necessarily fully strip the resist . . . followed by a dry physical argon etch . . .”)). Thus, *Mathews* discloses “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” (Ex. 1001 at 8:57-58 (emphasis added))).

B. Mathews Renders Claims 8-11 Obvious

1. Claim 8

113. In my opinion, Claim 8 is obvious in view of the knowledge of one of skill in the art over *Mathews* for the same reasons I noted in ¶¶ 90-100.

2. Claim 9

114. In my opinion, Claim 9 is obvious in view of the knowledge of one of skill in the art over *Mathews* for the same reasons I noted in ¶¶ 101-02.

3. Claim 10

115. In my opinion, Claim 10 is obvious in view of the knowledge of one of skill in the art over *Mathews* for the same reasons I noted in ¶¶ 103-04.

4. Claim 11

116. To the extent Claim 11 is not anticipated by *Mathews* because *Mathews* does not disclose claim element [11d], Claim 11 is nevertheless obvious in view of the knowledge of one of skill in the art over *Mathews* because (i) *Mathews* renders claim element [11d] obvious, and (ii) *Mathews* discloses all other elements of Claim 11, as I noted in ¶¶ 105-12.

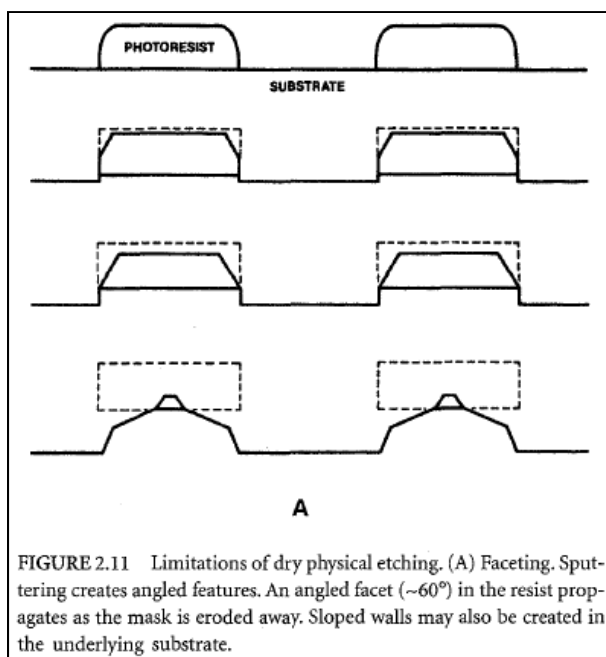
a. Claim Element [11d]

117. Claim 11 recites [11d] “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” (Ex. 1001 8:57-58).

118. As I noted, *Mathews* discloses facet sputter etching the corners of the contact opening, which corresponds to “tapering the top portion of the opening using an anisotropic etch process.” (See ¶ 95, 108, *infra*).

119. In one embodiment of *Mathews*, the resist layer is not completely stripped away prior to the facet sputter etch process. (Ex. 1004 at 3:45-49). Hence, according to one embodiment, portions of the resist layer will be present on the surface of the wafer when the facet sputter etching step begins.

120. A person of ordinary skill in the art would have understood the advantage of stripping away the resist adjacent the contact holes only and not etching the entire layer of resist. In addition to its inherent ability to etch the resist (See ¶ 110, *infra*), sputter etching also has an inherent tendency to create facets on a layer, such as at the corners or edges of a layer (See ¶ 45, *infra*). This is due to the high sensitivity of sputter etching to the angle of incidence; if the angle of incidence decreases, the etch rate increases (up to a critical angle). (See ¶ 45, *infra*; Ex. 1008 at p. 64). At the edges or corners of a layer, the ions will collide at a smaller angle of incidence and etch the edges or corners at a higher rate than the flat surface regions. (Ex. 1008 at p. 64). The difference in the etch rates creates facets. (*Id.*).



Ex. 1008 at FIG. 2.11A (p. 64): “Faceting” In Sputter Etching

121. Exposing the edges of the oxide layer by stripping a portion of the resist maximizes the faceting feature of sputter etching. If the resist covers the entire oxide layer, as shown above, the facet will not begin to form on the oxide (labeled “substrate”) until sputter etching removes the resist layer near the edges. This is inefficient and requires significant energy because sputter etching is much slower than dry chemical etching. (Ex. 1008 at Table 2.1 (p. 54); (p.63) (noting that sputter etch is “unselective and slow”)). On the other hand, removing the entire layer of resist to expose all of the oxide is also inefficient. While the faceting will begin on the oxide immediately, the speed of the facet formation will be offset by the speed at which the flat surface of the oxide recedes as it is etched simultaneously. This method also requires forming a thicker oxide layer to

account for the layer of oxide that would be removed during sputter etching. In contrast, if only the resist near the edges are removed prior to sputter etching, faceting on the edges of the oxide layer will begin immediately and, furthermore, the resist will protect the flat surface of the oxide from being etched vertically.

122. Knowing the inherent properties of sputter etching, a person of ordinary skill in the art would have understood the advantages of only partially removing the resist. In light of the advantage, a person of ordinary skill in the art would have been motivated to remove a portion of the resist layer near the contact hole to expose the edges of the oxide layer before conducting a sputter etch.

123. Therefore, in my opinion, Claim 11 is obvious in view of the knowledge of one of skill in the art over *Mathews*.

C. *Mathews* In View Of *Langley* Renders Claims 1-7 And Claim 11 Obvious

124. In my opinion, *Mathews* and *Langley*, when combined, disclose each and every element of Claims 1-7 and 11. Furthermore, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Langley* with *Mathews*, as noted in the paragraphs below. Therefore, in my opinion, Claims 1-7 and 11 are obvious over *Mathews* in view of *Langley*.

1. Motivation To Combine *Mathews* With *Langley*

125. In my opinion, a person of ordinary skill in the art at the time of the invention would have been motivated to combine the specific teachings of *Langley* with *Mathews*.

126. A person of ordinary skill in the art at the time of the invention, such as a process designer in the 1990s, would have been motivated to combine the etching steps disclosed in *Langley* with the CMP method disclosed in *Mathews*. As I noted, CMP processing replaced the traditional conformal process as the technology for creating interconnect layers. (See ¶ 29, *infra*). However, other aspects of semiconductor fabrication from the conformal process era were compatible with the CMP process, such as metallization and etching. Hence, process designers in the 1990s developed technologies that combined earlier etching, metallization, and other processing technologies with the CMP process. *Langley* discloses an etch technology for a conformal process while *Mathews* discloses an etch technology for a CMP process. Thus, a person of ordinary skill in the art would have found that combining the prior art etching techniques in *Langley* to the known methods in *Mathews* to yield the predictable results of improved (void-free) metal interconnects would have been obvious.

127. Additionally, *Langley* and *Mathews* are directed to the same field and problem and propose solutions that are interchangeable. Both relate to improved

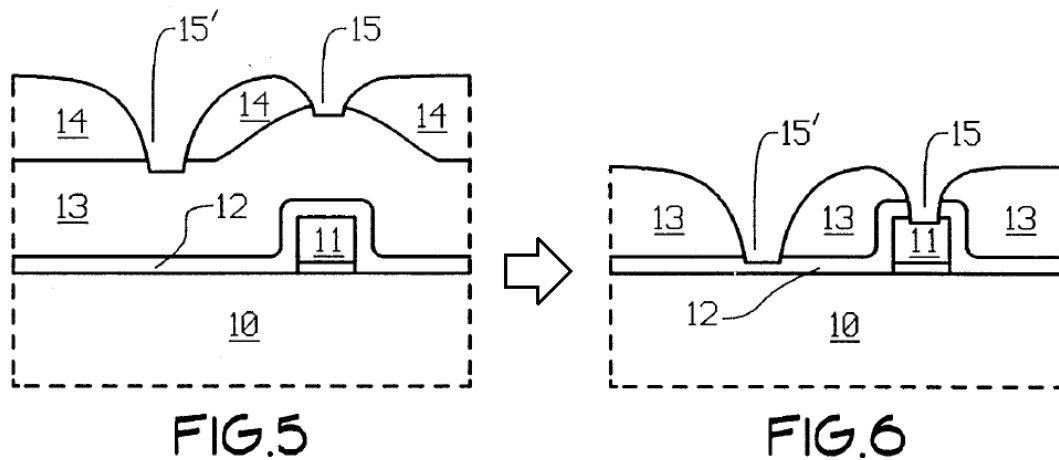
methods for forming metal interconnects in integrated circuits, and in particular, creating sloped sidewalls in the contact holes to reduce or eliminate cusp formation inside metal depositions. (Ex. 1004 at Abstract, 4:11-16; Ex. 1005 at Abstract, 1:51-60). Both propose steps for forming sloped sidewalls in the contact holes that use dry plasma etch processes. (Ex. 1004 at 3:40-47; Ex. 1005 at 3:36-4:20). Both disclose and suggest common reactive etchants (*e.g.*, CF₄ and CHF₃) for the dielectric etch (Ex. 1004 at 3:33-37; Ex. 1005 at 3:48-4:20), and both prefer performing all etching steps in a single reactive chamber (Ex. 1004 at 3:55-57; Ex. 1005 at 3:27-30). Thus, it would have been a simple substitution for a person of ordinary skill in the art to replace one or more known etch process steps in *Langley* for similar etch process steps in *Mathews*, which were also known.

2. Claim 11

128. To the extent Claim 11 is not anticipated or rendered obvious by *Mathews* because it does not disclose claim element [11d] or render claim element [11d] obvious, Claim 11 is nevertheless obvious over *Mathews* in view of *Langley* because: (i) *Langley* discloses claim element [11d]; and (ii) a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Langley* with *Mathews*, as I noted in ¶¶ 124-27.

a. Claim Element [11d]

129. Claim 11 recites [11d] “tapering the top portion of the opening using an anisotropic etch process while removing the resist layer.” (Ex. 1001 at 8:57-58 (emphasis added)). *Langley* discloses a four-step etch process for forming a contact hole with sloped sidewalls. In the second step of *Langley*, the oxide layers (13) and the resist layer (14) are etched simultaneously and at an equal (1:1) ratio, as shown below. (Ex. 1005 at 3:48-51, FIGS. 5-6). Hence, *Langley* discloses “tapering the top portion of the opening . . . while removing the resist layer.” (Ex. 1001 at 8:57-58 (emphasis added)).



Langley (Ex. 1005) at FIGS. 5-6: Residual Resist & Oxide Etch

130. Further, this second step disclosed in *Langley* is an anisotropic etch process. The shape of the etch profile in Figure 6 matches the “golf tee” profile in Figure 5 of the ‘638 patent.

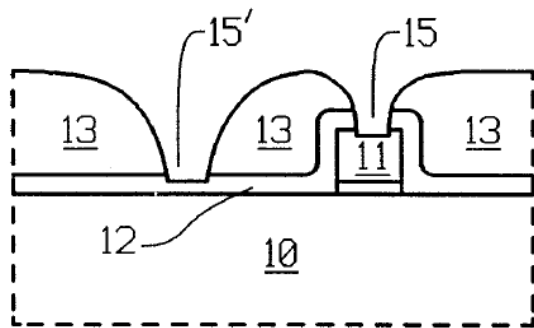


FIG. 6

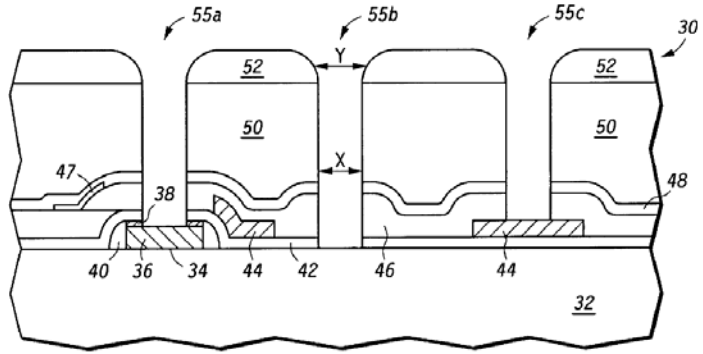
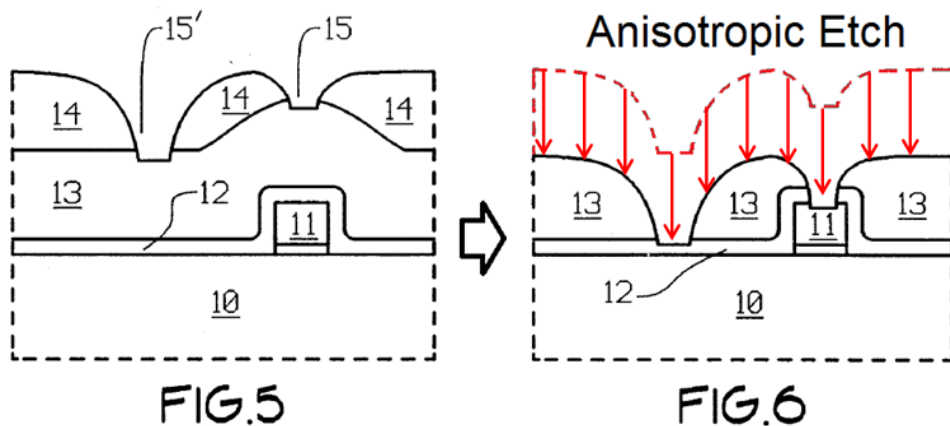


FIG. 5

Ex. 1005 at FIG. 6 Versus Ex. 1001 at FIG. 5:

Comparison of “Golf Tee” Profile

Since the '638 patent states that the “golf tee” profile is indicative of an anisotropic etch process, the result of the second step is also evidence of an anisotropic etch process. (Ex. 1001 at 6:61-65; see also ¶ 59, *infra*). Therefore, *Langley* discloses this claim element.



Langley (Ex. 1005) at FIGS. 5-6 (Annotated): Anisotropic Etch

131. Furthermore, the second step of *Langley* is an anisotropic etch process because the layers are etched in the vertical direction to preserve the slope that was

originally formed on the resist layer, as shown in the edited figure above. As shown, the resist and oxide layers are etched downward and the shape of the surface at the beginning of step two is retained at the end of this etch. (Ex. 1005 at FIGS. 5-6). As I noted, such a directional etch is anisotropic. (See ¶¶ 54-58, *infra*).

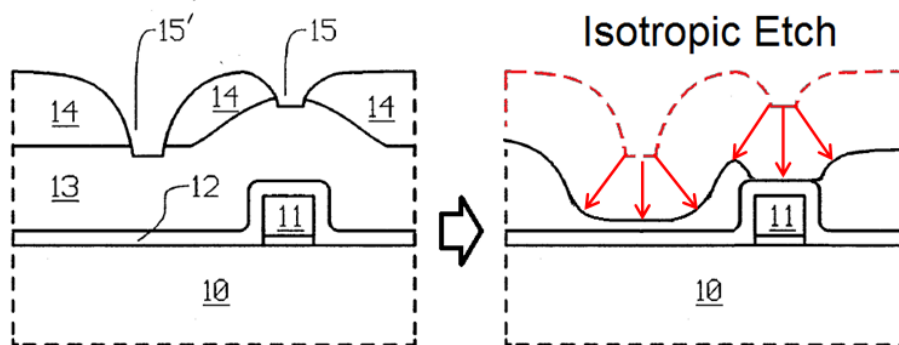


FIG.5

Langley (Ex. 1005): Result of Isotropic Resist & Oxide Etch (Annotated)

132. The edited and annotated figure above further illustrates why the second etch step in *Langley* is necessarily an anisotropic etch process. If the second etch step—*i.e.*, removing residual resist and oxide layer simultaneously at a 1:1 etch ratio—were performed isotropically, the resist and the oxide layer would be eroded both vertically and horizontally. Consequently, an isotropic etch would not maintain the original shape of the layer.

133. Therefore, the second etch step disclosed in *Langley* is an anisotropic etch process.

3. Claim 1

134. Claim 1 (Ex. 1001 at 7:33-67) recites:

1. A method for forming a contact structure, the method comprising the steps of:

[1a] forming a first conductive material overlying a semiconductor substrate;

[1b] forming a dielectric layer overlying the first conductive layer;

[1c] forming a resist layer over the dielectric layer;

[1d] patterning the resist layer to form an opening that exposes portions of the dielectric layer;

[1e] placing the semiconductor substrate into a reactive ion etching chamber and in-situ processing the semiconductor substrate as follows:

[1f] etching portions of the dielectric layer using a gas mixture that includes a fluorocarbon source gas to form an opening in the dielectric layer, the opening having a bottom portion and a sidewall portion;

[1g] etching a portion of the resist layer using a gas mixture that includes a fluorocarbon source gas and an oxygen source gas to remove the portion of the resist layer and expose a top surface portion of the dielectric layer adjacent the sidewall portion;

[1h] etching the top surface portion of the dielectric layer adjacent the sidewall portion to form a taper that extends between a top surface of the dielectric layer and the

sidewall portion, wherein the taper towards the top surface portion has a radius Y and the taper towards the sidewall portion has a radius X wherein $X < Y$; and
[1i] removing remaining portions of the resist layer;
[1j] depositing a second conductive material within the opening; and
[1k] polishing away a top portion of the conductive material and a top portion of the dielectric layer to remove the taper.

135. In my opinion, Claim 1 is obvious over *Mathews* in view of *Langley* because: (i) *Mathews* and *Langley*, when combined, disclose each and every element of Claim 1; and (ii) a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Langley* with *Mathews*, as I noted in ¶¶ 125-27.

a. Preamble, Claim Elements [1b]-[1d], [1h]-[1k]

136. Claim elements [1b]-[1d] and [1h]-[1k] are identical to, substantially identical to, or encompassed by claim elements [8a], [8e], [11d], [8f], and [8g]. For each of the following elements of Claim 1, I refer to my opinion regarding the corresponding elements of Claims 8 and 11:

- Claim 1, Preamble: See ¶ 91, *infra* (Claim 8, Preamble)
- Claim Element [1b]: See ¶ 92, *infra* (Claim Element [8a])
- Claim Element [1c]: See ¶ 92, *infra* (Claim Element [8a])

- Claim Element [1d]: See ¶ 92, *infra* (Claim Element [8a])
- Claim Element [1h]: See ¶¶ 96-98, *infra* (Claim Element [8e])
- Claim Element [1i]: See ¶¶ 109-12, 116-22, *infra* (Claim Element [11d])
- Claim Element [1j]: See ¶ 99, *infra* (Claim Element [8f])
- Claim Element [1k]: See ¶ 100, *infra* (Claim Element [8g])

b. *Claim Element [1a]*

137. *Mathews* discloses “forming a first conductive material overlying a semiconductor substrate.” (Ex. 1001 at 7:35-36; Ex. 1004 at Abstract, 2:57-58, 3:16-21, 4:66-67, 6:15-16). *Mathews* discloses that an active region is formed within a substrate, which includes the *source and drain regions* (including the source and drain electrodes) that are formed by doping the substrate with impurities. (Ex. 1004 at FIG. 4; see also ¶ 70, *infra*). The active area 38 is likely either the source or drain since a contact opening 44 is being formed through “which electrical connection is to be made” with the active area. (Ex. 1004 at FIG. 4; 3:16-32; FIG. 1; 1:12-36 (“[S]ubstrate includes a dopant diffusion/active region 16 to which electrical connection is to be made.”)).

138. Claim 7 of the ’638 patent, which is dependent on Claim 1, recites “. . . forming the first conductive layer as a doped current electrode for a transistor *within a substrate.*” (Ex. 1001 at 8:18-21 (Claim 7) (emphasis added)). Because

Claim 1 encompasses Claim 7, the process of “forming a first conductive [layer] *overlying* a semiconductor substrate” must necessarily encompass “forming the first conductive layer . . . *within* a substrate.” (Ex. 1001 at 7:35-36, 8:18-21 (emphasis added)). Accordingly, the active region depicted in Figure 4 of *Mathews* formed “within” the substrate is also encompassed by (and satisfies) the “overlying” requirement of claim element [1a]. Thus, *Mathews* discloses claim element [1a]. (Ex. 1004 at FIG. 4; 3:16-32; FIG. 1; 1:12-36)

139. In my opinion, *Langley* also discloses “forming a first conductive material overlying a semiconductor substrate.” (Ex. 1001 at 7:35-36; Ex. 1005 at Figs. 4-7). Figures 4-7 of *Langley* show a polysilicon layer (11), which is *a gate*, being formed over the substrate (10). A contact (15) is formed with the polysilicon layer (11) by etching the resist (14) and the oxide layers (13, 12). (Ex. 1005 at FIGS. 4-7). Therefore, the polysilicon layer (11) is “a first conductive material overlying a semiconductor substrate.” (Ex. 1001 at 7:35-36).

140. Furthermore, as I noted, a person of ordinary skill in the art would have been motivated to combine *Mathews* with *Langley*. (See ¶¶ 124-27, *infra*). In addition, with respect to claim element [1a] (“a first conductive material”), *Mathews* and *Langley* simply use different parts of a semiconductor device as an example—*i.e.*, *Mathews* uses the source or drain region as an example to show how to form a via on an integrated circuit, whereas *Langley* uses the gate electrode

as an example. Therefore, it would have been obvious to a person of ordinary skill in the art that if a via can be formed on the source or drain of a device, it can also be formed on the gate, and vice versa.

c. Claim Element [1e]

141. Both *Mathews* and *Langley* disclose “placing the semiconductor substrate into a reactive ion etching chamber and in-situ processing the semiconductor substrate.” (Ex. 1001 at 7:42-44).

142. *Mathews* explains that all mask stripping and etching are preferably conducted in the same chamber, which can be reactive. (Ex. 1004 at 3:54-46, 3:44-46). Further, various etchants are used for the etching and resist stripping in *Mathews*. For example, CF_4 and CHF_3 , which have high selectivity for oxide, are used for etching the oxide layer. (Ex. 1004 at 3:33-37).

143. *Langley* also states that “[t]he preferred method includes four timed etch steps in a single Lam 790 parallel plate plasma etch reactor, having an inert cathode such as anodized aluminum, and an anode on which substrate 10 is mounted.” (Ex. 1005 at 3:27-30). Hence, the chamber referenced in *Langley* is a reactive ion chamber.

144. That both *Mathews* and *Langley* disclose, as one embodiment, performing all etching and resist removal steps in a single reactive chamber further

demonstrates that the etching and resist removal steps proposed in these references are compatible with the other.

d. Claim Element [1f]

145. *Mathews* discloses “etching portions of the dielectric layer using a gas mixture that includes a fluorocarbon source gas to form an opening in the dielectric layer, the opening having a bottom portion and a sidewall portion.” (Ex. 1001 at 7:46-49). *Mathews* discloses conducting a “dry etch using a carbon/fluorene based chemistry, e.g., CF₄, CHF₃, and Ar,” *i.e.*, fluorocarbons, to form the vertical contact hole in the dielectric layer. (Ex. 1004 at 3:45-47, 3:33-35). As I noted, the contact hole has a bottom portion, sidewall portion, and a top portion. (See ¶ 94, *infra*). Therefore, *Mathews* discloses claim element [1f].

e. Claim Element [1g]

146. *Langley* discloses “etching a portion of the resist layer using a gas mixture that includes a fluorocarbon source gas and an oxygen source gas to remove the portion of the resist layer and expose a top surface portion of the dielectric layer adjacent the sidewall portion.” (Ex. 1001 at 7:50-54). *Langley* discloses that, in the first of the four etch steps, “a chamber atmosphere of O₂, He, CHF₃, and CF₄ is provided, widening, or forming slopes in, contacts 15 and 15’ by eroding resist 14.” (Ex. 1005 at 3:36-38). Therefore, *Langley* discloses claim element [1g].

147. Furthermore, as I noted, a person of ordinary skill in the art would have been motivated to combine this first step of *Langley* (i.e., partial resist erosion step) with *Mathews*. (See ¶¶ 124-27, *infra*).

148. In my opinion, *Mathew* further renders claim element [1g] obvious. *Mathews* states that “an oxygen etch is conducted to strip the resist and pull it away from the edge of the contact,” after a “dry etch using a carbon/fluorene based chemistry, e.g., CF₄, CHF₃, and Ar” is conducted to form the vertical contact hole. (Ex. 1004 at 3:44-48, 3:34-36). Because fluorocarbon gas was readily available for use in the chamber, it would have been obvious for a person of ordinary skill in the art to try adding oxygen to the fluorocarbon gas in the chamber (for the resist etch) instead of completely evacuating the fluorocarbon gas. In fact, it would have been simpler for a person of ordinary skill in the art to forego the evacuation step. Hence, a person of ordinary skill in the art would have been motivated to try adding CF₄ and CHF₃ to the O₂ gas mixture during the partial resist stripping process. Therefore, *Mathews* in view of *Langley* renders claim element [1g] obvious.

4. Claim 2

149. In my opinion, Claim 2 is also obvious over *Mathews* in view of *Langley* because *Mathews* additionally discloses that “the second conductive

material comprises tungsten.” (Ex. 1001 at 8:1-2; Ex. 1004 at 1:12-45, 1:59-2:6, 2:7-14, 4:1-5, 4:17-25, 4:33-42, 6:8-10, FIGS. 6-7).

5. Claim 3

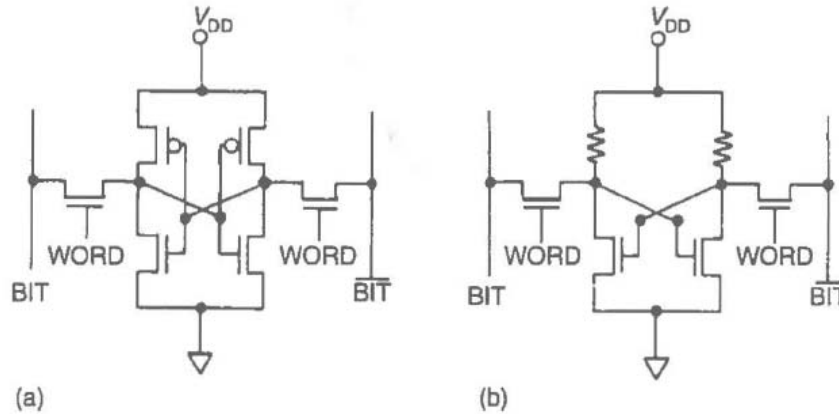
150. In my opinion, Claim 3 is also obvious over *Mathews* in view of *Langley* because *Mathews* and *Langley* each disclose “removing remaining portions of the resist layer is performed as part of in situ-processing in the reactive ion etching chamber.” (Ex. 1001 at 8:3-5; Ex. 1004 at 3:54-56; *Langley* at 3:27-28).

6. Claim 4

151. In my opinion, Claim 4 is also obvious over *Mathews* in view of *Langley* because *Mathews* discloses “using the top portion of the opening having the radius Y to reduce void formation in the contact structure due to the step of depositing.” (Ex. 1001 at 8:6-9; Ex. 1004 at 1:37-45, 1:59-2:6, 3:59-4:32, Figures 1-3, Figures 7-8).

7. Claim 5

152. In my opinion, Claim 5 is also obvious over *Mathews* in view of *Langley* because “forming the first conductive layer as a gate electrode which gates a transistor in an SRAM cell” would have been obvious to a person of ordinary skill in the art in light of *Mathews* and *Langley*. (Ex. 1001 at 8:10-13).



“Semiconductor Memories” (Ex. 1014) at FIG. 2-4 (a)-(b) (p.13)

153. As with all MOS circuits, an SRAM cell consist of a number of MOS transistors, each having a doped source, a doped drain and a gate. The gate electrodes of the storage transistors in an SRAM cell are coupled to at least two other regions—the drain of one or more opposing storage transistors and the drain/source of one or more access transistors. (See ¶¶ 61-63, *infra*; Ex. 1014 at FIGS. 2-3, 2-4). Therefore, a person of ordinary skill in the art would have understood that metal interconnects could be used to couple these three regions. Moreover, a person of ordinary skill in the art would have understood that gate electrodes are formed on, and therefore “overl[ie]” the substrate.

154. Furthermore, Claim 5 does not recite any limitations that are particularly suited for or applicable to an SRAM. The ‘686 patent states that the method for forming a contact “may also be used in microprocessors, other memory devices (i.e., EEPROM, EPROM, DRAM, ferroelectric devices, flash memory, etc.) or *any semiconductor device fabrication process using plug contacts.*”) (Ex. 1001

at 6:27-31 (emphasis added)). Therefore, it would have been obvious for a person of ordinary skill in the art to apply the teachings of *Mathews* and *Langley* to an SRAM cell.

155. Accordingly, Claim 5 would have been obvious to a person of ordinary skill in the art in light of his or her background knowledge regarding the structure of an SRAM cell and a MOS transistor.

8. Claim 6

156. In my opinion, Claim 6 is also obvious over *Mathews* in view of *Langley* because “forming the first conductive layer . . . [as] a polysilicon layer which is coupled to a storage node of an SRAM cell” would have been obvious to a person of ordinary skill in the art. (Ex. 1001 at 8:14-17).

157. A person of ordinary skill in the art would have known that the gate electrodes of the storage transistors in an SRAM cell are coupled to form the storage node. (See ¶¶ 61-65, *infra*). A person of ordinary skill in the art also would have known that the gate electrodes are commonly fabricated from polysilicon.

158. Furthermore, as I noted, it would have been obvious for a person of ordinary skill in the art to apply the teachings of *Mathews* and *Langley* to an SRAM cell. (See ¶¶ 152-55, *infra*).

159. Hence, Claim 6 would have been obvious to a person of ordinary skill in the art in light of his or her background knowledge regarding the structure of an SRAM cell and a MOS transistor.

9. Claim 7

160. In my opinion, Claim 7 is also obvious over *Mathews* in view of *Langley* because “forming the first conductive layer as a doped current electrode for a transistor within a substrate, the transistor being coupled in an SRAM cell” would have been obvious to a person of ordinary skill in the art. (Ex. 1001 at 8:18-21).

161. In my opinion, as discussed in paragraph 67, the term “current electrode” means “a current conducting electrode in a transistor, such as a source or drain electrode.”. (Ex. 1001 at 3:25-27 (equating “current electrode” with source and drain); see ¶ 67, *infra*). A person of ordinary skill in the art would have known that the source and drain electrodes of a MOS transistor are formed in or on the substrate and are doped according to the transistor type (n-doped for NMOS and p-doped for PMOS). A person of ordinary skill in the art would also have known that the drains of storage transistors are coupled to at least two other regions—the gate of opposing storage transistors and the source/drain of access transistors. (Ex. 1014 at FIG. 2-4 (p. 13)). A person of ordinary skill in the art

would have known that the drain regions of storage transistors could be coupled together using a metal interconnect.

162. Furthermore, as I noted, it would have been obvious for a person of ordinary skill in the art to apply the teachings of *Mathews* and *Langley* to an SRAM cell. (*See* ¶¶ 152-155, *infra*).

163. Hence, Claim 7 would have been obvious to a person of ordinary skill in the art in light of his or her background knowledge regarding the structure of an SRAM cell and a MOS transistor.

D. *Mathews In View Of Langley And Wu* Renders Claims 1-7 Obvious

164. In my opinion, *Mathews*, *Langley*, and *Wu*, when combined, disclose each and every element of Claims 1-7 and 11. Furthermore, in my opinion, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Mathews* and *Langley* with *Wu*. Therefore, in my opinion, Claims 1-7 and 11 would have been obvious to a person of ordinary skill in the art in light of *Mathews*, *Langley*, and *Wu*.

1. Motivation To Combine *Mathews* And *Langley* With *Wuu*

165. In my opinion, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Mathews* and *Langley* in implementing the SRAM structures disclosed in *Wuu*.

166. *Wuu* proposes forming a contact node in an SRAM cell using a tungsten plug (Ex. 1006 at 3:44-47, FIG. 9) and “conformally” filling the plugs with tungsten. (Ex. 1006 at 7:4-9). The problem with this approach, as the ’638 patent and *Mathews* (and *Langley*) point out, is that tungsten is not well-suited for conformal deposition. (Ex. 1001 at 1:29-32; Ex. 1004 at 1:37-45). As such, voids would likely form inside the tungsten plugs fabricated according to the teachings of *Wuu*. (Ex. 1001 at FIGS. 1-2; Ex. 1004 at FIG. 1). This frustrates the purpose of *Wuu*, which is to provide a low-resistance contact node, because the voids could prevent the layers from making proper contact with the tungsten plug.

167. A person of ordinary skill in the art practicing *Wuu* would have understood and sought solutions to this problem. Because *Mathews* and *Langley* provide a solution, a person of ordinary skill in the art practicing *Wuu* would have been motivated to apply the specific etching and CMP techniques of *Mathews* and *Langley* to *Wuu*.

2. Claim 1

168. In my opinion, Claim 1 is obvious over *Mathews* in view of *Langley* and *Wuu* for the same reason Claim 1 is obvious over *Mathews* in view of *Langley*. (See ¶¶ 134-48, *infra*).

3. Claim 2

169. In my opinion, Claim 2 is obvious over *Mathews* in view of *Langley* and *Wuu* for the same reason Claim 2 is obvious over *Mathews* in view of *Langley*. (See ¶ 149, *infra*).

4. Claim 3

170. In my opinion, Claim 3 is obvious over *Mathews* in view of *Langley* and *Wuu* for the same reason Claim 3 is obvious over *Mathews* in view of *Langley*. (See ¶ 150, *infra*).

5. Claim 4

171. In my opinion, Claim 3 is obvious over *Mathews* in view of *Langley* and *Wuu* for the same reason Claim 3 is obvious over *Mathews* in view of *Langley*. (See ¶ 151, *infra*).

6. Claim 5

172. Claim 5 recites “the step of forming the first conductive layer comprises forming the first conductive layer as a gate electrode which gates a transistor in an SRAM cell.” (Ex. 1001 at 8:10-13). Here, the conductive layer “overl[ies] a semiconductor substrate.” (Ex. 1001 at 7:35-36).

173. In my opinion, Claim 5 is also obvious over *Mathews* in view of *Langley* and *Wuu* because (i) *Wuu* discloses claim 5 and (ii) a person of ordinary skill in the art would have been motivated to apply the specific techniques of *Mathews* and *Langley* to *Wuu*.

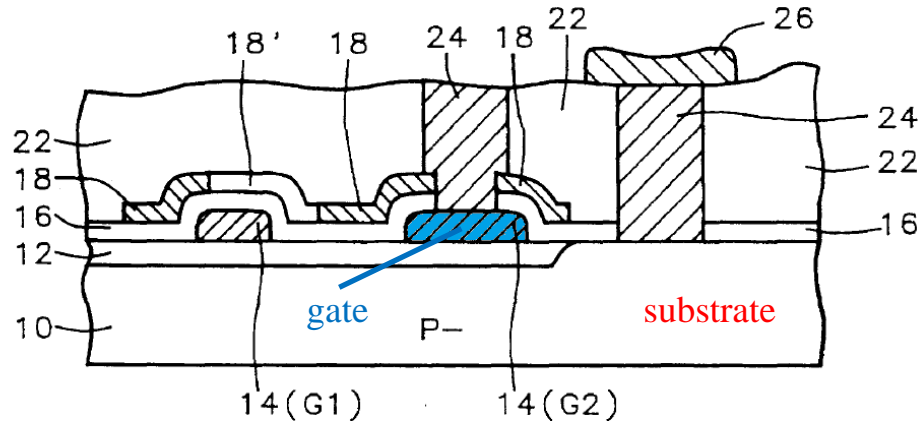


FIG. 9

Wuu (Ex. 1006) at FIG. 9: Cross Section of an SRAM Cell (Annotated)

174. The gate electrode **G2** in FIG. 9 of *Wuu* corresponds to “the conductive layer” because the gate electrode **G2** is formed on the substrate 10. The gate electrode **G2** gates one of the storage transistors in an SRAM cell. (Ex. 1006 at FIGS. 1, 9. Therefore, *Wuu* discloses Claim 5.

175. As I noted above, a person of ordinary skill in the art would have been motivated to apply the specific teachings of *Mathews* and *Langley* to *Wuu*. (See ¶¶ 164-68, *infra*).

176. Therefore, claim 5 is obvious over *Mathews* in view of *Langley* and *Wuu*.

7. Claim 6

177. Claim 6 recites “the first conductive layer is . . . a poly-silicon layer which is coupled to a storage node of an SRAM cell.” (Ex. 1001 at 8:14-17).

178. In my opinion, (i) *Wuu* discloses claim 5 and (ii) a person of ordinary skill in the art would have been motivated to apply the specific techniques of *Mathews* and *Langley* to *Wuu*.

179. As I noted, “a storage node of an SRAM cell” is a node of the storage transistors of an SRAM cell where the data (or its complement) is stored. (See ¶¶ 61-65, *infra*).

180. The gate electrode **G2** is “patterned form an N+ doped [] *polysilicon* layer 14.” (Ex. 1006 at 2:5-7, 6:4-8). G2 is also in contact with the contact plug 24, which forms the storage node **Q1**. (Ex. 1006 at FIG. 1). Therefore, the gate electrode G2 corresponds to “the first conductive layer,” as recited in Claim 6.

181. As I noted above, a person of ordinary skill in the art would have been motivated to apply the specific teachings of *Mathews* and *Langley* to *Wuu*. (See ¶¶ 164-68, *infra*).

182. Therefore, claim 6 is obvious over *Mathews* in view of *Langley* and *Wuu*.

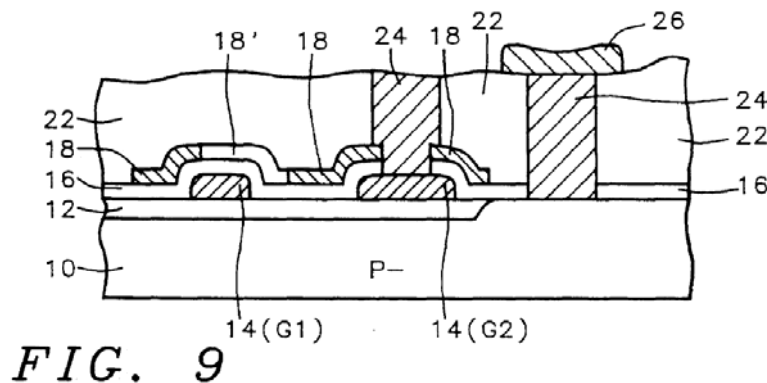
8. Claim 7

183. Claim 7 recites “forming the first conductive layer as a doped current electrode for a transistor within a substrate, the transistor being coupled in an SRAM cell.” (Ex. 1001 at 8:18-21).

184. In my opinion, Claim 7 is obvious over *Mathews* in view of *Langley* and *Wuu* because *Wuu* discloses claim 7.

185. As I noted, a “current electrode” includes the drain and the source. (*See* ¶ 67, *infra*).

186. Layer 18 in FIG. 9 of *Wuu* is “subjected to an ion implantation using a P type dopant” which “forms the source/drain doped regions of the P-channel TFTs.” (Ex. 1006 at 6:3-8).



Wuu (Ex. 1006) at Figure 9

187. Furthermore, as I noted, a person of ordinary skill in the art would have been motivated to combine the specific teachings of *Mathews* and *Langley* to *Wuu*. (*See* ¶¶ 164-68, *infra*).

188. Therefore, claim 7 is obvious over *Mathews* in view of *Langley* and *Wuu*.

VIII. AVAILABILITY FOR CROSS-EXAMINATION

189. *In signing this declaration*, I recognize that the declaration may be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will cooperate to the best of my ability to appear for cross examination within the United States during the time allotted for cross examination.

IX. RIGHT TO SUPPLEMENT

190. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available to me.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 5/5/2016

A handwritten signature in blue ink, appearing to read "Martin G. Walker", written over a horizontal line.

Martin G. Walker

Appendix A

Martin G. Walker, PhD

Consultant Curriculum Vitae

Expertise

IC Design

- EDA Software
- Digital circuit design and simulation
- Analog IC design and analysis
- Analog circuit design
- RF and microwave circuit design

Source Code

- Identification of copied source code
 - Analysis of copied source code
 - Analysis of alleged trade secret misappropriation
 - Patent infringement of source code
 - Copyright infringement of source code, including database schemas
-

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650-331-0200

Litigation Experience

Dr. Walker has testified in jury trials and arbitration involving software technology issues, including testifying in federal court and the ITC on matters relating to infringement and validity of various patents as well as misappropriation of trade secrets. He has been engaged as a “technology neutral” to assist in the resolution and adjudication of electronic discovery issues. Dr. Walker is particularly adept at explaining complex technology issues to lay audiences and, as such, has often been asked to present Markman tutorials and prepare demonstratives for arguments as well as his testimony. He regularly works with attorneys to help articulate and manage the many technology issues that arise in complex litigation.

Industry Experience

Dr. Walker is a recognized expert with over 40-years of experience in design of integrated circuits, including analog, digital and RF/microwave circuits. His analog IC circuit design experience includes analog components such as PLLs, voltage regulators/controllers and linear systems. In the digital IC design Dr. Walker has experience at the circuit level, including such structures as ESD components, level shifters, sense amps, SDRAM circuits such as DDR sequencing circuits and On-Die Termination (ODT). His RF/Microwave design experience includes microwave components (such as amplifiers, oscillators, mixers and switches) as well as sub-systems (tuners, low-noise down converters, etc).

Martin G. Walker, PhD

Consultant Curriculum Vitae

Dr. Walker has over 25 years experience in electronic design automation (EDA) software systems, simulation and circuit design and modeling. He is a recognized expert in the field of EDA systems, simulation, and modeling. He also has experience with the design of digital and analog IC, with verilog and VHDL analysis, synthesis of digital ICs such as flash memory controllers, analyses and verification of metal interconnects and related process technology.

During his consulting career, Dr. Walker has gained experience with smart-phone applications and system-level programming and integration with underlying hardware. For example, he has analyzed operation of Android and iOS systems to determine their functionality and analyze whether the functionality meets the claim limitations of cellular technology patents. For example, he has analyzed WiFi and cellular data communications, including the interfaces between the handset operating system and the WiFi and cellular chip sets.

Additionally, Dr. Walker has analyzed the operation of cellular modems, including hardware, firmware, and software to determine the operation of the modems as they related to various 3GPP, CDMA2000, and LTE cellular communication standards.

During the course of his practice, Dr. Walker has analyzed such diverse code as EDA software, VoIP software, database schema, mail-list processing software, speech-recognition systems and stock-brokerage software. He is familiar with a wide variety of source-code repositories including CVS, RCS, Subversion, Perforce, and Rational ClearCase.

Dr. Walker has also performed numerous analyses of systems-on-a-chip. The operation of such ICs is often defined by a combination of hardware and software. The hardware is usually specified at the RTL level in Verilog or VHDL. This hardware is often controlled by software running on an embedded processor, such as an ARM. He has been asked to understand, analyze, and document the operation of the system in the context of patent infringement or (in the case of potential prior art) invalidity. For example, he has investigated implementation of signal processing algorithms that implement 3GPP cellular telephone standards on baseband modem ICs.

Martin G. Walker, PhD
Consultant Curriculum Vitae

Litigation Projects

Matter	Sequence Design vs various defendants
Description	Patent infringement – pre-litigation investigation (EDA Software)
Law Firm	Thelen Reid
Client	Sequence Design
Status	Settled
Dates	2000-02
Matter	Silvaco v CSI
Description	Misappropriation of Trade Secrets; source code analysis (EDA Software)
Law Firm	Dechert, LLP
Client	Silvaco
Status	Settled
Dates	2001-03
Testimony	Multiple depositions; Testified at arbitration; Testified at trial
Matter	IRS v Taxpayer
Description	Analysis for tax purposes of EDA software valuation and associated royalty streams. Provided expert report.
Law Firm	FTI Teklicon (for IRS)
Client	IRS
Status	Completed
Dates	2001-02
Matter	Synopsys vs Nassda
Description	Patent infringement; misappropriation of trade secrets (EDA Software). Provided expert report and declarations. Analyzed evidence of electronic document spoliation.
Law Firm	Dechert LLP
Client	Synopsys
Status	Settled
Dates	2001-04
Testimony	Deposition
Matter	Aprés v Ho
Description	Misappropriation of trade secrets related to EDA software
Law Firm	Law offices of Al Reynaldo (for cross-defendant Après)
Client	Aprés
Status	Settled
Dates	2003
Testimony	Trial
Matter	HCL vs eKomas
Description	Analysis and identification of directly copied source code written in a

Martin G. Walker, PhD

Consultant Curriculum Vitae

	web-host scripting language. The product at issue is a web-based application for loan management.
Law Firm	Dechert
Client	HCL
Status	Settled
Dates	2003-04
Matter	Tera Systems vs InTime Software
Description	Patent infringement related to EDA software. Researched invalidity and supported claim construction.
Law Firm	McDermott
Client	InTime Software
Status	Settled
Dates	2004
Matter	Siliconix vs AATI
Description	Patent infringement regarding method for manufacturing a semiconductor device. Support for claim construction and invalidity analysis. Researched prior art.
Law Firm	Dechert LLP
Client	AATI
Status	Settled
Dates	2004-05
Matter	Berry vs Fleming, et al.
Description	Source code copyright and misappropriation of trade secrets of an SQL database schema as well as associated source code. Reviewed source code at issue. Provided expert report relating to software development, non-infringement of copyright, and analysis of forensic data to refute claims of electronic evidence spoliation.
Law Firm	Kirkland
Client	Flemming and other Defendants
Status	Completed - Summary judgment of non-infringement of copyright for more than 90% of potential damages. Jury verdict awarding minimal damages for balance of claims.
Dates	2005
Matter	Synopsys vs Magma
Description	Theft of IP relating to EDA software as well as patent infringement in two venues. Analyzed Magma software written mostly in C++ for infringement identified historical software supporting invalidity of Magma patents. Provided support for claim construction and invalidity analysis.
Law Firm	Dechert/Wilson Sonsini
Client	Synopsys
Status	Settled.

Martin G. Walker, PhD

Consultant Curriculum Vitae

Dates	2005
Matter	Keywords vs ISE
Description	Investigated allegations of source code copying and copyright infringement of source code written in an interpreted language similar to perl. Declaration ISO of opposition to preliminary injunction.
Client	ISE
Status	Settled.
Dates	2005
Matter	Experian v. I-Centrix
Description	Investigating allegations of source code copying and misappropriation of trade secrets. The code was originally written in Fortran, but then translated into the C programming language. Performed analysis of electronic data that suggested evidence tampering on the part of defendants. Expert Report documenting identification of literal copying of source code as well as copied algorithms. Also identified methods the defendants used in an attempt to disguise the misappropriated code and algorithms.
Law Firm	Jones Day
Client	Experian
Status	Settled.
Dates	2005-06
Testimony	Deposition
Matter	FIS v. CalAmp
Description	Investigation of alleged misappropriation of trade secrets. Performed investigation and created expert report regarding the alleged misappropriation.
Law Firm	Gordon Rees
Client	CalAmp
Status	Settled.
Dates	2006
Matter	LiveOps v. Teleo
Description	Misappropriation of trade secrets, copyright infringement of VoIP software systems. Investigation to detect software copying.
Law Firm	Gordon Rees
Client	LiveOps
Status	Settled.
Dates	2006

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Consultant Curriculum Vitae

Matter	Matsushita v. MediaTek
Description	Patent infringement investigations (invalidity, claim construction, infringement) relating to various patents, including design techniques and DFM technology. Provided expert report regarding infringement and validity of the patents at issue. Expert report on infringement and validity of DFM patent related to processing of metallization structures
Law Firm	Dewey Ballantine
Client	Matsushita
Status	Settled.
Dates	2006
Testimony	Markman Tutorial and Deposition
Matter	Apple Resellers et al v. Apple Computer
Description	Technology neutral appointed by Judge Jacobs May in Superior Court of Santa Clara to resolve the parties disputes regarding proper production of electronic documents. Presentation to the Court to explain the technology and issues relating to the electronic production by the various parties.
Status	Settled.
Dates	2006
Matter	iSmart International v I-Docsecure
Description	Plaintiffs allege that Defendants misrepresented certain technology in the context of an equity investment. Investigated to determine facts; provided declaration regarding business practices and lack of factual basis for claims. Source code at issue was written in a web-host scripting language.
Law Firm	Paul Hastings
Client	I-Docsecure
Status	Settled.
Dates	2006
Matter	Microsoft vs BWT Industry Technology
Description	Provided expert opinion regarding alleged pirating of Microsoft products.
Law Firm	Gordon Rees
Client	BWT Industry Technology
Status	Settled.
Dates	2006

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	Benedict v Mediatrac
Description	Expert testimony at a jury trial regarding standard level of care relating to IT practices.
Law Firm	Greenan, Peffer
Client	Mediatrac
Status	Jury award for Defendant.
Dates	2006
Testimony	Deposition and Trial

Matter	ST vs SanDisk
Description	Patent infringement regarding semiconductor design techniques and ESD circuits. Investigation in support of claim construction and non-infringement analysis.
Law Firm	Jones Day
Client	Mediatrac
Status	Settled
Dates	2006

Matter	Matsushita v. MediaTek
Description	Patent infringement investigations (validity, claim construction, infringement) relating to various patents, including phase-lock loop design.
Law Firm	McDermott Will & Emery
Client	Matsushita
Status	Settled
Dates	2006-07

Matter	Silvaco vs BindKey, et al
Description	Analysis and declarations regarding misappropriation of Silvaco trade secrets, including forensic analysis of hard disk drives used by defendants. The source code was written in C++.
Law Firm	Deschert
Client	Silvaco
Status	Settled
Dates	2006

Matter	Shore Venture Group v Authentidate
Description	Analysis and declarations regarding misappropriation of Silvaco trade secrets, including forensic analysis of hard disk drives used by defendants. The source code was written in C++.
Law Firm	Buchanan Ingersol
Client	Shore Venture Group
Status	Settled
Dates	2007

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Consultant Curriculum Vitae

Matter	Panpacifics v Tradebeam
Description	Selected as an independent expert to assist the arbitration panel with technology issues
Status	Settled
Dates	2007

Matter	Shareholders v Magma
Description	Documented facts relating to the technical aspects of false and misleading statements made by Magma. Provided technical consulting service to plaintiffs counsel to explain the scope and nature of the Defendants acts. Expert report addressed industry-standard software coding practices and level of care relating to possible misappropriation of trade secrets by employees, misappropriation of trade secrets
Law Firm	Millberg Weiss
Client	Shareholders
Status	Settled
Dates	2007

Matter	BHE Group v MTS Products
Description	Analysis of expert testimony; investigation relating to performance of computers
Law Firm	Miller Barondess
Client	BHE Group
Status	Closed. Jury award in excess of \$45,000,000 for client, BHE
Dates	2007
Testimony	Deposition; Jury trial

Matter	HP v Acer
Description	Retained as testifying expert. Analyzed ICs regarding infringement of Acer's circuit design patents. Analyzed and documented infringement of several different ICs. Research included on-site inspections of IC designs using owner-supplied design tools to demonstrate infringement.
Law Firm	Dechert
Client	Acer
Status	Settled
Dates	2007

Matter	Variphy, Inc. et al, v Clarus Systems, Inc.
Description	Investigate alleged misappropriation of trade secrets and source code copying of VoIP telephony and related applications.
Law Firm	Bergeson, LLP
Client	Clarus
Status	Settled
Dates	2008

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Consultant Curriculum Vitae

Matter	Sandisk v various Flash memory manufacturers
Description	Retained as consulting expert responsible for analyzing flash memory controller products for possible infringement of SanDisk patents. Analyzed the detailed design of various products and prepared infringement analyses. Support depositions of technical personnel and experts.
Law Firm	Wilson Sonsini
Client	Sandisk
Status	Closed
Dates	2008
Matter	Web.com v Go Daddy
Description	Prepared and presented claim construction tutorial explaining the background technology for 4 web-hosting related patents
Law Firm	Wilson Sonsini
Client	Sandisk
Status	Closed
Dates	2008
Testimony	Markman tutorial explaining technology for the web-hosting patents at issue.
Matter	On Semiconductor v Samsung
Description	Retained as testifying expert. Performed research to determine infringement and validity of four patents. Three of the patents related to circuits; one related to metallization systems. Prepared expert reports regarding infringement and validity. Prepared declarations in support of various discovery motions. Prepared Markman tutorial for all patents at issue. Assisted attorneys in deposition of Samsung's expert and other technology witnesses.
Law Firm	Jones Day
Client	On Semiconductor
Status	Settled
Dates	2007-08
Testimony	Deposition
Matter	Ricoh v Synopsys
Description	Consulting expert. Prepared technology tutorial. Researched and assisted in preparation of a Motion for Summary Judgment for non-infringement and reply.
Law Firm	Wilson Sonsini
Client	Synopsys
Status	Summary Judgment in favor of Synopsys
Dates	2008-09

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	Spansion v Samsung (ITC and District Court actions)
Description	Consulting expert. Provide analysis and discovery advice on evidence needed to demonstrate infringement of the patents at issue.
Law Firm	King and Spalding
Client	Spansion
Status	Closed
Dates	2009

Matter	Toshiba Medical v. Stubitsch
Description	Testifying expert. Provided expert report and declarations relating to the sufficiency of Toshiba trade secrets descriptions and their misappropriation. Analyzed and responded to motions regarding the particularization of the trade secrets.
Law Firm	Ford Marrin Esposito
Client	Toshiba Medical
Status	Closed
Dates	2009

Matter	Data Treasury v Wells Fargo, et al
Description	Testifying expert. Provided expert report relating to non-infringement of patents by Bancorp South in this extensive litigation in Eastern District of Texas. Reviewed documents and plaintiff expert reports. Developed and documented several bases for non-infringement.
Law Firm	Andrews Kurth
Client	Defendant Bancorp South
Status	Closed
Dates	2009

Matter	LSI Logic/Agere vs Xilinx, Inc
Description	Consulting expert responsible for four patents relating to design software and logic circuits. Prepared Non-infringement analyses/invalidity analyses. Examined circuits as possible prior art
Law Firm	Jones Day
Client	Xilinx
Status	Closed
Dates	2009-10

Matter	On Semi v Hynex, Elpida, and Nanya
Description	Retained as testifying expert. Performed research to determine infringement and validity of five patents. Four of the patents related to circuits; one related to methods of programming flash memory systems.
Law Firm	Perkins-Coie
Client	On Semi
Status	Closed
Dates	2009-10

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Consultant Curriculum Vitae

Matter	Red Bend Software v Google
Description	Testifying expert. Analyzed part of the Chrome browser software accused by Red Bend of infringing a Red Bend patent. Analyzed Red Bend infringement contentions and the browser component at issue. Prepared expert declaration supporting Google's opposition to motion for preliminary injunction. Supported attorneys in preparing oral arguments for Summary Judgment hearing.
Law Firm	Bingham McCutchin
Client	Google
Status	Concluded. Summary judgment in favor of Google
Dates	2009
Testimony	Deposition
Matter	2kDirect v. Azoogole Ads
Description	Testifying expert. Researched issues relating to proper practice by companies engaged in technology due diligence. Provided expert report documenting my opinions.
Law Firm	Cotchett, Pitre & McCarthy
Client	2kDirect
Status	Closed
Dates	2010
Testimony	Deposition
Matter	Scratch DJ LLC v Activision Publishing
Description	Identify source code implementing the asserted trade secrets. Determine if and to what extent defendant used misappropriated source code. Project involved code comparison between code bases in the presence of considerable third party source code.
Law Firm	Duffy Sweeney
Client	Scratch DJ LLC
Status	Closed
Dates	2010
Matter	Volterra v Primarion
Description	Testifying expert for matters relating to the validity or certain Volterra patents. The patents describe integrated semiconductor power switches and their implementation in silicon. My task involved review of the implementation of the devices and the efforts to copy those devices by the defendants. I provided an expert report and testified at deposition.
Law Firm	Farella Brown
Client	Volterra
Status	Closed
Dates	2010
Testimony	Deposition

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	Panasonic v Freescale
Description	Testifying expert in the ITC matter. Review the asserted claims of the patent at issue. Determined if the claims were infringed by certain of the Defendant's designs. Provided expert report relating to claim construction and infringement. Testified at deposition. The patent relates to IC design and manufacturing in general, and more particularly to the patterns of metal interconnects on the designs.
Law Firm	White Case
Client	Panasonic
Status	Closed
Dates	2010
Testimony	Deposition
Matter	Nuance v Vlingo
Description	Testifying expert regarding infringement and validity of speech recognition methods and devices. Analyzed source code and documented evidence of infringement. Considered alleged prior art and identified missing elements. The accused products are web-based speech to text software systems written in C++ and Java programming languages. Authored expert reports concerning infringement and validity.
Law Firm	Irell Manella
Client	Nuance
Status	Closed
Dates	2011
Testimony	Deposition and jury trial testimony regarding infringement and validity. Judge Zobel encouraged the jury to pose questions directly to me, which they did on several occasions.
Matter	Rambus v Freescale, et al
Description	Investigation relating to DDR2 memory interface and high speed serial interfaces, and possible defenses as well as documenting substantial non-infringing use. Created expert report documenting findings.
Law Firm	K&L Gates
Client	ST Microelectronics
Status	Closed
Dates	2011
Testimony	Deposition.

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	Freescall v. ChipMos
Description	Testifying expert regarding scope of licensed patents relating to a defense of patent exhaustion. Compared the scope of patent licenses granted in two contracts. Drafted expert report.
Law Firm	Jones Day
Client	Freescall
Status	Closed
Dates	2011
Testimony	Deposition.
Matter	Richtek v uPI
Description	Testifying expert regarding use of misappropriated trade secrets and elements of certain third party graphics board designs in an ITC enforcement action. Conducted an investigation relating to the Respondent's continued use of Richtek intellectual property. Drafted two expert reports and witness statements. Testified at the hearing.
Law Firm	Alston Bird
Client	Richtek
Status	Closed
Dates	2011
Testimony	ITC Hearing and Deposition.
Matter	Brown v TPL
Description	Testifying expert relating to misappropriation of trade secrets asserted by TPL against Brown. Investigated nature of the trade secrets and whether Brown had identified protectable trade secrets as well as evidence of misappropriation of the trade secrets. Testified at the jury trial.
Law Firm	GCA Law
Client	Brown
Status	Jury award for client Brown
Dates	2011-12
Testimony	Jury Trial and Deposition
Matter	Samsung v Apple
Description	Testifying expert relating to operation of baseband modem ICs that implement the 3GPP standard. Investigated hardware and firmware source code written in VHDL, Verilog, and C languages. Determined the signal coding and decoding in various ICs as compared operation to Samsung's alleged "standard-essential" patents. Drafted expert report.
Law Firm	Wilmer Hale
Client	Apple
Status	Closed
Dates	2012
Testimony	Deposition

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	I-V vs Hynex
Description	Testifying expert on infringement and validity of patents relating to design of certain DDR3 memory products. Investigation included analysis of circuit schematics for DDR3 memories. Provided expert reports supporting validity and infringement
Law Firm	Weil Gotshal
Client	Intellectual Ventures
Status	Closed
Dates	2011-12
Testimony	Deposition
Matter	SST Corp. v. eSilicon Corp
Description	Testifying expert on matters relating to misappropriation of IC design trade secrets and standard industry practices regarding licensing of silicon IP. Provided expert report.
Law Firm	Fenwick
Client	eSilicon
Status	Closed
Dates	2012
Testimony	Deposition
Matter	InterDigital v (Cell phone suppliers including Huawei and ZTE)
Description	Testifying expert relating to the operation of certain Android cell phones and the operation of the baseband modem ICs. Investigation including analysis of Android source code as well as the source code and HDL of the baseband modem. Provided expert reports
Law Firm	Wilson Sonsini
Client	InterDigital
Status	Closed
Dates	2012-13
Testimony	ITC Hearing; Deposition.
Matter	Dynetix v Synopsys
Description	Testifying expert on infringement of patents related to simulation of integrated circuits. Investigation included analysis simulator source code. Provided expert report.
Law Firm	Orrick
Client	Synopsys
Status	Closed
Dates	2012
Testimony	Deposition.

Martin G. Walker, PhD
Consultant Curriculum Vitae

Matter	AMCC v Sandforce, LSI Logic et al
Description	Testifying expert the process of IC design, particularly as it relates to the design of processors.
Law Firm	Gibson Dunn
Client	AMCC
Status	Closed
Dates	2013
Testimony	Deposition
Matter	Skyhook v Google
Description	Research the operation of handset location determination systems. Compared the operation to various patent claims for the purposes of determining infringement as well as whether certain prior-art systems meet the claim limitations. Provided expert reports relating to non-infringement and inventorship.
Law Firm	Steptoe and Johnson/Keker-Van Nest
Client	Google
Status	Closed
Dates	2011-2015
Testimony	Deposition
Matter	British Telecom plc v Google, Inc
Description	Research regarding non-infringement of two mobile data related patents and the operation of Google servers as well as components of the Android OS. Prepared expert reports relating to non-infringement by Google.
Law Firm	White Case
Client	Google
Status	Closed
Dates	2012-2014
Testimony	Deposition
Matter	Mortgage Grader v Costco
Description	Patent infringement. Analyzed operation of web-based application relating to anonymous pricing of mortgages. Created expert report describing the multi-tiered application.
Law Firm	TechKnowledge Law Group
Client	Mortgage Grader
Status	Closed
Dates	2014
Testimony	Deposition

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	Norman IP v Lexmark et al
Description	Patent Infringement relating to processor architecture of controllers used in communication modules used in the MBZ products. Researched non-infringement and invalidity.
Law Firm	Sherman & Sterling
Client	MBZ
Status	Closed
Dates	2013-14
Matter	SnapOn v Bosch
Description	Patent Infringement of software and hardware for wheel alignment systems. Research related to determining infringement.
Law Firm	Grippio & Elden
Client	SnapOn
Status	Closed
Dates	2012-14
Matter	Monster LLC
Description	Covered Business Method (CBM) review. Prepared invalidity analysis of two patents relating to web based methods for job searching and matching. Prepared declarations in support of the petitioner.
Law Firm	Dechert
Client	Monster LLC
Status	Closed
Dates	2014
Matter	HSM v. Fujitsu, et al.
Description	Patent Infringement by Micron memory specific analog and digital gate and transistor level circuits. Created tutorial and provided declarations in support of claim construction. Analyzed operation of accused devices. Provided expert reports supporting invalidity and non-infringement
Law Firm	Weil Gotshall
Client	Micron
Status	Closed
Dates	2013-2016
Testimony	Deposition
Matter	UnWired Planet v Apple
Description	Patent infringement by Apple server and client side software relating to speech recognition and location services.
Law Firm	Gibson Dunn
Client	Apple
Status	Closed
Dates	2013-14
Testimony	Presented Markman tutorial for all patents at issue.

Martin G. Walker, PhD
Consultant Curriculum Vitae

Matter	InterDigital v Nokia
Description	Patent infringement relating to the operation of certain Android cell phones and the operation of the baseband modem ICs. Investigation including analysis of Android source code as well as the source code and HDL of the baseband modem.
Law Firm	Wilson Sonsini/Latham
Client	InterDigital
Status	Closed
Dates	2013
Testimony	Testified at deposition and at ITC hearing.
Matter	InterDigital v Samsung
Description	Patent infringement relating to the operation of certain Android cell phones and the operation of the baseband modem ICs. Investigation including analysis of Android source code as well as the source code and HDL of the baseband modem.
Law Firm	Wilson Sonsini/Latham
Client	InterDigital
Status	Closed
Dates	2013
Testimony	Testified at deposition.
Matter	Realtek v LSI Logic
Description	Patent infringement and validity relating to the physical layout and performance of certain IC devices. Prepared expert reports and witness statements relating to infringement and validity.
Law Firm	Reed Smith
Client	Realtek
Status	Closed
Dates	2012-2014
Testimony	Testified at deposition and at the ITC evidentiary hearing.
Matter	Newell et al. v Yapstone et al.
Description	Investigation of the operation of a web-based application, including the software architecture, performance, and details of the operation. Provided expert report.
Law Firm	Valorem Law
Client	Newell
Status	Closed
Dates	2014-2015
Testimony	Testified at deposition

Martin G. Walker, PhD

Consultant Curriculum Vitae

Matter	XimpleWare, Inc. v Versata et al
Description	Investigation related to infringement of XimpleWare open source software licensed through the GNU copyright. Expert report detailed the scope of infringement and efforts by Defendants to remove the allegedly infringing source code.
Law Firm	Valorem Law
Client	Versata
Status	Closed
Dates	2014-2015
Matter	Oracle America, Inc. v Terix et al
Description	Investigation relating to the extent of alleged copyright infringement by the defendants relating to Sun Solaris software and firmware.
Law Firm	GCA Law
Client	Terix/Maintech
Status	Closed
Dates	2015
Matter	Lenovo et al v Personal Audio
Description	Investigation relating to personal music player patent held by Personal Audio. Research prior art, including source code analysis. Prepared Declaration supporting Petitioner's IPR
Law Firm	White Case
Client	Google
Status	Closed
Dates	2015
Testimony	Deposition
Matter	ATopTech v Synopsys
Description	Supported Patent Owner's response to IPR review of a Synopsys patent relating to static timing analysis. Researched and prepared declaration in support of Patent Owner's final response.
Law Firm	Jones Day
Client	Synopsys
Status	Closed
Dates	2014-2015
Testimony	Deposition
Matter	Synopsys v ATopTech
Description	Investigation relating to Synopsys claims of copyright infringement relating to ATopTech's use of Synopsys commands and output formats in their tool. Documented the extent of the infringement, prepared declarations and expert report.
Law Firm	Jones Day
Client	Synopsys

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Status	Closed
Dates	2014-2016
Testimony	Deposition
Matter	Verizon et al v Orlando Communications
Description	Investigation relating to aspects of Android OS. Prepared Declaration supporting Petitioner's request for re-exam of two Orlando Patents. Examinations were instituted in full.
Law Firm	Keker Van Nest
Client	Google
Status	Closed
Dates	2015-2016
Matter	Xilinx v McCubrey
Description	Investigation relating to design of FPGAs. Prepared Declaration supporting Petitioner's request for re-exam of two McCubrey Patents.
Law Firm	Haynes Boone
Client	Xilinx
Status	Closed
Dates	2015
Matter	NFC Technology v Samsung Electronics Co. LTD.
Description	Investigation relating aspects of NFC communications in Samsung mobile phones. Investigated operation of devices during various NFC communications modes.
Law Firm	Finnegan
Client	NFC Technologies
Status	On-going
Dates	2015-present
Matter	WTS Paradigm, LLC v EdgeAQ, LLC.
Description	Investigation to alleged misappropriation of EdgeAQ trade secrets relating to window and door configuration software. Investigated and reviewed the partys' source code and software configuration management systems to determine the extent of the alleged misappropriation
Law Firm	Foley and Lardner LLP
Client	EdgeAQ
Status	On-going
Dates	2015-present
Matter	Intellectual Ventures v Ricoh Americas Corp.
Description	Investigation to alleged infringement of two patents relating to design of printer and scanner hardware. Performed prior art investigation relating to the invalidity of the IV patents.

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Law Firm	Orrick
Client	Ricoh
Status	On-going
Dates	2016-present

Employment History

From:	2001	Brass Rat Group, Inc.
To:	Current	Woodside, CA
Position:		<i>CEO</i>

Brass Rat Group is a successful Silicon Valley based consulting organization specializing in litigation consulting and business consulting in the semiconductor (IC) design field. Dr. Walker provided litigation support and expert analysis for plaintiff Synopsys in Synopsys vs Nassda, which was recently settled resulting in a “significant victory” for Synopsys.

From:	2000	Knowledge Networks
To:	2001	Menlo Park, CA
Position:		<i>Chief Technology Officer</i>

Knowledge Networks is a pre-IPO market research company that is leveraging internet technology to revolutionize the market research industry. KN recruited a panel of over 50,000 consumers to be interviewed on a variety of topics weekly. Dr. Walker managed KN’s engineering group, which designed and created automated systems to create surveys, conduct interviews, process data, and manage the panel. He also managed the IT group which was responsible for high-availability web-based systems for fielding the interviews as well as the internal systems required to analyze the data and produce real-time reports.

From:	1995	Sequence Design (Formerly Frequency Technology)
To:	2000	
Position:		<i>Founder, Founding CEO, Director & CTO</i>

Sequence Design, formerly Frequency Technology, is the leader in the EDA segment called Design Closure. Sequence's products and services, consisting of pre- and post-layout optimization based on accurate layout extraction, enable designers to bring higher performance, lower-power integrated circuits quickly to tape out. Dr. Walker:

- Developed business plan and raised over \$9MM in financing;
- Hired staff and led development, including defining technical product definition; Personally developed many of the basic algorithms, which resulted in five issued patents;
- Led initial marketing efforts;
- Wrote numerous technical articles advancing the company’s technical position;

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- Served as chief technical spokesman for the company.

From: 1990 **Symmetry Design Systems**

To: 1995 Los Altos, CA

Position: *Founder, Director & Executive Vice President*

Symmetry, a self-funding enterprise, was a service and product business specializing in the analog simulation EDA market. Products included simulation-model libraries, modeling tools, and special-purpose analog simulators. Dr Walker was responsible for a joint venture in Beijing China, where new products were developed. Symmetry was acquired by Analogy, Inc.

- Initiated Japanese and European marketing activities.
- Developed conceptual framework and user-interface model for the Sun OpenLook-based product.
- Served as technical spokesman in customer and industry forums.
- Conducted sales training in the US, Asia, and Europe.

From: 1983

Analog Design Tools

To: 1990

Sunnyvale, CA

Position: *Founder, Director, Founding CEO & Chief Scientist*

ADT's first product, the Analog WorkBench, pioneered the market for Analog CAE workstations, including such fundamental concepts as multiple window CAE systems, and simulated test instruments as a paradigm for CAE user interface. ADT, which had grown to \$16MM in annual sales and 150 employees, was acquired by Cadence.

- Formulated original business plan and presented concept to venture investors. Raised initial venture financing. Led fund-raising activities through the series C round.
- Served as President during formative stage. Director and Chief Scientist (CTO) from the founding through acquisition. Set the product direction. Drove the technology development.
- Formulated ADT's initial marketing strategy. The international distribution strategy focused primarily on Japan.
- Developed the Japanese market for ADT's products. Responsible for establishing and maintaining our distributor relationship, negotiating contracts, supporting customers, and building sales that amounted to 20% of the installed base.

From: 1980

COMSAT

To: 1983

Palo Alto, CA

Position: *Director, Microwave Systems*

Managed a Navy sponsored program to develop high productivity

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techniques for manufacturing of microwave components. Developed a microwave circuit-synthesis product.

From: 1973 **Watkins-Johnson**
To: 1980 Palo Alto, CA
Position: *Member of the Technical Staff*
Developed GaAsMESFET-based microwave amplifiers, components, and tuners. Designed and produced the world's first GaAsMESFET amplifiers to be delivered in production quantities.

Consulting History (within last 5 years)

From: 2005 **Sequence Design**
To: 2007 Santa Clara
Duties: EDA software analysis

From: 2005 **Sabio Labs**
To: 2006 Palo Alto, CA
Duties: Created business plan, operating plan, and marketing plan for EDA startup focused on analog circuit optimization and synthesis

From: 2005 **Synopsys, Inc**
To: On-going Mountain View, CA
Duties: Technology investigations relating to IP issues. Presented technology overview to non-technical staff

Patents

<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
6,643,831	2003	Method and system for extraction of parasitic interconnect impedance including inductance
	2002	Method and system for extraction of parasitic interconnect impedance including inductance
6,381,730		
5,901,063	1999	System and method for extracting parasitic impedance from an integrated circuit layout

Education

<u>Year</u>	<u>College/University</u>	<u>Degree</u>
1987	AEA/Stanford Executive Institute	Completed w/distinction
1979	Stanford University, Stanford, CA	Ph.D., Electrical Engineering
1976	Stanford University, Stanford, CA	MS, Electrical Engineering
1973	Massachusetts Institute of Technology, Boston, MA	BS, Electrical Engineering

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Publications

Over fifty articles in the fields circuit design and design automation, including technical papers in peer-reviewed journals, an invited article in the IEEE Spectrum, and various conference proceedings. I have organized seminars, which were designed to enhance the technical credibility of my companies, and written numerous opinion pieces published in journals such as EETimes that served to establish and promote our corporate position. Some more recent publications are listed below.

Martin G. Walker, Modeling the Wiring of Deep Submicron ICs, IEEE Spectrum Vol 37, No. 3, March 01, 2000 at pp. 65-71.

Martin G. Walker, Keh-Jeng (KJ) Chang, Christopher J. Bianchi, SIPP's Why Do We Need a New Standard for Interconnect Process Parameters? VLSI: Systems on a Chip, Kluwer Academic Publishers, December, 1999.

Martin Walker, Timing Errors Haunt Interconnects, Electronic Engineering Times No. 1021, August 17, 1998.

Martin Walker, Interconnect Analysis Must Move to 3-D, Electronic Engineering Times No. 980, November 10, 1997.

Martin G. Walker, The Guardband Crisis, Electronic Engineering Times No. 929 November 25, 1996 at p. 43.

In addition to the foregoing, I also submitted opinion pieces to Integrated Systems Design (May 1997), Electronic Business (April 1998), and EE Times (June, July, and September 1998).

Professional Associations and Achievements

- 1999 Fortune Magazine "Cool Company" for Frequency Technology.
 - 1984 Electronic Products New Product of the Year award for the Analog Workbench
 - 1976 IEEE Microwave Applications award recognizing contributions to the design of GaAsFET amplifiers.
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