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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Ting P. Yen
Serial No.: 08/900,047
Title: METAL PLUG LOCAL INTERCONNECT
Filed: July 24, 1997
Attorney Docket No.: 0325.00124
Examiner: V. Wallace
Art Unit: 2503
In Response To: Office Action mailed October 3, 1997

#17/Respon.
1/15/98
VV

RESPONSE

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed October 3, 1997,
please consider the following remarks regarding the above-captioned
patent application.

REMARKS

The presently claimed invention concerns a semiconductor
structure comprising a silicon substrate having a top surface, a
diffusion region formed in said substrate adjacent to said top

surface, a polysilicon gate formed on the top surface of the substrate juxtaposed to but not contacting said diffusion region, a sidewall spacer adjacent to the polysilicon gate and disposed above the diffusion region, an insulator layer substantially covering the polysilicon gate and the diffusion region, and a conducting plug at least partially filling a via in said insulation layer that exposes the sidewall spacer in the absence of the conducting plug. The conducting plug provides direct electrical communication between the polysilicon gate and the diffusion region.

Rejection Under 35 U.S.C. § 102(e)

The rejection of claims 3-6, 9-14 and 16-17 under 35 U.S.C. § 102(e) as being anticipated by Sugiyama U.S. Patent No. 5,600,170 is respectfully traversed.

As evidenced by the attached Declaration (the executed version of which will be filed at the earliest opportunity) the present invention was conceived prior to the filing date of Sugiyama. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

REJECTIONS UNDER 35 U.S.C. 103

The rejection of Claims 2, 8 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Sugiyama et al. in view of Jones, Jr. (U.S. Patent No. 5,313,089) has been obviated in view of the attached Declaration under 37 C.F.R. 1.131 and should be withdrawn.

Jones alone does not render the presently pending claims 2, 8 and 15 obvious. Jones discloses a capacitor and memory cell formed therefrom. Nothing disclosed by Jones describes or suggests the via recited in the present claims. Therefore this ground of rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

Received: 1/ 5/98 4:08PM;

-> BLISS McGLYNN, P.C.; Page 10

Sent by: BLISS McGLYNN, P.C.

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The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our Deposit Account No. 02-2712.

Respectfully submitted,

BLISS McGLYNN, P.C.



Andrew D. Fortney, Ph.D.,
Esq.
Reg. No. 34,600


for Luis Miguel Acosta
Registration No. 32,187
2075 West Big Beaver Road, Suite 600
Troy, MI 48064-3443
(248) 649-6090

Dated: January 5, 1998

Docket No.: 0325.00124

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on January 5, 1998.

By:


Julie A. Barber

Received: 1/5/98 4:08PM;

-> BLISS McGLYNN, P.C.; Page 11

Sent by: BLISS McGLYNN, P.C.

248 649 6299;

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5PM; Jettfax #18 Page 7/10

GAU 2503



IN RE APPLICATION OF: Ting P. Yen

SERIAL NUMBER: 08/900,047

FILED: July 24, 1997

FOR: METAL PLUG LOCAL INTERCONNECT

ART UNIT: 2503

EXAMINER: Wallace, V.

Attorney Docket: 0325.00121

RESPONSE TRANSMITTAL AND
EXTENSION OF TIME REQUEST

(IF REQUIRED)

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GROUP 2500

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Enclosed please find an amendment, Affidavit Under 37 C.F.R. 1.131 and a postcard along with the fee calculation below:
FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)

	Claims Remaining	Highest No. Previous	Extra Rate	Additional Fee
Total Claims	10 minus	20 =	0 x \$ 22.00	\$ 0.00
Independent Claims	2 minus	=	0 x \$ 80.00	\$ 0.00
Multiple Dependent Claim First Added			+ \$260.00	\$ 0.00

TOTAL IF NOT SMALL ENTITY \$ 0.00

[] SMALL ENTITY STATUS - If applicable, divide by 2 \$ 0.00
[] Verified statement enclosed, if not previously filed.

[] Applicant also requests a _____ month extension of time
for response to the outstanding Office Action. The fee is \$ 0.00

[] Fee set forth in 37 C.F.R. 1.17 (p) for Information Disclosure
under 37 C.F.R. 1.97 (c). \$ 0.00

TOTAL FEE \$ 0.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 02-2712. A duplicate copy of this sheet is attached.

BLISS McGLYNN, P.C.

Andrew D. Fortney, Ph.D., Esq.
Reg. No. 34,600

2075 W. Big Beaver, Suite 600
Troy, MI 48064-3443
(248) 649-6090

By: [Signature]
for Luis Miguel Acosta
Reg No.: 32,187

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on January 5, 1998.

By: [Signature]
Julie A. Barber

Car 2503
#19



Art Unit: 2503)
Examiner: Wallace, V.)
Applicant(s): Ting P. Yen)
Serial No.: 08/900,047)
Filing Date: July 24, 1997)
For: METAL PLUG LOCAL INTERCONNECT)

TRANSMITTAL

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an executed Declaration of Jeff Watt Under 37
C.F.R. 1.131, Exhibit A, and Jeff Watt's curriculum vitae.

Respectfully submitted,

BLISS MCGLYNN, P.C.

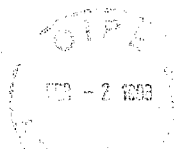
Christopher P. Maiorana
Registration No. P-42,829
2075 West Big Beaver Road, Suite 600
Troy, MI 48084-3443
(248) 649-6090

Dated: January 29, 1998

Docket No.: 0325.00124

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail
in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on January 29, 1998.

By:
Julie A. Barber



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2503)
Examiner: Wallace, V.)
Applicant(s): Ting P. Yen)
Serial No.: 08/900,047)
Filing Date: July 24, 1997)
For: METAL PLUG LOCAL INTERCONNECT)

Declaration of Jeff Watt
Under 37 C.F.R. 1.131

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Jeffrey Watt, hereby declare and state:

1. My curriculum vitae is attached hereto as Appendix 1.
2. I have been employed by Cypress Semiconductor Corporation since 1987, where my current job title is MEMBER OF TECHNICAL STAFF.
3. I have read the above-identified patent application and the subsequent amendment to the claims thereto filed on June 9, 1997. I understand the contents of said patent application and said amendment.

4. I understand that the invention claimed in the above-identified patent application concerns:

(A) a semiconductor structure comprising:

a silicon substrate having a top surface,

a diffusion region formed in the substrate adjacent to the top surface,

a polysilicon gate formed on the top surface of the substrate juxtaposed to, but not contacting, the diffusion region,

a sidewall spacer adjacent to the polysilicon gate and disposed above the diffusion region,

an insulator layer substantially covering the polysilicon gate and the diffusion region,

and

a conducting plug at least partially filling a via in the insulation layer that exposes the sidewall spacer in the absence of the conducting plug, the conducting plug providing direct electrical communication between the polysilicon gate and the diffusion region; and

(B) a method of forming a local interconnect in a semiconductor structure, comprising the step of:

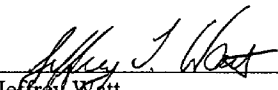
depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to the gate and a portion of a diffusion region such that the electrically conducting material contacts and provides electrical communication between the gate and the diffusion region, the semiconductor structure comprising the diffusion region in a silicon substrate, the gate being on the substrate juxtaposed to but not contacting the diffusion region, the

sidewall spacer being disposed above the diffusion region, the via being in an insulating material on the gate.

5. Prior to June 7, 1995, I witnessed, read and understood an Invention Disclosure Form (copy attached hereto as Exhibit A) describing the subject matter claimed in the above-identified patent application.

6. In my opinion, the Invention Disclosure Form that I witnessed describes the claimed invention and conveys information sufficient to enable one skilled in the relevant art to make and use the claimed invention.

7. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.



Jeffrey Watt

1/19/98

Date

EXHIBIT A**Metal Plug Local Shunt Patent Disclosure****Invention Objective:**

The purpose of this invention is to provide a cheaper method of strapping transistor gates to both N+ & P+ diffusion by using metal plugs which are, in general, already designed into sub-metal contacts. By employing the contact plugs for strapping purpose no additional process steps are necessary.

Current Method:

In order to strap from gate poly to both N+ and P+ diffusion using traditional buried contacts requires a complex set of process additions. The reason for this is that gate poly requires to be doped both P+ and N+, depending on the diffusion doping the poly is strapping to. Further more to minimize inter-diffusion between N+ and P+ doping in poly, extra process steps are required to lower diffusivity. This is even more difficult as design rules are scaled to deep sub-micron range. Other disadvantages are:

- to avoid dopant penetration into channel region, P+ doped poly needs to be implanted with very low energy B11 instead of BF2 (to avoid F+ enhanced dopant diffusion); poor manufacturability.
- For salicided poly: WSix case: this approach does not allow in-situ deposited doped poly/WSix
- TiSix case: this approach makes it difficult to match P+ doped and N+ doped polycide sheet resistance, plus where N+ and P+ poly is suppose to be connected as we have learned there will be a BREAK in the polycide.

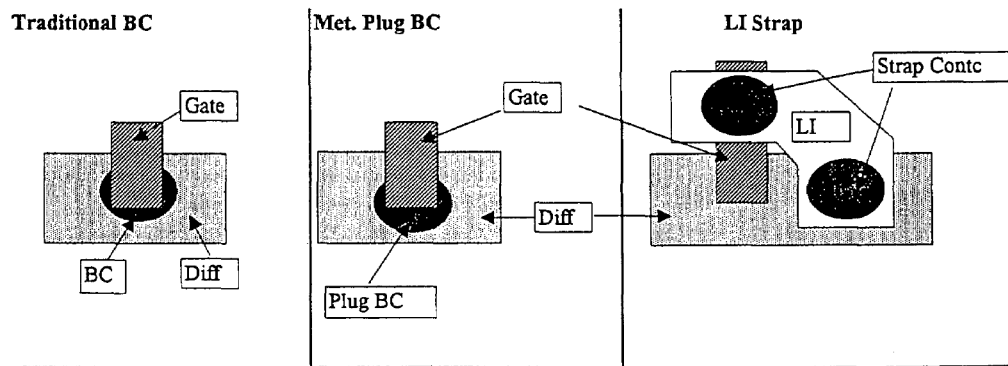
Other available method of strapping gate poly to both N+ and P+ diffusion:

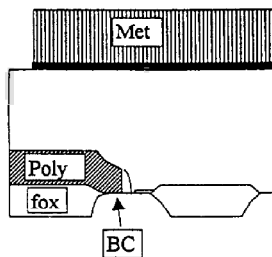
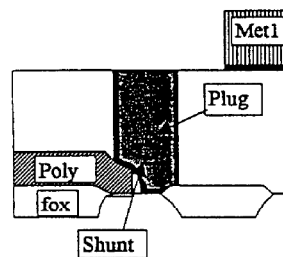
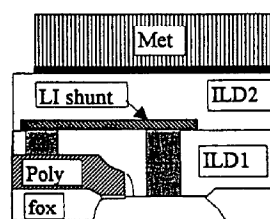
- another obvious method used today is to use a metallic local interconnect strap to shunt from the gate to diffusion. However, this requires: 1) insulating layer between LI and gate 2) open via in insulator 3) deposit LI layer 4) pattern LI layer. In addition from a topological point of view, this requires a lot more layout area than a buried contact at the intersection of gate to diffusion.

New Method:

(Assuming sub-metal plugged contacts by design)

By placing a metallic plugged contact where poly is required to shunt to diffusion, contacts to both P+ and N+ diffusion can be achieved independent of poly doping. Topologically, this will require no more layout area than the traditional buried contact. This method has potential process step savings of 8-11 steps over Trad. BC and 6-8 steps over strapping LI.

Top View

X-Section**Traditional BC****Met. Plug BC****LI Strap****Process Step Count:**

thin poly
BC1 msk
BC1 etch
(BC impl msk)
(BC P+ impl)
(BC N+ impl)
Amorp Si dep
N+ Impl
P+ poly msk
P+ poly impl
Si Recryst 8hr+
WSix dep
Nit/BPSG

-1
-1
-1
-1
-1
-1
-1
-1
-1
-1
-1
-1

Insitu dope Poly/WSix
Nit/BPSG

Insitu Poly/WSix
Nit/BPSG (ILD1)

Licon mask 1
Licon etch 1
Glue/LI dep 1
(W-plug) 1
(WEB) 1
Li mask 1
Li etch 1
ILD2 dep 1

Contact msk/etch
Glue dep
W-plug
WEB
Metal1

Contact msk/etch
Glue dep
W-plug
WEB
Metal1

Contact msk/etch
Glue2 dep
W-dep2
WEB2
Metal1

Summary**Current Technology****Plug BC**

Step Delta Estim from "Current"

High=

Low=

Step Delta Estim from "LI Techn"

High=

Low=

LI Technology

Jeffrey J. West 5/17/95

Jeffrey T. Watt

Cypress Semiconductor
3901 North First Street
San Jose, CA 95134
(408) 943-2916

SUMMARY:

Silicon process and device expert with over 8 years of industrial experience in the design, development, characterization, modeling and reliability of MOS transistors in advanced CMOS processes.

EXPERIENCE:

1997-Present: Member of Technical Staff, Advanced Development

Cypress Semiconductor Corp., San Jose, CA

Responsible for development of transistors for 0.18 um generation process technology.

1993-1997: Device Engineering Manager

Cypress Semiconductor Corp., San Jose, CA

Leader of group responsible for development of HSPICE models for transistors and interconnects, development of ESD protection structures and design rules, development of design rules to meet latchup specifications and process development for MOS transistor modules on platform CMOS SRAM technologies. Specific accomplishments include:

- Developed transistor processes for Cypress 0.5, 0.4 and 0.35 um CMOS SRAM technologies.
- Established methodology and deliverables for transistor development.
- Established methodology for incremental product shrinks for reduced die cost.
- Provided support to product lines on device issues.
- Determined root cause for EOS failures in burn-in and qual stresses. Developed process monitor and design rules for reduce EOS fallout with no impact on process cost.
- Developed novel ESD protection devices to meet HBM and CDM requirements on salicided and non-salicided technologies.

1989-1993: Senior Device Engineer,

Cypress Semiconductor, San Jose, CA

Responsible for transistor development, electrical design rule generation, electrical test structure design, ESD/latch-up design rules. Specific accomplishments include:

- Developed high-voltage transistor for 0.8 um PROM technology
- Developed transistor process for 0.65 um CMOS SRAM technology.
- Developed high-performance 0.6 um transistors for SPARC microprocessor.
- Supervised two technicians operating the ESD/latch-up qualification testing and failure analysis lab.
- Developed ESD protection devices for all 0.8 and 0.65 um technologies including BiCMOS, SRAM, Logic, PROM and PLD.
- Developed design rules to protect against CDM ESD, thereby reducing backend yield loss for ESD to ~0%.

EDUCATION

- 1989: Ph.D., Electrical Engineering, Stanford University, Stanford, CA**
NSERC Postgraduate Scholarship 1984-1987
Thesis: "Modeling the Performance of Liquid-Nitrogen Cooled CMOS"
Advisor: James D. Plummer
- 1984: M.S., Electrical Engineering, Stanford University, Stanford, CA**
Imperial Oil Graduate Research Fellowship 1983-1986
Sir James Lougheed Award of Distinction 1983-1985
- 1983: B.S., Electrical Engineering, Queen's University, Kingston, Canada**
B.S. in Electrical Engineering
Governor General's Gold Medal 1983

PUBLICATIONS:

- F. N. Trofimenkoff, R. H. Johnson, J. W. Haslett and J. T. Watt, "Image Theory Analysis of Fields Due to a Step in the Current on a Long Line on the Surface of the Earth," IEEE Trans. Geosci. Remote Sensing, vol. GE-22, March 1984.
- J. T. Watt, B. J. Fishbein and J. D. Plummer, "A Low-Temperature NMOS Technology with Cesium-Implanted Load Devices," IEEE Trans. Electron Devices, vol. ED-34, January 1987.
- A. K. Henning, N. N. Chan, J. T. Watt and J. D. Plummer, "Substrate Current at Cryogenic Temperatures: Measurements and a Two-Dimensional Model for CMOS Technology," IEEE Trans. Electron Devices, vol. ED-34, January 1987.
- B. J. Fishbein, J. T. Watt and J. D. Plummer, "Time Resolved Annealing of Interface Traps in Polysilicon Gate MOS Capacitors," J. Electrochem. Soc., 134(3), March 1987.
- J. T. Watt and J. D. Plummer, "Efficient Numerical Simulation of the High-Frequency MOS Capacitance," IEEE Trans. Electron Devices, vol. ED-34, October 1987.
- J. T. Watt, B. J. Fishbein and J. D. Plummer, "Characterization of Surface Mobility in MOS Structures Containing Interfacial Cesium Ions," IEEE Trans. Electron Devices, vol. 36, January 1989.
- J. T. Watt and J. D. Plummer, "The Effect of Interconnection Resistance on the Performance of Liquid-Nitrogen Cooled CMOS Circuits," IEEE Trans. Electron Devices, vol. 36, August 1989.
- J. T. Watt and J. D. Plummer, "Dispersion of MOS Capacitance-Voltage Characteristics Resulting from the Random Channel Dopant Ion Distribution," IEEE Trans. Electron Devices, vol. 41, November 1994.

CONFERENCE PRESENTATIONS:

- "Universal Mobility-Field Curves for Electrons and Holes in MOS Inversion Layers," 1987 Symposium on VLSI Technology, Karuizawa, Japan.
- "Effect of Interconnection Delay on Liquid-Nitrogen Temperature CMOS Circuit Performance," 1987 International Electron Devices Meeting, Washington, D.C.
- "Surface Potential Fluctuations in MOS Devices Induced by the Random Distribution of Channel Dopant Ions," 1988 Device Research Conference, Boulder, CO.
- "A Hot-Carrier Triggered SCR for Smart Power Bus ESD Protection," 1995 International Electron Devices Meeting, Washington, D.C.