Marc Heyns (editor) Marc Meuris & Paul Mertens (co-editors)

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Proceedings of the Second International Symposium on Ultra-clean Processing of Silicon Surfaces



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1. INTRODUCTION

In semiconductor device processing, silicon oxides are used in many forms for many different applications. Dense thermally grown silicon oxide is used as the gate dielectric film in MOS transistors. Steam grown thermal silicon oxide is used as a field oxidation dielectric layer. Doped silicon oxides such as phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG) are used as intermetal dielectrics because they can be easily planarized through reflow. During the processing of silicon based semiconductor devices, other types of silicon oxide films may be formed as the result of exposure of silicon surfaces to chemical processing step, or to the ambient environment. In many cases, these residual oxides are considered surface contaminants since they must be removed to allow the formation of a high quality electrical interface. Often, it is necessary to remove a chemical or native oxide, along with associated residues and contamination from a pattern feature bottom in the presence of one or more of the silicon oxides mentioned above. Oxide etching selectivity is of paramount importance in these cases since different oxides may be etched at drastically different rates.

A current trend in semiconductor wafer processing is towards using gas vapors or all dry gas processes in a cluster tool environment to remove residual oxides and contaminants. It has long been known that vapors of HF/water mixtures will etch various silicon oxide films, and this technology has been well studied [1,2] and commercialized. Etching of oxide films with anhydrous HF has also been well studied [3] and has been found to be affected by the quantity of residual water in the process environment and in the oxide film itself, such that the etching mechanisms appear to be similar to those for HF/water mixtures. A limitation encountered in the use of HF vapor phase etching of oxide films is the low etching rates for native and chemical silicon oxide films relative to doped silicon oxides

Wong et al. [1] have studied the selectivity of the HF vapor etching processes to many different types of oxide films. The results show that native, chemical, and thermal oxides are typically removed at rates up to 10 times slower than the removal rates of PSG and BPSG doped silicon oxides. This is problematic in several common processing circumstances. First of all, it is commonly necessary to clean native oxide and other contaminant from the bottom of contact holes through dielectric layers of BPSG. Using the current vapor phase processes, several hundred angstroms of the BPSG can be removed before the silicon oxides and contamination in the contact hole are removed. Secondly, it is common to use sandwich structures of different types of silicon oxide films. For instance, a BPSG layer between two undoped oxide layers is sometimes used as the intermetal dielectric film in the above mentioned contact application. Cleaning of contact or other topographic features through this type of composite film with the current HF vapor technology causes enhanced lateral etching of the BPSG layer relative to the undoped oxide layers. This results in an undercut profile which is difficult to fill with subsequent films without forming voids

Here, we describe the application of photochemical (UV-enhanced) processes for the rapid etching of doped and undoped oxide films, and the removal of thin chemical oxide surface layers. Previous work with ClF_3 reported enhanced selectivity of native oxide over silicon under UV irradiation [4]. The processes reported here employ ClF_3 gas in a dry nitrogen carrier stream and simultaneous UV irradiation. Doped and undoped oxides are observed to be removed at nearly identical rates in a large process window (pat. pending).

2. **EXPERIMENTAL**

The full-wafer reactor used in these studies was an experimental single wafer vacuum cluster module capable of conducting photochemical processing of 100, 150, or 200 mm wafers. The module was attached to a vacuum cluster The reactor module was constructed of hardcoated 6061 robotic handler. aluminum. A dry rough pump was used to pump the vacuum reactor to a base pressure below 10 mtorr. High purity sapphire windows were used to allow UV light exposure of the wafer front side. Gases were introduced in a uniform radial laminar flow, to enhance the transport of etching products away from the wafer surface. High intensity (~200-300 mW/cm² at 200-400 nm), broad band UV irradiation was achieved with a commercially available 300 W/inch, medium pressure mercury arc discharge lamp. The wafer pre-process temperature was controlled using a proximity heater. During the period of UV exposure the wafer temperature was transient due to IR output from the UV lamps. However, the wafer temperature typically did not exceed 300°C during processing. Process pressure was monitored and controlled using a capacitance manometer in a feedback loop with a downstream throttle valve.

Substrates used in this study were 150-mm p<100> silicon wafers, 1-5 ohm-cm. Oxide films were prepared by growing 4000Å of silicon oxide in a steam oxidation process at 1000 °C. 5000Å BPSG (3% B, 3% P) films were deposited by CVD over 1000Å of thermal oxide. The gases used C.P. grade (99.0%) ClF₃ and VLSI grade (99.998%) Cl₂. Dry N₂ from a liquid N₂ vapor delivery system was used as a diluent gas.

Thermal oxide and BPSG removal rates were measured by comparing the film thickness, measured by spectroscopic reflectometry, before and after

processing. Silicon removal rates were measured by stylus profilometry on wafers partially covered by a patterned oxide layer.

3. **RESULTS AND DISCUSSION**

Rates for etching of thermal silicon oxide and BPSG in UV/ClF₃ processes are shown in Figure 1 for an initial wafer temperatures of 150°C as a function of ClF₃ concentration. Total flow was maintained at 1000 sccm using dry N₂ as a diluent, and total pressure was maintained at 100 Torr. Thermal oxide and BPSG were found to etch at similar rates with a selectivity of better than 1.5 (BPSG:thermal oxide).





The removal of 10-20Å chemical oxide layers using UV/ClF₃ and UV/(ClF₃+Cl₂) processes was also investigated. Oxide patterned p<100> wafers, comprising 1-5µm lines and vias, were subjected to an RCA-type wet chemical clean to produce the chemical oxide layer in the unpatterned regions. The wafers were then processed with UV/ClF₃ or UV/(ClF₃+Cl₂). The ClF₃ only process used 2.5 sccm ClF₃ with 997.5 sccm N₂. The ClF₃+Cl₂ process used 2.5 sccm ClF₃, 50 sccm Cl₂ and 947.5 sccm N₂. Both processes were run at 100 torr with an initial wafer temperature of 100°C. Several wafers were exposed to UV for time periods ranging from 0.5 minutes to 3 minutes. The oxide pattern mask was subsequently stripped, and the depth of etching into the silicon substrate was measured using a

stylus profilometer. The results of these experiments are summarized in Figure 2. Regression of the time series back to a zero (undetectable silicon etch depth) indicates that the chemical oxide was removed after approximately 30 seconds of UV exposure under the experimental conditions. Comparison of the silicon surface roughening after chemical oxide removal for the two processes revealed that the UV/ClF₃ process resulted in a visually rough surface, while the UV/(ClF₃+Cl₂) process left the silicon surface substantially smoother. This process is expected to be applicable as a dry contact clean.



Figure 2. Silicon removal as a function of UV exposure time for UV/ClF3 and UV/(Cl2 + ClF3) processes indicating the time to remove 10-20Å of chemical oxide.

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