

***DSS Technology Mgmt., Inc. v. Intel Corp. et al., Case No. 6:15-cv-00130-RWS
(E.D. Tex.)***

Claim Construction Dates

	EVENT
Dec. 7, 2015	Opening Claim Construction Brief
Dec. 23, 2015	Responsive Claim Construction Brief
Jan. 4, 2016	Reply Claim Construction Brief
Jan. 11, 2016	Joint Claim Construction Chart
Jan. 25, 2016	Claim Construction Hearing

Local Patent Rule 4-3
Joint Claim Construction Statement

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION**

DSS Technology Management, Inc.,

Plaintiff,

v.

Intel Corporation, et al.,

Defendants.

Civil Action No. 6:15-cv-130-RWS

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT

Pursuant to Rule 4-3 of the Local Patent Rules (“P.R.”) of the Eastern District of Texas and the Docket Control Order (Dkt. 161), Plaintiff DSS Technology Management, Inc. and Defendants Intel Corporation, Dell, Inc., GameStop Corp., Conn’s, Inc., Conn Appliances, Inc., Wal-Mart Stores, Inc., Wal-Mart Stores Texas, LLC, and AT&T Mobility LLC (collectively referred to as “Defendants”) file this Joint Claim Construction and Prehearing Statement.

I. AGREED CLAIM CONSTRUCTIONS [P.R. 4-3(a)]

Pursuant to P.R. 4-3(a), the parties have agreed on proposed constructions of the following claim terms, phrases, or clauses, of the patents-in-suit, U.S. Patent No. 5,965,924 (“the ’924 patent”) and U.S. Patent No. 6,784,552 (“the ’552 patent”):

THE ’552 PATENT	
TERM	AGREED CONSTRUCTION
“contact region”	contact openings and/or vias

This construction is also reflected in the table attached as Exhibits A (U.S. Patent No. 6,784,552). If the parties are able to reach further agreement concerning the constructions of any

of the remaining claim terms, phrases, or clauses at issue, they will supplement the present Joint Claim Construction and Prehearing Statement.

II. DISPUTED CLAIM CONSTRUCTIONS [P.R. 4-3(b)]

Pursuant to P.R. 4-3(b), the parties' proposed constructions of disputed claim terms, phrases, or clauses are also reflected in the tables attached as Exhibits A and B, together with all references from the specification or prosecution history that support the construction and an identification of any extrinsic evidence. The parties expressly reserve the right to rely on any intrinsic and extrinsic evidence identified by the other party, and any evidence obtained, or that may be obtained, through claim construction discovery. The parties expressly reserve the right to amend, correct, or supplement their claim construction positions and supporting evidence in response to any change of position by the other party, in response to information received through claim construction discovery, including inventor depositions and expert depositions concerning claim construction declarations, or for other good cause.

III. LENGTH OF CLAIM CONSTRUCTION HEARING [P.R. 4-3(c)]

Defendants anticipate that the claim construction hearing will require a total of four hours. This would allow Plaintiff and Defendants two hours per side.

Plaintiff anticipates that the claim construction hearing will require a total of three hours. This would allow Plaintiff and Defendants an hour and a half per side.

IV. LIVE WITNESS TESTIMONY AT CLAIM CONSTRUCTION HEARING [P.R. 4-3(d)]

Neither party intends to call witnesses live at the claim construction hearing. However, the parties have agreed that deposition testimony and affidavits of expert and fact witnesses may be used as exhibits to the Claim Construction Briefs required by P.R. 4-5.

V. OTHER ISSUES [P.R. 4-3(e)]

According to the Docket Control Order, there is no prehearing conference scheduled before the claim construction hearing. The parties do not at this time have any other issues that might be appropriately taken up at either a prehearing conference before or at the claim construction hearing. Should any party become aware of such issues that it believes necessitates a prehearing conference, it will notify the other party and the Court and propose dates for a prehearing conference.

Dated: November 2, 2015

Respectfully submitted by:

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on November 2, 2015.

/s/ Michael E. Jones

EXHIBIT A

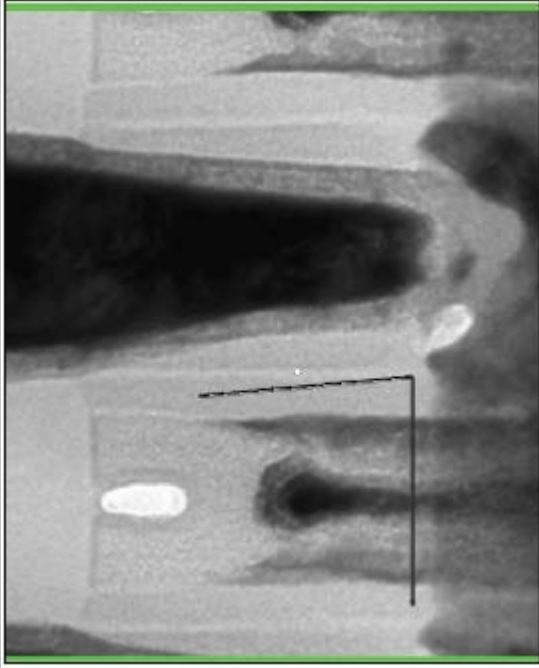
Parties' Proposed Claim Constructions for Claim Terms in U.S. Patent 6,784,552

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
"an etch stop material over said first insulating layer" (claim 1)	"an etch stop material around or above said first insulating layer" Generally, an etch stop material has an etch rate that is relatively higher than an adjacent or underlying material exposed to a specific etch process and may prevent etching of the adjacent or underlying material. Abstract; 4:12-17; 12:54-13:20; 13:58-52; 14:10-17; Fig. 4K; Fig. 4L; Claims US 6,004,875 Merriam Webster's Collegiate Dictionary (10th Ed. 1994) ("over")	"a material overlying the first insulating layer that is not effectively etched by the etchant used to create the contact region" Specification: "A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate without risk of exposing the device structures and layers because the device structuring and layers are protected from excessive etching by the etch stop layer 125." ('552 patent at 4:13-18.) "The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact opening 270 was formed through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence, the description of the silicon nitride layer 240 is described as an etch stop layer. The silicon nitride etch stop layer 240 protected the underlying TEOS layer 230 and spacer portion 235 so that the polysilicon layer 220 completely encapsulated." ('552 patent at 4:51-60.) "A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer,

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		for example a BPTEOS blanket layer 350." ('552 patent at 5:46-50.) "FIG. 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material. FIG. 4(G) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, and a distinct planarized insulating layer overlying the etch stop layer. FIG. 4(H) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material. . . . FIG. 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material. . . . FIG. 4(L) ..." ('552 patent at 9:19-56.) "Referring to FIG. 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, a silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms." ('552 patent at 11:63-66.)
"a side of the insulating spacer has an angle relative to the substrate surface that is either a right	Plain and ordinary meaning. Abstract; 12:66-13:18; 13:29-35; 14:10-17; Figs. 4D, 4K, 4L; Claims 3/3/03 Amendment and Request for Reconsideration	"a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than 85° and less than or equal to 90°" <u>Specification:</u>

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
angle or an acute angle of more than 85°” (claim 1)		Fig. 2(A) Fig. 2(B) Fig. 4(K) “FIG. 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride layer 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion 235 is sloping or tapered toward the contact opening 270. This result follows even where the spacer portion is originally substantially rectangular as in FIG. 2(A). The properties of the highly selective etch of the overlying etch stop layer 240 will transform a substantially rectangular spacer into a sloped spacer. FIG. 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.” (’552 patent at 5:4-17.) “The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer spacer portion 435. The low selectivity etch yields a TEOS layer spacer portion 435 that retains a rectangular or “boxy” profile. FIG. 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer spacer portion 435 is removed during the etch. Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		profile.” (’552 patent at 13:2-10.) “The phrase ‘substantially rectangular’ means that a side of the spacer has an angle relative to the substrate surface of more than 85°.” (’552 patent at 8:41-43). “Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.” (’552 patent at 2:54-56.) <u>File History:</u> “Dennison, et al. describes a method of forming a bit line over a capacitor array of memory cells. Element 18 in Figure 2 shows a spacer. This portion of the figure is reproduced below. As illustrated, the spacer has a sloping portion, and is not substantially rectangular.” (’552 File History, Amendment, Feb. 6, 2004 at 5.) <u>DSS’s Infringement Contentions:</u>

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		 (DSS' Infringement Contentions, Exhibit B at p. 7; see also <i>id.</i> at 6 (“The sidewall spacer is steeper than the shown reference angle of 85°, shown in black on the insulating spacer below.”).)
“insulating spacer” (claim 1)	Plain and ordinary meaning. Abstract; 4:34-56; 13:51-65; 14:10-17; Figs. 4D, 4K, 4L; Claims	“lateral spacer that electrically isolates the conductive layer from the contact region” <u>Specification:</u> Fig. 4(B)-(D) “The invention contemplates that the insulating layer has spacer portions between the conductive layers and the contact opening.” (’552 patent at 13:51-53.)

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		“Next, the insulating spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile.” (’552 patent at 7:30-36.) “Referring to FIGS. 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact openings by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact openings and adjacent to the polysilicon layer. . . . The spacer portions 435 of the TEOS layer 430 are demarked by ghost lines in FIG. 4(D). . . . As shown in FIG. 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile.” (’552 patent at 11:35-49.) “Thus, the remaining etch stop material adjacent to the spacer portion 435 of the TEOS layer 420 serves as additional spacer material to insulate the polysilicon layer 415 from a conductive contact that will subsequently be added to the contact opening 460.” (’552 patent at 12:61-65.) “The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region, and a device including a contact opening with a small alignment tolerance relative to a gate electrode or

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		other structure.” (’552 patent at 7:15-20.) “Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.” (’552 patent at 4:20-25.) “The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235.” (’552 patent at 4:39-42.)
“contact region” (claim 1)	<u>PARTIES’ AGREED CONSTRUCTION:</u> “contact openings and/or vias”	<u>PARTIES’ AGREED CONSTRUCTION:</u> “contact openings and/or vias” <u>Specification:</u> “Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and a first metal layer is called a ‘contact opening’, while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a ‘via’. For purposes of the claimed invention, henceforth ‘contact opening’ or ‘contact region’ will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure

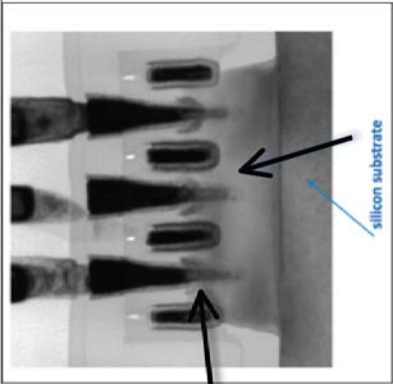
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		such as a gate.” (’552 patent at 1:33-45.) “Adjacent to the polysilicon layer 220 is a contact opening region 270.” (’552 patent at 4:38-40.) “In FIG. 2(A), a contact opening 270 has been opened through the BPTEOS layer 250.” (’552 patent at 4:49-51.) “FIG. 3 illustrates a prior art substrate with a gate and a contact region undergoing an RF sputter etch 380 Adjacent to the gate is a contact region 360.” (’552 patent at 5:41-51.) “FIG. 3 indicates the difference in contact opening widths for the same contact in prior art structures. w1 represents the width at the top of the planarized layer and w2 represents the width at the base of the contact region 360.” (’552 patent at 6:48-52.)

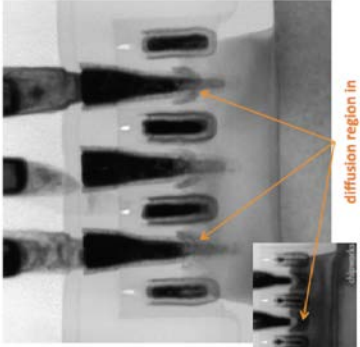
EXHIBIT B

Parties' Proposed Claim Constructions for Claim Terms in U.S. Patent 5,965,924

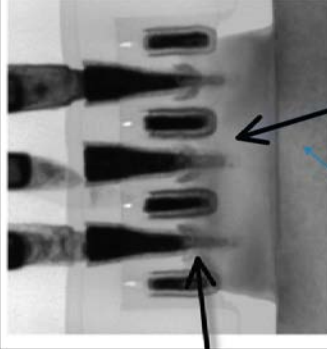
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
"diffusion region formed in said substrate" (claim 1)	"conductive terminal region such as a source or drain formed in said substrate" Abstract; 3:41-51; 4:6-10; 5:13-21; Fig. 3B; Claims Introduction to VLSI Systems, Mead & Conway (1980) US 8,405,132 US 6,163,057 US 5,747,837 Merriam Webster's Collegiate Dictionary (10th Ed. 1994) ("formed")	"conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate" <u>Specification:</u> Figs. 1A, 1B, 2A, 2B, 3A, 3B "Diffusion regions 70 and 72 of either N+ or P+ doping are first formed by an ion implantation process in the surface of the silicon substrate 74. This is accomplished by patterning through a photoresist layer and then etching to form openings for the diffusion regions for the ion implantation process. The photoresist layer is used as an implantation mask." ('924 patent at 3:49-55.) "In a preferred embodiment, a semiconductor structure is provided which includes a silicon substrate having a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface of the substrate adjacent to but not contacting the diffusion region, an insulator layer which covers the poly silicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conducting plug filling at least partially the via opening to provide electrical connection between the polysilicon gate and the diffusion region." ('924 patent at 3:1-11.) "Openings (not shown) are formed on the surface of

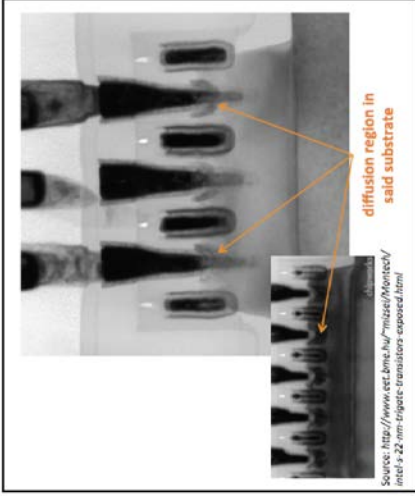
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		substrate 12 to expose sections of the substrate for the formation of buried contacts. An ion implantation process is performed at the openings to increase the surface dopant concentration for improved contact resistance. Subsequently, the photoresist layer is removed and a layer of polysilicon is deposited onto substrate 12. Thereafter, the polysilicon layer is patterned and etched, typically by a reactive ion etching method, to form a gate electrode 14 for making electrical connection with the diffusion region 16.” (’924 patent at 1:33-43) <u>File History:</u> “Nishigoori ’210 discloses a MOS type semiconductor device which has a contact hole opened in a layer of insulating material. The first contact hole has a length similar to the width of the corresponding source/drain diffusion regions. A refractory metal is then deposited to fill the contact hole.” (Amendment date Aug. 14, 1996 at pp. 5-6.) <u>DSS’s Infringement Contentions:</u> “The silicon substrate is the dark layer at the bottom of the image. Since the devices are incorporated into a multiplicity of fins incorporated in the silicon substrate, the fins are indistinguishable from the bulk, comprising the substrate. Even after features are machined into silicon bulk, the whole structure remains “bulk” silicon. The silicon bulk is the portion of silicon in which the channel forms by inverting the silicon surface with gate

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		voltage applied across the gate oxide. Thus, the silicon substrate includes the fin because it is within the silicon fin that the channel forms owing to its three-dimensional channel characteristic. The silicon substrate, including the fin structure, has a top surface.” (DSS’ Infringement Contentions, Exhibit A at p. 2.)  (DSS’ Infringement Contention, Exhibit A at p. 3.) “The diffusion region appears beneath the metal plugs adjacent to top surface of the substrate.” (DSS’ Infringement Contention, Exhibit A at p. 3.)

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
"diffusion region in a silicon substrate" (claim 7)	"conductive terminal region such as a source or drain in a silicon substrate" Abstract; 3:41-51; 4:6-10; 5:13-21; Fig. 3B; Claims Introduction to VLSI Systems, Mead & Conway (1980) US 8,405,132 US 6,163,057 US 5,747,837 Merriam Webster's Collegiate Dictionary (10th Ed. 1994) ("formed")	 Source: http://www.eet.bme.hu/~mike/monit/vintel%20nm-trigate-transistors%20exposed.html (DSS' Infringement Contention, Exhibit A at p. 3.) "conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate" Specification: Figs. 1A, 1B, 2A, 2B, 3A, 3B "Diffusion regions 70 and 72 of either N+ or P+ doping are first formed by an ion implantation process in the surface of the silicon substrate 74. This is accomplished by patterning through a photoresist layer and then etching to form openings for the diffusion regions for the ion implantation process. The photoresist layer is used as an implantation mask." ('924 patent at 3:49-55.) "In a preferred embodiment, a semiconductor structure is provided which includes a silicon substrate having a top surface, a diffusion region formed in the substrate

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		adjacent to the top surface, a polysilicon gate formed on the top surface of the substrate adjacent to but not contacting the diffusion region, an insulator layer which covers the poly silicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conducting plug filling at least partially the via opening to provide electrical connection between the polysilicon gate and the diffusion region.” (’924 patent at 3:1-11.) “Openings (not shown) are formed on the surface of substrate 12 to expose sections of the substrate for the formation of buried contacts. An ion implantation process is performed at the openings to increase the surface dopant concentration for improved contact resistance. Subsequently, the photoresist layer is removed and a layer of polysilicon is deposited onto substrate 12. Thereafter, the polysilicon layer is patterned and etched, typically by a reactive ion etching method, to form a gate electrode 14 for making electrical connection with the diffusion region 16.”(’924 patent at 1:33-43) <u>File History:</u> “Nishigoori ’210 discloses a MOS type semiconductor device which has a contact hole opened in a layer of insulating material. The first contact hole has a length similar to the width of the corresponding source/drain diffusion regions. A refractory metal is then deposited to fill the contact hole.” (Amendment date Aug. 14, 1996 at pp. 5-6.)

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		<u>DSS's Infringement Contentions:</u> “The silicon substrate is the dark layer at the bottom of the image. Since the devices are incorporated into a multiplicity of fins incorporated in the silicon substrate, the fins are indistinguishable from the bulk, comprising the substrate. Even after features are machined into silicon bulk, the whole structure remains “bulk” silicon. The silicon bulk is the portion of silicon in which the channel forms by inverting the silicon surface with gate voltage applied across the gate oxide. Thus, the silicon substrate includes the fin because it is within the silicon fin that the channel forms owing to its three-dimensional channel characteristic. The silicon substrate, including the fin structure, has a top surface.” (DSS’ Infringement Contention, Exhibit A at p. 2.)  Top Surface silicon substrate (DSS’ Infringement Contention, Exhibit A at p. 3.) “The diffusion region appears beneath the metal plugs

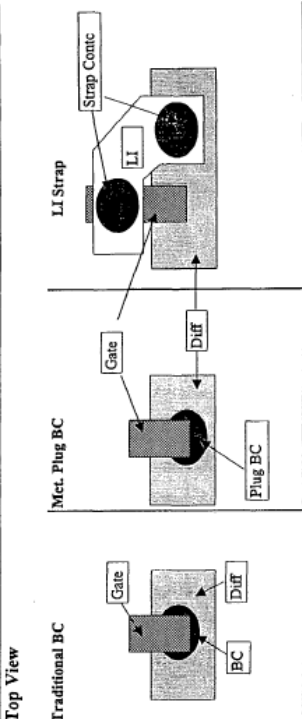
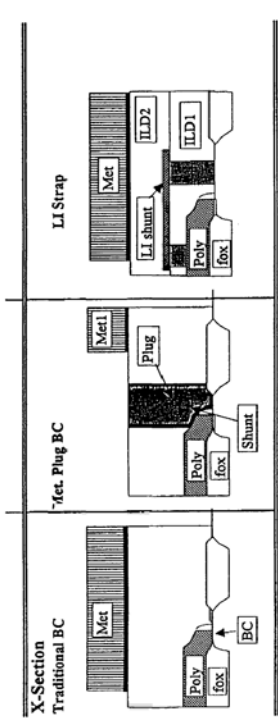
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
"conducting plug" (claim 1)	Plain and ordinary meaning. Abstract; 3:1-14; 3:41-45; 4:14-17; 5:13-21; Fig. 3B; Claims 11/07/96 Office Action; 6/10/97 ROA	adjacent to top surface of the substrate." (DSS' Infringement Contention, Exhibit A at p. 3.)  (DSS' Infringement Contention, Exhibit A at p. 3.)
"conducting plug" (claim 1)	Plain and ordinary meaning. Abstract; 3:1-14; 3:41-45; 4:14-17; 5:13-21; Fig. 3B; Claims 11/07/96 Office Action; 6/10/97 ROA	"electrically conducting material deposited into a via and separate from a strapping shunt layer" <u>Specification:</u> Figs. 1A, 1B, 2A, 2B, 3A, 3B" After the formation of the contact holes 24, a thin layer of titanium tungsten or titanium nitride is normally deposited into the contact hole to improve adhesion. A refractory metal plug such as a tungsten plug is then deposited into hole 24." ('924 patent at 1:50-54.) "One of such methods is to use a metallic local interconnect strap to shunt from a gate polysilicon to a

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		diffusion region.” ('924 patent at 2:13-15.) “In a local interconnect strap method, a polysilicon gate 32 is first formed without direct contact with the diffusion regions 34 and 36 in a silicon substrate 40. An insulating layer 42 of dielectric material is then deposited on top of the polysilicon and the diffusion regions. Vias are opened through masking/etching processes in the insulator layer 42. After the deposition of a glue layer (not shown), metal plugs 44, 46 and 48 are deposited into the vias. After a tungsten plug etch back and a local interconnect masking/etching process, a local interconnect shunt layer 50 is deposited. A separate shunt 52 is also deposited on metal plug 48 to allow the deposition of another metal plug 54 such that diffusion region 36 can be connected to the Metal I layer 56. The second metal plug 54 is formed in a via opened in the second insulating layer 60 of a dielectric material.” ('924 patent at 2:17-31.) “The local interconnect strap method, even though accomplishes the electrical connection between a polysilicon gate and a diffusion region, is a process-intensive method.” ('924 patent at 2:32-34.) “It is yet another object of the present invention to provide a metal plug local interconnect between a polysilicon gate and a diffusion region that does not require the use of a local interconnect strap.” ('924 patent at 2:56-59.) “It is another further object of the present invention to

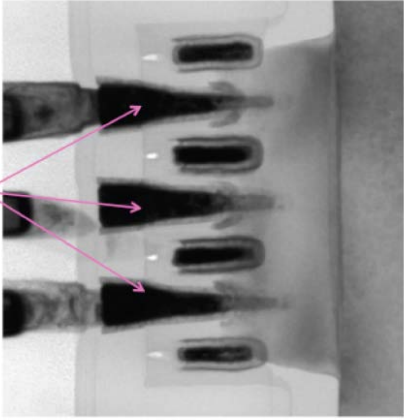
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		provide a metal plug local interconnect between a polysilicon gate and a diffusion region wherein the metal plug local shunt can be formed in a single metal contact formation step.” (’924 patent at 2:60-63.) “The present invention provides a semiconductor structure that has a metal plug local interconnect (or shunt) for connecting a polysilicon gate to a diffusion region in a structure and a method of forming such a semiconductor structure.” (’924 patent at 3:41-45.) “In the same process of making sub-metal plugged contacts on the device, an additional via opening 78 is provided for placing a metallic plug contact where the polysilicon gate is required to shunt to the diffusion region.” (’924 patent at 3:63-66.) “A metal plug local interconnect 80 thus formed interconnects the polysilicon gate at 82 and the diffusion region 70 at 84. Electrical contacts to both P+ and N+ diffusion regions can be achieved independent of the polysilicon doping. It should be noted that topologically, the present invention method does not require more layout area than a conventional buried contact method. Moreover, the present invention method requires substantially less layout area than a local interconnect strapping method.” (’924 patent at 4:6-15.) “The present invention metal plug local interconnect can be fabricated in a process that has substantially lesser number of processing steps required than either a conventional buried contact process or a local

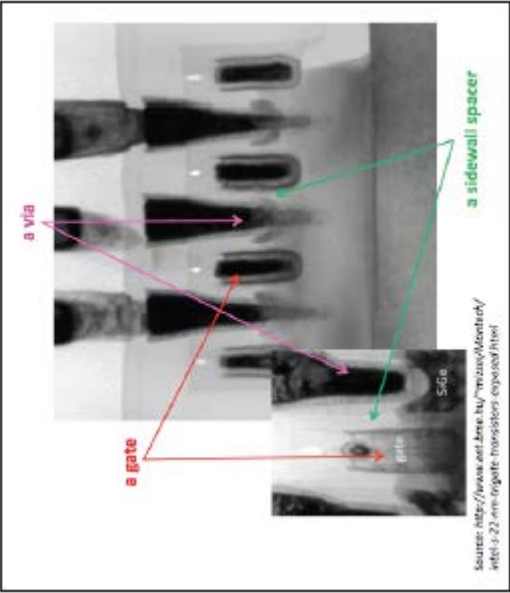
Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		interconnect strapping process. For instance, the present invention method saves 8-11 steps over a conventional buried contact process and saves 6-8 steps over a local interconnect strapping process.” (’924 patent at 4:18-26.) Conventional Buried Contact Process Step #1 - thin poly deposition #2 - BC1 mask #3 - BC1 etch #4 - (BC implantation mask) #5 - (BC P+ implantation) #6 - (BC N+ implantation) #7 - Amorp Si deposition #8 - N+ Implantation #9 - P+ poly mask #10 - P+ poly implantation #11 - Si Recryst 8 hr+ #12 - WSix deposition #13 - Nit/BPSG STEP 14 THROUGH 21 NOT REQUIRED #22 - Contact mask/etch #23 - Glue deposition #24 - W-plug #25 - WEB #26 - Metal I TOTAL PROCESSING STEPS = 18

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		Local Interconnect Strapping Process STEPS 1 THROUGH 11 NOT REQUIRED Step #12 - Insitu dope Poly/WSix #13 - Nit/BPSG (ILD1) #14 - Liicon mask #15 - Liicon etch #16 - Glue/LI deposition #17 - (W-plug) #18 - (WEB) #19 - Li mask #20 - Li etch #21 - ILD2 deposition #22 - Contact mask/etch #23 - Glue2 deposition #24 - W-deposition 2 #25 - WEB2 #26 - Metal I TOTAL PROCESSING STEPS = 15 Metal Plug Local Interconnect Process STEPS 1 THROUGH 11 NOT REQUIRED Step #12 - Insitu dope Poly/WSix #13 - Nit/BPSG STEPS 14 THROUGH 21 NOT REQUIRED #22 - Contact mask/etch #23 - Glue deposition #24 - W-plug #25 - WEB #26 - Metal I TOTAL PROCESSING STEPS = 7 (‘924 patent at 4:27-5:12.) <u>File History:</u>

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		Top View  X-Section  “The purpose of this invention is to provide a cheaper method of strapping transistor gates to both N+ & P+ diffusion by using metal plugs which are, in general, already designed into sub-metal contacts. By employing the contact plugs for strapping purpose no additional process steps are necessary.” (Rule 131 Declaration dated Jan. 29, 1998.) “another obvious method used today is to use a metallic local interconnect strap to shunt from the gate to diffusion. However ... from a topological point of view, this requires a lot more layout area than a buried contact at the intersection of gate to diffusion.” (Rule 131

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		Declaration dated Jan. 29, 1998.) “New Method... By placing a metallic plugged contact where poly is required to shunt to diffusion, contacts to both P+ and N+ diffusion can be achieved independent of poly doping. Topologically, this will require no more layout area than the traditional buried contact. This method has potential process step savings of 8-11 steps over Trad. BC and 6-8 steps over strapping LI.” (Rule 131 Declaration dated Jan. 29, 1998.) <u>DSS's Infringement Contentions:</u> “The conducting plug fills a gap that would expose the sidewall spacer if the plug were absent. The sidewall spacers are seen separating the conducting plug from the gate conductor, if the plug were removed, the sidewall spacer would be exposed.” (DSS' Infringement Contention, Exhibit A at p. 5.)

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		 (DSS' Infringement Contention, Exhibit A at p. 5.) “As seen in a TEM of the Intel Core i5-4690, Intel’s 22-nm FinFET process includes depositing an electrically conducting material in a via that would otherwise expose a portion of a gate.” (DSS’ Infringement Contention, Exhibit A at p. 10.)

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction and Support
		 The image is a grayscale micrograph showing a cross-section of a printed circuit board (PCB) or similar electronic component. It features a central vertical structure labeled 'a gate' with red arrows pointing to it from the left. To the right of the gate is a circular feature labeled 'a via' with a red arrow pointing to it. Further to the right is a rectangular feature labeled 'a sidewall spacer' with a green arrow pointing to it. The image is rotated 90 degrees clockwise. Below the image, there is a small text block: 'Source: http://www.ett.com/industry/infrastructure/22-err-gate-transfer-exposed.html'. (DSS' Infringement Contention, Exhibit A at p. 10.)

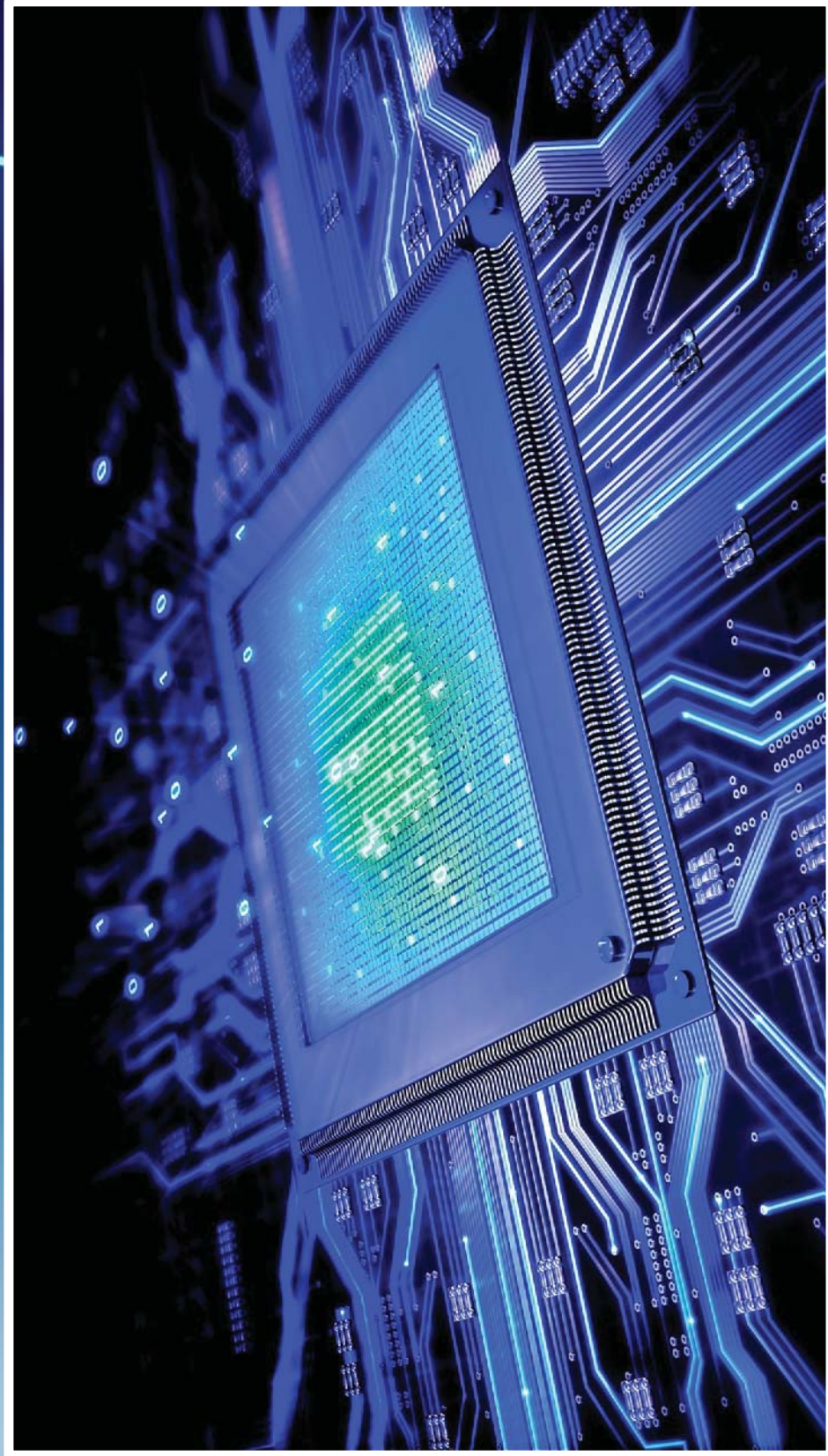
DSS Technology Tutorial

**TECHNOLOGY TUTORIAL FOR
U.S. PATENT NO. 5,965,924 & 6,784,552**

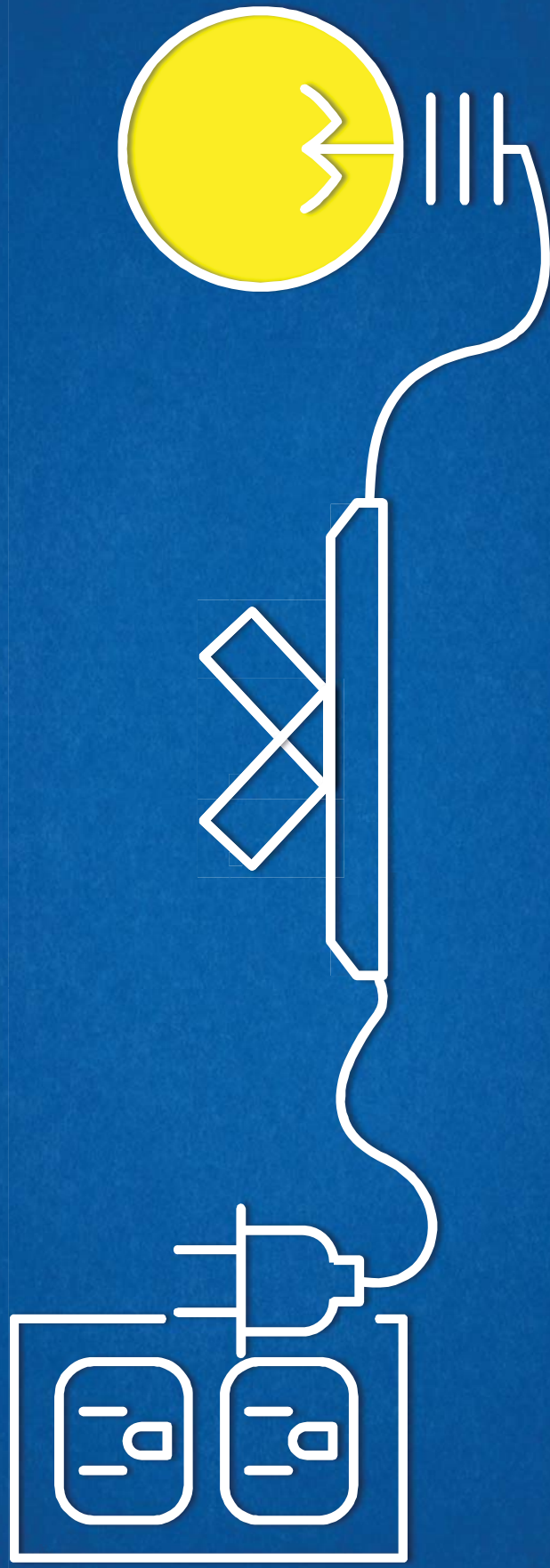
DSS Technology Management Inc.
v.
Intel Corporation et al.

***Civil Action No. 6:15-CV-130,
United States District Court for the Eastern District of Texas***

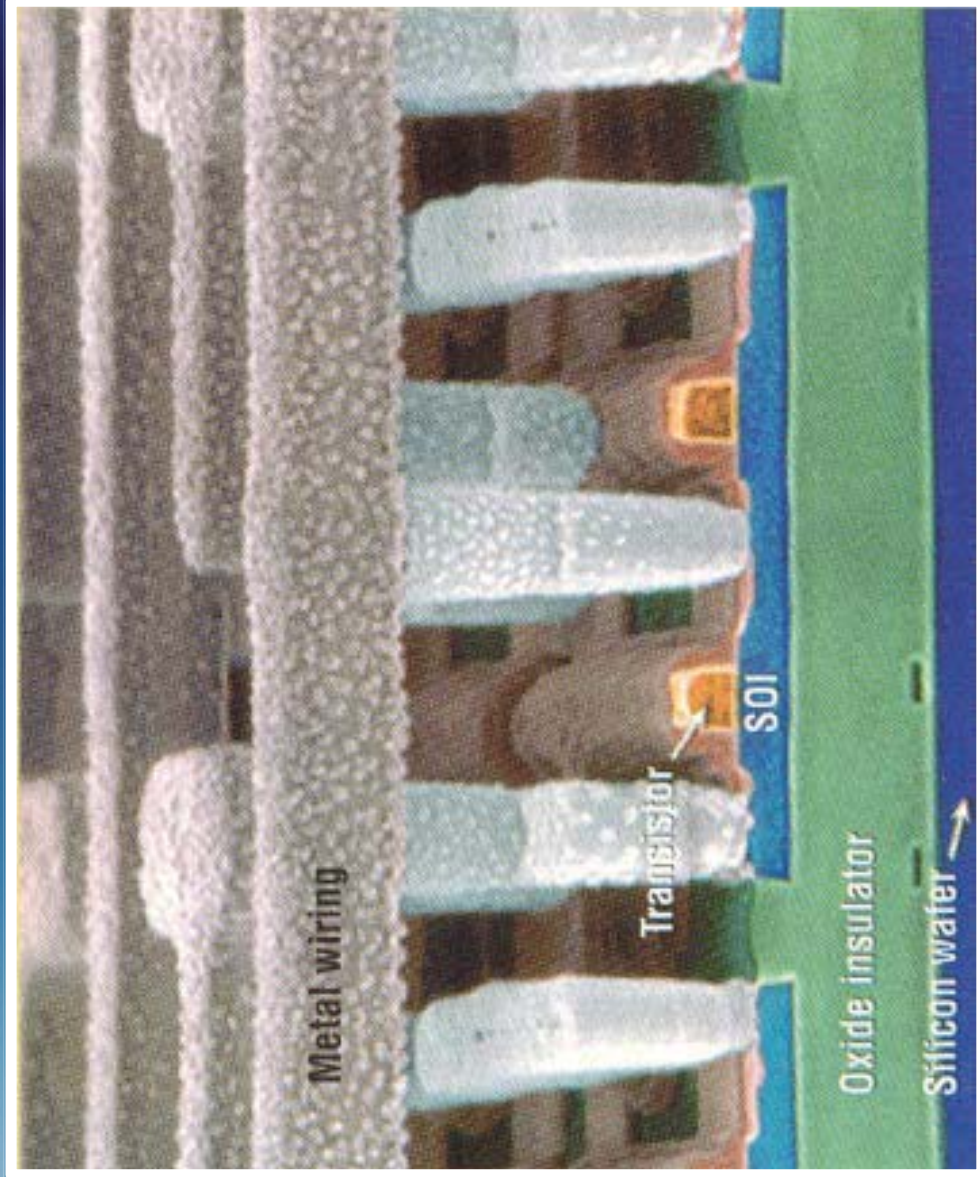
TECHNOLOGY BACKGROUND



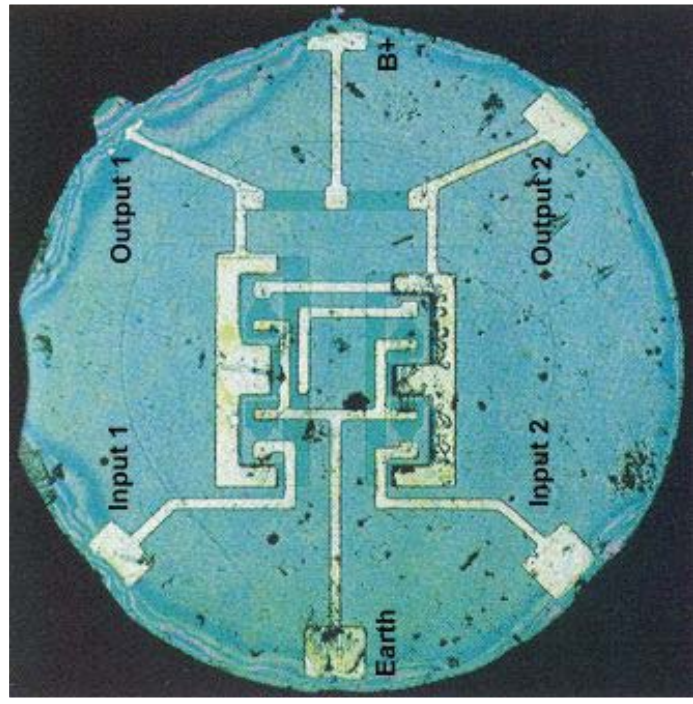
TECHNOLOGY BACKGROUND



TECHNOLOGY BACKGROUND

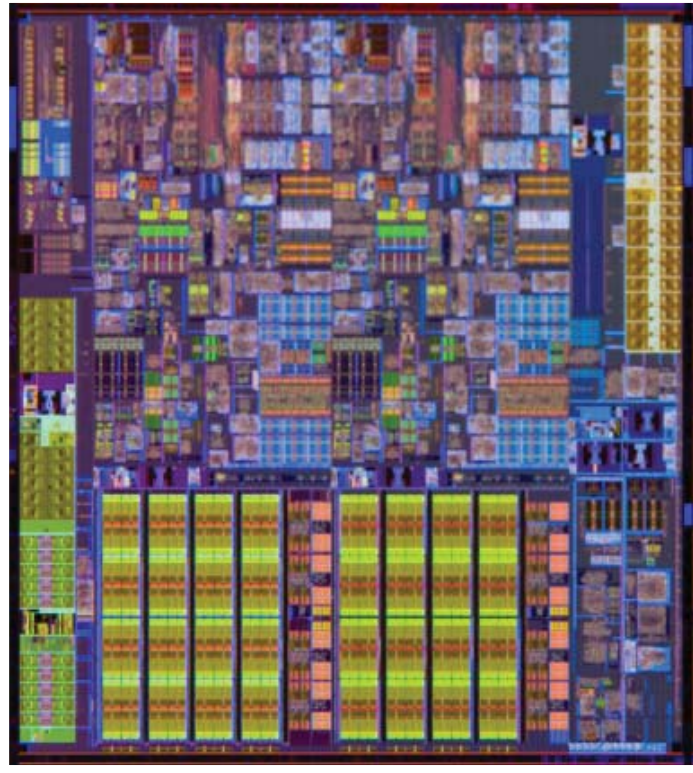


TECHNOLOGY BACKGROUND



1961

Feature size = 25 microns
(one thousandth of an inch)



2011

Feature size = 25 nanometers
(one millionth of an inch)

THE '924 and '552 PATENTS

'924 PATENT



US 5,965,924 A

United States Patent
Yen

(11) Patent Number: 5,965,924
(45) Date of Patent: Oct. 12, 1999

- [54] METAL PLUG LOCAL INTERCONNECT
- [75] Inventor: Ting P. Yen, Fremont, Calif.
- [73] Assignee: Cypress Semiconductor Corp., San Jose, Calif.
- [*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.536(a) and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).
- (21) Appl. No.: 08/900,047
- (22) Filed: Jun. 24, 1997
- [63] Continuation of application No. 08/561,951, Nov. 22, 1995, abandoned.
- [51] Int. Cl.⁶: H01L 29/76; H01L 29/94
- [52] U.S. Cl.: 257/383; 257/382; 257/388; 257/303; 438/647; 438/649
- [58] Field of Search: 257/387, 388, 903, 437/190, 125, 438/647, 649
- [56] References Cited
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Silicon Processing, Inc., The VLSI Etc., Vol. 2, Process Integration; Stanley et al., P.D., pp. 144-145, 212-214, and 354-355.

Primary Examiner—Valencia Martin-Wallace
Attorney, Agent, or Firm—Christopher P. Marone, P.C.

[57] **ABSTRACT**

A semiconductor structure that includes a silicon substrate which has a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface, and an insulator layer substantially covers the polysilicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conductive material is deposited in the via opening, thereby providing electrical communication between the polysilicon gate and the diffusion region.

17 Claims, 1 Drawing Sheet



'552 PATENT



US 6,784,552 B2

United States Patent
Nully et al.

(10) Patent No.: US 6,784,552 B2
(45) Date of Patent: Aug. 31, 2004

- [54] STRUCTURE HAVING REDUCED LATERAL SPACER EROSION
- [75] Inventors: James E. Nully, San Jose, CA (US); Christopher J. Petti, Mountain View, CA (US)
- [73] Assignee: Cypress Semiconductor Corporation, San Jose, CA (US)
- [*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.536(a) and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).
- (21) Appl. No.: 09/546,610
- (22) Filed: Mar. 31, 2000
- (65) US 2002/0146097 A1 Oct. 10, 2002
- Related U.S. Application Data
- (62) Division of application No. 08/577,751, filed on Dec. 22, 1995, now Pat. No. 6,066,555.
- (51) Int. Cl.⁷: H01L 23/52; H01L 29/40
- (52) U.S. Cl.: 257/774; 257/775; 257/776; 438/634; 438/637; 438/638; 438/657
- (58) Field of Search: 257/774, 775, 257/776, 756-760, 762, 765, 438/634, 637, 639, 257
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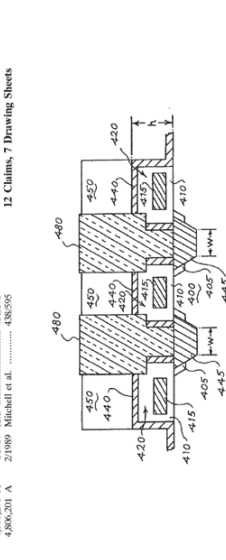
K.K. Shih et al., "Hafnium dioxide etch-stop layer for phase-shifting masks," *J. Vac. Sci. Technol. B* 11(6), Nov./Dec. 1993, pp. 2130-2131.

Primary Examiner—Bradley Baumeister
Assistant Examiner—Chris C. Chu
(34) Attorney, Agent, or Firm—Evan Law Group LLC

ABSTRACT

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small width and a high aspect ratio. The process includes the steps of forming a conductive layer on a semiconductor body, then depositing an insulating layer adjacent to the conductive layer. The insulating layer is etched back to form a rectangular lateral spacer profile of the first insulating layer. The etch stop layer is then deposited adjacent to the conductive layer. An etch stop layer is deposited adjacent to the gate electrode. An etch stop layer is removed to expose the conductive layer. The etch stop layer is then deposited adjacent to the conductive layer. The etch stop layer is then removed to expose the conductive layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and the semiconductor body. The apparatus is also capable of forming some other layer or structure, and is an effective structure for small feature size structures, particularly self-aligned contact structures.

12 Claims, 7 Drawing Sheets



THE '924 PATENT

'924 PATENT



US08065924A
Patent Number: 5,965,924
Date of Patent: *Oct. 12, 1999

United States Patent [19]
Yen

[54] METAL PLUG LOCAL INTERCONNECT
[73] Inventor: Ting P. Yen, Fremont, Calif.
[72] Assignee: Cypress Semiconductor Corp., San Jose, Calif.

[*] Notice: This patent issued on a continued prosecution application under 35 U.S.C. 115(a) and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No. 08/900,047
[22] Filed: Jan. 24, 1997

Related U.S. Application Data

[63] Continuation of application No. 08/241,951, Nov. 22, 1995, abandoned.
[51] Int. Cl.⁶ H01L 29/76; H01L 29/94
[52] U.S. Cl. 257/383; 257/382; 257/385; 257/303; 438/647; 438/649
[58] Field of Search 257/387; 388; 903; 437/190; 102; 438/647; 649

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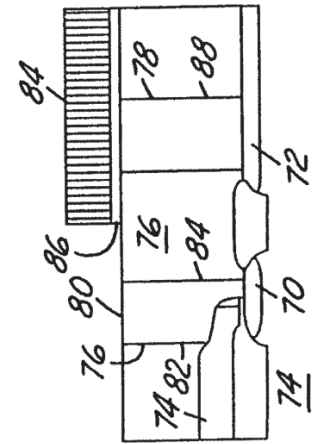
Silicon Processing, Inc. The VLSI Era, Vol. 2, Process Integration; Stanley et al. Ph.D. pp. 144-145, 212-214, and 354-355.

Primary Examiner—Valencia Martin-Wallace
Attorney, Agent, or Firm—Christopher P. Maloney, P.C.

ABSTRACT

A semiconductor structure that includes a silicon substrate which has a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface, and a metal plug electrically connecting the diffusion region to an insulator layer above. The plug covers the polysilicon gate and the diffusion region, the layer contains a via opening therein, and is electrically connected to the diffusion region. The plug is electrically providing electrical communication between the polysilicon gate and the diffusion region.

17 Claims, 1 Drawing Sheet



Patent Number: 5,965,924

Date of Patent: *Oct. 12, 1999

METAL PLUG LOCAL INTERCONNECT

Inventor: Ting P. Yen, Fremont, Calif.

Continuation of application No. 08/561,951, Nov. 22, 1995, abandoned.

THE '924 PATENT

'924 PATENT

US05965924A

United States Patent [19]

Yen

Patent Number: 5,965,924

Date of Patent: *Oct. 12, 1999

[54] METAL PLUG LOCAL INTERCONNECT

[73] Inventor: Ting P. Yen, Fremont, Calif.

[73] Assignee: Cypress Semiconductor Corp., San Jose, Calif.

[*] Notice: This patent issued on a continued prosecution application pursuant to 35 U.S.C. 1.56(a) and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No. 08/900,047

[22] Filed: Jul. 24, 1997

[63] Continuation of application No. 08/541,951, Nov. 22, 1995, abandoned.

[51] Int. Cl.⁶ H01L 29/76; H01L 29/94

[52] U.S. Cl. 257/383; 257/382; 257/385; 257/386; 438/647; 438/649

[58] Field of Search 257/387, 388, 903, 437/190, 192, 438/647, 649

[56] References Cited

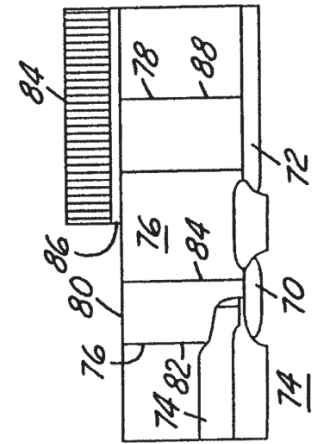
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5,053,551 10/1991 Farn et al. 67/572



17 Claims, 1 Drawing Sheet

[57] ABSTRACT

A semiconductor structure that includes a silicon substrate which has a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface of the substrate adjacent to but not contacting the diffusion region, an insulator layer substantially covers the polysilicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conducting plug filling at least partially the via opening providing electrical communication between the polysilicon gate and the diffusion region.

THE '924 PATENT

'924 PATENT

United States Patent [19] Patent Number: 5,965,924
Yen Date of Patent: *Oct. 12, 1999

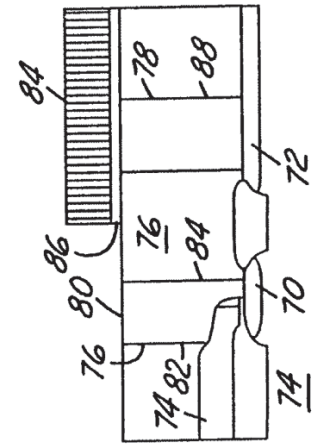
[54] METAL PLUG LOCAL INTERCONNECT
[73] Inventor: Ting P. Yen, Fremont, Calif.
[73] Assignee: Cypress Semiconductor Corp., San Jose, Calif.
[*] Notice: This patent issued on a continued prosecution application filed under 35 U.S.C. 1.56(a) and is subject to the twenty year patent term provisions of 35 U.S.C. 154(c)(2).

[21] Appl. No. 08/900,047
[22] Filed: Jul. 24, 1997
[63] Continuation of application No. 08/541,951, Nov. 22, 1995, abandoned.
[51] Int. Cl.⁶ H01L 29/76; H01L 29/94
[52] U.S. Cl. 257/383; 257/382; 257/385; 257/386; 438/647; 438/649
[58] Field of Search 257/387; 388; 403; 437/190; 102; 438/647; 649

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U.S. PATENT DOCUMENTS
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5,053,551 10/1991 Faza et al. 67/52

OTHER PUBLICATIONS
Silicon Processing, Inc. The VLSI Era, Vol. 2, Process Integration; Stanley et al. Ph.D. pp. 144-145; 212-214, and 354-355.
Primary Examiner—Valencia Martin-Wallace
Attorney, Agent, or Firm—Christopher P. Maloney, P.C.

ABSTRACT
A semiconductor structure that includes a silicon substrate which has a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface, an insulator layer substantially covering the polysilicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conducting plug filling at least partially the via opening providing electrical communication between the polysilicon gate and the diffusion region.

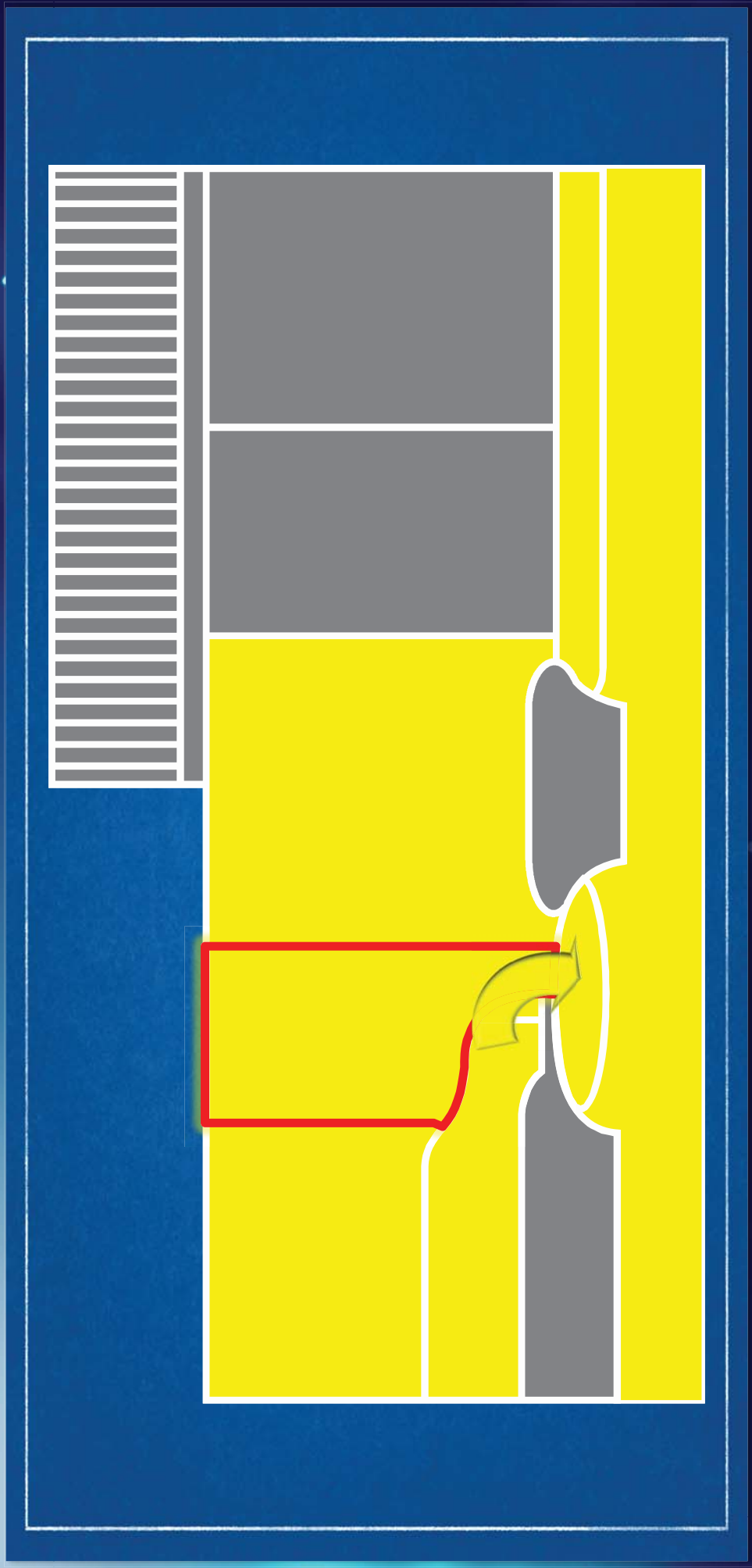


17 Claims, 1 Drawing Sheet

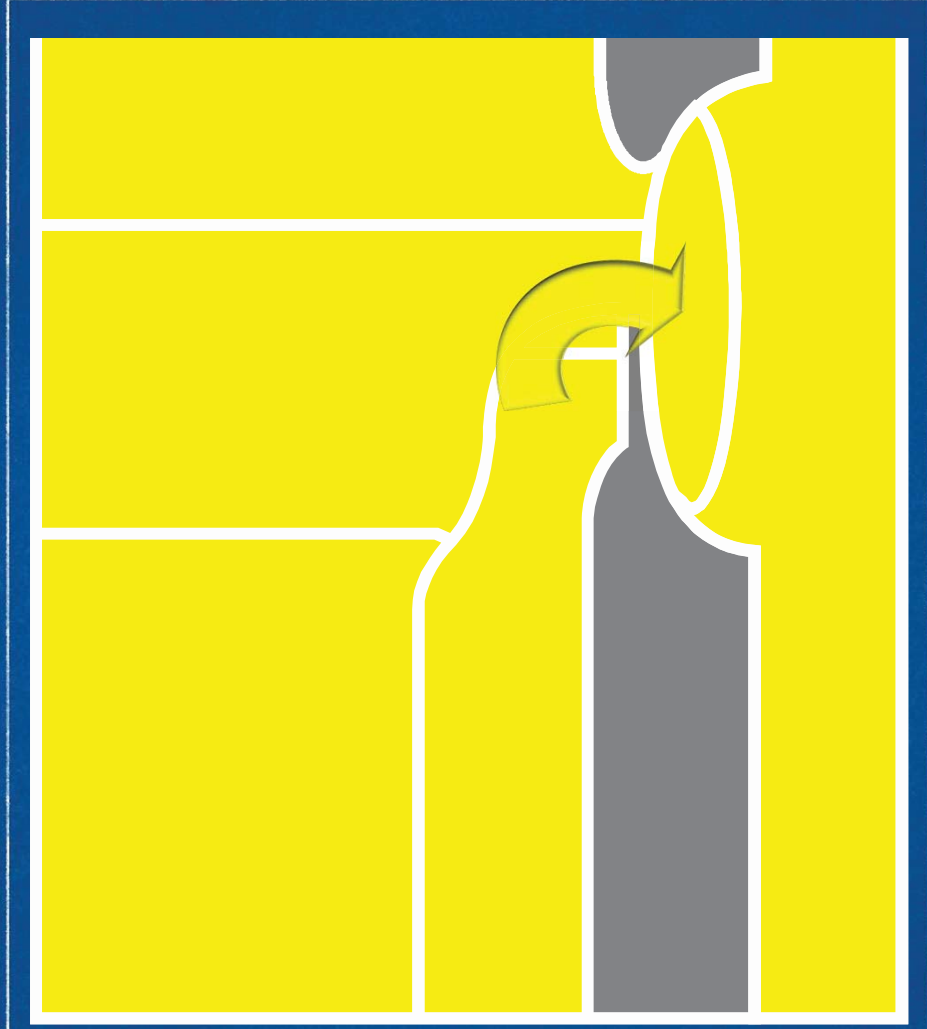
ABSTRACT

A semiconductor structure that includes a silicon substrate which has a top surface, a diffusion region formed in the substrate adjacent to the top surface, a polysilicon gate formed on the top surface of the substrate adjacent to but not contacting the diffusion region, an insulator layer substantially covers the polysilicon gate and the diffusion region, the layer contains a via opening therein, and an electrically conducting plug filling at least partially the via opening providing electrical communication between the polysilicon gate and the diffusion region.

THE '924 PATENT



CLAIM 1 OF THE '924 PATENT



1. A semiconductor structure comprising:

a silicon substrate having a top surface,

a diffusion region formed in said substrate adjacent to said top surface,

a gate formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region,

a sidewall spacer adjacent to said gate and disposed above said diffusion region,

an insulator layer substantially covering said gate and said diffusion region, and

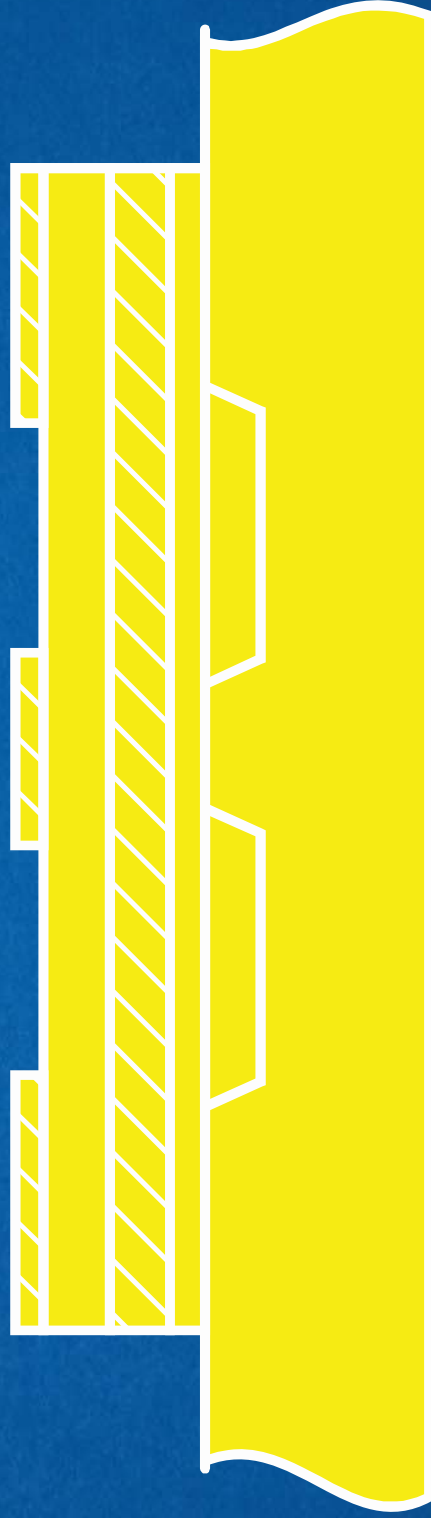
a conducting plug at least partially filling a via in said insulation layer that exposes said sidewall spacer in the absence of said conducting plug, said conducting plug providing direct electrical communication between said gate and said diffusion region.



THE '552 PATENT



THE '552 PATENT



THE '552 PATENT



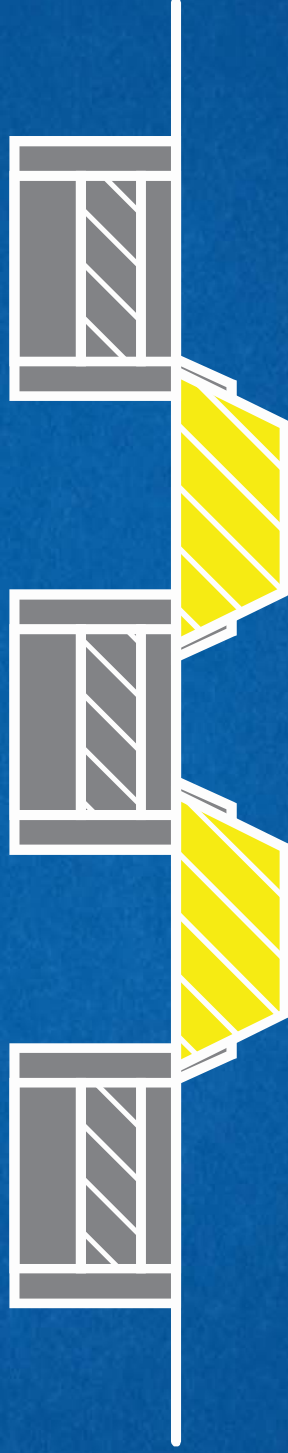
THE '552 PATENT



THE '552 PATENT



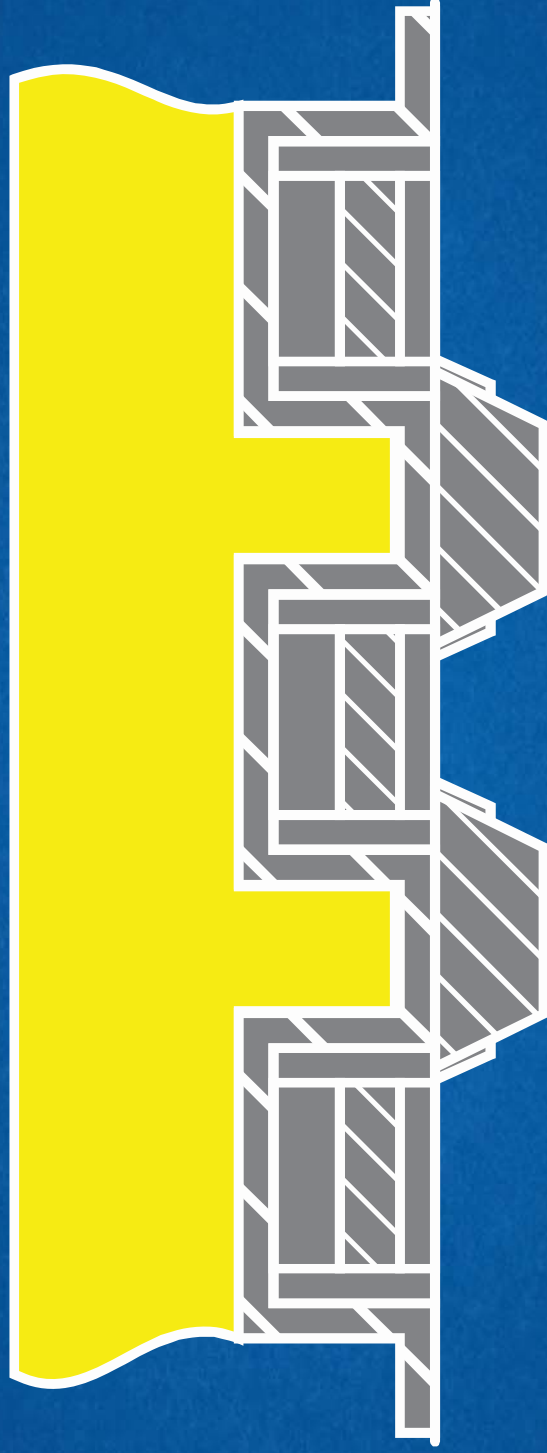
THE '552 PATENT



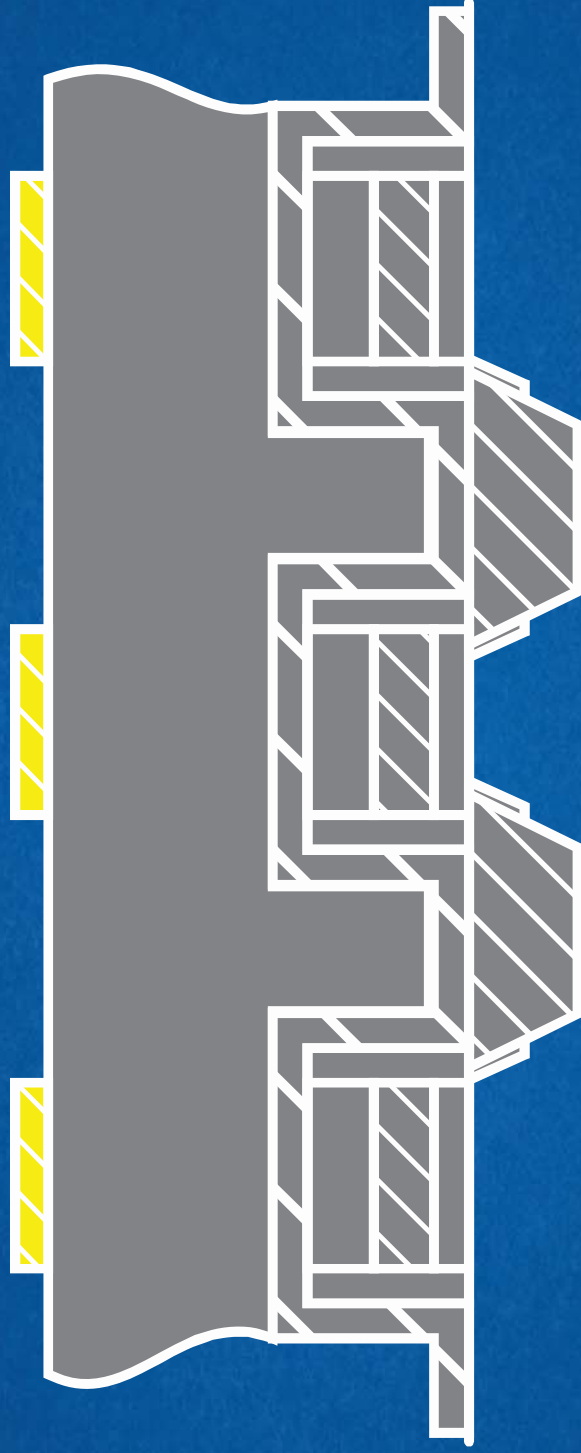
THE '552 PATENT



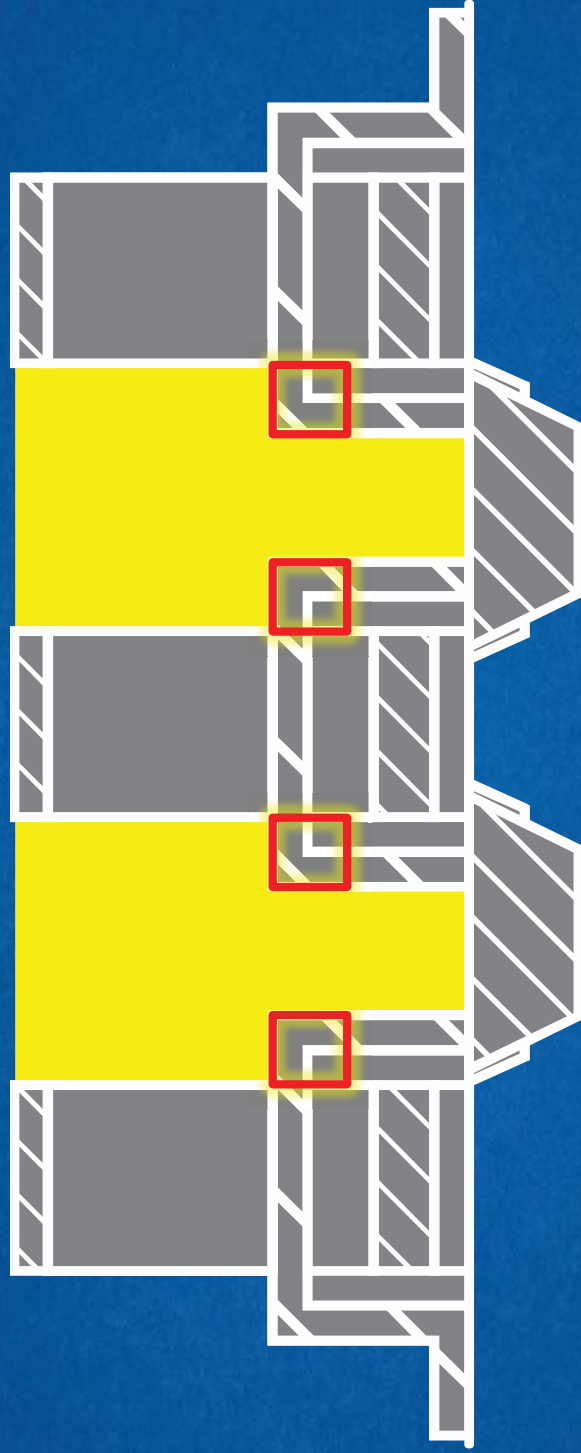
THE '552 PATENT



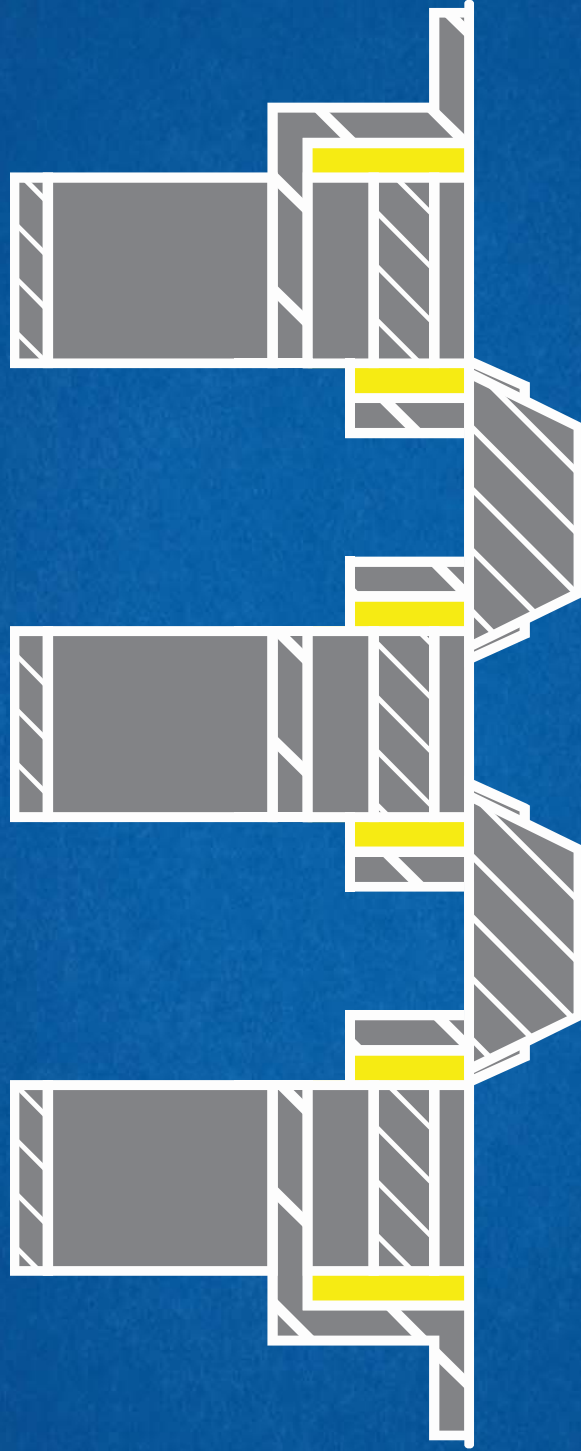
THE '552 PATENT



THE '552 PATENT



THE '552 PATENT



THE '552 PATENT

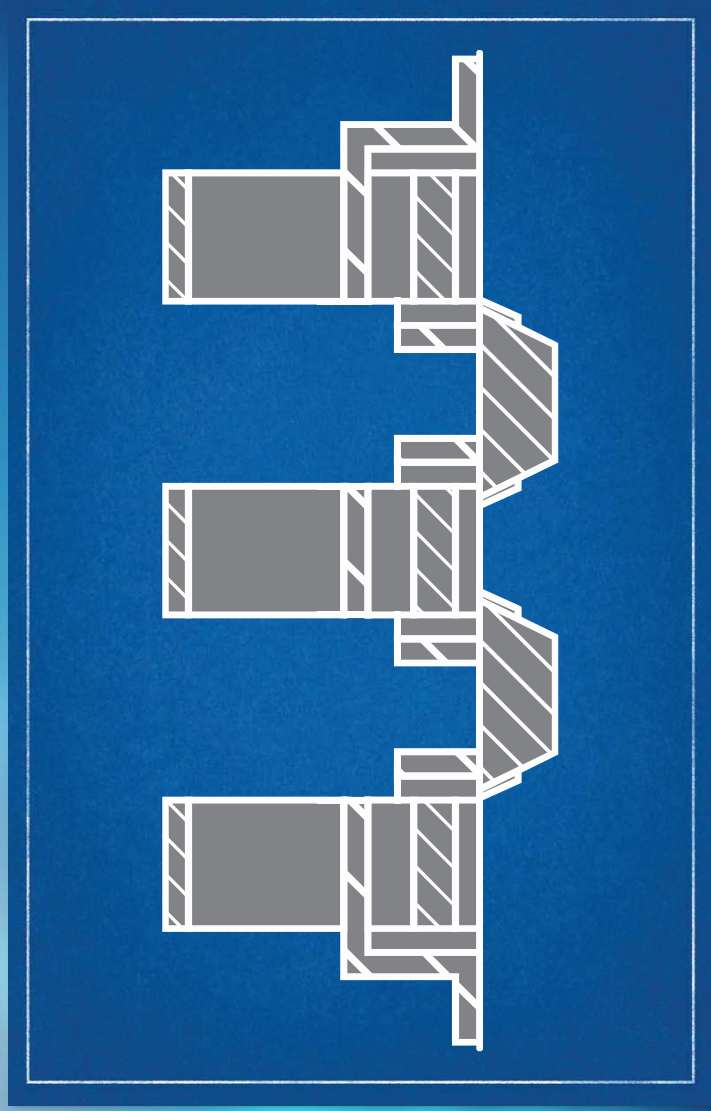


CLAIM 1 OF THE '552 PATENT

1. A structure, comprising:

- (a) a conductive layer disposed over a substrate;
 - (b) a first insulating layer on the conductive layer;
 - (c) a contact region in said first insulating layer;
 - (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and
 - (e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,
- wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

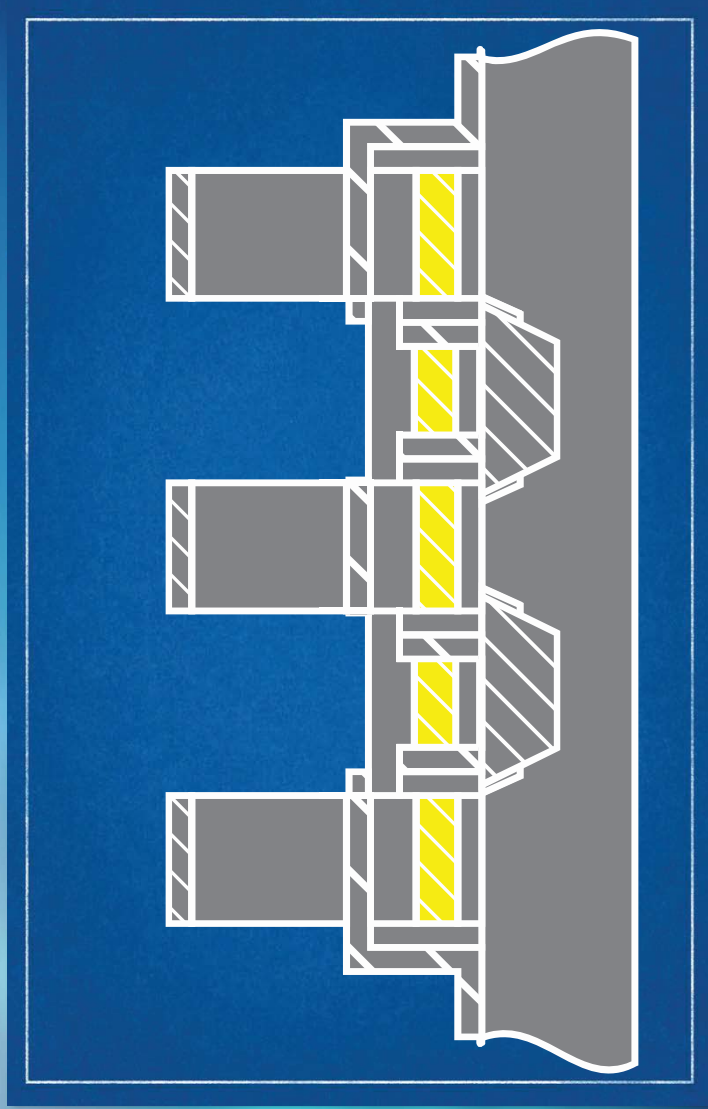
CLAIM 1 OF THE '552 PATENT



1. A structure, comprising:

- (a) a conductive layer disposed over a substrate;
 - (b) a first insulating layer on the conductive layer;
 - (c) a contact region in said first insulating layer;
 - (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and
 - (e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,
- wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

CLAIM 1 OF THE '552 PATENT



1. A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer:

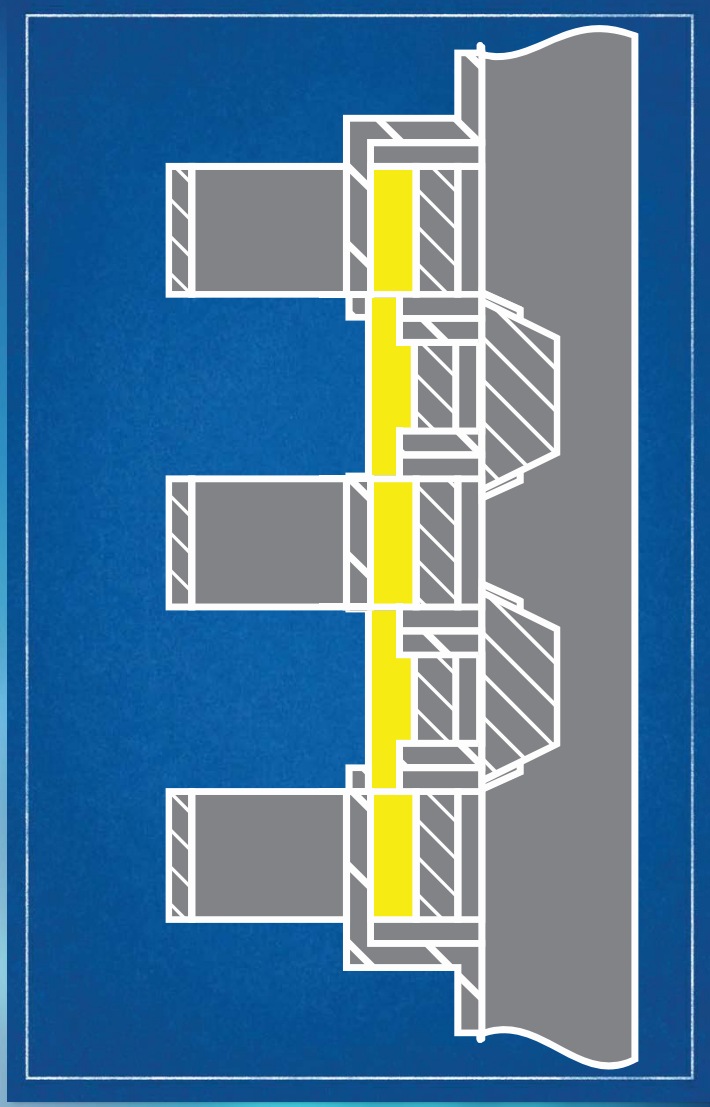
(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85° .

CLAIM 1 OF THE '552 PATENT



1. A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

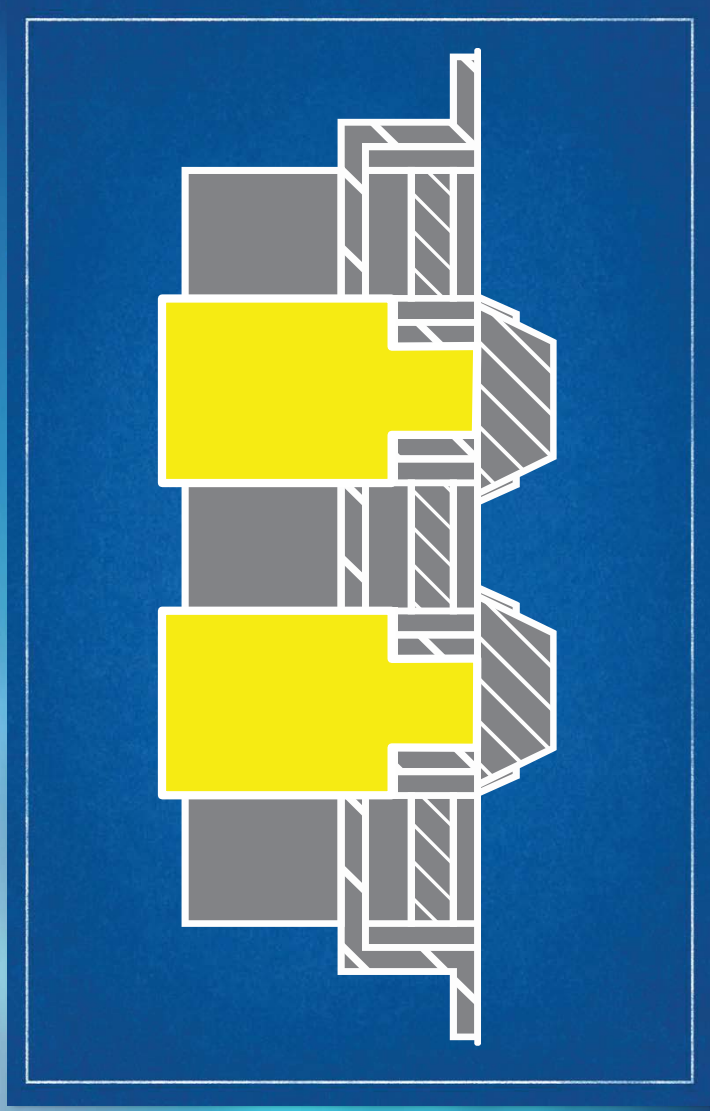
(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85° .

CLAIM 1 OF THE '552 PATENT



1. A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

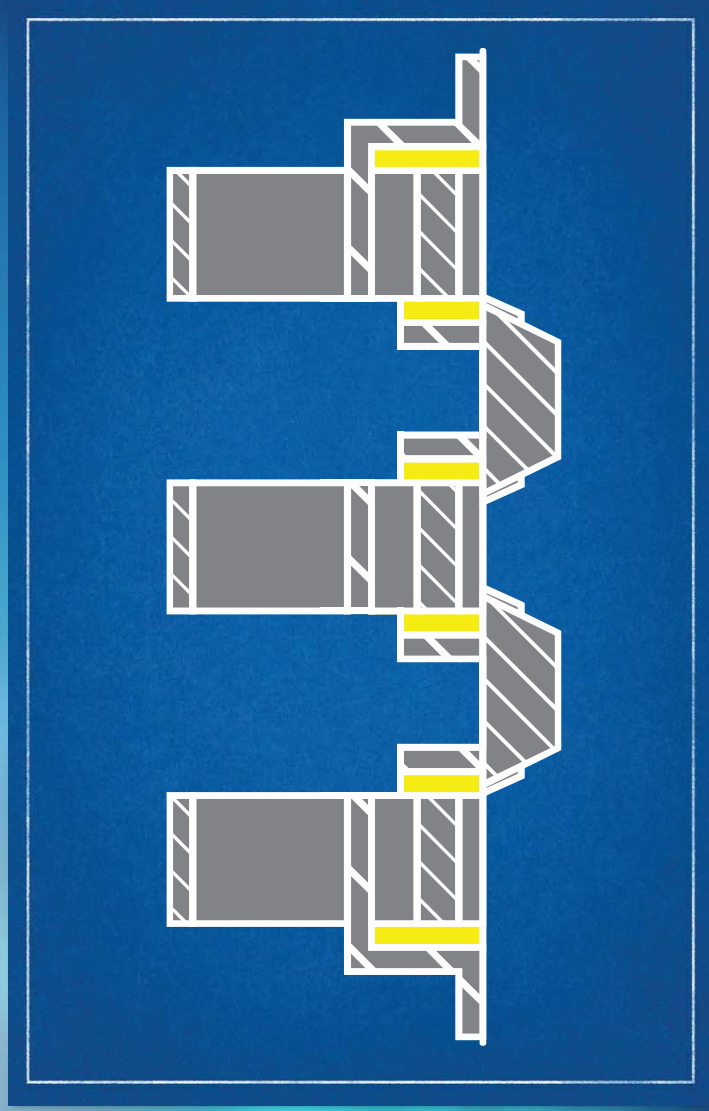
(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

CLAIM 1 OF THE '552 PATENT



1. A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

THE END