

DOCKET NO.: 54918.6

Filed on behalf of Qualcomm and GlobalFoundries

By: David M. O'Dell, Reg. No. 42,044
David L. McCombs, Reg. No. 32,271

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN MODULE
TWO LLC & CO. KG
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

Case IPR2016-01312

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 5,965,924
CHALLENGING CLAIMS 7-12, 15 and 17
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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Petitioner respectfully requests *Inter Partes* Review of claims 7-12, 15 and 17 of U.S. Patent No. 5,965,924 (the “’924 patent”) (Ex. 1101) pursuant to 35 U.S.C. §§ 311-19 and 37 C.F.R. § 42.1 *et seq.* The above-listed claims of the ’924 patent are presently the subject of a substantially identical petition for inter partes review styled *Intel Corporation v. DSS Technology Management, Inc.*, which was filed December 8, 2015 and assigned Case No. IPR2016-00289. Petitioner will seek joinder with that inter partes review under 35 U.S.C. § 315(c), 37 C.F.R. §§ 42.22 and 42.122(b).

I. INTRODUCTION

The ’924 patent claims a purportedly novel method for manufacturing transistors in semiconductors. But in fact, the claimed method merely duplicates a well-known technique disclosed by Osamu Sakamoto and others nearly three years before the alleged invention.

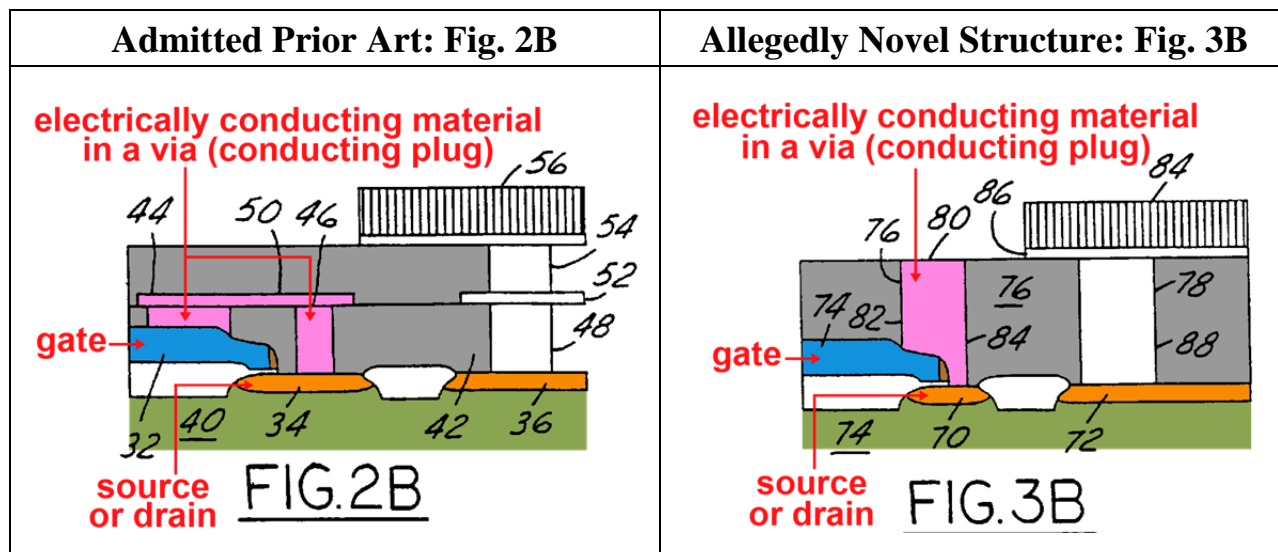
The ’924 patent is directed to certain aspects of the structure and fabrication of transistors used in semiconductor and integrated circuit products such as microprocessors and memory. Transistors act as microscopic switches that turn on and off at extraordinarily high rates to enable aggregations of transistors (and other components) to process data. Transistors are made up of various structures including “contacts” that provide electrically conductive pathways into and out of certain structures within a transistor, and which thereby are used to connect

transistors together. Declaration of Dr. Richard Blanchard (“Decl.”) ¶ 26 (Ex. 1102).

The ’924 patent is concerned with electrically connecting different transistor parts to each other in a particular way. Transistors typically have three terminals through which electrical signals may pass: a “source,” a “drain,” and a “gate.” The ’924 patent is concerned with connecting the gate of one transistor to, for example, the source or drain of a neighboring transistor. Decl. ¶ 27 (Ex. 1102).

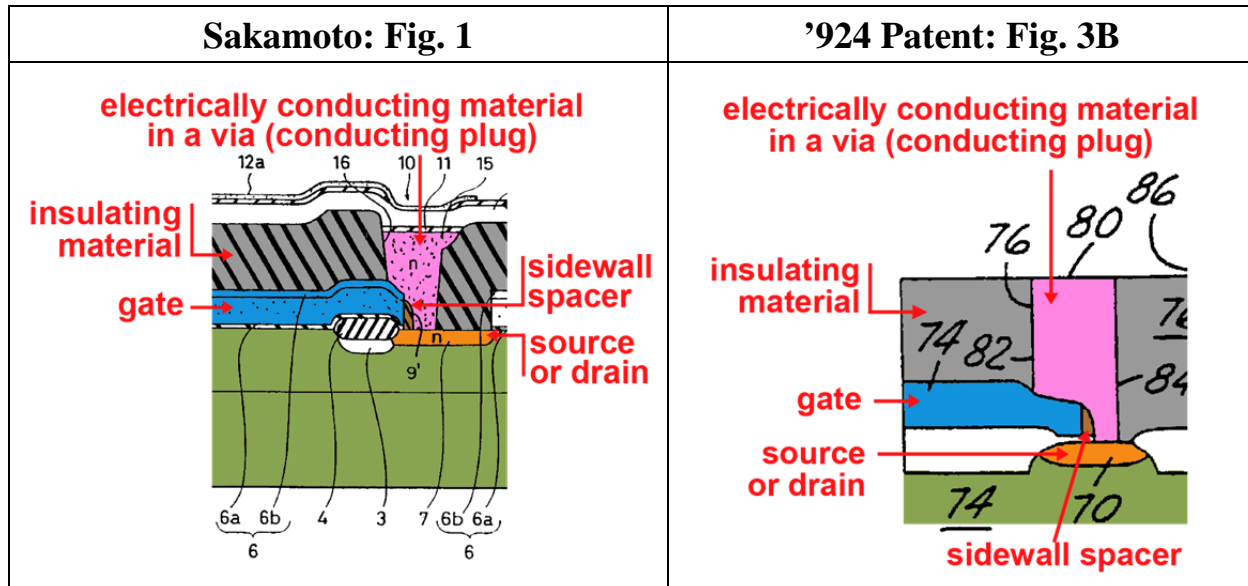
As the specification of the ’924 patent admits, there were many well-known ways of making electrical connections between different transistor parts. As shown in Figure 2B (below), for instance, one of the admitted prior art ways of connecting the components of two transistors was by using two electrical connections called “plugs”—one connected to the gate of one transistor, and the other connected to the source or drain of the other—and then connecting those plugs together. As shown in Figure 3B (below), the purported invention of the ’924 patent was to replace the two plugs with one plug. Decl. ¶ 28 (Ex. 1102).¹

¹ All emphasis and annotations are added unless otherwise indicated.



In both the admitted prior art (Figure 2B) and the allegedly novel structure of the '924 patent (Figure 3B), the **gate** is connected to a diffusion region (*i.e.*, a **source or drain**) by either two connected **plugs**, or a single **plug**. The patent does not claim that the one-plug structure provides any performance benefits over the two-plug structure. Instead, the only purported benefit was that the one-plug structure was easier to manufacture than the admitted prior art. '924 patent at 1:57-2:63, 4:18-5:12 (Ex. 1101); Decl. ¶ 29 (Ex. 1102).

But long before the '924 patent's November 22, 1995 priority date,² many others had already developed and used the exact same one-plug structure. U.S. Patent No. 5,475,240 ("Sakamoto"), for instance, which has an effective filing date of March 4, 1992, discloses the same one-plug structure that the '924 patent contends is novel. Specifically, as shown in the patents' respective figures, the one-plug structure of Sakamoto (Figure 1) is in all relevant aspects identical to the one-plug structure of the '924 patent (Figure 3B). Decl. ¶ 30 (Ex. 1102).

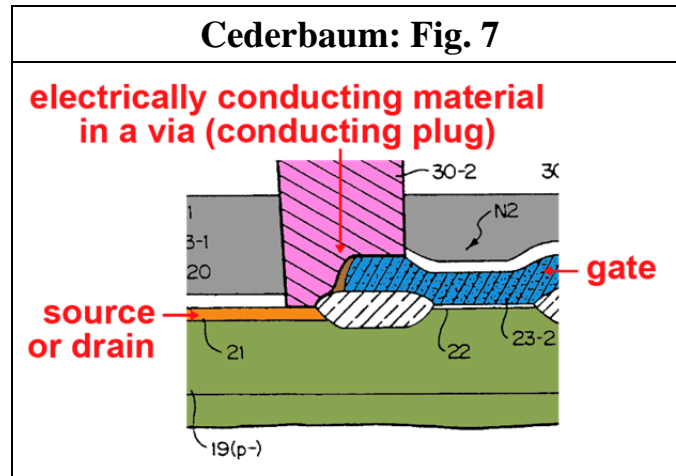


As shown, both structures include a **gate** connected to a **source or drain**

² The prior assignee claimed a conception date of May 17, 1995 during prosecution of the '924 application. Amendment and Rule 131 Declaration dated Jan. 5, 1998 (Ex. 1106). Even under that alleged conception date, the references relied upon by Petitioner all qualify as prior art and invalidate the '924 patent.

through a single **plug**. Decl. ¶ 31 (Ex. 1102).

Similarly, U.S. Patent No. 5,100,817 (“Cederbaum”) issued on March 31, 1992, and, just like the ’924 one-plug structure, discloses a single conducting **plug** connecting a **gate** to a **source or drain**. Decl. ¶ 32 (Ex. 1102).



These prior art references, which were not at issue during prosecution of the ’924 patent, anticipate and/or render obvious claims 7-12, 15 and 17 of the ’924 patent. Decl. ¶ 33 (Ex. 1102).

II. MANDATORY NOTICES

A. Real Party-in-Interest

Qualcomm Incorporated and GLOBALFOUNDRIES Inc.,
GLOBALFOUNDRIES U.S. Inc., GLOBALFOUNDRIES Dresden Module One
LLC & Co. KG, GLOBALFOUNDRIES Dresden Module Two LLC & Co. KG
(collectively “Petitioner”) are the real party-in-interest.

B. Related Matters

DSS has asserted the '924 patent in two separate proceedings: (1) *DSS Tech. Mgmt., Inc. v. Intel Corp. et al.*, Civil Action No. 6:15-CV-130-RWS (E.D. Tex. 2015); and (2) *DSS Tech. Mgmt., Inc. v. Qualcomm Inc.*, Civil Action No. 6:15-CV-692-JRG (E.D. Tex. 2015). These proceedings may be affected by a decision in this instant proceeding.

The '552 patent is currently being challenged before the Board in the following cases: *Intel Corporation v. DSS Technology Management, Inc.*, IPR2016-00289 and 00290. Also, the Petitioner is filing a separate *inter partes* review petition for claims 1-6, 13, 14 and 16 of the '924 patent.

C. Counsel

<u>Lead Counsel</u>	<u>Back-up Counsel</u>
David M. O'Dell HAYNES AND BOONE, LLP 2323 Victory Ave. Suite 700 Dallas, TX 75219 Phone: (972) 739-8635 Fax: (214) 200-0853 david.odell.ipr@haynesboone.com USPTO Customer No. 27683 USPTO Reg. No. 42,044	David L. McCombs HAYNES AND BOONE, LLP 2323 Victory Ave. Suite 700 Dallas, TX 75219 Phone: (214) 651-5533 Fax: (214) 200-0853 david.mccombs.ipr@haynesboone.com USPTO Customer No. 27683 USPTO Reg. No. 32,271

Please address all correspondence to lead and back-up counsel. Petitioner also consents to electronic service by email.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies pursuant to Rule 42.104(a) that the patent for which review is sought is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Pursuant to Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner challenges claims 7-12, 15 and 17 of the '924 patent.

A. Prior Art Patents

Petitioner relies upon the patents listed in the Table of Exhibits, including:

1. U.S. Pat. No. 5,475,240 ("Sakamoto" (Ex. 1103)), which was filed on August 19, 1994, as continuation of an earlier filed application filed on March 4, 1992, and issued on December 12, 1995. Sakamoto is prior art under 35 U.S.C. § 102(e).
2. U.S. Pat. No. 5,100,817 ("Cederbaum" (Ex. 1104)), which was issued on March 31, 1992, is prior art under 35 U.S.C. §§ 102(b).

B. Grounds for Challenge

Petitioner requests cancellation of claims 7-12, 15 and 17 of the '924 patent as unpatentable under 35 U.S.C. § 102 and § 103. This Petition, supported by the declaration of Dr. Richard Blanchard (Ex. 1102) filed herewith, demonstrates that

there is a reasonable likelihood that Petitioner will prevail with respect to cancellation of at least one challenged claim. *See* 35 U.S.C. § 314(a).

V. BRIEF DESCRIPTION OF TECHNOLOGY

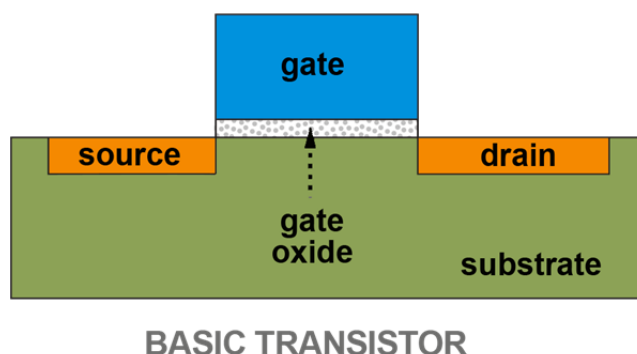
The '924 patent generally relates to the field of semiconductor integrated circuit manufacturing and claims particular structures for transistors in semiconductors, as well as a related method for manufacturing those structures. Decl. ¶ 34 (Ex. 1102).

A. Overview of Transistor Fabrication

1. Basic Structure of Transistors

Semiconductor integrated circuits, such as microprocessors and computer memory, are typically made up of hundreds of millions (and in some cases billions) of microscopic structures called transistors. Transistors act as microscopic switches that turn on and off at extraordinarily high rates to enable aggregations of transistors (and other components) to process data. Decl. ¶ 35 (Ex. 1102).

As shown in the figure below, transistors typically include three primary “electrodes” or “terminals”—a “gate,” a “source,” and a “drain.” Decl. ¶ 36 (Ex. 1102).

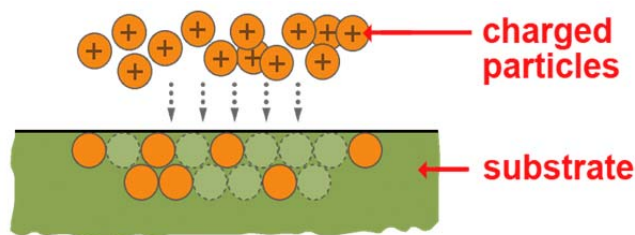


The source and drain regions (also referred to as “diffusion regions”) are transistor components that emit (source) and receive (drain) current when the transistor is “on.” The gate typically sits between the source and drain and is a terminal that can have a voltage applied to it that in turn causes a current to flow between the source and drain. As of the time of the invention of the ’924 patent, the source and drain of a transistor were typically formed in the surface of a semiconductor “substrate,” while the gate typically sat above the substrate and separated from it by a thin layer of insulator (“gate oxide”). Decl. ¶ 37 (Ex. 1102).

2. Formation of Transistor Components

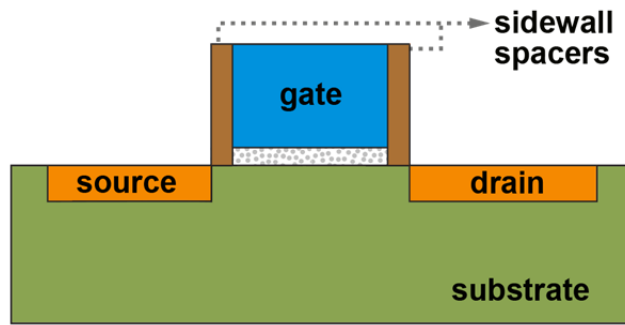
Transistor fabrication typically starts with a silicon substrate. In typical planar transistors, the source and drain regions (“diffusion regions”) are created by implanting regions of the substrate with ions (charged atomic particles) of different materials—called “dopants” or “impurities”—to make those regions conductive. (Once implanted the ions become neutral atoms). This process—referred to as

“doping” because it dopes the silicon substrate with atomic particles that have additional charge carriers—is shown below. Decl. ¶ 38 (Ex. 1102).



Structures can then be formed above the substrate by depositing layers of other materials onto the substrate. A gate electrode, for example, is formed by first growing or depositing a “gate oxide” (an insulator) on the substrate followed by depositing a conductive material (metal or polysilicon) on top of the gate oxide. The conductive material acts as the gate, and the gate oxide creates a layer of isolation between the gate and the source/drain regions (“S/D regions” or “diffusion regions”). Decl. ¶ 39 (Ex. 1102).

Insulating materials may then be deposited around and over the gate and the source/drain regions to maintain electrical isolation where desired. Sidewall spacers, for instance, can be formed on each side of the gate electrode as shown below.



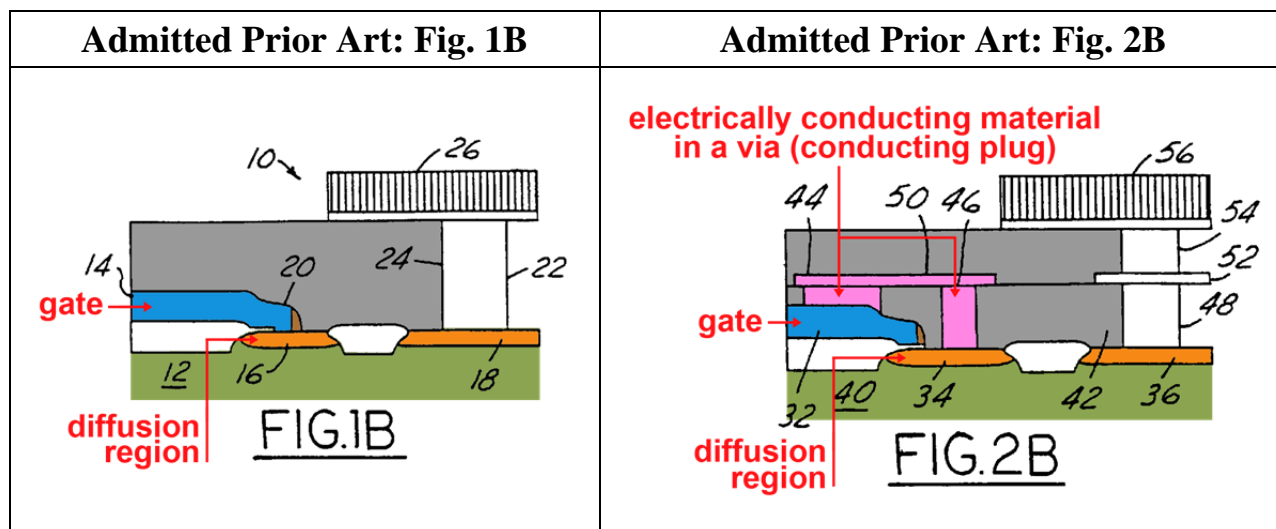
As was known as of the time of the alleged '924 invention, such sidewall spacers help to prevent direct electrical contact between the gate electrode and nearby components and thus help to prevent short-circuits. Decl. ¶ 40 (Ex. 1102).

3. Local Interconnects

Many transistors can be connected together to form electronic circuits. For certain types of circuits, it is sometimes useful to connect the gate of one transistor to a diffusion region (the source or drain) of a nearby transistor. This type of connection is called a “local interconnect,” because connections are made locally between nearby transistors. Decl. ¶ 41 (Ex. 1102).

As the specification of the '924 patent concedes, a variety of different types of local interconnects were well-known prior to the purported invention. For example, as shown in Figure 1B of the '924 patent, one well-known way to form a local interconnect was to position the gate in a location where it physically touches the diffusion region on one side, creating an electrical connection. As shown in Figure 2B of the '924 patent, another well-known way to make a local interconnect

was to place one electrically conductive “plug” above the gate and another “plug” above the diffusion (e.g., source or drain) region, and then electrically connect the two plugs together. Decl. ¶ 42 (Ex. 1102).



The '924 patent acknowledges that both examples were known prior art. See '924 patent at Figs. 1A, 1B, 2A, 2B, 1:25-2:45, 3:30-35 (Ex. 1101); Decl. ¶ 43 (Ex. 1102).

B. Overview of the '924 Patent

The '924 patent issued from U.S. App. No. 08/900,047, which was filed on July 24, 1997, and claims priority to an application filed on November 22, 1995. '924 patent at cover page (Ex. 1101). The purported invention of the '924 patent is a single plug to connect different transistor parts. '924 patent at 2:32-67, 4:18-5:12 (Ex. 1101); Decl. ¶ 44 (Ex. 1102).

1. Alleged Problem

The '924 patent purports to address manufacturing inefficiencies in forming local interconnects. Figures 1 and 2 of the '924 patent are admitted prior art and show examples of two well-known types of local interconnects that (according to the '924 patent) are inefficient to manufacture. Decl. ¶ 45 (Ex. 1102).

Figure 1B shows a “buried contact” local interconnect structure in which the gate directly touches—*i.e.*, is in direct electrical connection with—a diffusion region. According to the '924 patent, the problem with this structure is that the gate has to be implanted with the same type of impurities as those implanted in the diffusion region. *See* '924 patent at 1:57-2:11 (Ex. 1101). But most manufacturers use a variety of different types of impurities in different transistors. To use the “buried contact” approach, a manufacturer would have to ensure that any two transistors connected using this approach use the same impurities, which complicates the manufacturing process. *See id.*; *see also* Decl. ¶ 46 (Ex. 1102).

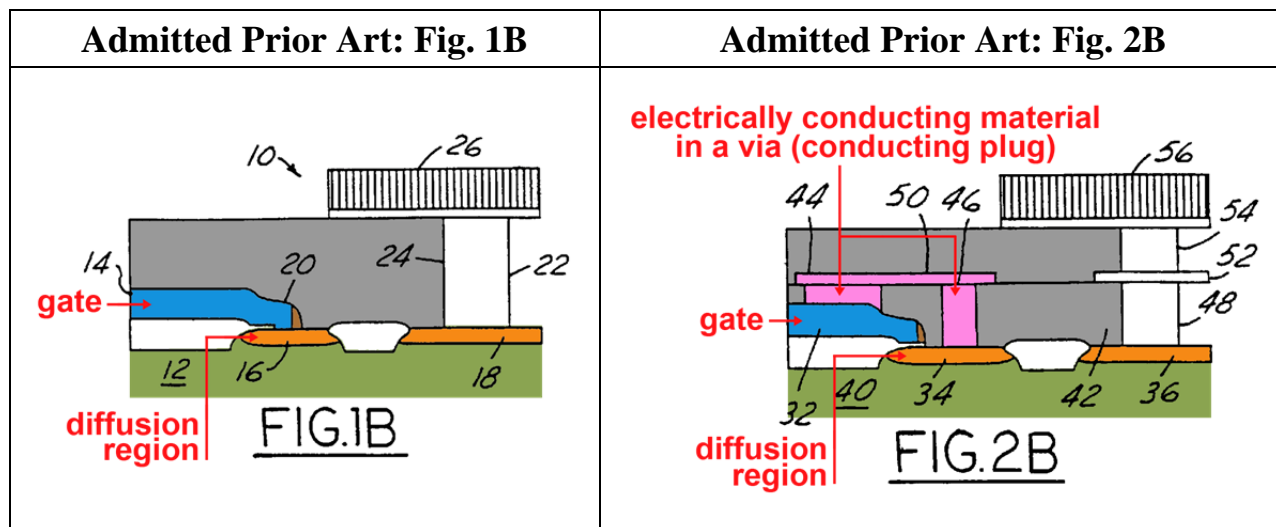
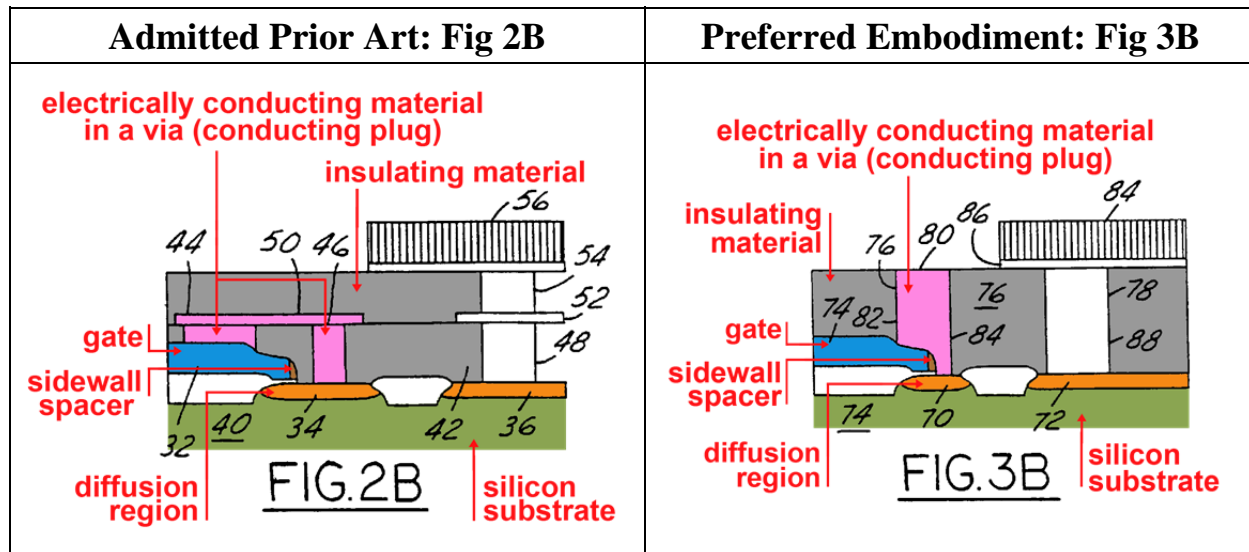


Figure 2B shows another prior art local interconnect structure, using what is called a “strapping” technique. To form this “strapping” local interconnect structure, a manufacturer creates two electrically conductive **plugs** (numbers 44 and 46)—one above the **gate** and one above a **diffusion region**. The manufacturer then places an electrically conductive “**local strap**” (number 50) on top of the **plugs**, electrically connecting the two **plugs** together. This **local strap** is also sometimes called a “shunt” or a “shunt layer.” In combination, the two **plugs** and the **local strap** electrically connect the **gate** to a **diffusion region**. See ’924 patent at 2:12-32 (Ex. 1101). According to the ’924 patent, the problem with the strapping technique is that it requires a large number of manufacturing process steps, as well as significant space to accommodate the two plugs and the local strap. See ’924 patent at 2:33-41 (Ex. 1101); *see also* Decl. ¶ 47 (Ex. 1102).

2. Summary of Alleged Invention of the '924 Patent

The '924 patent's claimed structure includes nearly identical components as the admitted prior art described in the specification. Decl. ¶ 48 (Ex. 1102). Specifically, both the claimed structure and the admitted prior art include a substrate, a gate, a diffusion region, a sidewall spacer adjacent to the gate, and an insulating material. Decl. ¶ 48 (Ex. 1102).



As shown in Figures 2B and 3B, in both the admitted prior art of the '924 patent and the allegedly novel structure, the gate is connected to the diffusion region (source or drain), by either two connected plugs, or a single plug. The diffusion region is located in a substrate and is not directly connected to the gate. The gate is substantially covered by an insulating material. Decl. ¶ 49 (Ex. 1102).

The patent's only alleged novelty—shown in Figure 3B—is the use of a single metal plug to connect the gate and the diffusion region, rather than

connecting the two components directly (as in the prior art “buried contact” technique (Figure 1B)) or using two plugs (as in the prior art “strapping” technique (Figure 2B)). ’924 patent at 2:64-67, 3:35-36 (describing Figure 3B as “a cross-sectional view of a preferred embodiment of the present invention.”), 4:18-5:12, claims 1, 7 (Ex. 1101); *see also id.* at 2:42-63; Decl. ¶ 50 (Ex. 1102).

But as explained below, there is nothing novel about using a single conducting plug.

3. The Challenged Claims

This petition challenges claims 7-12, 15 and 17 of the ’924 patent. Independent claim 7 describes a method of forming a local interconnect in a semiconductor structure, in which a plug provides a direct electrical connection between a diffusion region formed in a substrate and a gate formed on top of the substrate. ’924 patent at claim 7 (Ex. 1101). Claim 7 also specifies additional well known features, including a sidewall spacer and insulating material on the gate, as noted below.

7. A method of forming a local interconnect in a semiconductor structure, comprising the step of:

[a] depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication

between said gate and said diffusion region,

[b] said semiconductor structure comprising said diffusion region in a silicon substrate,

[c] said gate being on said substrate juxtaposed to but not contacting said diffusion region,

[d] said sidewall spacer being disposed above said diffusion region,

[e] said via being in an insulating material on said gate.

The dependent claims add well-known implementation details such as defining particular types of diffusion regions (*id.* at claim 8), insulating material (*id.* at claim 9), conducting plug material (*id.* at claims 10-12), and gate material (*id.* at claims 15, 17).

4. Prosecution History

The '924 patent issued from a “continued prosecution application” (“CPA”) of U.S. App. No. 08/561,951. CPA Request dated Feb. 10, 1999 (Ex. 1105). During prosecution of the '924 patent, the Applicant purportedly antedated a prior art reference, based on a lab notebook dated May 17, 1995. Amendment and Rule 131 Declaration dated Jan. 5, 1998 (Ex. 1106). For purposes of this Petition, the references relied upon by Petitioner all qualify as prior art even if the Patent Owner could ultimately prove a conception date as early as May 17, 1995. Decl. ¶ 51 (Ex. 1102).

According to this lab notebook, the purported novelty of the '924 invention arises from the use of a single plug—which is what allegedly leads to fewer processing steps as compared to known prior art techniques. *See* Rule 131 Declaration dated January 5, 1998, Exhibit A (“By *placing a metallic plugged contact* where poly is required to shunt to diffusion, contacts to [different types of] diffusion can be achieved [T]his will require no more layout area than the traditional buried contact. This method has potential [manufacturing] process step savings of 8-11 steps over Trad. BC [traditional buried contact local interconnect (as shown in Figure 1B of the '924 patent)] and 6-8 steps over strapping [local interconnect (as shown in Figure 2B of the '924 patent)].”) (Ex. 1106). Decl. ¶ 52 (Ex. 1102).

However, during prosecution, rather than relying on the supposedly novel “single plug” structure, the Applicant relied on other alleged differences to overcome the prior art applied by the Examiner. The present petition relies on new art—not before the Examiner—that teaches not only the allegedly novel “single plug” aspect of the invention, but also all of the additional minor differences that the Applicant used to allegedly distinguish the Examiner’s prior art. Decl. ¶ 53 (Ex. 1102).

a) The “sidewall spacer” limitations

The Examiner rejected the original claims under 35 U.S.C. § 102(e) based on U.S. Patent No. 5,451,434 to Nicholls (“Nicholls”). Office Action dated Nov. 7, 1996 at p. 3 (Ex. 1107). Nicholls taught a single metal plug that connects a diffusion region and a gate. In order to overcome the rejection, the Applicant added a limitation to the claims requiring a sidewall spacer adjacent to the gate. Amendment dated June 9, 1997 at pp. 2-3 (Ex. 1109). Nicholls expressly teaches the placement of a sidewall during manufacture, but also teaches that the sidewall can be completely or “partially removed” in a later manufacturing step. Nicholls at 4:25-32 (Ex. 1108). The Applicant overcame the rejection by arguing that the removal of the sidewall during manufacturing taught away from retaining a sidewall spacer adjacent to the gate. Amendment dated June 9, 1997 at pp. 3-4 (Ex. 1109). The prior art relied upon in this petition teaches the “sidewall spacer” limitation. Decl. ¶ 54 (Ex. 1102).

b) Direct electrical connection

The Examiner also rejected the claims under 35 U.S.C. § 102(e) based on U.S. Patent No. 5,541,427 to Chappell (“Chappell”). Office Action dated February 24, 1998 (Ex. 1110). Chappell taught a single metal plug that connects to both a diffusion region and a gate region. Chappell at 4:38-48 (Ex. 1111). The Applicant overcame the rejection by arguing that the metal plug of Chappell purportedly

contacts a portion of the gate region that is not conductive, rather than the conductive portion of the gate itself. *See* Amendment dated April 23, 1998 at p. 4 (“when the opening 42 is filled with an electrically conductive material, there is **no contact** to the electrically conductive portion of the gate stack”) (emphasis in original) (quoting Chappell at 4:38-48) (Ex. 1112). The prior art references relied upon in this petition teach a direct electrical connection between the diffusion region and the electrically conductive portion of the gate. Decl. ¶ 55 (Ex. 1102).

VI. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES

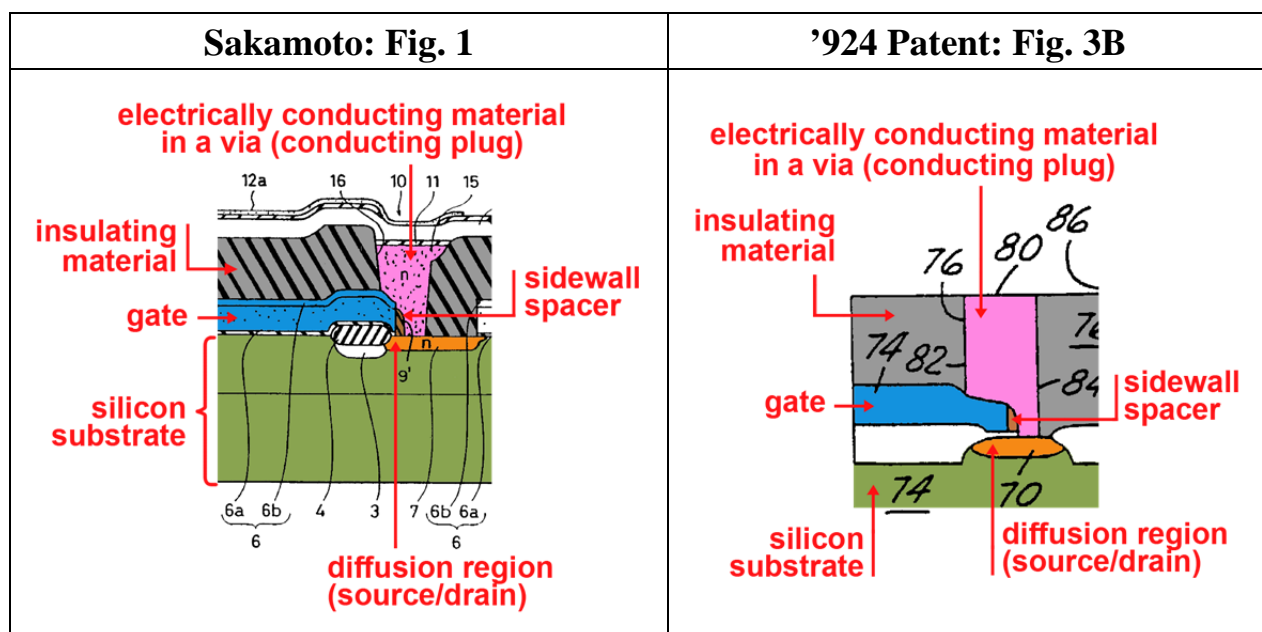
The claimed invention of the '924 patent—using a single plug to electrically connect the gate to the diffusion region—was well-known as of the May 17, 1995 purported conception date. Decl. ¶ 56 (Ex. 1102). Each of the prior art references relied upon in this petition has an effective filing date earlier than that alleged conception date.

A. Overview of Sakamoto

Sakamoto was filed on August 19, 1994, as a continuation of an earlier application filed on March 4, 1992, and issued on December 12, 1995. It is therefore prior art to the '924 patent under 35 U.S.C. § 102(e). Decl. ¶ 57 (Ex. 1102).

Sakamoto is directed to precisely the same problem as the '924 patent—how to effectively and efficiently connect different transistor portions together —and

discloses precisely the same solution claimed in the '924 patent—using a single plug. Sakamoto at 4:45-49 (“The first interconnection structure comprises a silicon plug layer embedded within an opening formed in the interlevel insulating layer and connected to both gate electrode of the first MOS drive transistor and source/drain region of the second MOS transfer transistor...”)(Ex. 1103); *see also id.* at 1:13-14. Figure 1 of Sakamoto shows a structure with the same components arranged in the same way as shown in Figure 3B of the '924 patent. *Id.* at Fig. 1; '924 patent at Fig. 3B (Ex. 1101); Decl. ¶ 58 (Ex. 1102).

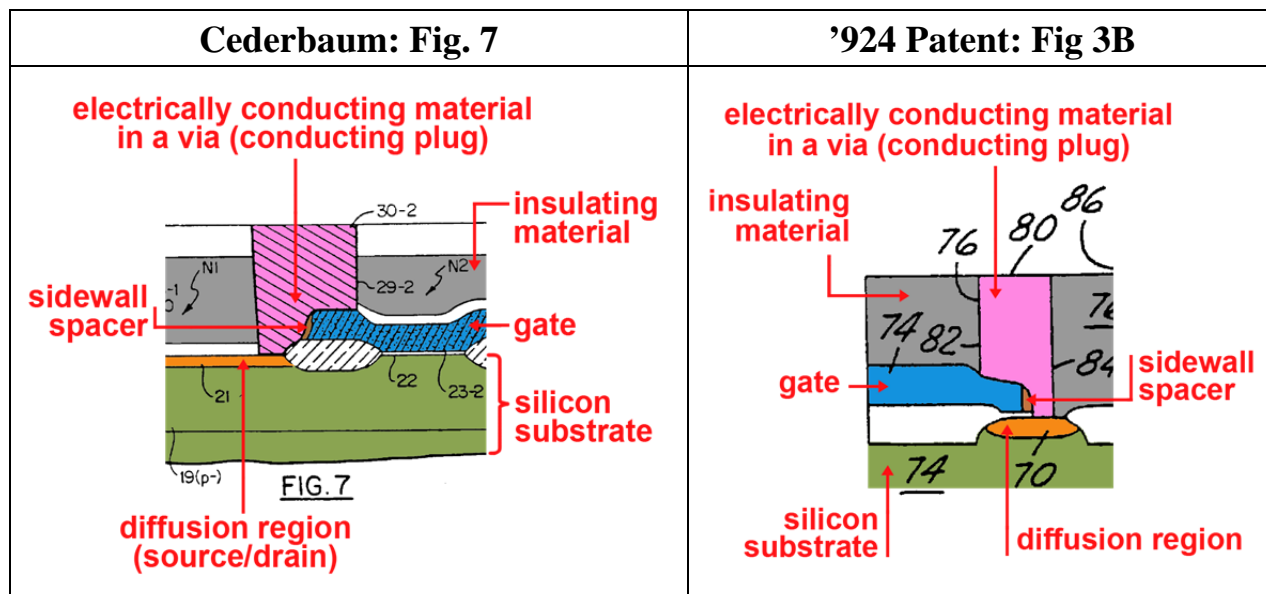


Both Figure 1 of Sakamoto and Figure 3B of the '924 patent show a cross-sectional structure with a single **plug**. The **plug** fills an opening (labeled 16 in Sakamoto) containing a **sidewall spacer** and directly electrically connects a **diffusion region** to a **gate**. The **diffusion region** is located in a **substrate** and is not

directly connected to the [gate](#). The gate is also substantially covered by an insulating material. *See* Sakamoto at 6:52-58 (“An opening 16 is formed in an interlevel insulating layer 9. An n+ [source/drain region 7](#) of an n channel MOS transfer transistor 22b and a [gate electrode 6](#) of an n channel MOS drive transistor 20a are exposed at the bottom of opening 16. A [plug layer 15](#) of polycrystalline silicon directly connected to the n+ [source/drain region 7](#) and [gate electrode 6](#) is embedded within opening 16.”), 7:47-51 (“An opening 16 for direct contact is formed in interlevel insulating layer 9 ... formation of the opening 16 leaving a [sidewall spacer 9'](#) from the interlevel insulating layer 9 ...”), 7:26-27 (“Oxide films 5 form gate oxide films 5,5 of MOS transistors 20a, 22b.”) (Ex. 1103); *see also* ’924 patent at 3:46-4:17 (Ex. 1101). Thus, Sakamoto and the ’924 patent both solve the same problem of connecting different transistor portions (e.g., source/drain to gate) by using a single plug interconnect. Sakamoto at 6:49-7:13 (Ex. 1103); Decl. ¶ 59 (Ex. 1102).

B. Overview of Cederbaum

Cederbaum issued on March 31, 1992 and is prior art under 35 U.S.C. § 102(b). Figure 7 of Cederbaum also discloses a structure that includes components arranged in a way that is identical in all relevant aspects as the structure in Figure 3B of the ’924 patent. Cederbaum at Fig. 7 (Ex. 1104); ’924 patent at Fig. 3B (Ex. 1101); Decl. ¶ 60 (Ex. 1102).



Both Figure 7 of Cederbaum and Figure 3B of the '924 patent show a single **plug** (which Cederbaum calls a “**contact stud**”). The **plug** fills an opening (labeled 28-2 (Figure 6) in Cederbaum) containing a **sidewall spacer** and directly connects the **source/drain region** to the **gate**. See Cederbaum at Figs. 4-7, 7:33-49 (Figs. 4-7 show “**active regions 21** ... to constitute the **source and drain regions**” and “[n]umeral[] ... 23-2 designate[s] ... the **gate electrodes** ...”), 7:49-57 (“Oxide **sidewalls** or spacers 24 have been formed on the lateral sides of the polysilicon **gate electrodes** for a better definition of the channel length of NFETs.”) (Ex. 1104). The **diffusion region** is located in a **substrate**, and not directly connected to the **gate**, which is substantially covered by the **insulating material**. Cederbaum at 7:33-40 (“The starting material consists of a conventional P⁺ silicon substrate 18 having a P⁻ epitaxial layer 19.... N⁺ implanted active regions 21 have been formed

in the epitaxial layer 19 to constitute the source and drain regions....”), 8:26-50 (explaining the formation of the insulating phosphosilicate glass (PSG) layer 26 over the gate and substrate) (Ex. 1104). The **contact stud** is created by filling the opening with a “highly conductive material” that is “typically a metal.” *Id.* at 9:32-34, 9:35-43 (“Prior to tungsten (W) filling, a titanium (Ti) layer is deposited” followed by “a thin titanium nitride (TiN).”); Decl. ¶ 61 (Ex. 1102).

VII. CLAIM CONSTRUCTION

The '924 patent expired on November 22, 2015. Accordingly, Petitioner has applied claim construction based on the *Phillips* standard rather than the broadest reasonable interpretation standard applicable to non-expired patents. *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (Board review of expired patent claims is “similar to that of a district court’s review”); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-14 (Fed. Cir. 2005) (*en banc*) (describing process for construing claims in district court).³

A. “diffusion region in a silicon substrate”

The term “diffusion region in a silicon substrate” is an element of all challenged claims. The term should be construed to mean a “conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon

³ Under either standard, the '924 patent is invalid.

substrate.” In its pending litigation with Petitioner, the Patent Owner has proposed to construe the term as a “conductive terminal region such as a source or drain in a silicon substrate.” The Patent Owner thus agrees with Petitioner that the term requires a conductive terminal region, such as a source or drain, in the silicon substrate. As a result, the only dispute between the parties is whether the diffusion region “contains dopants implanted in the silicon substrate.” The patent makes clear that it does. Decl. ¶ 63 (Ex. 1102).

The plain language of the claims requires the diffusion region to be formed in the silicon substrate. Claim 1, for example, requires a “diffusion region formed in said [silicon] substrate.” ’924 patent at claim 1 (Ex. 1101). Similarly, claim 7 requires a “diffusion region in a silicon substrate.” *Id.* at claim 7. The specification then explains, in a section describing “[t]he present invention,” that the diffusion region is formed in the substrate by implanting dopants in the substrate:

The present invention provides a semiconductor structure that has a metal plug local interconnect (or shunt) for connecting a polysilicon gate to a diffusion region in a structure and a method of forming such a semiconductor structure.

Referring initially to FIGS. 3A and 3B wherein an enlarged top view and a cross-sectional view of the

present invention metal plug local interconnect is shown, respectively. Diffusion regions 70 and 72 of either *N+ or P+ doping* are first formed by an *ion implantation* process in the *surface of the silicon substrate* 74.

'924 patent at 3:40-51 (Ex. 1101); *see also id.* at 1:36-38 (explaining that the “ion implantation process ... increase[s] the surface dopant concentration” in substrate), 1:21-22 (describing “region doped by impurity ions in a semiconductor substrate”). The '924 patent does not describe any way of forming diffusion regions in a silicon substrate other than by implanting dopants in the substrate. Decl. ¶ 64 (Ex. 1102). Accordingly, consistent with Petitioner’s proposed construction, the '924 patent makes clear that the claimed diffusion regions contain dopants implanted in the substrate. Decl. ¶ 64 (Ex. 1102).

Moreover, at the time of the alleged invention of the '924 patent, one skilled in the art would have readily understood that a diffusion region is a conductive terminal region, such as a source or drain, that contains dopants implanted in the substrate. *See* Decl. ¶ 65 (Ex. 1102). As Dr. Blanchard explains, in order to form a diffusion region in a substrate, the dopants need to be inserted into the substrate. As the '924 patent explains, at the time of the alleged invention, this was done by implanting dopants into the substrate. Decl. ¶ 65 (Ex. 1102). This is confirmed by contemporaneous prior art references. Sakamoto and Nicholls, for example, teach

the use of ion implantation to form a diffusion region. Sakamoto at 7:32-38 (“N type impurity *ion* ... is *implanted* ... by an ion implantation method.... Thus, *n+* *source/drain regions* ... are formed.”) (Ex. 1103); Nicholls at 2:64-66 (“As shown in FIG. 1b, a *dopant* is then *implanted* into the silicon substrate so as to form active silicon implant regions 8, 10”), 3:55-4:13 (Ex. 1108). Decl. ¶ 65 (Ex. 1102).

Accordingly, the term “diffusion region in a silicon substrate” should be construed to mean a “conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate.”⁴ Decl. ¶ 66 (Ex. 1102).

⁴ In the pending litigation between the Patent Owner and Petitioner, the parties have proposed competing constructions for one additional limitation. But because the prior art indisputably meets this limitation under either party’s construction, it does not need to be construed for the purposes of this petition. (Petitioner believes the prior art also discloses the required “diffusion region in a silicon substrate” limitation under either party’s construction but understands that Patent Owner may dispute that.) Decl. ¶ 66 fn.2 (Ex. 1102). The parties’ constructions, claim construction filings, and schedule for claim construction are set forth in Exhibit 1118.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention would have had at least a B.S. degree in electrical engineering or materials science (or equivalent experience), and would have at least two or three years of experience with semiconductor device fabrication and design. Decl. ¶ 67 (Ex. 1102).

IX. SPECIFIC GROUNDS FOR PETITION

Sakamoto anticipates claims 7-9, 15 and 17 of the '924 patent (Ground I), and, in combination with Cederbaum, renders claims 10-12 obvious (Ground II). The sections below, as confirmed by the Blanchard Declaration, demonstrate how the claims are anticipated or rendered obvious by the prior art. *See* 37 C.F.R. 42.104(b)(4)-(5).

A. Ground I: Claims 7-9, 15 and 17 are anticipated by Sakamoto

1. Independent Claim 7

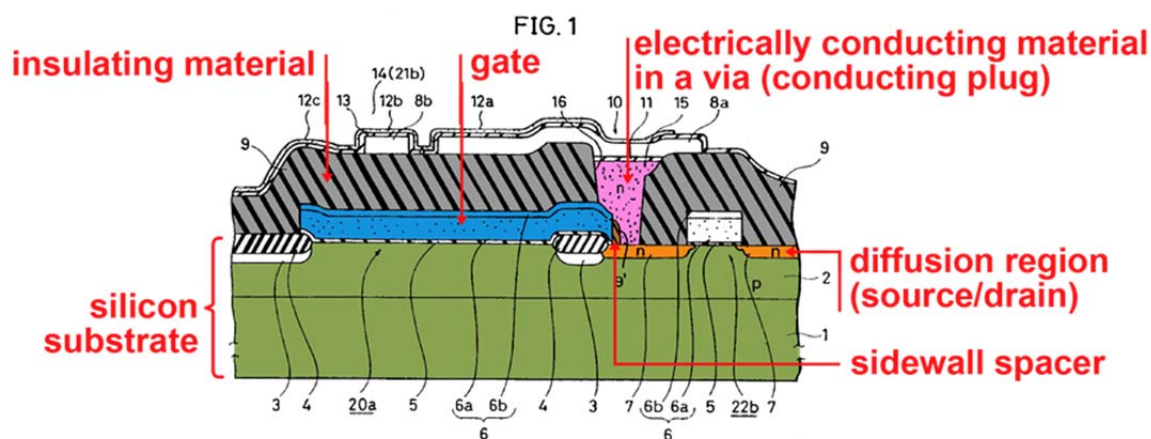
Sakamoto discloses each and every element of claim 7 and thus, anticipates the claim under 35 U.S.C. § 102(e). Decl. ¶ 69 (Ex. 1102).

a) “A method of forming a local interconnect in a semiconductor structure, comprising the step of:”

Sakamoto expressly discloses a method of forming a local interconnect by describing a series of “[s]teps of manufacturing the memory cell of the SRAM shown in FIG. 1.” Sakamoto at 7:14-15 (Ex. 1103); *see also id.* at 7:16-8:52. One

skilled in the art would understand that the SRAM memory cell of Sakamoto discloses “a semiconductor structure.” Decl. ¶ 70 (Ex. 1102); Sakamoto at Fig. 1, 6:39-8:52 (describing Figure 1), Title (“Contact structure of an interconnection layer for a *semiconductor device* and a multilayer interconnection SRAM”), 1:13-16 (“The present invention relates to improvement of a contact structure of an interconnection in a region having steps in *a semiconductor device* having a multilayer interconnection structure.”) (Ex. 1103); *see also id.* at claims 1-9, Abstract, Title, 1:18-3:35, 3:60-4:2, 5:1-18, 5:33-50, 13:13-25. Decl. ¶ 70 (Ex. 1102).

Figure 1 of Sakamoto (shown below) discloses a local interconnect structure:

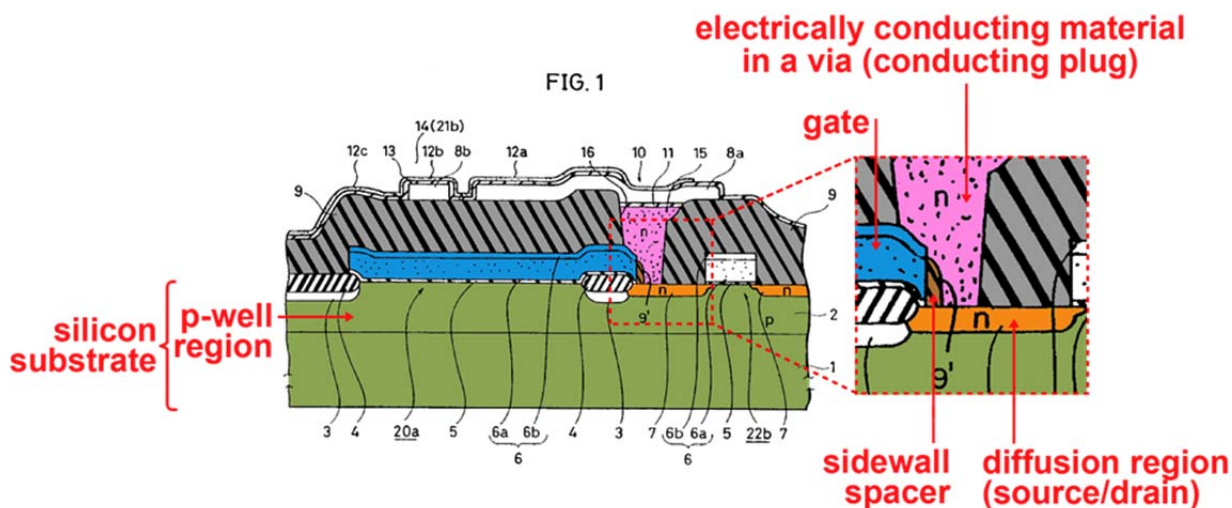


Sakamoto at Fig. 1, 6:39-8:52 (describing Figure 1), claims 1-9, 3:55-57 (an “object of the present invention is to provide a method of manufacturing an

interconnection having an interconnection structure....”), Title, Abstract, 1:13-16, 3:38-59 (Ex. 1103); Decl. ¶ 71 (Ex. 1102).

b) [a]: “depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region”

Sakamoto discloses the claimed electrically conducting material. Figure 1 (which is the structure formed by the manufacturing method disclosed in Sakamoto) shows (and Sakamoto explains) depositing an electrically conducting material (plug layer 15) in a via (opening 16):

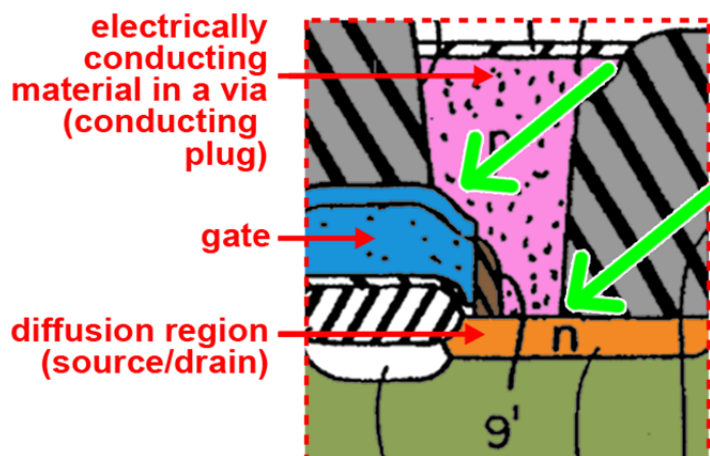


Sakamoto at Fig. 1 (Ex. 1103); *see also id.* at Figs. 2-5, claims 1, 4, and 7, 6:49-7:14 (“An opening 16 is formed in an interlevel insulating layer 9 A plug layer 15... directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16.”), 7:15-8:12 (plug layer 15 is formed when

“[p]olycrystalline silicon layer 15a is deposited ... to fill opening 16 [and] is etched, leaving a portion of the ... layer only within opening 16....”). Decl. ¶ 72 (Ex. 1102).

As shown in the figure above, absent the **conducting material 15**, the via exposes at least a portion of the gate (**gate electrode 6**), a sidewall spacer (**sidewall spacer 9'**) that is adjacent to the gate (**gate electrode 6**) and a portion of a diffusion region (n+ **source/drain region 7**). Compare Sakamoto at Fig. 2 (showing portion of **gate electrode 6**, **sidewall spacer 9'** and portion of n+ **source/drain region 7** exposed in opening 16 during manufacturing process before **plug 15** is formed) with Fig. 4 (showing **plug 15** covering portion of **gate electrode 6**, **sidewall spacer 9'** and portion of n+ **source/drain region 7** later in the process) (Ex. 1103). See also *id.* at Fig. 1, 6:52-55 (“[a]n n+ **source/drain region 7** ... and a **gate electrode 6** ... **are exposed** at the bottom of opening 16.”), 7:46-50 (“a **sidewall spacer 9'**” is located in the opening 16), 2:49-52, claims 4, 6, 7 and 9. Decl. ¶ 73 (Because Sakamoto teaches the **source/drain 7 region** and **gate electrode 6** are “exposed” by opening 16, the **sidewall spacer 9'** is also exposed by the opening 16) (Ex. 1102).

Figure 1 also shows (and Sakamoto explains) that the electrically conducting material (**plug layer 15**) contacts and provides direct electrical communication between the **gate** and the **diffusion region**:



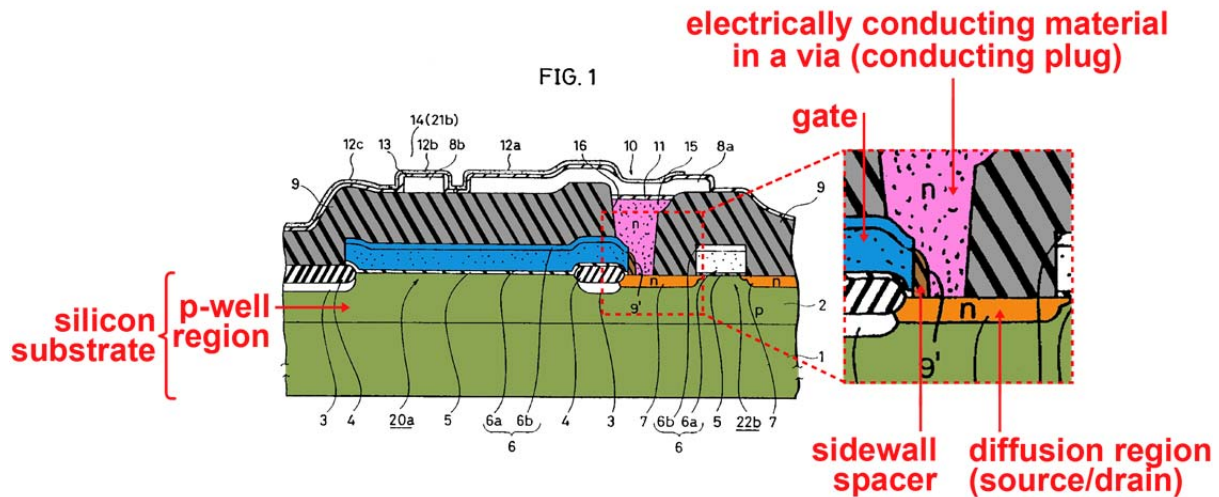
Sakamoto at Fig. 1, 6:49-7:14 (“An opening 16 is formed.... A **plug layer 15** of polycrystalline silicon *directly connected* to the n+ **source/drain region 7** and **gate electrode 6** is embedded within opening 16. N type impurity ... is introduced into polycrystalline silicon **plug layer 15 in order to provide conductivity.**”), 1:47-57 (Ex. 1103). As Figure 1 shows, the **plug layer 15** directly touches both of those elements and is “electrically conducting material.” *Id.* at Fig. 1, 6:56-61; *see also id.* at 6:66-7:13, 7:47-50, 7:53-61, claims 1-4, 6, 7 and 9. Decl. ¶ 74 (Ex. 1102).

c) [b]: “said semiconductor structure comprising said diffusion region in a silicon substrate”

As discussed above in the Claim Construction section, the term “diffusion region in a silicon substrate” should be construed as a “conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate.”

Sakamoto discloses the claimed diffusion region.⁵ Decl. ¶ 75 (Ex. 1102).

Figure 1 of Sakamoto discloses a semiconductor structure comprising the diffusion region (n+ source/drain region 7) in a silicon substrate (silicon substrate 1 with p-well region 2).



Sakamoto at Fig. 1 (Ex. 1103); Decl. ¶ 76 (Ex. 1102).

As shown in Figure 1 above, the p-well region 2 is formed below the top surface of the silicon substrate 1, and the source/drain region 7 is formed below the

⁵ Even the '924 patent admits that a diffusion region in a silicon substrate was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent (admitted prior art) at Fig. 2B, 2:15-20 ("a polysilicon gate 32 is first formed without direct contact with the diffusion region 34 and 36 in a silicon substrate 40.") (Ex. 1101); Decl. ¶ 75 fn.3 (Ex. 1102).

top surface of the p-well region 2 (and thus below the top surface of the substrate). See Sakamoto at Fig. 1 (Ex. 1103); see also *id.* at 2:23-29 (“[a]n n channel MOS drive transistor 20a and an n channel MOS transfer transistor 22b each comprises n+ source/drain regions 7, 7, a gate oxide film 5 and gate electrode 6.”), claim 1 (“...said first MOS transfer transistor and said second MOS transfer transistor being formed *on the main surface of the silicon substrate ... a source/drain region* of said second MOS transfer transistor... *a source/drain region* of said first MOS transfer transistor...”), Title, Abstract, 1:13-16, 2:23-29, 3:60-4:2, 4:20-67, 5:1-18, 5:33-50, 6:39-61, 7:14-39, 12:57-58, 13:13-25; Decl. ¶ 77 (Ex. 1102).

Sakamoto teaches that the diffusion region is a “conductive terminal region, such as a source or drain,” because it constitutes a source/drain region 7 of a transistor and electrically connects the transistor to other components in the semiconductor structure. Sakamoto at 6:51-61 (“An n+ source/drain region 7 of an n channel MOS transfer transistor 22b and a gate electrode 6 of an n channel MOS drive transistor 20a are exposed at the bottom of opening 16. A plug layer 15 of polycrystalline silicon directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16. N type impurity... is introduced into polycrystalline silicon plug layer 15 in order to provide conductivity.”), claim 1 (“...said first MOS transfer transistor and said second MOS transfer transistor being formed *on the main surface of the silicon substrate ... a source/drain*

region of said second MOS transfer transistor... *a source/drain region* of said first MOS transfer transistor...” (Ex. 1103). Decl. ¶ 78 (Ex. 1102).

Sakamoto further teaches that the *diffusion region* contains dopants implanted in the silicon substrate. Sakamoto at 7:17-21 (“p type impurity *is implanted in a main surface of a silicon substrate 1*... Subsequently, implanted p type impurity is *diffused to the depth* of about 2-3 μm *from the main surface of substrate 1* by heat treatment to *form a p well 2*.”), 7:32-38 (“N type impurity ion ... *is implanted into p well 2* by an ion implantation method... Thus, n+ *source/drain regions 7* ... are formed.”) (Ex. 1103); Decl. ¶ 79 (Ex. 1102).⁶

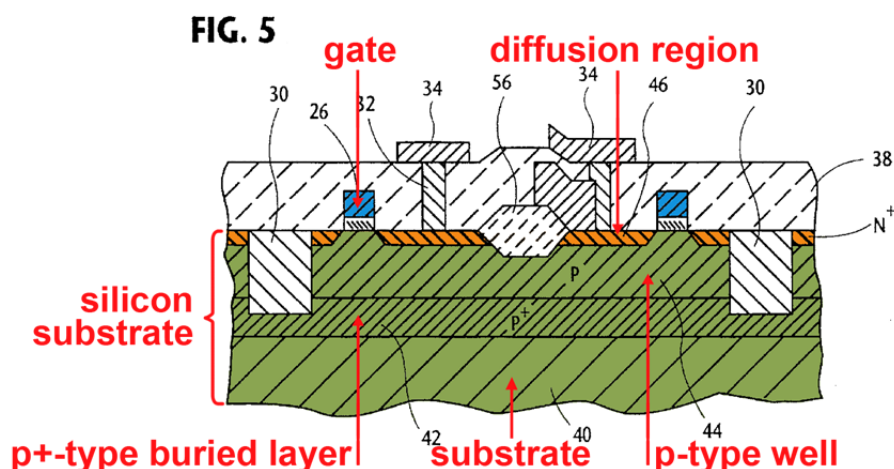
⁶ In the pending litigation between the Patent Owner and Petitioner, the Patent Owner has proposed to construe “diffusion region a silicon substrate” as “conductive terminal region such as a source or drain in a silicon substrate.”

Sakamoto teaches the Patent Owner’s construction as well because, as explained in above in section IX.A.1.c, it teaches a diffusion region that is a conductive terminal region such as a source or drain (Sakamoto at 6:51-61 (Ex. 1103)) and that it is in the silicon substrate (*id.* at Fig. 1, 7:17-38). Accordingly, even under the Patent Owner’s construction, Sakamoto discloses this claim limitation. Decl. ¶ 79 fn.4 (Ex. 1102).

Finally, one skilled in the art would understand that Sakamoto teaches that the silicon substrate is the **silicon substrate 1 with p-well region 2**—for several reasons. Sakamoto at Fig. 1 (Ex. 1103). Decl. ¶ 80 (Ex. 1102).

First, although Figure 1 shows a line delineating the **p-well region 2**, the text of Sakamoto makes clear to one skilled in the art that the **p-well region 2** is a part of the **silicon substrate 1** because the “**p well 2**” is formed in the “surface of **substrate 1**.” Sakamoto at 7:17-21 (“p type impurity *is implanted in a main surface of a silicon substrate 1*... Subsequently, implanted p type impurity is *diffused to the depth* of about 2-3 μm *from the main surface* of substrate 1 by heat treatment to *form a p well 2*.”), 2:22-26 (Ex. 1103); *see also id.* at 1:19-24, 4:14-19, 4:20-67, 6:39-48 (explaining the similarity between Figure 1 and background Figure 28), 7:40-43, 8:13-17, and claims 1, 4 and 7; Decl. ¶ 81 (Ex. 1102).

Second, during prosecution of the parent application for the '924 patent, the Examiner similarly considered a p-type well formed in a silicon substrate to be part of the substrate, even though the relevant prior art figure shows them delineated with different labels. Specifically, as shown below in Figure 5 of U.S. Patent No. 5,453,640 (“Kinoshita”) (Ex. 1113), the prior art disclosed a **diffusion region 46** that is *formed within the p-type well 44* and shows the gate electrode 26 *formed on a top surface of the p-type well 44*:



Kinoshita at Fig. 5 (Ex. 1113); *id.* at 4:20-35 (identifying gate electrode 26, substrate 40, buried layer 42, p-type well 44, and diffusion region 46 in Figure 5), 3:34-35. Confirming that the Examiner considered the p-type well to be part of the substrate, the Examiner concluded that Figure 5 discloses “a semiconductor device comprising: a silicon substrate (40), a diffusion region (46) *formed within* said substrate, [and] a polysilicon gate electrode (26) *formed on a top surface of* said substrate” April 17, 1996 Office Action at 3 (Ex. 1117); Decl. ¶ 82 (Ex. 1102). This conclusion is consistent with what a person of ordinary skill in the art would understand. Decl. ¶ 82 (Ex. 1102).

In responding to the Examiner’s rejection, the Applicant did not dispute the Examiner’s assertion that the p-type well 44 was part of the substrate 40. In fact, the Applicant expressly acknowledged that another separately delineated layer in Figure 5—the buried layer 42—is also part of the substrate 40. *See* Amendment dated August 14, 1996 at 4 (“Kinoshita further teaches a block of static memory

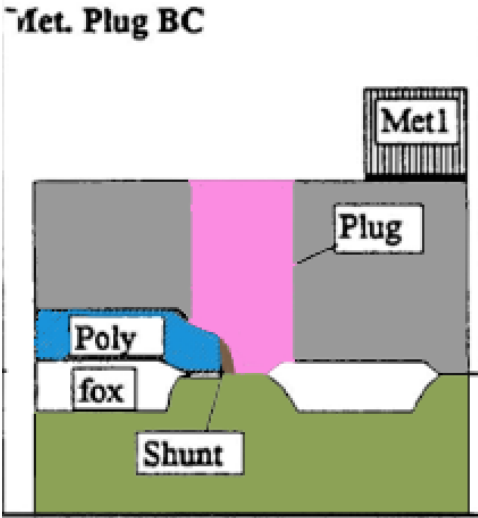
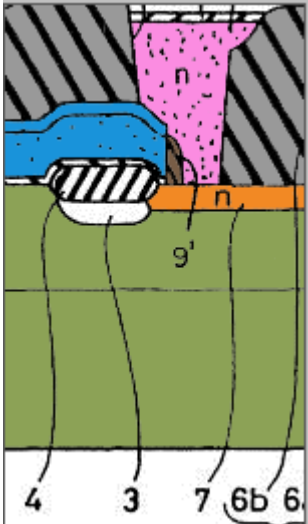
cells using CMOS transistors, wherein metal interconnections, e.g., ground lines for the CMOS transistors, are simplified by *using buried layers in the substrate... .*) (Ex. 1114). Decl. ¶ 83 (Ex. 1102).

Third, the line delineating the p-well region 2 part of silicon substrate 1 is not present in all figures of Sakamoto, and Sakamoto elsewhere explicitly shows that regions, such as well regions, are formed in silicon substrate 1 (making clear that p-well region 2 is a part of the silicon substrate). See Sakamoto at Fig. 25, 12:57-58 (“On a surface of a silicon substrate 1, for example, an n type impurity region 30 is formed.”), claim 1 (“...said first MOS transfer transistor and said second MOS transfer transistor being formed *on the main surface of the silicon substrate* ... a source/drain region of said second MOS transfer transistor... a source/drain region of said first MOS transfer transistor...” (Ex. 1103). Thus, one skilled in the art would understand that the p-well region 2 is part of silicon substrate 1 in the semiconductor structure disclosed in Sakamoto. Decl. ¶ 84 (Ex. 1102).

d) [c]: “said gate being on said substrate juxtaposed to but not contacting said diffusion region”

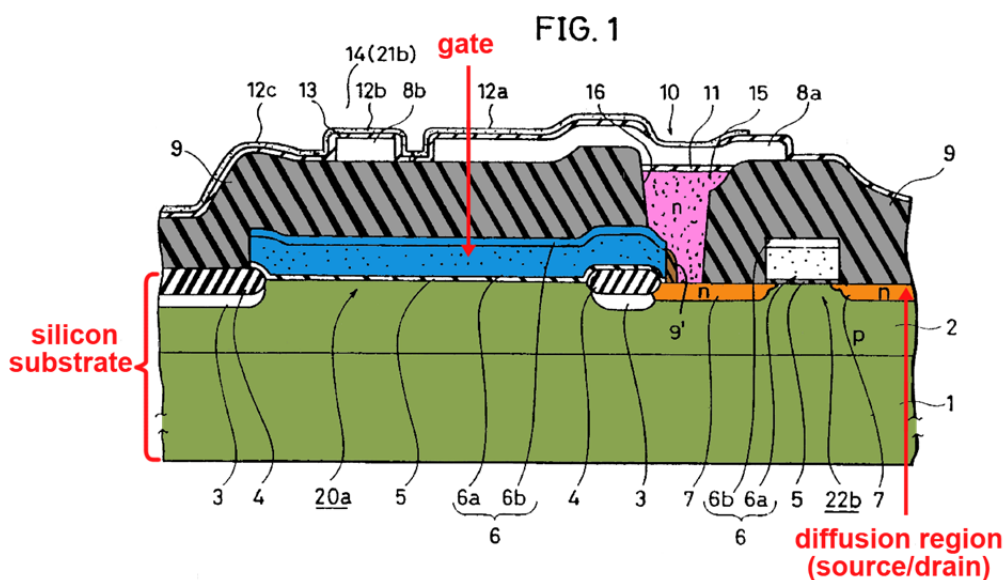
Sakamoto discloses a gate (gate electrode 6) being on the substrate (silicon substrate 1 with p-well region 2):⁷

⁷ Sakamoto shows the gate on top of a “field oxide film 4.” Sakamoto at 7:17-29 (Ex. 1103). Applicant’s purported conception documents also show the gate over the same field oxide (labeled “fox”). Accordingly, Sakamoto’s gate is on the substrate, just like the ’924 patent’s gate is on the substrate.

Rule 131 Declaration	Sakamoto: Fig. 1
	

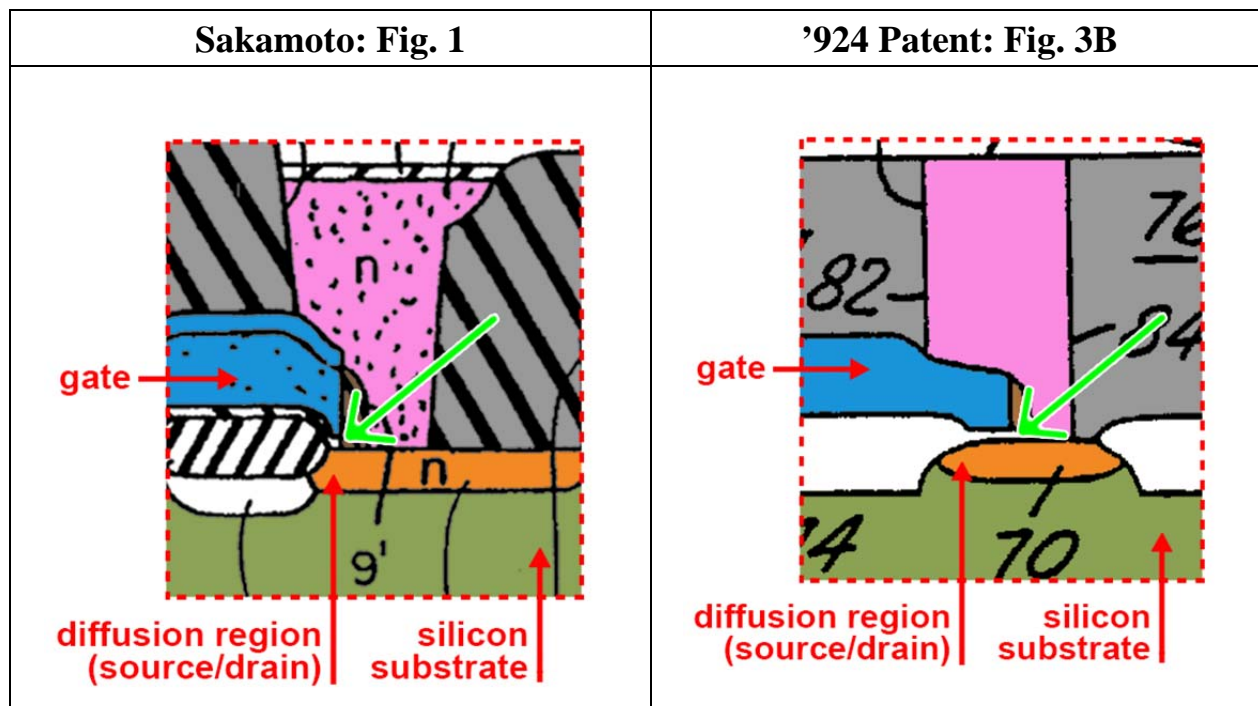
Rule 131 Declaration, Exhibit A (Ex. 1106); Sakamoto at Fig. 1 (Ex. 1103). Decl.

¶ 85 fn.5 (Ex. 1102).



Sakamoto at Fig. 1, 6:52-58 (“A plug layer 15 of polycrystalline silicon directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16.”), 7:17-32 (“a silicon substrate 1 ... form gate electrodes 6, 6 of MOS transistors 20a, 22b...”)(Ex. 1103); *see also id.* at claim 1, 2:23-32, 4:20-67, 6:39-7:7, 7:17-52, 12:57-58. Decl. ¶ 85 (Ex. 1102).

As shown in Figure 1, Sakamoto also discloses that the **gate** is juxtaposed to but not contacting the diffusion region (n+ **source/drain region 7**), as shown by the white space identified by the green arrow separating the **gate** from the **diffusion region**. Decl. ¶ 86 (Ex. 1102).



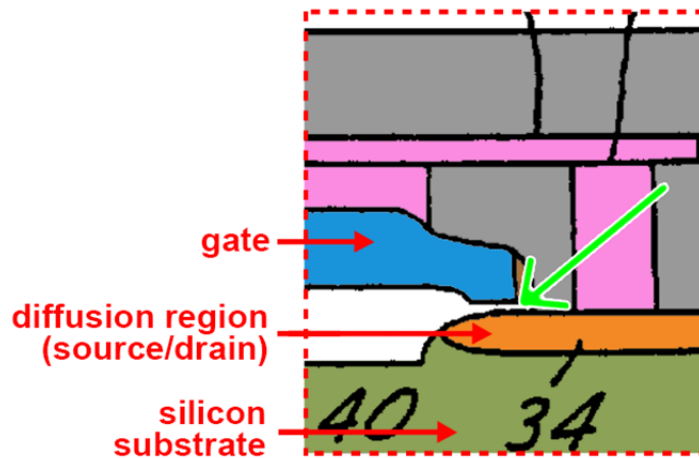
The white region is an oxide film 5 that separates the gate from the diffusion region. Sakamoto at Fig. 1, 7:24-27 (“Oxide films 5 of 12 nm-15 nm thickness are formed on the surface of the p well 2.... Oxide films 5 form gate oxide films 5,5 of MOS transistors 20a, 20b.”) (Ex. 1103); *see also id.* at 2:23-31, 6:42-45, 6:52-58, 6:66-7:7, 7:17-52, 12:57-58. This is identical to the structure shown above in Figure 3B of the '924 patent. '924 patent at Fig. 3B (Ex. 1101). Indeed, there would be no need for a plug to connect the gate and diffusion region if they were directly connected. *See, e.g., id.* at Figs. 1A, 1B, 1:24-2:10 (describing the prior art

buried contact approach where gate and diffusion region are directly connected and there is no plug); Decl. ¶ 87 (Ex. 1102).⁸

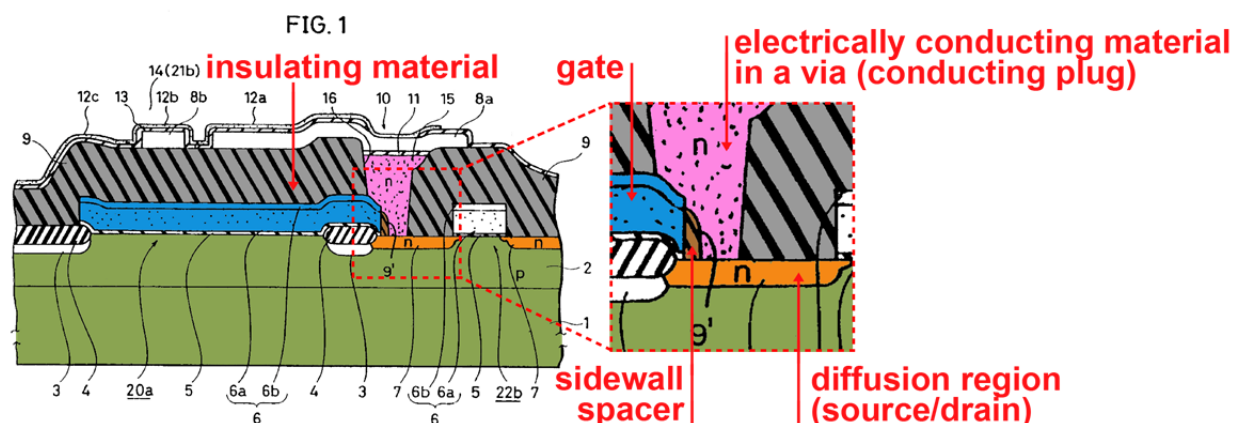
e) [d]: “said sidewall spacer being disposed above said diffusion region”

Figure 1 of Sakamoto discloses a sidewall spacer (sidewall spacer 9') disposed above the diffusion region (source/drain region 7):

⁸ As is shown in Figure 2B of the admitted prior art, even the '924 patent admits that a gate being on said substrate juxtaposed to but not contacting said diffusion region, was known to a person of ordinary skill in the art at the time of the '924 patent:

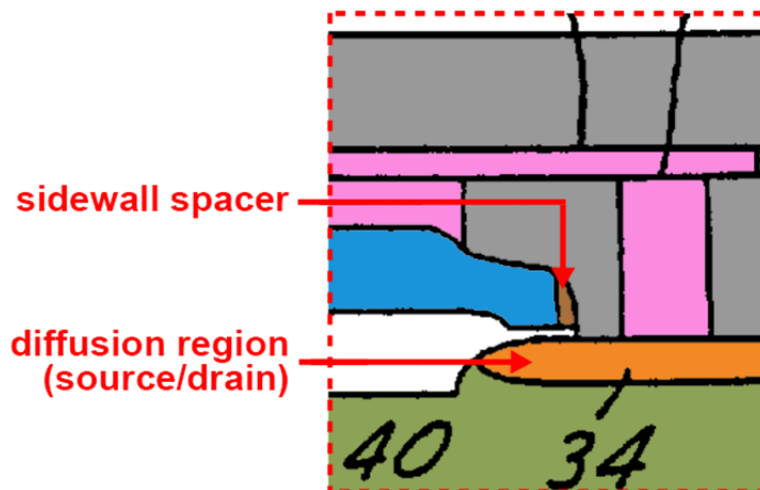


'924 patent (admitted prior art) at Fig. 2B, 2:15-20 (“a polysilicon gate 32 is first formed without direct contact with the diffusion regions 34 and 36 in a silicon substrate 40.”) (Ex. 1101); Decl. ¶ 87 fn.6 (Ex. 1102).



Sakamoto at Fig. 1, 7:44-52 (“a **sidewall spacer 9**” is located in the “opening 16”), claims 6 and 9 (Ex. 1103).⁹ Decl. ¶ 88 (Ex. 1102).

⁹ As is shown in Figure 2B of the admitted prior art, even the '924 patent admits that a sidewall spacer being disposed above the diffusion region was known to a person of ordinary skill in the art at the time of the '924 patent:

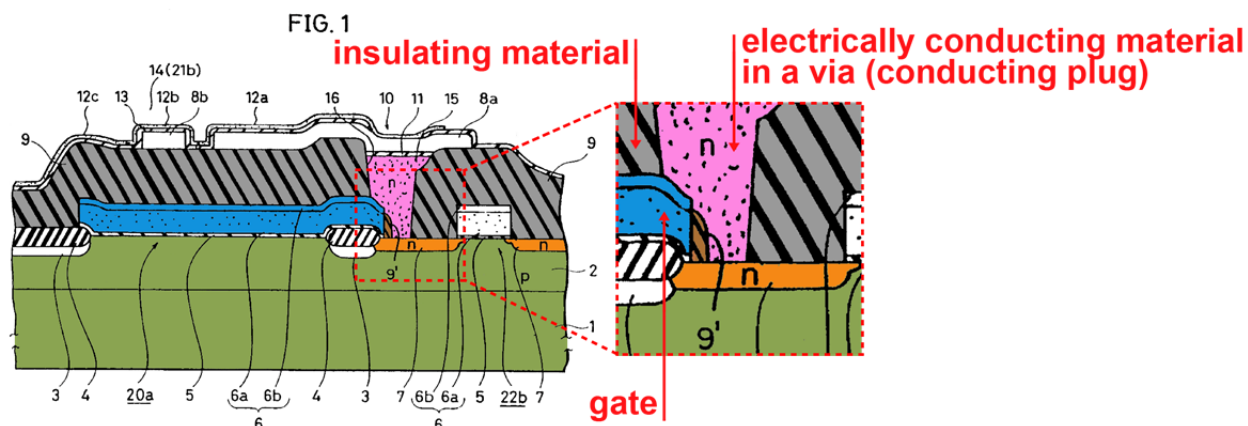


diffusion region
(source/drain)

⁹²⁴ patent (admitted prior art) at Fig. 2B (Ex. 1101). Decl. ¶ 88 fn.7 (Ex. 1102).

f) [e]: “said via being in an insulating material on said gate.”

Figure 1 of Sakamoto discloses a via (opening 16) in an insulating material (insulating layer 9) on the gate (gate electrode).



Sakamoto at Fig. 1, 7:40-47 (“Subsequently, a BPSG (BoroPhospho Silicate Glass) film is deposited on the whole surface of silicon substrate 1.... In this step, an interlevel insulating layer 9 having a planarized surface is formed.”), 2:47-53 (“[a]n opening 16 is formed in interlevel insulating layer 9. Inside opening 16, gate electrode 6 of n channel MOS drive transistor 20a and one of n+ source/drain regions 7 of n channel MOS transfer transistor 22b is exposed.”) (Ex. 1103); *see also id.* at Fig. 2, Abstract, claims 1, 4, and 7, 2:33-34, 3:60-63, 4:20-67, 5:3-6, 5:20-23, 5:35-38, 6:39-7:14, 7:47-52. Decl. ¶ 89 (Ex. 1102).

2. Claim 8: “A method according to claim 7, wherein said diffusion region is an N+ or a P+ region.”

Sakamoto discloses that the diffusion region (n+ source/drain region 7) is “an N+ or a P+ region” (*i.e.*, an n+ region).¹⁰ Specifically, Sakamoto discloses that the diffusion region is an “N+ ... region,” because it expressly refers to the diffusion region as an “n+ source/drain region 7.” Sakamoto at 6:52-58 (“An n+ source/drain region 7 [is] exposed at the bottom of opening 16.”), 7:32-38 (“Thus, n+ source/drain regions 7 of four MOS transistors 20a, 20b, 22a, 22b are formed.”) (Ex. 1103); *see also id.* at 2:22-29. Decl. ¶ 90 (Ex. 1102).

3. Claim 9: “A method according to claim 7, wherein said insulating material is selected from the group consisting of silicon oxide and silicon nitride.”

Sakamoto discloses forming the insulating layer 9 from a BPSG (BoroPhospho Silicate Glass) film. Sakamoto at 7:39-47 (“a BPSG (BoroPhospho Silicate Glass) film ... is softened and reflowed by heat treatment, so that a surface of the BPSG film is planarized. In this step, an interlevel insulating layer 9 ... is

¹⁰ Even the '924 patent admits that N+ and P+ diffusion regions were known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent (admitted prior art) at 1:15-2:11 (“In the semiconductor fabrication process, it is frequently required to make local interconnect between a gate polysilicon layer to N+ and P+ diffusion regions.”) (Ex. 1101). Decl. ¶ 90 fn.8 (Ex. 1102).

formed.”) (Ex. 1103). A person of skill in the art would readily recognize that BPSG is a type of silicon oxide. Decl. ¶ 91 (Ex. 1102); *see also* Hiatt (1994) at p. 185 (“Doped silicon oxides such as phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG)...”) (Ex. 1115); ’924 patent at 3:61-63 (“an insulating layer 76 of *silicon oxide*”), 4:39 (“#13-Nit/**BPSG**”), 4:52 (“#13-Nit/**BPSG**”) (Ex. 1101).

A person of ordinary skill would further recognize that silicon oxide and silicon nitride are commonly used interchangeably in semiconductor structures. For example, even the ’924 patent itself, in discussing the “prior art interconnect” structures at column 1:15-2:45, discloses the interchangeability of the silicon oxide (“BPSG”) with silicon nitride (“Nit”). ’924 patent at 4:39 (“#13-Nit/**BPSG**”), 4:52 (“#13-Nit/**BPSG**”) (Ex. 1101). Decl. ¶ 92 (Ex. 1102).

Thus, one skilled in the art would understand that Sakamoto discloses an insulating material selected from the group consisting of silicon oxide and silicon nitride, *i.e.*, formed of either silicon oxide or silicon nitride. Decl. ¶ 93 (Ex. 1102).

4. Claim 15: “A method according to claim 7, wherein said gate is a polysilicon gate.” / Claim 17: “The method according to claim 7, wherein said gate comprises polysilicon.”

Sakamoto discloses that the [gate electrode 6](#) comprises polysilicon and is, in fact, a polysilicon gate.¹¹ Polysilicon is also known as “polycrystalline silicon.” Decl. ¶ 94 (Ex. 1102); *see also* Cederbaum at 1:17 (“polycrystalline silicon (polysilicon)”) (Ex. 1104); Seto (1975) at Introduction (Ex. 1116) (“polycrystalline silicon (polysilicon)”). Sakamoto discloses that the [gate electrode 6](#) is “formed of polycrystalline silicon” (*i.e.* polysilicon). Sakamoto at 2:28-32, 2:49-52, 7:27-32 (“A polycide film formed of polycrystalline silicon 6a and refractory metal silicide 6b ... is patterned ... to form [gate electrodes 6, 6](#)”) (Ex. 1103); Decl. ¶ 94 (Ex. 1102).

¹¹ Even the '924 patent admits that a polysilicon [gate](#) was known to a person of ordinary skill in the art at the time of the '924 patent. *See* '924 patent (admitted prior art) at 2:11-32 (“a polysilicon [gate](#) 32 is first formed without direct contact with the diffusion regions 34 and 36 in a silicon substrate.”), 1:15-1:24 (“In the semiconductor fabrication process, it is frequently required to make local interconnect between a [gate](#) polysilicon layer to N+ and P+ diffusion regions.”), 1:25-2:11 (Ex. 1101). Decl. ¶ 94 fn.9 (Ex. 1102).

B. Ground II: Claims 10-12 are obvious in view of the combination of Sakamoto and Cederbaum

Dependent claims 10-12 add limitations specifying particular (and obvious design) choices for the material used in the conducting plug. Sakamoto, when combined with Cederbaum renders obvious these claims under 35 U.S.C. § 103(a). Each of these claims depends from claim 7. Therefore the analysis with respect to claim 7 as set forth above in Ground I (§ IX.A) is incorporated by reference as if recited herein. Decl. ¶ 95 (Ex. 1102).

1. Claim 10: “a method according to claim 7, wherein said electrically conducting plug is a metal plug” / Claim 11: “a method according to claim 7, wherein said electrically conducting plug is preferably a refractory metal plug” / Claim 12: “a method according to claim 7, wherein said electrically conducting plug is formed of a material selected from the group consisting of titanium, tantalum, molybdenum and tungsten”

Sakamoto discloses an electrically conducting **plug** made of polycrystalline silicon. Sakamoto at 6:56-58 (“**plug layer 15** of *polycrystalline silicon* directly connected to the n+ source/drain region 7 and gate electrode 6 is embedded within opening 16.”) (Ex. 1103); *see also id.* at 6:66-7:13, 7:53-62, 8:7-21, 9:67-10:23. Decl. ¶ 96 (Ex. 1102).

Claim 10: Cederbaum discloses an electrically conducting plug (**contact stud 30-2**) which is a metal plug formed of tungsten, thereby disclosing the limitations of claim 10. Cederbaum at 9:31-65 (“[Prior to *tungsten (W) filling*, a

titanium (Ti) layer is deposited [in] the first stud openings 28-1, 28-2 and 28-3....

Next, a thin titanium nitride (TiN) layer is formed over the titanium layer.... A

tungsten layer is then deposited ... to entirely fill the first stud openings

Planarization of the Ti-TiN and **W [i.e., tungsten]** composite layer produces first

contact pads 29 and **first contact studs 30** in first stud openings 28.”), claim 14

(Ex. 1104). Decl. ¶ 97 (Ex. 1102).

Claim 11: Cederbaum’s tungsten metal plug (**contact stud 30-2**) is also a refractory metal plug, which meets the requirement of claim 11. *See, e.g.*, Cederbaum at 9:31-65, claim 14 (Ex. 1104); ’924 patent at 1:53-54 (“A **refractory metal plug such as a tungsten plug** is then deposited...”) (Ex. 1101); Nicholls at 6:41-60 (“refractory metal such as tungsten” and “[e]xamples of such selectively depositable refractory metals are tungsten, copper, molybdenum and tantalum.”) (Ex. 1108); Decl. ¶ 98 (Ex. 1102).

Claim 12: Finally, as already stated above, Cederbaum discloses an electrically conducting plug (**contact stud 30**) formed of tungsten, which is a material selected from the group consisting of titanium, tantalum, molybdenum and **tungsten**, as required by claim 12. Cederbaum at 9:31-65, claim 14 (Ex. 1104); Decl. ¶ 99 (Ex. 1102).

It would have been obvious for one skilled in the art to replace the **polycrystalline plug 15** of Sakamoto with the refractory metal **tungsten plug**

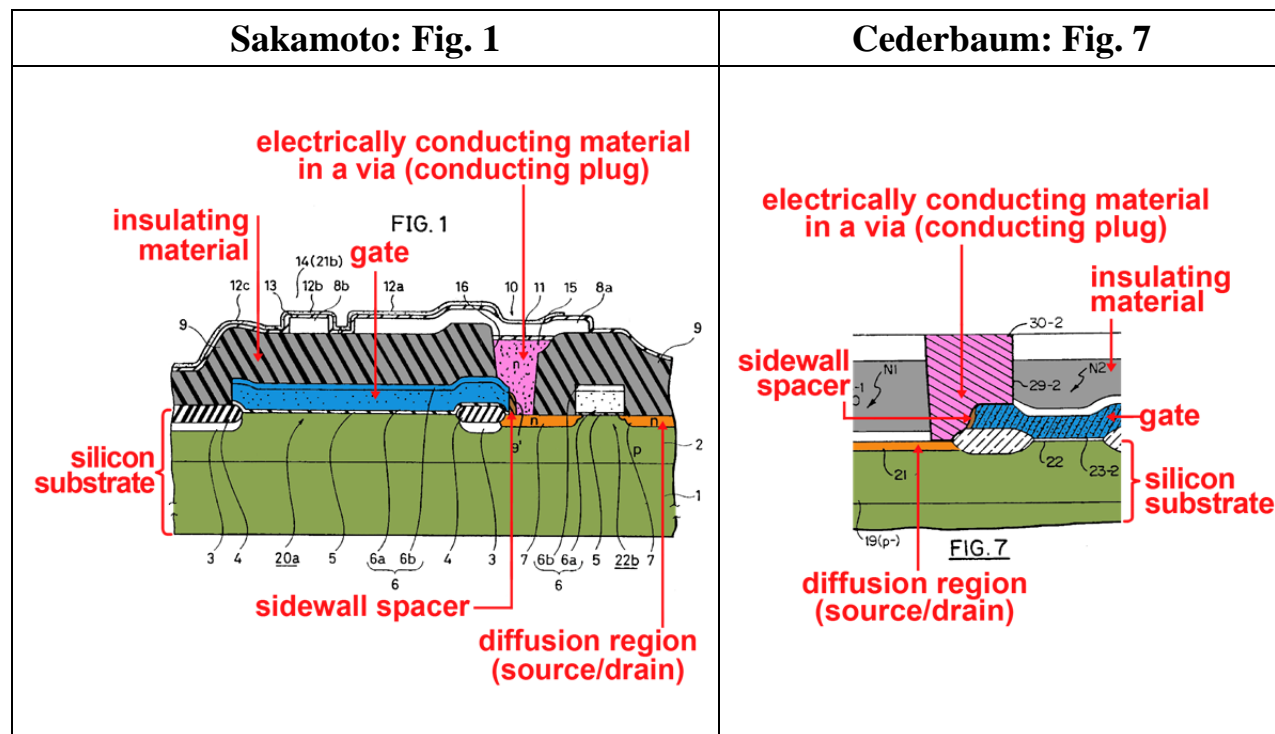
(contact stud 30) of Cederbaum for multiple reasons.¹² Decl. ¶ 100 (Ex. 1102).

First, both Sakamoto and Cederbaum describe the same type of devices directed to the same problem: improving the structure of transistors used in semiconductor devices—in particular, the problem of *stacking* transistors in a particular type of memory circuit called a Static Random Access Memory (“*SRAM*”) cell. *See* Sakamoto at 1:29-32 (“a semiconductor device having a structure in which semiconductor elements are *stacked* on a substrate, a structure of an *SRAM* (*Static Random Access Memory*) will be described.”), 1:13-16 (Ex. 1103); Cederbaum at 1:7-14 (“The present invention relates to ... a method of forming *stacked*, self-aligned polysilicon gate PFET devices.... In particular, the method has applicability in the forming of *stacked* self-aligned polysilicon gate

¹² Even the ’924 patent admits that a tungsten refractory metal *conducting plug* was known to a person of ordinary skill in the art at the time of the ’924 patent. *See* ’924 patent (admitted prior art) at 1:50-56 (“A refractory metal plug such as a *tungsten plug* is then deposited into hole 24.”), 2:23-32 (“After the deposition of a glue layer (not shown), *metal plugs 44, 46 and 48* are deposited into the vias. After a tungsten plug etch back and a local interconnect masking/etching process...”)
(Ex. 1101). Decl. ¶ 100 fn.10 (Ex. 1102).

PFETs ... in six device (6D) **SRAM cells.**”) (Ex. 1104); *see also* ’924 patent at 2:32-63, 4:10-15 (Ex. 1101); Decl. ¶ 101 (Ex. 1102).

In fact, Sakamoto and Cederbaum (and the ’924 patent) disclose nearly identical structures with nearly identical components. Decl. ¶ 102 (Ex. 1102).



Like Figure 1 of Sakamoto, Figure 7 of Cederbaum shows an electrically conducting plug (contact stud 30-2) within an opening 28-2 (Figure 6) which contains a sidewall spacer 24 (Figure 4). The contact stud 30-2 directly connects a diffusion region (source/drain 21) to a gate (gate electrode 23-2). The source/drain 21 is formed in a substrate and is not directly connected to the gate electrode 23-2, which is substantially covered by an insulating material 26. Cederbaum at Figs. 4-7, 7:31-40, 7:37-52 (“N+ implanted active regions 21... constitute the source and

drain regions of the NFETs,” “[n]umeral[]...23-2 designate[s]...the gate electrode[] of NFETs...,” and “[o]xide sidewalls or spacers 24 have been formed on the lateral sides of the polysilicon gate electrodes”), 8:26-39, 9:28-68, 13:31-37 (Ex. 1104); Decl. ¶ 103 (Ex. 1102).

Second, the particular material to be used for electrical conductivity would have been a simple design choice to one of ordinary skill in the art. Decl. ¶ 104 (Ex. 1102). It was known that there were multiple materials that could be used to make an electrical connection between different parts of a transistor. *See, e.g.*, Nicholls at 6:41-54 (explaining “an advantage of using a refractory metal such as tungsten over aluminium” as a plug), 6:55-60 (“The present invention is not limited to the use of tungsten [as a plug] but can be carried out utilising any refractory metal ... which preferably can be selectively deposited into a contact hole. Examples of such selectively depositable refractory metals are tungsten, copper, molybdenum and tantalum.”) (Ex. 1108). The use of a refractory metal is thus a mere implementation detail which one skilled in the art would have known about and been motivated to use. Decl. ¶ 104 (Ex. 1102).

Third, as both Sakamoto and Cederbaum explain, there are advantages to using an electrically conducting plug formed of a refractory metal, such as tungsten (as in Cederbaum) instead of a polycide film formed from polycrystalline silicon and a metal (as in Sakamoto). Sakamoto describes the benefits of increased

conductivity of the **plug** and increased conductivity and ohmic contact between the **plug** and other components, such as the **source/drain region 7**. See Sakamoto at 8:5-12 (“Impurity ion is ion-implanted into polycrystalline silicon **plug layer 15** ... in order to provide conductivity.”), 2:28-32, 2:62-64, 6:58-63, 7:3-7 (“ohmic contact of interconnection layer 8a, polycrystalline silicon **plug layer 15**, and **source/drain region 7** can be obtained by having titanium silicide layer 11 interposed between interconnection layer 8a and polycrystalline silicon **plug layer 15**.”), 7:26-28, 10:5-8 (“Fine ohmic contact can be also provided between the silicon **plug layer** and the upper interconnection layer of p type conductivity by interposing a refractory metal silicide layer etc.”) (Ex. 1103); Decl. ¶ 105 (Ex. 1102). Cederbaum then describes a tungsten conducting plug (**contact stud 30-2**) that has the better conductivity and lower resistivity as compared to a polycide/polycrystalline silicon plug (like Sakamoto’s plug). Cederbaum at 4:39-41 (“[p]olycide is a quite good conductive material, however it is known to exhibit higher resistivities than metal.”), 9:32-34 (“filling the first stud openings with a highly conductive material (typically a metal, such as tungsten)”), 6:47-48 (“[t]he [conventional] N+/P+ diode contact structure is replaced by a tungsten contact stud forming an ohmic contact.”) (Ex. 1104). Decl. ¶ 105 (Ex. 1102).

X. CONCLUSION

Based on the foregoing, claims 7-12, 15, and 17 of the '924 patent recite subject matter that is unpatentable. The Petitioner requests institution of an *inter partes* review to cancel these claims.

Respectfully submitted,

/David M. O'Dell/

David M. O'Dell

Lead Counsel for Petitioner

Registration No. 42,044

HAYNES AND BOONE, LLP

Telephone: 972/739-8635

Dated: July 1, 2016

List of Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 5,965,924

Exhibit	Description
1101	U.S. Patent No. 5,965,924
1102	Blanchard Declaration
1103	U.S. Patent No. 5,475,240 (“Sakamoto”)
1104	U.S. Patent No. 5,100,817 (“Cederbaum”)
1105	Continued Prosecution Application Request dated February 10, 1999
1106	Amendment and Rule 131 Declaration dated January 5, 1998
1107	Office Action dated November 7, 1996
1108	U.S. Patent No. 5,541,434 (“Nicholls”)
1109	Amendment dated June 9, 1997
1110	Office Action dated February 24, 1998
1111	U.S. Patent No. 5,541,427 (“Chappell”)
1112	Amendment dated April 23, 1998
1113	U.S. Patent No. 5,453,640 (“Kinoshita”)
1114	Amendment dated August 14, 1996
1115	C. Fred Hiatt, Jeffery W. Butterbaugh and David C. Gray, <i>UV-Enhanced Etching of Silicon Oxide by Chlorine Trifluoride</i> , in PROCEEDINGS OF THE SECOND INTERNATIONAL SYMPOSIUM ON ULTRA-CLEAN PROCESSING OF SILICON SURFACES (Marc Heyns ed. 1994) (“Hiatt”).
1116	J. Seto, “The electrical properties of polycrystalline silicon films,” <i>Journal of Applied Physics</i> , 46 (1975) (“Seto”)

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1117	Office Action dated April 17, 1996
1118	Compilation of Claim Construction Deadlines and Filings in DSS Tech. Mgm't, Inc. v. Intel Corp. et al., 6:15-cv-00130-RWS (E.D. Tex.)

CERTIFICATE OF WORD COUNT

Pursuant to 37 CFR § 42.24, the undersigned hereby certifies that according to Microsoft Word's automatic word-counting tool, there are less than 14,000 words, not including table of contents, table of authorities, grounds for standing under § 42.104, § 42.204, or § 42.304, mandatory notices under § 42.8, certificate of service or word count, or appendix of exhibits or claim listing.

CERTIFICATE OF SERVICE

I hereby certify that on July 1, 2016, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 5,965,924 Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibits 1101-1118
- List of Exhibits for U.S. Patent No. 5,965,924 Petition for *Inter Partes* Review (Ex. 1101-1118)
- Power of Attorney

to be served via Federal Express on the following attorney of record as listed on PAIR:

Smith & Hopen (private clients)
Attn: General Patent Matters
180 Pine Avenue North
Oldsmar FL 34677

/David M. O'Dell/
David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044