

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,  
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN  
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN  
MODULE TWO LLC & CO. KG,  
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,  
Patent Owner.

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Case IPR2016-01312  
Patent 5,965,924

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Before BRYAN F. MOORE, BRIAN J. McNAMARA, and  
MINN CHUNG, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## BACKGROUND

Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG (collectively, “Petitioner”) filed a petition, Paper 3 (“Pet.”), to institute an *inter partes* review of claims 7–12, 15, and 17 (the “challenged claims”) of U.S. Patent No. 5,965,924 (“the ’924 Patent”). 35 U.S.C. § 311. Petitioner also timely filed a Motion for Joinder (Paper 4 (“Mot. For Joinder”)) of this proceeding with *Intel Corporation v. DSS Technology Management, Inc.*, Case IPR2016-00290 (“Intel IPR2016-00290”), which is the subject of a Decision to Institute entered on June 8, 2016. Petitioner represents that the instant Petition “is identical to the petition in [Intel IPR2016-00290].”<sup>1</sup> Mot. For Joinder 6. We have jurisdiction under 37 C.F.R. § 42.4(a) and 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Having considered the arguments and the associated evidence presented in the Petition, for the reasons described below, we institute *inter partes* review of claims 7–12, 15, and 17.

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<sup>1</sup> We understand Petitioner to mean identical in all substantive matters, as the identity of the parties is different. Petitioner also acknowledges that it relies on the testimony of a different expert than the expert witness in Intel IPR2016-00290, but states that the testimony is essentially the same. Mot. For Joinder 7.

### REAL PARTIES IN INTEREST

Petitioner Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG identifies itself as real parties-in-interest. Pet. 5.

### PENDING LITIGATION

The parties state that Patent Owner has asserted '924 Patent in the following litigation: (1) *DSS Technology Management, Inc. v. Intel Corp.*, No. 6:15-CV-130-RWS (E.D. Tex. 2015); and (2) *DSS Technology Management, Inc. v. Qualcomm Inc.*, No. 6:15-CV-692-JRG (E.D. Tex. 2015). Pet. 6.

Petitioner notes that it has filed a separate petition for *inter partes* review of claims 1–6, 13, 14, and 16 of the '924 Patent. Pet. 5. That proceeding has been designated IPR2016-01313.

### THE '924 PATENT (EXHIBIT 1101)

The '924 Patent relates to semiconductor fabrication in general, and in particular concerns a metal plug local interconnect that is formed in the same process of forming metal plugs that are already designed as sub-metal plugged contacts. Ex. 1101, col. 1, ll. 9–11. The '924 Patent discloses that in semiconductor fabrication, it is often necessary to make a local interconnect between a gate polysilicon layer to N+ or P+ diffusion regions. *Id.* at col. 1, ll. 16–17. According to the '924 Patent, conventionally such

local interconnects were fabricated using buried contacts, as shown in Figures 1A and 1B of the '924 Patent (*id.* at col. 1, l. 25–col. 2, l. 11) or with a metallic local interconnect strap to shunt from a gate polysilicon to a diffusion region, as illustrated in Figures 2A and 2B of the '924 Patent (*id.* at col. 2, l. 12–41).

The '924 Patent discloses a semiconductor structure in which a diffusion region is formed in a silicon substrate and a polysilicon gate is formed on the top surface of the silicon substrate adjacent to, but not contacting, the diffusion region. Ex. 1101, col. 3, ll. 1–6, 14–18. A layer of insulating material is then deposited on top of the polysilicon gate and the diffusion region. *Id.* at col. 3, ll. 6–7, 19–20. A via opening is formed in the insulating material to expose a portion of the polysilicon gate and a portion of the diffusion region. *Id.* at col. 3, ll. 7–8, 20–22. An electrically conducting material is deposited to at least partially fill the via opening to provide an electrical connection between the polysilicon gate and the diffusion region. *Id.* at col. 3, ll. 8–11, 23–27.

#### ILLUSTRATIVE CLAIM

7. A method of forming a local interconnect in a semiconductor structure, comprising the step of:  
depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said sidewall spacer

being disposed above said diffusion region, said via being in an insulating material on said gate.

#### ART CITED IN PETITIONER’S CHALLENGES

Petitioner cites the following references in its challenges to patentability:

Sakamoto, U.S. Patent No. 5,475,240 issued Dec. 12, 1995, Ex. 1103 (“Sakamoto”); and

Cederbaum et al., U.S. Patent No. 5,100,817 issued Mar. 31, 1992, Ex. 1104 (“Cederbaum”).

#### CHALLENGES ASSERTED IN PETITION

Claims	Statutory Basis	Challenge
7–9, 15, and 17	35 U.S.C. § 102(e)	Anticipation by Sakamoto
10–12	35 U.S.C. § 103	Obviousness over the combination of Sakamoto and Cederbaum

#### ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

Petitioner states that the instant Petition is substantially identical to the petition in *Intel Corporation v. DSS Technology Management, Inc.*, which was filed December 8, 2015 and assigned Case No. IPR2016-00289 (Intel IPR2016-00289). Pet. 1. In Intel IPR2016-00289, Intel challenged different claims, i.e., claims 1–6, 13, 14, and 16 of the ’924 Patent. Petitioner’s reference to IPR2016-00289 appears to be a typographical error. Based on

the claims identified in the Petition and on the representations in Petitioner's Motion for Joinder, we understand Petitioner to represent that the instant Petition is identical in substance to the petition filed in Intel IPR2016-00290, in which Intel challenged claims 7–12, 15, and 17 of the '924 Patent. Petitioner also acknowledges that it relies on the testimony of a different expert than the expert witness in Intel IPR2016-00290, but states that the testimony is essentially the same. *Id.* at 7. Thus, we understand that Petitioner challenges the claims of the '924 Patent on the same grounds on which we instituted *inter partes* review in Intel IPR2016-00290.

We incorporate by reference our decision in Intel IPR2016-00290 and institute *inter partes* review in this proceeding on the same grounds, for the same reasons.

### SUMMARY

For the reasons discussed above, on the current record we are persuaded that Petitioner has demonstrated a reasonable likelihood that it will succeed on the following challenges to patentability:

Claims 7–9, 15, and 17 as anticipated under 35 U.S.C. § 102(e) by Sakamoto; and

Claims 10–12 as obvious under 35 U.S.C. § 103(a) over the combination of Sakamoto and Cederbaum.

### ORDER

In consideration of the foregoing, it is hereby:

ORDERED that pursuant to 35 U.S.C. § 314(a) an *inter partes* review of the '924 Patent is hereby instituted, commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

FURTHER ORDERED that the trial is limited to the following grounds and no other grounds are authorized:

Claims 7–9, 15, and 17 as anticipated under 35 U.S.C. § 102(e) by Sakamoto; and

Claims 10–12 as obvious under 35 U.S.C. § 103(a) over the combination of Sakamoto and Cederbaum.

FURTHER ORDERED that the trial will be conducted in accordance with the Scheduling Order entered in Intel IPR2016-00290.

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