

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
and
QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES
DRESDEN MODULE TWO LLC & CO. KG,
Petitioners

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner

Case IPR2016-00290¹
Patent 5,965,924

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and
MINN CHUNG, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37 C.F.R. § 42.73

¹ Case IPR2016-01312 has been joined with this proceeding.

BACKGROUND

On June 8, 2016 we instituted an *inter partes* review of claims 7–12, 15, and 17 of U. S. Patent No. 5,965,924 (“the ’924 Patent”) based on a Petition filed by Intel Corporation. Paper 10 (“Dec. to Inst.”). DSS Technology Management, Inc. (“Patent Owner”) waived its right to file a Preliminary Response. On August 29, 2016 we instituted *inter partes* review of the same claims on the same grounds based on a substantially identical petition filed by Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG, in IPR2016-01312. We then joined IPR2016-00290 and IPR2016-01312. Papers 17, 18. In this joined proceeding, we refer to Intel Corporation, Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG, collectively as “Petitioner.”

On September 7, 2016, Patent Owner filed a Patent Owner Response that contained no citations to evidence and no argument, other than noting that in contrast to the standard applied in reaching a decision to institute (i.e., a reasonable likelihood Petitioner will prevail on its challenge to patentability of a claim), the standard for reaching a final decision is whether the Petitioner proved unpatentability by a preponderance of the evidence. PO Resp. 2. Patent Owner then stated it “defers to the Board to make this determination based on its impartial analysis of the prior art and Petitioners’ arguments.” *Id.*

In its Reply filed on December 7, 2016, Petitioner stated that Patent Owner has provided no testimony or any other evidence that contradicts or

rebutts the testimony of Petitioner's expert, Dr. John Bravman, and that the challenged claims should be found unpatentable (Paper 21, "Pet. Reply").

We did not conduct an oral hearing in this case.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the papers submitted by the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable.

THE '924 PATENT (Ex. 1001)

The '924 Patent relates to semiconductor fabrication in general, and in particular concerns a metal plug local interconnect that is formed in the same process of forming metal plugs that are already designed as sub-metal plugged contacts. Ex. 1001, col. 1, ll. 9–11. The '924 Patent discloses that in semiconductor fabrication, it is often necessary to make a local interconnect between a gate polysilicon layer to N+ or P+ diffusion regions. *Id.* at col. 1, ll. 16–17. According to the '924 Patent, conventionally such local interconnects were fabricated using buried contacts, as shown in Figures 1A and 1B of the '924 Patent (*id.* at col. 1, l. 25–col. 2, l. 11) or with a metallic local interconnect strap to shunt from a gate polysilicon to a diffusion region, as illustrated in Figures 2A and 2B of the '924 Patent (*id.* at col. 2, l. 12–41).

The '924 Patent discloses a semiconductor structure in which a diffusion region is formed in a silicon substrate and a polysilicon gate is formed on the top surface of the silicon substrate adjacent to, but not

contacting, the diffusion region. Ex. 1001, col. 3, ll. 1–6, 14–18. A layer of insulating material is then deposited on top of the polysilicon gate and the diffusion region. *Id.* at col. 3, ll. 6–7, 19–20. A via opening is formed in the insulating material to expose a portion of the polysilicon gate and a portion of the diffusion region. *Id.* at col. 3, ll. 7–8, 20–22. An electrically conducting material is deposited to at least partially fill the via opening to provide an electrical connection between the polysilicon gate and the diffusion region. *Id.* at col. 3, ll. 8–11, 23–27.

ILLUSTRATIVE CLAIM

7. A method of forming a local interconnect in a semiconductor structure, comprising the step of:

depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said sidewall spacer being disposed above said diffusion region, said via being in an insulating material on said gate.

GROUND OF INSTITUTION

In our Decision to Institute, we instituted trial on the following challenges to patentability:

Claims 7–9, 15, and 17 as anticipated under 35 U.S.C. § 102(e) by Sakamoto;² and

Claims 10–12 as obvious under 35 U.S.C. § 103(a) over the combination of Sakamoto and Cederbaum.³

CLAIM CONSTRUCTION

In our Decision to Institute, we applied the ordinary and customary meaning to the terms not construed. We applied the broadest reasonable interpretation to the following term that required construction. Noting a claim construction dispute in co-pending district court litigation, Petitioner proposed that we construe the “diffusion region formed in said substrate” to mean “conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate.” Pet. 24. As discussed in the Decision to Institute, we determined that the subject matter of the claims concerns a local interconnect between a gate and a diffusion region and that there was no need to further construe “the diffusion region formed in said substrate” for purposes of this decision. Dec. to Inst. 5–6. Based on the complete record now before us, we discern no reason to change the constructions.

ANALYSIS OF PRIOR ART CHALLENGES

Introduction

As previously discussed, Patent Owner has provided no evidence or argument in response to claim challenges advanced in the Petition. Patent

² U.S. Patent No. 5,475,240 issued Dec. 12, 1995, Ex. 1003 (“Sakamoto”).

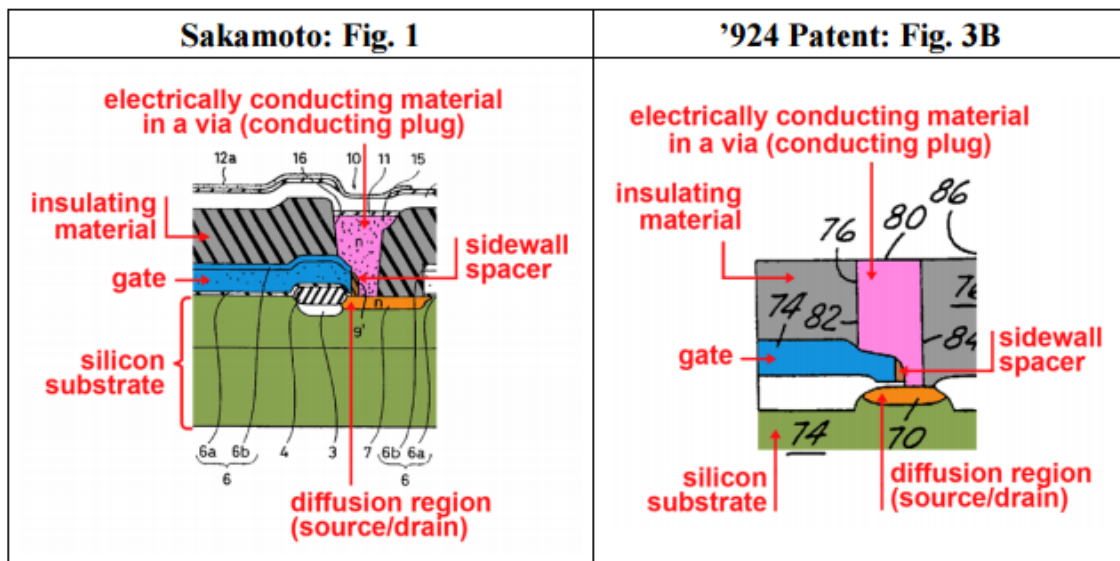
³ U.S. Patent No. 5,100,817 issued Mar. 31, 1992, Ex. 1004 (“Cederbaum”).

Owner's election not to file a Patent Owner Preliminary Response does not implicate any adverse inference. 37 C.F.R. § 42.107(a); Office Patent Trial Practice Guide. 77 Fed Reg. 48756, 48,764 (Aug. 14, 2012). However, as to the Patent Owner Response after institution of trial, under our Scheduling Order "Patent Owner is cautioned that any arguments for patentability not raised in the response will be deemed waived." Paper 11, 3; *see In re Nuvasive*, 842 F. 3d 1376, 1381 (Fed. Cir. 2016) (finding that NuVasive waived public accessibility arguments in its Preliminary Response by failing to challenge public accessibility during the trial phase, i.e. by not addressing public accessibility in its Trial Response and explicitly declining to make further arguments at oral hearing). In this case, Patent Owner "defers to the Board" to determine whether Petitioner has demonstrated the challenged claims are unpatentable by a preponderance of the evidence. PO Resp. 2. There is no argument or evidence, other than that presented in the Petition and the accompanying Exhibits, for us to consider. Nevertheless, "In an *inter partes* review, the burden of persuasion is on the petitioner to prove 'unpatentability by a preponderance of the evidence,' . . . and that burden never shifts to the patentee." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)).

Anticipation By Sakamoto

Petitioner contends that Sakamoto not only is directed to the same problem as that addressed by the '924 Patent, i.e., connecting different transistor portions together, but also that Sakamoto discloses the same solution as that found in the '924 Patent, i.e., using a single plug. Pet. 19–20.

Sakamoto “relates to improvement of a contact structure of an interconnection in a region having steps in a semiconductor device having a multilayer interconnection structure.” Ex. 1103, col. 1, ll. 12–16. Petitioner provides the following figure comparing an annotated version of Figure 1 of Sakamoto on the left with an annotated version of Figure 3B of the ’924 Patent on the right:



Petitioner’s comparison of Sakamoto Fig. 1
and ’924 Patent Figure 3B

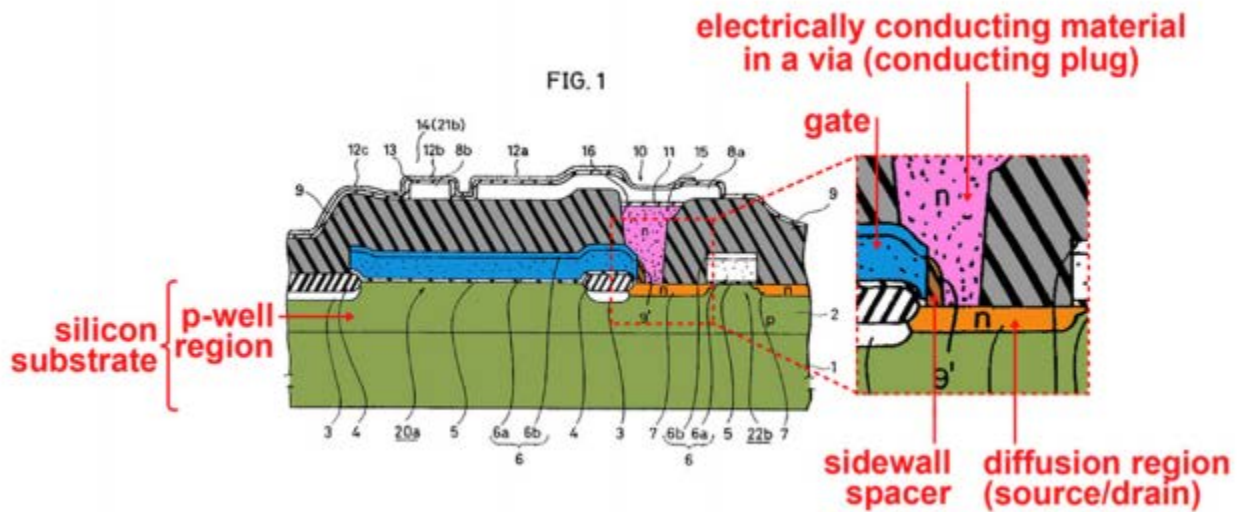
Pet. 20. Petitioner contends that Sakamoto discloses a plug filling an opening having a sidewall spacer that electrically connects a diffusion region to a gate, as claimed in the ’924 Patent. *Id.* at 20–21. Petitioner addresses each of the limitations of the claims challenged as anticipated by Sakamoto and discusses why specific features of Sakamoto are anticipatory. *Id.* at 27–46.

Turning to claim 7, Petitioner notes that Sakamoto discloses a method of forming a local interconnect in a series of steps for manufacturing a static

random access memory (SRAM) cell and that the Sakamoto's SRAM cell is a semiconductor structure. Pet. 27–28 (citing Ex. 1103, col. 7, ll. 14–15, col. 6, l. 39–col. 8, l. 52; Bravman Decl. ¶ 70).

Petitioner next compares the method recited in claim 7 with the disclosure in Sakamoto. Claim 7 recites the following elements as designated by Petitioner: (a) depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, (b) said semiconductor structure comprising said diffusion region in a silicon substrate, (c) said gate being on said substrate juxtaposed to but not contacting said diffusion region, (d) said sidewall spacer being disposed above said diffusion region, and (e) said via being in an insulating material on said gate. Although framed as a method claim, claim 7 recites the single step of depositing electrically conducting material in a via exposing at least a portion of a gate and a portion of a diffusion region, such that the electrically conducting material contacts the gate and diffusion region. The remaining elements of the claim recite effects (e.g., the contact by the electrically conducting material provides electrical communication between the gate and diffusion region) or structural features (e.g., the semiconductor structure comprising a diffusion region in the silicon substrate, a sidewall spacer, the via being in an insulating material on the gate).

Turning to element (a), Petitioner provides the following annotated illustration of Figure 1 of Sakamoto, including an expanded view of the region where the electrically conducting plug is located:



Petitioner's annotated illustration of Figure 1 of Sakamoto
with exploded view of electrically conducting contact

Pet. 29. Petitioner uses this figure to illustrate that Sakamoto shows electrically conducting plug 15 in via opening 16 formed in insulating layer 9 and that plug 15 is connected directly to source/drain region 7 and gate electrode 6. *Id.* at 29–30. Figure 1 of Sakamoto also shows sidewall spacer 9'. *Id.* at 30. Petitioner points out that Sakamoto describes the plug layer 15 is formed when polycrystalline silicon layer 15a is deposited to fill opening 16 and is etched leaving a portion of the layer only within opening 16. *Id.* at 29–30 (citing Bravman Decl. ¶ 72). An N type impurity is introduced into the polycrystalline silicon plug layer 15 to provide conductivity. *Id.* at 31 (citing Ex. 1103, col. 6, ll. 49–col. 7, l. 14). Via 16 exposes a portion of gate electrode 6 and diffusion region (source/drain region 7), so that when plug layer 15 is present, contact between the gate and diffusion region provides electrical communication. *Id.* at 30–31.

Element (b) of claim 7, as identified by Petitioner, recites that the semiconductor structure comprises the diffusion region in a silicon substrate. Petitioner contends that Sakamoto teaches that the diffusion region constitutes source/drain region 7 and that the diffusion region contains dopants implanted in the silicon substrate. Pet. 33–34. Figure 1 of Sakamoto delineates a main silicon substrate 1 and a p-well region 2 above it. Petitioner acknowledges that Figure 1 of Sakamoto illustrates a p-well region 2, but contends that the p-well region is part of the silicon substrate. *Id.* at 35–37. Petitioner argues that p-well region 2 is formed below the top surface of silicon substrate and a source/drain region 7 is formed in the silicon substrate below the top surface of p-well region 2. *Id.* at 32–33. Petitioner contends that p-well region 2 is part of the silicon substrate because p-well region 2 is formed in the surface of the substrate. *Id.* at 35 (citing Ex. 1103, col. 7, ll. 17–21, disclosing that a “p type impurity is implanted in a main surface of a silicon substrate” and that the “implanted p type impurity is diffused to the depth of about 2–3 μm from the main surface of substrate 1 by heat treatment to form a p well 2”). Petitioner also notes that during prosecution, the applicant for the ’924 Patent did not dispute the Examiner’s assertion that a diffusion region is formed within a silicon substrate and argued that the cited reference (Kinoshita) disclosed buried ground layers in the substrate. *Id.* at 35–37 (citing Ex. 1113 and Ex. 1114). Petitioner further contends that in at least one embodiment (the fifth embodiment shown in Figure 25), Sakamoto does not delineate the p-well region, stating that an n-type impurity region is formed on a surface of the silicon substrate. *Id.* at 37 (citing Ex. 1103, col 12, ll. 57–58). Whether or not there is a distinction to be drawn between Sakamoto’s first four

embodiments, which all delineate p-well region 2 and Sakamoto's fifth embodiment in which p-well region 2 is not shown, based on the record in this proceeding, we are persuaded that the evidence supports Petitioner's contention that the implanted p-well region is part of the silicon substrate.

Based on this analysis, we are persuaded by Petitioner's argument that Sakamoto discloses element (a) depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region. As to element (b), we are persuaded by Petitioner's argument that Sakamoto discloses a semiconductor structure comprising a diffusion region in a silicon substrate.

Element (c) of claim 7, as designated by Petitioner, recites "said gate being on said substrate juxtaposed to but not contacting said diffusion region." Figure 1 of Sakamoto illustrates field oxide film 4 and p+ isolation layer 3 formed on a prescribed region of a surface of p-well 2 for isolation. Ex. 1103, col. 7, ll. 22–23. Oxide film 5 is formed on the surface of the p-well 2. *Id.* at col. 7, ll. 23–24. A polycide film of polysilicon and refractory metal silicide is deposited on the surface of oxide film 5 and patterned to form gate electrode 6. *Id.* at col. 7, ll. 24–31.

Petitioner contends that the placement of the gate electrode in Sakamoto over a field oxide layer constitutes forming the gate on said substrate because the applicant for the '924 Patent relied on conception of the same physical construct during prosecution in a Declaration under 37 C.F.R. § 1.131 ("Rule 131 Declaration"). Pet. 38 n.7 (citing Ex. 1106,

Ex. A).⁴ The specification of the '924 Patent does not discuss forming the gate electrode on the substrate in detail, stating only that a photoresist layer used to pattern and etch openings for the diffusion regions is removed and that polysilicon then deposited on substrate 74 is etched to form gate electrode 74. Ex. 1101, col. 3, ll. 49–58. In this context, the statements in applicant's Rule 131 Declaration provide context to the meaning of "said gate being on said substrate." In order to antedate a reference, Patent Owner demonstrated an invention in which the gate electrode is formed over a field oxide layer. Therefore, based on the complete record before us, we agree with Petitioner that taken in the proper context, notwithstanding the presence of the field oxide layer 4 and field oxide film 5, Sakamoto discloses the gate electrode formed on the substrate.

Petitioner also argues that the gate in Sakamoto is juxtaposed from but is not in direct contact with the diffusion region, as recited in claim 7. Pet. 39–41. Petitioner contends that oxide film 5 separates the gate from the diffusion region, noting that there would be no need for the claimed plug to connect the gate and the diffusion region if this were not the case. *Id.* at 40. Sakamoto states:

The sectional structure of the memory cell shown in FIG. 1 [of Sakamoto] is the same as the sectional structure of a conventional memory cell shown in FIG. 28 except for a structure of direct contact. . . .

Direct contact portion 10 includes an n type polycrystalline silicon plug layer 15 . . . directly connected to the n⁺ source/drain region 7 and gate electrode 6 . . . embedded within opening 16.

⁴ Petitioner appears to be citing to the center figure at the top of page 11 of Ex. 1106.

Ex. 1103, col. 6, ll. 42–58. Figures 1 and 28 in Sakamoto illustrate that because of the presence of oxide film 5, in the absence of plug 15, there is no direct contact between gate 6 and source/drain region 7. Therefore, on this record we agree that Petitioner has shown Sakamoto discloses element (c) of claim 7, as designated by Petitioner.

Petitioner designates as element (d) of claim 7 the recitation “said sidewall spacer being disposed above said diffusion region.” Pet. 41. Petitioner designates as element (e) of claim 7 the recitation of “said via being in an insulating material on said gate.” *Id.* at 43. Petitioner cites insulating layer 9 shown in Figure 1 of Sakamoto as disclosing element (e) of claim 1 of the '924 Patent. *Id.* Petitioner cites sidewall spacer 9' in Figure 1 of Sakamoto as disclosing the claimed sidewall spacer. *Id.* at 41–42. On this record, we agree with Petitioner’s arguments because Sakamoto discloses interlevel insulating layer 9 disposed above the gate and diffusion region and that an opening 16 for direct contact formed using a photolithography method leaves sidewall spacer 9'. Ex. 1103, col. 7, ll. 47–51.

Based on this analysis and the record in this proceeding, Petitioner has demonstrated by a preponderance of the evidence that Sakamoto discloses all of the elements of claim 7.

Claim 8 depends from claim 7 and recites that the diffusion region is an N⁺ or P⁺ region. Petitioner notes, and we agree, that Sakamoto discloses the diffusion region as an N⁺ region because it expressly refers to an n⁺ source drain region 7. Pet. 44.

Claim 9 depends from claim 7 and recites that the insulating material is selected from the group consisting of silicon oxide and silicon nitride.

Petitioner cites Sakamoto's disclosure of softening and reflowing BoroPhosphoSilicate Glass (BPSG) film to form insulating layer 9, stating that BPSG is a type of silicon oxide. *Id.* at 44–45 (citing Bravman Decl. ¶ 91; Ex. 1115, at 185).⁵ We credit Dr. Bravman's testimony and are persuaded that insulating layer 9 is formed of silicon oxide.

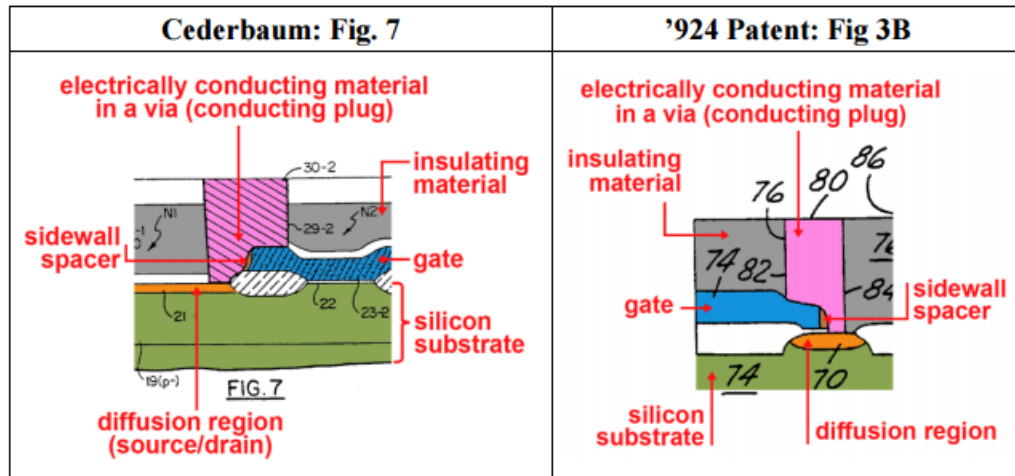
Claim 15 depends from claim 7 and recites "said gate is a polysilicon gate." Claim 17 depends from claim 7 and recites "said gate comprises polysilicon." Petitioner notes, and we agree, that Sakamoto discloses the gate electrode 6 is formed of polycrystalline silicon, which is another name for polysilicon. *Id.* at 46.

In consideration of the above, the record in this proceeding demonstrates that Petitioner has shown by a preponderance of the evidence that claims 7–9, 15 and 17 are anticipated by Sakamoto.

Obviousness Over Sakamoto and Cederbaum

Petitioner contends that claims 10–12 are obvious over the combination of Sakamoto and Cederbaum. Comparing Figure 7 of Cederbaum to Figure 3B of the '924 Patent, Petitioner contends that Cederbaum discloses a structure that includes components arranged in a way that is identical to those of Fig. 3B of the '924 Patent. Pet. 23. The figure below is Petitioner's comparison of Fig 7 of Cederbaum on the left and Figure 3B of the '924 Patent on the right.

⁵ Although Petitioner does not cite Ex. 1115 as a basis for its challenge that claim 9 is anticipated by Sakamoto, we understand Petitioner's citation to demonstrate that one of ordinary skill would infer the limitation is disclosed by Sakamoto. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991).



Petitioner's Comparison of Fig. 7 of Cederbaum
to Fig 3B of the '924 Patent

Id. at 22. Petitioner emphasizes that, like the '924 Patent, Cederbaum concerns the use of a contact stud or conducting plug to fill an opening with a sidewall spacer to directly connect a source/drain region to a gate electrode. *Id.*

Claim 10 recites “said electrically conducting plug is a metal plug.” Claim 11 recites “said electrically plug is preferably a refractory metal plug.” Claim 12 recites “said electrically conducting plug is formed of a material selected from the group consisting of titanium, tantalum, molybdenum and tungsten.” Petitioner cites Cederbaum’s disclosure at column 9, lines 31–65 as disclosing a tungsten conducting plug. *Id.* at 47–48. Petitioner argues that one of ordinary skill would have been motivated to combine the teachings of Cederbaum with those of Sakamoto because they both teach the same type of device and are directed to the same problem, i.e., stacking transistors in a SRAM. Pet. 49. Petitioner points out that Cederbaum and Sakamoto also disclose nearly identical structures with

nearly identical components, with both employing an electrically conducting plug within an opening that contains a sidewall spacer to directly connect a diffusion region to a gate. *Id.* at 50–51. Petitioner cites Cederbaum’s disclosure of materials, such as refractory metals, to be used in forming the conductive plug and Sakamoto’s discussion of the advantages to using a conductive plug of increased conductivity. *Id.* at 51–52. In view of these disclosures, we agree with Petitioner that it would have been obvious to one of ordinary skill to replace the polycrystalline plug 15 of Sakamoto with a refractory metal plug of tungsten, as disclosed by Cederbaum. *Id.* at 48–49.

The complete record before us supports Petitioner’s contentions. In consideration of the above, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 10–12 are obvious over the combination of Sakamoto and Cederbaum.

CONCLUSION

Based on the record in this proceeding, we conclude Petitioner has demonstrated by a preponderance of the evidence that:

Claims 7–9, 15, and 17 of the ’924 Patent are unpatentable under 35 U.S.C. §102 as anticipated by Sakamoto; and

Claims 10–12 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Sakamoto and Cederbaum.

ORDER

In consideration of the above it is:

ORDERED that claims 7–10, 12, 15, and 17 of the ’924 Patent are unpatentable; and

FURTHER ORDERED, that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER

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