SILICON PROCESSING **FOR** THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

STANLEY WOLF Ph.D.

Professor, Department of Electrical Engineering California State University, Long Beach Long Beach, California

Instructor, Engineering Extension, University of California, Irvine

RICHARD N. TAUBER Ph.D.

Manager of VLSI Fabrication TRW - Microelectronics Center Redondo Beach, California and

Instructor, Engineering Extension, University of California, Irvine

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images, gives good critical dimension control, good contrast, and adequate depth of focus. It also has the potential for allowing the slope of the resultant images to be controlled without the film thickness loss normally present in conventional positive resist processing. Wall angles in excess of 90° (i.e. inverted wall angles) may even be produced, a feature that could be useful in metal lift-off processing.

Multilayer Resist Processes

As resist films cross over steps their local thickness is altered. This arises because the resist that crosses the top of the steps is much thinner than the resist that covers wafer regions which are low-lying. Thus, during exposure either the thin resist becomes overexposed, or the thicker resist underexposed. Upon development, a resist pattern crossing a step will therefore possess a linewidth variation (i.e. narrower on the top of the step). For lines in which step heights approach the size of the linewidth (e.g. for linewidths or spaces of 1 μ m or less), such variations in dimension become intolerable. In addition, standing wave effects in thick resist layers reduces their minimum resolution. Finally, reflective substrates also degrade resolution in thick resist films (see section Linewidth Variation Over Steps).

The use of thin resist films could relieve the problems from standing waves and reflective substrates, but would not overcome the step coverage limitation. A thick planarizing layer under a thin-imaging layer would, however, reduce the impact of all of the problems listed above. Approaches using such underlying planarizing layers are known as multi-level resist (MLR) processes, since two or more layers are required to implement them²¹.

In MLR processes, an organic layer is therefore first spun onto the wafer, thicker than the underlying steps, to provide a surface which is smooth and significantly more planar than the original wafer topography. After pre-baking this bottom layer, a thin imaging layer is deposited. In some cases a third thin transfer layer, such as SiO_2 , is deposited on the thick layer prior to depositing the imaging layer. High resolution patterns are then created in the thin top layer. These are next precisely transferred into the bottom layer using the delineated imaging layer as a blanket exposure mask, or as an etching mask to pattern the planarizing layer. Patterns with resolutions less than 0.5 μ m have been delineated with MLR processes.

The advantages gained by MLR processes, however, are obtained at the expense of added complexity. This can result in diminished throughput, possible increase in defects, and increased costs. The degree of additional complexity that can be tolerated, and the expected increase in defect density depend on the maturity of the alignment tools and the overall device process.

Three multilayer resist processes will be described in this section: a) a portable conformable mask process, or PCM; b) an organic tri-layer process; and c) a bilayer process utilizing an inorganic resist (Ag_2Se/Ge_xSe_{1-x}) as the imaging layer.

The *PCM* is the simplest MLR scheme, and is the only one that has reportedly been used by 1985 in a VLSI production mode²². In this process, a thick underlying layer of resist (e.g. PMMA, which is sensitive to deep UV), is used to planarize the surface. A thin resist that is sensitive to the near UV, but opaque to deep UV, is then deposited over the PMMA.

The upper layer is conventionally patterned, and subsequently used as a conformal deep UV mask for PMMA. The PMMA is then flood exposed (using deep UV) and developed. The resolution of the PCM process, and that of the tri-layer processes are equal, since they utilize the same imaging resist layer. The resolution of Ge_xSe_{1-x} layer process is higher because of its edge sharpening effect. The instability of the PMMA under dry etch, however, is a limitation of the PCM process. To improve the durability during dry-etching, the imaging resist is often retained on top of the PMMA. This is often referred to as a capped structure. Another attraction

of the PCM process is that it can be done on conventional lithographic equipment, together with a source of deep-UV for the flood exposure of the PMMA. On the other hand, film interface layers at the PMMA /optical resist interface can cause exposure and develop problems.

In the *tri-layer resist* process (Fig. 11), a thick organic layer is again used to partially planarize the surface²³. Materials investigated for this layer have included conventional positive optical photoresist, polyimide, and polysulfone. A thin layer of SiO₂ (spin-on or PECVD) is then deposited to act as an etch mask for the bottom layer. An imaging resist layer is finally applied, and patterned in a conventional manner (e.g. near-UV exposure and wet development). To minimize effects from standing waves and reflections from the substrate, the lower layer is treated to increase its optical density (see the section on *Resist Processing: Exposure*). The SiO₂ and lower layer are dry etched anisotropically to precisely transfer the pattern from the thin imaging layer into the thick lower layer. The main disadvantage of the tri-layer process is the added complexity that it requires.

In Ge-Se based bilayer processes, the high contrast and resolution advantages of Ge-Se chalcogenide glasses are exploited (see section on *Inorganic Resists*). These materials are used for the imaging layer of a bilayer structure. The bottom layer is again a thick polymer, such as AZ2400 resist. This process exhibits the highest resolution limit of the three MLR processes discussed, but is also the most complicated to develop. Since its resolution capability is potentially so small, however, it has been identified as a process that might compete favorably with x-ray or electron beam lithography²¹.

Contrast Enhancement Layers

An alternative technique to the multilayer resist processes for increasing the maximum resolution obtainable with projection aligners, uses a photobleachable top layer called a *contrast* enhancement layer (CEL)²⁴. The penalties incurred for obtaining the improved resolution are

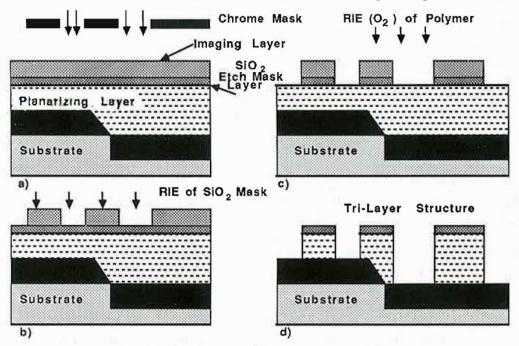


Fig. 11 Schematic of the tri-layer process²¹. Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

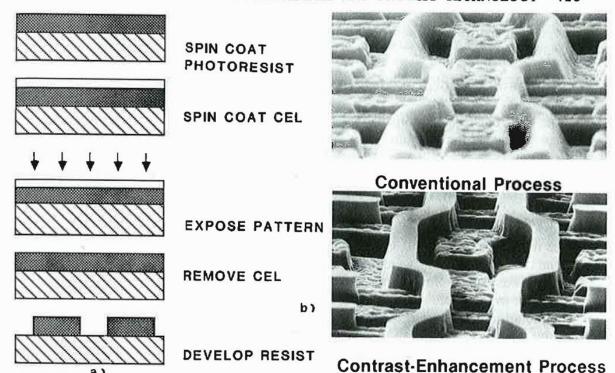


Fig. 12 (a) Photoresist process incorporating the CEL concept. Added CEL steps are outlined in boxes. (b) SEMs (8000X) of identical microcircuits produced with and without a CEL. Courtesy of the General Electric Research and Development Center.

increased process complexity, longer exposure times, and longer development times. Note, however, that use of a CEL increases exposure time by ~3x, but stepper time by only ~15%.

The CEL layer consists of a material that is spun onto a resist-coated wafer to a thickness of 1000-3000Å after soft-bake. This layer is normally opaque, but becomes transparent (bleached), when exposed to the light of the aligning tool. When the mask image from a projection printer is focused onto the wafer, regions of the opaque CEL layer that are struck by high-intensity light become transparent. This creates windows in the CEL through which light can shine and expose the resist. The unbleached CEL regions continue to absorb the relatively weak diffracted light. Since the CEL is in direct contact with the resist, it acts much like a thin mask used in contact printing. As discussed in Chap. 13, contact printers have higher resolution capabilities than projection printers. In addition, because the CEL is applied as a relatively thin film, it has an inherently high resolution capability. As such, use of a CEL layer allows the advantages of projection printing to be exploited, together with the benefits, but without the limitations of contact printing. In addition, unlike the PCM process, no interface layer problems are reported with CEL processes. The name is derived from the fact that the presence of the CEL layer increases the contrast of illumination that effectively reaches the resist.

Following exposure, the CEL layer is completely stripped prior to developing. This requires that an extra dispense head in a spray developer (see section on Resist Processing: Development) be used to spray on the stripping solution. A spin dry step is then performed before the normal development cycle is begun. The CEL stripping operation adds about 30 seconds to the development process.

Linewidths of ~0.5 μ m using commercially available optical photoresists and stepper projection systems have been achieved with the aid of a CEL compared to the 1 μ m resolution limit without CEL. Figure 12 shows SEM photographs of 2 μ m wide lines in photoresist

patterned with and without use of a CEL layer, and demonstrates the improvement that use of a CEL may provide.

Inorganic Photoresists

The finite contrast, γ , of organic-based resists limits their resolution capability. In order to increase the resolution capability of a photoresist process, without having to increase the numerical aperture NA of the system, or decrease the wavelength, λ , of the system source, a technique must be used to increase the resist contrast. It has been demonstrated that *inorganic resist materials* exhibit extremely high contrasts, and therefore high resolution capability (e.g. $\gamma = 6.8$ for inorganic resists, versus $\gamma \cong 2$ for organic resists). Delineation of 0.4 μ m lines and spaces using conventional optical lithography has been demonstrated by utilizing $\lambda = 405$ nm, a lens of NA = 0.35, and such an inorganic resist²¹.

The first such materials were based on the Ge-Se, that we introduced in the tri-layer MLR process discussion³¹. In such resists, Ge_xSe_{1-x} glasses are deposited as thin films by rf sputtering or evaporation. Next, a 1000Å layer of silver (Ag) is deposited by plating from an $AgNO_3$ solution onto the Ge_xSe_{1-x} surface, by a dip into an aqueous solution of $AgNO_3$. When this composite film is exposed to UV light (or electron radiation), the Ag diffuses into and dopes the Ge-Se matrix (Fig. 13). This renders the Ag-doped Ge-Se almost insoluble to alkaline solutions that would normally dissolve an amorphous Ge-Se film. Thus this process exhibits a negative resist type behavior. Note that although this mechanism implies that wet developing is used to create patterns in Ge-Se films, dry development in CF_4 is also feasible.

The resist also demonstrates a unique *edge-sharpening* behavior. That is, rapid lateral diffusion of the Ag during exposure (photodoping) takes place across the boundary between exposed and unexposed regions. The resulting Ag profile compensates for diffraction at the image edges, which leads to the sharp edges.

Inorganic resist materials also exhibit other attractive features for VLSI lithographic applications, including the following: a) there is no swelling during development and the edges have anisotropic profiles; b) the material is resistant to oxygen plasmas and hence is compatible with dry etched bilayer MLR processes; c) the materials possess a broad-band spectral response to all regions of the UV spectrum, while appearing opaque to light of all wavelengths up to 450 nm (thereby eliminating standing waves on reflective substrates) and is transparent to visible light.

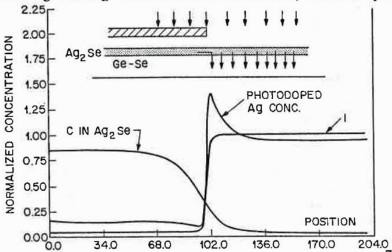


Fig. 13 Mechanism of edge sharpening effect in inorganic resist material⁷⁷. Reprinted with permission of the publisher, the Electrochemical Society.

performed before priming and spin-coating a wafer with resist. When carried out at atmospheric pressure, dehydration baking evolves moisture at three temperature plateaus³²: a) surface water molecules are liberated at 150-200°C; b) loosely held water of hydration is evolved at about 400°C; and c) total dehydration has been postulated to occur at temperatures in excess of 750°C. It is believed, however, that upon cooling, the water of hydration removed in step c) is reabsorbed from atmospheric moisture. Thus, some reports argue that no significant improvement over baking at 400°C should be expected. What is apparently important is the time delay between the dehydration bake and coating. In fact, to assure uniformity of processing, the recommended procedure is to carry out coating immediately after the dehydration bake. Dehydration bakes of up to 400°C are generally carried out in convection ovens, while 800°C bakes are performed in furnace tubes (both, of course, in dry-gas ambients).

Following the dehydration bake, the wafer is normally primed with a pre-resist coating of a material designed to improve adhesion even further³³. The most widely used priming substance is hexamethyldisilazane (HMDS)³⁴. Figure 15 shows how one end of the HMDS molecule reacts with wafer-oxide surfaces to tie up molecular water on a hydroxilated SiO₂ surface. It also shows how the other end of the HMDS molecule forms a bond with the resist. Thus, it is seen that the HMDS behaves as surface-linking adhesion promoter (e.g. SiO₂ surface-to-resist surface linkage). The wafers should be coated with resist as quickly as possible after priming, and it is recommended that coating be performed no later than 60 min after completing the priming step.

The HMDS is typically applied to the surface in one of two methods: a) spin coating; and b) vapor priming. In *spin coating*, the HMDS is dispensed onto the wafer surface through an additional nozzle present in the resist spin coating system. After the HMDS is dispensed, the wafer is spun at 3000-6000 rpm for 20-30 sec, causing approximately a monolayer of HMDS to remain on the wafer surface. In *vapor priming*, the HMDS is introduced in vapor form into a chamber containing the wafers. An exposure of the wafer surfaces to the HMDS vapor for ~10 min primes the surface so that good adhesion is obtained. The advantages of vapor priming are the following: a) wafers can be batch primed; b) since only vapors come in contact with the wafer surface, potential contamination from particles present in the HMDS solution is avoided; and c) less HMDS is used per wafer, thus providing a cost savings. Equipment that combines a vacuum dehydration bake of the wafers in the same chamber, prior to introducing HMDS vapors, is also commercially available. Such systems offer the opportunity to prime the wafers after vacuum dehydration baking (i.e. at a temperature less than is required for an atmospheric pressure bake), and without subsequently having to expose the wafers to atmospheric moisture.

Resist Processing: Coating

Following cleaning, dehydration baking, and priming, the wafers are ready to be coated with photoresist. The goal of the coating step is to produce a uniform, adherent, defect-free polymeric

Fig. 15 HMDS bonding mechanism with SiO₂³⁴.

film of desired thickness over the entire wafer. Spin coating is by far the most widely used technique to apply such films 35,36 . This procedure is carried out by dispensing the resist solution onto the wafer surface, and then rapidly spinning the wafer until the resist is essentially dry. In order to maintain reproducible linewidth in VLSI fabrication applications, resist film uniformity across the wafer (and from wafer-to-wafer) should be within at least ± 100 Å.

The spin coating procedure involves three stages: a) dispensing the resist solution onto the wafer; b) accelerating the wafer to the final rotational speed; and c) spinning at a constant speed to establish the desired thickness (and to dry the film).

The dispensing stage (a) can either be accomplished by flooding the entire wafer with resist solution before beginning the spinning, or by dispensing a smaller volume of resist solution at the center of the wafer and spinning at low speeds (e.g. 200 rpm for ~1 sec) to produce a uniform liquid layer across the wafer (spread cycle). In the latter method ~3.0 ml of resist is dispensed onto 100 mm wafers, and ~5.0 ml onto 150 mm wafers. It has also been found that static dispense (in which the wafer is stationary as the resist is dispensed), provides more uniform coatings than if the wafer is rotating (dynamic dispense).

In Stage (b) the wafers are normally accelerated as quickly as is practical to the final spin speed. High ramping rates have been shown to yield better film uniformities than low ramping rates. This is due to the fact that the solvent in the resist evaporates rapidly from the resist after it has been dispensed onto the wafer. Since film thickness depends on the viscosity of the liquid resist solution, the more time that is allowed for the solvent to evaporate during the spin-ramping to the final speed, the greater are the drying and film setting-up tendencies that contribute to thickness non-uniformity. A spin-ramp of 20,000 rpm /sec has been suggested as an adequate compromise to provide maximum coating uniformity, without causing motor-wear problems or excessive wafer breakage.

During Stage (c) the resist layer acquires a relatively uniform, symmetrical flow profile

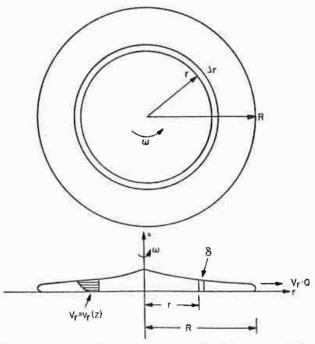


Fig. 16 Symmetrical flow pattern of a homogeneous liquid on a rotating disk showing flow rate, Q, and velocity profile v_r (z). Copyright 1977 by International Business Machines Corporation; reprinted with permission.

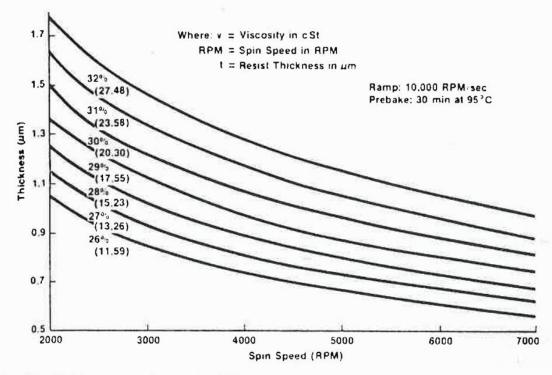


Fig. 17 Thickness vs spin speed of Kodak 820 resist. Courtesy of Eastman-Kodak Company.

(as shown in Fig. 16). Once this structure has been formed, the remainder of the high speed spinning cycle consists of solvent evaporation to produce the solid film. Most spin coating processes are performed with a final spin speed in the 3000-7000 rpm range for 20-30 sec, as this range provides good film uniformity, as well as limited spin-motor wear and wafer breakage. The highest degree of thickness uniformity ($\pm 100 \,\text{Å}$) is observed at the upper end of the range (6000-7000 rpm).

The spin coating fluid dynamics have been studied in some detail³⁵. It has been determined that prior to reaching the "equilibrium" form of Fig. 16⁴², the resist layer undergoes some intermediate shapes. At the start of spinning (i.e. within a few hundredths of a second), a wave of resist is created that then moves toward the wafer edge. The *corona stage* is next observed, in which the bulk of the resist that supported the wave runs out to the wafer edge to form a crown-like structure. When most of the resist has been driven off the wafer, the wave and corona disappear. At that point, centrifugal forces drive the remaining resist material off the surface in a fine spray that exhibts a spiral-like appearance. This *spiral stage* generates thousands of resist droplets as the material reaches the wafer edge and is flung off. The droplets leave the wafer at high speed and are thus subject to being bounced off of the spinner bowl sides, and redeposited on the wafer surface. To avoid this possibility, plastic splashguards and special exhausted bowl designs have been developed. An *edge bead* (a remnant of the corona stage, several times as thick as the deposited resist layer), also develops along the wafer edge during the spinning process³⁹. Edge-rounding of the wafers significantly reduces the edge-bead, and wafer backside washing with solvent after spin-coating can entirely remove it (as described further in Chap. 15).

The resist film thickness after spin coating, for a resist of constant molecular weight, solution concentration, etc., depends only on the spinning parameters. As an example, Fig. 17 shows the thickness curves of Kodak Micro Positive Resist 820 as a function of spin speed. Various mathematical relationships have been developed to predict the resist thickness as it depends upon such factors as percent solids, spin speed, etc. Most users, however, utilize data from the resist manufacturer to plan a baseline spin-coating process, and then empirically

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generate spin speed curves for their own specific process applications (i.e. that will depend on such specific parameters as resist formulation, spinner type, wafer size, spin parameters, and ambient temperature during deposition)⁴⁰. A study of thickness variation across a wafer as a function of many such parameters, including volume of resist dispensed, wafer diameter, resist viscosity, wafer spin-speed during dispense, wafer acceleration, and final spin-speed, was published in Refs. 37 and 38.

Resist film thickness can be measured in many ways. Contacting types of thickness measuring instruments are surface profilometers, which are capable of resolving 200Å steps. These are described in more detail in Chap 10. Noncontact types of thickness instruments utilize optical techniques of ellipsometry or interferometry. Automatic interferometer-based instruments have become widely used for resist thickness measurement, since they are easy to use, accurate, and perform the measurement quickly. Such instruments are discussed in Chap. 8.

There are also a variety of other aspects of the coating procedure that must be controlled in order to maintain an effective coating process, including: a) defect generation; b) the environment in which the coating is performed; and c) wafer handling and storage.

Defects can be introduced during the coating process in a number of ways, and some steps to minimize their generation include the following: a) Since the resist film is sticky until being soft-baked, it can easily entrap airborne particles. Thus, spinning should be done in a Class-100, or better, environment; b) The resist itself should be clean and free of all particulate matter above 0.2 µm in diameter. (Resist cleanliness and filtration prior to use is considered in an earlier section of this chapter.); c) The resist solution should be free of all entrapped air, as air bubbles can cause defects in the resist image that have the same effect as those caused by particles. Allowing a resist to sit for several days after filtration, and prior to application, will let dissolved air and gases to escape; d) radial resist striations (i.e. radial streaks of thickness different than the nominal resist thickness) are a form of defect caused by non-uniform solvent evaporation. One cause of striations has been attributed to excessive venting of the spin bowl³⁵. This depletes the solvent content from the ambient around a spinning wafer, and apparently leads to striation formation. Spin bowl exhaust flow can be controlled by special flow meters designed to sense the flow of gases in the bowl exhaust lines. When multiple bowls are exhausted by a single pump, the exhaust flow in a single line can vary if it is not controlled. This can cause resist thickness nonuniformities⁸³; e) the spin bowl should be designed to prevent splashback by resist droplets being spun off of the wafers; f) the nozzle that dispenses resist onto the wafer should be set close to the wafer surface to prevent splashing effects; g) the pump that controls the resist being dispensed through the nozzle should be designed to provide a suck-back action after the resist volume is dispensed onto the wafer. This suck-back function draws excess resist from the nozzle tip back into the supply line, thus preventing unwanted dripping onto the spinning wafer. The suck-back stroke must be adjustable so that air is not inadvertently drawn up into the nozzle tip. This could cause bubbles to become entrapped in the resist present in the nozzle line; and h) the chuck should be properly designed. That is, the chuck diameter should be large enough to consistently hold wafers and prevent breakage, and the vacuum ports should fasten wafers to the chuck in such a fashion that does not cause a resist puddle to form at the center of the wafer (due to dishing). Multiple vacuum ports are therefore preferred, as they distribute the vacuum force across the wafer area. (Note that new wafer hold-down mechanisms may need to be developed as wafer diameters and thicknesses continue to increase.)

The environment in which the spin-coating is carried out, must also be controlled. Since resist viscosity, and hence film thickness, depends on temperature, the latter should be controlled to $\pm 1^{\circ}$ C. In addition, the wafers, resist, and spinner hardware all need to maintained in thermal

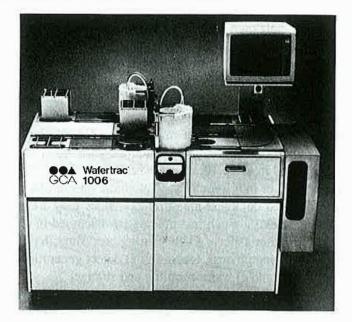


Fig. 18 Photograph of an automated in-line wafer spin coater. Courtesy of the GCA Corp.

equilibrium with one another. During spinning, solvent evaporation can lead to wafer cooling, and this may cause condensation of moisture on the resist surface. To avoid this problem, it has been recommended that the humidity be maintained at less than 50% RH. Since solvent vapors are flammable, exhaust equipment should also be spark-resistant to prevent the possibility of fire.

Upon completing the spin-coating cycle, wafers should be transported to the next step of the process, namely soft-bake, as soon as possible. Unbaked freshly spun films should not be stored in excess of a few hours, since their tacky consistency makes them vulnerable to particulate contamination. If particles contact the resist surface prior to soft-bake they become almost impossible to remove, and they will lead to pinhole or opaque defects after exposure and development. The wafers should be placed in a dry box for short-term storage, and should be soft-baked immediately before exposure.

Resist coating equipment (e.g. Fig. 18) is manufactured by a variety of suppliers⁴¹. Most suppliers offer equipment with cassette-to-cassette operation. Wafer handling and transport systems vary from one model to another. Microprocessor control, including programming capability, and a *lock-out* feature, is also typically offered (i.e. in lock-out, once the coating process recipe has been programmed into the machine, it cannot be altered unless the system is "unlocked", presumably by a responsible authority). Equipment process control and diagnostic capabilities are also offered. Since more than one wafer size may need to be processed, the ability to handle multiple wafer sizes may be important. Equipment that can perform priming, baking, and coating on one track in an automated manner, is also coming into widespread use.

Resist Processing: Soft-Bake

After wafers are coated with resist, they are subjected to a temperature step, called *soft-bake* (or *pre-bake*)^{42,43}. This step accomplishes several important purposes, including: a) driving off solvent from the spun-on resist, reducing its level in the film from ~20-30% to ~4-7%; b) improving the adhesion of the resist, so that it is better able to adhere during the development step; and c) annealing the stresses caused by the shear forces encountered in the spinning process.

temperature been determined to yield the desired undercut?

- c) If dry etching is to be used, how susceptible is the resist to erosion?
- d) Does the etching procedure make the resist difficult to remove?
- 3) Sizes of Patterned Features:
 - a) Can the critical dimension (CD) objectives (linewidth and spacing) be met by the resist resolution under all normal process variations? (i.e. is there sufficient process latitude in resist system?)
 - b) Have optimization experiments for bake, exposure and development been conducted?
- 4) Equipment Considerations:
 - a) Are the resists and developers compatible with existing processing equipment?
 - b) Is the resist sensitive enough to yield adequate exposure throughput?
 - c) What is the technological life of the equipment with which the resist is used?

 (i.e. If it is short, will the resist still be compatible with replacement equipment?)
 - d) Have other users of the resist system and equipment combination under consideration been identified? If so, it may be possible to learn from their experience.
- 5) Ecological and Disposal Considerations:
 - a) Do the resist or developer materials contain any toxic or hazardous components that cannot be safely handled with existing current processing equipment?
 - b) Have disposal recommendations been obtained form the resist vendor?
 - c) What are the current guidelines for legal disposal?

With the answers to these questions, the number of candidate resists can probably be reduced to a small enough group to construct a test matrix to allow the final selection to be made.

REFERENCES

- M.J. Bowden, "A Perspective on Resist Materials for Fine Line Lithography", in Materials for Microlithography, Advances in Chemistry Series, No. 266, American Chemical Society, 1984, Washington, D.C., Chap. 3, p. 39-117.
- 2. J. Bargon, "Lithographic Materials", in Methods and Materials in Microelectronic Technology, J. Bargon, Ed., Plenum Publishers, New York, 1984.
- C.G. Willson, "Organic Resist Materials Theory and Chemistry", L.F. Thompson, C.G. Willson, M.J. Bowden, Eds., Introduction to Microlithography, Advances in Chemistry Series, No. 219, American Chemical Society, Washington, D.C., 1983, Chap. 3, p. 87-157.
- 4. P.S. Gwozdz, "Positive vs. Negative: A Photoresist Analysis", SPIE Proceedings, Semiconductor Microlithography VI, Vol. 275 (1981), p. 156.
- 5. M.C. King, "Principles of Optical Lithography", in N.G. Einspruch, Ed., VLSI Electronics, Microstructure Science, Academic Press, New York, 1981, Chap. 2.
- 6. R.W. Wake, M.C. Flanigan, "A Review of Contrast in Positive Resists", Proceedings SPIE, Vol. 539, Advances in Resist Technology and Processing, II, 1985, p. 291.
- 7. K.L. Tai, et al., J. Vac. Sci. Technol., 17, 1169 (1980).
- L.F. Thompson and M.J. Bowden, "Resist Processing", in L.F. Thompson, C.G. Willson, M.J. Bowden, Eds., *Introduction to Microlithography*, Advances in Chemistry Series No. 219, American Chemical Society, Washington, D.C., 1983, Chap. 4, 172.
- 9. ibid., Ref. 1, p. 49.
- 10. H., Gokan, K. Tanigaki, Y. Ohnishi, "Dry-Etch Resistance of Metal-Free and Halogen-Substituted Resist Materials", Solid State Technol., May '85, p. 163.
- 11. P.H. Singer, "Trends in Resist Design and Use", Semiconductor International, Aug. '85, p. 68.
- 12. American Society for Testing and Materials, Published Methods and Procedures, "Standard

- Methods for Testing Photoresists in Microelectronic Fabrication"; Test Std F-66-84, (1984)
- M.L. Long, "Photoresist Particle Control for VLSI Microlithography", Solid State Technol., Mar. '84, p. 159.
- 14. N.J. Sax, Dangerous Properties of Industrial Materials, Reinhold, New York, 1980.
- 15. D.J. Elliot, Integrated Circuit Fabircation Technology, McGraw-Hill, New York, 1982.
- 16. T. Pampalone,"Novalac Resins Used in Pos. Resist Systems" Sol. State Tech., June 84,p 115.
- 17. R., Rubner, E. Kuhn, ACS Div. Org. Coatings and Plast. Chem. Preprint 1977, 37, (2), 118
- 18. ibid., Ref. 5, p. 51.
- S.A. MacDonald, et al., "The Production of a Negative Image in a Positive Photoresist", Kodak Microelectronics Seminar, San Diego, 1982.
- E. Alling and C. Stauffer, "Image Reversal Process of Positive Resist" Proceedings SPIE, Volume 539, Advances in Resist Technology and Processing II, Mar. 11-12, 1985, p. 194.
- E. Ong and E.L. Hu, "Multilayer Resists for Fine Line Optical Lithography," Solid State Technol., June '84.
- 22. K. Bartlett, et al., Proceedings SPIE, Vol. 394, Optical Microlithography II, 1983, p. 49.
- 23. J. M. Moran and D.J. Magdan, J. Vac. Sci. Technol., 16, 1620 (1979).
- B.F. Griffing and P.R. West, "Contrast Enhanced Lithography", Solid State Technology, May '85, p. 152.
- 25. M.J. Bowden and L.F. Thompson, Polymer Eng. and Sci., 14, 525 (1974).
- 26. ibid., Ref. 1, p. 103-106.
- 27. ibid., Ref. 1, p. 56.
- 28. ibid., Ref. 1, p. 57-65.
- 29. T.D. Berker and S.E. Bernacki, IEEE Trans. Electron Dev. Lett. EDL-2, 281, (1981).
- R. Rubner, H. Ahne, E. Kuhn, and G. Kolodziej, "A Photopolymer The Direct Way to Polyimide Patterns", Phot. Sci. Eng., 23 (5), 303, (1979).
- 30. O. Rohde, et al, "Recent Advances in Photoimagable Polyimides," Proceedings SPIE, Vol. 539, Advances in Resist Technology and Processing II, 1985, p. 175.
- 31. A. Yoshikawa, et al, Appl. Phys. Letts., 31, 167 (1977).
- 32. R.D. Lussow, J. Electrochem. Soc., 115, p. 660-663, (1968).
- 33. K. Mittal, "Factors Affecting Adhesion of Lithographic Matls" Sol. State Tech., May 79, p.89.
- 34. R.H. Collins and F.T. Deverse, U.S. Patent No. 3,549,368, Dec. 22, 1970.
- 35. ibid., Ref. 15, Chap. 6, "Spin Coating", p. 125-44.
- 36. ibid., Ref. 8, p. 186-94.
- P.O'Hagan and W.J. Daughton, "An Analysis of the Thickness Variance of Spun-On Photoresist," Kodak Interface Conference Proceedings, 1977, p. 95.
- 38. W. Daughton, P. O'Hagan, and F.L. Givens, "Thickness Variance of Spun-On Photoresist, Revisited", Kodak Interface Conference Proceedings, 1979, p. 16.
- 39. M.W. Chan, "Another Look at Edge Bead", Kodak Seminar Proceedings, 1975, p. 16.
- American Society of Materials and Testing; Published Methods and Procedures "Standard Practice for Producing Spin Coating Resist Thickness Curves", Test Standard F-804-83.
- 41. ibid., Ref. 15, Chap. 7, "Softbake", p. 145-163.
- 42. B. D Washo, IBM Journal of Research and Development, 21 (2), 190 (1977).
- 43. ibid, Ref. 8, p. 195-8.
- 44. T. Batchelder, J. Piatt, "Bake Effects in Positive Resist" Solid State Technol., Aug. 83, p.211.
- 45. G. MacBeth, "Prebaking Positive Photoresists", Proc. Kodak Interface Seminar, 1982, p. 87.
- J.A. Irvin and T.J. Weber, "Characterization of Baking Operations in Photolithographic Processes", Proceedings Kodak Interface Seminar, 1982, p. 31.
- 47. ibid., Ref. 15, Chap. 8, "Exposure", p. 165-188.

- 48. ibid., Ref. 8, p. 199.
- 49. D.F. Ilten and K.V. Patel, "Standing Wave Effects on Photoresist Exposure", Image Technology, Feb.-Mar., 1979, p. 9.
- A.R. Neureuther, P.K. Jain, W.G. Oldham, "Factors Affecting Linewidth Control Including Multiple Wavelength Exposure and Chromatic Aberation", SPIE Proceedings, Vol. 275, Semiconductor Microlithography, 1981, p. 110.
- 51. I. Bol, Kodak Interface Microelectronics Seminar, San Diego, 1984.
- 52. W. Arden & L. Mader, "Linewidth Control in Optical Projection Printing: Influence of Resist Parameters", SPIE Proc. Vol. 539, Adv. in Resist Technol. and Processing II (1985), p. 219.
- 53. K. Harrison and C. Takemoto, "The Use of Antireflection Coatings for Photoresist Linewidth Control", Kodak Interface Microelectronics Seminar, 1983, p. 107.
- 54. A.T. Jeffries, et al, "Two Anti-Reflective Coatings for Use Over Highly Reflective Topography", SPIE Proc., Vol. 539, Advances in Technology and Processing II, 1985,p. 342.
- 55. R.D. Coyne and T. Brewer, "Resist Processes on Highly Reflective Surfaces Using Anti-Reflection Coatings", Kodak Interface Seminar Proceedings, 1983, p. 40.
- 56. ibid., Ref. 15, Chap. 9, "Development", p. 209-31.
- 57. ibid., Ref. 8, p. 204-210.
- 58. D. Burkman and A. Johnson, "Centrifugal On-Center, Flood Spray Development of Positive Resist", Solid State Technol., May '83, p. 125.
- 59. R.F. Leonard and J.A. McFarland, "Puddle Development of Positive Photoresists", SPIE Proceedings, Vol. 275, Semiconductor Microlithography VI, (1981).
- T. Rodriguez, P.D. Krasicky, and R.J. Groele, "Dissolution Rate Measurements", Solid State Technol., May '85, p. 125.
- J.S. Peterson, A.E. Kozlowski, "Optical Performance and Process Characterizations of Several High Contrast Metal-Ion Free Developer Processes", SPIE Proceedings, Vol. 469, Advances in Resist Technology (1984), p. 46.
- 62. D.W. Frey, J.R. Gould, and E.B. Hryhorenko, "Edge Profile and Dimensional Control for Positive Resist", Kodak Interface Seminar Proceedings, 1981, p. 40.
- 63. P. Burggraaf, "Wafer Inspection for Defects", Semiconductor International, July, 1985, p. 57.
- D. Nyyssonen, "Optical Linewidth Measurement on Patterned Wafers," SPIE Proceedings, Vol. 480, Integrated Circuit Metrology, 1984, p. 65.
- 65. G. Toro-Lira and R. Mellen, "Critical Dimension Control in the Late Eighties", Microelectronic Manufacturing and Testing, Part 1, Jan. '85, p. 9, Part II, Feb. '85, p. 19.
- 66. ibid., Ref. 15, Chap. 10, "Postbaking", p. 233-243.
- 67. ibid., Ref. 8, p. 211.
- K. Massau, R.A. Levy, and D.L. Chadwick, "Modified Phosphosilicate Glasses for VLSI Applications", J. Electro. Chem. Soc., Vol. 132, No. 2, Feb. '85, p. 409.
- 69. P. van Pelt, "Processing Deep UV Resists" SPIE Proc. Vol. 275, Semicon. Litho. 1981, p. 150.
- Y.T. Yen and M. Foster, "Deep UV and Plasma Hardening of Positive Photoresist Patterns", Proceedings Kodak Interface Seminar, 1982, p. 125.
- 71. DRMR Development Rate Monitor PEO-4587, Perkin-Elmer Corp, Garden Grove, CA, Aug '84.
- D.G. Seiler and D.V. Sulway, "Precision Linewidth Measurement Using a Scanning Electron Microscope", SPIE Proceedings, Vol. 480, Integrated Circuit Metrology, 1984, p. 86.
- J.T. Lindow, S.D. Bennet, and I. Smith, "Scanned Laser Imaging for Integrated Circuit Metrology", SPIE Proceedings, Micron and Submicron Circuit Metrology, Vol. 565, 1985, p. 81.
- 74. P. Singer, "Linewidth Measurement & Process Control", Semiconductor Int'l., Feb.'85, p. 66.
- M.T. Postek, "Critical Dimension Measurement in the Scanning Electron Microscope", Proceedings SPIE, Vol. 480, IC Metrology II, 1984, p. 109.

- 76. P.E. Russell, et al, "Development of SEM-based Dedicated IC Metrology System", Proceedings SPIE, Vol. 480, IC Metrology II, 1984, p. 101.
- 77. K.L. Tai, Proc. Symp. on Inorganic Resist Systems, 1982, Electrochemical Soc. 82-9, p.49
- 78. T.R. Pampalone and F.A. Kuyan, "Improving Linewidth Control Over Reflective Surfaces Using Heavily Dyed Resists", J. Electrocem. Soc., 133, 192, (1986).
- 79. E.B. Hryhorenko, "A Positive Approach to Resist Process Characterization for Linewidth Control", Eastman-Kodak, Rochester, N.Y., 1980.
- 80. J.D. Cuthbert, "Optical Projection Printing", Solid State Technology, p. 59, Aug. 1977.
- H. Yanzawa, et al, "Chemical Characterization of Photoresist to Silicon Adhesionin Integrated Circuit Technology", Kodak Interface Seminar, 1977.
- 82. J. J. Chisholm, "A New Linewidth Measurement on 1 μm Geometry Process Wafers Using Fluorescence", SPIE Proc. 480, Integrated Circuit Metrology, 1984, p. 49
- 83. "Flow-Monitors for Controlling Spin Bowl Exhausts", Sierra Instruments, Carmel, California
- D. Ditmer and M.V. Hanson, "Stepper Exposed Critical Dimension Tolerances Using a Vapor Jet Developer Nozzle", SPIE Proc. Optical Microlithography III, Vol. 470,1984, p. 203.
- J.C. Mathews and J. I. Wilmott, "Stabilization of Sinle Layer and Multilayer Resist Patterns to Al Etching Environments", SPIE Proc., Optical Lithography III, Vol. 470, 1984, p. 194.

PROBLEMS

- 1. Explain why a resist with higher contrast can lead to higher resolution of features transferred from a mask to the wafer surface than a resist with a lower contrast.
- 2. In examining Fig. 3, which of the positive resists exhibits (a) the highest contrast, and (b) the highest sensitivity. Determine this also for the negative resists shown in the figure.
- 3. Why is it important that a resist exhibits a high actinic absorbance?
- 4. Explain why a multi-layer resist process offers the potential of higher resolution than a single-layer resist process. What prices are paid for this benefit?
- 5. In a photoresist process it is important that the resist film thickness be highly uniform. List five or more parameters that impact the thickness of the resist film by the time it has been spun-on and soft-baked.
- 6. Explain how under-softbaking leads to an apparent increase in the photosensitivity of the resist. Why is not generally possible to utilize under-softbaking to exploit this effect?
- 7. Calculate the number of standing wave maxima that will be produced in a positive resist layer that is 1.0 µm thick, and has an index of refraction of 1.68 at the G-line of exposing radiation.
- 8. Explain how higher resolution is achieved by the use of (a) contrast enhancement layers, (b) anti-reflective coatings, and (c) incorporation of dyes in the resist. Cite the advantages and disadvantages of each of these methods.
- 9. Describe four techniques utilized to measure the linewidth of patterned features on a substrate. Why is accurate linewidth measurement more difficult on wafer surfaces than on the mask and reticle substrates?
- 10. Rounding of the resist profiles by elevated post-bake temperatures (Fig. 38) is sometimes used to produce a tapered profile in the etched feature (by anisotropically dry-etching the resist and the layer to be patterned at an equal etch rate). Why does this procedure become ineffective when the dimension of the etched feature approaches that of the resist film thickness?