

FILE HISTORY

60/071,628

INVENTORS: ALFRED GRILL
JOHN P. HUMMEL
CHRISTOPHER V. JAHES
VISHUNUBHAI V. PATEL
KATHERINE L. SAENGER

TITLE: DUAL DAMASCENE PROCESSING
FOR SEMICONDUCTOR CHIP
INTERCONNECTS

APPLICATION NO: 60/071,628

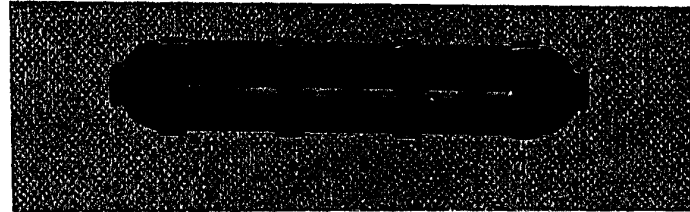
FILED: 16 JAN 1998

COMPILED: 29 JUL 2015



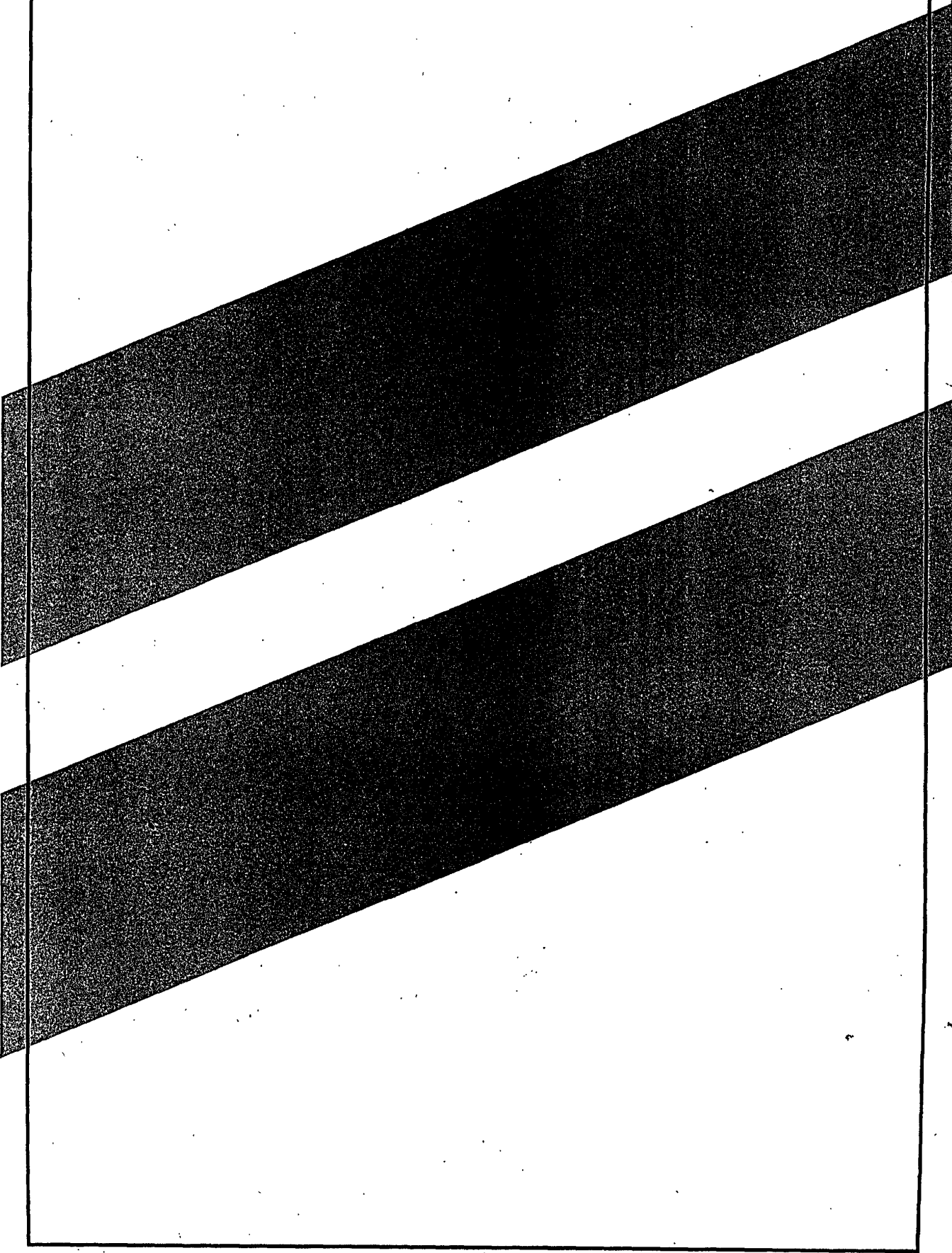
Class	Subclass
ISSUE CLASSIFICATION	

SCANNED 4



PROVISIONAL
APPLICATION
NUMBER

BEST COPY



Form PTO-1625
(Rev. 5/95)

SCANNED 4
QC

(FACE)

60/071,628

DUAL DAMASCENE PROCESSING FOR SEMICONDUCTOR CHIP
INTERCONNECTS

Transaction History

Date	Transaction Description
02-02-1998	Initial Exam Team nn
03-18-1998	IFW Scan & PACR Auto Security Review
03-23-1998	Preexamination Location Change
09-21-2001	Set Application Status

55
60/1131028
012/06/15

Date
Entered
or
Counted

PATENT APPLICATION



60071628

APPROVED FOR LICENSE

FEB 20 9 8 05

INITIALS

Date
Received
or
Mailed

CONTENTS

1.	Application	02/09/15
2.	Specification	2-27-15
3.	Claims	7-28-15
4.		
5.		
6.		
7.		
8.		
9.		
10.		
11.		
12.		
13.		
14.		
15.		
16.		
17.		
18.		
19.		
20.		
21.		
22.		
23.		
24.		
25.		
26.		
27.		
28.		
29.		
30.		
31.		
32.		

(FRONT)

POSITION		ID NO.	DATE
CLASSIFIER		45	2/20/98
EXAMINER		66080	3/20/98
TYPIST			
VERIFIER			
CORPS CORR.			
SPEC. HAND			
FILE MAINT			
DRAFTING			

(LEFT INSIDE)

SERIAL NUMBER		FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.	
60/071,628 PROVISIONAL		01/16/98		0000	YO997-130	
APPLICANT	ALFRED GRILL, WHITE PLAINS, NY; JOHN P. HUMMEL, MILLBROOK, NY; CHRISTOPHER V. JAHES, MONSEY, NY; VISHUNUBHAI V. PATEL, YORKTOWN HEIGHTS, NY; KATHERINE L. SAENGER, OSSINING, NK.					
	CONTINUING DOMESTIC DATA*** VERIFIED _____					
	371 (NAT'L STAGE) DATA*** VERIFIED _____					
	FOREIGN APPLICATIONS*** VERIFIED _____					
	FOREIGN FILING LICENSE GRANTED 03/20/98					
Foreign Priority claimed 35 USC 119 (a-d) conditions met		<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and Acknowledged		Examiner's Initials _____ Initials _____	NY	8		
ADDRESS	ROBERT M TREPP IMB CORPORATION INTELLECTUAL PROPERTY LAW DEPT P O BOX 218 YORKTOWN HEIGHTS NY 10598					
	DUAL DAMASCENE PROCESSING FOR SEMICONDUCTOR CHIP INTERCONNECTS					
TITLE						
FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:			<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		
\$150						

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

02/09/1998 PALLER 00000131 DAB:090468 60071628
01 FC:114 150.00 CH

PTO-1556
(5/87)

PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION under 37 CFR 1.53(b)(2).

DOCKET NUMBER		Y0997-130		Type a plus (+) inside this box		+	
INVENTOR(s)/APPLICANT(s)							
LAST NAME		FIRST NAME		MIDDLE INITIAL		RESIDENCE (City and either State or Foreign Country)	
Grill		Alfred		N/A		White Plains, New York 10605	
Hummel		John		P.		Millbrook, New York 12545	
Jahnes		Christopher		V.		Monsey, New York 10952	
Patel		Vishnubhai		V.		Yorktown Heights, New York 10598	
Saenger		Katherine		L.		Ossining, New York 10562	
TITLE OF THE INVENTION (280 characters max)							
Dual Damascene Processing for Semiconductor Chip Interconnects							
CORRESPONDENCE ADDRESS							
Robert M. Trepp; IBM Corporation; Intellectual Property Law Dept.; P.O. Box 218; Yorktown Heights, New York 10598							
STATE		New York		ZIP CODE		10598	
COUNTRY		USA					
ENCLOSED APPLICATION PARTS (check all that apply)							
<input checked="" type="checkbox"/> Specification		Number of Pages		10		<input type="checkbox"/> Small Entity Statement	
<input checked="" type="checkbox"/> Drawing(s)		Number of Sheets		8		<input type="checkbox"/> Other (specify) _____	
METHOD OF PAYMENT (check one)							
<input type="checkbox"/> A check or money order is enclosed to cover the Provisional filing fees				PROVISIONAL FILING FEE AMOUNT (\$)		\$150.00	
<input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge filing fees and credit Deposit Account Number 09-0468							

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

- ☒ No
- ☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE Robert M. Trepp Date: Jan 16, 1998

TYPED or PRINTED NAME Robert M. Trepp Registration No. 25,933

- ☐ Additional inventors are being named on separately numbered sheets attached hereto.

PROVISIONAL APPLICATION FILING ONLY

Express Mail Label: EM455587215US
Date of Deposit: January 16, 1998

A/PROV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

jc575 U.S. PTO
01/16/98

In re Provisional Application of:

ALFRED GRILL et al.

Serial No.: (to be assigned)

Group Art No:

Filed: herewith

Examiner:

For: Dual Damascene Processing for Semiconductor Chip Interconnects

Commissioner of Patents and Trademarks
Box Provisional Patent Application
Washington, D. C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EM455587215US

Date of Deposit January 16, 1998

I hereby certify that the following attached paper or fee

1. Acknowledgment Post Card;
2. Provisional Application Cover Sheet (in duplicate);
3. Provisional Application; and
4. Set of eight (8) Informal Drawings

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D. C. 20231.

ROBERT M TREPP

(Type or print name of person mailing paper or fee)

Robert M Trepp
(Signature of person mailing paper or fee)

NOTE: Each paper must have its own certificate and the "Express Mail" label number as a part thereof or attached thereto. When, as here, the certification is presented on a separate sheet, that sheet must (1) be signed and (2) fully identify and be securely attached to the paper or fee it accompanies. Identification should include the serial number and filing date of the application as well as the type of paper being filed, e.g. complete application, specification and drawings, responses to rejection or refusal, notice of appeal, etc. If the serial number of the application is not known, the identification should include at least the name of the inventor(s) and the title of the invention.

NOTE: The label number need not be placed on each page. It should, however, be placed on the first page of each separate document, such as, a new application, amendment, assignment, and transmittal letter for a fee, along with the certificate of mailing by "Express Mail." Although the label number may be on checks, such a practice is not required. In order not to deface formal drawings it is suggested that the label number be placed on the back of each formal drawing or the drawings be accompanied by a set of informal drawings on which the label number is placed.

DOCKET NO. YO997-130

Dual Damascene Processing for Semiconductor Chip Interconnects

Field of the Invention

- 5 The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips.

Background of the Invention

- 10 Device interconnections in Very Large Scale Integrated (VLSI) or Ultra-Large Scale Integrated (ULSI) semiconductor chips are typically effected by multilevel interconnect structures containing patterns of metal wiring layers called traces. Wiring structures within a given trace or level of wiring are separated by an intralevel dielectric, while the individual wiring levels are separated from each other by layers of an interlevel dielectric. Conductive vias are formed in the interlevel dielectric to provide interlevel contacts between the wiring traces.

- 15 By means of their effects on signal propagation delays, the materials and layout of these interconnect structures can substantially impact chip speed, and thus chip performance. Signal propagation delays are due to RC time constants wherein R is the resistance of the on-chip wiring, and C is the effective capacitance between the signal lines and the surrounding conductors in the multilevel interconnection stack. RC time constants are reduced by lowering the specific resistance of the wiring material, and by using interlevel and intralevel dielectrics with lower dielectric constants.

- 20 A preferred metal/dielectric combination for low RC interconnect structures might be Cu metal with a carbon-based dielectric such as diamond-like-carbon (DLC). Due to difficulties in subtractively patterning copper, however, interconnect structures containing copper are typically fabricated by a Damascene process. In a Damascene process, metal patterns inset in a layer of dielectric are formed by the steps of

- 25 etching holes (for vias) or trenches (for wiring) into the interlevel or intralevel dielectric,

optionally lining the holes or trenches with one or more adhesion or diffusion barrier layers,

overfilling said holes and trenches with a conductive wiring material, by a process such as physical vapor deposition (for example, sputtering or evaporation), chemical vapor deposition, or plating, and

- 30 removing the metal overfill by planarizing the metal to be even with the upper surface of the dielectric.

This process is repeated until the desired number of wiring and via levels have been fabricated.

- 35 Fabrication of interconnect structures by Damascene processing can be substantially simplified by using a process variation known as Dual Damascene, in which a wiring level and its underlying via level are filled in with metal in the same deposition step. However, fabrication by this route requires transferring two patterns to one or more layers of dielectric in a single block of lithography and/or etching steps. This has previously been accomplished by using a layer of masking material that is patterned twice, the first time with a via pattern and the second time with a wiring pattern. This procedure typically comprises the steps of:

- 40 forming one or more layers of dielectric having a total thickness equal to the sum of the via level and wiring level thicknesses,

applying a layer of a hard mask material such as SiO₂ or Si₃N₄ having different etch characteristics than the underlying dielectric,

patterning the hard mask material with the via level pattern, typically by etching through a photoresist stencil,

- 5 transferring said via level pattern into a first upper thickness of said one or more layers of dielectric by a process such as etching,

repatterning the same layer of hard mask material with the wiring level pattern,

- transferring the wiring level pattern into a second upper thickness of said one or more layers of dielectric in such a manner as to simultaneously transfer the previously etched via pattern to a bottom thickness of said one or more layers of dielectric, said second upper and bottom thicknesses closely approximating the wiring and via level thicknesses, respectively.
- 10

- While this "twice patterned single mask layer" process has the virtue of simplicity, difficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics. Such would be the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC. A typical cause for rework would be a misalignment between the via-patterned hard mask/upper dielectric layers and the wiring-patterned resist layer. However, lithographic rework at this stage is a problem because the sidewalls of the via-patterned dielectric are not protected from the resist stripping steps necessary for removing a misaligned wiring-patterned resist layer.
- 15

20 Summary of the Invention

- The present invention relates to improved methods for defining and transferring two patterns (or a single dual relief pattern) to one or more layers of dielectric in a single block of lithography and/or etching steps. The invention comprises two preferred modifications of a prior art "twice patterned single mask layer" Dual Damascene process and two preferred embodiments of a fabrication process for a dual pattern hard mask which may be used to form dual relief cavities for Dual Damascene applications.
- 25

- The first and second preferred modifications of a prior art "twice patterned single mask layer" process introduce an easy-to-integrate sidewall liner which protects organic interlevel and intralevel dielectrics from potential damage induced by photoresist stripping steps which may be needed, for example, during rework processing to correct for lithographic misalignment. In the first modification, the liner may be permanent, in which case portions of the liner can remain in the final structure. In the second modification, the liner may be disposable, in which case the liner would be removed from the finished structure. Use of these inventive modifications allows problem-free rework with minimal impact on processing.
- 30

- The two preferred embodiments of a dual pattern hard mask fabrication process provide a mask wherein the lithographic alignment for both via and wiring levels is completed before any pattern transfer into the underlying interlevel/intralevel dielectric. The dual pattern hard mask might preferably comprise a bottom layer of silicon nitride with a first pattern and a top layer of SiO₂ with a second pattern. The two embodiments differ by the order in which said first and second patterns are transferred into the hard mask layers.
- 35
- 40

It is thus an object of the present invention to improve the existing "twice patterned single mask layer" Dual Damascene process by adding a protective sidewall liner which may or may not remain in the final structure.

It is a further object of the present invention to teach the use of a Dual Damascene process in which a dual pattern hard mask containing both via and wiring level patterns is fabricated on a substrate comprising at least one layer of an interlevel/intralevel dielectric, prior to any pattern transfer into the interlevel/intralevel dielectric.

- 5 It is a further object of the present invention to provide a general method for forming a dual pattern hard mask, said dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a second set of one or more layers with a second pattern.

- 10 It is a further object of the present invention to teach a method for transferring said first and second patterns of said dual pattern hard mask to an underlying substrate to form a dual relief patterned structure.

Brief Description of the Drawings

These and other features, objects, and advantages of the present invention will become apparent upon a consideration of the following detailed description of the invention when read in conjunction with the drawings, in which:

- 15 Figs. 1A - 1L show in cross section view the prior art "twice patterned single mask layer" Dual Damascene process flow for forming a wiring layer and its associated underlying via layer;

Figs. 2A - 2D show in cross section view an exaggeration of the rework problem that may be encountered with the process flow of Fig. 1;

Figs. 3A - 3G show in cross section view a first preferred modification of the Fig. 1 process;

- 20 Figs. 4A - 4F show in cross section view a second preferred modification of the Fig. 1 process;

Figs. 5A - 5H illustrate in cross section view a Dual Damascene process flow utilizing a first preferred embodiment of the disclosed dual pattern hard mask;

Figs. 6A - 6J illustrate in cross section view a Dual Damascene process flow utilizing a trilayer variation of a first preferred embodiment of the disclosed dual pattern hard mask;

- 25 Figs. 7A - 7I illustrate in cross section view a Dual Damascene process flow utilizing a second preferred embodiment of the disclosed dual pattern hard mask; and

Fig. 8A - 8D illustrate in cross section view a three pattern hard mask, and some associated materials issues.

Description of the Preferred Embodiments

- 30 Figs. 1A - 1L show in cross section view a prior art "twice patterned single mask layer" Dual Damascene process flow for forming a wiring layer and its underlying via layer. The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown), conductive via 4, and dielectric passivation layer 6.

- 35 A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a via level dielectric 8, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. Via and wiring dielectrics 8 and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 might be a material such as SiO₂, Si₃N₄, silicon-containing DLC (SiDLC), etc. The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thicknesses.
- 40

For a description of DLC, reference is made to US Patent No. 5,xxx,xxx; for a description of FDLC reference is made to US Patents No. 5,xxx,xxx and 5,xxx,xxx; for a description of SiDLC, reference is made to US Patent No. 5,xxx,xxx.

5 A hard mask layer 14, formed from a material such as SiO₂ or Si₃N₄ having different etch characteristics from the underlying dielectric 12, is then applied to produce the structure of Fig. 1C. A resist layer 16 patterned with a first pattern is then formed on hard mask 14, as shown in Fig. 1D. The first pattern in patterned resist layer 16 would typically be a via level pattern. If resist layer 16 is for some reason misaligned with respect to underlying structures such as via 4, resist layer 16 may be removed by a process such as ashing without damaging underlying dielectric 12, since
10 dielectric 12 is still protected by hard mask 14. Resist 16 is then reapplied and patterned until the desired alignment is achieved. Hard mask layer 14 is then patterned with said first pattern by etching through the openings in patterned resist layer 16, as shown in Fig. 1E. Said first pattern is then transferred into the entire thickness of dielectric 12 by an etching process such as reactive ion etching (RIE), as shown in Fig. 1F.

15 A resist layer 18 patterned with a second pattern is then formed on the structure of Fig. 1F to produce the structure of Fig. 1G. Said second pattern in patterned resist layer 18 would typically be a wiring level pattern. Hard mask layer 14 is then patterned with said second pattern by etching through the openings in pattern resist layer 18, as shown in Fig. 1H. Exposed regions of optional dielectric etch stop 10 would typically also be removed during this etching step, as well. Dielectrics
20 8 and 12 are then etched to transfer the second pattern into the entire thickness of dielectric 12, and the first pattern into the entire thickness of dielectric 8, as shown in Fig. 1I. Exposed regions of optional dielectrics 10 and 7 are then removed to produce the structure of Fig. 1J containing dual relief cavity 20. Cavity 20 is optionally lined with one or more adhesion or diffusion barrier layers (not shown) and then overfilled with conductive wiring material 22, by a process such as physical
25 vapor deposition, chemical vapor deposition, solution deposition, or plating to produce the structure of Fig. 1K. Conductive wiring material 22 is then planarized by a process such as chemical mechanical polishing (CMP) to be approximately even with the top surface of dielectric 12 and/or remaining hard mask 14. Remaining hard mask 14 is then optionally removed to produce the structure of Fig. 1L. Additional wiring/via levels may be fabricated by repeating the steps shown in
30 Figs. 1B - 1L.

Figs. 2A - 2D show in cross section view an exaggeration of the rework problem that may be encountered with the process flow of Figs. 1B - 1L if resist 18 of Fig. 1G is misaligned. Fig. 2A shows the structure of Fig. 1F after application of resist 26. Fig. 2B shows the structure of Fig. 2A after resist layer 26 has been patterned with said second pattern to produce misaligned patterned
35 resist layer 28. Fig. 2C shows the structure of Fig. 2B after an ashing process to remove misaligned patterned resist layer 28. Sidewalls 30 of dielectric 12 are clearly undercut. Such a result may not be a problem when the dimensions of said second pattern substantially exceed the dimensions of the first pattern, since the undercut regions would be etched anyway. However, it will be a problem for cases in which the dimensions of the first and second patterns are similar, as shown in Fig. 2D,
40 since the undercut sidewall profile will persist in the final structure. Such undercutting makes critical dimension control more difficult and produces cavities that are more difficult to line with a conductive liner and fill with a conductive wiring material 22.

Figs. 3A - 3G show a first preferred modification of the Figs. 1A - 1L "twice patterned single mask layer" process described above, in cross section view. The process of Figs. 3A - 3G differs
45 from that of Figs. 1A - 1L by the addition of a sidewall liner which may remain in the final structure. In addition, the first and second patterns to be transferred are the wiring and via patterns in the process of Figs. 3A - 3G, as opposed to the via and wiring patterns in the process of Figs. 1A - 1L.

Fig. 3A shows the structure of Fig. 1C after application of an overlayer of resist 34 analogous
50 to resist layer 16, but patterned with a wiring level pattern. Hard mask layer 14 is then patterned

with the wiring pattern of resist layer 34, to produce the structure of Fig. 3B. The wiring pattern of resist layer 34 is then transferred to dielectric layer 12, and preferably to dielectric etch stop layer 10 as well, to form cavity 36 in Fig. 3C. A thin layer of conductive or insulating liner material 38 that may also be used as a hard mask is then conformally deposited over the topography of Fig. 3C to form the lined cavity 40 shown in Fig. 3D. Possible hard mask/liner materials for hard mask/liner material 38 include conductive barrier materials such as Ta, Cr, or TaN, semiconductors such as amorphous hydrogenated silicon (a-Si:H), and insulators such as SiO₂, and Si₃N₄. Hard mask/liner material 38 is preferably conducting if any of it is to be left in the final structure.

Fig. 3E shows the structure of Fig. 3D after application of an overlayer of resist 42 patterned with a via level pattern. In the event patterned resist 42 is misaligned, patterned resist 42 may be removed by a process such as ashing without damaging the sidewalls of dielectric layer 12 or the top surface of dielectric layer 8. The steps of applying an overlayer of resist 42 and patterning resist 42 may be repeated until patterned resist 42 is properly aligned. The pattern of resist layer 42 is then transferred to hard mask/liner layer 38, to produce the structure of Fig. 3F, and then transferred further to dielectric layers 8 and 7 to produce the dual relief cavity 44 in Fig. 3G. After optional removal (not shown) of some or all of patterned hard mask/liner 38 by a process such as selective etching, the structure is overfilled with a conductive material and planarized, as shown in Figs. 1K - 1L. Any portions of hard mask/liner 38 remaining above dielectric 12 after the final polishing step are preferably removed before fabrication of any overlying wiring or via levels.

Figs. 4A - 4F show a second preferred modification of the Fig. 1A - 1L "twice patterned single mask layer" process, in cross section view. The process of Figs. 4A - 4F differs from that of Figs. 1A - 1L by the addition of a disposable sidewall coating which is removed from the structure at an intermediate stage in processing. However, it is similar to the prior art Figs. 1A - 1L process in that a single hard mask layer is patterned twice, first with a via pattern and then with a wiring pattern.

Fig. 4A shows the structure of Fig. 1F after application of thin disposable liner 46 conformally deposited over the topography of Fig. 1F to form lined cavity 50. Liner 46 may be conductive or insulating, and is preferably selected from the group of materials resistant to the oxygen ashing of the resist stripping process, and preferably has a thickness between 1 and 50 nm. Possible liner materials include Ta, Cr, or TaN, amorphous hydrogenated silicon (a-Si:H), SiO₂, and Si₃N₄. Resist layer 18 patterned with a wiring level pattern is then formed on the structure of Fig. 4A. If resist layer 18 must be reworked, liner 46 will protect dielectric 12 from damage during processing.

If alignment of resist layer 18 with the via level pattern is satisfactory, the wiring level pattern is then transferred into disposable liner 46 and hard mask 14 to form the structure of Fig. 4C with disposable liner sidewalls 52. The wiring pattern of hard mask 14 is then transferred into dielectric layers 12 and 10 while the via pattern in dielectric 12 is transferred into dielectrics 8 and 7. If sidewall liner 52 is still present after these etching steps, it is removed by selective etching to produce the structure of Fig. 4D containing cavity 54 which is overfilled with conductive material 22 and planarized as shown in Figs. 1K - 1L.

A satisfactory approximation to the structure of Fig. 4C may be formed from the structure of Fig. 1F by etching exposed etch stop 10 in such a manner as to redeposit etch stop material to form sidewall liners 52, as illustrated in Fig. 4E. A preferred resputtering process to form sidewall liners 52 would be ion beam sputtering or low pressure, high bias voltage RIE.

Alternatively, the structure of Fig. 4F might be formed by the selective deposition of a liner material 55 on the sidewalls of dielectric 12 or on both the sidewalls of dielectric 12 and the exposed top surface of dielectric etch stop 10.

Dual pattern hard masks may comprise a first layer of a first material with a first pattern and a second layer of a second material with a second pattern. More generally, a dual pattern hard mask may comprise a first set of one or more layers with a first pattern, and a second set of one or more

layers with a second pattern, materials of said first and second sets of layers selected respectively from a first group of materials and a second group of materials.

5 Figs. 5A - 5E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of a first material with a first pattern, and a second layer of a second material with a second pattern; Figs. 5F - 5H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a wiring level pattern. However, the via and wiring level patterns should be viewed as special cases of the general category of dual relief patterns in which all features of a smaller area (via) pattern completely fit within the features of a larger area (wiring) pattern.

10 Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58. Hard mask layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8. For example, lower hard mask layer 56 might be formed from Si₃N₄ and upper hard mask layer 15 58 might be formed from SiO₂. Other suitable hard mask materials may include SiO₂-based materials, other oxides, nitrides other than Si₃N₄, carbon-based dielectrics, and polycrystalline silicon, and amorphous hydrogenated silicon. A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58 to form the structure of Fig. 5B. If resist layer 60 is misaligned, rework at this stage presents no problem. The pattern of resist layer 60 is transferred into upper hard mask layer 58 by an etching process to form the structure of Fig. 5C. The etching process is preferably selective, for example a selective SiO₂ to Si₃N₄ etch, so that lower hard mask layer 56 will remain intact during any overetching of hard mask layer 58.

20 A second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D. Again, resist rework at this stage presents no problem because lower hard mask layer 56 is still in place to protect dielectric 12. The pattern of resist layer 62 is then transferred into lower hard mask layer 56. Fig. 5E shows the completed dual pattern hard mask, comprising patterned hard mask layers 56 and 58, with patterned resist layer 62 still in place.

25 The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of Fig. 5F. The etching conditions are then changed to removed exposed portions of lower hard mask layer 56 and optional etch stop 10, to form the structure of Fig. 5G. Dielectrics 8 and 12 are then etched to transfer said second pattern into the entire thickness of dielectric 12, and said first pattern into the entire thickness of dielectric 8, as shown in Fig. 5H. The cavity structure may then be completed as shown in Fig. 1J, and, for 30 interconnect applications, filled with wiring material 22 as shown in Figs. 1K to 1L.

35 Figs. 6A - 6F show a trilayer variation of the Fig. 5 method for forming a dual pattern hard mask; Figs. 6G - 6J show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. This trilayer variation may be preferable to the Fig. 5 dual layer dual pattern hard mask because it provides a resist-free dual pattern hard mask prior to any pattern transfer into the substrate. This can be desirable when resist loading is a concern, or if the resist thickness has to be thinned to allow its removal to coincide with the endpoint of the cavity patterning process.

40 Fig. 6A shows the structure of Fig. 1B after application of lower hard mask layer 66, middle hard mask layer 68, and upper hard mask layer 70. Hard mask layers 66, 68, and 70 are preferably formed from materials having different etch properties than dielectric underlayers 12 and 8. Hard mask layers 66 and 70 may be formed from the same material, but preferably one different from that of hard mask layer 68. For example, lower hard mask layer 66 might be formed from a 20 nm thickness of Si₃N₄, middle hard mask layer 68 might be formed from a 50 nm thickness of SiO₂, and upper hard mask layer 70 might be formed from a 40 nm thickness of SiO₂. Other suitable

hard mask materials may include SiO₂-based materials, other oxides, nitrides other than Si₃N₄, carbon-based dielectrics, and polycrystalline silicon, and amorphous hydrogenated silicon.

- 5 A first resist layer 72, patterned with a first (wiring level) pattern, is formed on layer 70 to form the structure of Fig. 6B. If resist layer 72 is misaligned, rework at this stage presents no problem. The pattern of resist layer 72 is transferred into upper hard mask layer 70 by an etching process. Said etching process might preferably be selective with respect to hard mask layer 68, but it may be nonselective as well. Patterned resist layer 72 is then removed by a process such as ashing to form the structure of Fig. 6C.

- 10 A second resist layer 74, patterned with a second (via level) pattern, is then formed on the structure of Fig. 6C to produce the structure of Fig. 6D. Again, resist rework at this stage presents no problem. The pattern of resist layer 74 is then transferred into middle hard mask layer 68 by an etching process. Said etching process is preferably selective with respect to hard mask layer 66, for example, a selective oxide to nitride etch for the preferred hard mask layer materials cited above. Patterned resist layer 74 is then removed by a process such as ashing to form the structure of Fig. 6E. The via pattern of patterned hard mask layer 68 is then transferred to bottom hard mask layer 66 by an etching process that may be selective or nonselective to produce the completed, resist-free trilayer dual pattern hard mask of Fig. 6F, comprising patterned hard mask layers 66, 68, and 70.

- 20 The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of Fig. 6G. The etching conditions are then changed to removed exposed portions of middle hard mask layer 68 and optional etch stop 10, to form the structure of Fig. 6H with wiring level pattern contained in middle and top hard mask layers 68 and 70. The wiring level pattern is then transferred into bottom hard mask layer 66 by an etching process that would typically also remove the exposed portions of hard mask 70, to produce the structure of Fig. 6I. Dielectrics 8 and 12 are then etched to transfer said second (wiring level) pattern into the entire thickness of dielectric 12, and said first (via level) pattern into the entire thickness of dielectric 8, as shown in Fig. 6J. The cavity structure may then be completed as shown in Fig. 1J, and, for interconnect applications, filled with wiring material as shown in Figs. 1K to 1L.

- 30 Figs. 7A - 7E show a second preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of a first material with a first pattern, and a second layer of a second material with a second pattern; and Figs. 7F - 7I show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. The main difference between the second embodiment of Fig. 7A - 7I and the first embodiment of Fig. 5A - 5H is the order in which the via and wiring level patterns are transferred into the two layers of the dual pattern hard mask.

- 35 Fig. 7A shows the structure of Fig. 1B after application of lower hard mask layer 76 and upper hard mask layer 78. Hard mask layers 76 and 78 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8. For example, lower hard mask layer 76 might be formed from Si₃N₄ and upper hard mask layer 78 might be formed from SiO₂. A first resist layer 80, patterned with a via level pattern, is formed on layer 78 to form the structure of Fig. 7B. If resist layer 80 is misaligned, rework at this stage presents no problem. The pattern of resist layer 80 is transferred into upper hard mask layer 78 by an etching process to form the structure of Fig. 7C. Said etching process is preferably selective, for example a selective SiO₂ to Si₃N₄ etch, to insure that lower hard mask layer 76 will remain intact during any overetching of hard mask layer 78.

- 45 A second resist layer 82, patterned with a wiring level pattern, is then formed on the structure of Fig. 7C to produce the structure of Fig. 7D. Again, resist rework at this stage presents no problem because lower hard mask layer 76 is still in place to protect dielectric 12. The wiring pattern of resist layer 82 is then at least partially transferred into upper hard mask layer 78 while simultaneously transferring the via pattern in upper mask layer 78 to lower hard mask layer 76, to form

the structure of Fig. 7E. The etching process is preferably accomplished by a nonselective oxide/nitride etch. The wiring pattern is then transferred into the entire thickness of upper hard mask layer 78 by an etching process. Again, the etch of upper hard mask layer is preferably selective with respect to the lower hard mask layer, to insure that lower hard mask layer 76 will remain intact during any overetching of hard mask layer 78. Fig. 7F shows the completed dual pattern hard mask, comprising patterned hard mask layers 76 and 78, with patterned resist layer 82 still in place.

The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to form the structure of Fig. 7G. The etching conditions are then changed to removed exposed portions of lower hard mask layer 76 and optional etch stop 10, to form the structure of Fig. 7H. Dielectrics 8 and 12 are then etched to transfer the second pattern into the entire thickness of dielectric 12, and the first pattern into the entire thickness of dielectric 8, as shown in Fig. 7I. The cavity structure may then be completed as shown in Fig. 1J, and, for interconnect applications, may be filled with wiring material 22 as shown in Figs. 1K to 1L.

It should be noted that the dual pattern hard masks of Figs. 6F and 7F are actually special cases of multiple pattern hard masks comprising two or more overlaid patterns. Fig. 8A shows an example of a three pattern hard mask 90 on patternable substrate 94. Three pattern mask 90 comprises a first layer 96 with a first pattern, a second layer 98 with a second pattern, and a third layer 100 with a third pattern. The patterned hard mask layers 96, 98, and 100 are preferably formed from different materials that may be selectively etched with respect to one another. Such a materials choice allows controlled removal of each patterned mask layer after its pattern has been transferred to the substrate. This is illustrated in Figs. 8B - 8D, starting with Fig. 8B which shows three pattern mask 90 after the pattern of layer 96 has been transferred to the substrate, but before the exposed portion of hard mask layer 96 has been removed to allow transfer of the next hard mask layer pattern 98 into the substrate. When hard mask layer 96 is selectively etchable with respect to hard mask layers 98 and 100, hard mask layers 98 and 100 retain their original thicknesses when exposed portions of hard mask layer 96 are removed, as shown in Fig. 8C. However, when hard mask layer 96 is not selectively etchable with respect to hard mask layers 98 and 100, hard mask layers 98 and 100 may be substantially thinned when exposed portions of hard mask layer 96 are removed, as shown in Fig. 8D. This may be tolerable with careful selection of the individual hard mask layer thicknesses, but it makes process control more difficult. SiO₂, Si₃N₄, and polycrystalline silicon comprise one set of three selectively etchable materials that might be suitable for patterned hard mask layers 96, 98, and 100.

While there has been described and illustrated

two modifications of a prior art "twice patterned single mask layer" Dual Damascene process, and two embodiments of a process for forming a dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a second set of one or more layers with a second pattern,

it will be apparent to those skilled in the art that further modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

40 Claims

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

Claim 1. A dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a second set of one or more layers with a second pattern.

Claim 2. The dual pattern hard mask of claim 1 wherein layer materials of said first set of layers are selected from the group of materials containing SiO₂, SiO₂-based materials, other oxides,

Si₃N₄, other nitrides, carbon-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.

- 5 Claim 3. The dual pattern hard mask of claim 1 wherein layer materials of said second set of layers are selected from the group of materials containing SiO₂, SiO₂-based materials, other oxides, Si₃N₄, other nitrides, carbon-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.

Claim 4. A method for forming the dual pattern hard mask of claim 1 comprising the steps of Fig. 5 method.

- 10 Claim 5. A method for forming the dual pattern hard mask of claim 1 comprising the steps of Fig. 6 method.

Claim 6. A method for forming the dual pattern hard mask of claim 1 comprising the steps of Fig. 7 method.

Claim 7. A method for forming a pattern of dual relief depressions in a substrate, at least one step of said method comprising etching said substrate through the dual pattern hard mask of claim 1.

- 15 Claim 8. A method for forming dual relief cavities in a substrate, at least one step of said method comprising etching said substrate through the dual pattern hard mask of claim 1.

Claim 9: A method for forming dual relief cavities in a substrate, said method comprising the steps of

forming the dual pattern hard mask of claim 1,

- 20 transferring said first pattern of said dual pattern hard mask into a first upper thickness of said substrate by a process such as etching,

removing said first pattern from said dual pattern hard mask to leave a modified hard mask, said modified hard mask comprising one or more hard mask layers with said second pattern,

- 25 transferring said second pattern of said modified hard mask into a second upper thickness of said substrate by a process such as etching, in such a manner as to simultaneously transfer the previously transferred first pattern to a bottom thickness of said substrate, sum of said second upper and bottom thicknesses closely approximating a desired total depth of said dual relief cavity,

optionally removing some or all of the remaining hard mask.

- 30 Claim 10. A method for forming a dual relief pattern of conductive material embedded in a layered dielectric stack, said dual relief pattern comprising overlaid first and second patterns of conductive material, said layered dielectric stack comprising one or more layers of dielectric material having a total thickness closely approximating the summed thicknesses of said first and second patterns of conductive material, said method comprising the steps of

depositing said layered dielectric stack,

- 35 forming dual relief cavities in said layered dielectric stack by the method of claim 9, wherein said substrate of claim 9 comprises said layered dielectric stack, said dual relief cavities closely approximating the desired dimensions of said first and second patterns of conductive material,

optionally lining said dual relief cavities with diffusion barrier or adhesion layers,
overfilling said dual relief cavities with a conductive material, and
planarizing said conductive material.

5 Claim 11. A multilevel interconnect structure containing at least one wiring/via level pair fabricated by the method of Claim 10.

Claim 12. A method for forming a multilevel interconnect structure comprising the steps of
standard twice patterned single mask layer
further comprising the steps of
forming a disposable liner (a la Fig. 4).

10 Claim 13. The method of claim 12 further including the step of selecting a liner material from the group of materials including refractory metals such as Ta and Cr, conductive nitrides such as TaN, silicon materials such as polycrystalline silicon or amorphous hydrogenated silicon, SiO₂, SiO₂-based materials, Si₃N₄, and other nitrides.

15 Claim 14. A multilevel interconnect structure containing at least one wiring/via level pair fabricated by the method of Claim 12.

Claim 15. A method for forming a multilevel interconnect structure comprising the steps of
standard twice patterned single mask layer
further comprising the steps of
forming a permanent liner (a la Fig. 3).

20 Claim 16. The method of claim 15 further including the step of selecting a liner material from the group of materials including refractory metals such as Ta and Cr, conductive nitrides such as TaN, silicon materials such as polycrystalline silicon or amorphous hydrogenated silicon, SiO₂, SiO₂-based materials, Si₃N₄, and other nitrides.

25 Claim 17. A multilevel interconnect structure containing at least one wiring/via level pair fabricated by the method of Claim 15.

Abstract

30 The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels. The invention comprises a twice patterned single mask layer Dual Damascene process modified by the addition of an easy-to-integrate sidewall liner to protect organic interlevel and intralevel dielectrics from potential damage induced by photoresist stripping steps during lithographic rework. The invention further comprises a method for forming a dual pattern hard mask which may be used to form dual
35 relief cavities for use in Dual Damascene processing, said dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a second set of one or more layers with a second pattern.

SHEET 1 OF 8
A. GRILL ET AL.
RMT YO997¹³⁰

PRIOR ART

FIG 1A

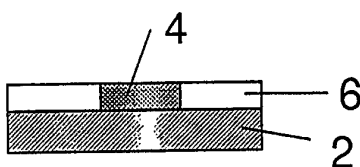


FIG 1B

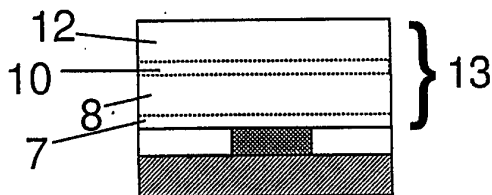


FIG 1C

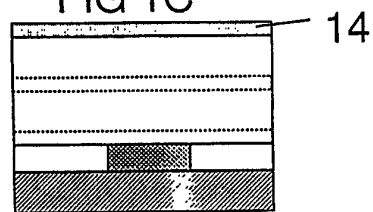


FIG 1D

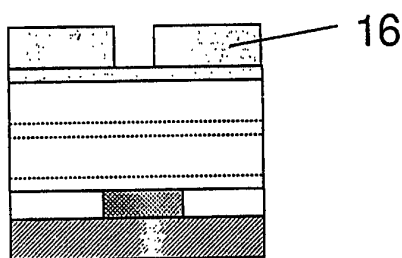


FIG 1E

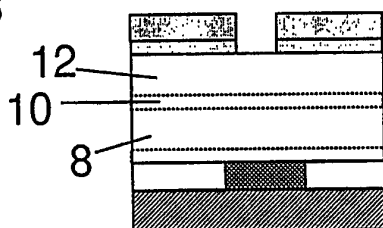


FIG 1F

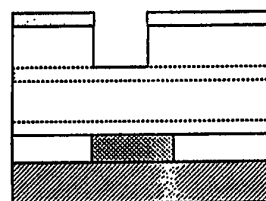


FIG 1G

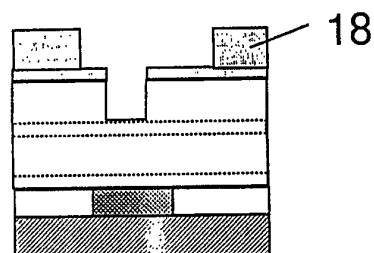


FIG 1H

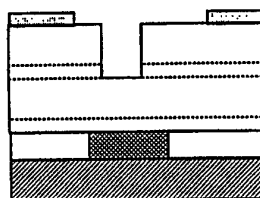


FIG 1I

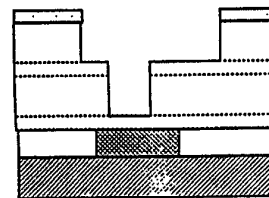


FIG 1J

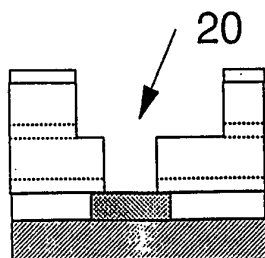


FIG 1K

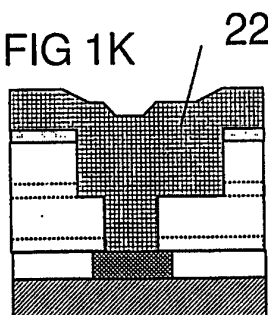


FIG 1L

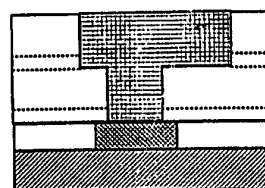


FIG 3A

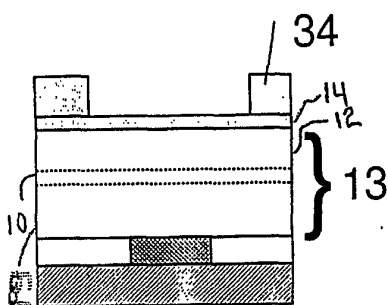


FIG 3B

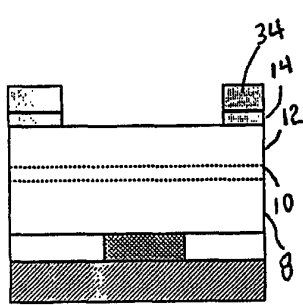


FIG 3C

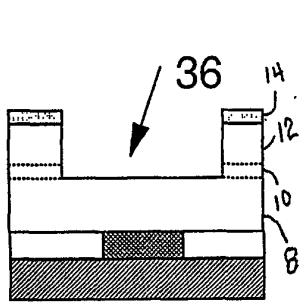


FIG 3D

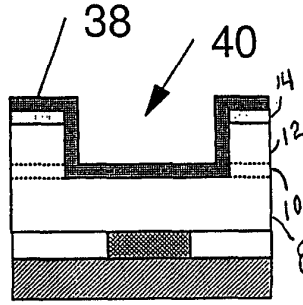


FIG 3E

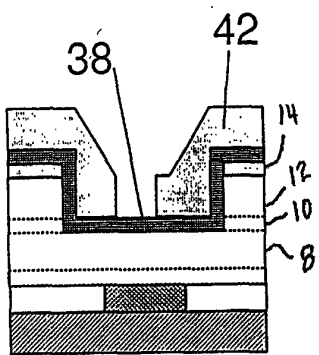


FIG 3F

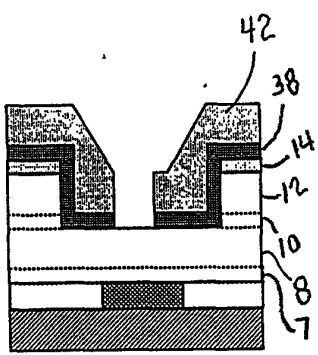


FIG 3G

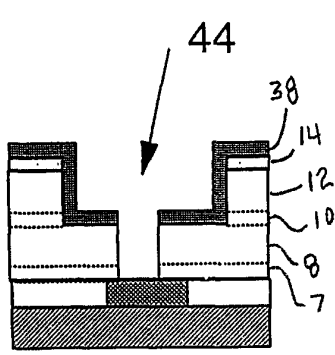


FIG 2A

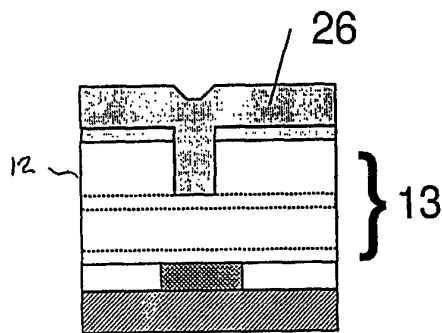


FIG 2B

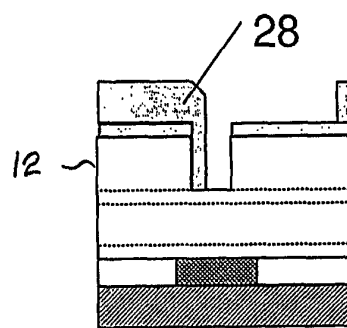


FIG 2C

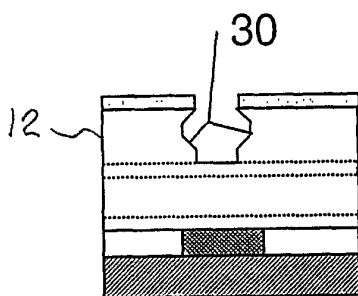
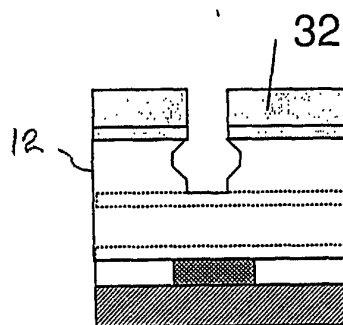


FIG 2D



2007-03-20

FIG 4A

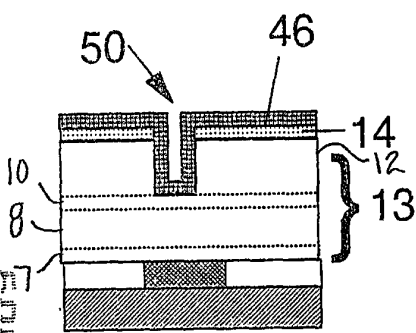


FIG 4B

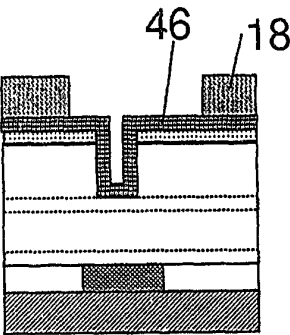


FIG 4C

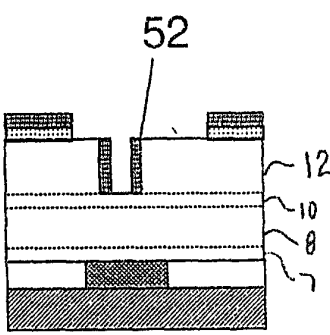


FIG 4D

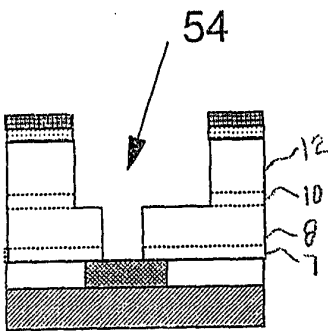


FIG 4E

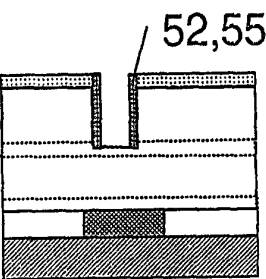


FIG 4F

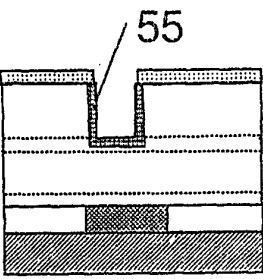


FIG 5A

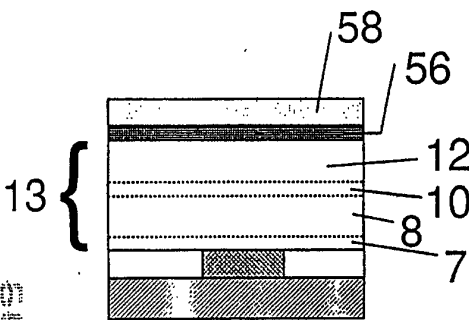


FIG 5B

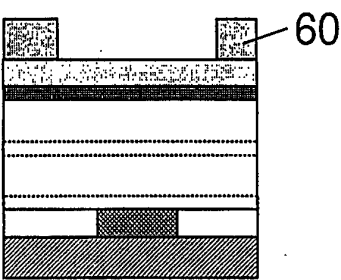


FIG 5C

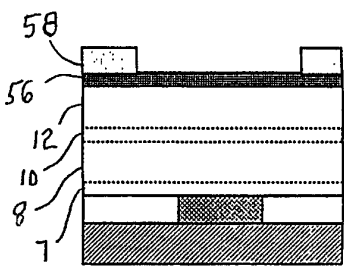


FIG 5D

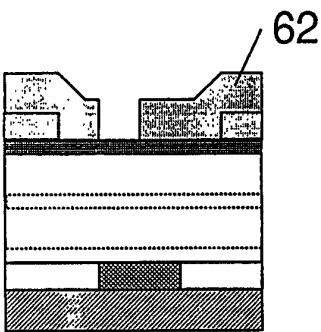


FIG 5E

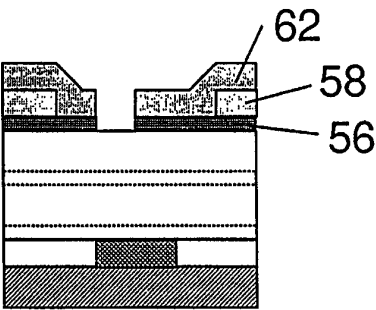


FIG 5F

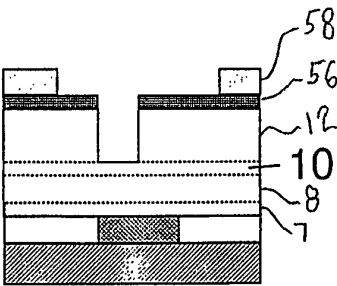


FIG 5G

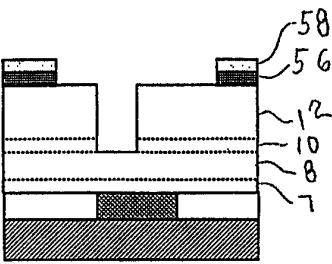


FIG 5H

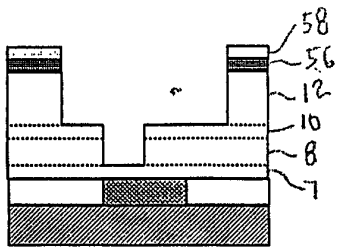


FIG 6A

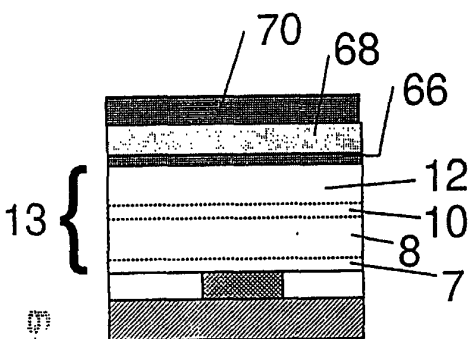


FIG 6B

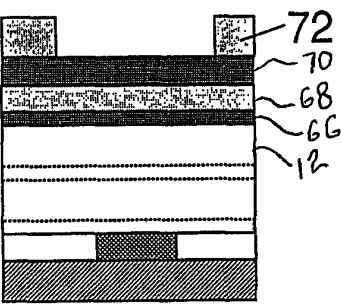


FIG 6C

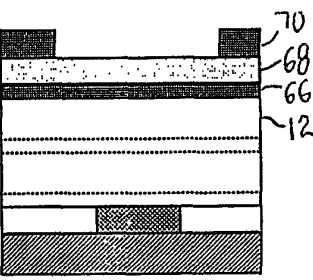


FIG 6D

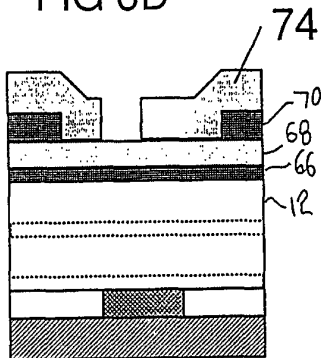


FIG 6E

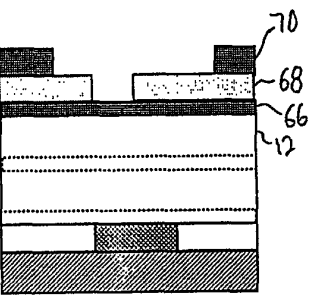


FIG 6F

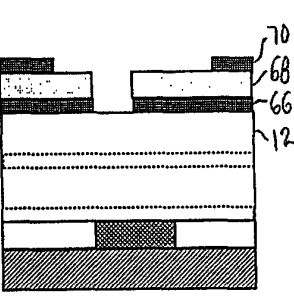


FIG 6G

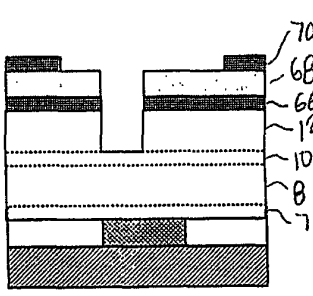


FIG 6H

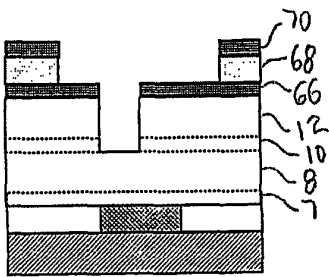


FIG 6I

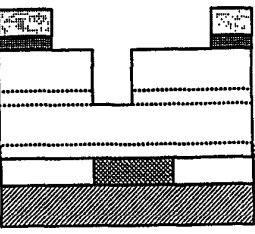


FIG 6J

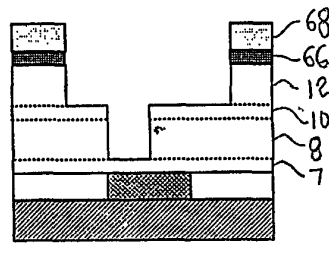


FIG 7A

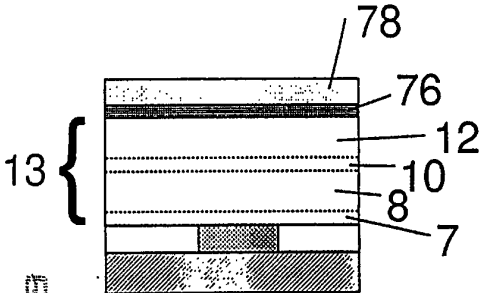


FIG 7B

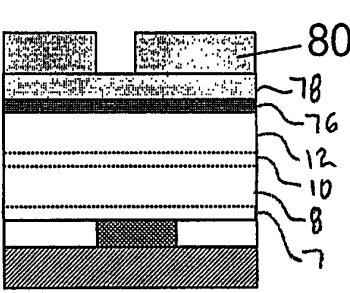


FIG 7C

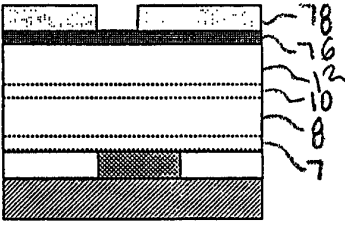


FIG 7D

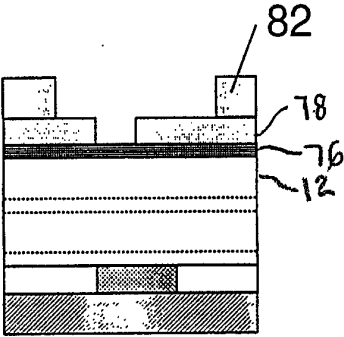


FIG 7E

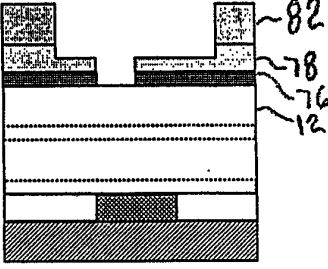


FIG 7F

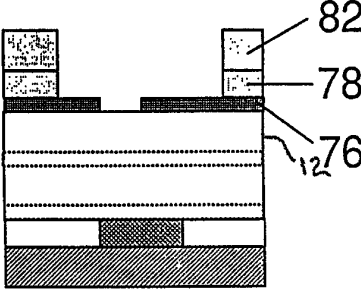


FIG 7G

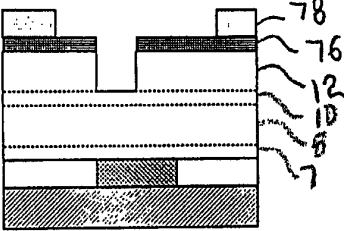


FIG 7H

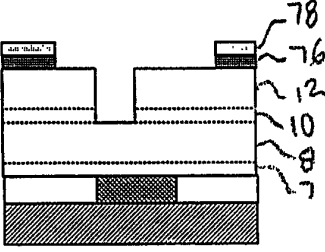


FIG 7I

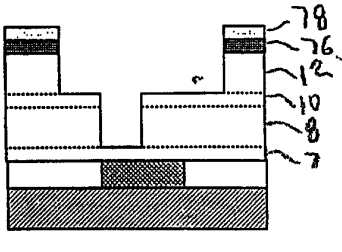


FIG 8A

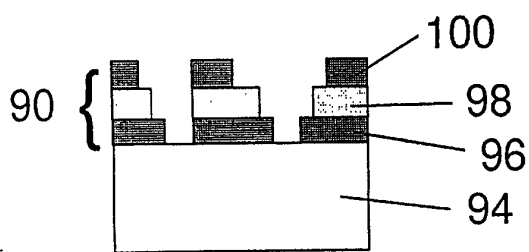


FIG 8B

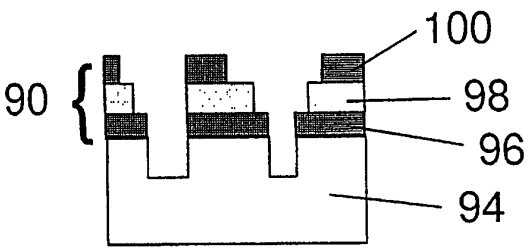


FIG 8C

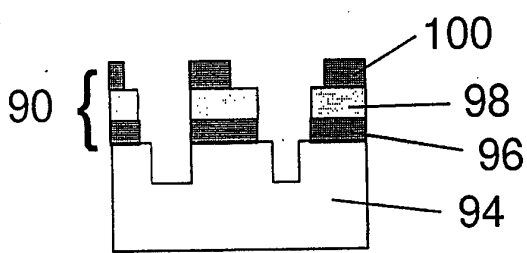
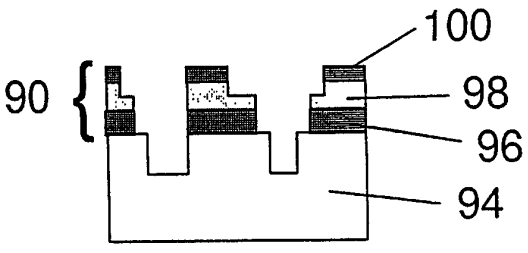


FIG 8D



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR ACCESS TO AN ABANDONED APPLICATION UNDER 37 CFR 1.14

Bring completed form to:
File Information Unit, Suite 3A20
2800 South Randolph Street
Arlington, VA 22206

Telephone: (703) 756-1800

In re Application of

RECEIVED
FEB 27 2015

Application Number

Filed

00/071,628

1/16/98

Paper No.

#2

BY: I hereby request access under 37 CFR 1.14(a)(1)(iv) to the application file record of the above-identified ABANDONED application, which is not within the file jacket of a pending Continued Prosecution Application (CPA) (37 CFR 1.53(d)) and which is identified in, or to which a benefit is claimed, in the following document (as shown in the attachment):

United States Patent Application Publication No. _____, page, _____ line _____.

United States Patent Number 6448176, column _____, line, _____.

WIPO Pub. No. _____, page _____, line _____.

Related Information About Access to Applications Maintained in the Image File Wrapper System (IFW) and Access to Pending Applications in General

A member of the public, acting without a power to inspect, cannot order applications maintained in the IFW system through the FIU. If the member of the public is entitled to a copy of the application file, then the file is made available through the Public Patent Application Information Retrieval system (Public PAIR) on the USPTO internet web site (www.uspto.gov). Terminals that allow access to Public PAIR are available in the Public Search Room. The member of the public may also be entitled to obtain a copy of all or part of the application file upon payment of the appropriate fee. Such copies must be purchased through the Office of Public Records upon payment of the appropriate fee (37 CFR 1.19(b)).

For published applications that are still pending, a member of the public may obtain a copy of:
the file contents; the pending application as originally filed; or any document in the file of the pending application.

For unpublished applications that are still pending:

- (1) If the benefit of the pending application is claimed under 35 U.S.C. 119(e), 120, 121, or 365 in another application that has: (a) issued as a U.S. patent, or (b) published as a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of: the file contents; the pending application as originally filed; or any document in the file of the pending application.
- (2) If the application is incorporated by reference or otherwise identified in a U.S. patent, a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of the pending application as originally filed.

Signature [Signature]
Typed of printed name Arif B. Resny

Date 2/27/15

Registration Number, if applicable
703-686-1150
Telephone Number

FOR PTO USE ONLY

Approved by: _____

Unit: _____

RECEIVED
FEB 27 2015

This collection of information is required by 37 CFR 1.11 and 1.14. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. BRING TO: File Information Unit, Suite 3A20, 2800 South Randolph Street, Arlington, Virginia.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

REQUEST FOR ACCESS TO AN ABANDONED APPLICATION UNDER 37 CFR 1.14

Bring completed form to:
 File Information Unit, Suite 3A20
 2800 South Randolph Street
 Arlington, VA 22202
 Telephone: (703) 756-1800

In re Application of _____

Application Number

Filed

60-071628

Jan-16-1998

Paper No. 3

I hereby request access under 37 CFR 1.14(a)(1)(iv) to the application file record of the above-identified ABANDONED application, which is not within the file jacket of a pending Continued Prosecution Application (CPA) (37 CFR 1.53(d)) and which is identified in, or to which a benefit is claimed, in the following document (as shown in the attachment):

United States Patent Application Publication No. _____, page, _____ line _____

United States Patent Number 6140226, column _____, line, _____

WIPO Pub. No. _____, page _____, line _____

Related Information About Access to Applications Maintained in the Image File Wrapper System (IFW) and Access to Pending Applications in General

A member of the public, acting without a power to inspect, cannot order applications maintained in the IFW system through the FIU. If the member of the public is entitled to a copy of the application file, then the file is made available through the Public Patent Application Information Retrieval system (Public PAIR) on the USPTO internet web site (www.uspto.gov). Terminals that allow access to Public PAIR are available in the Public Search Room. The member of the public may also be entitled to obtain a copy of all or part of the application file upon payment of the appropriate fee. Such copies must be purchased through the Office of Public Records upon payment of the appropriate fee (37 CFR 1.19(b)).

For published applications that are still pending, a member of the public may obtain a copy of:

the file contents; the pending application as originally filed; or any document in the file of the pending application.

For unpublished applications that are still pending:

- (1) If the benefit of the pending application is claimed under 35 U.S.C. 119(e), 120, 121, or 365 in another application that has: (a) issued as a U.S. patent, or (b) published as a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of: the file contents; the pending application as originally filed; or any document in the file of the pending application.
- (2) If the application is incorporated by reference or otherwise identified in a U.S. patent, a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of the pending application as originally filed.

Signature

Typed of printed name

Registration Number, if applicable

Telephone Number

Date

FOR PTO USE ONLY

RECEIVED

Approved by:

Unit:

BY: SLO

This collection of information is required by 37 CFR 1.11 and 1.14. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. BRING TO: File Information Unit, Suite 3A20, 2800 South Randolph Street, Arlington, Virginia.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.