UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01376
Patent 6,197,696 B1

DECLARATION OF DR. BRUCE W. SMITH, PH.D.
IN SUPPORT OF PETITIONER'S REPLY

TSMC Exhibit 1049
TSMC v. IP Bridge
IPR2016-01376

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I, Dr. Bruce W. Smith, Ph.D., declare as follows:

I. Introduction

1. My name is Dr. Bruce W. Smith. I previously signed a declaration in relation to these proceedings on July 11, 2016, which I understand is Exhibit 1002. My qualifications, a summary of my opinions, a list of materials reviewed, and an explanation of the relevant legal standards I was asked to apply appear at paragraphs 1 through 31 of Exhibit 1002, which I incorporate herein by reference for brevity.

II. Materials Reviewed

2. In addition to the references listed in Exhibit 1002, I have reviewed the following references in forming the opinions expressed in this declaration:

- Declaration of Dr. Bruce W. Smith, Ph.D. dated July 11, 2016 (which I understand is Exhibit 1002);
- U.S. Provisional Patent Application No. 60/071,628 with line numbers appended (which I have been told is Exhibit 1048);
- Translation of Japanese Patent Application No. 10-079371 to Aoi (which I have been told is Exhibit 2012);
- Excerpts from James D. Plummer et al., "Silicon VLSI Technology: Fundamentals, Practice, and Modeling" (2000) ("*Plummer*," which I have been told are Exhibits 1030 and 2016);

- Excerpts from C.Y. Chang & S. M. Sze, "ULSI Technology" (1996) ("*Chang & Sze*," which I have been told is Exhibit 1031);

- Excerpts from S. Wolf & R.N. Tauber, "Silicon Processing for the VLSI Era: Volume 1: Process Technology" (1986) ("*Wolf & Tauber*," which I have been are Exhibits 1032 and 2020);

- U.S. Patent No. 5,091,047 to Cleeves et al. ("*Cleeves*," which I have been told is Exhibit 1033);

- U.S. Patent No. 6,287,973 to Aoi et al. ("the '973 patent," which I have been told is Exhibit 1034);

- U.S. Patent No. 4,560,436 to Bukhman et al. ("*Bukhman*," which I have been told is Exhibit 1035);

- U.S. Patent No. 6,091,081 to Matsubara et al. ("*Matsubara*," which I have been told is Exhibit 1036);

- U.S. Patent No. 4,473,437 to Higashikawa et al. ("*Higashikawa*," which I have been told is Exhibit 1037);

- U.S. Patent No. 5,880,018 to Boeck et al. ("*Boeck*," which I have been told is Exhibit 1038);

- U.S. Patent No. 4,832,789 to Cochran et al. ("*Cochran*," which I have been told is Exhibit 1039);

- U.S. Patent No. 4,855,252 to Peterman et al. ("*Peterman*," which I have been told is Exhibit 1040);

- U.S. Patent No. 5,786,276 to Brooks et al. ("*Brooks*," which I have been told is Exhibit 1041);

- U.S. Patent No. 5,756,216 to Becker et al. ("*Becker*," which I have been told is Exhibit 1042);

- U.S. Patent No. 5,821,168 to Jain ("*Jain 168*," which I have been told is Exhibit 1043);

- J.M. Moran & D. Maydan, "High Resolution, Steep Profile Resist Patterns," J. Vac. Sci. & Tech., vol. 16, no. 6 (Nov./Dec. 1979) ("*Moran & Maydan*," which I have been told is Exhibit 1044);

- M.M. O'Toole et al., "Linewidth Control in Projection Lithography Using a Multilayer Resist Process," IEEE Transactions on Electron Devices, vol. ED-28, no. 11 (Nov. 1981) ("*O'Toole*," which I have been told is Exhibit 1045);

- E. Bassous et al., "A Three-Layer Resist System for Deep U.V. and RIE Microlithography on Nonplanar Surfaces," J. Electrochem. Soc.: Solid-State Sci. & Tech. (Feb. 1983) ("*Bassous*," which I have been told is Exhibit 1046);

- Transcript of the Deposition of Dr. A. Glew (June 30, 2017) ("*Glew Deposition*," which I have been told is Exhibit 1047);

- Transcript of the Deposition of Dr. B. Smith (March 23, 2017) ("*Smith Deposition*," which I have been told is Exhibit 2010);

- J.R. Sheats & B.W. Smith, "Microlithography: Science and Technology," Chapters 9 & 10 (1998) (which I have been told is Exhibit 2017);

- K. Suzuki & B.W. Smith, "Microlithography: Science and Technology," Chapter 12 (2d ed., 2007) (which I have been told is Exhibit 2018);

- K. Suzuki & B.W. Smith, "Microlithography: Science and Technology," Chapter 11 (2d ed., 2007) (which I have been told is Exhibit 2019);

- M. Schaepkens et al., "Influence of Reactor Wall Conditions on Etch Processes in Inductively Coupled Fluorocarbon Plasmas," J. Vac. Sci. & Technol. A, vol. 16, no. 4, pp. 2099–2107 (July–Aug. 1998) ("*Schaepkens*" which I have been told is Exhibit 2014);

- Declaration of Alexander Glew, Ph.D. (which I have been told is Exhibit 2009);

- Patent Owner's Preliminary Response Under 37 C.F.R. § 42.107 (March 23, 2017) ("Paper 6");

- Decision on Institution (January 18, 2017) ("Paper 11"); and

- Patent Owner's Response Under 37 C.F.R. § 42.120 (April 14, 2017) ("Paper 19").

III. Legal Standards for Obviousness

3. I am not an attorney and have not been asked to offer my opinion on the law. As an expert offering an opinion on whether the claims in the '696 patent are patentable, however, I have been told I am obliged to follow existing law. In addition to the legal standards expressed at paragraphs 15 through 31 of Exhibit 1002, I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §§ 102 and 103.

4. I have been told a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements. I have been told the proper test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. I have been told a reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.

5. I have been told a reference "teaches away" from the claimed invention when a person of ordinary skill in the art, upon reading the reference, would be discouraged from following the path set out in the reference. I have also been told the existence of better alternatives in the prior art does not mean that an inferior alternative is inapt for obviousness purposes.

6. I have been told a person of ordinary skill in the art is a person of ordinary creativity, not an automaton, and knows how to combine familiar prior art elements to achieve the same functions. I have been told it is improper to ignore modifications that one skilled in the art would make to a device borrowed from the prior art.

7. I have been told it is improper to rely on drawings that are neither expressly to scale nor linked to quantitative values in the text.

IV. Application of the Board's Claim Construction

A. The plain meaning of "using the [designated layer] as a mask"

8. I have been told the Board adopted a preliminary claim construction in this matter. I understand that the Board has construed "using the [designated layer] as a mask" to mean "using the [designated layer] to define areas for etching."

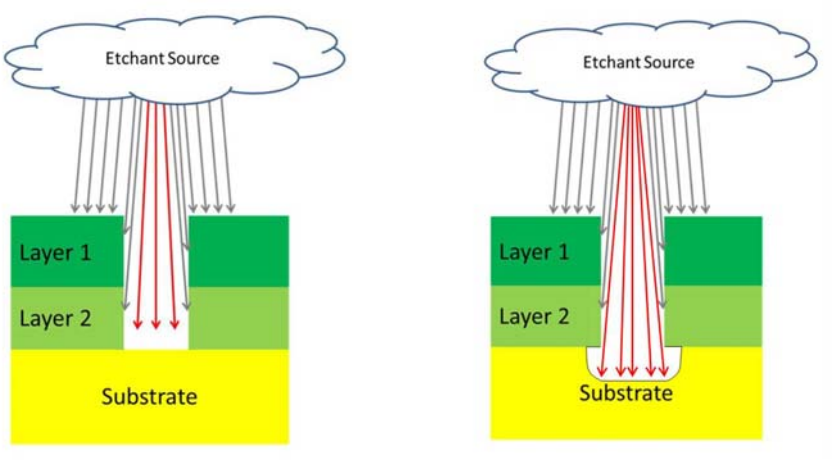
9. I have been told the designated layer "must actually be used to define areas for etching." For example, I have been told the Board determined a mask pattern that is entirely within a surrounding resist layer is not a mask. In addition, I have been told the Board found a buried layer (i.e., a layer without any portion of its top surface exposed to the etchant during a particular etch process) is not a mask simply because it has a lateral edge "in line and flush with [a lateral] edge of" the overlying layer.

10. In my opinion, the Board's claim construction and its application of the claim construction matches the plain and ordinary meaning of the term "mask" as used by those of ordinary skill in the art.

11. I disagree with IPB and Dr. Glew when they speculate that a buried layer might be mask because of particles traveling laterally. One of the fundamental requirements for a successful dual damascene technology is the ability to perform highly anisotropic etches that faithfully reproduce specified patterns. The etches at issue here are highly directional, with minimal lateral deviation. This is not due to any "masks" preventing lateral etching, but due to the reactive ion etch ("RIE") processes which are highly directional. *Plummer* at 611 ("[M]odern fabrication methods tend to employ directional etching and vertical steps with little undercutting."); *Plummer* at 619 ("[D]irectional etching is due to the presence of ionic species in the plasma and the electric fields that direct them normal to the wafer surface."); *Plummer* at 625 ("[I]t is usually assumed that all the ions arrive normal to the wafer surface, as shown in Figure 10-11(b)."); *Plummer* at 627 ("[D]irectional etching occurs [in RIE] because of the directionality of the ions. . . . Since the ions are striking normal to the wafer surface, the enhancement will occur normal to the wafer surface."); *Chang & Sze* at 329 ("Integrated circuit fabrication processes that use reactive plasmas are commonplace in today's semiconductor production lines because of their potential

for very-high-accuracy transfer of resist patterns, i.e., anisotropic etching, as shown in Fig. 1."); *Chang & Sze* at 338 ("[I]on transport must be perpendicular to the surface so that only the etch rate of the bottom surface is enhanced."). A mask, therefore, shields etchant particles traveling normal to the surface being etched. The vertical sidewalls in the opening that defines the pattern being etched do not "mask" the etch and are not relevant to the masking function.

12. If lateral particles were a problem as IPB suggests, those particles would cause significant undercutting in the layer being etched. IPB and Dr. Glew cite as evidence the figure on the left below, but that is not an accurate representation of what occurs during reactive ion etching. Even if it were, IPB and Dr. Glew ignore the resulting undercutting (shown to the right below). IPB's figure is inaccurate because such undercutting does not occur in these RIE processes, which produce nearly vertical sidewalls. If such undercutting did occur, it would lead to problems like void formation and electromigration, increased contact resistivity, and possibly contact failure. IPB's misleading figure does not provide evidence that the internal sidewall plays any role in defining areas for etching. What matters instead are sizes and shapes of the openings as seen from above in the plan view, not the internal sidewalls of a buried layer.



13. IPB cited *Plummer* but does not address the chapter devoted to etching (Chapter 10) or Section 10.2.2.1 ("Plasma Etching Mechanisms"), which explain RIE is highly directional. *Plummer* at 621–28. In RIE (the most common dry etch process, usually synonymous with dry etching), both neutral and ionic species are present. The ionic species are highly directional (i.e., anisotropic), traveling normal to the substrate. The neutral species are essentially isotropic, traveling in all directions. The plasma contains both chemically reactive species and chemically neutral species. Chemically reactive species remove material by reacting with it to form volatile species that come off the surface of the material being etched. Chemically neutral species remove material from a surface by physically bombarding it.

14. In RIE, all of these particles and processes work together synergistically, resulting in a highly directional etch, as *Plummer* explains:

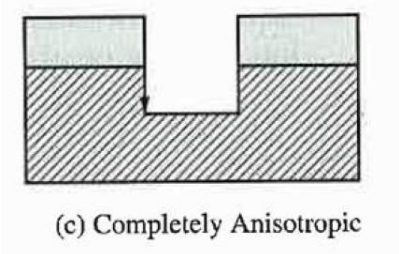
> In ion-enhanced etching, both chemical and physical components are acting, but the profiles are not just a linear combination of isotropic

chemical etching and anisotropic physical etching as illustrated in Figure 10-3(b). Instead, the profile for ion-enhanced etching is much more like the case for physical etching acting alone, as in Figure 10-3(c). If the chemical component in the etch system is increased, the vertical etching is increased but not the lateral etching, which is not what would be expected from chemical etching. . . .

So not only can one achieve very anisotropic etch profiles, but also a high degree of selectivity as well. This is something that is very difficult to achieve when the two components work independently. In addition, high etch rates can be achieved. Thus gas chemistries and etch conditions are usually chosen to promote ion-enhanced etching and to suppress independent chemical and physical etching. . . .

Whatever the exact mechanism for ion-enhanced etching, . . . directional etching occurs because of the directionality of the ions. The enhancement of the process . . . occurs only where the ions strike the surface. Since the ions are striking normal to the wafer surface, the enhancement will occur normal to the wafer surface. This directional enhancement will result in directional, anisotropic etching.

Plummer at 626–27.



***Plummer*, Figure 10-3(c)**

15. As a matter of physics, the interior surfaces of the layers above the layer being etched do not play the masking role IPB and Dr. Glew suggest. Such usage of the term "mask" is therefore improper even in the hyper-technical sense IPB and Dr. Glew suggest.

16. I disagree with IPB and Dr. Glew when they mistakenly suggest that multi-layer resist processes (e.g., tri-layer resists) are examples of buried layers acting as masks because they have flush interior sidewalls. IPB erroneously cites portions of my textbook to suggest I "admitted in prior publications that a 'multiple layer resist' having flush edges can be used to define a 'substrate film material' to be etched—i.e., can be used as a mask." Paper 19, at 17.

17. As I explained in my deposition, a tri-layer resist includes "two etch processes and a develop process." *Smith Deposition* at 64:9–10; *see also* 59:2–65:8. In this way, [m]ultilayer resist techniques . . . ease requirements for resist performance . . . by using physically distinct layers to separate the imaging function from the etch resistance, planarization, and reflection suppression functions." EX2017 at 79; EX2018 at 33.

18. The basic multi-layer resist process was developed in the late 1970s at Bell Labs and, to my knowledge, was first published in a paper by Moran & Maydan. As I explained in my deposition, first, a planarizing polymer layer (e.g., a photoresist) is formed on the wafer, followed by an etch-stop layer (e.g., SiO_2) that

provides oxygen etch resistance. Then, an imaging photoresist layer is deposited and developed to form the etch pattern. This is shown in the top image of Moran & Maydan's Figure 4 (see below). RIE is used to transfer the pattern of the imaging layer into the etch-stop layer using the imaging layer as a mask. This is shown in the middle image of Moran & Maydan's Figure 4 (see below). Finally, the pattern is transferred by RIE into the planarizing layer. Because the imaging layer and planarizing layer are both organic materials, the imaging layer (which is much thinner than the planarizing layer) is completely removed during this process. This is shown in the bottom image of Moran & Maydan's Figure 4 (see below). Other texts similarly describe the multi-layer resist process. *Moran & Maydan* at 1622–24, Figure 4; *Chang & Sze* at 294–95, 361, FIGURE 17; *Wolf & Tauber* at 424, Fig. 11; *Cleeves* at 3:29-41, FIGS. 1–4; *Bassous* at 479–80, Fig. 1; *O'Toole* at 1407, Fig. 6. The intermediate layer does not act as a mask until it is no longer buried (see figures below). In my textbook, I also provide a figure (Figure 12.3(c) on page 18 of EX2018) that combines into a single figure the independent tri-layer resist process steps depicted in each of the figures below. This figure in my textbook does not depict a physical structure as IPB and Dr. Glew appear to suggest.

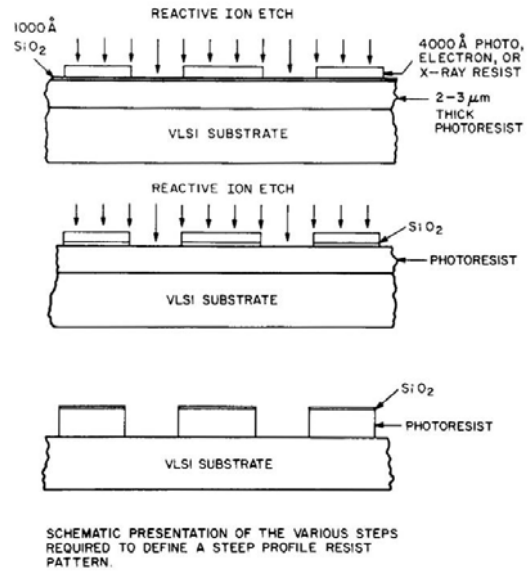
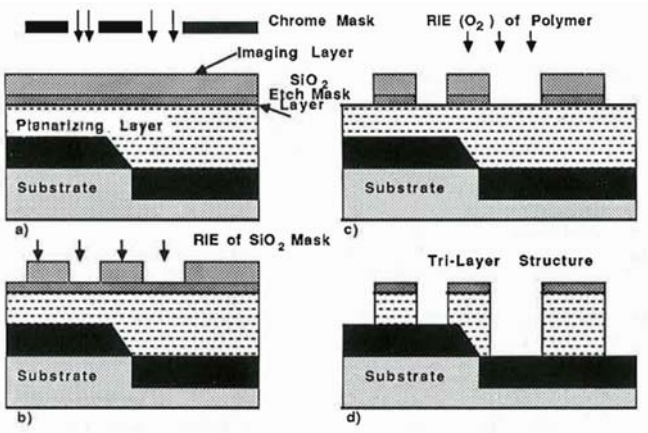


FIG. 4. Processing sequence for three level, high resolution patterning.

***Moran & Maydan*, Figure 4**



***Wolf & Tauber*, Fig. 11 (chapter 12)**

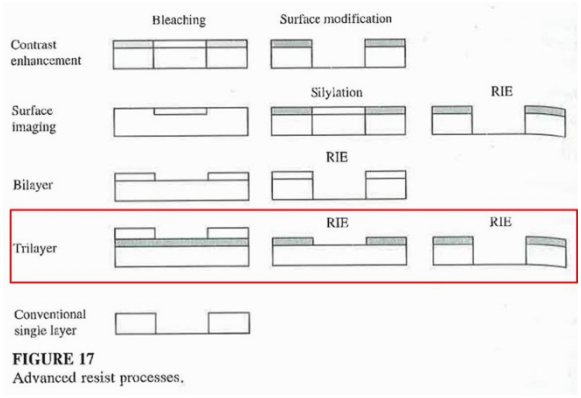
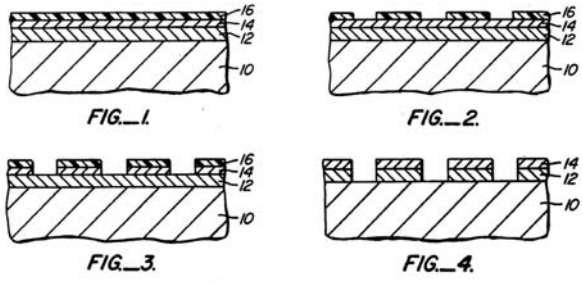


FIGURE 17
Advanced resist processes.

***Chang & Sze*, FIGURE 17 (chapter 6)**



***Cleeves*, FIGS. 1–4**

19. Likewise, in the final structures above, the planarizing layer does not act as a mask for etching the layer immediately below the planarizing layer. The purpose of the etch-stop layer is to act as a mask by providing etch resistance when layers below are etched. The etch-stop layer is chosen not only to resist the etch of the planarizing layer, but typically to also resist the etch used to transfer the pattern into the layer immediately below the planarizing layer. The purpose of the

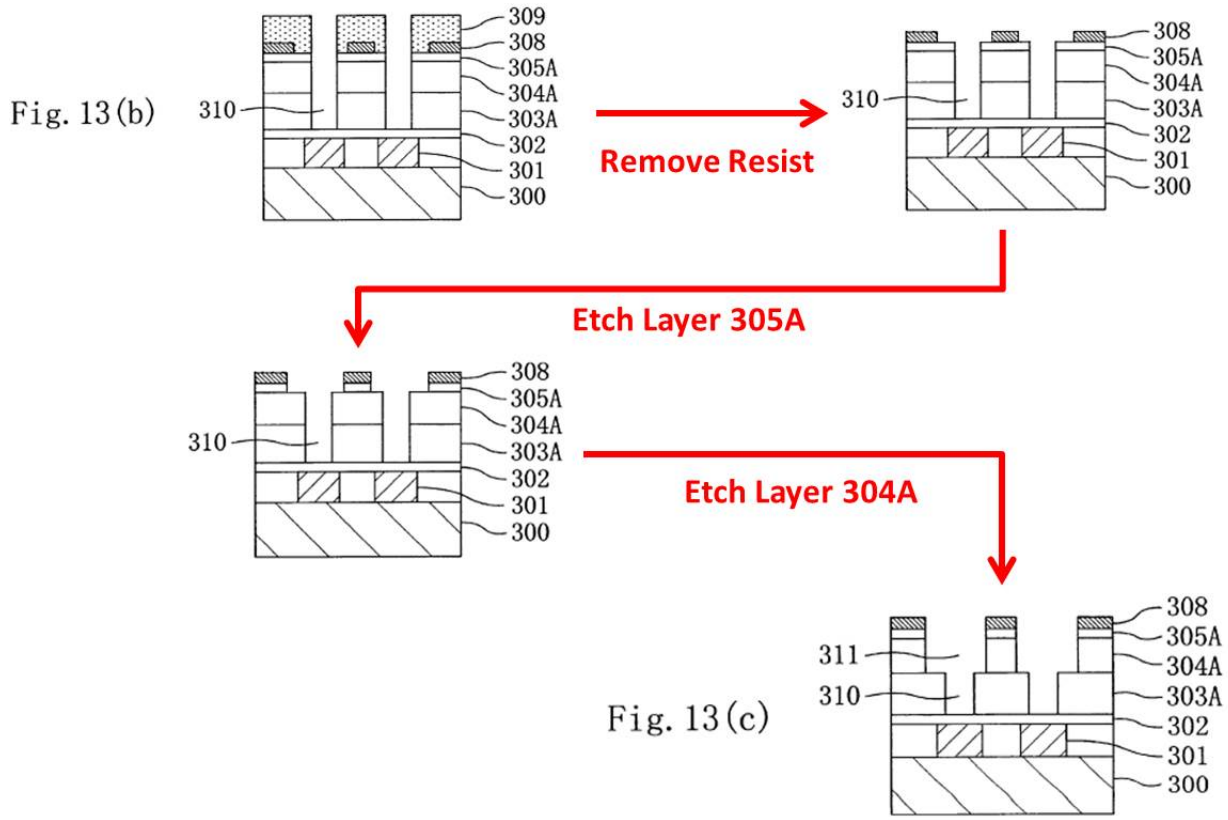
planarizing layer, on the other hand, is to prevent problems associated with optical lithography used to expose and develop the top imaging layer. In some instances, the planarizing layer could be used as a mask during subsequent etching (e.g., etching a SiO_2 film below the planarizing layer when the etch-stop layer is made of SiO_2), but only once the etch-stop layer is completely removed, not while the etch-stop layer is still intact. In other words, the planarizing layer does not act as a mask because of its interior sidewalls. My textbook does not suggest otherwise.

B. The specification of the '696 patent is internally inconsistent

20. I do not agree with IPB's suggestion that a buried layer acts as a mask simply because it has a lateral edge "in line and flush with [a lateral] edge of" the overlying layer. I have never heard anyone suggest such a layer would be a mask.

21. IPB appears to base its suggestion on three inconsistencies in the '696 patent, detailed immediately below, which in my opinion are errors:

> **(1)** **Buried Layer 305A as a "Mask"**—"Next, as shown in FIG. 13(c), the second resist pattern 309 is removed and the patterned second organic-containing silicon dioxide film 305A is dry-etched using the mask pattern 308 as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film 305A. Thereafter, the patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A having the openings for wiring grooves as a mask, thereby forming the wiring grooves 311." '696 patent at 17:30–40 (underlining added).



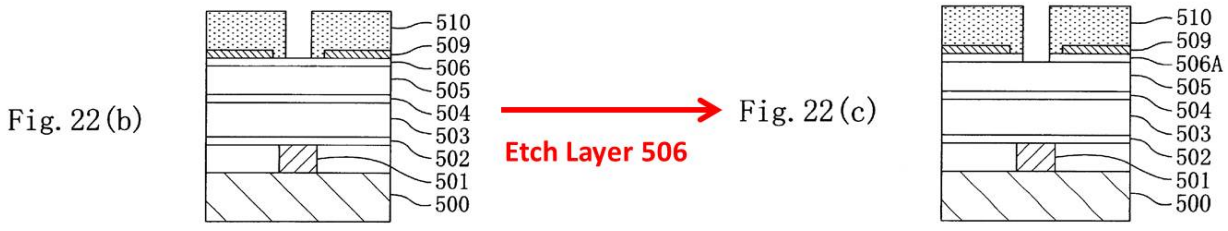
(2) **Buried Layer 355A as a "Mask"**—"Thereafter, as shown in FIG. 16(d), the patterned organic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves 362." '696 patent at 19:50–54 (underlining added).

(3) **Buried Layer 556B as a "Mask"**—"Then, the patterned second organic film 555A is dry-etched using the mask pattern 559 and the patterned second silicon dioxide film 556B as a mask, and the first organic film 553 is dry-etched using the patterned first silicon dioxide film 554A

as a mask, thereby forming a patterned second organic film 555B having wiring grooves 561 and a patterned first organic film 553A having contact holes 562 as shown in FIGS. 26(c) and 29(a)." '696 patent at 26:30–40 (underlining added).

22. During my deposition, I explained the second example is "not consistent with what is described in the rest of the process flow nor is it consistent with the diagrams." *Smith Deposition* at 45:1–47:18. The same is true of the other two examples.

23. I understand that Dr. Glew also found incorrect teachings in the '696 patent, such as when the '696 patent mistakenly identifies layer 509 as a mask in Figures 22(b) and 22(c) (see figures below). *Glew Deposition* at 97:12–99:21; '696 patent at 23:40–46.

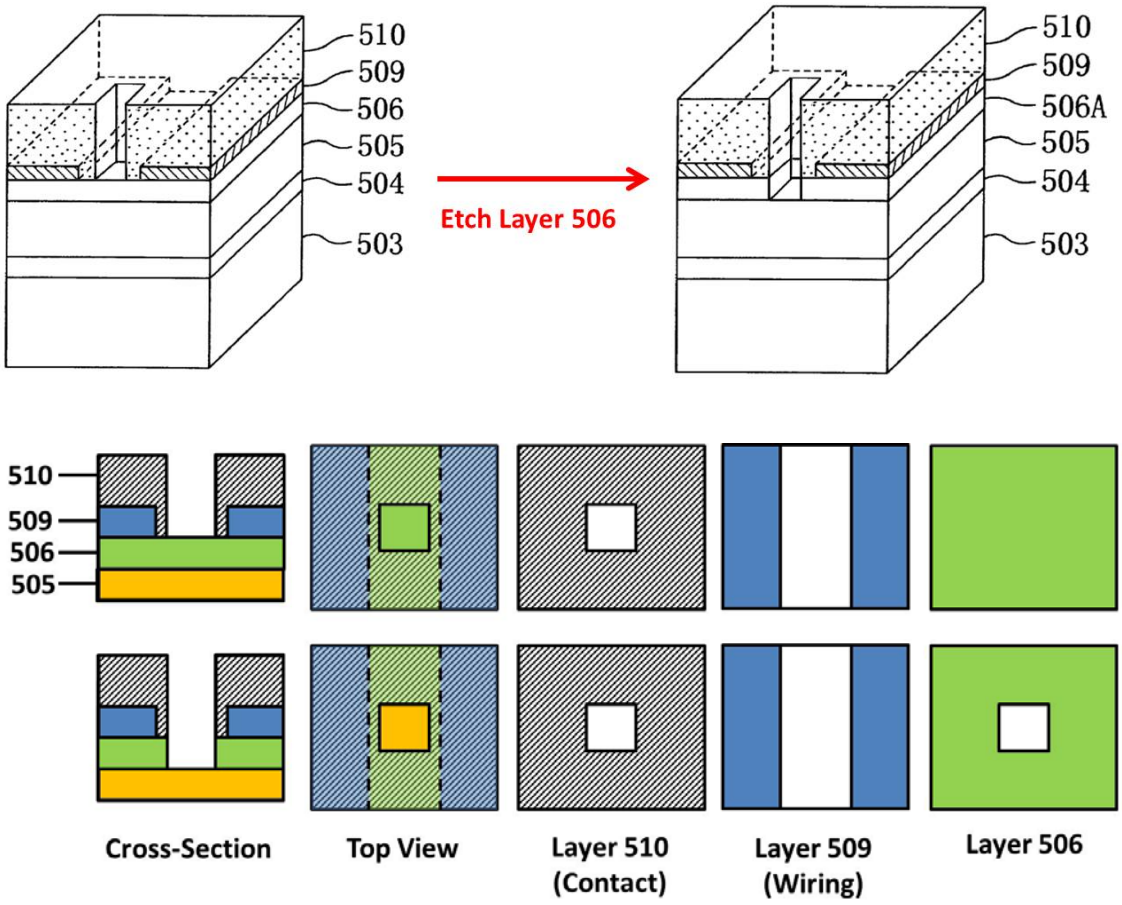


24. The statement in IPB's Preliminary Response that "there are other cross-sections in which the second resist pattern and the mask pattern, shown in

one cross-section in Figures 22(b) and 22(c), either have edges lined up and flush with one another that are used to etch the second silicon dioxide film (EX1001 at 17:50-62, 19:63-20:8), or are 'offset' such that the second resist pattern and the mask pattern are both used to define areas for etching" (Paper 6 at 42) is untrue, as even Dr. Glew admits. *Glew Deposition* at 97:12–99:21.

25. The opening in layer 510 of the figures above defines the contact hole. '696 patent at 23:40–42. The pattern in layer 509 of the figures above defines the wiring pattern. '696 patent at 23:25–32. As a person of skill in the art would have understood, and as Figures 27(a) through 29(a) of the '696 patent illustrate, the wiring grooves extend into and out of the cross-sections shown in Figures 22(b) and 22(c). That is because wiring grooves define the circuit layout of the integrated circuit, connecting many individual device structures. Each contact hole, on the other hand, is restricted to an individual device structure. The contact hole extends only minimally into and out of the cross-sections in Figures 22(b) and 22(c). The figures below explain how a person of ordinary skill in the art would have understood Figures 22(b) and 22(c). Just as Figure 27(b) represents the cross-section in Figure 25(c), the top figures below depict Figures 22(b) and 22(c). The bottom figures below illustrate the plan view of Figures 22(b) and 22(c). As shown in both sets of images, layer 509 is completely buried by the resist layer 510. There

are no "edges lined up and flush with" layer 510 or "offset[s]" that expose layer 509. Paper 6, at 42.

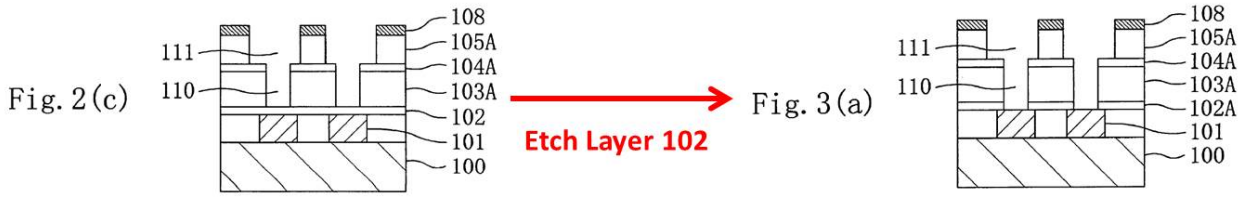


26. As these images illustrate and Dr. Glew's testimony confirms, a person of ordinary skill in the art would have understood the draftsperson made an error in the '696 specification by identifying layer 509 as a mask in Figures 22(b) and 22(c). The rationale proposed by IPB (Paper 6, at 42) makes no sense, because it would limit the example above to obscure, restrictive, and difficult-to-imagine circuit layouts with complex and unnecessary shapes. This would run contrary to the general nature of this processing technology and other examples in the '696

patent. In fact, the ’696 patent does not discuss circuit layouts at all, nor is there any technical reason for such restrictive and incomprehensible circuit layouts. To deem layer 509 a “mask” in this etch step would, in my view, would be contrary to the way a person of ordinary skill would have viewed the disclosure.

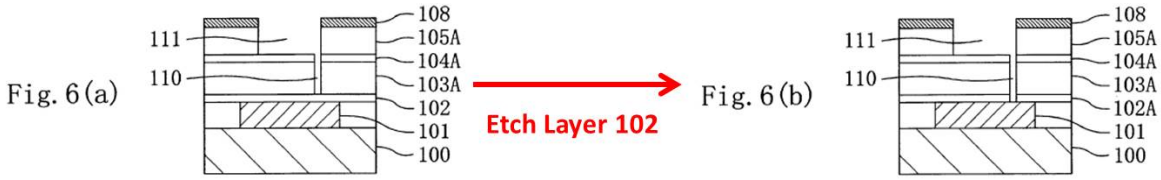
27. In my opinion, a person of ordinary skill in the art would have disregarded the misstatements made in the three examples IPB identified where a buried layer is called a “mask” in the specification. Not only do these examples contradict the common and ordinary meaning of what it means to act as a mask, they also contradict at least seven examples in the specification where a buried layer is not called a “mask”:

(1) **Buried Layer 103A not a “Mask”**—“Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in FIG. 3(a).” ’696 patent at 11:51–55 (underlining added).

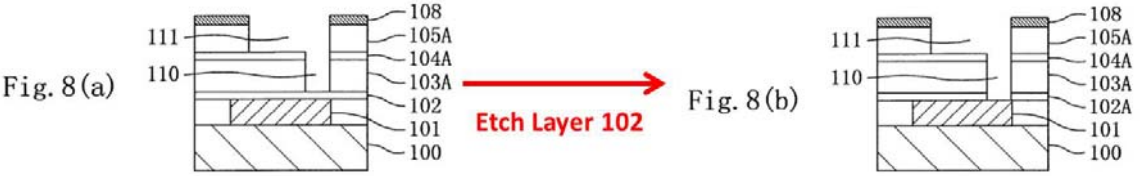


(2) **Buried Layer 103A not a “Mask”**—“[T]he silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes

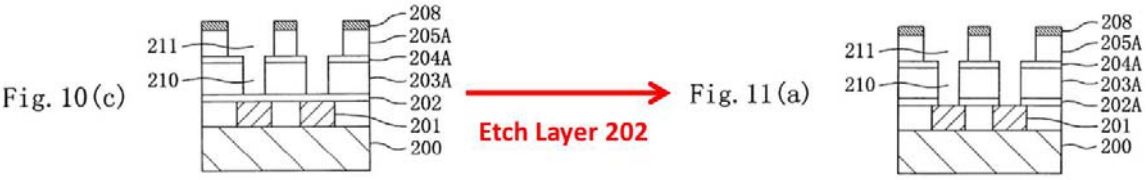
110 as shown in FIG. 6(b).” ’696 patent at 13:37–41 (underlining added).



(3) **Buried Layer 103A not a “Mask”**—“[T]he silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 withinthe contact holes 110 as shown in FIG. 8(b).” ’696 patent at 14:41–45 (underlining added).



(4) **Buried Layer 203A not a “Mask”**—“[T]he silicon nitride film 202 is dry-etched using the patterned organic-containing silicon dioxide film 204A as a mask, thereby forming a patterned silicon nitride film 202A and exposing the first metal interconnects 201 within the contact holes 210 as shown in FIG. 11(a).” ’696 patent at 16:7–11 (underlining added).



(5) **Buried Layers 304A and 305A not “Masks”**—“[T]he second organic-containing silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic-containing silicon dioxide film 303 are sequentially dry-

etched using the second resist pattern 309 as a mask. As a result, a patterned second organic-containing silicon dioxide film 305A, a patterned low-dielectric-constant SOG film 304A and a patterned first organic-containing silicon dioxide film 303A having contact holes 310 are formed as shown in FIG. 13(b)." '696 patent at 17:20–29 (underlining added).

Fig. 13(a)

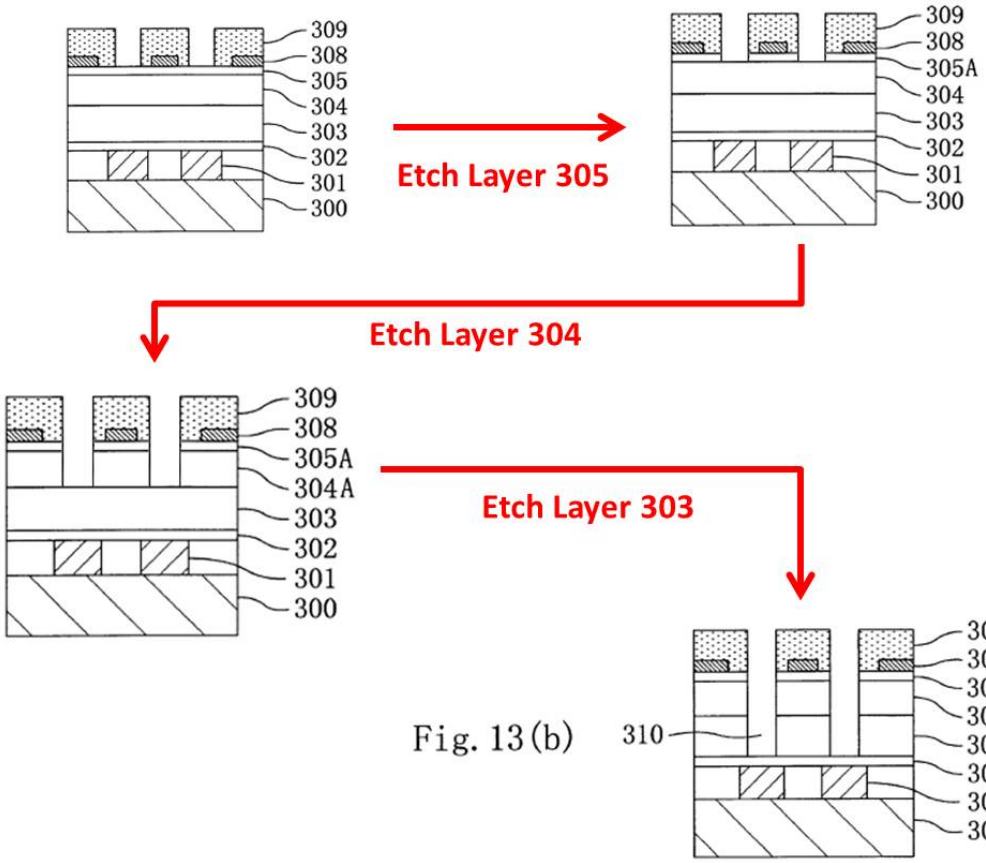
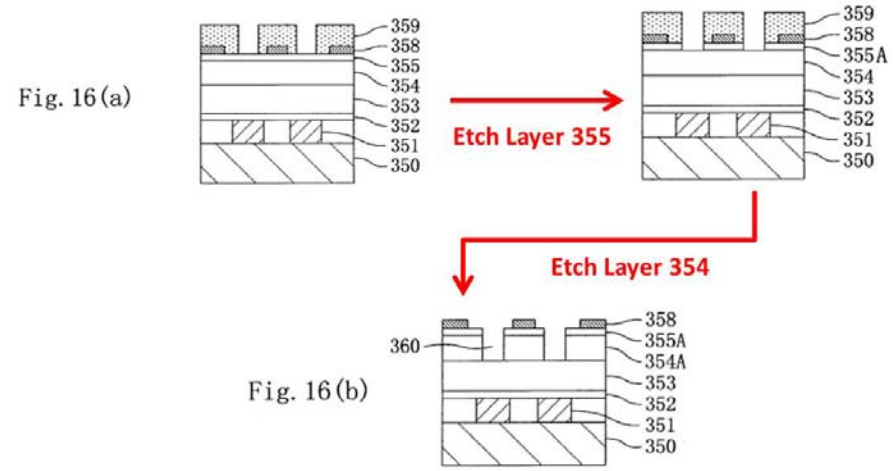
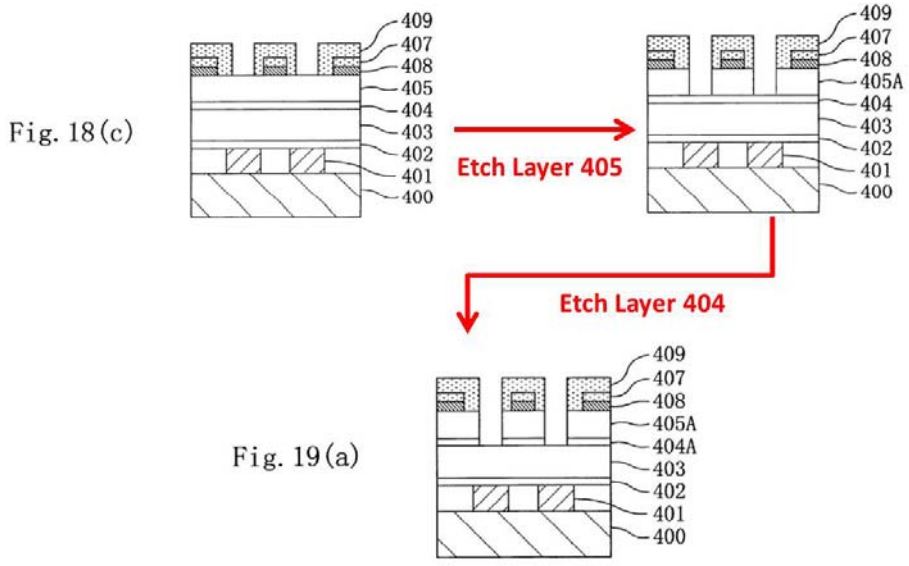


Fig. 13(b)

(6) **Buried Layer 355A not a "Mask"**—"[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask, thereby forming a patterned second silicon dioxide film 355A and a patterned organic film 354A having openings 360 for forming contact holes as shown in FIG. 16(b). In this case, the second resist pattern 359 is removed during the step of etching the organic film 354." '696 patent at 19:33–40 (underlining added).



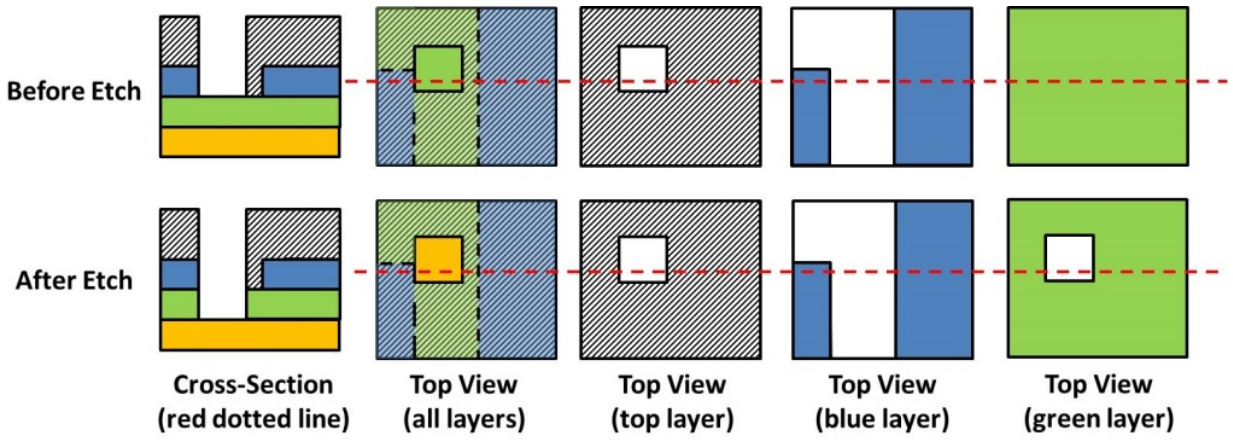
(7) **Buried Layer 405A not a "Mask"**—"[T]he second low-dielectric-constant SOG film 405 and the organic-containing silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask, thereby forming a patterned second low-dielectric-constant SOG film 405A and a patterned organic-containing silicon dioxide film 404A as shown in FIG. 19(a)." '696 patent at 21:33–39 (underlining added).



28. The discussion in this section demonstrates the specification of the '696 patent is inconsistent regarding buried layers acting as "masks."

V. Japanese patent application No. 10-079371 does not disclose all elements of claim 13

29. IPB suggests that a buried layer acts as a mask even when it has nothing to do with the etch. Consider the illustrations below. The top layer (striped layer) contains the via (i.e., contact hole) pattern, and the buried layer (blue) contains the wiring pattern. The etch I am describing is used to transfer the via pattern into the green layer. In IPB's view, the blue layer in this example acts as a mask even though it does not define the via pattern. This would make the term "mask" meaningless and confusing to a person of ordinary skill in the art.

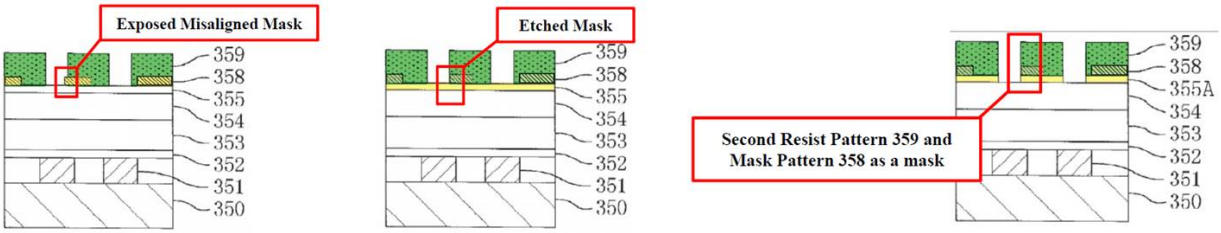


30. IPB's argument that the Japanese '371 application supports step h) of claim 13 hinges on the description of a contingent process used to compensate for unwanted misalignment errors. The Japanese '371 application explains the process:

> If the second resist pattern 359 may have been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. That is to say, if the mask pattern 358 is partially

> exposed inside the openings of the second resist pattern 359 for forming contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask.

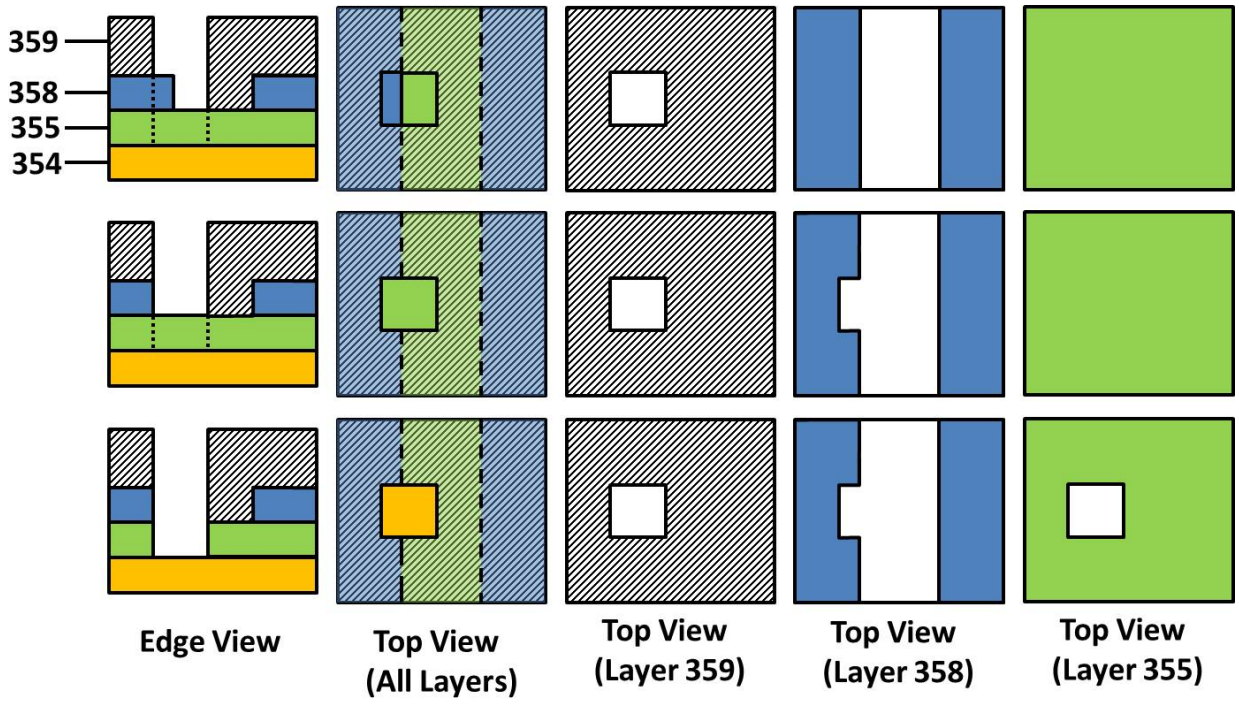
EX2012 at 39:12–21; Japanese '371 application at ¶ 96. The figures IPB uses in support of its position are reproduced below.



31. The description IPB relies on states, "[T]he second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask." The Japanese '371 application makes no mention of using layer 358 as a "mask" in this process, which is appropriate because layer 358 is not a mask in this process. The sole purpose of this process is to eliminate exposed portions of layer 358 so it does not act as a mask. The Japanese '371 application requires removing the exposed portions of layer 358, otherwise layer 358 would define a narrower contact hole pattern than designed, causing increased contact resistance, void formation during metallization, reduced reliability, and/or failed contacts. Japanese '371 application at ¶ 54, Fig. 6(c); EX2012, 26:20-24, Fig. 6(c). In other words, a person of

ordinary skill in the art would have understood the Japanese ’371 application teaches how to avoid layer 358 inadvertently becoming a mask.

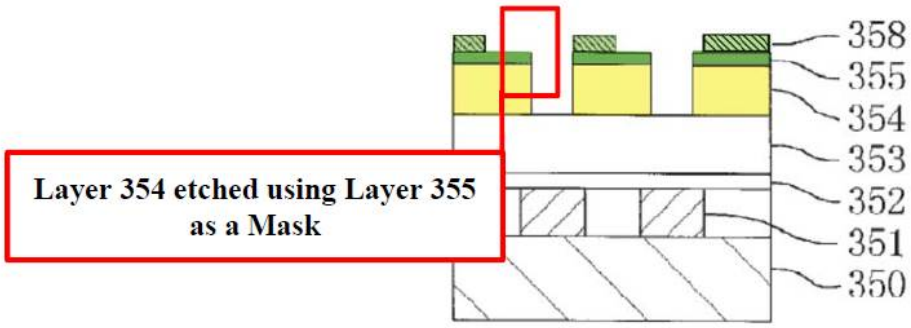
32. The top view of this process illustrates why IPB’s suggestion that layer 358 acts as a mask is wrong. The images in the first column below show the cross-section; the images in the second column illustrate the composite top view; the images in the third column illustrate the top view of layer 359 only (the contact hole, i.e., via); the images in the fourth column illustrate the top view of layer 358 only (the wiring groove); and the images in the fifth column illustrate the top view of layer 355 only. The top row illustrates the misalignment of resist layer 359; the second row illustrates the etching of the exposed portion of layer 358; and the third row illustrates the etching of layer 355. The goal of this process, like the goal of the process without misalignment, is to transfer the via pattern of layer 359 into layer 355 faithfully. Layer 358, which contains the wiring pattern, does not “define areas for etching” a via in layer 355. As these images show—and the text of the Japanese ’371 application explains—layer 359 is the sole mask used to define the square-shaped areas for etching in layer 355. Japanese ’371 application at ¶ 93, 96.



33. Even accepting the '696 patent's incorrect descriptions of certain buried layers with flush edges acting as "mask," layer 358 in the example above is different. Each example of a buried "mask" IPB identifies in the '696 patent is a buried layer that shares the same pattern as the top layer (specifically, the wiring pattern). '696 patent at 17:35–40, 19:50–54, 26:15–29. In the example above, however, layer 358 contains a wiring pattern, whereas layer 359 contains the via pattern being etched. The wiring groove in layer 358 therefore does not act as a mask during the via etch because layer 359 completely defines the via pattern.

34. IPB also mistakenly suggests the Japanese '371 application supports step i) of claim 13, citing the following figure below and a statement in the Japanese '371 application that "the second resist pattern 359 is removed during the

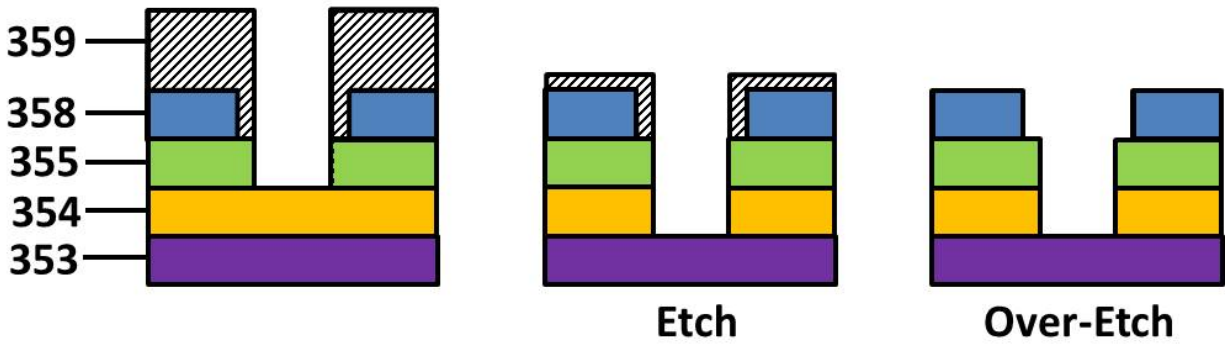
step of etching the organic film 354." Japanese '371 application at ¶ 93; EX2012 at 38:17–19. What IPB fails to address, however, is the statement in the Japanese '371 application that "the second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask." Japanese '371 application at ¶ 93; EX2012 at 38:13–17. Because the Japanese '371 application does not teach layer 355 (the alleged "third insulating film") as a mask for layer 354 (the alleged "second insulating film"), the Japanese '371 application does not support step i) of claim 13.



35. IPB mistakenly suggests layer 355 is a mask just because second resist pattern 359 is removed during the process used to etch organic film 354. In my opinion, there is no reason to think second resist pattern 359 is removed before the complete patterning of layer 354. Instead, I believe a person of ordinary skill in the art would have understood that layer 354 is patterned before second resist pattern 359 is fully removed.

36. When the Japanese '371 application explains layer 359 acts as a mask for etching layer 354 and "is removed during the step of etching the organic film

354" (Japanese '371 application at ¶ 93; EX2012 at 38:13-19), a person of ordinary skill in the art would have understood that layer 354 is patterned before second resist pattern 359 is completely removed. Not only does the Japanese '371 application expressly state that layer 359 is the mask, those of ordinary skill in the art would have already understood from their training that it would be common for layer 354 to be patterned before completely removing the remnants of second resist pattern 359. This technique, called "overetch," was known by those of ordinary skill in the art to be used where a via etch takes place over a stepped structure (as in the Japanese '371 application). *Chang & Sze* at 341 ("In the case of a via etch a large amount of overetch time is required."); *Plummer* at 614 ("[O]veretching is also required to remove residual film from steps."). The over-etching process for a via etch is shown below.



VI. U.S. Patent Application No. 60/071,628 discloses all elements of *Grill*'s claim 28

37. I have been asked to provide my opinions regarding whether the '628 application supports claim 28 of the *Grill* patent. As I explained in Appendix B of

my declaration dated July 11, 2016, it is my opinion that a person of ordinary skill in the art would have understood the '628 application to disclose all the limitations of claim 28.

38. There are two typographical errors in Appendix B of my declaration dated July 11, 2016, which I corrected during my deposition. *Smith Deposition* at 29:2–30:18. One of those was first identified shortly after TSMC's Petition was filed. The sentence at page B-10 of Appendix B says, "A person of ordinary skill in the art would have understood that etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have similar etch properties" (emphasis added). It should read, "A person of ordinary skill in the art would have understood that etching layer 12 under such circumstances concurrently etches layer 62 because the two layers have similar etch properties" (emphasis added). I have been told TSMC sought correction of that error but was denied permission to do so at that time. I again identified this mistake, along with another one, during my deposition. *Smith Deposition* at 29:2–30:18. The identification of layer 58 instead of layer 62 as the layer concurrently etched with layer 12 was a simple transcription error as at least four points clarify.

39. First, the relevant entry of the table in Appendix B states:

> Although the non-provisional application for the '696 patent added a statement that the "[p]atterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to

pattern dielectric 12," *Grill* at 7:64-66, a person of ordinary skill in the art would have already understood this to be part of the '628 application's disclosures.

The purpose of this entry is to explain why a person of ordinary skill in the art would have understood that layer 62 is concurrently removed as layer 12 is etched.

40. Second, the sentence in question on page B-10 as written makes no sense because it is false. The '628 application makes clear that layer 58 has "*different* etch properties from . . . the dielectric underlayers 12 and 8." EX1048 at 15:12–15 (emphasis added). The statement on page B-10, however, falsely states, "A person of ordinary skill in the art would have understood that etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have *similar* etch properties" (emphasis added). Identifying layer 58 in this context would make no sense.

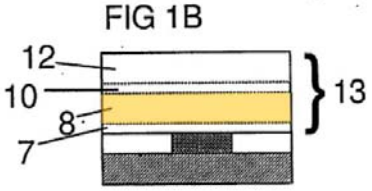
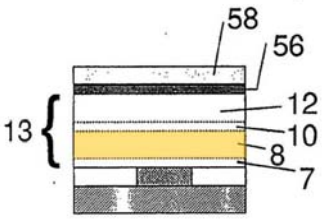
41. Third, the only two materials being removed between FIG. 5E and FIG. 5F, which illustrate the etching process for layer 12, are layer 62 and layer 12. Layer 58 is not affected. In addition, layer 58 is colored purple, which does not correspond with the coloring of any part of the claim language.

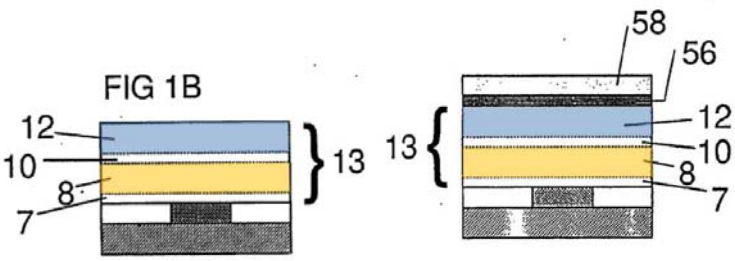
42. Fourth, the sentence immediately preceding the sentence in question states, "'interconnect dielectric and the photoresist stencil used to pattern the hard mask [may] have similar etch characteristics,' such as 'the case when an organic

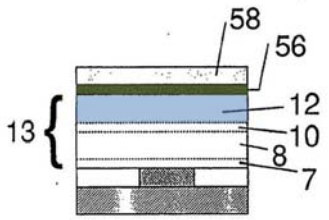
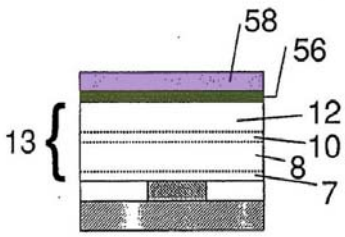
photoresist and a carbon-based interconnect dielectric such as DLC.'" EX1002 at 135 (quoting the '682 application). Layer 12 is a carbon-based interconnect dielectric such as DLC, and layer 62 is a photoresist stencil. EX1048 at 12:37-38, 15:23-28. Layer 58, however, is SiO_2, which is neither a photoresist nor a carbon-based dielectric. EX1048 at 15:14-15. Stating "[a] person of ordinary skill in the art would have understood that etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have similar etch properties" makes no sense in the context of the preceding sentence. Instead, the preceding sentence shows why a person of ordinary skill in the art would have understood that layer 62 (a photoresist), not layer 58 (SiO_2), is concurrently removed as layer 12 (DLC) is etched.

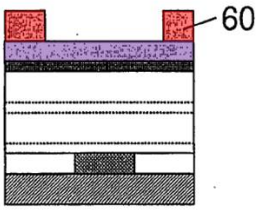
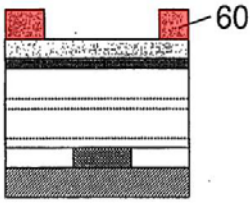
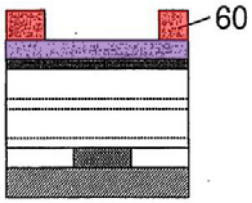
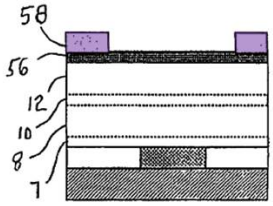
43. The chart below corrects those errors and again explains how the '628 application supports claim 28 of the *Grill* patent:

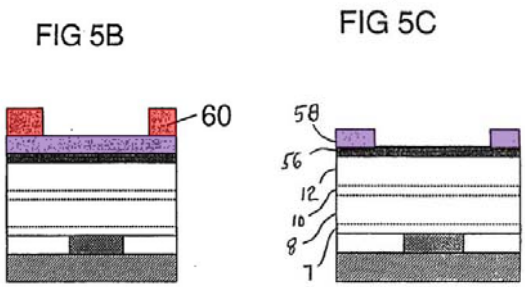
***Grill* Claim 28 Element**	**Disclosure of U.S. Provisional Application 60/071,628 ("'628 application")**
28. A method for forming an interconnect structure on the upper surface of a **substrate** having conductive regions comprising the steps of:	"Figs. 5A-5E show a first preferred embodiment of a method for forming a dual pattern hard mask comprising a first layer of material with a first pattern, and a second layer of material with a second pattern; Figs. 5F-5H show how this dual pattern hard mask may be used to fabricate a dual relief cavity for use in a Dual Damascene process. For purposes of illustration, one of said first and second patterns will be a via level pattern, and the other of said first and second patterns will be a

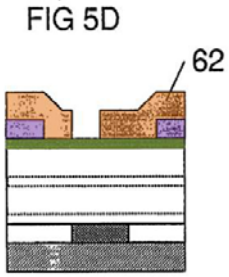
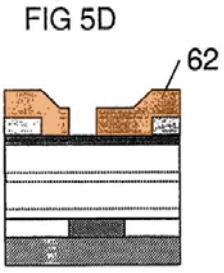
	wiring level pattern." EX1048 at 15:3-8.
forming over said **substrate** a **first dielectric layer** having a thickness corresponding to the thickness of an interconnect via,	FIG 1B  FIG 5A  **'628 application at FIGS. 1B, 5A** "The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown), conductive via 4, and dielectric passivation layer 6. "A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a **via level dielectric 8**, an optional dielectric etch stop layer 10, and a wiring level dielectric 12 are then applied to produce the structure of Fig. 1B. **Via** and wiring **dielectrics 8** and 12 might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 may be materials such as SiO2, Si3N4, silicon-containing DLC (SiDLC), etc. **The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.**" EX1048 at 12:35-40. *See also* EX1048 at 15:11-12 ("Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58.").

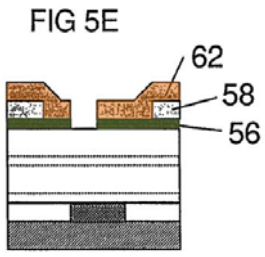
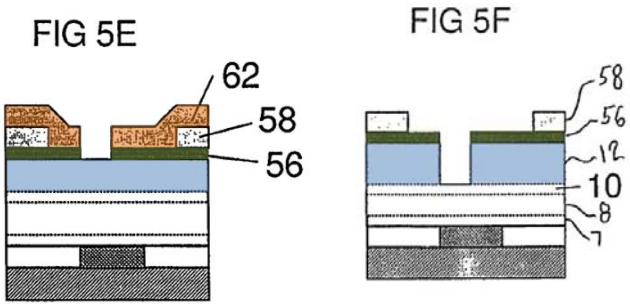
forming over said **first dielectric layer** a **second dielectric layer** having a thickness corresponding to the thickness of an interconnect wiring layer,	FIG 5A  **'628 application at FIGS. 1B, 5A** "The process flow may be exercised on a variety of substrates but is illustrated for the simplified substrate of Fig. 1A which comprises a semiconductor base 2 containing arrays of electrical devices (not shown), conductive via 4, and dielectric passivation layer 6. "A layered dielectric stack 13 comprising an optional dielectric passivation/adhesion layer 7, a **via level dielectric 8**, an optional dielectric etch stop layer 10, and a **wiring level dielectric 12** are then applied to produce the structure of Fig. 1B. **Via** and **wiring** dielectrics **8** and **12** might be carbon-based materials such as DLC or fluorinated DLC (FDLC), and optional dielectric etch stop 10 may be materials such as SiO2, Si3N4, silicon-containing DLC (SiDLC), etc. **The total thickness of layered dielectric stack 13 closely approximates the sum of the via and wiring level thickness.**" EX1048 at 12:31-40. *See also* EX1048 at 15:11-12 ("Fig. 5A shows the structure of Fig. 1B after application of lower hard mask layer 56 and upper hard mask layer 58.").

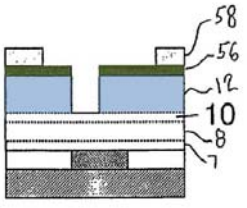
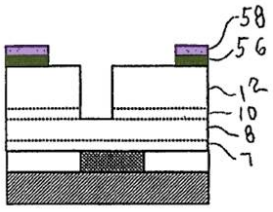
forming a **first hard mask layer** over said **second [dielectric] layer**,	FIG 5A  **'628 application at FIG. 5A** "Fig. 5A shows the structure of Fig. 1B after application of **lower hard mask layer 56** and upper hard mask layer 58. **Hard mask layers 56** and 58 are preferably formed from different materials which have different etch properties from each other and from dielectric **underlayers 12** and 8." EX1048 at 15:11-13.
forming a **second hard mask layer** over said **first hard mask layer**, said **second hard mask layer** preferably formed of a material different from said **first hard mask** to permit selective etching of said **second hard mask layer** with respect to said **first hard mask layer**,	FIG 5A  **'628 application at FIG. 5A** "Fig. 5A shows the structure of Fig. 1B after application of **lower hard mask layer 56** and **upper hard mask layer 58**. Hard mask layers **56** and **58** are preferably formed from different materials which have different etch properties from each other and from dielectric underlayers 12 and 8. For example, **lower hard mask layer 56** might be formed from Si3N4 and **upper hard mask layer 58** might be formed from SiO2. . . . . The etching process is preferably selective, for example a selective SiO2 to Si3N4 etch, so that **lower hard mask layer 56** will remain intact during any overetching of **hard mask layer 58**." EX1048 at 15:11-22.

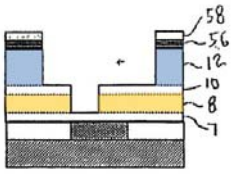
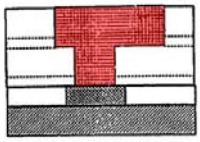
forming a **first layer of resist** over said **second hard mask layer**,	FIG 5B  **'628 application at FIG. 5B** "A **first resist layer 60**, patterned with a first (wiring level) pattern, is formed on **layer 58** to form the structure of Fig. 5B." EX1048 at 15:17-18.
patterning said **first layer of resist** with a wiring pattern,	FIG 5B  **'628 application at FIG. 5B** "A **first resist layer 60**, **patterned with a first (wiring level) pattern**, is formed on layer 58 to form the structure of Fig. 5B." EX1048 at 15:17-18.
patterning said **second hard mask layer** using said wiring-patterned **first layer of resist** as a mask,	FIG 5B  FIG 5C  **'628 application at FIGS. 5B, 5C** "The **pattern of resist layer 60** is transferred into **upper hard mask layer 58** by an etching process

	to form the structure of Fig. 5C. The etching process is preferably selective, for example a selective SiO2 to Si3N4 etch, so that lower hard mask layer 56 will remain intact during any overetching of **hard mask layer 58**." EX1048 at 15:19-22.
removing said wiring-patterned **first layer of resist**,	 **'628 application at FIGS. 5B, 5C** Although the *Grill* patent later added a statement that the "[p]atterned resist layer 60 is . . . removed by a process such as ashing or wet chemical etching," a person of ordinary skill in the art would have already understood this to be taught by the '628 application. The '628 application teaches that rework problems are caused when the photoresist and dielectric material have similar etch properties. EX1048 at 11:13-15 ("[D]ifficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics. Such would be the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC."). Accordingly, a person of ordinary skill in the art would have understood that resist rework is not a problem at this stage because the upper hard mask layer 58 and **photoresist layer 60** have different etch properties. EX1048 at 15:12-19 ("Hard mask layers 56 and 58 are preferably formed from different materials which have different etch

	properties from each other and from the dielectric underlayers 12 and 8. . . . If **resist layer 60** is misaligned, rework at this stage presents no problem.”). A person of ordinary skill in the art thus would have understood that the photoresist layer 60 is removed after hard mask layer 58 is etched. A person of ordinary skill in the art would have understood that the transition between Figures 5B and 5C above occurs by first etching layer 58, and subsequently removing the remaining photoresist layer 60.
forming a **second layer of resist** over said **first [hard mask layer]** and **second hard mask layer**,	 **’628 application at FIG. 5D** “A **second resist layer 62**, patterned with a second (via level) pattern, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D.” EX1048 at 15:23-24.
patterning said **second layer of resist** with a via pattern,	 **’628 application at FIG. 5D** “A **second resist layer 62**, **patterned with a second (via level) pattern**, is then formed on the structure of Fig. 5C to produce the structure of Fig. 5D.” EX1048 at 15:23-24.

patterning said **first hard mask layer** using said via-patterned **second layer of resist** as a mask,	 **'628 application at FIG. 5E** "The **pattern of resist layer 62** is then transferred into **lower hard mask layer 56**." EX1048 at 15:25-26.
transferring said via pattern in said patterned **first hard mask layer** into said **second dielectric layer**, while concurrently removing said via-patterned **second layer of resist**, and	 **'628 application at FIGS. 5E, 5F** "The **via level pattern** is then transferred into **dielectric 12** by an etching process such as reactive ion etching, to produce the structure of Fig. 5F." EX1048 at 15:29-30. Although the *Grill* patent later added a statement that the "[p]atterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12," *Grill* at 7:64–66, a person of ordinary skill in the art would have understood this to be taught by the '628 application. The '628 application teaches that the "interconnect dielectric and the photoresist stencil used to pattern the hard mask [may] have similar etch characteristics," such as "the case with an organic photoresist and a carbon-based interconnect dielectric such as DLC." EX1048 at 11:12-15. A person of ordinary skill in the art

	would have understood that etching layer 12 (DLC) under such circumstances concurrently removes layer 62 (photoresist) because the two layers have similar etch properties. A person of ordinary skill in the art would have further understood that photoresist layer 62 is not removed prior to etching layer 12. Photoresist layer 62 cannot be removed by a dry process before patterning layer 12 because any dry process for removing layer 62 would concurrently etch layer 12, as claim 28 reqires. Again, layers 12 and 62 (photoresist and DLC) have similar etch properties. Similarly, any attempt to strip the photoresist using a wet checmical process before etching layer 12 would cause the problems described with regard to Figures 2C and 2D and damage exposed dielectric layer 12. '682 application at 4, Fig. 2C, 2D. A person of ordinary skill in the art would have thus understood that the transition between Figures 5E and 5F involves concurrently removing photoresist layer 62 and dielectric layer 12.
patterning said via-patterned **first hard mask layer** using said wiring-patterned **second hard mask layer** as a mask,	FIG 5F  FIG 5G  **'628 application at FIG. 5G** "The etching conditions are then changed to removed [sic] exposed portions of **lower hard mask layer 56** and optional etch stop 10, to form the structure of Fig. 5G." EX1048 at 15:30-32.

transferring, at least partially concurrently, said via pattern into said **first dielectric layer** to form via cavities corresponding to said via pattern, and said wiring pattern into said **second dielectric layer** to form wiring cavities corresponding to said wiring pattern, and	FIG 5H  **'628 application at FIG. 5H** "Dielectrics **8** and **12** are then etched to transfer said **second pattern [wiring level]** into the entire thickness of **dielectric 12**, and said **first pattern [via level]** into the entire thickness of **dielectric 8**, as shown in Fig, 5H." EX1048 at 15:32-34.
filling said cavities with **conductive material** to make electrical contact with said conductive regions and to form said vias and said wiring pattern.	FIG 1L  **'628 application at FIG. 1L** "The cavity structure may then be completed as shown in FIG. 1J, and, for interconnect applications, filled with **wiring material** as shown in FIGS. 1K to 1L." EX1048 at 15:34-35.

44. I believe IPB only challenges one aspect of the chart in the previous paragraph—the limitation of "transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, while concurrently removing said via-patterned second layer of resist." IPB argues that *Grill* has a statement that constitutes "new matter": "Patterned second resist layer 62 is absent from FIG. 5F

because it is typically removed by the etching process used to pattern dielectric 12." *Grill* at 7:64–66.

45. I have been told an amendment that merely clarifies a disclosure in a previously filed application does not constitute new matter. In my opinion, this statement merely clarifies what a person of ordinary skill in the art would have understood from the '628 application. In my opinion, the '628 application teaches that a patterned second layer of resist (i.e., photoresist layer 62) is removed while transferring the via pattern into a second dielectric layer (i.e., DLC layer 12).

46. Layer 62 is photoresist, and layer 12 is a carbon-based material, such as diamond-like carbon (DLC) or fluorinated DLC. EX1048 at 12:37-38, 15:23-28. The '628 application explains that photoresist and carbon-based dielectrics like DLC "have similar etch characteristics." EX1048 at 11:12-15; *see also* 13:31-42, FIGS. 2A-2D (describing undercut resulting from simultaneous removal of a photoresist and DLC layer). A person of ordinary skill in the art would have known from this fact that any process for patterning (i.e., etching) layer 12 (a carbon-based material) concurrently removes layer 62 (a photoresist with similar etch properties).[1] Because layers 12 and 62 have similar etch properties, any attempt to

[1] As the '696 patent confirms, "removing" a layer refers not just to complete removal, but also partial removal. '696 patent at 11:19–31, 23:51–65, 26:3–14, 28:55–67, 30:62–31:6. As I understand it, claim 28 recites the phrase "while

remove layer 62 before patterning layer 12 would cause the problems described in relation to FIGS. 2C and 2D of the '628 application. It is therefore not a viable option. The only viable option is to begin patterning layer 12 while layer 62 is in place. And because layers 12 and 62 have similar etch properties, the very act of patterning (i.e., etching) layer 12 will concurrently remove layer 62.

47. Even without this explicit disclosure, I believe a person of ordinary skill in the art would have understood from the layer chemistries disclosed by the '628 application that photoresist layer 62 would be removed while patterning carbon-based layer 12. Persons of ordinary skill in the art knew organic photoresist (the most common photoresists, typically synonymous with "photoresist") and carbon-based dielectrics (e.g., DLC or FDLC) have similar etch properties.

48. *Matsubara* explains that photoresist and carbon-based dielectrics (e.g., DLC and fluorinated DLC) are simultaneous removed by the same etch:

> Of course, if ashing of resist can be easily performed, the silicon oxide film can be etched until the DLC film 44 is exposed without removing the resist. It may then be removed at the same time that the DLC film 44, the amorphous carbon fluoride film 43, and the DLC film 42 are etched.

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concurrently removing," which indicates the removal process need not be completed for the claim element to be satisfied.

Matsubara at 13:54–59.

49. *Zhao* explains that photoresist and carbon-based dielectrics are removed simultaneously by the same etch:

> [A]n anisotropic photoresist strip etch using O_2 plasma is used to remove the remaining photoresistive material 16. As an example, a high-density plasma etch utilizing low pressure, typically less than 5 mTorr can be used for this step. The resulting structure is shown in FIG. 5. It is to be noted that the photoresist strip step can cause the removal of some of the low-$\in$ material of layer 14 residing below the opening 17, as shown in FIG. 5. However, since another low-$\in$ material layer will be deposited and planarized, such partial etching of the low-$\in$ material at the particular location is not a concern.

Zhao at 6:43–53, *see also* 2:1–8, 7:30–46, 8:9–18, Figs. 5, 8.

50. *Boeck* explains that photoresist and carbon-based dielectrics (e.g., polyphenylquinoxaline (PPQ) or polyimides) are simultaneously removed by the same etch:

> In one embodiment, dielectric layer 40 is patterned using a plasma comprising oxygen, and photoresist mask 44 used to define the opening within dielectric layer 40 is removed at the same time that dielectric layer 40 is etched. Therefore, in this embodiment the etch process used to pattern dielectric layer 40 also simultaneously removes some or all of the photoresist mask 44 used to define the opening within dielectric layer 40.

Boeck at 6:19–26; *see also* 5:56–65.

51. *Higashikawa* explains that photoresist and carbon-based materials (e.g., organic materials) are simultaneous removed by the same etch:

> Using the pattern of resist layer 4 as an etching mask, mask material layer 3 is patterned as shown in FIG. 1(a). Subsequently, using mask material layer 3 as an etching mask, organic material layer 2 is etched off anisotropically and resist layer 4 is removed as shown in FIG. l(b).

Higashikawa at 1:30–35, Figs. 1(a), 1(b).

52. *Wolf & Tauber* explain why this concurrent removal occurs when carbon is present in both materials (i.e., carbon reacts with oxygen to form CO and CO_2):

> Plasmas containing pure oxygen at moderate pressures produce species that attack organic materials to form CO, CO_2, and H_2O as end products. Such oxygen plasmas provide a highly selective method for removing organic materials, since the O_2 plasmas do not etch Si, SiO_2, or Al.

Wolf & Tauber at 564–65.

53. When *Grill* added the statement that "Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12" (*Grill* at 7:64–66), it was not new matter. Not only does the '628 application explicitly state that these layers have similar etch properties,

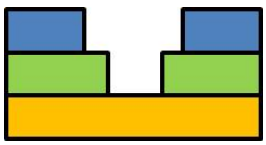
but a person of ordinary skill in the art would have understood this from the basic layer chemistries disclosed by the ’628 application. A person of ordinary skill in the art, therefore, would have understood that the process used to pattern layer 12 (a DLC or FDLC layer) typically removes layer 62 (a photoresist layer). The atypical situations in which layer 62 would not be concurrently removed include, for example, using inorganic photoresists (e.g., chalcogenide glasses), which would have been an unconventional choice, but not one the inventors would have excluded for any particular reason. Just because such unconventional alternatives were possible does not change the fact that a person of ordinary skill in the art reading the ’628 application would have understood that photoresist layer 62 is typically removed concurently with carbon-based layer 12.

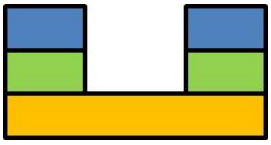
54. It is my opinion that the ’628 application discloses each element of *Grill*’s claim 28.

VII. *Grill*’s Dual-Relief Pattern

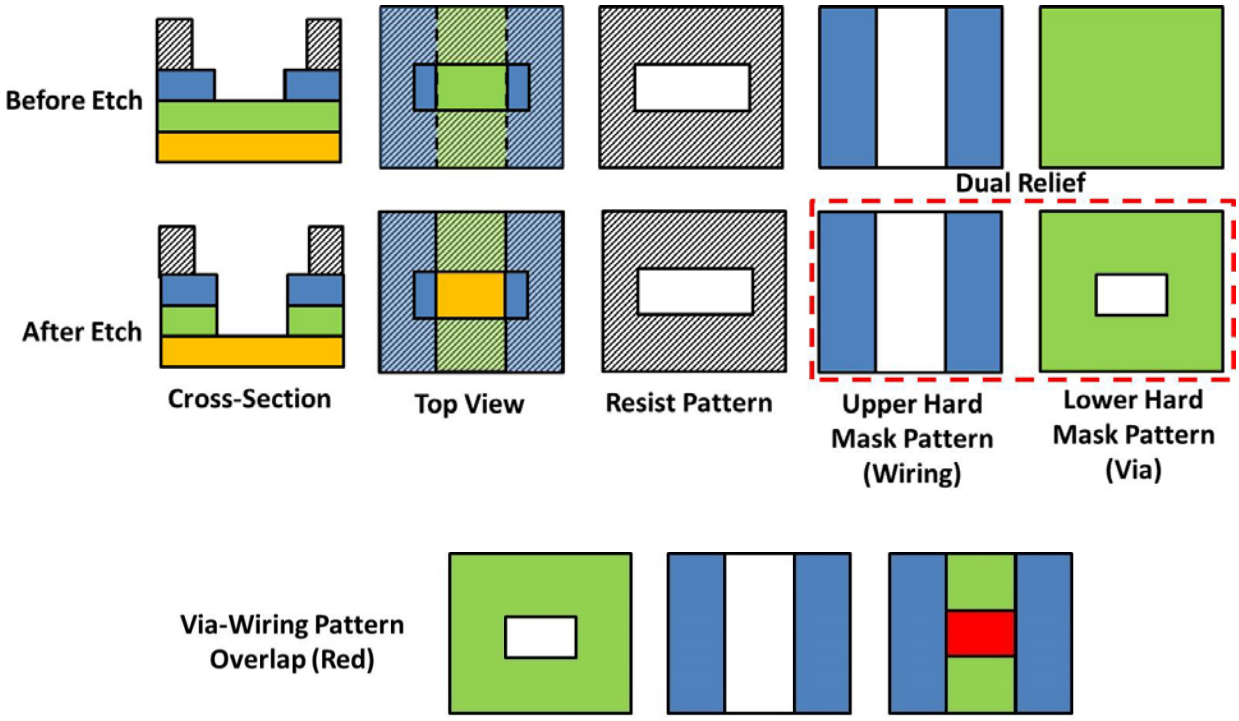
55. I have been asked to provide my opinion whether using *Aoyama*’s via pattern (i.e., a contact pattern wider than the wiring groove to reduce the likelihood of misalignment) eliminates the “dual-relief pattern” *Grill* teaches. In my opinion, it would not. As I explained in paragraph 162 of my declaration dated July 11, 2016, “*Grill*’s and *Aoyama*’s solutions complement one another in addressing the problem of misalignment in semiconductor damascene processes.”

56. *Grill*'s "dual relief pattern" is not limited the way IPB and Dr. Glew suggest. IPB argues that *Grill*'s dual-relief pattern must have the cross-section shown on the left below. But a cross-section like the one on the right below is also a dual relief pattern when the top layer (blue) contains a wiring pattern and the middle layer (green) contains a via pattern. I disagree that using a via pattern wider than the wiring groove, as *Aoyama* teaches, undermines the purpose of the *Grill* process.





57. *Grill* states, "all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern." *Grill* at 7:22–30. In the *Grill-Aoyama* combination I discussed in my declaration dated July 11, 2016, the via pattern substantially (even completely) overlaps the wiring pattern. The illustrations below provide the complete picture a person of ordinary skill in the art would have understood. The dual relief pattern collectively refers to the openings in the blue layer (a wiring pattern) and the green layer (a via pattern).



VIII. The Use of *Aoyama*'s Via Pattern With *Grill*

58. I have been asked to provide my opinion whether using *Aoyama*'s via pattern (i.e., a via pattern that is wider than the wiring groove so as to reduce the likelihood of misalignment) would lead to premature erosion of layer 58 and prevent the *Grill-Aoyama* combination from working. In my opinion, it would not lead to such premature erosion or prevent the *Grill-Aoyama* combination from working.

59. IPB and Dr. Glew misunderstand "selectivity" when they argue silicon dioxide layer 58 is necessarily etched "at a much faster rate" than silicon nitride layer 56 "when both films are exposed to a silicon nitride etch process." Paper 19, at 57–58. This is unequivocally a false statement.

60. A person of ordinary skill in the art would have known many processes for selectively etching silicon nitride relative to silicon dioxide. For example, *Wolf & Tauber* explains that "favorable selectivity [of Si_3N_4 over SiO_2] (e.g. 9–10) can be obtained with the use of NF_3 plasmas." *Wolf & Tauber* at 556. *Chang & Sze* further explain that "Si_3N_4 can be etched anisotropically in an RIE mode with high selectivity to Si and SiO_2 by CHF_3/O_2, CH_2F_2, or CH_3F." *Chang & Sze* at 358. *Brooks* provides etch recipes using combinations of CF_4, O_2, and CH_2F_2 with selectivity ranging as large as 872. *Brooks* at tbls. 3C, 3D, FIG. 4. *Plummer* explains that the etch chemistries discussed by *Chang & Sze* and *Brooks* are "[v]ery anisotropic; selective over Si and SiO_2." *Plummer* at 645. And *Becker* discloses a process by which "nitride 3 is removed at a rate 49 times faster than the oxide 2 is removed" using a combination of CF_4 and CHF_3. *Becker* at 3:42–45; *see also* 3:23–25. These selective etch processes, by definition, etch silicon nitride at a much faster rate (up to 872 times faster) than silicon dioxide. A person of ordinary skill in the art, therefore, would have known that by using any of these well-known processes, *Grill*'s SiO_2 layer 58 would not prematurely degrade while etching Si_3N_4 layer 56.

61. IPB's conclusion that silicon dioxide is necessarily etched "at a much faster rate" than a silicon nitride "when both films are exposed to a silicon nitride

etch process" (Paper 19, at 57–58; EX2009 at ¶ 155) appears to arise from a fundamental misapplication of the definition of etch selectivity.

62. *Plummer* provides a textbook definition of selectivity:

> The selectivity, S, of an etch process between two materials, 1 and 2, is simply the ratio of their etch rates, r, in that etchant, or
>
> $$S = \frac{r_1}{r_2} \qquad (10.4)$$
>
> Material 1 is usually the film being etched, and material 2 is either the masking material (photoresist or perhaps silicon dioxide) or the material below the film. We often speak of an etch process for material 1 having a certain selectivity over (or "with respect to," or just "to") material 2. For a large selectivity ($S >> 1$) we say that the etch process for material 1 has good selectivity over material 2.

Plummer at 613.

63. When *Wolf & Tauber* states, for example, that "[t]he selectivity of a CF_4 isotropic Si_3N_4 etching process with respect to SiO_2 is ~2-3," it means the silicon nitride etches about 2–3 times faster than silicon dioxide, not (as Dr. Glew and IPB stated) that silicon dioxide etches 2–3 times faster than silicon nitride. IPB and Dr. Glew got the definition backwards and cite this statement as evidence that silicon dioxide is necessarily etched "at a much faster rate" than silicon nitride "when both films are exposed to a silicon nitride etch process." Paper 19, at 57–58; EX2009 at ¶ 155. IPB's evidence actually disproves its argument.

64. Dr. Glew and IPB also cite the *Schaepkens* paper, which discusses a process with which "oxide could be etched at a high rate and at the same time selectively to nitride." *Schaepkens* at 2100. This evidence also fails to support IPB's argument. As FIG. 2 (below) from the *Schaepkens* reference shows, this process is designed to etch silicon dioxide selectively with respect to silicon nitride. The oxide is etched at a rate of about 350 to 375 nm/min., whereas the nitride is etched at a rate of about 25 to 50 nm/min. In other words, IPB and Dr. Glew actually cite a selective silicon dioxide etch process (a process designed to etch silicon dioxide faster than silicon nitride) to support their argument that a silicon nitride etch process necessarily etches silicon dioxide faster than silicon nitride. Paper 19, at 57–58; EX2009 at ¶ 155. A person of ordinary skill in the art, however, knew many processes for selectively etching silicon nitride with respect to silicon dioxide, some of which I identified in paragraph 60 above.

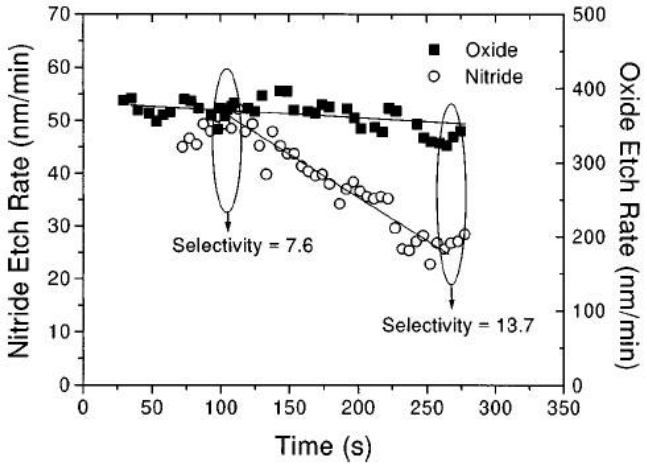


FIG. 2. Nitride etch rate and oxide etch rate as a function of the time that the plasma was switched on (1400 W inductive power, 6 mTorr operating pressure, −100 V self-bias).

65. Even if IPB *were* correct (and it is not) that a silicon nitride etch would prematurely thin layer 58, a person of ordinary skill in the art would have been able to compensate by making layer 58 slightly thicker. I disagree with IPB that "widely varied" and "arbitrary" thickness variations would have resulted here, because the thickness variations are negligible. *Grill*'s hard mask layers are about 20 to 50 nm thick. *Grill* at 8:24–31. *Plummer* provides a simulation of photolithography over a 400 nm step that confirms IPB's argument is irrelevant at these thicknesses. *Plummer* at 270, Figure 5-50. Even with a fairly small etch selectivity of 5 (which is 1–2 orders of magnitude less than the selectivity of the well-known, selective nitride etches discussed above in paragraph 60) and a thick 50 nm upper hard mask, the maximum additional thickness would be 1/5 of 50 nm, i.e. 10 nm, which is trivial in terms of the lithography. Even on a perfectly flat wafer, the "highest degree of thickness uniformity" was about ±10 nm. *Wolf & Tauber* at 432.

IX. *Aoyama*'s Via Pattern Does Not Depend on a Carbon Etch-Stop Layer

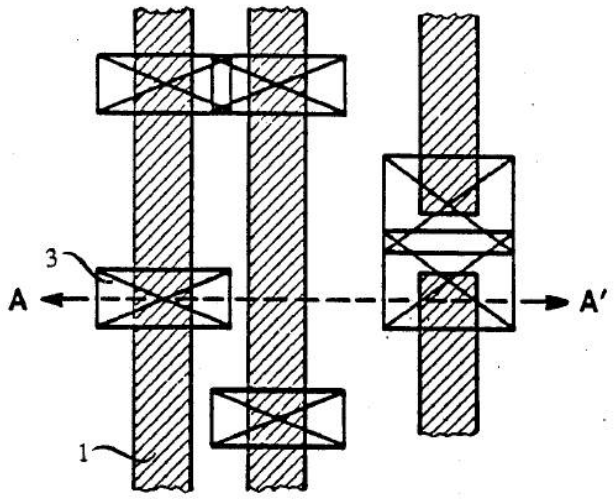
66. I have been asked to provide my opinions whether using *Aoyama*'s via pattern (i.e., a via pattern that is wider than the wiring groove so as to reduce the likelihood of misalignment) depends on a carbon etch-stop layer. In my opinion, it does not. All that is required is that the etch-stop film act as a mask during the via transfer etch.

67. *Aoyama* does not limit its method to using a carbon etch stopper because it defines the etch stopper in terms of its function, not its material. *Aoyama* at 15:60–63. Those of ordinary skill in the art had known for many years how to form vias using patterns wider than the wiring groove. Nothing limited the etch-stop layer to carbon. *Cochran*, for example, describes the same process without identifying a particular material for the etch-stop layer at all:

> It is noted that the windows, as defined in the resist, are oversized along the critical dimensions, and the etch stop layer 29 will provide self alignment during the subsequent window etch, i.e., layer 29 prevents etching of the underlying dielectric material thereby forming self-aligned windows.

Cochran at 2:64–3:45, FIGS. 1–4. All that is required is that the layer provide adequate masking for the via (i.e., "window") etch. This is shown in *Cochran*'s FIG. 1, for example, reproduced below.

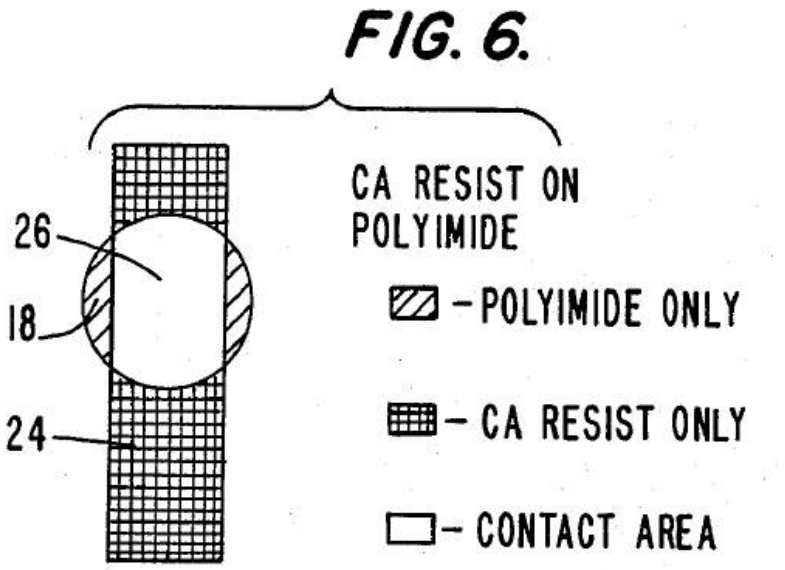
FIG. 1



As another example, *Peterman* uses a polyimide etch-stop layer 18:

> Referring to FIG. 6, since the contact window 26 was etched into the BPSG layer using both the photoresist layer 24 and the polyimide layer 18 as etch masks, the contact through the BPSG layer 16 will coincide precisely with the trench 22 which was previously defined to be the area for the metal interconnect lines. The result is a self-aligned contact to metal line structure.

Peterman, at 3:39–45, FIGS. 5–6. This is shown in *Peterman*'s FIG. 6, reproduced below, which strongly resembles Fig. 36 of the '696 patent.

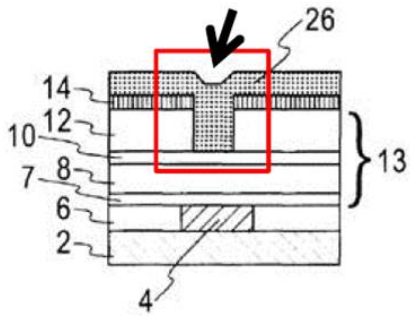
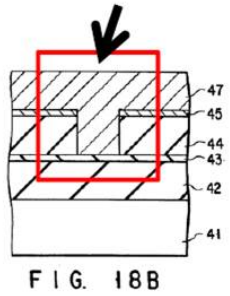


68. *Aoyama*'s method is perfectly suitable to *Grill*'s process, as illustrated in paragraph 227 of my declaration dated July 11, 2016. Comparing *Aoyama*'s structure with and without stopper 45, as IPB does at page 66 of its Response, is irrelevant.

X. *Aoyama*'s Contact Pattern Would Not Have Reduced Critical Dimension Control When Used With *Grill*

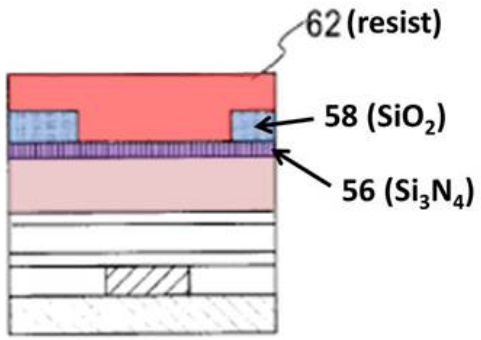
69. I have been asked to provide my opinions whether using *Aoyama*'s via pattern (i.e., a contact pattern that is wider than the wiring groove so as to reduce the likelihood of misalignment) would have reduced critical dimension control when used with *Grill*'s process. I do not believe it would have.

70. IPB makes the following false comparison between *Grill*'s FIG. 2A and a modified version of *Aoyama*'s FIG. 18B. Paper 19, at 72.

Grill (FIG.2A)	Aoyama (FIG.18B-modified)
	 FIG. 18B

71. In both examples above, only one hard mask is used, such that the interlevel dielectric (layer 12 on the left and layer 44 on the right) and the photoresist (layer 26 on the left and layer 47 on the right) come into contact with one another. When the interlevel dielectric has similar etch characteristics to the photoresist layer, any rework due to misalignment during photolithography will damage the interlevel dielectric. In the *Grill-Aoyama* combination, however, this is not an issue because the *Grill-Aoyama* combination uses two hard masks (see

modified FIG. 5D below based on Fig. 5D″ from page 91 of my declaration dated July 11, 2016). The photoresist layer never comes into contact with the interlevel dielectric because the extra hard mask layer 56 provides a barrier between them.



72. The photoresist and interlevel dielectric never come into contact because "the lithographic alignment for both via and wiring levels is completed before any pattern transfer into the underlying interlevel/intralevel dielectric." *Grill* at 2:64–3:1. If the photoresist is misaligned, it is easily stripped for rework because only the silicon dioxide and silicon nitride hard masks are exposed to the photoresist removal chemistry. IPB bases its argument on the notion that the interlevel dielectric would be exposed to the chemistry used to strip the photoresist for rework. This is irrelevant to the *Grill-Aoyama* combination.

73. I also disagree with IPB's suggestion that the step between layer 56 and layer 58 in modified Fig. 5D above "would have created problems for dimensional control" because of "widely varied exposure requirements" between the thicker resist inside the wiring groove and the thinner resist in other areas.

Paper 19 at 72. As explained in paragraph 65 above, interlevel dielectric layer 58 is only about 20 to 50 nm thick. *Grill* at 8:24–31. The photoresist layer would have been about 1,000 to 2,000 nm thick. This is a thickness variation about 1-5%. The example IPB identifies, on the other hand, involves a step in an interlevel dielectric layer that would have been about 300 to 1000 nm thick, which is comparable to the photoresist thickness. *See Zhao* at 6:58–60; *Jain 168* at 3:8–9. This is a thickness variation about 15-50%. IPB's analogy is therefore inappropriate. The small step at issue would not have been an obstacle to combining *Grill* and *Aoyama*.

74. *Plummer* shows a simulation of photolithography over a 400 nm step. *Plummer* at 270, Figure 5-50. In addition, my textbook shows a usable depth of focus (UDOF) of 1.8 μm (1,800 nm), and notes, "At best focus, a relatively large range of exposure variation can be tolerated." EX2019 at 33–34; EX2017 at 25–26. *Plummer* and *Chang & Sze* respectively show UDOF values of 700 nm and 1,000 nm, both of which are much larger than the 20 to 50 nm step size at issue. *Plummer* at 202; *Chang & Sze* at 273. Thus, routine lithography would have been able to accommodate the step between layers 56 and 58 easily in the *Grill-Aoyama* combination. Additionally, a person of ordinary skill in the art would have been familiar with several well-known photolithography enhancement methods, such as optical proximity correction and phase-shift masks, which can accommodate even significant step heights much larger than 50 nm. *Plummer* at 230–34; *Chang & Sze*

at 284–88. In my opinion, a person of ordinary skill in the art would not have been deterred by the small step between layers 56 and 58 in the *Grill-Aoyama* combination.

XI. Certification

75. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

76. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 21st day of July 2017, in Rochester, New York.

Dated: 7/21/17 By: _____
Dr. Bruce Smith, Ph.D.