

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01376
Patent 6,197,696 B1

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company, Ltd. (“Petitioner”) filed a Petition for *inter partes* review of claims 13 and 15 (“the challenged claims”) of U.S. Patent No. 6,197,696 B1 (Ex. 1001, “the ’696 patent”). Paper 2 (“Pet.”). Godo Kaisha IP Bridge 1 (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). Pursuant to our authorization (Paper 7), Petitioner filed a Reply (Paper 9, “Reply”) and Patent Owner filed a Sur-Reply (Paper 10, “Sur-Reply”), directed to the issue of the parties’ respective burdens of production if disputes arise prior to institution as to whether a challenged claim or cited prior art is entitled to the benefit of an earlier priority date.

We have authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition, the Preliminary Response, Petitioner’s Reply, and Patent Owner’s Sur-Reply, and for the reasons explained below, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail on at least one asserted ground with respect to all of the challenged claims. *See* 35 U.S.C. § 314(a). Accordingly, we institute trial as to claims 13 and 15 of the ’696 patent.

A. *Related Proceedings*

The parties indicate that the ’696 patent has been asserted in *Godo Kaisha IP Bridge 1 v. Broadcom Ltd.*, No. 2-16-cv-00134 (E.D. Tex. 2016). Paper 4, 2; Pet. 76. Petitioner has filed three additional petitions challenging claims of the ’696 patent—namely, in IPR2016-01377, IPR2016-01378, and IPR2016-01379. Pet. 74–75; Paper 4, 2–3.

B. The Applied References and Evidence

Petitioner relies on the following references.

Reference	Date	Exhibit
U.S. Patent No. 6,140,226 (“Grill”)	Oct. 31, 2000	Ex. 1005
U.S. Patent No. 5,592,024 (“Aoyama”)	Jan. 7, 1997	Ex. 1018

Petitioner further relies on the Declaration of Bruce W. Smith, Ph.D. (Ex. 1002, “Smith Declaration”).

C. The Asserted Grounds

Petitioner sets forth its challenges to claims 13 and 15 as follows. Pet. 36–74.

Reference(s)	Basis	Claim(s) Challenged
Grill	§ 103	13
Grill and Aoyama	§ 103	13, 15

D. The ’696 Patent

The ’696 patent relates to a “method for forming an interconnection structure in a semiconductor integrated circuit.” Ex. 1001, 1:5–7. According to the ’696 patent, “[a]n object of the present invention is providing a method for forming an interconnection structure in which an insulating film with a low dielectric constant can be formed by an ordinary resist application process.” *Id.* at 3:2–5.

The ’696 patent describes various embodiments of methods of forming an interconnection structure. *Id.* at Abstract. The manufacturing process for a modified example of the sixth embodiment is depicted in Figures 33(a)–(c), 34(a)–(c), and 35(a)–(c). *Id.* at 29:62–32:9.

Figure 33(a) of the '696 patent is reproduced below.

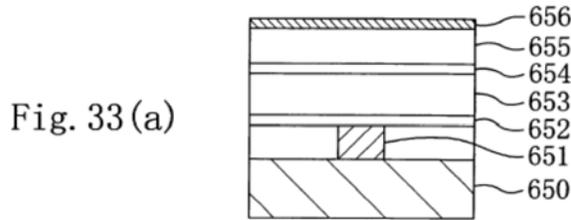


Figure 33(a), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. Ex. 1001, 9:60–63. As seen in Figure 33(a), silicon nitride film 652 is formed over first metal interconnects 651, which are formed on semiconductor substrate 650. *Id.* at 30:1–3. First organic film 653, silicon dioxide film 654, second organic film 655, and titanium nitride film 656 are deposited sequentially. *Id.* at 30:6–16.

Figure 33(b) of the '696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

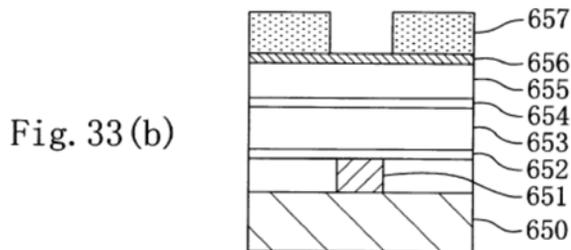


Figure 33(b), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. *Id.* at 9:60–63. In this step, first resist pattern 657 is formed on titanium nitride film 656. *Id.* at 30:36–37. First resist pattern 657 includes openings for forming wiring grooves of the interconnection structure. *Id.*

Figure 33(c) of the '696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

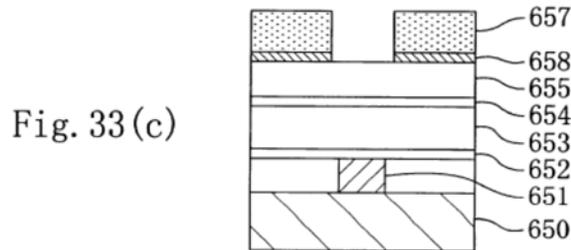


Figure 33(c), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. Ex. 1001, 9:60–63. In this step, titanium nitride film 656 is dry-etched using first resist pattern 657 as a mask, thereby forming mask pattern 658. *Id.* at 30:38–40.

Figure 34(a) of the '696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

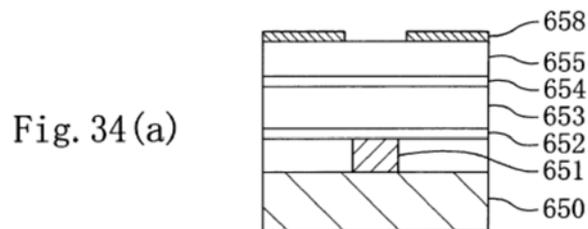


Figure 34(a), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. *Id.* at 9:64–67. In this step, first resist pattern 657 is removed. *Id.* at 30:44–45.

Figure 34(b) of the '696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

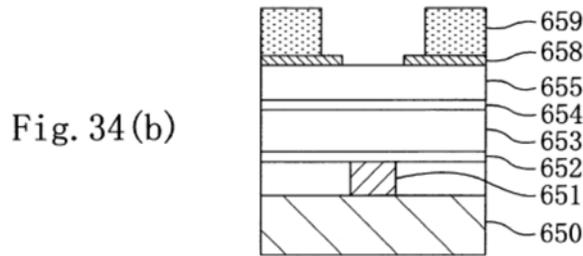


Figure 34(b), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. Ex. 1001, 9:64–67. In this step, second resist pattern 659 is formed on mask pattern 658. *Id.* at 30:49–51. Second resist pattern 659 includes openings for forming contact holes of the interconnection structure. *Id.* In this embodiment, the openings in second resist pattern 659 are larger than the designed size of the contact holes “in respective directions vertical and parallel to the wiring grooves.” *Id.* at 30:51–56.

Figure 34(c) of the '696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

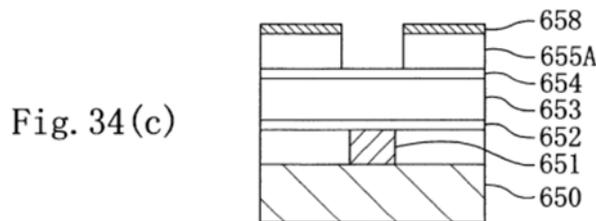


Figure 34(c), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. *Id.* at 9:64–67. In this step, second organic film 655 is dry-etched using both second resist pattern 659 and mask pattern 658 as a mask, thereby forming

patterned second organic film 655A. *Id.* at 30:58–62. In this embodiment, second resist pattern 659 also is removed during this etching. *See id.* at 30:66–31:1.

A three-dimensional depiction of etching using both second resist pattern 659 and mask pattern 658 as a mask is provided in the '696 patent with respect to the modified fifth embodiment in Figure 27(b). Figure 27(b) of the '696 patent is reproduced below.

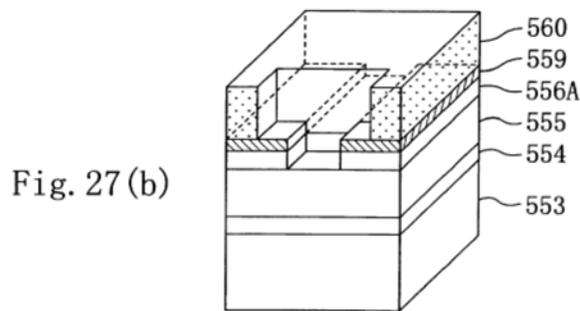


Figure 27(b), reproduced above, is a perspective view of a partially-formed interconnection structure during a process step for forming the same, according to the modified fifth embodiment. Ex. 1001, 9:40–42. Second resist pattern 560 of Figure 27(b) is similar to second resist pattern 659 of Figure 34(b); mask pattern 559 of Figure 27(b) is similar to mask pattern 658 of Figure 34(b); and patterned second silicon dioxide film 556A of Figure 27(b) is similar to patterned second organic film 655A of Figure 34(c). Patterned second organic film 655A (element 556A in Figure 27(b)) is etched only where the openings in the second resist pattern 659 (element 560 in Figure 27(b)) and mask pattern 658 (element 559 in Figure 27(b)) overlap.

According to the '696 patent, using larger openings in second resist pattern 659 allows “openings of the patterned second organic film 655A for

forming contact holes [to] be formed to be self-aligned with the openings of the mask pattern 658 for forming wiring grooves,” “even if the openings of the second resist pattern 659 for forming contact holes have misaligned with the openings of the mask pattern 658 for forming wiring grooves.” *Id.* at 31:54–60. This self-alignment occurs “because the openings of the patterned second organic film 655A for forming contact holes are formed in respective regions where the openings of the second resist pattern 659 for forming contact holes overlap with corresponding openings of the mask pattern 658 for forming wiring grooves.” *Id.* at 31:60–67.

Figure 35(a) of the '696 patent, illustrating a subsequent step in the method of the modified sixth embodiment, is reproduced below.

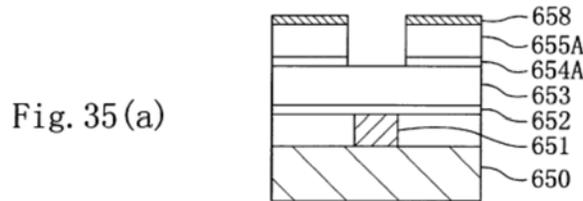


Figure 35(a), reproduced above, is a cross-sectional view of a partially-formed interconnection structure during a process step for forming the same. *Id.* at 10:1–4. In this step, silicon dioxide film 654 is dry-etched using patterned second organic film 655A as a mask, thereby forming patterned second silicon dioxide film 654A. *Id.* at 31:7–10; *see also id.* at Fig. 28(a) (showing a similar step of the modified fifth embodiment).

is dry-etched using patterned first organic film 653A as a mask. *Id.* at 31:19–22. This etching forms patterned silicon dioxide film 654B having wiring grooves and patterned silicon nitride film 652A having contact holes, and also exposes first metal interconnects 651 within contact holes 661. *Id.* at 31:22–26. Then, a metal film is deposited over the surface of the substrate to fill in contact holes 661 and wiring grooves 660, thus forming second metal interconnects 662 and contacts 663. *Id.* at 31:30–44.

E. Illustrative Claim

Of the challenged claims, claim 13 is independent, and claim 15 depends therefrom. Claim 13 of the '696 patent, reproduced below, is illustrative of the challenged claims:

13. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask

pattern, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

Ex. 1001, 34:58–36:10.

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Under the broadest reasonable construction standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic*

Tech., Inc., 504 F.3d 1249, 1257 (Fed. Cir. 2007). The claims, however, “should always be read in light of the specification and teachings in the underlying patent,” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (citations omitted). Further, any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, however, limitations are not to be read from the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Petitioner does not propose an express construction for any limitation, but asserts that the broadest reasonable interpretation should be applied to all claim terms. Pet. 28. Patent Owner proposes express construction for the phrase “using the [first resist pattern [step f]/second resist pattern and the mask pattern [step h]/patterned third insulating film [step i]] as a mask,” which we discuss below. Prelim. Resp. 4–9. No issue in this Decision requires express construction of any other claim terms. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Claim 13 recites etching “using” various layers—for example, first resist pattern [step f]/second resist pattern and the mask pattern [step h]/patterned third insulating film [step i]—“as a mask.” Patent Owner argues that the “broadest reasonable construction of this term in light of the

specification is ‘using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] to define areas for etching.’”

Prelim. Resp. 5.

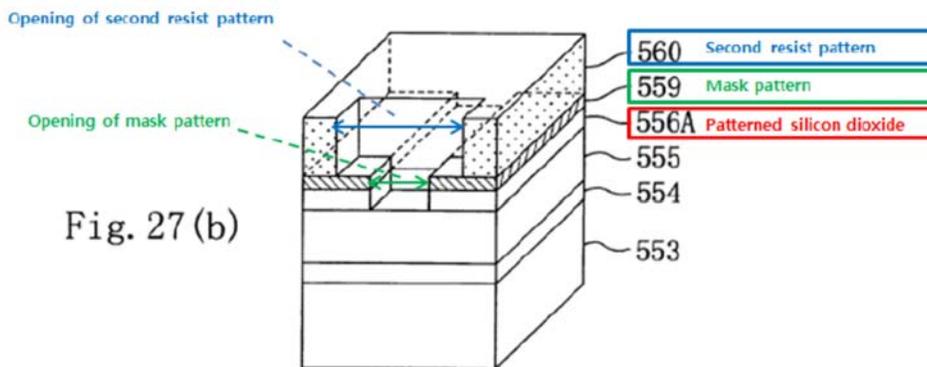
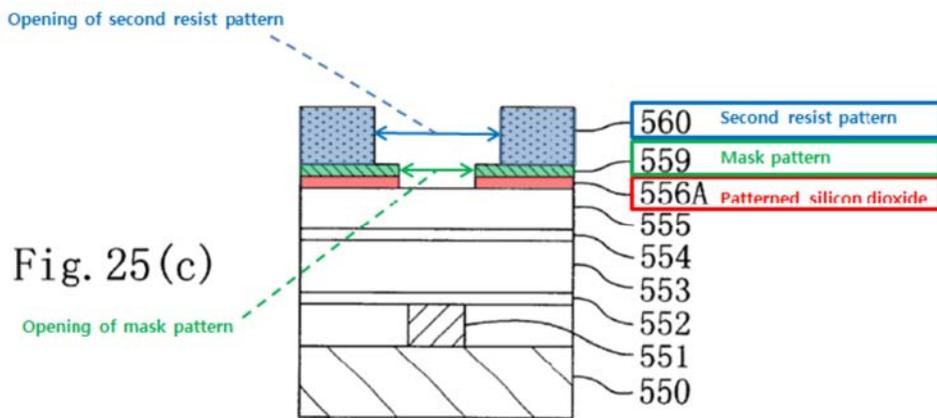
A mask can be used to shield selected areas during an etching process. *See Mask Definition*, MERRIAM-WEBSTER.COM (last accessed Dec. 17, 2016) (Ex. 3001) (2d: “a pattern of opaque material used to shield selected areas of a surface (as of a semiconductor) in deposition or etching (as in producing an integrated circuit)”); *see also* Ex. 2001,¹ 280; Ex. 2002,² 601–02; Ex. 2003,³ 456; Ex. 2004,⁴ 454. The Specification of the ’696 patent includes many examples of various layers being used as masks during etching. For instance, Patent Owner points to an example in “the ’696 patent [that] teaches how both the second resist pattern and the mask pattern are used to define areas for etching: the underlying layer is patterned (etched) where the openings of the resist pattern and the openings of the mask pattern overlap.” Prelim. Resp. 6–7 (citing Ex. 1001, 7:62–8:7, 25:52–57, 26:63–27:3, 27:19–60, 31:60–67, Figs. 25(c), 27(b), 34(b), 37(a), 37(b)). By way of illustration, Patent Owner provides annotated versions of Figures 25(c) and 27(b) of the ’696 patent (*id.* at 7–8), reproduced below.

¹ NEIL SCLATER & JOHN MARKUS, MCGRAW-HILL ELECTRONICS DICTIONARY (6th ed. 1997).

² RUDOLF F. GRAF, MODERN DICTIONARY OF ELECTRONICS (6th ed., 7th prtng. 1992).

³ RUDOLF F. GRAF, MODERN DICTIONARY OF ELECTRONICS (7th ed. 1999).

⁴ STEVEN M. KAPLAN, WILEY ELECTRICAL AND ELECTRONICS ENGINEERING DICTIONARY (2004).



Figures 25(c) and 27(b) are cross-sectional and perspective views, respectively, of a partially-formed interconnection structure during a process step for forming the same, according to an embodiment of the '696 patent. Ex. 1001, 9:32–35, 9:40–42. As described by Patent Owner, “the underlying insulating film (556A) is etched only where the openings of the second resist pattern (560) and the mask pattern (559) overlap, and . . . both the second resist pattern (560) and the mask pattern (559) define the area to be etched.” Prelim. Resp. 7. As further illustration, we provide an annotated version of Figure 27(b) of the '696 patent below.

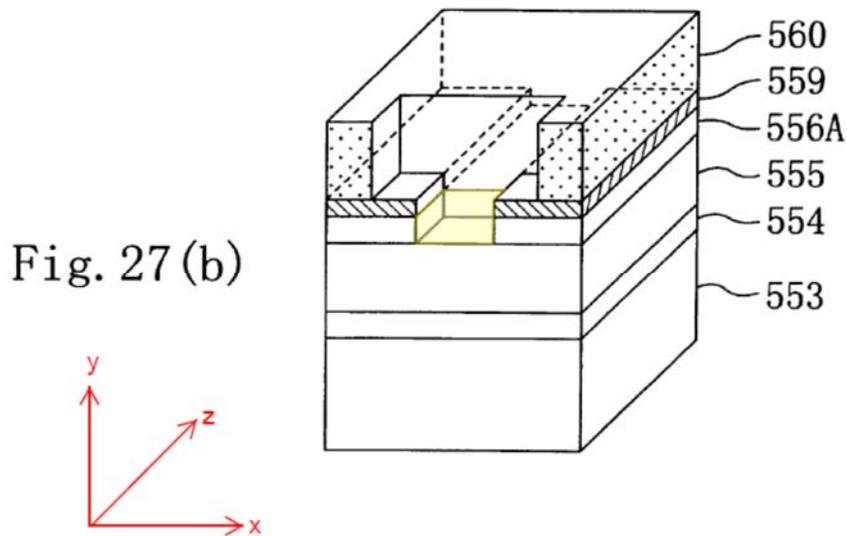


Figure 27(b) is a perspective view of a partially-formed interconnection structure (Ex. 1001, 9:40–42), with the portion of the underlying insulating film that was removed during etching highlighted in yellow and an x-y-z axis added for reference. From the perspective of Figure 27(b), mask pattern 559 defines the areas for etching in the x-axis direction, and second resist pattern 560 defines the areas for etching in the z-axis direction.

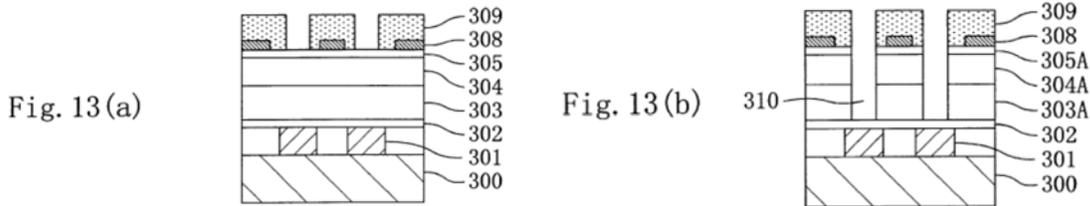
Based on the above, and for purposes of this Decision, we construe “using the [designated layer] as a mask” as proposed by Patent Owner: “using the [designated layer] to define areas for etching.”⁵ For purposes of this Decision, and based on the record now before us, however, we need to discuss further the metes and bounds of this phrase.

We agree with Patent Owner that to meet the limitation “using the [designated layer] for etching,” the designated layer “must actually be *used* to *define areas for etching*.” Prelim. Resp. 6 (emphasis by Patent Owner). For example, we do not consider a mask pattern that is entirely within a

⁵ We note that the district court construed the phrase in the same manner in an Order dated November 9, 2016. Ex. 3002, 20–22.

surrounding resist layer to be “used as a mask” within the meaning of claim 13.

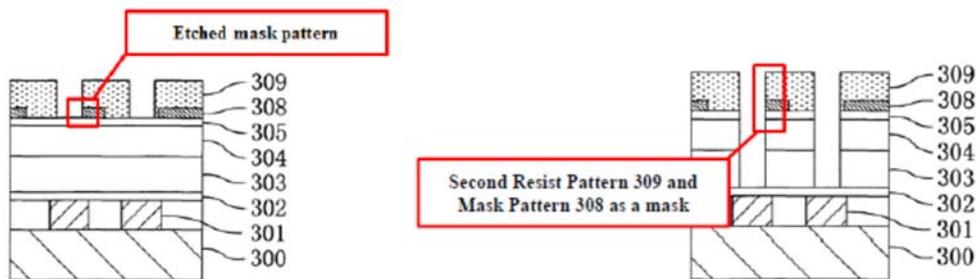
As an illustration, Figures 13(a) and 13(b) of the '696 patent are reproduced below.



Figures 13(a) and 13(b) are cross-sectional views illustrating partially-formed interconnection structures during process steps for forming the same, according to an embodiment of the '696 patent. Ex. 1001, 8:58–60. As described in the '696 patent, layers 303, 304, and 305 of Figure 13(a) are etched “using the second resist pattern 309 as a mask” to form patterned layers 303A, 304A, and 305A of Figure 13(b). *Id.* at 17:20–29. The description does not reference using mask pattern 308 in forming these patterned layers.⁶ Based on a comparison of this disclosure with that discussed above with respect to Figures 25(c) and 27(b), we agree with Patent Owner that a teaching such as that described with respect to Figures 13(a) and 13(b), *without more*, does not mean that the underlying layer (i.e., layer 308 in Figures 13(a) and 13(b)) is “used as a mask” for etching within the meaning of claim 13. *See, e.g.*, Prelim. Resp. 42 (discussing Petitioner’s mapping of Grill to claim 13).

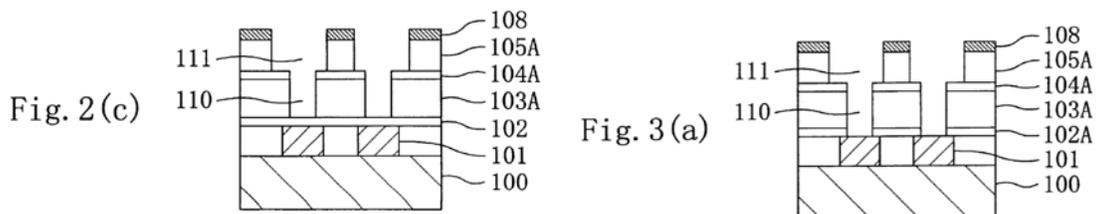
⁶ Mask pattern 308 is used at a subsequent processing step, after removal of second resist pattern 309, as a mask for further etching patterned layer 305A. *See* Ex. 1001, 17:30–35, Fig. 13(c).

We do not agree with Patent Owner’s contention, however, that if an edge of a layer (positioned between an overlying layer and the layer being etched) is “in line and flush with an edge of” the overlying layer, that the overlying layer and the between layer are “both together . . . used to define an area for etching.” See Prelim. Resp. 40. By way of illustration, Patent Owner provides modified and annotated versions of Figure 13(a) of the ’696 patent (*id.* at 14), reproduced below.



The figures, reproduced above, are cross-sectional views illustrating an embodiment of the ’696 patent, as modified by Patent Owner to show the process if second resist pattern 309 has been misaligned when formed. See *id.* at 12–14. According to Patent Owner, “when the underlying third insulating film (305) is thereafter etched, both the second resist pattern (309) **and** the mask pattern (308) necessarily define the areas for etching of the third insulating film (305).” *Id.* at 14.

We disagree. The ’696 patent Specification does not support Patent Owner’s contention in this regard. Illustrative of an example, Figures 2(c) and 3(a) of the ’696 patent are reproduced below.



Figures 2(c) and 3(a) are cross-sectional views illustrating partially-formed interconnection structures during process steps for forming the same, according to an embodiment of the '696 patent. Ex. 1001, 8:14–16. The '696 patent describes the step that occurs between these figures as “the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask.” *Id.* at 11:51–53. Notably, it does not describe using patterned film 104A *and* patterned first organic film 103A as the mask. *See also id.* at 14:41–45 (discussing Figs. 8(a), 8(b)), 16:7–9 (discussing Figs. 10(c), 11(a)), 17:20–24 (discussing Figs. 13(a), 13(b)), 21:33–36 (discussing Figs. 18(c), 19(a)), 21:60–62 (discussing Figs. 19(c), 20(a)).

We, therefore, are not persuaded that a layer, positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer, is “used as a mask” within the meaning of claim 13. Instead, to be “used as a mask,” the between layer would need to define an additional portion of the layer being etched that is to be shielded from etching.⁷ An example of this is described above with respect to Figures 25(c) and 27(b) of the '696 patent.

In summary, for purposes of this Decision, we construe “using the [first resist pattern [step f]/second resist pattern and the mask pattern [step h]/patterned third insulating film [step i]] as a mask” as “using the [first resist pattern [step f]/second resist pattern and the mask pattern

⁷ Our construction does not preclude, for example, a layer positioned between an overlying layer and the layer being etched from acting as a mask, within the meaning of claim 13, in an instance where the overlying layer also is removed during the etching, and thus, the between layer acts to shield the layer being etched during etching.

[step h]/patterned third insulating film [step i]] to define areas for etching.” This construction, however, is further limited, as discussed above.

B. Principles of Law — Obviousness

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic*, 504 F.3d at 1259. The level of ordinary skill in the art may be reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

We analyze the asserted grounds of unpatentability in accordance with those principles.

C. Whether Grill Qualifies as Prior Art

Each of the asserted grounds relies, at least in part, on Grill. *See* Pet. 36–74. Patent Owner argues “Petitioner fails to show in its Petition a

reasonable likelihood of proving that Grill is prior art to the '696 patent.” Prelim. Resp. 9–10; *see id.* at 9–38. We, thus, at the outset determine the prior art status of Grill as to claims 13 and 15 of the '696 patent.

The application that issued as the '696 patent was filed on March 23, 1999. Ex. 1001, at [22]. The '696 patent claims priority to Japanese Application No. 10-079371, filed on March 26, 1998 (“the Japanese priority application”⁸). *Id.* at [30].

Grill was filed on July 30, 1998 and issued on October 31, 2000. Ex. 1005, at [22], [45]. Grill also claims priority to U.S. Provisional Application No. 60/071,628, filed January 16, 1998 (“Grill provisional application”). *Id.* at [60].

Petitioner asserts that “[d]ue to its July 30, 1998, filing date, *Grill* is prior art to the '696 patent under [35 U.S.C.] § 102(e).” Pet. 28. Petitioner argues further that the challenged claims are not entitled to the filing date of the Japanese priority application. *Id.* at 20–27. Patent Owner argues that the '696 patent is entitled to its claimed priority date of March 26, 1998 (Prelim. Resp. 10–19), and that, because Petitioner does not attempt to show in its Petition that Grill is entitled to the priority date of the Grill provisional application, Petitioner cannot rely on the provisional application’s filing date to show that Grill is prior art to the challenged claims (*id.* at 20–26).

The parties dispute also whether Petitioner must show, in its Petition, that the claims of the '696 patent are not entitled to the claimed foreign priority date, or whether the burden is on Patent Owner first to show that the claims of the '696 patent are entitled to the claimed foreign priority date; and

⁸ Petitioner provided a certified translation of the Japanese priority application. Ex. 1014.

whether the Petition must address if the asserted prior art (i.e., Grill) is entitled to the filing date of its provisional application. *See* Paper 7; Reply; Sur-Reply. Because we are persuaded, based on the current record and as discussed below, by Petitioner’s argument that claims 13 and 15 are not entitled to rely on the filing date of the Japanese priority application, we need not address the issue of the parties’ respective burdens for purposes of this Decision.

The ’696 Patent’s Claim to the Japanese Priority Application

“Under [35 U.S.C.] section 119, the claims set forth in a United States application are entitled to the benefit of a foreign priority date if the corresponding foreign application supports the claims in the manner required by section 112, ¶ 1.” *In re Gosteli*, 872 F.2d 1008, 1010 (Fed. Cir. 1989); *see also K & K Jump Start/Chargers, Inc. v. Schumacher Elec. Corp.*, 13 F. App’x 982, 983 (Fed. Cir. 2001) (non-precedential) (“The later filed [U.S.] patent . . . is entitled to the filing date of the earlier filed [foreign] patent . . . if the earlier filed patent meets the written description test of 35 U.S.C. § 112, first paragraph.”).

Petitioner points to several features of independent claim 13 that it contends are not supported in the Japanese priority application. Pet. 21–27. In particular, Petitioner asserts that the embodiments described in the Japanese priority application do not disclose steps (g), (h), or (i) of claim 13. *See id.* Patent Owner argues that each of these features is, in fact, supported in the Japanese priority application. Prelim. Resp. 10–19.

Claim 13, step (g)

Claim 13, step (g) recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

Petitioner argues that the first, second, and fourth embodiments of the Japanese priority application do not disclose step (g) of claim 13, but instead show forming the second resist pattern before removing the first resist pattern. Pet. 21–23. We agree. See Ex. 1014 ¶¶ 34, 43, 50, 68, 107, Figs. 1(c), 5(a), 9(c), 18(c).

As noted by Patent Owner (Prelim. Resp. 11–12), however, the third embodiment and the described variant thereof of the Japanese priority application clearly disclose removing first resist pattern 307 prior to forming second resist pattern 309. Ex. 1014 ¶¶ 79, 93, Figs. 13(a), 16(a). Thus, Petitioner’s argument that the Japanese priority application does not disclose this claim step is not persuasive.

Claim 13, step (h)

Claim 13, step (h) recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

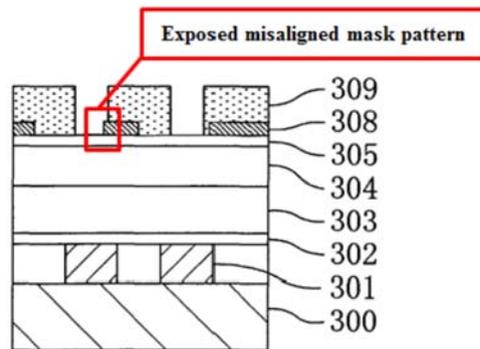
Petitioner argues that the third, variant of the third, and fourth embodiments of the Japanese priority application do not disclose step (h) of claim 13. Pet. 23–25. Because we determine above that the fourth embodiment does not include step (g) of claim 13, we focus our discussion on the third embodiment, and the described variant thereof. See *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998) (“For a claim in a later-filed application to be entitled to the filing date of an earlier application

under 35 U.S.C. § 120 (1994), the earlier application must comply with the written description requirement of 35 U.S.C. § 112, ¶ 1 (1994). . . . A disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations.” (citing *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1571–72 (Fed. Cir. 1997)); see also *K & K Jump Start*, 13 F. App’x at 984 (“In order for claim 1 of the [U.S.] patent to be entitled to the priority date of the [foreign] application, the test set forth in [*Tronzo*, 156 F.3d at 1158] must be satisfied.”).

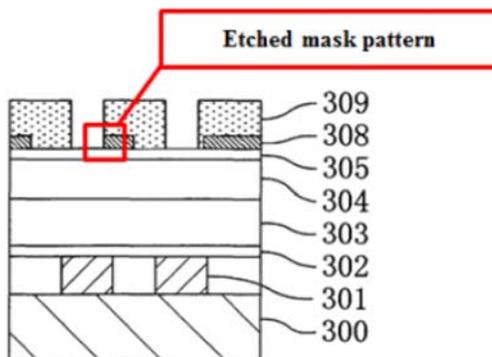
Patent Owner’s argument that this claim step is disclosed in the Japanese priority application is as follows:

For example, the [Japanese priority] application discloses that the second resist pattern may be misaligned during fabrication. To address this misalignment, the underlying mask pattern is etched using the second resist pattern as a mask. As an effect of such etching, edges of the second resist pattern line up and become flush with the edges of the mask pattern. Accordingly, when the underlying third insulating film is subsequently patterned, both the second resist pattern and the mask pattern together define areas for the patterning—*i.e.*, they are both “used . . . as a mask,” as claimed.

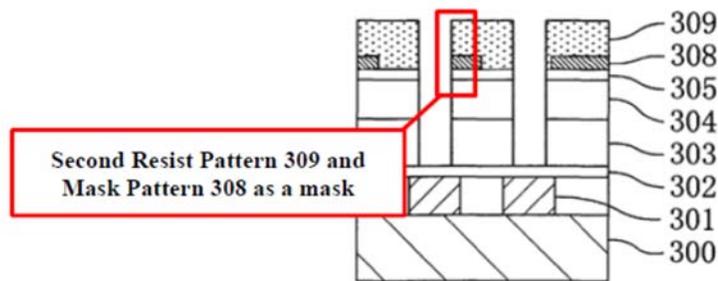
Prelim. Resp. 12; see Ex. 1014 ¶¶ 81, 96. Patent Owner provides a series of illustrations to support this point. Prelim. Resp. 13–14. First, Patent Owner includes a modified version of Figure 13(a) of the Japanese priority application, reproduced below.



According to Patent Owner, the above figure “shows the state of the layers ‘if the mask pattern 308 is exposed to the openings of the second resist pattern 309 for the formation of contact holes because of the misalignment.’” *Id.* at 13 (citing Ex. 1014 ¶ 81). Patent Owner then provides another modified version of Figure 13(a) of the Japanese priority application, reproduced below.



According to Patent Owner, the above figure “shows the layers after ‘the mask pattern 308 is dry-etched using the second resist pattern 309 as a mask.’” *Id.* (citing Ex. 1014 ¶ 81). Patent Owner further includes a modified version of Figure 13(b) of the Japanese priority application, reproduced below.



According to Patent Owner, the above figure “shows that, when the underlying third insulating film (305) is thereafter etched, both the second resist pattern (309) *and* the mask pattern (308) necessarily define the areas for etching of the third insulating film (305).” *Id.* at 14 (citing Ex. 1014 ¶ 79).

Patent Owner’s arguments in this regard are premised on its proposed construction of “using the [designated layer] as a mask,” in which, given a structure having a layer positioned between an overlying layer and the layer being etched that is “in line and flush with an edge of” the overlying layer, the overlying layer and the between layer are both “used as a mask.” For the reasons discussed above, we do not adopt this aspect of Patent Owner’s claim construction. *See supra* Section II.A. Based on our construction of “using the [designated layer] as a mask,” the disclosure relied upon by Patent Owner discloses only using second resist pattern 309 as a mask for etching third insulating film 305. Ex. 1014 ¶ 79 (films 305, 304, and 303 are “sequentially dry-etched using the second resist pattern 309 as a mask”). The cited disclosure does not teach using mask pattern 308 as a mask for etching third insulating film 305, which would be required to show support for step (h) of claim 13 (“dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask”).

Claim 13, step (i)

Claim 13, step (i) recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.” Petitioner argues that the third, variant of the third, and fourth embodiments of the Japanese priority application do not disclose step (i) of claim 13. Pet. 25–27. Patent Owner argues this claim step is disclosed in the third embodiment, and variant thereof, of the Japanese priority application. Prelim. Resp. 16–19. Because we determine above, that the Japanese priority application does not disclose step (h) of claim 13, we need not address the teachings of the Japanese priority application with respect to step (i) for purposes of this Decision.

Conclusion

Based on the record now before us, we determine that, at least, step (h) of claim 13 is not supported by the Japanese priority application. Accordingly, we are persuaded that Grill is available as prior art as to claims 13 and 15 of the '696 patent.

D. Obviousness in View of Grill

Petitioner asserts that claim 13 is unpatentable under 35 U.S.C. § 103 as obvious in view of Grill. Pet. 36–52. In its Preliminary Response, Patent Owner argues that Grill is missing certain features of claim 13.⁹ Prelim. Resp. 38–48. We have reviewed the parties' contentions and supporting

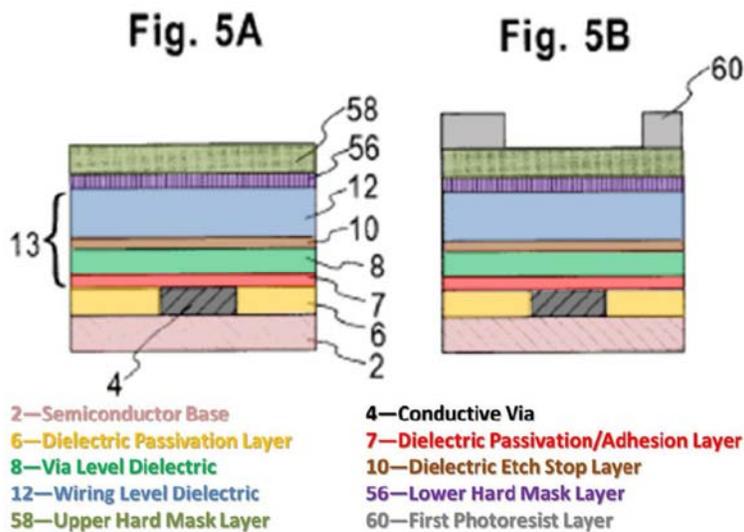
⁹ Patent Owner also argues that Grill is not available as prior art as to the '696 patent claims (Prelim. Resp. 9–38), which we have addressed above and determined that, based on the record now before us, Grill is available as prior art as to the challenged claims (*see supra* Section II.C).

evidence in the current record, and, for the reasons explained below, determine that the information presented does not show a reasonable likelihood that Petitioner would prevail on this asserted ground.

1. Summary of Grill

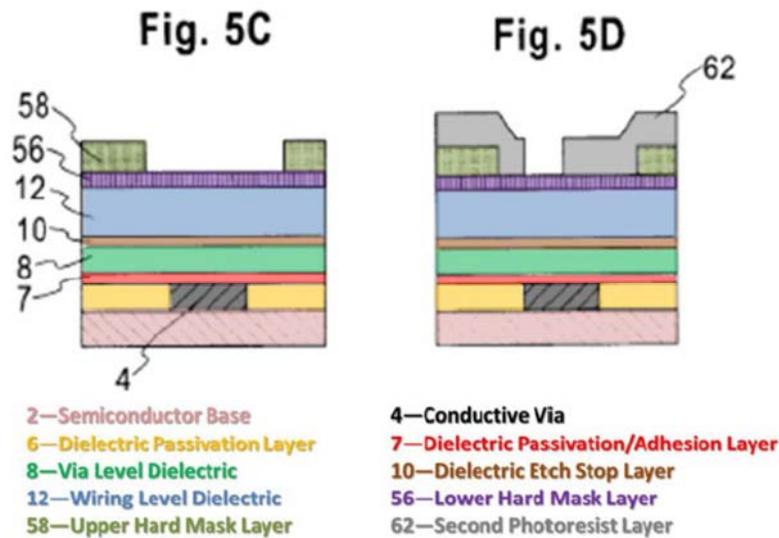
Grill relates to “lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process.” Ex. 1005, Abstract.

Grill describes various embodiments; one exemplary embodiment is depicted in Figures 5A–5H and 1J–1L. Petitioner provides annotated and colored versions of Figures 5A and 5B of Grill (Pet. 30), reproduced below.



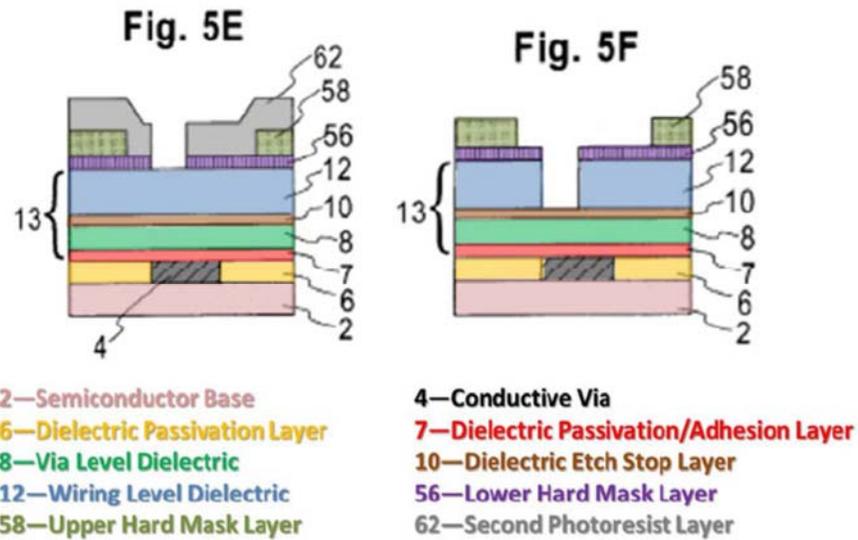
Petitioner’s annotated versions of Figures 5A and 5B of Grill, reproduced above, show cross-sectional views of partially-formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The structure of Figure 5A is formed, and then first photoresist layer 60 is formed and patterned, as shown in Figure 5B. *Id.* at 7:30–44.

Petitioner provides annotated and colored versions of Figures 5C and 5D of Grill (Pet. 31), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



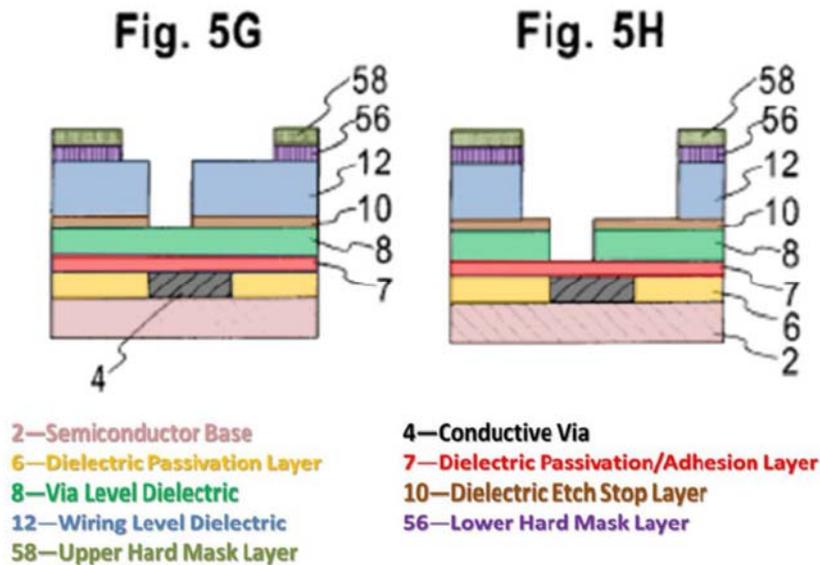
Petitioner's annotated versions of Figures 5C and 5D of Grill, reproduced above, show cross-sectional views of partially-formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The pattern of photoresist pattern 60 is transferred into upper hard mask layer 58, as shown in Figure 5C. *Id.* at 7:45–50. Pattern 60 is removed and second photoresist layer 62 is formed and patterned, as shown in Figure 5D. *Id.* at 7:51–55.

Petitioner provides annotated and colored versions of Figures 5E and 5F of Grill (Pet. 31), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



Petitioner's annotated versions of Figures 5E and 5F of Grill, reproduced above, show cross-sectional views of partially-formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The pattern of photoresist pattern 62 is transferred into lower hard mask layer 56, as shown in Figure 5E. *Id.* at 7:57–61. The pattern is further transferred to wiring level dielectric layer 12, by an etch that also removes second photoresist layer 62, as shown in Figure 5F. *Id.* at 7:62–66.

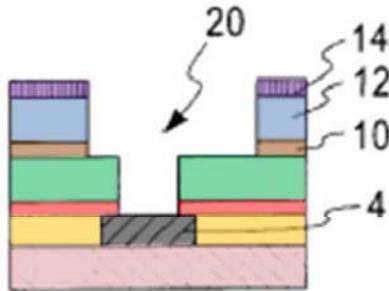
Petitioner provides annotated and colored versions of Figures 5G and 5H of Grill (Pet. 32), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



Petitioner's annotated versions of Figures 5G and 5H of Grill, reproduced above, show cross-sectional views of partially-formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. Exposed portions of lower hard mask layer 56 and etch stop layer 10 are removed by etching, as shown in Figure 5G. *Id.* at 7:67–8:2. A further etch removes exposed portions of dielectric layers 8 and 12, as shown in Figure 5H. *Id.* at 8:2–5.

As noted in Grill, after completion of the step shown in Figure 5H, the structure may be completed as shown in Figures 1J–1L. *See id.* at 8:5–8. A final etch removes the exposed portions of optional dielectric layer 7, which also removes the exposed portions of etch stop 10, as shown in Figure 1J, an annotated and colored version of which is reproduced below (Pet. 32). Ex. 1005, 4:61–64, 8:5–8; Ex. 1002 ¶ 148.

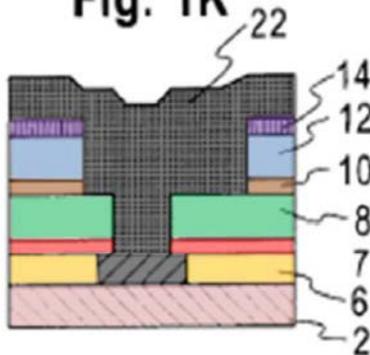
Fig. 1J



- | | |
|---------------------------------------|--|
| 2—Semiconductor Base | 4—Conductive Via |
| 6—Dielectric Passivation Layer | 7—Dielectric Passivation/Adhesion Layer |
| 8—Via Level Dielectric | 10—Dielectric Etch Stop Layer |
| 12—Wiring Level Dielectric | 56—Lower Hard Mask Layer |
| 58—Upper Hard Mask Layer | |

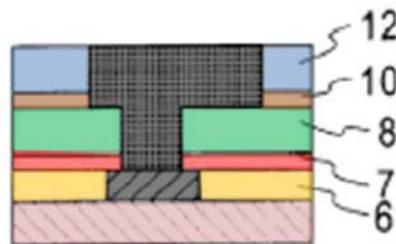
Petitioner's annotated version of Figure 1J, reproduced above, shows a cross-sectional view of a partially-formed structure during one step in a dual damascene process flow. Ex. 1005, 3:33–36. Petitioner provides annotated and colored versions of Figures 1K and 1L of Grill (Pet. 33), which illustrate subsequent steps in the method of this embodiment and are reproduced below.

Fig. 1K



- | |
|---------------------------------------|
| 2—Semiconductor Base |
| 6—Dielectric Passivation Layer |
| 8—Via Level Dielectric |
| 12—Wiring Level Dielectric |
| 22—Wiring Level |

Fig. 1L



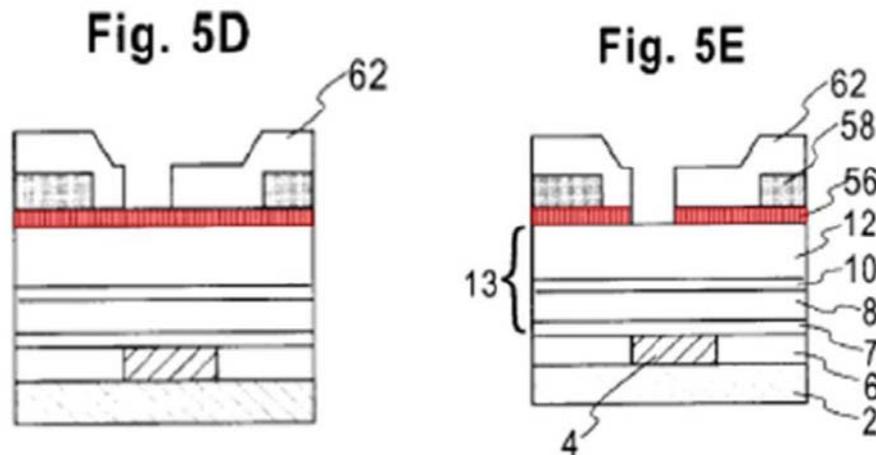
- | |
|--|
| 4—Conductive Via |
| 7—Dielectric Passivation/Adhesion Layer |
| 10—Dielectric Etch Stop Layer |
| 14/56—Hard Mask Layer |

Petitioner’s annotated versions of Figures 1K and 1L, reproduced above, show cross-sectional views of partially-formed structures during process steps in a dual damascene process flow. Ex. 1005, 3:33–36. As seen in Figure 1K, cavity 20 (Fig. 1J) is filled with conductive material 22, as shown in Figure 1K, which is then planarized by a chemical-mechanical polishing process, as shown in Figure 1L. *Id.* at 4:64–5:8, 8:5–8.

2. Analysis

Claim 13 recites, *inter alia*, in step (h) “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

Petitioner relies on Figures 5D and 5E of Grill, and the discussion corresponding thereto, as teaching this claimed feature. Pet. 44–46 (citing Ex. 1005, 7:57–66, Figs. 5D, 5E; Ex. 1002 ¶¶ 193–197; Ex. 1001, 23:42–46, Figs. 22(b), (c)). According to Petitioner, “*Grill* discloses the exact same thing [as Figures 22(b) and 22(c) of the ’696 patent], as highlighted Figures 5D and 5E show.” *Id.* at 45 (citing Ex. 1005, 7:57–66, Figs. 5D, 5E; Ex. 1002 ¶¶ 193–197). Petitioner’s annotated versions of Figures 5D and 5E of Grill (*id.*) are reproduced below.



Petitioner’s annotated versions of Figures 5D and 5E of Grill, reproduced above, show cross-sectional views of partially-formed interconnection structures during process steps for forming the same, according to one embodiment of Grill. Ex. 1005, 3:45–47. Highlighted in red is Grill’s lower hard mask layer 56, which Petitioner maps to claim 13’s third insulating film. See Pet. 44–46.

According to Petitioner, “[a]s Grill’s Figures 5D and 5E show above, and based on the description of the ’696 patent, a [person of ordinary skill in the art] would have understood that the resist layer [62] and the upper hard mask [58] mask the lower hard mask [56] during etching in the manner described in the ’696 patent.” *Id.* at 45 (citing Ex. 1002 ¶¶ 193–97) (brackets by Petitioner).

Based on our construction of “using [a designated layer] as a mask” (*see supra* Section II.A), however, we disagree that this cited portion of Grill teaches “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask,” as recited in claim 13.

As noted by Patent Owner (Prelim. Resp. 38–40), there simply is no disclosure in Grill of using both the second resist pattern and the mask

pattern as a mask. The discussion in Grill corresponding to Figures 5D and 5E states only that “[t]he pattern of resist layer 62 [the alleged second resist pattern] is then transferred into lower hard mask layer 56 [the alleged third insulating film].” *Id.* at 38 (quoting Ex. 1005, 7:57–58 (modifications by Patent Owner)). The discussion in the ’696 patent corresponding to Figures 22(b) and 22(c), on the other hand, describes expressly that “the second silicon dioxide film 506 is dry-etched using the second resist pattern 510 *and the mask pattern 509* as a mask.” Ex. 1001, 23:42–44 (emphasis added).

We agree with Patent Owner that Figures 5D and 5E of Grill, without any further disclosure in the discussion regarding upper hard mask 58 being used as a mask for etching lower hard mask 56, do not disclose “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask,” simply because they look similar to Figures 22(b) and 22(c) of the ’696 patent.

For the reasons discussed, we are not persuaded that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that Grill renders claim 13 obvious.

E. Obviousness in View of Grill and Aoyama

Petitioner asserts that claims 13 and 15 are unpatentable under 35 U.S.C. § 103 as obvious in view of the combination of Grill and Aoyama. Pet. 52–74. In its Preliminary Response, Patent Owner argues that Grill is missing certain features of claim 13, and that one of ordinary skill in the art would not have combined the references in the manner asserted by Petitioner. Prelim. Resp. 46–53. We have reviewed the parties’ contentions and supporting evidence in the current record, and, for the reasons explained

below, determine that the information presented shows a reasonable likelihood that Petitioner would prevail on this asserted ground.

1. Summary of Aoyama

Aoyama teaches a dual damascene process in which the opening in a via resist pattern is wider than the wiring groove. Ex. 1018, 15:48–51, 16:3–5, Figs. 18A–18C, 19A–19B. Petitioner’s annotated versions of Figures 18B, 19A, and 19B of Aoyama (Pet. 36) are reproduced below.

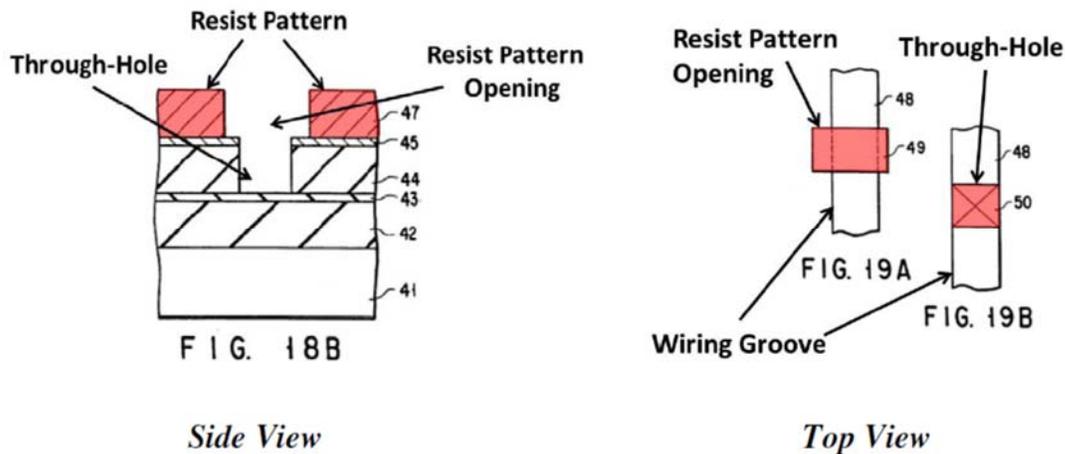


Figure 18A is a cross-sectional view of an intermediate structure formed at a process step for forming a through-hole according to an embodiment of Aoyama. Ex. 1018, 8:42–45. Figures 19A and 19B are plan views of the embodiment of Figure 18A. *Id.* at 8:46–48. As is highlighted in Petitioner’s annotated figures, opening 49 in resist pattern 47 for forming through-hole 50 is wider than the wiring groove 48. *Id.* at 16:3–8, Figs. 18B, 19A. According to Aoyama, this allows the through-hole to be formed having the same width as the wiring groove, even if resist pattern 47 is misaligned. *Id.* at 16:14–16, Fig. 19B.

2. *Analysis*

Claim 13

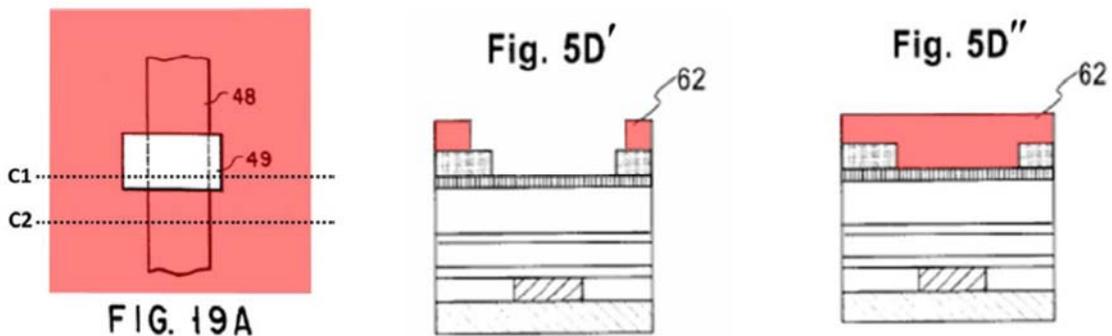
Claim 13 recites a “method for forming an interconnection structure.” Grill is titled “Dual Damascene Processing for Semiconductor Chip Interconnects,” and discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” Pet. 37 (citing Ex. 1005, at [54], Abstract); *id.* at 57. The following table provides a basic summary of Petitioner’s mapping of the combination of Grill and Aoyama to the physical elements of claim 13.

Claim 13	Grill & Aoyama
lower-level interconnects	conductive via 4 of Grill
first insulating film	dielectric etch stop layer 10 of Grill
second insulating film	wiring level dielectric 12 of Grill
third insulating film	lower hard mask layer 56 of Grill
thin film	upper hard mask layer 58 of Grill
mask pattern	patterned upper hard layer 58 of Grill
first resist pattern	patterned first resist layer 60 of Grill
second resist pattern	patterned second resist layer 62 of Grill, as modified by Aoyama’s teachings
contact holes	cavity 20 of Grill (holes in etch stop 10 and via level dielectric 8), as modified by Aoyama’s teachings
wiring grooves	cavity 20 of Grill (holes in lower hard mask 56 and wiring level dielectric 12), as modified by Aoyama’s teachings

Claim 13	Grill & Aoyama
upper-level metal interconnects	conductive wiring material 22 of Grill
contacts	conductive wiring material 22 of Grill

See Pet. 37–43, 45–46, 49–51, 57–70 (citing Ex. 1005, 1:25–27, 3:60–4:13, 4:64–5:8, 7:30–55, 7:62–8:8, 8:29–31, Figs. 1K, 1L, 5A–5H; Ex. 1018, 16:18–21, Fig. 19A; Ex. 1002 ¶¶ 169–89, 195–96, 203, 206–07, 215, 217–23, 225–27, 231–32, 236–37, 241–43, 245). Petitioner also cites to evidence in the record that the combination of Grill and Aoyama teaches each of the method steps recited in claim 13. See *id.*

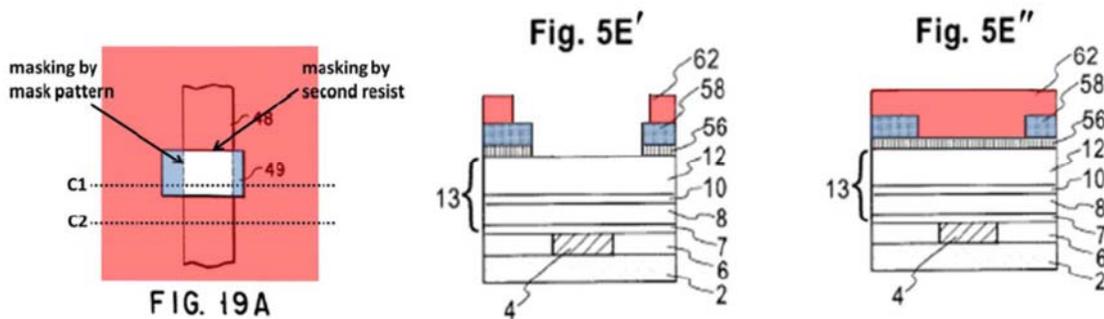
Further, Petitioner describes exactly how a person of ordinary skill in the art would have modified Grill based on the teachings of Aoyama. See Pet. 59–70. Petitioner’s modified and annotated versions of Figure 19A of Aoyama and Figure 5D of Grill (*id.* at 61) are reproduced below.



Petitioner’s annotated version of Figure 19A of Aoyama, reproduced above, shows the shape of Aoyama’s through-hole, viewed from above. *Id.* at 60. Petitioner’s annotated versions of Figure 5D of Grill, reproduced above, are cross-sectional views of a partially-formed interconnection structure at a step in a method of forming the same, according to one embodiment of Grill, as

modified by Aoyama, along line C1 of Figure 19A (Fig. 5D') and along line C2 of Figure 19A (Fig. 5D''). *Id.* (citing Ex. 1002 ¶ 221).

In Petitioner's proposed modification, second resist layer 62 of Grill is modified to have a through-hole shaped as taught by Aoyama. *Id.* (citing Ex. 1002 ¶¶ 220–21; Ex. 1018, 16:18–21). According to Petitioner, when lower hard mask layer 56 of Grill is etched, in the Grill-Aoyama combination, a person of ordinary skill would have understood that second resist pattern 62 and mask pattern 58 are used as masks, thus meeting the limitations recited in step (h) of claim 13. *Id.* at 62 (citing Ex. 1002 ¶¶ 226–27). As illustration, Petitioner provides modified and annotated versions of Figure 19A of Aoyama and Figure 5E of Grill (*id.*), which are reproduced below.



Petitioner's annotated version of Figure 19A of Aoyama, reproduced above, shows the shape of Aoyama's through-hole, viewed from above, with red areas indicating photoresist (i.e., second resist pattern 62) and blue areas indicating a layer corresponding to mask pattern 58 of Grill. Pet. 62.

Petitioner's annotated versions of Figure 5E of Grill, reproduced above, are cross-sectional views of a partially-formed interconnection structure at a step in a method of forming the same, according to one embodiment of Grill, as

modified by Aoyama, along line C1 of Figure 19A (Fig. 5E') and along line C2 of Figure 19A (Fig. 5E''). *Id.* (citing Ex. 1002 ¶ 227).

Based on the record now before us, we are persuaded by Petitioner's showing that its proposed combination of Grill and Aoyama teaches using both patterned second resist layer 62 of Grill as modified by the teachings of Aoyama (i.e., the claimed second resist pattern) and patterned upper hard layer 58 (i.e., the claimed mask pattern) as a mask for etching lower hard mask layer 56 (i.e., the claimed third insulating film), as required by claim 13, step (h).

We also are persuaded, based on the record now before us, that Petitioner has shown sufficiently that all of the other recited method steps of claim 13 are taught by the combination of Grill and Aoyama. *See* Pet. 37–43, 45–46, 49–51, 57–70. We address in more detail, below, Petitioner's reasons for combining the references, and Patent Owner's arguments presented in the Preliminary Response.

Reasons to Combine Grill and Aoyama

Petitioner asserts that both Grill and Aoyama relate to problems involving misalignment of masks during interconnect formation. *See* Pet. 52–55. In particular, according to Petitioner, Grill addresses the problem of “lithographic rework” required when misalignment between the via and wiring patterns occurs. *Id.* at 52–53 (citing Ex. 1005, 2:26–38). Such rework can cause damage to the underlying dielectric. *Id.* at 53 (citing Ex. 1005, 2:26–32). Grill addresses this problem using two hard masks on top of the wiring-level dielectric, which allows lithographic alignment for both via and wiring levels to be completed and the patterns transferred

before the underlying inter-level dielectrics are exposed. *Id.* (citing Ex. 1005, 2:64–3:6, Fig. 5A).

Further, according to Petitioner, “*Aoyama* explains that misalignment of the photomask during via formation can cause the via dimensions to be too small and the wiring dimensions to be too large,” which is undesired. *Id.* at 53–54 (citing Ex. 1018, 3:18–21, 3:29–38, 6:7–14, Figs. 5B, 5D).

Aoyama addresses this problem by “using a resist pattern having a via opening that is wider than the wiring groove.” *Id.* at 54 (citing Ex. 1018, 16:3–5, Figs. 18B, 19A). Using this wider resist pattern “increases misalignment tolerance.” *Id.* (citing Ex. 1018, 16:14–16).

Petitioner argues that a person of ordinary skill in the art “would have appreciated that *Grill*’s and *Aoyama*’s solutions complement one another in addressing the problem of misalignment in semiconductor damascene processes.” *Id.* at 55 (citing Ex. 1002 ¶ 162). Specifically, Petitioner asserts that “[w]hen misalignment occurs, *Grill*’s structure permits lithographic rework without damaging the interlevel dielectrics below” (*id.* (citing Ex. 1005, 2:26–38; Ex. 1002 ¶ 162)) and “[t]he wider via pattern of *Aoyama* reduces instances of misalignment, preventing the time-consuming, inefficient, and costly process of photolithographic rework” (*id.* (citing Ex. 1002 ¶ 162)).

Petitioner provides testimony of Dr. Smith that a person of ordinary skill in the art “would have found it obvious that combining *Grill*’s two hard masks with *Aoyama*’s widened via pattern would not require modification of the *Grill* process” (Ex. 1002 ¶ 163) and “would have understood that the combination of *Aoyama* and *Grill* predictably reduces instances of

misalignment and permits lithographic rework when misalignment does occur” (Ex. 1002 ¶ 164). *See* Pet. 56.

Patent Owner argues that Petitioner has not demonstrated that it would have been obvious to combine Grill and Aoyama. Prelim. Resp. 48–53. In particular, Patent Owner argues that “Petitioner’s selective citations from Grill and Aoyama ignore aspects of Aoyama that *would* interfere with at least one of Grill’s contemplated approaches for addressing misalignment: controlling critical dimension and reducing damage to carbon based layers during rework.” *Id.* at 48–49. We have reviewed Patent Owner’s arguments in this regard, and based on the record now before us, do not find them persuasive.

Patent Owner identifies two problems described in Grill, which Petitioner allegedly does not address with respect to its proposed combination of Grill and Aoyama. *See id.* at 49–53. However, both issues that Patent Owner references (i.e., those illustrated in Figures 2A and 2C of Grill) relate to problems that Grill describes with respect to the prior art process upon which Grill purports to improve. *See* Ex. 1005, 3:33–39, 5:9–33. The embodiment of Grill upon which Petitioner relies (described with respect to Figures 5A–5H of Grill), purports to solve the problems described in Figures 2A and 2C by use of the use of hard mask layers 56 and 58. *See id.* at 7:16–61 (discussing that resist rework “presents no problem” due to hard mask layers 56 and 58). Further, Petitioner provides testimony that “nothing about the width of the via pattern in *Aoyama* affects the dual-hard mask structure of *Grill*, and nothing about the dual-hard mask structure of *Grill* affects the width of the via pattern in *Aoyama*.” Ex. 1002 ¶ 163; *see* Pet. 56.

Based on the record now before us, we are persuaded that Petitioner has shown sufficiently that one of ordinary skill in the art would have had reason to combine Grill and Aoyama in the manner asserted by Petitioner.

“dry-etching the third insulating film”

Patent Owner argues that Grill does not teach *dry-etching* lower hard mask 56, upon which Petitioner relies as teaching the claimed third insulating film. Prelim. Resp. 46–48. According to Patent Owner, “Petitioner relies solely on the testimony of its declarant, Dr. Smith, to argue a [person of ordinary skill in the art] would have understood that pattern is transferred by dry-etching, as required by step 13(h).” *Id.* at 46 (citing Pet. 45–46). We, however, credit Dr. Smith’s testimony in this regard (*see* Ex. 1002 ¶¶ 42–47, 196), and, based on the record now before us, are persuaded that Petitioner has shown sufficiently that it would have been obvious to use dry-etching to remove lower hard mask 56 of Grill.

Conclusion

Based on the record now before us, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that the combination of Grill and Aoyama renders claim 13 obvious.

Claim 15

Claim 15 depends from claim 13 and further recites that “a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.” Ex. 1001, 36:14–18. Petitioner relies on Aoyama as disclosing this limitation. *See* Pet. 72–74. In

particular, Petitioner asserts that Aoyama teaches that problems caused by misalignment of the photomask during through-hole (via) formation may be solved by using a resist pattern with a through-hole wider than the wiring groove. *Id.* (citing Ex. 1018, 3:18–21, 3:29–38, 6:7–14, 16:3–5, 16:14–16, Figs. 5, 5D, 18B, 19A; Ex. 1002 ¶¶ 248–53).

In its Preliminary Response, Patent Owner does not substantively discuss dependent claim 15, apart from its discussion of independent claim 13.

We determine that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that claim 15 would have been obvious in view of Grill and Aoyama.

III. CONCLUSION

For the foregoing reasons, we institute an *inter partes* review of claims 13 and 15. At this preliminary stage in the proceeding, we have not made a final determination with respect to the patentability of any challenged claim or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 13 and 15 of the U.S. Patent No. 6,197,696 B1 on the following ground:

Claims 13 and 15 under 35 U.S.C. § 103 as obvious in view of Grill and Aoyama;

FURTHER ORDERED that no other ground of unpatentability is authorized for this *inter partes* review; and

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FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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