

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Taiwan Semiconductor Manufacturing Company, Ltd.

Petitioner

v.

Godo Kaisha IP Bridge 1

Patent Owner

Patent No. 6,197,696

Filing Date: March 23, 1999

Issue Date: March 6, 2001

Title: METHOD FOR FORMING INTERCONNECTION STRUCTURE

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*Inter Partes* Review No. IPR2016-01376

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**PETITION FOR *INTER PARTES* REVIEW  
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET SEQ.***

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## **LIST OF EXHIBITS**

- Petition Exhibit 1001: U.S. Patent No. 6,197,696 to Aoi et al.
- Petition Exhibit 1002: Expert Declaration of Dr. Bruce W. Smith, Ph.D.
- Petition Exhibit 1003: U.S. Patent No. 3,617,824 to Shinoda et al.
- Petition Exhibit 1004: U.S. Patent No. 3,838,442 to Humphreys.
- Petition Exhibit 1005: U.S. Patent No. 6,140,226 to Grill et al.
- Petition Exhibit 1006: U.S. Patent No. 5,635,423 to Huang et al.
- Petition Exhibit 1007: U.S. Patent No. 5,741,626 to Jain et al.
- Petition Exhibit 1008: C. Akrouit et al., "A 480-MHz Microprocessor in a  $0.12\mu\text{m}$   $L_{\text{eff}}$  CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998).
- Petition Exhibit 1009: J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting (December 1996).
- Petition Exhibit 1010: U.S. Patent No. 6,100,184 to Zhao et al.
- Petition Exhibit 1011: U.S. Patent No. 6,103,616 to Yu et al.
- Petition Exhibit 1012: File History of U.S. Patent No. 6,197,696 to Aoi et al.
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- Petition Exhibit 1014: Certified Translation of Japanese Patent Application No. 10-079371 to Aoi.
- Petition Exhibit 1015: Japanese Patent Application No. 11-075519 to Aoi.
- Petition Exhibit 1016: Certified Translation of Japanese Patent Application No. 11-075519 to Aoi.
- Petition Exhibit 1017: U.S. Provisional Patent Application No. 60/071,628.

Petition Exhibit 1018: U.S. Patent No. 5,592,024 to Aoyama et al.

## **I. Preliminary Statement**

U.S. Patent No. 6,197,696 (Ex. 1001) is directed to methods for forming integrated circuit “interconnects,” which link components in a microchip. In particular, the ’696 patent is directed to common “dual damascene” processes for forming interconnects.

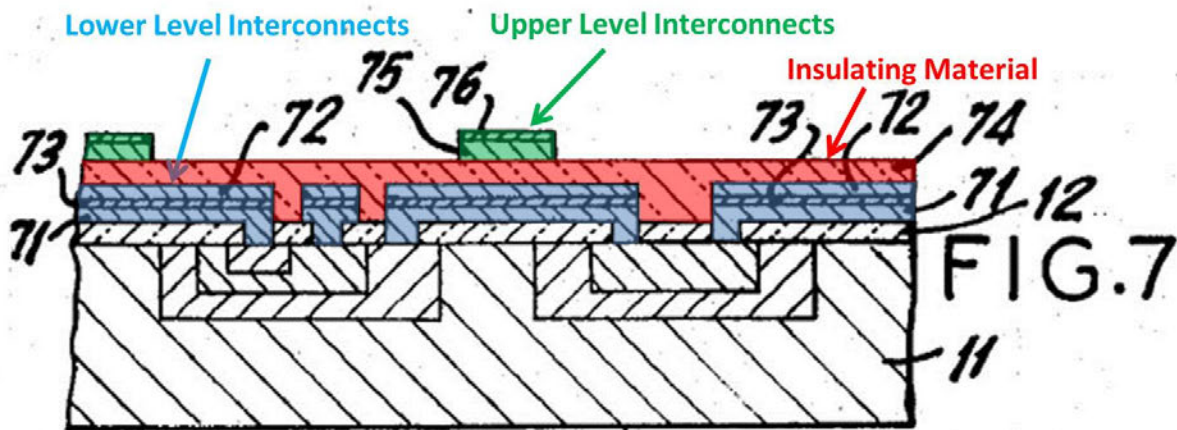
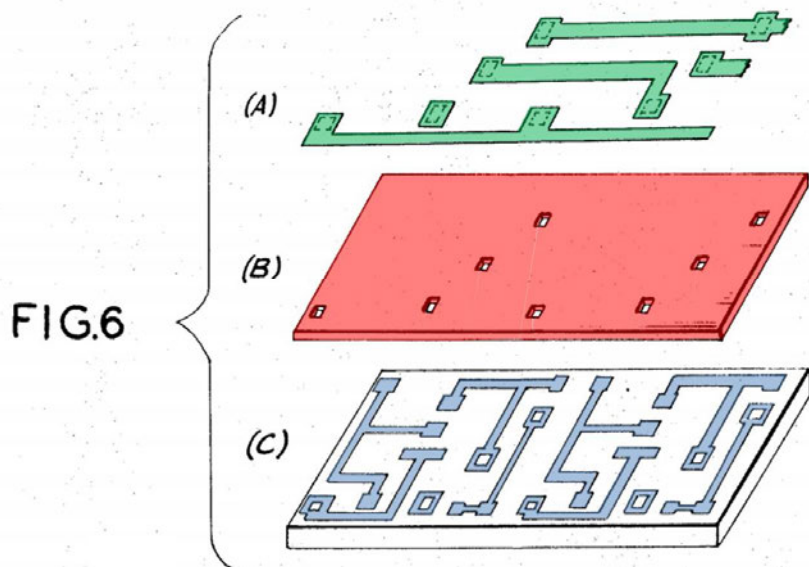
Supported by the Expert Declaration of Bruce Smith, Ph.D., (Ex. 1002), this Petition establishes that challenged claims 13 and 15 are unpatentable. Rather than defining novel or nonobvious subject matter, the challenged claims recite well-known processes for making well-known structures. TSMC respectfully requests *inter partes* review under 35 U.S.C. §§311–319 and 37 C.F.R. §42.100 *et seq.*, and cancellation of the challenged claims.

## **II. Technological Background**

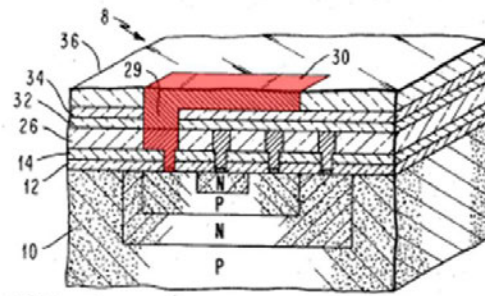
### **A. Integrated Circuits and Interconnections**

Integrated circuits contain millions of discrete semiconductor devices electrically connected by “interconnections,” or “interconnects,” to form circuits. U.S. Patent No. 3,617,824 to Shinoda et al. (Ex. 1003), which dates to 1965, provides an early example. (Ex. 1003, 4:30–73, Figs. 6, 7 (below with highlights and annotations).)

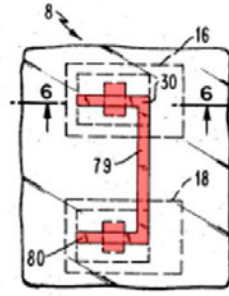




Interconnects typically have “via” portions extending between the planes of adjacent layers to provide electrical connections between those layers. (Ex. 1002, ¶33.) Interconnects also typically have “trench” patterns, which act as wires to define circuits by linking the vias appropriately. These interconnect schemes were common years before the application for the ’696 patent was filed. (See, e.g., Ex. 1004, Abstract, 1:54–2:6, 8:19–54, Figs. 6, 6A (below with highlights), 7, 7A.)



**FIG. 6**



**FIG. 6A**

Multiple levels of interconnects are typical. (Ex. 1002, ¶34.) Examples of this type of wiring scheme, which was also common years before the time the application for the '696 patent was filed, appear below. (Ex. 1008, 1–4, Fig. 2; Ex. 1009, 1–2, Fig. 2; Ex. 1002, ¶34.)

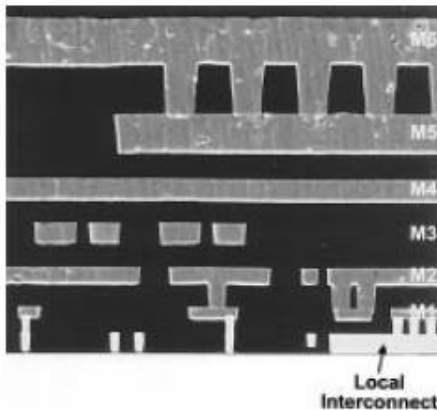


Fig. 2. Scanning electron microscope of six copper metal levels and local interconnect.

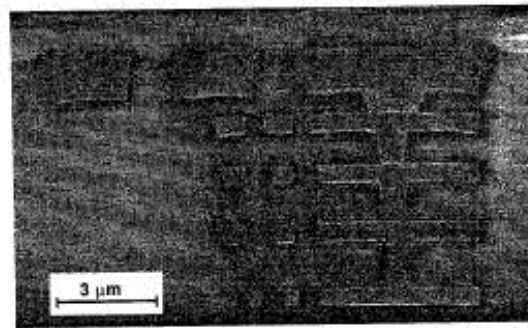
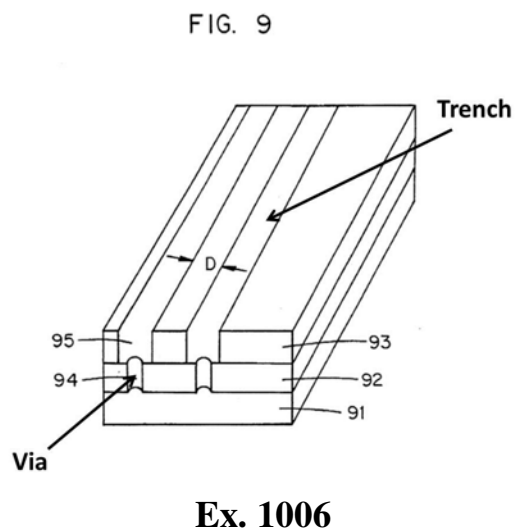
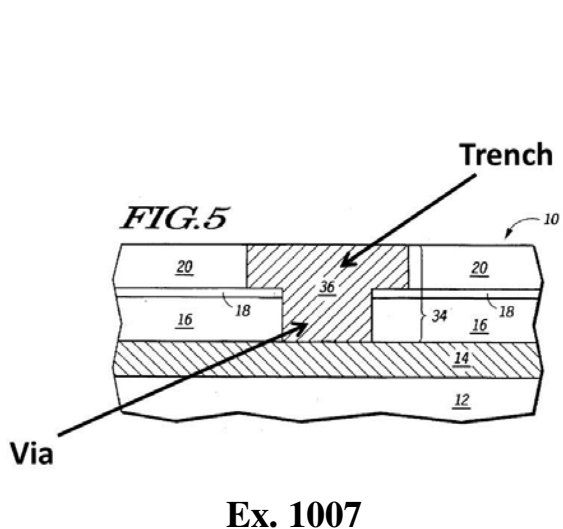
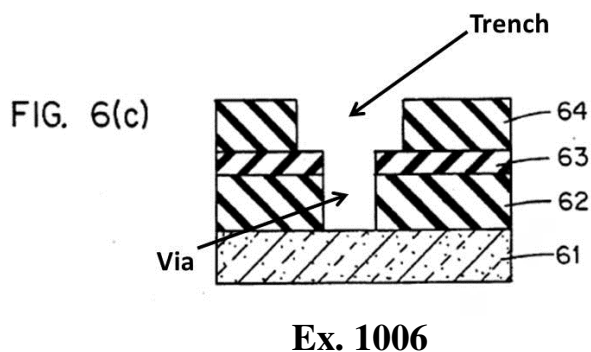
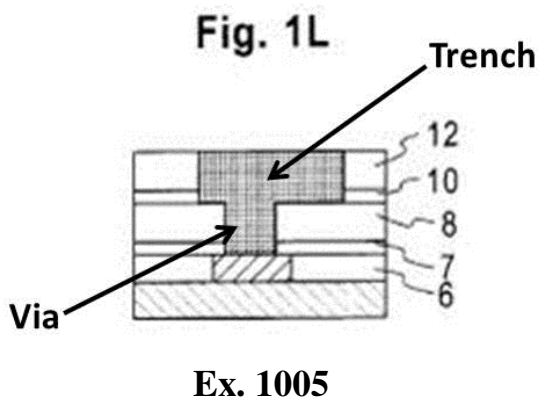


Fig. 2. Cross-sectional SEM of a five-level Cu-damascene interconnect structure with oxide isolation. (Note that the structure is illustrated to demonstrate the VLSI capability of the process; the dimensions of metal layers, vias, and oxide isolation are different from the ones used for the inductor fabrication.)

In a dual damascene process, such the ones as described by the '696 patent, the via and trench structures are formed during the same process. (See Ex. 1009, 1; Ex. 1002, ¶35.) The via and trench patterns are etched into insulating material and then filled with metal and polished flat. (Ex. 1002, ¶35.) Like other interconnect structures, dual damascene processes result in vias that vertically link metallization

levels and trenches that link the vias together horizontally to form circuits. (Ex. 1005, 1:45–48, 3:33–36; Ex. 1006, Abstract, 2:61–3:2, 3:54–57; Ex. 1007, 2:15–20.) Examples appear below with annotations. (Ex. 1005, Fig. 1L; Ex. 1006, Figs. 6(c), 9; Ex. 1007, Fig. 5.)

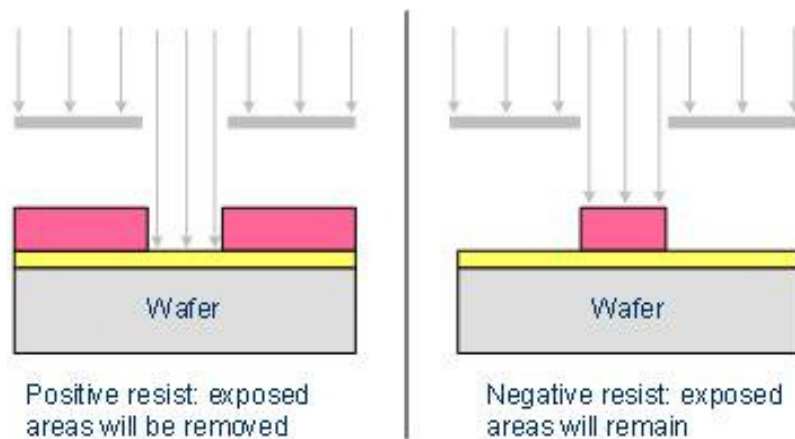


## B. Semiconductor Etching and Photolithography

Two processing technologies that can create patterns in a semiconductor wafer are photolithography and etching. In photolithography, a chemical called photoresist uniformly coats the surface of the semiconductor wafer. (Ex. 1002,

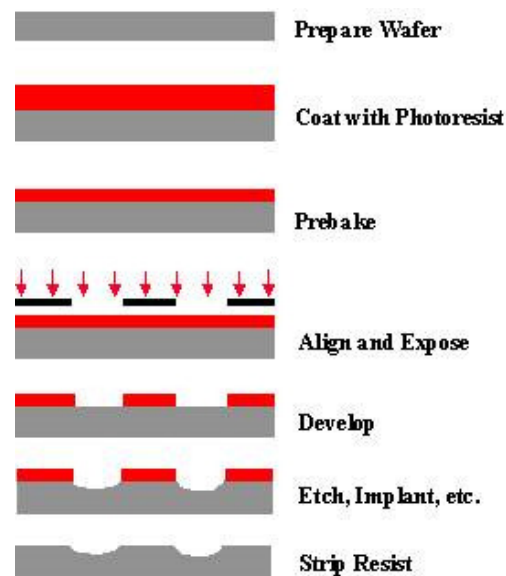
¶37.) Photoresist is sensitive to light and will change its molecular structure when illuminated under the right conditions. (*Id.*) A photomask, which is transparent in some regions and opaque in others, contains a pattern that can be transferred to the photoresist on the surface of the wafer. (*Id.*, ¶38.) After the photomask is aligned, the photoresist is illuminated through the photomask. (*Id.*) The exposed photoresist is altered by the light, and any photoresist not part of the pattern can be removed with a chemical called a “developer.” (*Id.*, ¶39.)

The processed wafer retains the patterned photoresist layer, which can be used to pattern material underneath the photoresist. (*Id.*, ¶39.) Schematic representations of photolithography appear below. (*Id.*, ¶40.)



A patterned photoresist layer can serve as a mask during an “etch” process. In etching, the surface of the processed wafer (semiconductor substrate and/or overlying layers) is exposed to corrosive chemicals to remove certain portions of the wafer. (*Id.*, ¶42.) After etching, the photoresist may then be “stripped” (removed) from the wafer by another chemical treatment. (*Id.*, ¶43.) In some

cases, the etching process itself may even remove the photoresist. A representation of photolithography and etching appears below.



(*Id.*)

An etch that attacks all exposed materials is called a non-selective etch, whereas an etch that attacks certain material compositions more than others is called a selective etch. (*Id.*, ¶44.) An etch that attacks a material in all directions is called isotropic, whereas an etch that attacks in a preferred direction (often perpendicular to the surface of the wafer) is called anisotropic. (*Id.*, ¶45.) An etch that uses a liquid etching agent is called a “wet” etch, whereas an etch that does not use a liquid etching agent (typically using ionized gas, called a “plasma”) is called a “dry” etch. (*Id.*, ¶46.) Dual damascene processes typically use selective, anisotropic, dry etching. (*Id.*, ¶47; *see also, e.g.*, Ex. 1006, 2:61–63; Ex. 1010, 2:44–48; Ex. 1011, 4:9–12.)

### **III. The '696 Patent**

#### **A. Description of the Challenged Claims**

This Petition challenges the patentability of claims 13 and 15 of the '696 patent. Independent claim 13 recites “[a] method for forming an interconnection structure,” and claim 15 depends from claim 13. (Ex. 1001, 34:58–36:18.) As explained further below, claim 13 reads on both the fifth and sixth embodiments of the '696 patent, including the modified fifth and sixth embodiments.<sup>1</sup> (Ex. 1002, ¶¶48–115; *see also* Ex. 1001, 22:47–29:60, Figs. 21(a)–37(b).) The steps of claim 13 are described below with reference to these embodiments. The declaration of Dr. Smith also describes the challenged claims and the embodiments of the '696 patent. (*See* Ex. 1002, ¶¶48–121.)

##### **1. step a) of Claim 13**

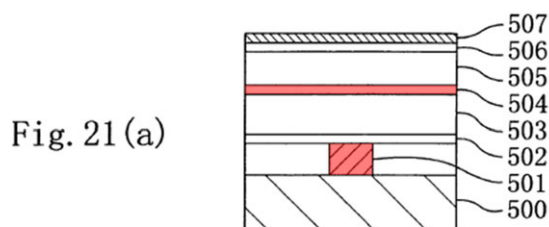
Step a) of claim 13 recites “forming a first insulating film [504, 603] over lower-level metal interconnects [501, 601].”

In the fifth embodiment, the claimed first insulating film is element 504 [or 554], located over lower-level interconnects 501 and made of silicon dioxide (an

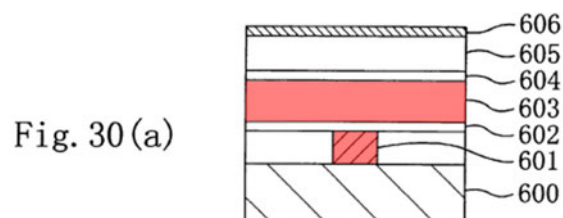
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<sup>1</sup> The modified fifth and sixth embodiments differ from their unmodified counterparts only in that the width of the contact hole in the second resist pattern is larger than the width of the wiring grooves. (*See* Ex. 1001, 25:29–34, 30:51–56, Figs. 25(b), 27(b), 34(b), 36, 37(a)–(b).)

insulating film). (Ex. 1001, 22:52–62, 24:60–25:3, Figs. 21(a), 24(a); Ex. 1002, ¶¶51–52.) Similarly, in the sixth embodiment the claimed first insulating film is element 603 [or 653], located over lower-level interconnects 601 [or 651] and formed of an insulating organic film. (Ex. 1001, 28:1–9, 30:1–11, Figs. 30(a), 33(a); Ex. 1002, ¶¶53–54.) Examples from the '696 patent of step a) appear with highlights in the Figures below. (Ex. 1001, 22:52–23:24, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶50–55.)



***Fifth Embodiment***



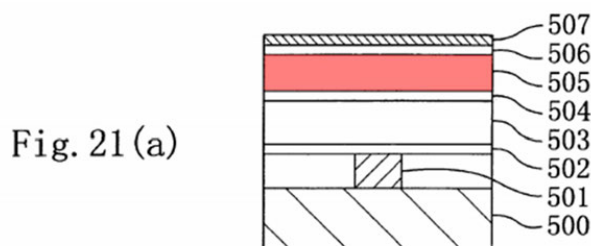
***Sixth Embodiment***

## **2. step b) of Claim 13**

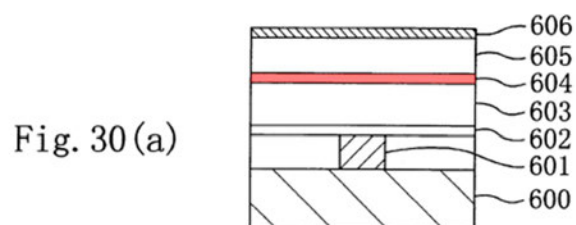
Step b) of claim 13 recites “forming a second insulating film [505, 604], having a different composition than that of the first insulating film, over the first insulating film [504, 603].”

In the fifth embodiment, the composition of the claimed second insulating film 505 [or 555] differs from the composition of the claimed first insulating film 504 [or 554]. Second insulating film 505 [or 555] is an organic insulating film, whereas first insulating film 504 [or 554] is silicon dioxide. (Ex. 1001, 22:60–64, 25:1–6, Figs. 21(a), 24(a); Ex. 1002, ¶¶57–58.) In the sixth embodiment, the

composition of the claimed second insulating film 604 [or 654] differs from the composition of the claimed first insulating film 603 [or 653]. Second insulating film 604 [or 654] is silicon dioxide, whereas first insulating film 603 [or 653] is an organic film. (Ex. 1001, 28: 6–11, 30:6–11, Figs. 30(a), 33(a); Ex. 1002, ¶¶59–60.) Examples from the '696 patent of step b) appear with highlights in the Figures below. (Ex. 1001, 22:52–23:24, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶56–61.)



***Fifth Embodiment***



***Sixth Embodiment***

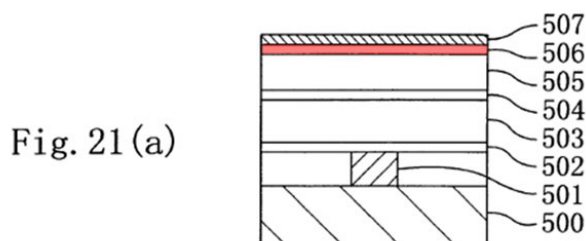
### **3. step c) of Claim 13**

Step c) of claim 13 recites “forming a third insulating film [506, 605], having a different composition than that of the second insulating film, over the second insulating film [505, 604].”

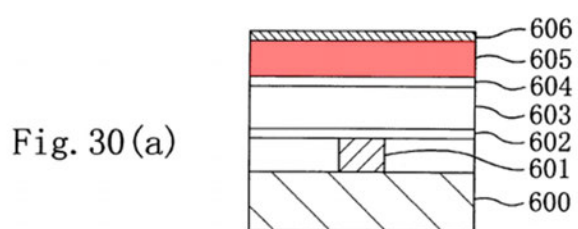
In the fifth embodiment, the composition of the claimed third insulating film 506 [or 556] differs from the composition of the claimed second insulating film 505 [or 555]. Third insulating film 506 [or 556] is silicon dioxide (an insulating film), whereas second insulating film 505 [or 555] is an organic insulating film. (Ex. 1001, 22:62–67, 25:3–9, Figs. 21(a), 24(a); Ex. 1002, ¶¶63–64.) In the sixth



embodiment, the composition of the claimed third insulating film 605 [or 655] differs from the composition of the claimed second insulating film 604 [or 654]. Third insulating film 605 [or 655] is an organic insulating film, whereas second insulating film 604 [or 654] is silicon dioxide. (Ex. 1001, 28: 9–13, 30:9–14, Figs. 30(a), 33(a); Ex. 1002, ¶¶65–66.) Examples from the '696 patent of step c) appear with highlights in the Figures below. (Ex. 1001, 22:52–23:24, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶62–67.)



*Fifth Embodiment*



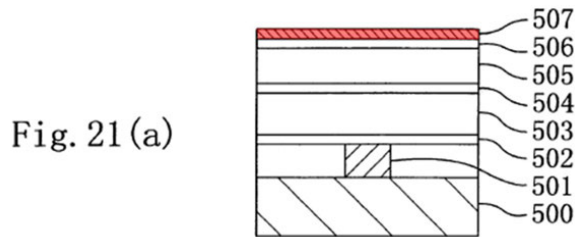
*Sixth Embodiment*

#### 4. step d) of Claim 13

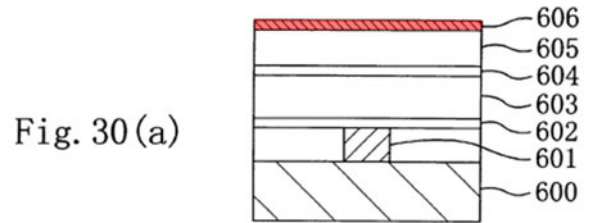
Step d) of claim 13 recites “forming a thin film [507, 606] over the third insulating film [506, 605].”

In the fifth embodiment, “a titanium nitride film 507[/557] (thin film) is deposited to be 50 nm thick.” (Ex. 1001, 23:1–3, 25:9–11, Figs. 21(a), 24(a); Ex. 1002, ¶¶69–70.) Similarly, in the sixth embodiment, “a titanium nitride film 606[/656] (thin film) is deposited to be 50 nm thick.” (Ex. 1001, 28:14–16, 30:14–16, Figs. 30(a), 33(a); Ex. 1002, ¶¶71–72.) Examples from the '696 patent of step

d) appear with highlights in the Figures below. (Ex. 1001, 22:52–23:24, 28:1–36, Figs. 21(a), 30(a); Ex. 1002, ¶¶68–73.)



*Fifth Embodiment*



*Sixth Embodiment*

## 5. step e) of Claim 13

Step e) of claim 13 recites “forming a first resist pattern [508, 607] on the thin film [507, 606], the first resist pattern having openings for forming wiring grooves.”

In the fifth embodiment, “a first resist pattern 508[/558], having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 507[/557].” (Ex. 1001, 23:25–27, 25:19–21, Figs. 21(b), 24(b); Ex. 1002, ¶¶75–76.) Similarly, in the sixth embodiment “a first resist pattern 607[/657], having openings for forming wiring grooves, is formed by lithography on the titanium nitride film 606[/656].” (Ex. 1001, 28:37–39, 30:37–39, Figs. 30(b), 33(b); Ex. 1002, ¶¶77–78.) Examples from the ’696 patent of step e) appear with highlights in the Figures below. (Ex. 1001, 23:25–32, 28:37–43, Figs. 21(b), 30(b); Ex. 1002, ¶¶74–79.)

Fig. 21 (b)

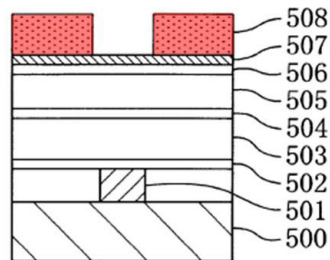
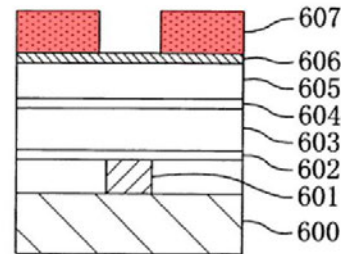
*Fifth Embodiment*

Fig. 30 (b)

*Sixth Embodiment*

## 6. step f) of Claim 13

Step f) of claim 13 recites “etching the thin film [507, 606] using the first resist pattern [508, 607] as a mask, thereby forming a mask pattern [509, 608] out of the thin film to have the openings for forming wiring grooves.”

In the fifth embodiment, “the titanium nitride film 507[/557] is dry-etched using the first resist pattern 508[/558] as a mask, thereby forming a mask pattern 509[/559], having openings for forming wiring grooves, out of the titanium nitride film 507[/557].” (Ex. 1001, 23:27–32, 25:21–25, Figs. 21(c), 24(c); Ex. 1002, ¶¶81–82.) Similarly, in the sixth embodiment “the titanium nitride film 606[/656] is dry-etched using the first resist pattern 607[/657] as a mask, thereby forming a mask pattern 608[/658], having openings for forming wiring grooves, out of the titanium nitride film 606[/656].” (Ex. 1001, 28:39–43, 30:39–43, Figs. 30(c), 33(c); Ex. 1002, ¶¶83–84.) Examples from the ’696 patent of step f) appear with highlights in the Figures below. (Ex. 1001, 23:25–32, 28:37–43, Figs. 21(c), 30(c); Ex. 1002, ¶¶80–85.)

Fig. 21 (c)

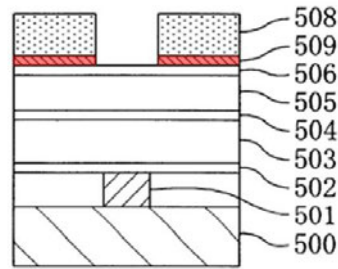
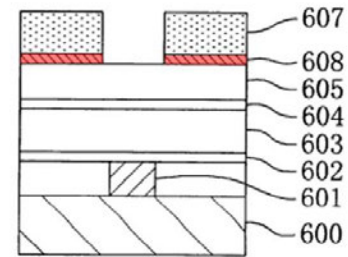
*Fifth Embodiment*

Fig. 30 (c)

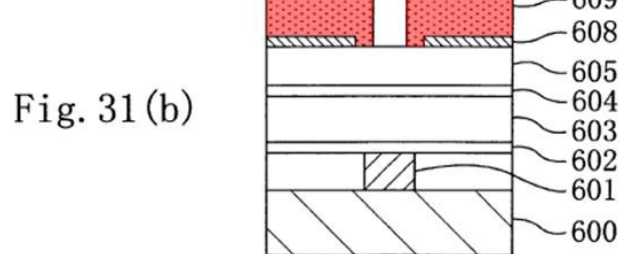
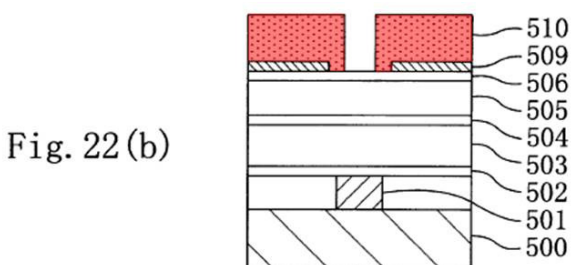
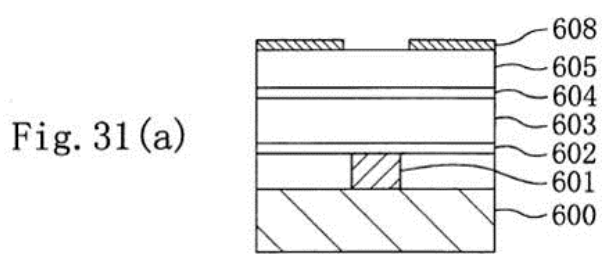
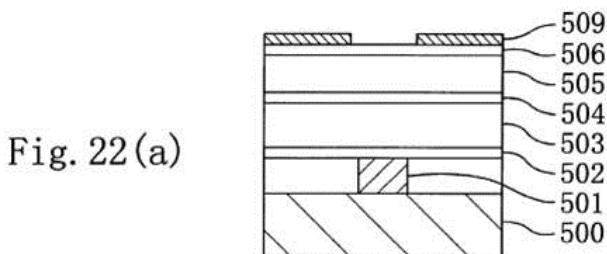
*Sixth Embodiment*

## 7. step g) of Claim 13

Step g) of claim 13 recites “removing the first resist pattern [508, 607] and then forming a second resist pattern [510, 609] on the third insulating film [506, 605] and the mask pattern [509, 608], the second resist pattern having openings for forming contact holes.”

In the fifth embodiment, “the first resist pattern 508[558] is removed.” (Ex. 1001, 23:33–34, 25:26–27, Figs. 22(a), 25(a), 27(a).) “Then, as shown in FIG. 22(b)[/FIG. 25(b)], a second resist pattern 510[/560], having openings for forming contact holes, is formed by lithography on the mask pattern 509[/559].” (Ex. 1001, 23:40–42, 25:27–35, Figs. 22(b), 25(b); Ex. 1002, ¶¶87–88.) Similarly, in the sixth embodiment, “the first resist pattern 607[/657] is removed.” (Ex. 1001, 28:44–46, 30:44–46, Figs. 31(a), 34(a).) “Then, as shown in FIG. 31(b)[/FIG. 34(b)], a second resist pattern 609[/659], having openings for forming contact holes, is formed by lithography on the mask pattern 608[/658].” (Ex. 1001, 28:49–51, 30:49–57, Figs. 31(b), 34(b); Ex. 1002, ¶¶89–90.) Examples from the ’696 patent

of step g) appear with highlights in the Figures below. (Ex. 1001, 23:33–42, 28:44–51, Figs. 22(a), 22(b), 31(a), 31(b); Ex. 1002, ¶¶86–91.)



#### *Fifth Embodiment*

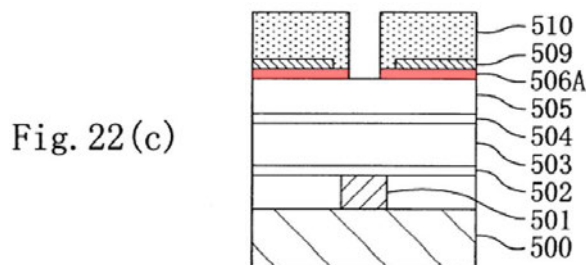
#### *Sixth Embodiment*

### **8. step h) of Claim 13**

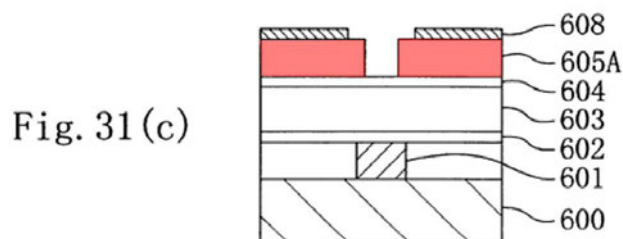
Step h) of claim 13 recites “dry-etching the third insulating film [506, 605] using the second resist pattern [510, 609] and the mask pattern [509, 608] as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

In the fifth embodiment, “the second silicon dioxide film 506[556] is dry-etched using the second resist pattern 510[560] and the mask pattern 509[559] as a mask, thereby forming a patterned second silicon dioxide film 506A[556A] having openings for forming contact holes.” (Ex. 1001, 23:42–46, 25:36–41, Figs.

22(c), 25(c), 27(b); Ex. 1002, ¶¶93–94.) Similarly, in the sixth embodiment, “the second organic film 605[/655] is dry-etched using the second resist pattern 609[/659] and the mask pattern 608[/658] as a mask, thereby forming a patterned second organic film 605A[/655A] having openings for forming contact holes.” (Ex. 1001, 28:51–55, 30:58–62, Figs. 31(c), 34(c); Ex. 1002, ¶¶95–96.) Examples from the ’696 patent of step h) appear with highlights in the Figures below. (Ex. 1001, 23:42–46, 28:51–55, Figs. 22(c), 31(c); Ex. 1002, ¶¶92–97.)



*Fifth Embodiment*



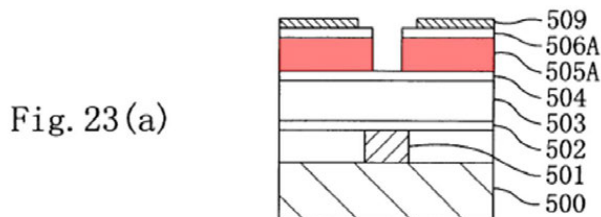
*Sixth Embodiment*

## 9. step i) of Claim 13

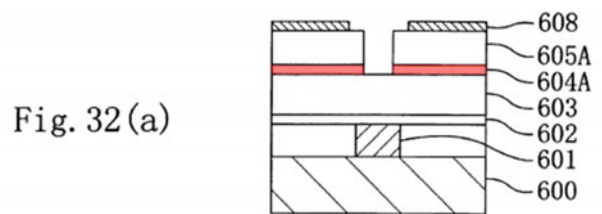
Step i) of claim 13 recites “dry-etching the second insulating film [505, 604] using the patterned third insulating film [506A, 605A] as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

In the fifth embodiment, “the second organic film 505[/555] is dry-etched using the patterned second silicon dioxide film 506A[/556A] as a mask, thereby forming a patterned second organic film 505A[/555A] having openings for

forming contact holes.” (Ex. 1001, 23:47–51, 25:66–26:3, Figs. 23(a), 26(a), 28(a); Ex. 1002, ¶¶99–100.) Similarly, in the sixth embodiment, “the silicon dioxide film 604[/654] is dry-etched using the patterned second organic film 605A[/655A] as a mask, thereby forming a patterned silicon dioxide film 604A[/654A] having openings for forming contact holes.” (Ex. 1001, 29:1–5, 31:7–11, Figs. 32(a), 35(a); Ex. 1002, ¶¶101–02.) Examples from the ’696 patent of step i) appear with highlights in the Figures below. (Ex. 1001, 23:47–51, 29:1–5, Figs. 23(a), 32(a); Ex. 1002, ¶¶98–103.)



*Fifth Embodiment*



*Sixth Embodiment*

## 10. step j) of Claim 13

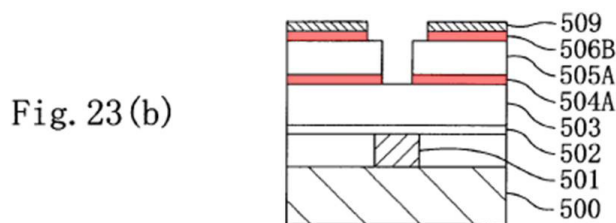
Step j) of claim 13 recites “dry-etching the patterned third insulating film [506A, 605A] and the first insulating film [504, 603] using the mask pattern [509, 608] and the patterned second insulating film [505A, 604A] as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

In the fifth embodiment, “the patterned second silicon dioxide film 506A[/556A] and the first silicon dioxide film 504[/554] are dry-etched using the

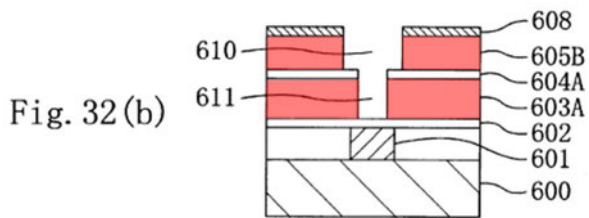
mask pattern 509[/559] and the patterned second organic film 505A[/555A] as respective masks, thereby forming a patterned second silicon dioxide film 506B[/556B] having openings for forming wiring grooves and a patterned first silicon dioxide film 504A[/554A] having openings for forming contact holes.” (Ex. 1001, 23:66–24:6, 26:15–22, Figs. 23(b), 26(b), 28(b); Ex. 1002, ¶¶105–06.)

Similarly, in the sixth embodiment, “the patterned second organic film 605A[/655A] and the first organic film 603[/653] are dry-etched using the mask pattern 608[/658] and the patterned silicon dioxide film 604A[/654A] as respective masks, thereby forming a patterned second organic film 605B[/655B] having wiring grooves 610[/660] and a patterned first organic film 603A[/653A] having contact holes 611[/661].” (Ex. 1001, 29:6–12, 31:12–18, Figs. 32(b), 35(b); Ex. 1002, ¶¶107–08.)

Examples from the '696 patent of step j) appear with highlights in the Figures below. (Ex. 1001, 23:66–24:6, 29:6–12, Figs. 23(b), 32(b); Ex. 1002, ¶¶104–09.)



***Fifth Embodiment***



***Sixth Embodiment***



## **11. step k) of Claim 13**

Step k) of claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects [513, 612] and contacts [514, 613] connecting the lower- and upper-level metal interconnects together.”

In the fifth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 512[/562] and the wiring grooves 511[/561].” (Ex. 1001, 24:22–24, 26:38–41, Figs. 23(d), 26(d), 29(b).) “As a result, second metal interconnects 513[/563] and contacts 514[/564], connecting the first and second metal interconnects 501[/551] and 513[/563] together, are formed.” (Ex. 1001, 24:33–35, 26:44–47; Ex. 1002, ¶¶111–12.) Similarly, in the sixth embodiment, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 611[/661] and the wiring grooves 610[/660].” (Ex. 1001, 29:24–26, 31:30–32, Figs. 32(c), 35(c).) “As a result, second metal interconnects 612[/662] and contacts 613[/663], connecting the first and second metal interconnects 601[/651] and 612[/662] together, are formed.” (Ex. 1001, 29:35–38, 31:41–44; Ex. 1002, ¶¶113–14.) Examples from the ’696 patent of step k) appear with highlights in the Figures below. (Ex. 1001, 24:22–24, 29:24–39, Figs. 23(d), 32(c); Ex. 1002, ¶¶110–15.)

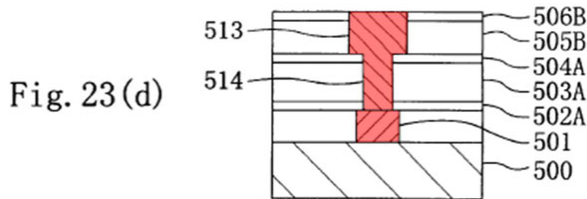


Fig. 23(d)

*Fifth Embodiment*

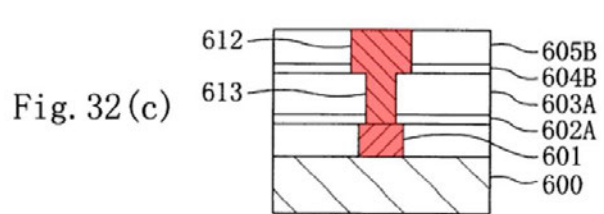


Fig. 32(c)

*Sixth Embodiment*

## 12. Dependent Claim 15

Claim 15 depends from claim 13 and further recites “wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.” (*See* Ex. 1001, 23:40–42, 25:26–65, 26:12–60, 28:49–51, 30:52–56, 31:49–32:6, Figs. 22(b), 25(b), 31(b), 34(b), 27(b), 36, 37(a); Ex. 1002, ¶¶116–21.)

### B. Examination of the '696 Patent

The application for the '696 patent was filed March 23, 1999, and claims foreign priority to Japanese Patent Application No. 10-079371, filed March 26, 1998.

The original application for the '696 patent included 15 claims. (Ex. 1012, 150–58.) The Examiner issued a first-action Notice of Allowability, accompanied by a statement of reasons for allowance, stating simply, “Prior art lacks the steps of forming an interconnection structure as recited in the claims.” (*Id.*, 352–53.) The '696 patent issued March 6, 2001, with all 15 original claims.

**C. The Challenged Claims Are Not Entitled to the Benefit of Foreign Priority**

The '696 patent claims priority to Japanese Patent Application No. 10-079371 (Ex. 1013; Ex. 1014) (“the '371 application”), filed March 26, 1998, but the challenged claims are not entitled to such priority. Patent Owner bears the burden of proving entitlement to the benefit of foreign priority, *Fiers v. Revel*, 984 F.2d 1164, 1169 (Fed. Cir. 1993); *Core Survival, Inc. v. S&S Precision, LLC*, PGR2015-00022, Paper 8, at 7–10 (Feb. 19, 2016), but Patent Owner cannot meet its burden here. Moreover, “genuine issue[s] of material fact . . . will be viewed in the light most favorable to the petitioner.” 37 C.F.R. §42.108.

The challenged claims are directed to the fifth, modified fifth, sixth, and modified sixth embodiments of the '696 patent (the “new embodiments”). (Ex. 1002, ¶¶48–121) The '371 application, however, describes only the first through fourth embodiments of the '696 patent. (*Compare* Ex. 1014, ¶¶0028–0062, Figs. 1(a)–8(c), *with* Ex. 1001, 10:22–14:56, Figs. 1(a)–8(c); *compare* Ex. 1014 ¶¶0063–0074, Figs. 9(a)–11(c), *with* Ex. 1001, 14:58–16:38, Figs. 9(a)–11(c); *compare* Ex. 1014 ¶¶0075–0088, Figs. 12(a)–14(c), *with* Ex. 1001, 16:39–18:53, Figs. 12(a)–14(c); *compare* Ex. 1014 ¶¶0089–0102, Figs. 15(a)–17(c), *with* Ex. 1001, 18:59–20:49, Figs. 15(a)–17(c); *compare* Ex. 1014, ¶¶0103–0115, Figs. 18(a)–20(c), *with* Ex. 1001, 20:51–22:44, Figs. 18(a)–20(c).)

The '371 application does not disclose the new embodiments to which the challenged claims are directed. (*Compare generally* Ex. 1014, *with* Ex. 1001, 22:46–32:9, Figs. 21(a)–37(b); *see also* Ex. 1002, ¶¶122–24.) It also does not include Figures 21(a)–37(b) or claims 10–15, which relate to the new embodiments of the '696 patent. (*See* Ex. 1014, [Claim 1]–[Claim 9], [Figure 1]–[Figure 20].) The descriptions, figures, and claims relevant to the subject matter challenged in this petition were added in Japanese Patent Application No. 11-075519 (“the '519 application”) (Ex. 1015; Ex. 1016), filed March 9, 1999, and the application for the '696 patent, filed March 23, 1999. (*See* Ex. 1016, [Claim 9]–[Claim 15], ¶¶0124–0201; Ex. 1012, 125–49, 154–58.)

None of the embodiments described in the '371 application disclose all of the steps recited in claim 13.<sup>2</sup> The challenged claims are not entitled to the benefit of foreign priority. *See, e.g., In re Ziegler*, 992 F.2d 1197, 1200 (Fed. Cir. 1993).

**1. The first, second, and fourth embodiments of the '371 application do not disclose step g) of claim 13**

Step g) of claim 13 recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.”

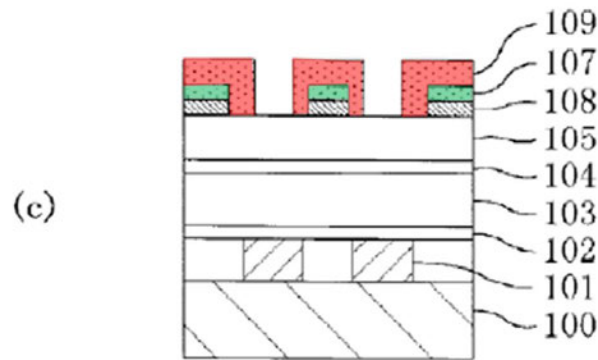
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<sup>2</sup> The examples contained herein are illustrative, not limiting. Again, Patent Owner must establish priority.

The first, second, and fourth embodiments do not teach “removing the first resist pattern” before “forming a second resist pattern.” Each of those embodiments instead teaches forming the second resist pattern *before* removing the first resist pattern. (*See* Ex. 1002, ¶¶125–27.)

The description of the first embodiment in the '371 application states, “[T]he second resist pattern 109 is formed without removing the first resist pattern 107.” (Ex. 1014, ¶0043; *see also* ¶¶0050, 0056, Figs. 1(c), 5(a), 7(a).) The description of the second embodiment similarly states that “a second resist pattern 209, having openings for the formation of contact holes is formed by lithography on the second organic film 205 without removing the first resist pattern 207.” (*Id.*, ¶0068; *see also* Fig. 9(c).) And the description of the fourth embodiment states that “a second resist pattern 409 having openings for the formation of contact holes is formed by lithography on the second low-dielectric-constant SOG film 405 without removing the first resist pattern 407.” (*Id.*, ¶0107; *see also* Fig. 18(c).)

Figure 1(c) of the '371 patent application, shown below with highlights, demonstrates the formation of the second resist pattern (red) without removing the first resist pattern (green). (*See also id.*, Figs. 5(a), 7(a), 9(c), 18(c).)



**2. The third, variant of the third, and fourth embodiments do not disclose step h) of claim 13**

Step h) of claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

The third, variant of the third, and fourth embodiments of the ’371 application do not disclose “dry-etching the third insulating film using . . . the mask pattern as a mask.” The descriptions of these embodiments disclose only that the second resist pattern acts as a mask during this etch step. (*See* Ex. 1002, ¶¶128–36.)

To map the third embodiment to claim 13, the third insulating film must be either layer 304 or layer 305. Otherwise, the claimed layer stacking sequence would not be possible. But the third embodiment of the ’371 application states, “[T]he second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG film 304 and the first organic constituent-incorporated

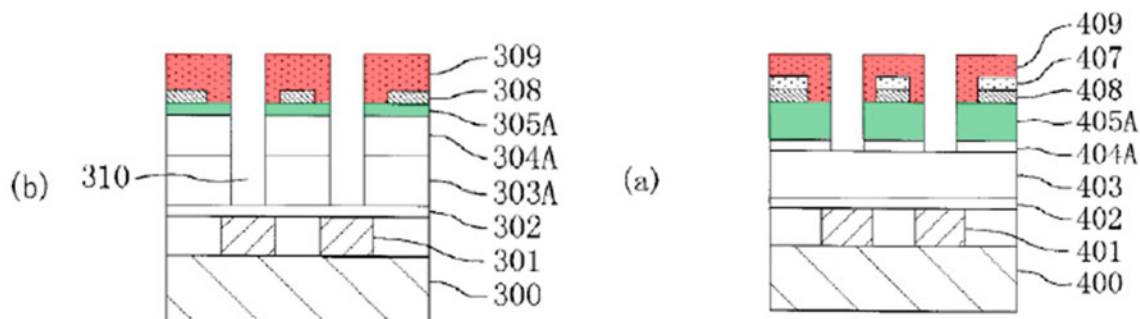
silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” (*Id.*, ¶0079; *see also*, Fig. 13(b).) Pattern 308 is not disclosed as a mask for this step. (Ex. 1002, ¶¶130–31.)

To map the variant of the third embodiment to claim 13, the third insulating film must be layer 355. Otherwise, step j) of claim 13 would not be met. But the variant of the third embodiment states, “[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask.” (*Id.*, ¶0093; *see also* Fig. 16(b).) Pattern 358 is not disclosed as a mask for this etch step. (Ex. 1002, ¶¶132–33.)

To map the fourth embodiment to claim 13, the third insulating film must be layer 405. Otherwise, step j) of claim 13 would not be met. But the fourth embodiment states, “[T]he second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask.” (*Id.*, ¶0107; *see also* Fig. 19(a).) Pattern 408 is not disclosed as a mask for this etch step. (Ex. 1002, ¶¶134–5.)

Thus, the third, variant of the third, and fourth embodiments do not disclose “dry-etching the third insulating film using . . . the mask pattern as a mask.” Figures 13(b) and 19(a) of the ’371 patent application illustrate this point and

appear below on the left and right, respectively, with highlights. (*See also* Ex. 1014, Fig. 16(b).)



**3. The third, variant of the third, and fourth embodiments do not disclose step i) of claim 13**

Step i) of claim 13 similarly recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

The third, variant of the third, and fourth embodiments of the ’371 application do not disclose “dry-etching the second insulating film using the patterned third insulating film as a mask.” Instead, these embodiments disclose using the second resist pattern as a mask when etching the second insulating film. (*See* Ex. 1002, ¶¶137–39.)

To map the third embodiment to claim 13, the second insulating film must be either layer 303 or layer 304. Otherwise, the claimed layer stacking sequence would not be possible. But the third embodiment states, “[T]he second organic constituent-incorporated silicon dioxide film 305, the low-dielectric-constant SOG

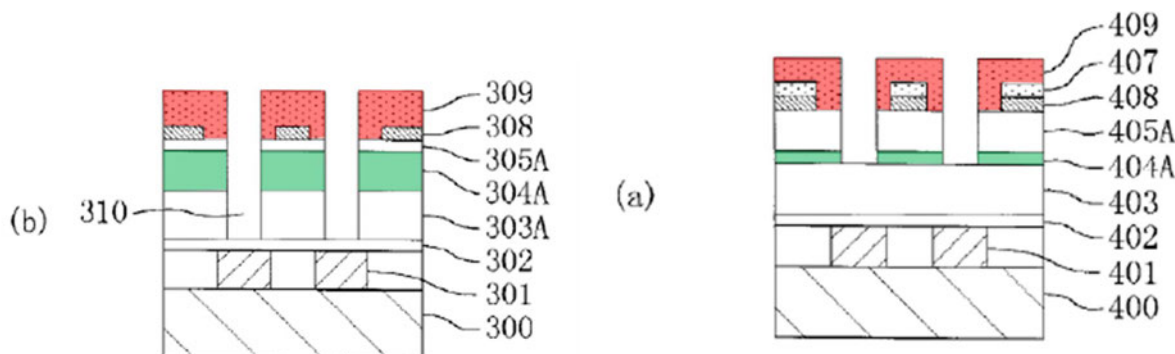


film 304 and the first organic constituent-incorporated silicon dioxide film 303 are sequentially dry-etched using the second resist pattern 309 as a mask.” (Ex. 1014, ¶0079; *see also*, Fig. 13(b).) The patterned third insulating film (layer 304 or 305) is not disclosed as a mask during this etch step. (Ex. 1002, ¶139.)

To map the variant of the third embodiment to claim 13, the second insulating film must be layer 354. Otherwise, step j) of claim 13 would not be met. But the variant of the third embodiment states, “[T]he second silicon dioxide film 355 and the organic film 354 are sequentially dry-etched using the second resist pattern 359 as a mask.” (Ex. 1014, ¶0093; *see also* Fig. 16(b).) The patterned third insulating film (layer 355) is not disclosed as a mask during this etch step. (Ex. 1002, ¶139.)

To map the fourth embodiment to claim 13, the second insulating film must be layer 404. Otherwise, step j) of claim 13 would not be met. But the fourth embodiment states, “[T]he second low-dielectric-constant SOG film 405 and the organic constituent-incorporated silicon dioxide film 404 are sequentially dry-etched using the second resist pattern 409 as a mask.” (*Id.*, ¶0107; *see also* Fig. 19(a).) The patterned third insulating film (layer 405) is not disclosed as a mask during this etch step. (Ex. 1002, ¶138.)

Figures 13(b) and 19(a) of the '371 patent application illustrate this point and appear below on the left and right, respectively, with highlights. (See also Ex. 1014, Fig. 16(b).)



#### **IV. Statement of Precise Relief Requested for Each Claim Challenged**

##### **A. Claims for Which Review is Requested**

TSMC requests review under 35 U.S.C. §311 of claims 13 and 15 and the cancellation of those claims as unpatentable.

##### **B. Statutory Grounds of Challenge**

Claims 13 and 15 are unpatentable under 35 U.S.C. §103.

##### **C. Level of Ordinary Skill**

A person of ordinary skill in the art (“POSITA”) would possess (1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development. (Ex. 1002, ¶141.) Additional graduate education could substitute

for professional experience, and significant work experience could substitute for formal education. (*Id.*)

#### **D. Claim Construction**

Claim terms are given their ordinary and accustomed meaning as understood by a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). A claim in an unexpired patent in post-grant review receives the “broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. §42.100(b). The broadest reasonable construction should apply to all claims of the ’696 patent.

#### **V. Claims 13 and 15 of the ’696 Patent Are Unpatentable Over the Prior Art**

##### **A. Disclosures of the Prior Art**

##### **1. Grill (U.S. Patent No. 6,140,226)**

*Grill* was filed July 30, 1998, and claims priority to U.S. Provisional Patent Application No. 60/071,628 (Ex. 1017) (“the ’628 application”), filed January 16, 1998. Due to its July 30, 1998, filing date, *Grill* is prior art to the ’696 patent under §102(e). Because of the ’628 application, *Grill* would still qualify as prior art under §102(e) even if the challenged claims were entitled to the benefit of foreign priority.<sup>3</sup> *Grill* was neither considered nor cited during prosecution.

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<sup>3</sup> Petitioner does need not do anything more at this stage to meet its initial burden of production to demonstrate *Grill* is prior art under §102(e). *See Dynamic*

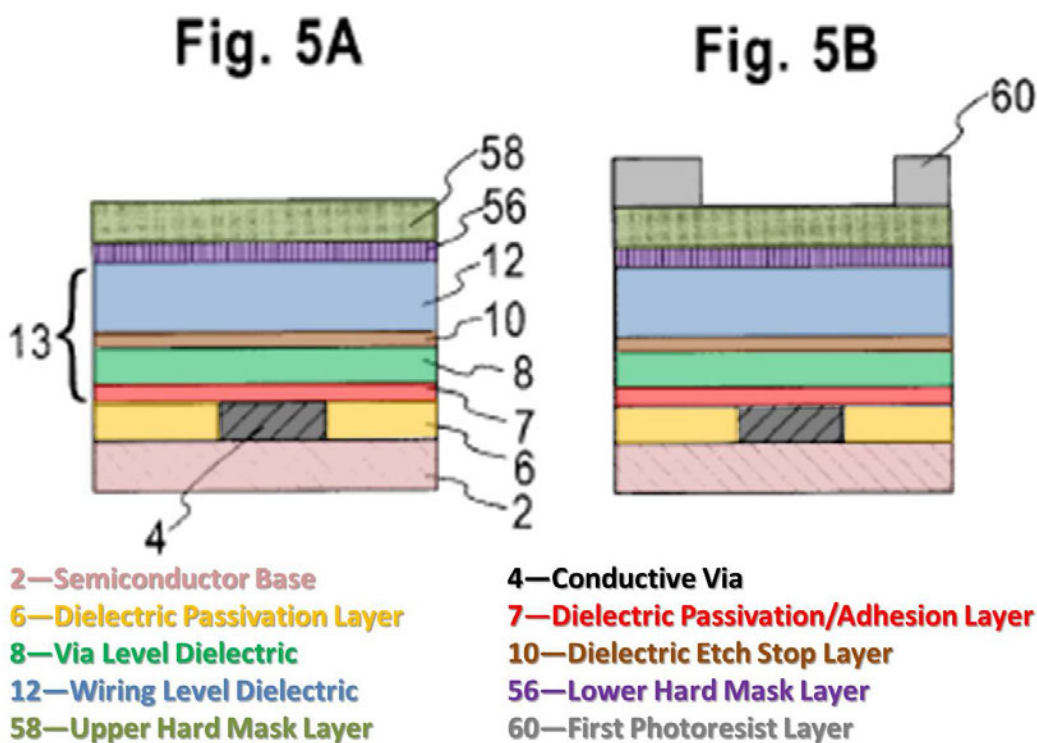
*Grill* discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (Ex. 1005, Abstract; *see also* 7:16–30.) Although *Grill* discloses several

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*Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015); *Ariosa Diagnostics, Inc. v. Illumina, Inc.*, IPR2014-01093, Paper 69 at 10, 12–13 (Jan. 7, 2016). IPB bears the burden of production to show that the challenged claims are entitled to a priority date before July 30, 1998. *Dynamic Drinkware*, 800 F.3d. at 1380; IPR2014-01093, Paper 69 at 14. If IPB could do so, the burden of production would shift back to Petitioner, *Dynamic Drinkware*, 800 F.3d. at 1380; IPR2014-01093, Paper 69 at 14–15, who would be permitted to establish that *Grill* antedates the earliest priority date of the ’696 patent because of the ’628 application. Although Petitioner need not show *Grill* is supported by the ’628 application unless Patent Owner shows the challenged claims antedate *Grill*, Dr. Smith provides a provisional claim chart in his declaration, showing support for *Grill*’s claim 28 in the ’628 application. (*See also* Ex. 1002, ¶¶5, 153.) The disclosures of the ’628 application that demonstrate the unpatentability of the challenged claims are at pages 10–14, 16, and 17 and Figures 5A–5H, 1J–1L of Exhibit 1017. (Ex. 1002, ¶153.)

processes for forming a dual damascene structure, this Petition focuses on the embodiment described at 4:60–5:8 and 7:16–8:8 and minor variations.

The structure of *Grill*'s Fig. 5A is formed first, followed by patterning a first photoresist layer [60], as Figure 5B shows. (*Id.*, 7:30–44.) This photolithography defines what will become the trench level of the interconnection. (Ex. 1002, ¶145.)



Next, an etch transfers the photoresist pattern [60] into the upper hard mask layer [58], as Figure 5C shows. (Ex. 1005, 7:45–50.) The first layer of photoresist [60] is then removed, and a second layer of photoresist [62] is patterned to define what will become the via level of the interconnection, as Figure 5D shows. (*Id.*, 7:51–55; Ex. 1002, ¶146.)

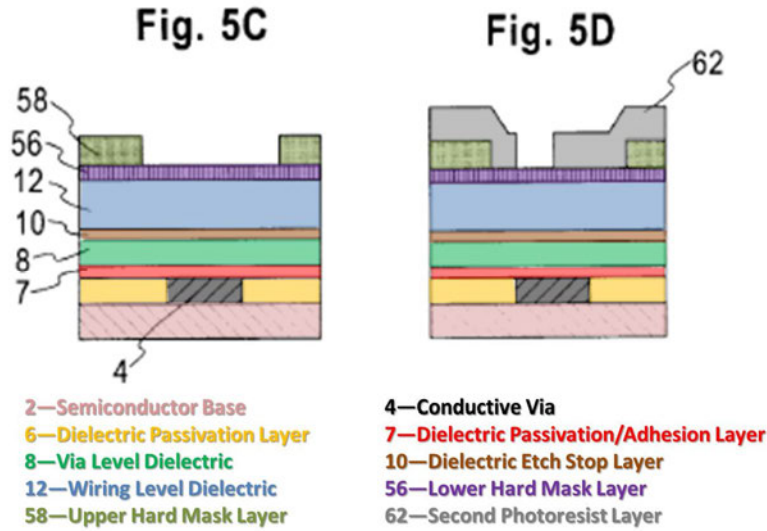
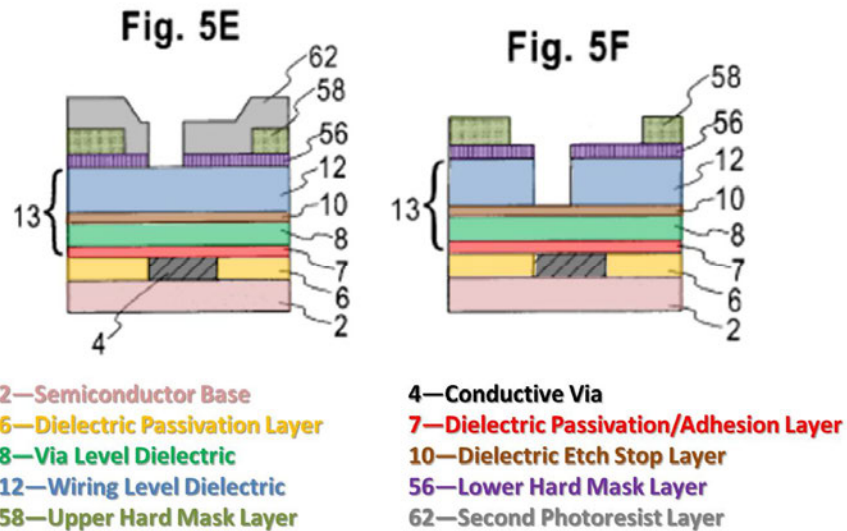
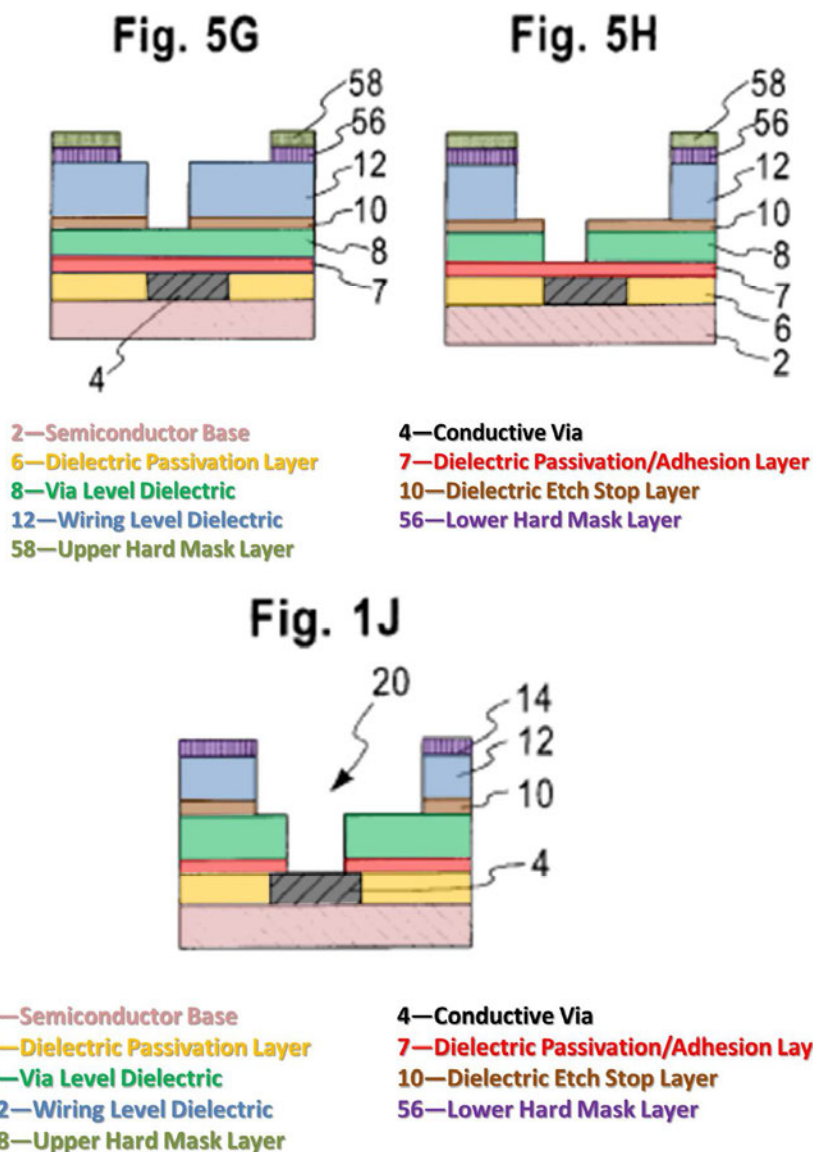


Figure 5E shows the next step of performing an etch to transfer the photoresist pattern [62] into the lower hard mask layer [56]. (Ex. 1005, 7:57–61.) This pattern is then transferred into layer [12] by another etch, which also removes the second photoresist layer [62] (as in Figure 5F). (*Id.*, 7:62–66; Ex. 1002, ¶147.)



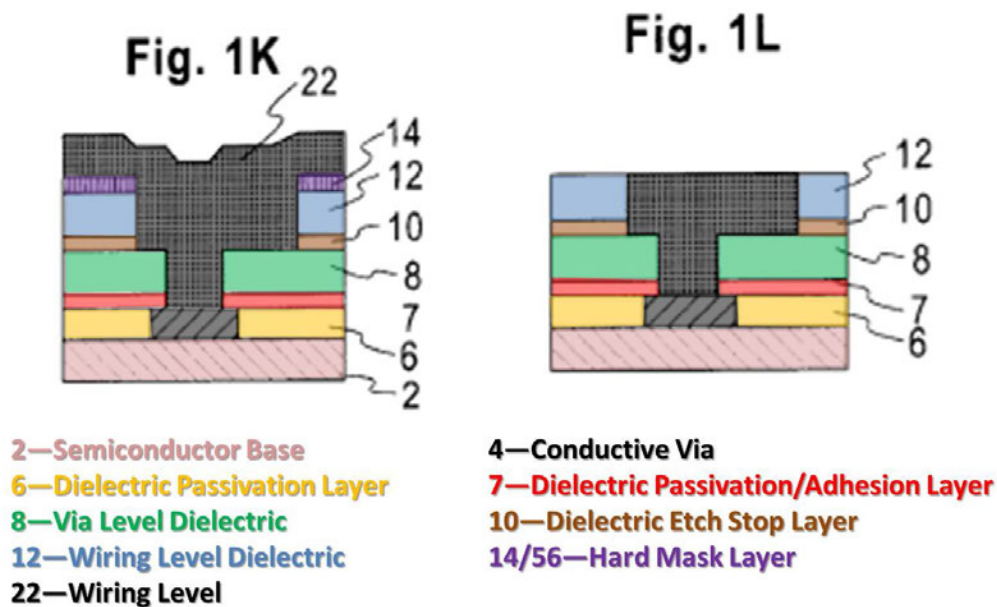
Another etch is then performed to remove the exposed portions of both the lower hard mask [56] and etch stop layer [10], as Figure 5G shows. (Ex. 1005,

7:67–8:2.) A further etch removes the exposed portions of dielectric layers 8 and 12, as FIG. 5H shows. (*Id.*, 8:2–5.) A final etch removes the exposed portions of optional dielectric layer 7, which also removes the exposed portions of etch stop [10] to form the dual-relief cavity of Fig. 1J. (*Id.*, 4:61–64, 8:5–8; Ex. 1002, ¶148.)



The cavity is filled with conductive material [22], as Figure 1K shows, and planarized by a chemical-mechanical polishing (CMP) process, as Figure 1L

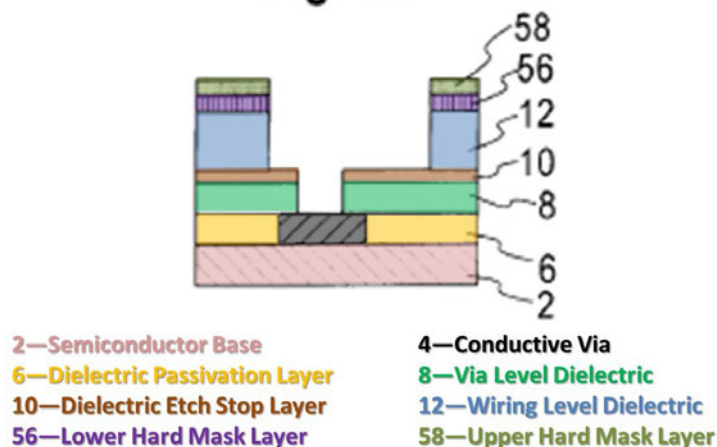
shows. (Ex. 1005, 4:64–5:8, 8:5–8.) Hard mask 14, which is analogous to lower hard mask 56 and upper hard mask 58 (*compare* Ex. 1001, 4:24–29, Figs. , 1C, 1I, *with* Ex. 1005, 7:30–42, Figs. 5A, 5H), may remain in the final structure. (Ex. 1005, 5:5–8; Ex. 1002, ¶149.)



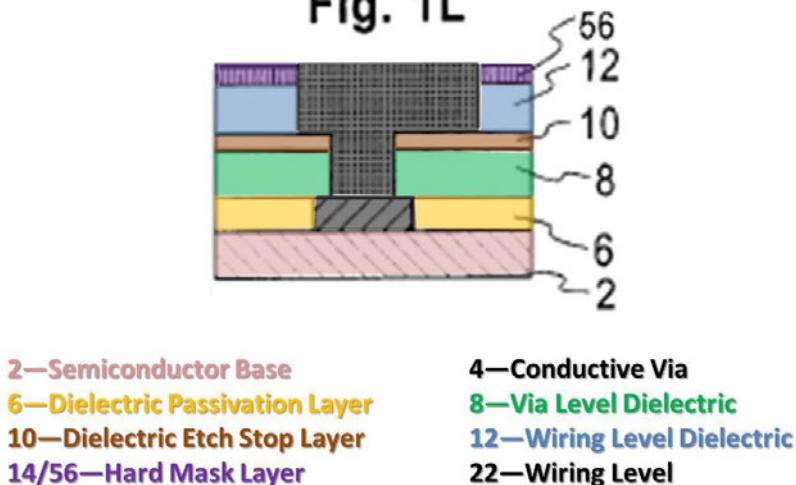
Although this is the only illustration of the described embodiment, other variations are disclosed. For example, *Grill* teaches that layer 7 is an optional dielectric passivation/adhesion layer, and dielectric etch stop layer 10 is also optional. (Ex. 1005, 4:1–5, 4:61–63.) Modified Figures 5H' and 1L' below illustrate how a POSITA would understand the alternative embodiment in which optional layer 7 is not used. (Ex. 1002, ¶¶150–52.)



**Fig. 5H'**



**Fig. 1L'**



## 2. *Aoyama* (U.S. Patent No. 5,592,024)

*Aoyama* (Ex. 1018) teaches a damascene process in which the opening in the via resist pattern is wider than the wiring groove. (Ex. 1018, 15:48–51, 16:3–5, Figs. 18A–18C, 19A–19B.) *Aoyama* was filed October 28, 1994, and issued January 7, 1997, so it qualifies as prior art under §102(b). *Aoyama* was neither considered nor cited during prosecution.

*Aoyama* explains a problem in which misalignment of the photomask when forming through-hole (via) can cause the it to be smaller than desired and the wiring groove to be wider than desired at the through-hole. (*Id.*, 3:18–21, 3:29–32, Figs. 5B, 5D (below).) This increases contact resistance, degrades reliability, and hinders increased integration density. (*Id.*, 3:33–38, 6:7–14.)

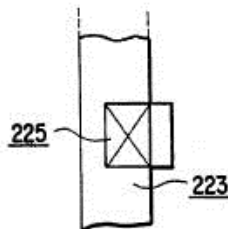


FIG. 5D PRIOR ART

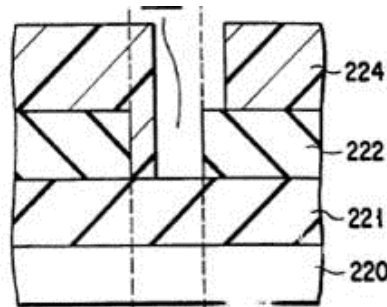
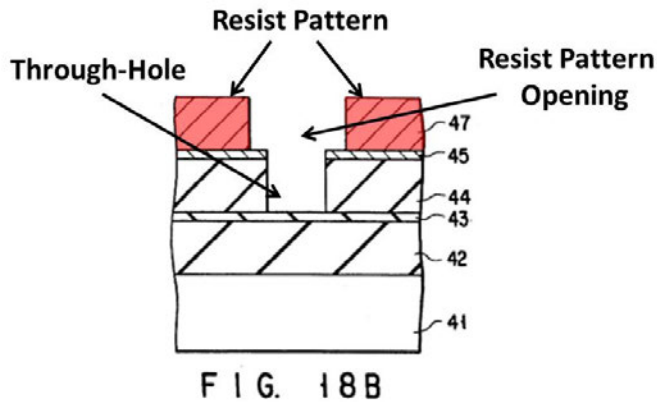
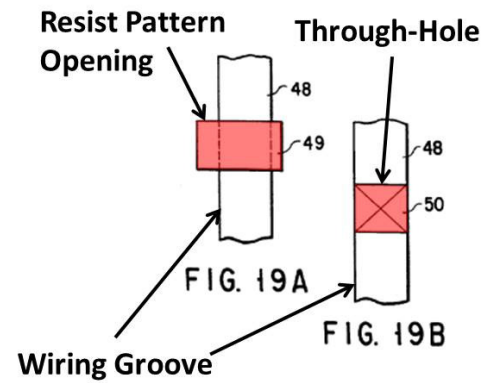


FIG. 5B PRIOR ART

*Aoyama* resolves this problem using a resist pattern with a through-hole wider than the wiring groove. (*Id.*, 16:3–5, Figs. 18B, 19A (each below with annotations and highlights).) Even when misaligned, a through-hole having the same width as the wiring groove is formed. (*Id.*, 16:14–16, Fig. 19B (below with annotations and highlight).)



*Side View*



*Top View*

## B. *Grill* Renders Claim 13 Obvious

As detailed below, *Grill* is virtually identical to the fifth embodiment of the '696 patent, which claim 13 covers. (Ex. 1002, ¶¶48–115.) The arguments that follow in this subsection are based on *Grill*'s disclosure that the dielectric passivation/adhesion layer 7 is optional. (Ex. 1005, 4:1–5, 4:61–63.) A POSITA would have understood that the expressly disclosed embodiment of *Grill* at 4:60–5:8 and 7:16–8:8, without optional layer 7, is a process that meets every limitation of claim 13 and renders it obvious.<sup>4</sup> See, e.g., *Upsher-Smith Labs., Inc. v. PamLab L.L.C.*, 412 F.3d 1319, 1322 (Fed. Cir. 2005) (“‘[O]ptional inclusion’ of

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<sup>4</sup> Because this ground of unpatentability relies in part on what a POSITA would have understood about a variant *Grill* suggests but does not describe in detail (the embodiment without optional layer 7), Petitioner presents this ground as a single-reference obviousness argument.

antioxidants teaches vitamin supplement compositions that both do and do not contain antioxidants.”).

**1. Claim 13 is obvious in view of *Grill***

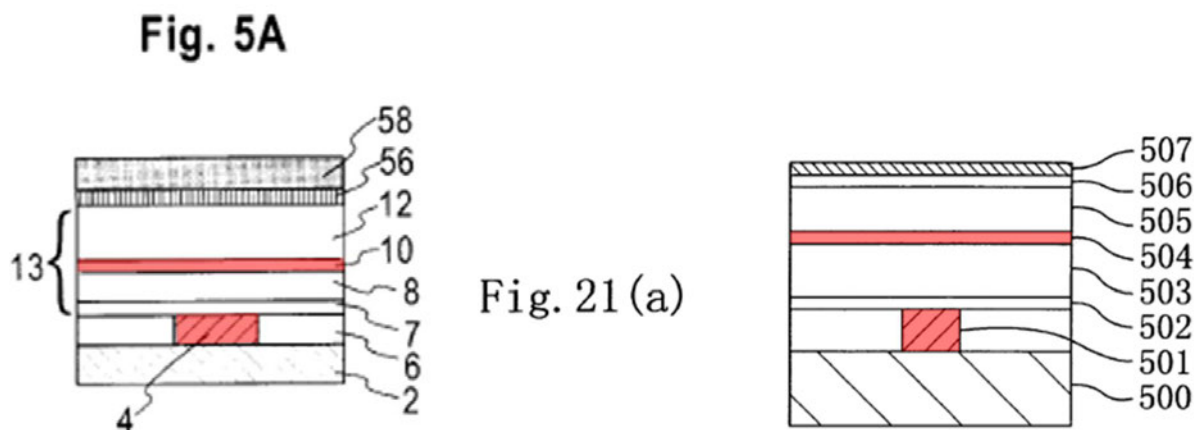
**a. [13.1] *Grill* discloses the preamble of claim 13**

The preamble of claim 13 recites “[a] method for forming an interconnection structure.” *Grill*, titled “Dual Damascene Processing for Semiconductor Chip Interconnects,” discloses “methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels.” (Ex. 1005, Abstract; *see also* 1:12–15, 7:16–30, Fig. 1L; Ex. 1001, Abstract, Fig. 3(c).)

**b. [13.2] *Grill* discloses “forming a first insulating film”**

Claim 13 recites “forming a first insulating film over lower-level metal interconnects.” *Grill* discloses “dielectric etch stop layer 10,” which “might be a silicon-containing material such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiO<sub>x</sub>N<sub>y</sub>, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” (Ex. 1005, 4:1–13.) A POSITA would have understood that the disclosed etch stop layer [10] is an insulating film. (Ex. 1002, ¶170.) Further, *Grill* discloses a “conductive via 4,” which is “formed in the interlevel dielectric to provide interlevel contacts between the wiring traces.” (Ex. 1005, 1:25–27, 3:60–67, Fig. 5A.) As *Grill*’s Figure 5A shows below, a POSITA would have understood that etch stop [10] is located over the conductive via [4].

(Ex. 1002, ¶171; *see also* Ex. 1005, Fig. 5A; *supra* §III.A.1.) Figure 21(a) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶169–72.)



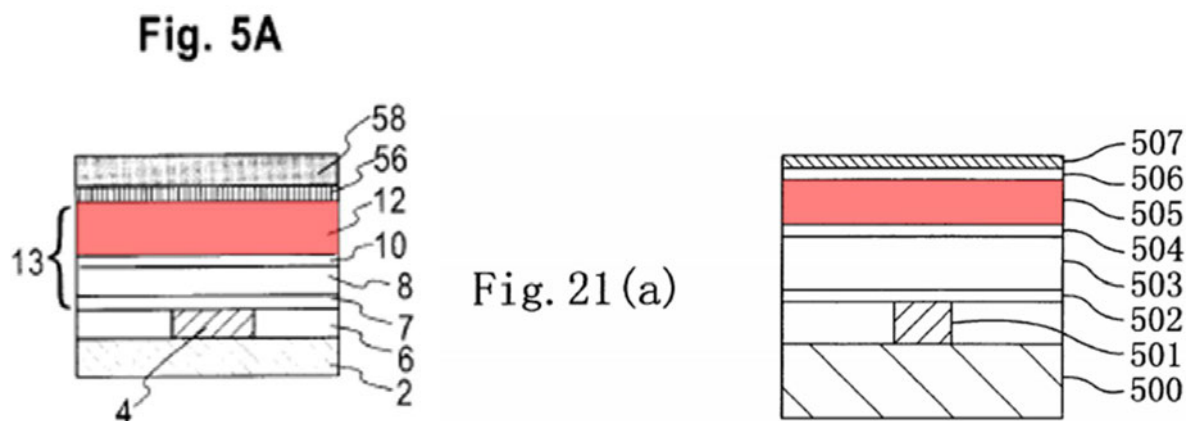
**c. [13.3] *Grill* discloses “forming a second insulating film”**

Claim 13 recites “forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film.”

*Grill* discloses “wiring level dielectric 12,” which “might be carbon-based materials such as DLC or fluorinated DLC (FDLC), SiCO or SiCOH compounds, or organic or inorganic polymer dielectrics.” (Ex. 1005, 4:1–13.) A POSITA would have understood that the disclosed wiring level dielectric [12] is an insulating film. (Ex. 1002, ¶174.)

*Grill* teaches that etch stop [10] “might be a silicon-containing material such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiO<sub>x</sub>N<sub>y</sub>, SiCOH compounds, silicon-containing DLC (SiDLC), etc.” *Grill* therefore teaches a wiring level dielectric [12] and etch stop [10] having

different compositions (e.g., FDLC and SiOxNy, respectively). (Ex. 1005, 4:1–13.) As *Grill*'s Figure 5A shows below, a POSITA would have understood that the wiring level dielectric [12] is located over etch stop [10]. (Ex. 1002, ¶175; *see also* Ex. 1005, Fig. 5A; *supra* §III.A.2.) Figure 21(a) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶173–76.)

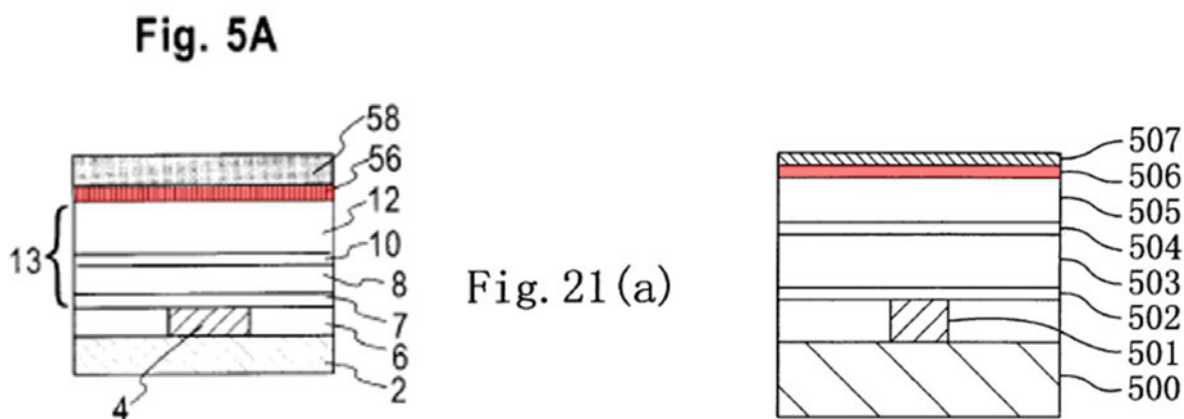


**d. [13.4] *Grill* discloses “forming a third insulating film”**

Claim 13 recites “forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film.” *Grill* discloses “lower hard mask layer 56,” which is “preferably formed from different materials which have different etch properties from . . . the dielectric underlayer[] 12.” (Ex. 1005, 7:31–35; *see also id.*, 4:1-13, 7:38-42.) “[S]uitable hard mask materials may include SiO<sub>2</sub>-based materials, other oxides, nitrides other than Si<sub>3</sub>N<sub>4</sub>, carbon-based dielectrics, SiC-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.” (*Id.*, 7:38–42.) A POSITA would

have understood that the lower hard mask layer [56] is an insulating film that has a different composition than the wiring level dielectric [12]. (Ex. 1002, ¶178.)

As *Grill*'s Figure 5A shows below, a POSITA would have understood that the lower hard mask layer [56] is located over the wiring level dielectric [12]. (Ex. 1002, ¶179; *see also* Ex. 1005, Fig. 5A; *supra* §III.A.3.) Figure 21(a) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶177–80.)

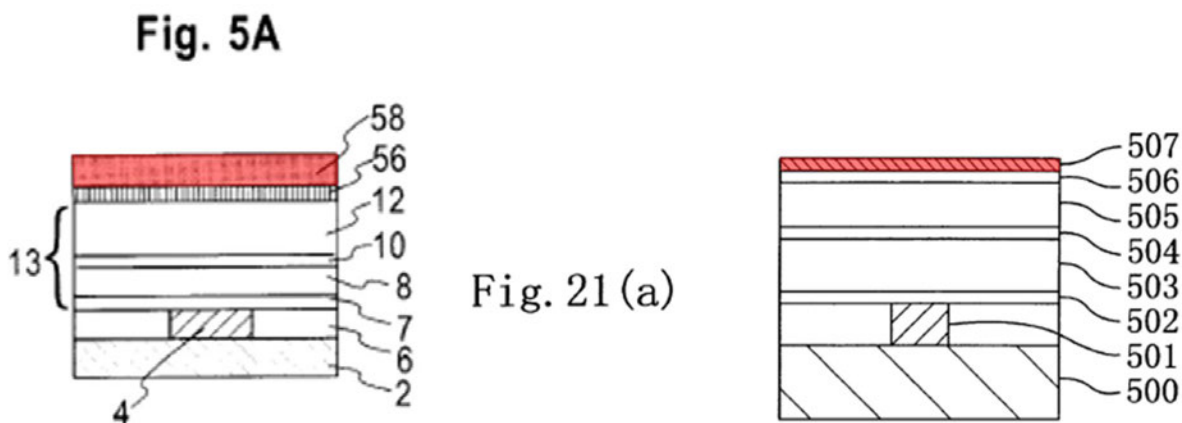


**e. [13.5] *Grill* discloses “forming a thin film”**

Claim 13 recites “forming a thin film over the third insulating film.” *Grill* discloses “upper hard mask layer 58,” which “might be formed from SiO<sub>2</sub>.” (Ex. 1005, 7:31–35.) “Other suitable hard mask materials may include SiO<sub>2</sub>-based materials, other oxides, nitrides other than Si<sub>3</sub>N<sub>4</sub>, carbon-based dielectrics, SiC-based dielectrics, polycrystalline silicon, amorphous hydrogenated silicon, and metals.” (*Id.*, 7:38–42.) In one example, *Grill* states that the upper hard mask layer “might be formed from a 40 nm thickness of Si<sub>3</sub>N<sub>4</sub>.” (*Id.*, 8:29–31.) A

POSITA would have understood that the upper hard mask layer [58] is a thin film. (Ex. 1002, ¶182.)

As *Grill*'s Figure 5A shows below, a POSITA would have understood that the upper hard mask layer [58] is located over the lower hard mask layer [56]. (Ex. 1002, ¶183; *see also* Ex. 1005, Fig. 5A; *supra* §III.A.4.) Figure 21(a) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶181–84.)

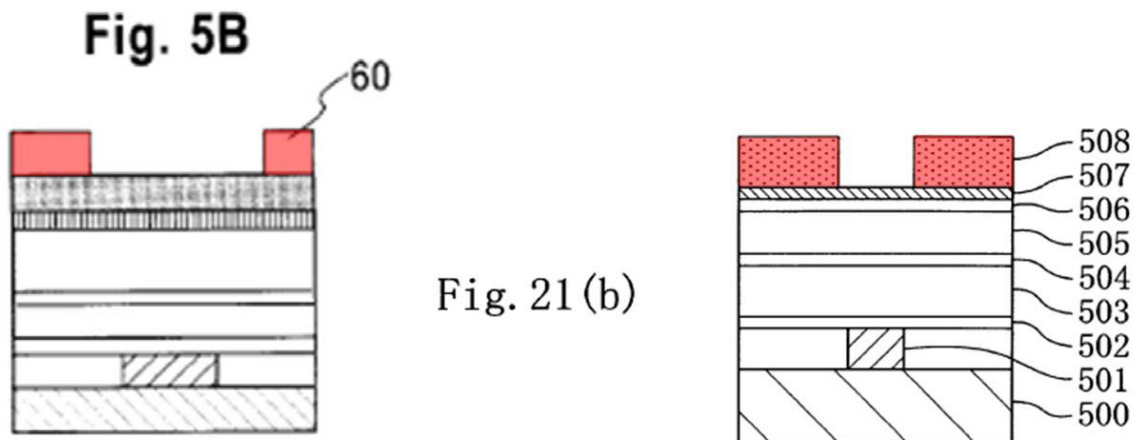


**f. [13.6] *Grill* discloses “forming a first resist pattern”**

Claim 13 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.” *Grill* states, “A first resist layer 60, patterned with a first (wiring level) pattern, is formed on layer 58.” (Ex. 1005, 7:42–44, Fig. 5B.) This is depicted in *Grill*'s Figure 5B below. (*See also supra* §III.A.5.) A POSITA would have understood that the first resist layer [60] is located on the upper hard mask layer [58] and that its opening corresponds to a



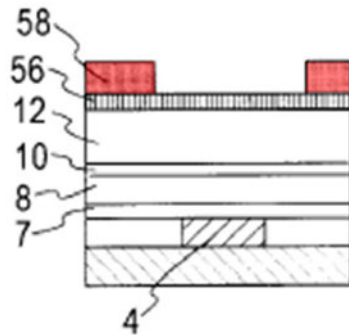
wiring groove. (Ex. 1002, ¶185.) Figure 21(b) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶185–86.)



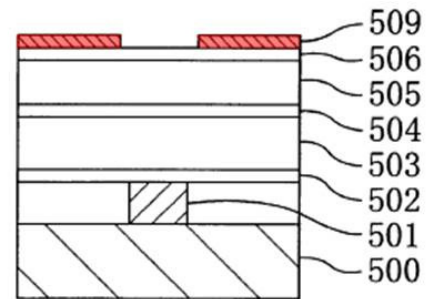
**g. [13.7] *Grill* discloses “etching the thin film”**

Claim 13 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.” *Grill* states, “The pattern of resist layer 60 [the wiring level pattern] is transferred into upper hard mask layer 58 by an etching process.” (Ex. 1005, 7:42–47, Fig. 5C.) This is depicted in *Grill*’s Figure 5C below. (*See also supra* §III.A.6.) A POSITA would have understood that the resist layer [60] masks the upper hard mask [58] and that the width of the openings in upper hard mask [58] correspond to the wiring grooves. (Ex. 1002, ¶188.) Figure 22(a) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶187–89.)

**Fig. 5C**

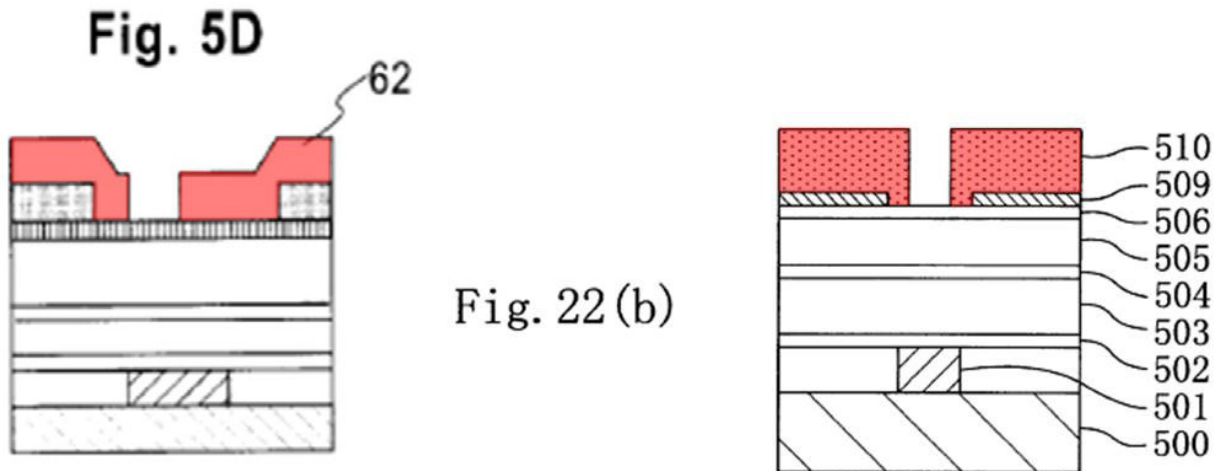


**Fig. 22(a)**



**h. [13.8] *Grill* discloses “removing the first resist pattern and then forming a second resist pattern”**

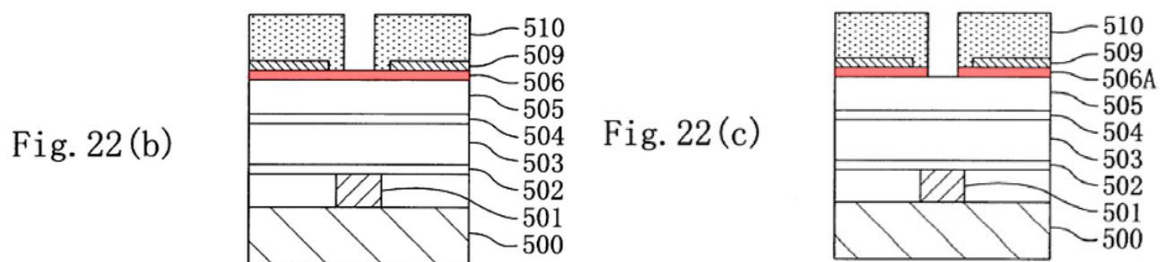
Claim 13 recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.” *Grill* states, “Patterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (Ex. 1005, 7:51–55, Figs. 5B, 5C, 5D.) As *Grill*’s Figure 5D shows below, a POSITA would have understood that the second resist layer [62] is formed on the lower hard mask layer [56] and the mask pattern [58]. (*Id.*, Fig. 5D; *see also supra* §III.A.7.) Figure 22(b) from the fifth embodiment of the ’696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶190–92.)



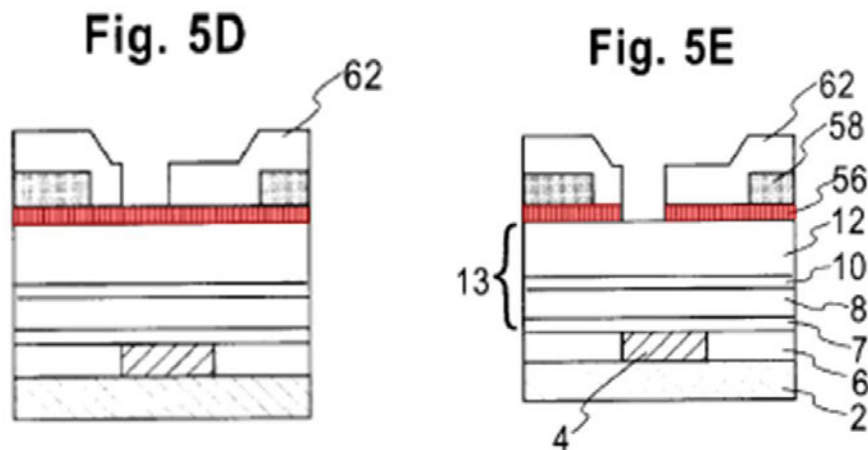
i. [13.9] *Grill* discloses “dry-etching the third insulating film”

Claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

The '696 patent explains, “the second silicon dioxide film 506 is dry-etched using the second resist pattern 510 and the mask pattern 509 as a mask, thereby forming a patterned second silicon dioxide film 506A having openings for forming contact holes as shown in FIG. 22(c).” (Ex. 1001, 23:42–46.) Figures 22(b) and 22(c) of the '696 patent appear below with highlights.



*Grill* discloses the exact same thing, as highlighted Figures 5D and 5E show below. (Ex. 1005, 7:57–66, Figs. 5D, 5E; Ex. 1002, ¶¶193–97.)



In describing this etch step, *Grill* states, “The pattern of resist layer 62 [the via level pattern] is then transferred into lower hard mask layer 56.” (Ex. 1005, 7:57–61, Fig. 5E.) As *Grill*’s Figures 5D and 5E show above, and based on the description of the ’696 patent, a POSITA would have understood that the resist layer [62] and the upper hard mask [58] mask the lower hard mask [56] during etching in the manner described in the ’696 patent. (Ex. 1002, ¶¶193–97; *see also supra* §III.A.8.) A POSITA would have further understood that the lower hard mask layer [56] has openings for forming contact holes because it contains the via level pattern of the second resist layer 62. (Ex. 1005, 7:51–55, Figs. 5B, 5C, 5D; Ex. 1002, ¶195.) Additionally, a POSITA would have understood that the second resist pattern [62] is transferred into the lower hard mask layer [56] by dry etching. (Ex. 1002, ¶196.) Layer 56 may be Si<sub>3</sub>N<sub>4</sub> (Ex. 1005, 7:34–37), and the etch in

Figures 5D and 5E is anisotropic to preserve the dimensions of the via level pattern (Ex. 1002, ¶196). Because a POSITA would have understood that anisotropic etches of Si<sub>3</sub>N<sub>4</sub> are dry etches, a POSITA would have understood this is a dry etching step. (*Id.*)

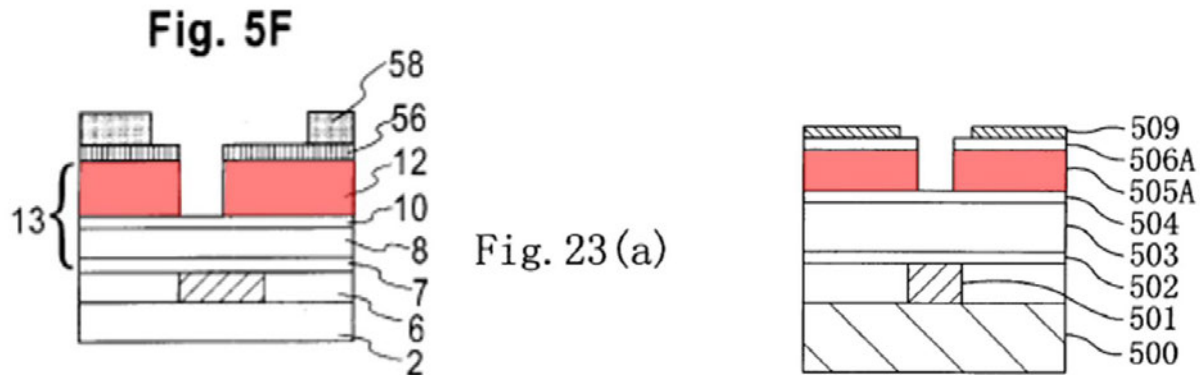
**j. [13.10] *Grill* discloses “dry-etching the second insulating film”**

Claim 13 recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.” *Grill* states that “[t]he via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (Ex. 1005, 7:62–63, Fig. 5F.) As *Grill*’s Figure 5F shows below,<sup>5</sup> a POSITA would have understood that the wiring level dielectric [12] has openings for forming contact holes. (Ex. 1002, ¶199; *see also supra* §III.A.9.) Figure 23(a)

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<sup>5</sup> “Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12.” (Ex. 1005, 7:64–66; Ex. 1002, ¶199 & n.3.) Lower hard mask [56] acts as a mask as the second resist pattern [62] is removed during the etch process. (*Id.*, ¶199.) The fifth, modified fifth, sixth, and modified sixth embodiments of the ’696 patent teach the same. (Ex. 1001, 23:47–59, 25:66–26:14, 28:49–61, 30:58–31:6, Figs. 23(a), 26(a), 31(c), 34(c).)

from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶198–200 & n.3.)



**k. [13.11] *Grill* discloses “dry-etching the patterned third insulating film and the first insulating film”**

Claim 13 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.” *Grill* states, “The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.” (Ex. 1005, 7:67–8:2, Fig. 5G.) As *Grill*’s Figures 5F and 5G show below, a POSITA would have understood that upper hard mask [58] masks lower hard mask [56], and wiring level dielectric [12] masks etch stop [10]. (Ex. 1002, ¶¶201–04.) Figures 23(a) and 23(b) from the fifth embodiment of the '696 patent show the same. (*See also* Ex. 1001, 23:66–24:6.)

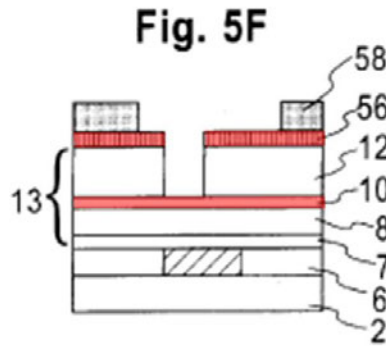


Fig. 23(a)

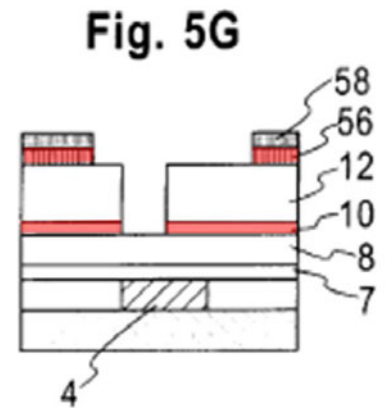
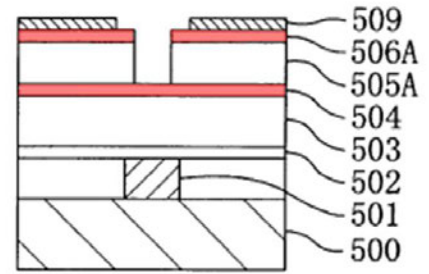
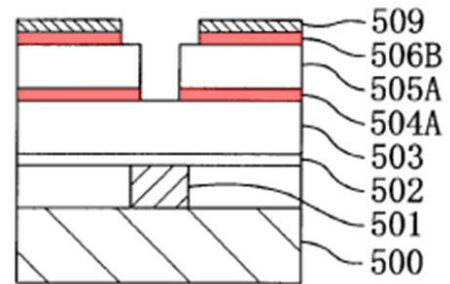


Fig. 23(b)



These Figures further clarify that the width of the hole in the lower hard mask [56] corresponds to the wiring groove, and the width of the hole in etch stop [10] corresponds to the width of the contact hole.<sup>6</sup> (Ex. 1002, ¶203; *see also supra* §III.A.10; Ex. 1001, 23:66–24:6.)

<sup>6</sup> A contact hole in the '696 patent is part of the final via that extends from the lower-level metal interconnect to the upper-level metal interconnect. Some openings for forming contact holes are removed before the final structure. (Ex. 1001, 23:40–42, 25:27–29, 28:49–51, 30:49–51, Figs. 22(b), 25(b), 27(b), 31(b), 34(b).) Others become wiring grooves. (*Id.*, 23:42–46, 25:66–26:3, 28:51–55,

**I. [13.12] *Grill* discloses “filling in the wiring grooves”**

Claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.”

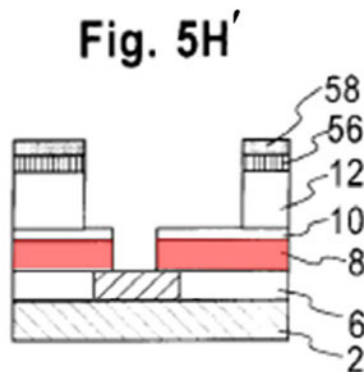
A POSITA would have understood that, before performing this claimed step, an additional etch is required to remove the layer immediately above the conductive via [4] to expose the conductive via [4]. (Ex. 1002, ¶¶206–07; Ex. 1005, 8:2–8, Fig. 5H.) The fifth and sixth embodiments of the ’696 patent expressly teach this additional, unclaimed etch step. In describing the fifth embodiment, the ’696 patent discloses that, after forming contact holes in the first insulating film, “silicon nitride film 502 is dry-etched using the patterned first silicon dioxide film 504A as a mask, thereby forming a patterned first silicon nitride film 502A (see FIG. 23(d)) and exposing the first metal interconnects 501 within the contact holes 512.” (Ex. 1001, 24:14–18; *see also id.* at 29:13–20, Fig. 23(c), Fig. 32(b)). Because claim 13 uses the open-ended transitional phrase

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30:58–62, Figs. 23(a), 26(a), 28(b), 31(c), 34(c).) Some, such as patterns 504A and 554A, are contact holes in the final structure. (*See id.*, Figs. 23(d), 26(d); Ex. 1002, ¶203.) The aperture in *Grill*’s etch stop [10] is the same as layers 504A and 554A. They begin as openings for forming contact holes and remain contact holes in the final structure. (Ex. 1002, ¶203; *see also* Ex. 1001, Figs. 23(d), 26(d).)



“comprising,” the absence of any tie of this intermediary step to claim 13 is inconsequential. Prior art that discloses all of the claimed steps of claim 13, like *Grill*, invalidates claim 13 regardless of the presence any unclaimed steps. *See, e.g., Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009). A POSITA would have understood the unclaimed etch of *Grill*, as depicted in Figure 5H'.<sup>7</sup> (Ex. 1002, ¶¶206–07; *compare also supra* §III.A.10, *with supra* §III.A.11.)



Thus, a POSITA would have understood that, in *Grill*'s embodiment that does not have optional layer 7, conductive via [4] is exposed after progressing to the step in Figure 5H'. (Ex. 1002, ¶207.) Because the conductive via [4] is already

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<sup>7</sup> Figure 5H' is the Petitioner's depiction of the *Grill* embodiment that omits optional layer 7, and was modified for this Petition. It depicts what a POSITA would have understood regarding *Grill*'s alternative embodiment without optional layer 7. (Ex. 1002, ¶206 & n.4.)

exposed, a POSITA also would have understood that the additional step in Figure 1J of *Grill* is unnecessary and likely harmful to the device. (*Id.*) The wiring level pattern would not be transferred into etch stop 10.<sup>8</sup> (*Id.*)

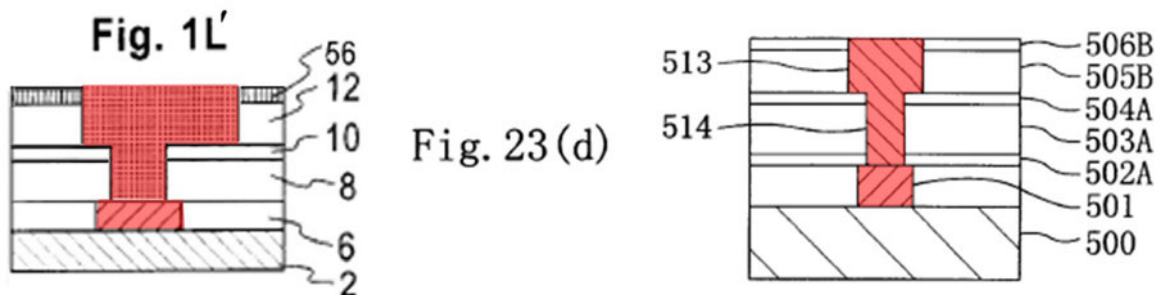
For the step of filling the wiring grooves, *Grill* states, “Cavity 20 is . . . overfilled with conductive wiring material 22, by a process such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (Ex. 1005, 4:64–5:2, Fig. 1K.) Then, the conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Id.*, 5:2–8, Fig. 1L.) As Figure 1L’ shows,<sup>9</sup> a POSITA would have understood that, if layer 7 were absent, metal would fill the contact holes in etch stop [10] and via level dielectric [8] and fill the wiring grooves in the lower hard

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<sup>8</sup> Even if the optional passivation/adhesion layer [7] is used, a POSITA would have understood that in many cases it is desirable not to etch the etch stop [10] as the passivation/adhesion layer [7] is etched, by using a selective etch. (*See, e.g.*, Ex. 1010, 6:25–29, 6:62–7:2, 7:15–18, 7:55–65, Fig. 10; Ex. 1002, ¶207 & n.5.)

<sup>9</sup> Figure 1L’ is the Petitioner’s depiction of the *Grill* embodiment that omits optional layer 7, and was created for this Petition. It depicts what a POSITA would have understood regarding *Grill*’s alternative embodiment without optional layer 7. (Ex. 1002, ¶208 & n.6.)

mask [56] and wiring level dielectric [12]. (Ex. 1002, ¶¶208; *see also supra* §III.A.11.) Figure 23(d) from the fifth embodiment of the '696 patent appears below for comparison. (*See also* Ex. 1002, ¶¶205–09.)



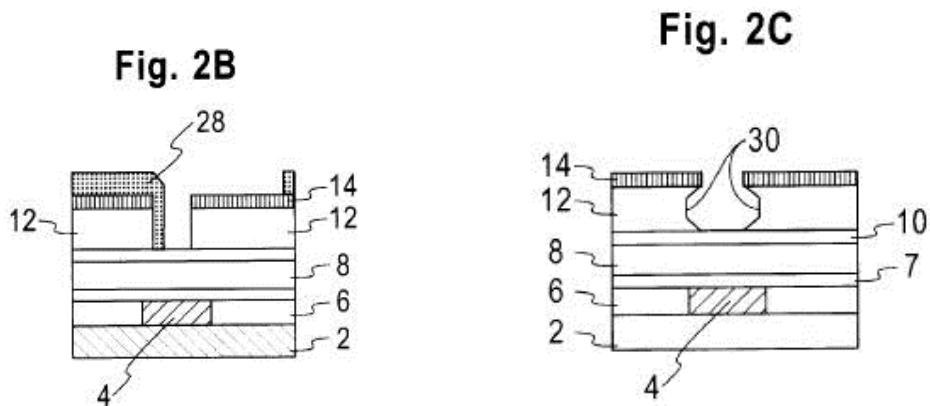
### C. The Combination of *Grill* and *Aoyama* Renders Claims 13 and 15 Obvious

As detailed below, the *Grill-Aoyama* combination is very similar to the modified fifth embodiment of the '696 patent. As in section V.B, the analysis reflects *Grill*'s disclosure that the dielectric passivation/adhesion layer 7 is optional. (Ex. 1005, 4:1–5, 4:61–63.) A POSITA would have understood that the disclosed embodiment of *Grill* at 4:60–5:8 and 7:16–8:8, without optional layer 7, as combined with the relevant teachings of *Aoyama*, is a process that meets every limitation of claims 13 and 15 and renders them obvious.

#### 1. A POSITA would have combined the relevant teachings of *Grill* and *Aoyama*

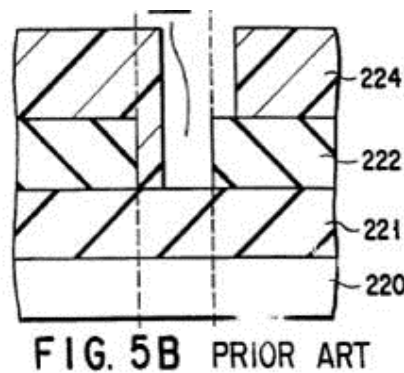
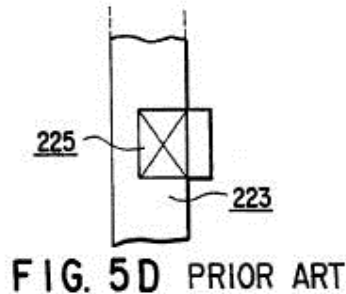
A POSITA would have found it obvious to combine certain teachings of *Grill* and *Aoyama*. (Ex. 1002, ¶¶157–65.) One of the problems *Grill* sought to address was the problem of “lithographic rework” because of misalignment

between the via and wiring patterns during photolithography. (Ex. 1005, 2:26–38.) Organic and other low-k materials may have similar etch characteristics to photoresist, so stripping a misaligned photoresist pattern may not only remove the photoresist but also damage the underlying dielectric. (*Id.*, 2:26–32.) To address this problem, *Grill* uses two hard masks on top of the wiring-level dielectric. (*Id.*, 2:64–3:6, Fig. 5A.) In this way, lithographic alignment for both via and wiring levels is completed and transferred into thin films on the surface of the device before the underlying inter-level dielectrics are exposed. (*Id.*, 2:64–3:1.) As Figures 2B and 2C of *Grill* show below, stripping misaligned photoresist 28 can damage inter-layer dielectric 12 and make it difficult to control the critical dimension of the via pattern. (*Id.*, 5:13–33.)

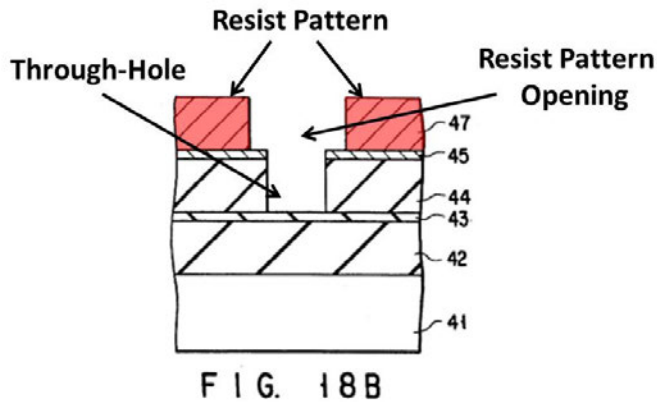


*Aoyama* solves a related problem involving misalignment. *Aoyama* explains that misalignment of the photomask during via formation can cause the via dimensions to be too small and the wiring dimensions to be too large. (Ex. 1018, 3:18–21, 3:29–32, Figs. 5B, 5D (shown below).) This leads to an increase in

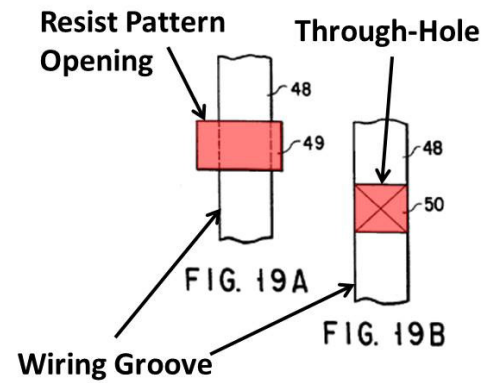
contact resistance, a degradation in reliability, and difficulty in achieving higher integration density. (*Id.*, 3:33–38, 6:7–14.)



*Aoyama* discloses a resist pattern with a via opening wider than the wiring groove. (*Id.*, 16:3–5, Figs. 18B, 19A (each below with annotations and highlights).) This added width increases misalignment tolerance since the width of the via is defined by the width of the wiring groove. (*Id.*, 16:14–16.) Thus, a via having the same width as the wiring groove is formed even when misaligned. (*Id.*, 16:14–16, Fig. 19B (below with highlight and annotations).)



*Side View*



*Top View*

*Aoyama* does not completely eliminate the possibility of a misaligned photomask. (Ex. 1002, ¶161.) A wider via opening in the photomask may provide increased misalignment tolerance, but it does not guarantee proper alignment. (*Id.*) For example, the misalignment in Figure 5D above is still possible even with the wider pattern in Figure 19A. (*Id.*)

A POSITA would have appreciated that *Grill*'s and *Aoyama*'s solutions complement one another in addressing the problem of misalignment in semiconductor damascene processes. (Ex. 1002, ¶162.) When misalignment occurs, *Grill*'s structure permits lithographic rework without damaging the inter-level dielectrics below. (Ex. 1005, 2:26–38; Ex. 1002, ¶162.) The wider via pattern of *Aoyama* reduces instances of misalignment, preventing the time-consuming, inefficient, and costly process of photolithographic rework. (Ex. 1002, ¶162.)

A POSITA would have further found it obvious to combine *Grill*'s two hard masks with *Aoyama*'s widened through-hole pattern without modifying the *Grill* process. (*Id.*, ¶163.) Nothing about the width of the via pattern in *Aoyama* affects the dual-hard mask structure of *Grill*, and nothing about the dual-hard mask structure of *Grill* affects the width of the via pattern in *Aoyama*. (*Id.*)

A POSITA would have understood that the combination of *Aoyama* and *Grill* predictably reduces instances of misalignment and permits lithographic rework when misalignment occurs. (Ex. 1002, ¶164.) This combination therefore avoids increased contact resistance, degradation of reliability, and damage to the inter-layer dielectrics from misalignment, and facilitates higher integration density. (Ex. 1005, 2:26–38, 2:64–3:6, 5:13–33; Ex. 1018, 3:33–38, 6:7–14; Ex. 1002, ¶164.)

In the language of *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007), the combination of *Grill* and *Aoyama* is merely a combination of familiar elements according to known methods to yield predictable results; use of known techniques to improve similar devices, methods, or products in the same way; and application of known techniques to known devices, methods, or products ready for improvement to yield predictable results. (*See, e.g.*, Ex. 1005, 2:26–38, 2:64–3:6, 5:13–33; Ex. 1018, 3:33–38, 6:7–14; Ex. 1002, ¶165.)

**2. Claim 13 is obvious in view of the *Grill-Aoyama* combination**

**a. [13.1] *Grill* discloses the preamble of claim 13**

The preamble of claim 13 recites “[a] method for forming an interconnection structure.” As discussed in section V.B.1.a, *Grill* discloses this feature.

**b. [13.2]–[13.5] *Grill* discloses forming first, second, and third insulating films, and a thin film**

Claim 13 recites “forming a first insulating film over lower-level metal interconnects; forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; [and] forming a thin film over the third insulating film.”

As discussed in sections V.B.1.b through V.B.1.e, *Grill* discloses these features. Figure 5A of *Grill* and Figure 24(a) from the modified fifth embodiment of the ’696 patent appear below with annotations and highlights for comparison. The first insulating film corresponds to *Grill*’s layer 10 (and the ’696 patent’s layer 554). The second insulating film corresponds to *Grill*’s layer 12 (and the ’696 patent’s layer 555). The third insulating film corresponds to *Grill*’s layer 56 (and the ’696 patent’s layer 556). The thin film corresponds to *Grill*’s layer 58 (and the ’696 patent’s layer 557). (*Compare* Ex. 1005, 3:60–4:13, 7:30–42, *with*, Ex. 1001, 24:60–25:11; Ex. 1002, ¶213.)



Fig. 5A

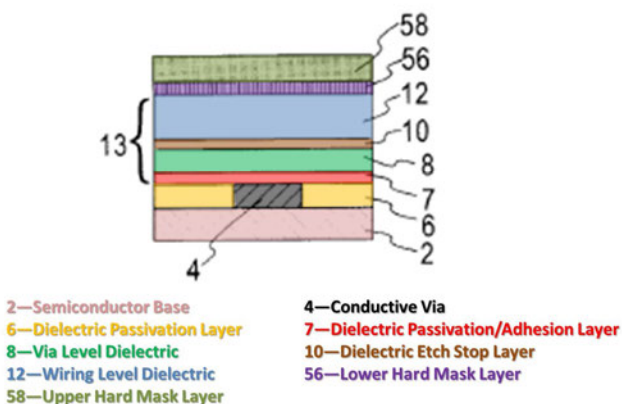
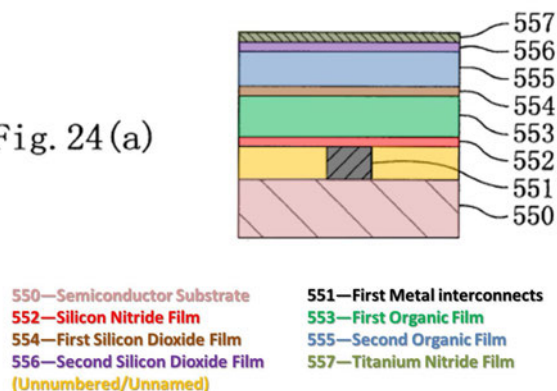


Fig. 24(a)



c. [13.6] *Grill* discloses “forming a first resist pattern”

Claim 13 recites “forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves.” As discussed in section V.B.1.f, *Grill* discloses this feature. Figure 5B of *Grill* and Figure 24(b) from the modified fifth embodiment of the ’696 patent appear below with highlights for comparison. The first resist pattern corresponds to *Grill*’s layer 60 (and the ’696 patent’s layer 558). (*Compare* Ex. 1005, 7:42–44, with Ex. 1001, 25:19–21; *see also* Ex. 1002, ¶215.)

Fig. 5B

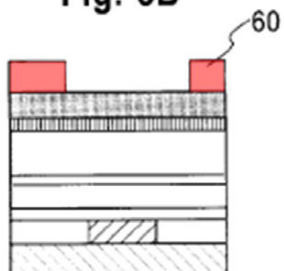
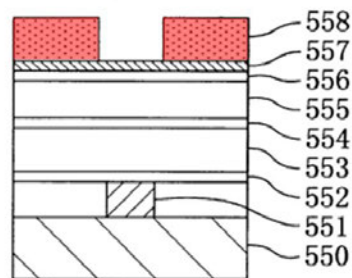


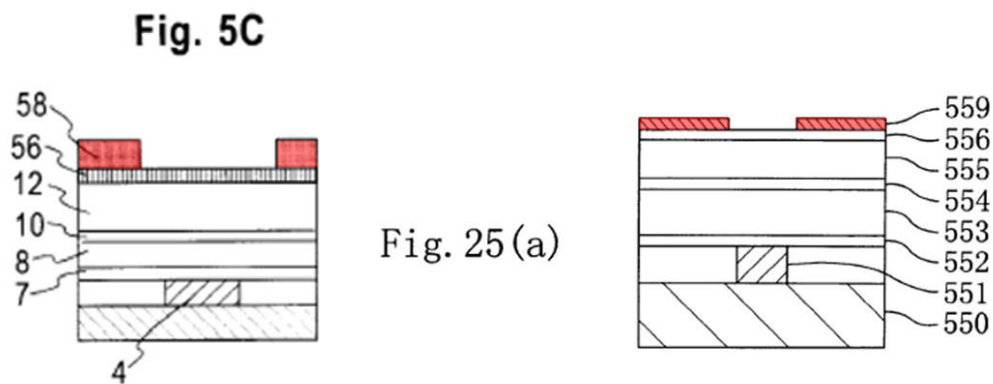
Fig. 24(b)



**d. [13.7] *Grill* discloses “etching the thin film”**

Claim 13 recites “etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves.” As discussed in section V.B.1.g, *Grill* discloses this feature. Figure 5C of *Grill* and Figure 25(a) from the modified fifth embodiment of the '696 patent appear below with highlights for comparison. The mask pattern corresponds to *Grill*'s patterned layer 58 (and the '696 patent's layer 559).

(Compare Ex. 1005, 7:45–50, with, Ex. 1001, 25:21–25; see also Ex. 1002, ¶217.)



**e. [13.8] The *Grill-Aoyama* combination discloses “removing the first resist pattern and then forming a second resist pattern”**

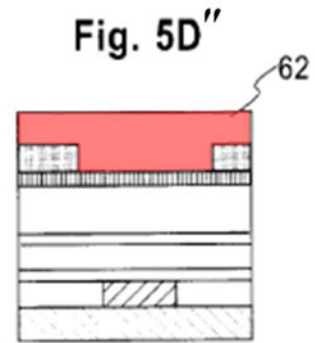
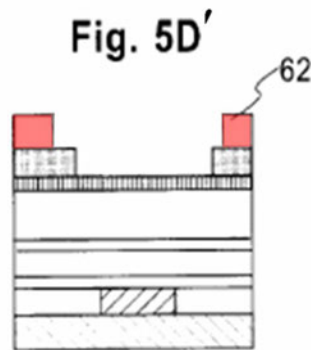
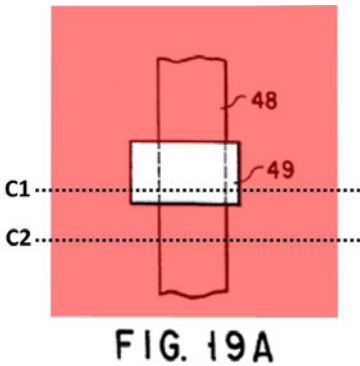
Claim 13 recites “removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes.” The *Grill-Aoyama* combination discloses this feature. (Ex. 1002, ¶¶218–23.)

*Grill* states, “Patterned resist layer 60 is then removed by a process such as ashing or wet chemical etching, and a second resist layer 62, patterned with a second (via level) pattern, is then formed on the structure.” (Ex. 1005, 7:51–55, Figs. 5B, 5C, 5D.)

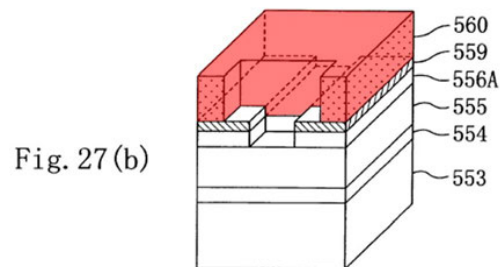
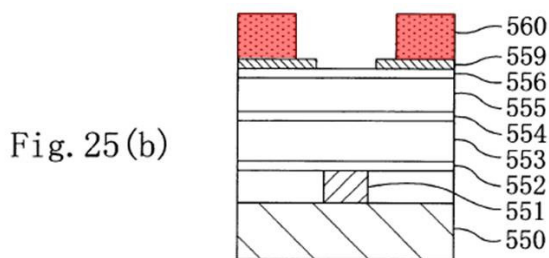
A POSITA would have understood that second resist layer 62 is formed on the lower hard mask [56] and the mask pattern [58] in the *Grill-Aoyama* combination. (Ex. 1002, ¶220.) Figure 19A below shows the shape of *Aoyama*’s through-hole, viewed from above. The areas colored red in Figure 19A indicate that photoresist is located in the areas other than the through-hole location. (*Id.*, ¶221.) Two dashed lines have been added to indicate cross-sections C1 and C2. Element 48 is a trench. (Ex. 1018, 16:18–21.) Cross-section C1 of the *Grill-Aoyama* combination appears below in Figure 5D’.<sup>10</sup> (Ex. 1002, ¶221.) Cross-section C2 of the *Grill-Aoyama* combination appears below in Figure 5D”. (*Id.*) The Figures below show that the second resist pattern is on the lower hard mask [56] and the mask pattern [58]. (*Id.*)

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<sup>10</sup> The prime in a figure number indicates that it has been modified from the original *Grill* figure by Petitioner.



Figures 25(b) and 27(b) from the modified fifth embodiment of the '696 patent appear below with highlights for comparison. (*See also* Ex. 1001, Fig. 37(a).) According to the '696 patent, “a second resist pattern 560, having openings for forming contact holes, is formed by lithography on the mask pattern 559 as shown in FIG. 25(b).” (Ex. 1001, 25:27–35.)



**f. [13.9] The *Grill-Aoyama* combination discloses “dry-etching the third insulating film”**

Claim 13 recites “dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes.”

*Grill* states, “The pattern of resist layer 62 [the via level pattern] is then transferred into lower hard mask layer 56.” (Ex. 1005, 7:57–61, Fig. 5E.) As

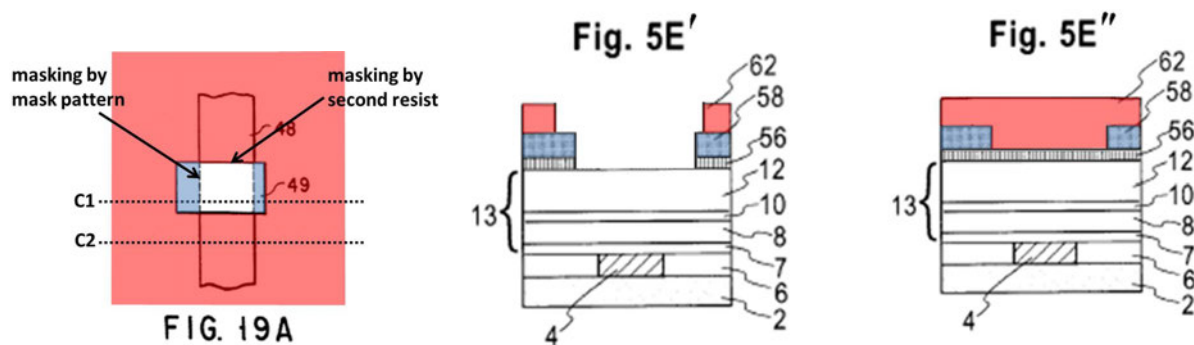
explained in section V.B.1.i, a POSITA would have understood that the lower hard mask layer [56] has openings for forming contact holes because it contains the via level pattern of the second resist layer 62. (Ex. 1005, 7:51–55; Ex. 1002, ¶225.)

As section V.B.1.i also explains, a POSITA would have understood that dry etching transfers second resist pattern [62] into the lower hard mask layer [56].

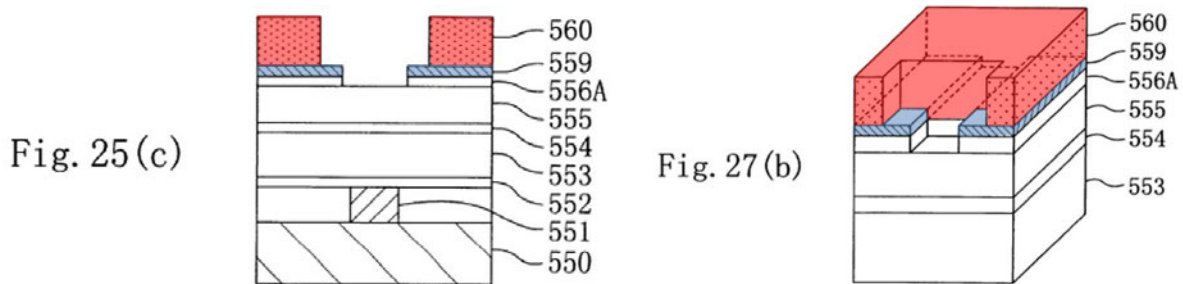
(Ex. 1002, ¶225.)

A POSITA would have further understood that the lower hard mask [56] is etched using the second resist pattern [62] and the mask pattern [58] as masks.

(*Id.*, ¶226.) Figure 19A below shows the shape of *Aoyama*'s through-hole, viewed from above. The red areas indicate photoresist [62], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination appears below in Figure 5E'. (*Id.*, ¶227.) Cross-section C2 of the *Grill-Aoyama* combination appears below in Figure 5E''. (*Id.*) The Figures below show masking during the etch by mask pattern [58] and second resist layer [62]. (*Id.*)



Figures 25(c) and 27(b) from the modified fifth embodiment of the '696 patent appear below with highlights for comparison. (See also Ex. 1001, Fig. 37(a).) According to the '696 patent, “the second silicon dioxide film 556 is dry-etched using the second resist pattern 560 and the mask pattern 559 as a mask, thereby forming a patterned second silicon dioxide film 556A having openings for forming contact holes.” (Ex. 1001, 25:36–41.)



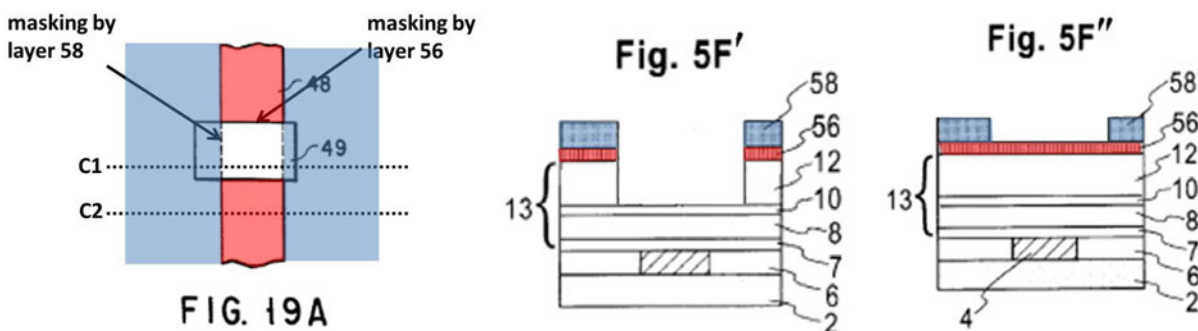
**g. [13.10] The *Grill-Aoyama* combination discloses “dry-etching the second insulating film”**

Claim 13 recites “dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes.”

*Grill* states that “[t]he via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching.” (Ex. 1005, 7:62–63, Fig. 5F.) A POSITA would have understood that the lower hard mask [56] acts as a mask during this etch in the *Grill-Aoyama* combination. (Ex. 1002, ¶¶231–32.)

Figure 19A below shows the top surface of *Aoyama*’s structure, as viewed from above. The resist pattern [62] is removed during the etch of dielectric layer

12, thereby exposing the mask pattern [58] and lower hard mask [56]. (Ex. 1005, 7:64–66, Figs. 5E, 5F.) The red areas of Figure 19A indicate the lower hard mask [56], and the blue areas indicate the mask pattern [58]. Cross-section C1 of the *Grill-Aoyama* combination appears below in Figure 5F'. (Ex. 1002, ¶232.) Cross-section C2 of the *Grill-Aoyama* combination appears below in Figure 5F''. (*Id.*) The Figures below show masking during the etch by lower hard mask [56], as well as by mask pattern [58]. (*Id.*)



Figures 26(a) and 28(a) from the modified fifth embodiment of the '696 patent appear below with highlights for comparison. (*See also* Ex. 1001, Fig. 37(a).) According to the '696 patent, “the second organic film 555 is dry-etched using the patterned second silicon dioxide film 556A as a mask, thereby forming a patterned second organic film 555A having openings for forming contact holes.” (Ex. 1001, 25:66–26:3.)

Fig. 26(a)

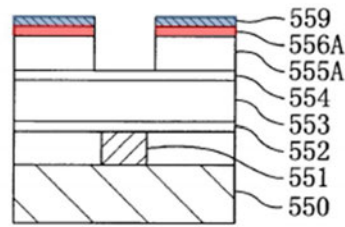
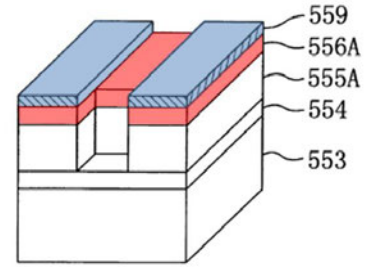


Fig. 28(a)



**h. [13.11] The *Grill-Aoyama* combination discloses “dry-etching the patterned third insulating film and the first insulating film”**

Claim 13 recites “dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively.”

*Grill* states, “The etching conditions are then changed to removed [sic] exposed portions of lower hard mask layer 56 and optional etch stop 10.” (Ex. 1005, 7:67–8:2, Fig. 5G.) A POSITA would have understood that in the *Grill-Aoyama* combination, upper hard mask [58] masks lower hard mask [56] in the wiring groove and wiring level dielectric [12] masks etch stop [10] in the contact hole. (Ex. 1002, ¶¶203, 236; *see also supra* §V.B.1.k, at n.6.) A POSITA also would have understood that this etch is a dry etch. (*Id.*)

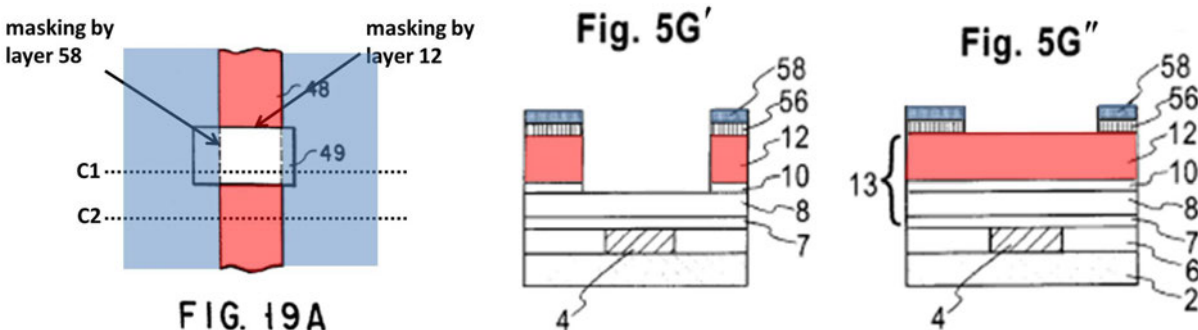
Figure 19A below shows the top surface of *Aoyama*’s structure, as viewed from above. The red areas of Figure 19A indicate the patterned second insulating film [12], and the blue areas indicate the mask pattern [58]. Cross-section C1 of



the *Grill-Aoyama* combination appears below in Figure 5G'. (Ex. 1002, ¶237.)

Cross-section C2 of the *Grill-Aoyama* combination appears below in Figure 5G".

(*Id.*) The Figures below show masking during the etch by the patterned second insulating film [12], as well as by the mask pattern [58]. (*Id.*)



Figures 26(b) and 28(b) from the modified fifth embodiment of the '696 patent appear below with highlights for comparison. (*See also* Ex. 1001, Fig. 37(a).) According to the '696 patent, "the patterned second silicon dioxide film 556A and the first silicon dioxide film 554 are dry-etched using the mask pattern 559 and the patterned second organic film 555A as respective masks, thereby forming a patterned second silicon dioxide film 556B having openings for forming wiring grooves and a patterned first silicon dioxide film 554A having openings for forming contact holes." (Ex. 1001, 26:15–22.)

Fig. 26 (b)

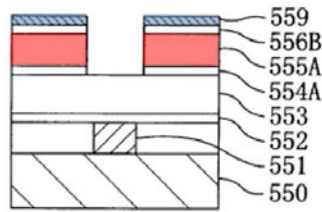
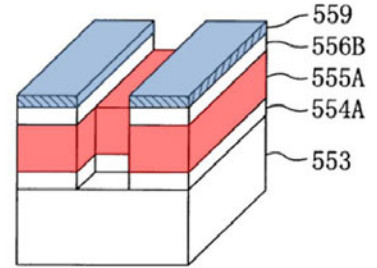


Fig. 28 (b)



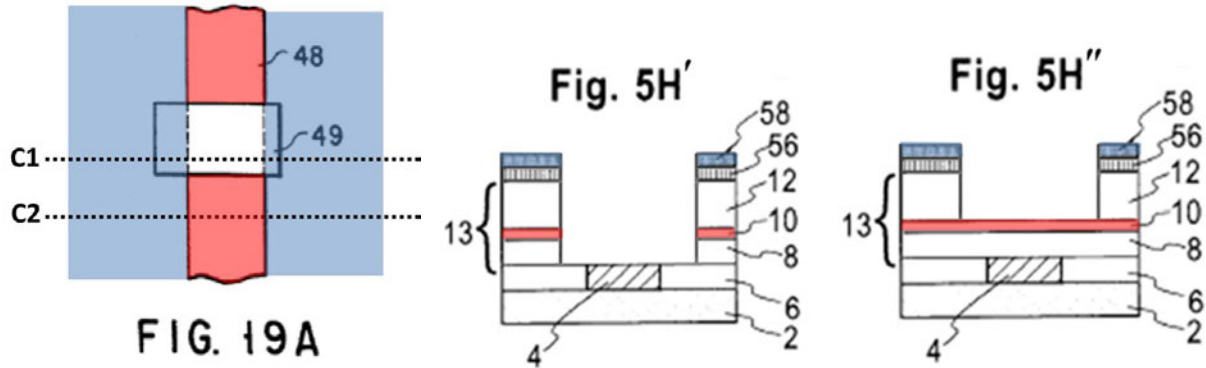
**i. [13.12] The *Grill-Aoyama* combination discloses “filling in the wiring grooves”**

Claim 13 recites “filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.” A POSITA would have understood that, before performing this claimed step, an additional etch is required to remove the layer immediately above the conductive via [4] to expose the conductive via [4]. (Ex. 1002, ¶241; Ex. 1005, 8:2–8; *supra* §V.B.1.1.) As explained in section V.B.1.1, the ’696 patent expressly teaches this additional, unclaimed etch step. (Ex. 1001, 24:14–18; *see also id.* at 29:13–20, Fig. 23(c), Fig. 32(b).)

Because claim 13 uses the open-ended transitional phrase “comprising,” the absence of any tie of this intermediary step to claim 13 is inconsequential. Prior art that discloses all of the claimed steps of claim 13, like the *Grill-Aoyama* combination, invalidates claim 13 regardless of the presence any unclaimed steps. *See, e.g., Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009). A POSITA would have understood the unclaimed etch of the *Grill-Aoyama*

combination as depicted in Figures 19A, 5H', and 5H''.<sup>11</sup> (Ex. 1002, ¶241.)

Figures 5H' and 5H'' depict cross-sections C1 and C2 of Figure 19A.



Thus, a POSITA would have understood that the conductive via [4] is exposed after progressing to the step shown above. (Ex. 1002, ¶242.) Because the conductive via [4] is already exposed, a POSITA would have also understood that the additional step in Figure 1J of *Grill* is unnecessary and likely harmful. (*Id.*) The wiring level pattern, therefore, would not be transferred into etch stop 10.<sup>12</sup> (*Id.*)

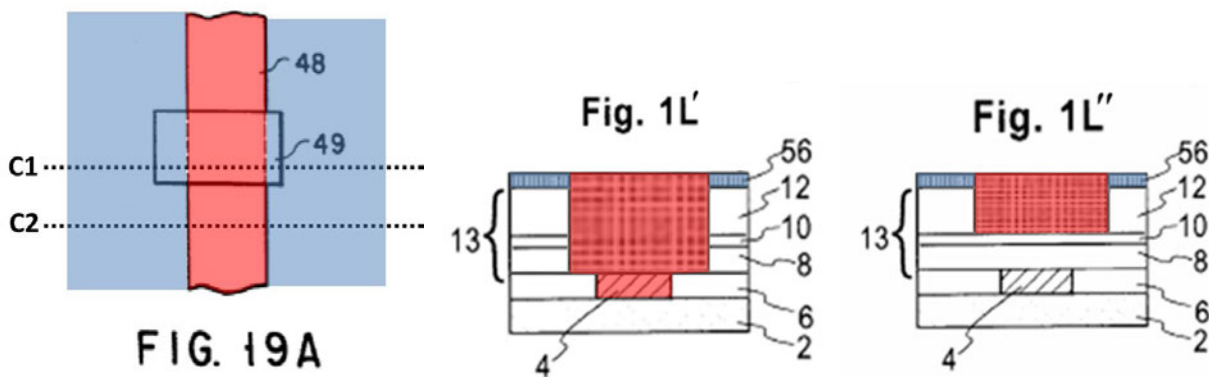
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<sup>11</sup> Figures 5H' and 5H'' are the Petitioner's depiction of the *Grill-Aoyama* combination using the *Grill* embodiment that omits optional layer 7. It shows what a POSITA would have understood regarding *Grill*'s alternative embodiment without optional layer 7, as combined with *Aoyama*. (Ex. 1002, ¶241 & n.8.)

<sup>12</sup> See also *supra* §V.B.1.1, at n.7.

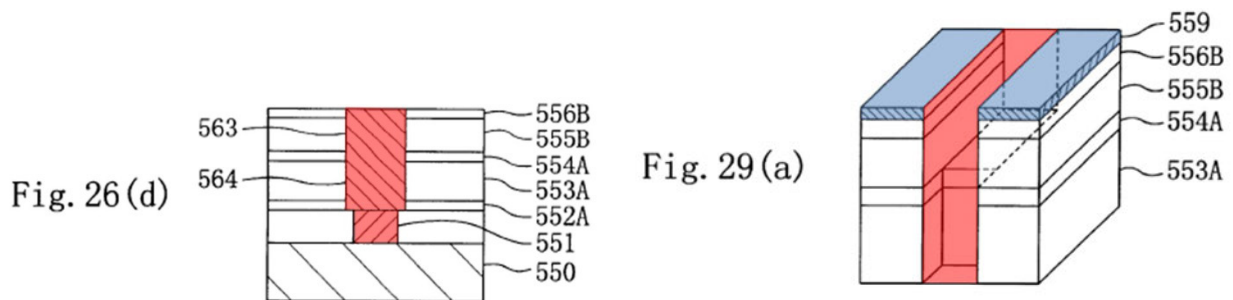
For the step of filling the wiring grooves, *Grill* states, “Cavity 20 is . . . overfilled with conductive wiring material 22, by a process such as physical vapor deposition, chemical vapor deposition, solution deposition, or plating.” (Ex. 1005, 4:64–5:2, Fig. 1K.) Then, the conductive wiring material [22] is planarized by CMP to be approximately even with the top surface of dielectric 12 or remaining hard mask. (*Id.*, 5:2–8, Fig. 1L; *see also* Ex. 1002, ¶243.)

Figure 19A below shows the top surface of *Aoyama*’s structure, as viewed from above. The red areas of Figure 19A indicate the metallized regions, and the blue areas indicate the lower hard mask [56]. Cross-section C1 of the *Grill-Aoyama* combination appears below in Figure 1L’. (Ex. 1002, ¶244.) Cross-section C2 of the *Grill-Aoyama* combination appears below in Figure 1L’’. (*Id.*)



As Figure 1L' shows, a POSITA would have understood that, if layer 7 were absent, metal would fill the contact holes in etch stop [10] and via level dielectric [8] and fill the wiring grooves in the lower hard mask [56] and the wiring level dielectric [12]. (Ex. 1002, ¶245; *see also supra* §§III.A.11, V.B.1.1.)

Figures 26(d) and 29(a) from the modified fifth embodiment of the '696 patent appear below for comparison. According to the '696 patent, “a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes 562 and the wiring grooves 561.” (Ex. 1001, 26:38–41.) “As a result, second metal interconnects 563 and contacts 564, connecting the first and second metal interconnects 551 and 563 together, are formed.” (Ex. 1001, 26:44–47.)

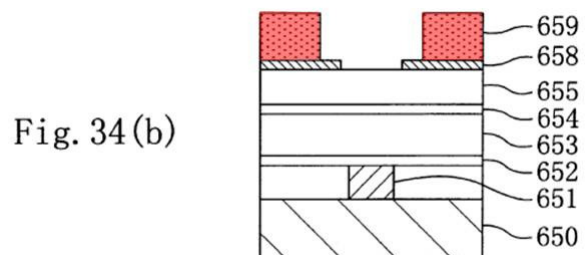
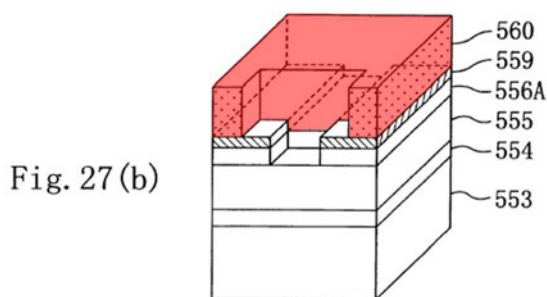
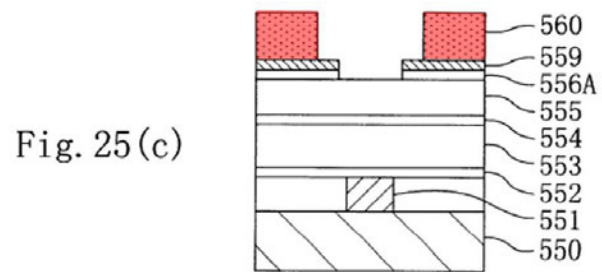
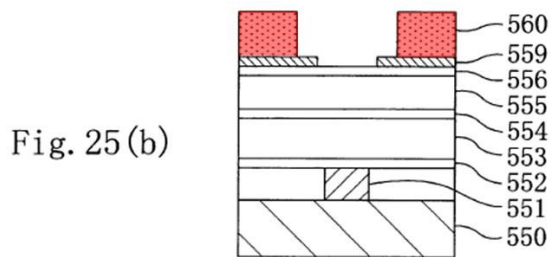


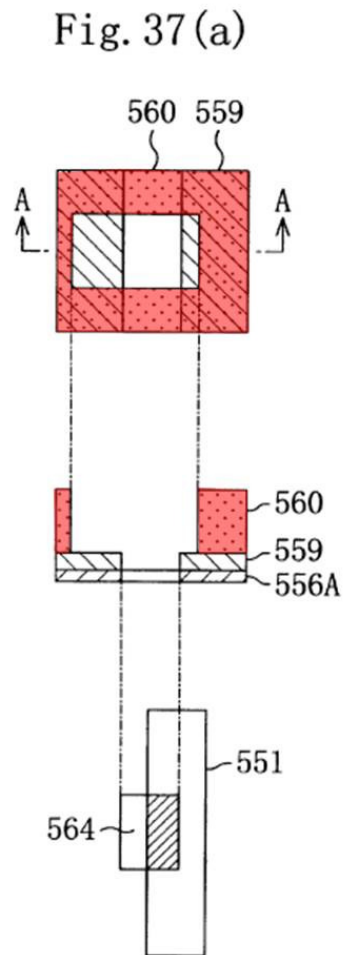
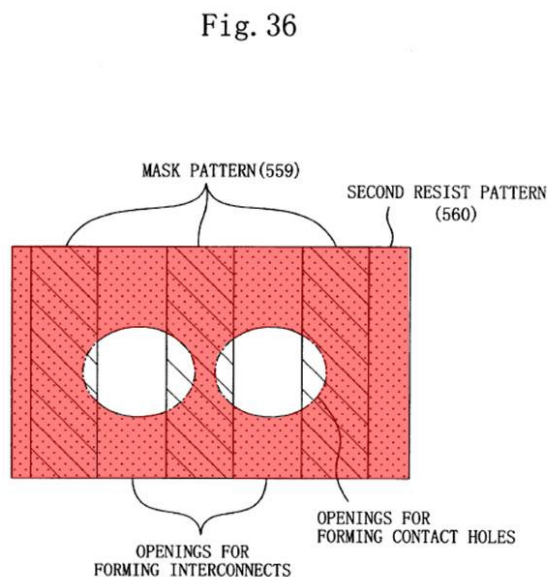
### 3. Claim 15 is obvious in view of the *Grill-Aoyama* combination

Claim 15 depends from claim 13 (*see* §V.C.2) and further recites that “a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.” As explained in section V.C.2, a POSITA would have understood that the *Grill-Aoyama* combination discloses each limitation of claim 13. (*See* Ex. 1002, ¶¶248–53.)

The '696 patent discusses this feature with reference to Figures 25(b), 25(c), 27(b), 34(b), 36, and 37(a), all shown below with highlights. (*See* Ex. 1001,

25:26–65, 30:49–57, 31:49–67.) The '696 patent explains that “even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves, the openings of the patterned second silicon dioxide film 556A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern 559 for forming wiring grooves.” (*Id.*, 25:46–52.) In addition, “the contacts 564 can connect the first and second metal interconnects 551 and 563 together with a lot more certainty.” (*Id.*, 25:63–65; *see also* 25:42–65, 27:12–60, 31:49–67, Fig. 37(b).)





*Aoyama* discloses the same solution to the same problem. *Aoyama* states that misalignment of the photomask during through-hole (via) formation can cause the through-hole to be smaller than desired and the wiring groove wider than desired at the location of the through-hole. (Ex. 1018, 3:18–21, 3:29–32.) This increases contact resistance, degrades reliability, and makes it difficult to achieve a higher integration density. (*Id.*, 3:33–38, 6:7–14.) The problem is illustrated below by Figures 5B and 5D of *Aoyama*. Figure 37(b) of the '696 patent is also shown below for comparison. (*See also* Ex. 1001, 27:31–51.)





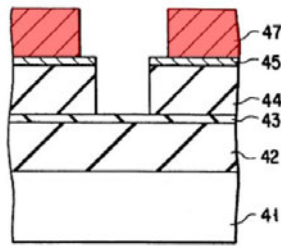


FIG. 18B

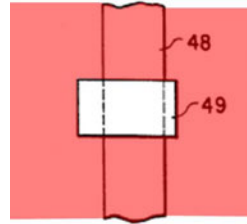
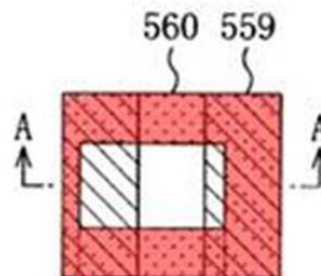
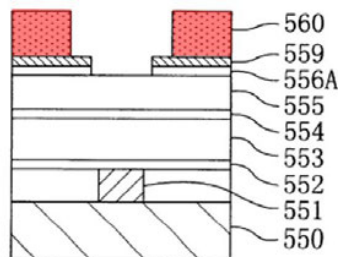


FIG. 19A

Fig. 37(a)

Fig. 25(c)



A POSITA would have understood that these disclosures would remain unaffected by the combining them with the relevant teachings of *Grill* and regardless of whether layer 7 of *Grill* is used. (Ex. 1002, ¶¶248–53; *see also supra* §V.C.1.)

## VI. Mandatory Notices Under 37 C.F.R. §42.8

### A. Real Parties-In-Interest

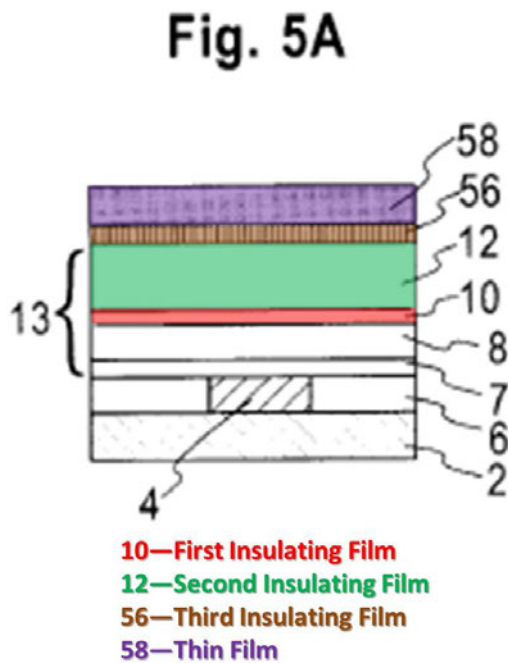
The real party in interest is Taiwan Semiconductor Manufacturing Company, Ltd. (“TSMC”).

### B. Related Matters

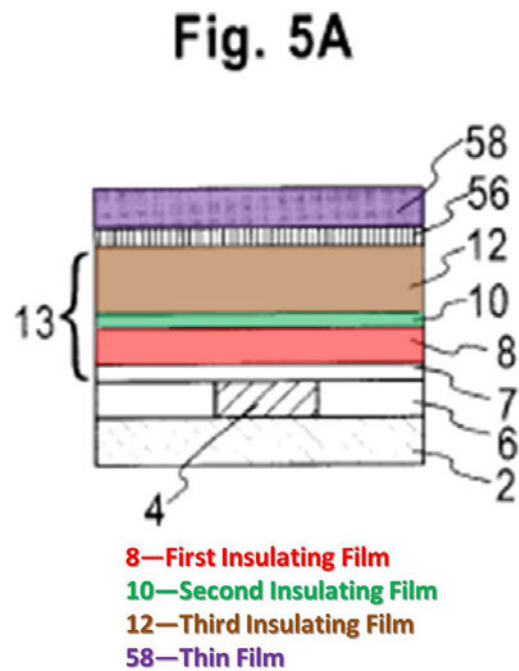
TSMC is concurrently filing related *inter partes* petitions IPR2016-01377, IPR2016-01378, and IPR2016-01379 challenging several claims of the ’696 patent.

None of the grounds proposed in these related petitions is redundant. Neither of IPR2016-01377 and IPR2016-01379 challenges claim 13 or claim 15. Like the present Petition, IPR2016-01378 challenges claim 13 based on the *Grill* and *Aoyama* references, but IPR2016-01378 does not challenge claim 15, and it also challenges claim 14. And in the present Petition *Grill* is submitted for single-reference obviousness under §103, whereas in IPR2016-01378 *Grill* is submitted for anticipation under §102.

Notably, the present Petition and IPR2016-01378 map the layers of the *Grill* reference to the challenged claims in a considerably different manner, such that the substantive basis and supporting arguments for the petitions materially differ. This appears in the Figures below.



***This Petition***



***IPR2016-01378***

Patent Owner Godo Kaisha IP Bridge 1 filed a recent lawsuit asserting infringement of the '696 patent. In Case No. 2:16-cv-00134-JRG-RSP (E.D. Tex. Feb. 14, 2016), Patent Owner has sued Avago Technologies Ltd., Avago Technologies US, Inc., Broadcom Corporation, Broadcom Limited, and LSI Corporation. TSMC is not aware of any other related matters involving the '696 patent.

**C. Lead and Back-Up Counsel**

**Lead Counsel:** Darren M. Jiron (Reg. No. 45,777; Tel. (571) 203-2729; darren.jiron@finnegan.com), attorney at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Two Freedom Square, 11955 Freedom Drive, Reston, VA 20190-5675.

**Back-Up Counsel:** E. Robert Yoches (Reg. No. 30,120; Tel. Tel. (202) 408-4039; bob.yoches@finnegan.com) J.P. Long (Reg. No. 65,125; Tel. (202) 408-4347; jp.long@finnegan.com), attorneys at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, 901 New York Avenue, NW, Washington, DC 20001-4413.

**D. Service Information**

TSMC consents to service by e-mail at the following addresses:  
darren.jiron@finnegan.com, jp.long@finnegan.com, bob.yoches@finnegan.com,  
and TSMC-IPB-PTAB@finnegan.com.

## **VII. Certification Under 37 C.F.R. §42.24(d)**

This Petition complies with 37 C.F.R. §42.24. As calculated by the “Word Count” feature of Microsoft Word 2010, it contains 12,339 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices Under 37 C.F.R. §42.8, Certification Under §42.24(d), and Certificate of Service.

## **VIII. Payment of Fees**

The required fees are submitted electronically in accordance with 37 C.F.R. §§42.103(a) and 42.15(a). If any additional fees are due during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 06-0916.

## **IX. Time for Filing Petition**

The ’696 patent issued on March 6, 2001, and this Petition is being filed more than nine months after the date the patent was granted (December 6, 2001). *See* 35 U.S.C. §311(c); 37 C.F.R. §42.102(a). Because TSMC has not been served with a complaint alleging infringement of the ’696 patent, the one-year bar date of 37 C.F.R. §42.101(b) does not apply.

## **X. Grounds for Standing**

Under 37 C.F.R. §42.104(a), TSMC certifies that the ’696 patent is available for *inter partes* review and that TSMC is not barred or estopped from requesting *inter partes* review of the ’696 patent to challenge the claims on the grounds identified in this Petition.

## **XI. Conclusion**

For the reasons set forth above, the challenged claims are unpatentable.

Trial should be instituted and the claims should be cancelled.

Respectfully submitted,

Dated: July 12, 2016

By: /Darren M. Jiron/  
Darren M. Jiron, Reg. No. 45,777

## **CERTIFICATE OF SERVICE**

The undersigned certifies that the foregoing Petition for Inter Partes Review, the associated Power of Attorney, and Exhibits 1001 through 1018 were served on July 12, 2016, by Federal Express at the following address of record for the '696 patent and an address known to the petitioner as likely to effect service:

### **Address of Record**

Attn: Gerald J. Ferguson, Jr.  
SIXBEY, FRIEDMAN, LEEDOM &  
FERGUSON, P.C.  
8180 Greensboro Drive, Suite 800  
McLean, VA 20001

### **Address Likely to Effect Service**

Attn: Melissa Richards Smith  
GILLAM & SMITH, LLP  
303 South Washington Avenue  
Marshall, TX 75670

/Sheila Y. West/  
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