UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case No. IPR2016-01376
Patent Number 6,197,696

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges.*

DECLARATION OF ALEXANDER GLEW, Ph.D.

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I, Dr. Alexander Glew, Ph.D., hereby declare under penalty of perjury under the laws of the United States of America:

I. Qualifications

1. I am currently President of Glew Engineering Consulting, Inc. ("Glew Engineering") of Mountain View, California. Glew Engineering provides consulting and engineering services relating to various technology or engineering areas, including CVD technology. My responsibilities at Glew Engineering include acting as a consultant and as a principal managing the company. [1]

2. I received a Bachelors of Science degree in Mechanical Engineering from University of California, Berkeley in 1985; a Master of Science degree in Mechanical Engineering from University of California, Berkeley in 1987; a Master of Science in Materials Science and Engineering from Stanford University in 1995. I later also obtained a Doctor of Philosophy degree in Materials Science and Engineering from Stanford University in 2003. A copy of my Curriculum Vitae is attached to this report as **Attachment A**.

[1] All emphasis and annotations added unless otherwise noted. A list of exhibits considered is attached to this Declaration as **Attachment B**. Citations to the exhibits in this declaration are exemplary and are not meant to be limiting.

3. The subject matter of my doctoral dissertation at Stanford University related to chemical vapor deposition ("CVD") of dielectric films. CVD generally consists of mixing two or more gases in a process reactor or chamber, and having the gases meet on the surface of a substrate to deposit a thin film. Many of the CVD films that I worked on were deposited on undoped silicon glass (SiO2), and boron and phosphorous doped glass. The CVD equipment to be manufactured in this case was to mix various gaseous chemicals and to deposit the chemicals onto glass to produce certain types of specialty glasses. For my doctoral dissertation, I constructed a CVD reactor. Then, I developed CVD processes for certain low k dielectric films such as diamond-like carbon and fluorinated amorphous carbon. Further, I characterized those thin films for their engineering properties, including optical, electrical, and mechanical. Also, I analyzed the chemical composition of the thin films.

4. From 1987-1997, I was employed by Applied Materials, Inc. ("Applied Materials"), one of the world's largest and most advanced manufacturers of, among other things, CVD-related equipment. I was hired by the CVD division. The first process tool that I worked on was the Precision 5000 CVD tool. It was the first cluster tool, a tool with multiple CVD processing chambers. Because this tool represented the major advance in tool architecture, multiple chambers attached to a central vacuum load lock chamber, resulting in the ability to process one

workpiece at a time instead of in batch, it was eventually placed in the Smithsonian Institute, Natural History Museum.

5. From approximately 1987-1989, I was a Systems Engineer for Applied Materials. In this position, I designed semiconductor processing equipment, and worked with all aspects of the process tool. After a period of time, along with the product marketing manager, I signed off on every tool or machine that we shipped. My signature was required to ensure that the manufactured process tool and the chemical processes it produced matched what was required by the purchase order, and that it was built accordingly and safely.

6. Subsequent to being a Systems Engineer, from approximately 1989-1991, I was an Engineering Manager at Applied Materials responsible for customer engineering specials ("CES"). This included customization of equipment to meet customer requests and specifications. The CES requests were diverse and covered nearly all aspects of the equipment, including modifying process chambers, gas panels, wafer handlers/robotics, wafer storage elevators, sensors, vacuum systems, framing, and other components. We worked on very tight schedules, and exercised disciplined project management. If our engineering work was not completed on time, and the materials not procured, then this would hold up the shipment of a multimillion dollar CVD process tool. Because we exercised disciplined project management, such delays rarely happened. We also had to accurately estimate the

cost of our work, materials and labor, because the CES projects were billed to the customer.

7. Next, I was the manager of the engineering design and support group for the CVD division of Applied Materials. In this capacity, I was in charge of all of the designers and drafters, generating all of the engineering drawings, and reviewing all of the engineering design work. I am intimately familiar with computer aided design ("CAD") and engineering documentation.

8. In the early 1990s, I was awarded the position of Core Technologist (one of only 15 at Applied Materials). My area of expertise was gas and chemical systems and components. The gas and chemical systems largely delivered ultra-high purity fluids to the process chambers and reactors. Components used in the systems included the following: valves, flow controllers, pressure regulators, filters, purifiers, pressure transducers and related devices, and systems as a whole. As a core technologist, I was responsible for consulting with different divisions during the design of new products, testing fluid delivery components, reviewing invention disclosures, and reviewing papers written by Applied Materials personnel, holding meetings across the divisions for workers in the field, setting technology trends with suppliers, and reviewing technology trends with customers. Our different divisions included product lines such as CVD, ETCH, CMP, implant, TFT, and others. I also represented the company at industry consortium meetings. The core

technology group met monthly with the president or other senior executives of the company.

9. From 1994-1996, I managed a project funded by SEMATECH (Semiconductor Manufacturing Technology—a non-profit R&D consortium to advance chip manufacturing) that I proposed to its factory working group. These efforts resulted in the publication of two SEMATECH technology transfer standards. The goal of this project was to develop industry standard methods to determine the effects of trace chemicals and contamination on semiconductor processing and on semiconductor equipment reliability. As part of this project, I designed, built, and tested gas delivery systems, including the components contained therein, such as filter cartridges or assemblies, flow controllers, valves, and pressure regulators, and tested them to failure. Approximately 90% of wafer yield loss is from particles, so the industry was very interested in the particle effects of the chemical delivery system. I also tested the effects of micro-contamination in the process gas stream on tungsten CVD deposition and on metal etching. In some of the tests, we introduced controlled amounts of fluid into corrosive gas streams, and then measured the effect on system reliability, including particle generation.

10. As part of the SEMATCH project, we studied the effects of trace chemical contamination on tungsten CVD processing and on metal etching. We

introduced trace chemicals into a standard process, measured the amounts of chemical in the process chamber by residual gas analyzer (RGA), and then measured the resulting film quality and properties by multiple techniques, and measured incorporation of the trace chemicals into the deposited layers.

11. From 1994-1997, I was a CVD Supplier Quality Engineering Manager at Applied Materials. During this time, I was the engineering manager responsible for the suppliers of the components of the fluid delivery systems, such as valves, flow controllers, pressure regulators, filters, purifiers, pressure transducers and related devices, and systems as a whole. I tested and evaluated fluid delivery components. I both supervised and personally conducted this testing.

12. Since leaving Applied Materials in 1997 and until the present, I have served as president of Glew Engineering. At Glew Engineering, I have worked on projects that include for example: project turnaround for failed projects, testing / metrology, gas panel design, integrated circuits failures, semiconductor equipment failures, Excimer laser sources for photolithography, KrF and ArF. I have assisted component suppliers, and equipment suppliers, and, to a lesser extent, investors.

13. My practice at Glew Engineering also includes multi-physics finite element analysis and CAD modeling, which includes three dimensional modeling of machinery, and analysis of the heat transfer, radiation, fluid flow, resultant stresses and strains from running such machinery.

14. I am or have been a member of a number of professional organizations including: American Society of Mechanical Engineers, Materials Research Society, and IEEE (Institute of Electrical and Electronics Engineers). Glew Engineering is an Affiliate Member of the Semiconductor Equipment and Materials Institute (SEMI). In addition to being a member of these professional organizations, I have served on committees at SEMATECH.

15. I have authored or co-authored dozens of papers, reports, and presentations relating to semiconductor processing, and semiconductor equipment, fluid delivery components in semiconductor processing, and equipment reliability.

16. I am an inventor of three issued U.S. Patents, Nos. 6,679,476, related to a high-purity control valve; 6,204,174, related to semiconductor processing; and 7,118,090, related to a high-purity fluid control valve. I have another patent application pending relating to design of CVD equipment components.

17. For more aspects of my qualifications and publications, see my curriculum vitae ("CV"), attached hereto as **Attachment A**.

18. I have been retained on behalf of Patent Owner Godo Kaisha IP Bridge 1 ("IP Bridge" or "Patent Owner") to offer opinions regarding certain issues relating to U.S. Patent No. 6,197,696 ("the '696 patent") assigned to Patent Owner, as well as other references presented to me by counsel for Patent Owner. I

have also been retained by Patent Owner to offer certain opinions relating to the ’696 patent in a co-pending litigation in the Eastern District of Texas.

19. Glew Engineering charges an hourly rate of $665 per hour plus expenses for my work performed in connection with this *Inter Partes* Review. I have received no additional compensation for my work in this *Inter Partes* Review, and my compensation does not depend on the contents of this report, any testimony I provide, or the ultimate outcome of this or any other *Inter Partes* Review.

II. Materials Considered

20. In developing my opinions below relating to the ’696 Patent, I have considered the following materials:

- U.S. Patent No. 6,197,696 (Exhibit EX1001);
- U.S. Patent No. 6,197,696 Patent File History (Exhibit EX1012);
- Petition for *Inter Partes* Review of U.S. Patent No. 6,197,696 (IPR2016-01376) (“Petition” or “Pet.”) (Paper No. 1);
- Patent Owner’s Preliminary Response (IPR2016-01376) (Paper No.6;
- Decision – Institution of *Inter Partes* Review (IPR2016-01376) (Paper No. 11) (“ID”);
- Declaration of Bruce W. Smith (IPR2016-01376) (Exhibit EX1002);
- Japanese Patent Application No. 10-079371 to Aoi (Exhibit EX1013)
- Certified Translation of Japanese Patent Application No. 10-079371 to Aoi (Exhibit EX1014)

- Japanese Patent Application No. 11-075519 to Aoi (Exhibit EX1015)
- Certified Translation of Japanese Patent Application No. 11-075519 to Aoi (Exhibit EX1016)
- U.S. Patent No. 6,140,226 to Grill et al ("Grill") (Exhibit EX1005)
- U.S. Provisional Patent Application No. 60-071,628 ("'628" or "Grill Provisional") (Exhibit EX1017)
- U.S. Patent No. 5,592,024 to Aoyama et al ("Aoyama") (Exhibit EX1018)
- U.S. Patent No. 3,617,824 to Shinoda et al ("Shinoda") (Exhibit EX1003)
- U.S. Patent No. 3,838,442 to Humphreys ("Humphreys") (Exhibit EX1004)
- U.S. Patent No. 5,635,423 to Huang et al ("Huang") (Exhibit EX1006)
- U.S. Patent No. 5,741,626 to Jain et al ("Jain") (Exhibit EX1007)
- C. Akrout et al., "A 480-MHz Microprocessor in a 0.12μm Leff CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998) ("Akrout") (Exhibit EX1008)
- J.N. Burghartz et al.,"Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Tech. & Low-Loss Substrates," Int'l Electron Devices Mtg (Dec. 1996) ("Burghartz") (Exhibit EX1009)
- U.S. Patent No. 6,100,184 to Zhao et al (Exhibit EX1010)
- U.S. Patent No. 6,103,616 to Yu et al (Exhibit EX1011)
- Transcript of the Deposition of Bruce W. Smith, Ph.D. (March 23, 2017) ("Smith Dep.") (Exhibit EX2010);
- Redline Comparing Grill (EX1005) with Grill's Provisional (EX1017) Application (Exhibit EX2011)
- Translation of Japanese Application 10-079371 to Aoi as Submitted in European Patent Application No. 99 105 946.0 (Exhibit EX2012)

- Declaration of Takeo Ohashi, Ph.D. (Exhibit EX2013)
- Influence of reactor wall conditions on etch processes in inductively coupled fluorocarbon plasmas by M. Schaepkens, et al. (Exhibit EX2014)
- Handbook of VLSI Microlithography, Second Edition, Principles, Technology, and Applications by John N. Helbert (excerpted) (Exhibit EX2015)
- Silicon VLSI Technology Fundamentals, Practice and Modeling by James D. Plummer, et al. (excerpted) (Exhibit EX2016)
- Microlithography: Science and Technology by James R. Sheats and Bruce W. Smith (excerpted) [First Edition] (Exhibit EX2017)
- Microlithography: Science and Technology by Kazuaki Suzuki and Bruce W. Smith (excerpted) [Second Edition] [Ch 12] (Smith Dep. Exhibit 3) (Exhibit EX2018)
- Microlithography: Science and Technology by Kazuaki Suzuki and Bruce W. Smith (excerpted) [Second Edition] [Ch 11] (Smith Dep. Exhibit 9) (Exhibit EX2019)
- Silicon Processing for the VLSI Era Vol. 1 by S. Wolf and R.N. Tauber (excerpted) [Ch 16] (Exhibit EX2020)
- Mask Definition, Merriam-Webster.com (last accessed Dec. 17,2016) (https://www.merriam-webster.com/dictionary/mask) (Exhibit EX3001)
- District Court Claim Construction, 2:16-CV-134-JRG-RSP (E.D. Tex.) (Exhibit EX3002)
- All other materials referenced herein, including those referenced in Attachment B.

III. Level of Ordinary Skill for the ’696 Patent

21. I understand that the factors that may be considered in determining the ordinary level of skill in the art include: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology. I understand that a person of ordinary

skill in the art (also referred to as a "skilled person") is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above.

22. At least as of March 26, 1998, the foreign priority date of the '696 patent, a person of ordinary skill in the art would have had a Bachelor's of Science degree in materials science engineering, electrical engineering, mechanical engineering, chemical engineering, or an equivalent degree, and at least two years of experience in semiconductor processing or equipment.

23. I met and surpassed these criteria as of at least March 26, 1998 (and thereafter), and consider myself to be a person with at least ordinary skill in the art of the '696 patent. My analyses set forth herein are from the perspective of a person of ordinary skill in March 26, 1998, as set forth above. My opinions would not change even if the '696 patent is only entitled to the later priority date of March 23, 1999 (*see* §VII).

24. I note that Dr. Smith has opined that a person of ordinary skill in the relevant art for the '696 patent would have at least a Master of Science degree in Electrical Engineering, Materials Science, Physics, or the equivalent, a working knowledge of semiconductor processing technologies for integrated circuits, and at least two years of experience in related semiconductor processing analysis, design and development. EX1002 at ¶141. Dr. Smith has further opined that "[a]dditional

graduate education could substitute for professional experience, and significant work experience could substitute for formal education." EX1002 at ¶141. I disagree with Dr. Smith that this is the appropriate level of skill in the art, but even applying Dr. Smith's standard, my opinions herein would not change.

25. Unless otherwise stated, when I state that something would have been known or understood by a person of ordinary skill in the art, I am referring to a person with the level of education and experience expressed in ¶¶21-24 above, as of March 26, 1998. As described above and in my CV (Attachment A), I have decades of experience with semiconductor devices, including the design and fabrication of memory devices. As of March 28, 1998, I had a Master degree of Science in Materials Science and Engineering, and in Mechanical Engineering, and over 10 years of industry as well as academic experience in semiconductor processing or equipment. I would have qualified as one of ordinary skill in the art according to any of the above definitions. Therefore, I am qualified to testify about what a person of ordinary skill in the art would have known and understood at that time.

IV. Relevant Legal Standards

26. I have been informed that if an independent claim is found to be novel and non-obvious, every claim that depends from it is also novel and non-obvious. I have also been informed that if an independent claim is not found to be novel and

non-obvious, the claims which depend from it may still be found to be novel and non-obvious. I understand that to be valid, a patent claim must be novel and non-obvious.

27. I understand that a party challenging validity carries the burden of proving invalidity by a preponderance of the evidence on a claim-by-claim basis. Each claim is analyzed independently. It is my understanding that when a party has the burden of proving a claim or defense by a preponderance of the evidence, that party must show that it is more likely than not.

A. Anticipation

28. I also understand that a patent claim is not novel if is anticipated by a single prior art reference – that is, a single prior art reference discloses each and every element of the claim either expressly or inherently. I also understand that a single reference cannot merely disclose each element. Rather, it must disclose all of the elements as arranged in the claim. I further understand that for a reference to "inherently" disclose something, the missing descriptive matter must necessarily be present in the reference, not merely probably or possibly present, and that it would be so recognized by a person of ordinary skill. I understand that if an element of the claim is not disclosed by one prior art reference, then the claim is not anticipated.

29. I understand that a limitation is found inherently within a reference only if that limitation is necessarily disclosed by the reference (*e.g.*, "necessarily present" in the reference). The mere fact that something may result from a given set of circumstances is not sufficient to show inherency, as inherency cannot be established by probabilities or possibilities. Instead, there must be no other possible alternative to the implementation of the feature, in view of the prior art reference's disclosure.

B. Obviousness

30. I understand that under §103 of the patent statutes, a patent claim is deemed obvious if the differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art. That is, a person of ordinary skill must have had a reasonable expectation of success in making or practicing the claimed invention, based on the prior art. I also understand that the obviousness analysis does not permit the use of hindsight. One way of avoiding a hindsight analysis is to point to a suggestion or a motivation in the prior art to make or practice the claimed invention.

31. I have been informed that to render a claim obvious, a combination of prior art references must disclose each and every claim element of that claim, and that obviousness is a question of law (*i.e.*, for the Board to determine) based on the

underlying facts. I understand that the underlying factual inquiries are: (1) the scope and content of the prior art, (2) the differences between the prior art and the claims at issue, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations of nonobviousness. I also understand that a patent composed of several elements is not proven to be obvious by simply demonstrating that each of its elements was, independently, known in the prior art. Instead, I understand that there must be some rationale given to support the conclusion.

32. I have also been advised that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a person having ordinary skill in the art. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in

the same field or in a different one, so that if a person of ordinary skill can implement a predictable variation, the variation is likely obvious;

- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was "obvious to try," particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

33. I understand that an invention might not be obvious if (1) the combination requires an expert to rely on the patent itself as a roadmap, (2) the prior art teaches away from the invention or the combination because a person of

ordinary skill in the art would be discouraged from following the path set out in the reference or would be led in a direction divergent from the path that was taken by the inventor, (3) the combination would change the basic principles under which the prior art was designed to operate, or (4) the combination would render the prior art inoperable for its intended purpose.

C. Priority Date of a Patent

34. I understand that a patent reference may claim the benefit of a filing date of a provisional application that may predate the filing date of the patent reference in the United States Patent & Trademark Office ("USPTO"). In order to claim the benefit of the filing date of the provisional application, the patent reference must expressly claim the benefit of the earlier filing date and the disclosure of the provisional application must provide support for the claims of the patent reference. I understand that in order to provide support for the claims of the patent reference, the provisional application must enable and provide written description support for the claims. I understand that the written description requirement is met if the claimed subject matter is described by the provisional application, or if the invention is disclosed such that a person or ordinary skill in the art can reasonably understand that the inventor was in possession of the claimed subject matter. I also understand that the enablement requirement is

satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.

35. My understanding is that, similarly, a claim of a patent can claim priority to an earlier filing date of a foreign patent application in the same manner that a claim of a patent can claim priority to an earlier filing date of a provisional application.

D. Standard for Claim Construction in *Inter Partes Review*

36. I have also been informed that for purposes of *inter partes* review a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. While claim terms are generally given their ordinary and customary meaning, which is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, the construction must also be consistent with the specification, and the claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.

37. I understand that the Board has instituted an *inter partes* review of claims 13 and 15 of the ’696 patent. I understand that trial is limited to the following ground: whether claims 13 and 15 are rendered obvious by Grill and Aoyama. ID at 43. I further understand that the Petition was denied as to all other grounds and trial is accordingly limited to this ground. I understand that the Board

"has not made a final determination with respect to the patentability of any claim term." *Id*.

V. Background of the '696 Patent

38. The '696 patent, entitled "Method for Forming Interconnection Structure," was filed on March 23, 1999, and issued on March 6, 2001, and claims priority to Japanese Provisional Patent Application No. 10-079371 ("the '371 application) filed March 26, 1998. The patent names inventor Nobuo Aoi.

39. The '696 patent has 4 independent claims and 11 dependent claims. The '696 patent relates to a complex process for multiple masking to form interconnect structures using low-k dielectric constant ("low-k") materials. Interconnect structures connect the millions of semiconductor circuits, devices and elements formed within a physical semiconductor device (*e.g.*, a "die") and are thus essential to the operation of any semiconductor product. Interconnect structures formed with low-k materials can be scaled to smaller dimensions than interconnect structures formed without low-k materials. The inventor of the '696 patent succeeded in developing a method to use standard lithography techniques to form dense interconnect structures using low-k materials.

40. An interconnect structure includes at least two groups of materials—conductors (metals) and insulators. The shapes, arrangements, and compositions of these materials within the interconnect structure affect electrical performance

(described by, *e.g.*, resistivity and capacitance) of the interconnect structure. The electrical performance of the interconnect structure in turn affects the speed, electrical-signal integrity, heat dissipation, and power consumption of an overall semiconductor product, which is filled with such interconnect structures. For example, the dielectric constant—referred to as "k"—of the low-k insulating materials used in the interconnect structure reduces capacitance among interconnect structures. This reduced capacitance improves electrical performance and permits denser packing of interconnect structures. The improved electrical performance reduces the need for additional circuitry and/or metal wiring which may otherwise be needed to improve the integrity of electric signals that are routed around a semiconductor product. Thus, the denser packing of interconnect structures and reduction in additional circuitry and wiring facilitated by using low-k insulators also leads to reduction in area of the chip, and thus a smaller die size.

41. Low-k dielectric films can be particularly difficult to pattern by semiconductor photolithographic methods. The claimed invention of the '696 patent allows for the use of standard lithography techniques to form interconnect structures having low-k dielectric materials. *See, e.g.*, EX1001 3:2-4:67.

42. In prior processing methods, a low-k dielectric would be damaged in the ashing process used to remove polymer based photoresist layers. *See, e.g.*, EX1001 2:41-52, 3:47-62. Ashing is a process of exposing a polymer-based

photoresist to an oxygen plasma and burning it off the wafer, thereby turning the photoresist into "ash." Many low-k materials are carbon compounds, and cannot withstand exposure to oxygen based plasma used in an ashing process.

43. The '696 patent avoids damaging low-k materials by practicing certain patterning, lithography and etching, methods. An intermediary material is patterned with a photolithography resist, and the resist is removed by ashing without damaging an underlying delicate low-k material. *See, e.g.*, EX1001 3:2-4:67. This process may also be part of a photo-resist strip ("PRS"). The '696 discloses, for example, that the interconnection structure of the modified third embodiment can be formed by a method illustrated in Figures 15(a)-17(c). EX1001 18:59-20:49. For example, as illustrated in Figures 16(c)-16(d), annotated below, the patterned organic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A as a mask (*e.g.,* using, as a mask, two layers having flush edges).[2] EX1001 19:50-54.

[2] As illustrated herein layers being used as a mask for a certain step are indicated in green, layers to be or having been etched for a certain step are indicated in yellow, and other layers are sometimes indicated in blue.

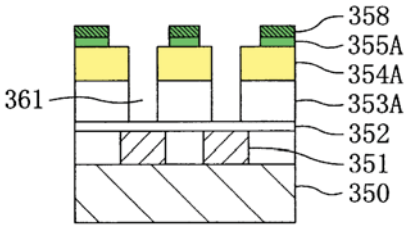


Fig. 16(c)

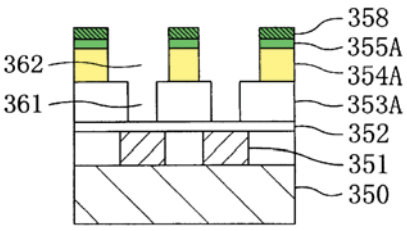


Fig. 16(d)

As illustrated in Figures 16(d)-17(a), annotated below, the silicon nitride film 352 is dry-etched using the patterned first silicon dioxide film 353A as a mask. EX1001 20:9-13.

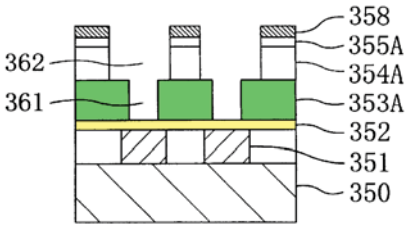


Fig. 16(d)

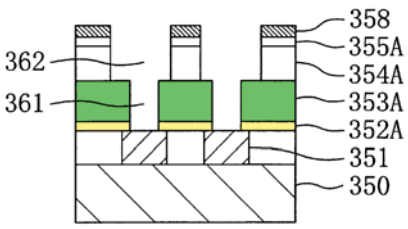


Fig. 17(a)

VI. Claim Construction

A. Proper construction of "using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] as a mask" (Claim 13)

44. Claim 13 requires etching "using" various layers "as a mask." I understand that this term has already been preliminarily construed by the Board at Institution. ID at 15. Per the Board's construction, "using" one or more layers "as a mask" during etching means using the one or more layers to define areas for etching. *Id.* (defining the term "using the [designated layer] for etching" as "using

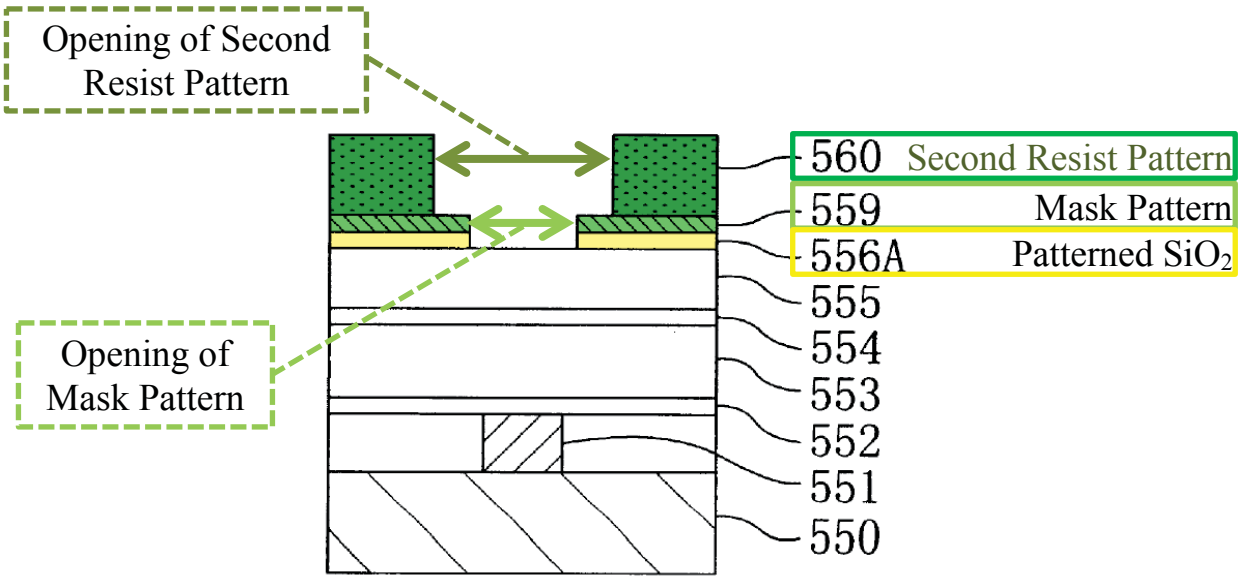
the [designated layer] to define areas for etching").[3] I agree with this construction. I also agree with the Board that a layer positioned between an overlying layer and an underlying layer being etched also acts as a mask, within the meaning of claim 13, in an instance where the overlying layer also is removed during etching, and thus, the intermediate layer acts to shield the layer being etched. *See* ID 18, fn.7.

45. This construction of the term is consistent with the use of the term throughout the '696 patent specification, which discloses numerous examples of structures being used as masks during etching; in each case, the structures are defining areas for etching. *See, e.g.*, EX1001 22:47-24:19, 24:54-26:34, 26:52-27:60, 27:62-29:20, 29:62-31:26, 31:49-32:9; Figs. 21-37. For example, for the limitation "using the second resist pattern and the mask pattern as a mask" in step 13(h), both the second resist pattern and the mask pattern must actually be *used* to *define areas for etching*—it would not satisfy this limitation to have either a second resist pattern or a mask pattern that does not define such an area.

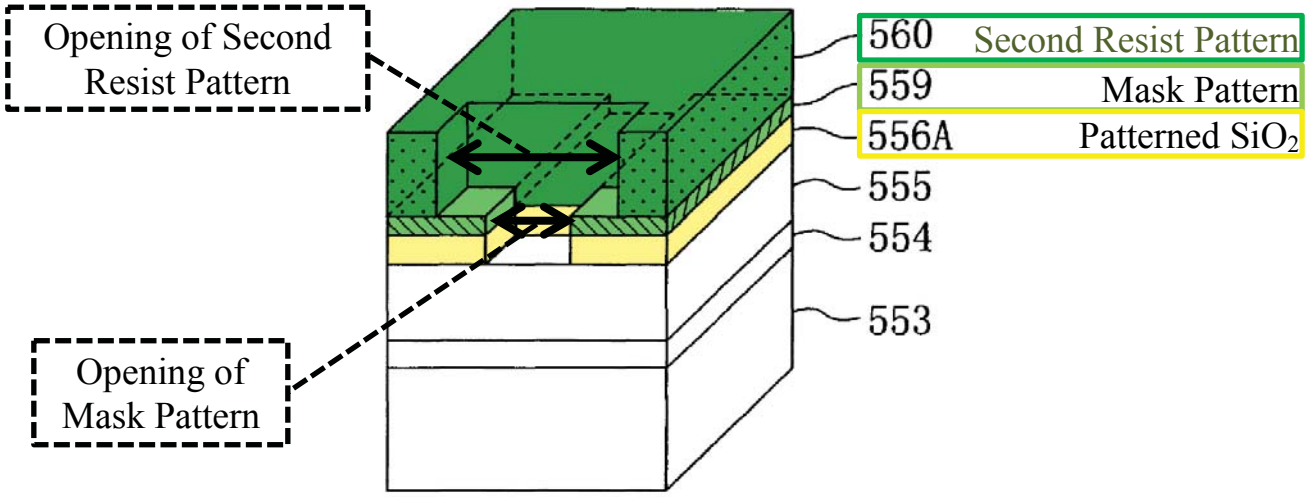
46. By way of further example, the '696 patent teaches how both the second resist pattern and the mask pattern are used to define areas for etching: the underlying layer is patterned (etched) where the openings of the resist pattern and

[3] The Board has replaced the terms "[first resist pattern/second resist pattern and the mask pattern/patterned third insulating film]" with "[designated layer]." ID 15.

the openings of the mask pattern overlap. *See, e.g.*, EX1001 8:1-6 ("[T]he openings of the patterned third insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves."), 7:62-8:7, 25:52-57, 26:63-27:3, 27:19-60, 31:60-67, Figs. 25(c), 27(b), 34(b), 37(a)-(b). Figures 25(c) and 27(b), for example, together illustrate using both the second resist pattern and the mask pattern as a mask, showing that the underlying insulating film (556A) is etched only where the openings of the second resist pattern (560) and the mask pattern (559) overlap, and that both the second resist pattern (560) and the mask pattern (559) define the area to be etched:



EX1001, FIG. 25(c).



EX1001, FIG. 27(b).

47. Contemporaneous dictionary definitions further support the above construction of "using the [designated layer] as a mask." *See*, *e.g.*, EX2001, 3 (defining masking as "[a]pplying a covering or coating on a semiconductor surface to provide a masked area for selective deposition or etching"); EX2002, 3 (defining a mask as "[a] device ... used to shield selected portions of a base during a deposition process," and a "template used to etch circuit patterns on semiconductor wafers"); EX2003, 4; EX2004, 3 (defining a mask as "[a]n object, stencil, or other device which is applied or placed upon a surface, so as to permit the selective passing of particles, beams, rays, substances, and so on, to form any desired patterns," and the use of said object "to selectively shield portions of semiconductor wafers, or other materials, during manufacturing").

48. I understand that the Board, based on the record then before it and without the benefit of my testimony about how this term would be understood by a person of ordinary skill in the art, has imposed an additional negative limitation upon the construction of "using the [designated layer] as a mask." Although the Board construed "***using the*** [designated layer] ***as a mask***" as "***using the*** [designated layer] ***to define areas for etching,***" the Board has also imposed an additional negative limitation to exclude "a layer, positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer" from being "used as a mask" within the context of claim 13. ID 18. I disagree with this additional negative limitation.

49. This exclusion of using two layers having flush edges as a mask is not supported by the claim language and is: (1) inconsistent with the disclosure the '696 patent and the priority document of the '696 patent (the '371 application) as understood by a person of ordinary skill in the art, and (2) inconsistent with the plain and ordinary meaning and understanding of a person of ordinary skill in the art as further demonstrated by a publication by Petitioner's expert.

1. The exclusion of using two layers having flush edges as a mask is inconsistent with the understanding of a skilled person in view of the disclosure of the '696 patent and the '371 application

50. I understand that claim constructions that exclude a preferred embodiment are rarely, if ever, correct.

51. The ’696 patent discloses three preferred embodiments that use two layers having flush edges as a mask (the modified third embodiment (also referred to as the “third embodiment variant” or “variant of third embodiment”), third embodiment, and modified fifth embodiment).

52. In the modified third embodiment, the ’696 patent discloses dry-etching the patterned organic film 354A “using the mask pattern 358 and the patterned second silicon dioxide film 355A … as a mask.” EX1001 19:50-53. This process of using two flush layers (358 and 355A) as a mask to etch layer 354A is illustrated in annotated Figures 16(c) and 16(d), provided below. Layer 358 (green) and layer 355A (light green) have edges that are flush, and are used as a mask to etch underlying layer 354A (yellow) in Fig. 16(c) to form the structure of Fig. 16(d).[4]

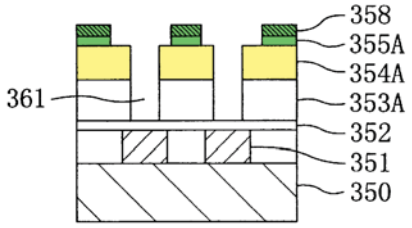


Fig. 16(c)

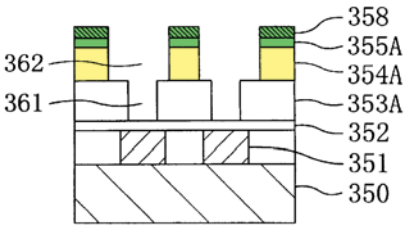


Fig. 16(d)

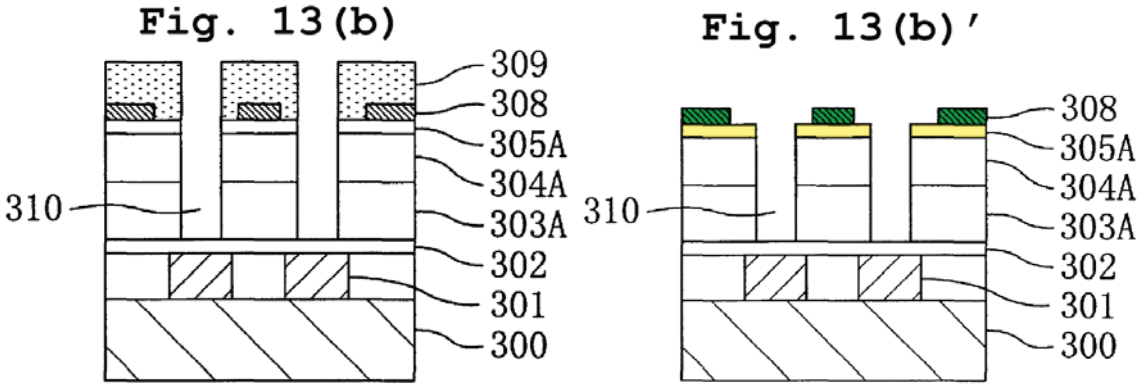
[4] As illustrated herein layers being used as a mask for a certain step are indicated in green, layers to be or having been etched for a certain step are indicated in yellow, and other layers are sometimes indicated in blue.

53. This modified third embodiment of the ’696 patent is fully supported by the ’371 application. Figures 16(c) and 16(d) of the ’696 patent correspond to Figures 16(c) and 16(d) of the ’371 application. *Cf.* EX1001 Figs.16(c)-(d) with EX1014 Figs.16(c)-(d). The passages of the ’696 patent that describe “using the mask pattern 358 and the patterned second silicon dioxide film 355A … as a mask” are present in the ’371 application. *cf.* EX1001 19:50-53 with EX1014 ¶[0095].

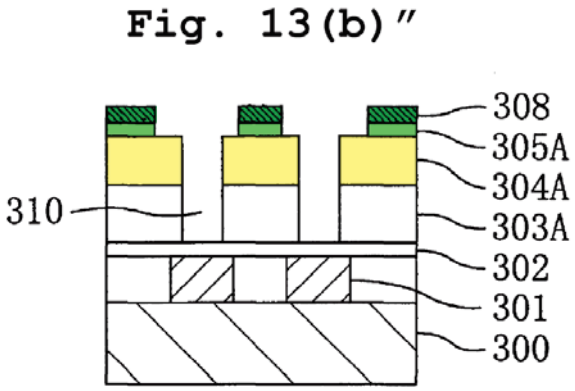
54. In the third embodiment, the ’696 patent discloses dry-etching a patterned low-dielectric-constant SOG film 304A “**using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A … as a mask**.” EX1001 17:34-40. This process of using two flush layers (308 and 305A) as a mask to etch layer 304A is illustrated in the sequence of annotated figures based on Figures 13(b) and 13(c), provided below, forming wiring grooves 311 in the example.

55. Starting from Fig. 13(b), resist layer 309 is removed, resulting in the structure of Fig. 13(b)’.[5] EX1001 Fig. 13(b), 17:30-31.

[5] Figures indicated with a ’, ’’, or ’’’ or –[ ] herein have been modified from their original appearance to reflect other disclosures as discussed herein.

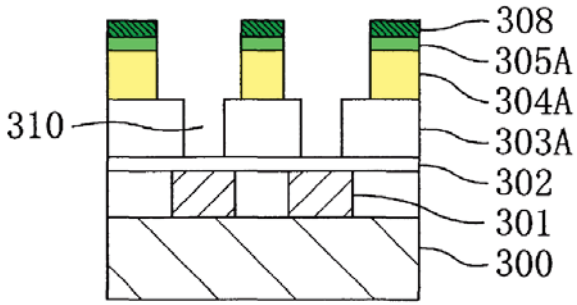


56. Next, from Fig. 13(b)', layer 305A is dry-etched using layer 308 as a mask, resulting in the structure of Fig. 13(b)'', where underlying layer 305A has an edge that is in line and flush with overlying layer 308. EX1001 17:31-35.



57. Next, from Fig. 13(b)'', layer 304A is dry-etched "using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A" (which have flush edges) "as a mask," resulting in the structure of Fig. 13(c). EX1001 17:35-40, Fig. 13(c).

Fig. 13(c)



58. This third embodiment of the ’696 patent is fully supported by the ’371 application. Figures 13(b) and 13(c) of the ’696 patent correspond to Figures 13(b) and 13(c) of the ‘371 application. *Cf.* EX1001 Figs.13(b)-(c) with EX1014 Figs.13(b)-(c). The passages of the ’696 patent that describe the sequence of operations that includes “using the mask pattern 308 and the patterned second organic containing-silicon dioxide film 305A … as a mask” are present in the ’371 application. *cf.* EX1001 17:30-40 with EX1014 ¶[0080].

59. In a certified translation of the ’371 application to which the ’696 patent claims priority provided by Petitioner, paragraph [0094] (describing the modified third embodiment) has been translated to recite using layers 355A and 354A “as masks” to etch layer 353, and paragraph [0095] (also describing the modified third embodiment) has been translated to recite using layers 358 and 355A “as masks” to etch layer 354A. However, I understand these translated paragraphs to be inconsistencies and errors in the translation, and that the correct translations for paragraph [0094] should recite using layers 355A and 354A “as a

mask" to etch layer 353 and should recite using layers 358 and 355A "as a mask" to etch layer 354A. EX2013 ¶¶8-17. Even if the word could be translated to mean "a mask" or "masks," a person having ordinary skill in the art would have understood the word to refer to "a mask" in the context of these paragraphs.

60. For example, within the same certified translation provided by Petitioner, a similar passage at paragraph [0080] has been translated to describe using two layers 308 and 305A "as a mask" to etch layer 304A. EX1014 ¶[0080]; EX2013 ¶8-9. I understand that other paragraphs within the certified translation use the same Japanese characters and are translated in singular form. EX1014 ¶¶[0094],[0095]; EX2013 ¶¶8-17. Additionally, in an English language translation of the '371 application provided by the applicant to the European Patent Office, the passages at paragraphs [0080], [0094], and [0095] were translated as using two layers having flush edges "as a mask" in the singular form. EX2012 at 30:11-15, 34:20-24, 35:1-4. This understanding of using two layers having flush edges "as a mask" is consistent with the understanding of a person of ordinary skill, as I describe further below in the context of multi-layer resists as masks. *See* §VI.2. Nonetheless, both translations have substantially the same meaning in the context of flush edges. Using two layers as "masks" to etch a third layer, or using two layers as "a mask" to etch a third layer, have the same result when the first two

layers have flush edges. Even if it were determined that Petitioner's translation were not in error, it would not alter my opinions.

61. The modified fifth embodiment of the '696 patent discloses dry-etching a patterned second organic film 55A "using the mask pattern 559 and the patterned silicon dioxide film 556B as a mask …." EX1001 26:15-19. This process is illustrated below in annotated versions of Figs.28(b) and 29(a). *Id.* Figs.28(b) and 29(a). These annotated figures provide a three dimensional view of the process of using two layers having flush edges as a mask. As seen below, layers 559 and 556B (both colored green), are used to etch layer 555A to uncover layer 554A.

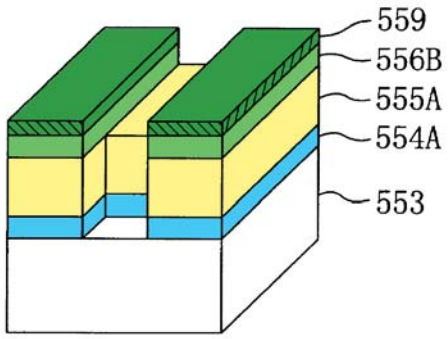


Fig. 28(b)

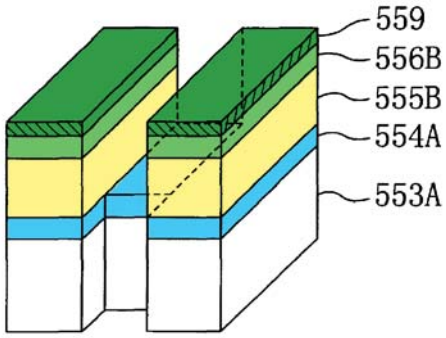


Fig. 29(a)

62. Thus, at least three embodiments, two of which are supported by the '371 application, clearly disclose using two layers having flush edges as a mask. Excluding the use of two layers having flush edges as a mask is inconsistent with these disclosures, incorrectly excludes these three embodiments, and thus is incorrect.

2. The exclusion of using two layers having flush edges as a mask is inconsistent with the plain and ordinary meaning in view of the disclosure of the '696 patent and the '371 application as understood by a person of ordinary skill in the art.

(1) A skilled person understands that two layers having flush edges may be used as a mask

(a) The Sidewalls and Top Surfaces of a Layer Serve as a Mask

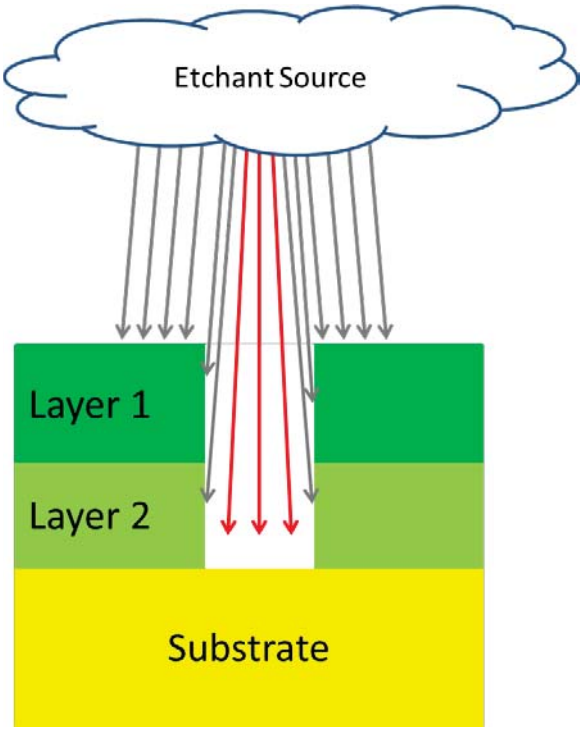
63. In imposing the additional negative limitation, the Board has taken a narrow view that considers only top surfaces of a layer and excludes sidewalls of a layer from defining areas for etching that is inconsistent with the term's plain and ordinary meaning in view of the claims and the specification for at least the reasons discussed above. *See* ID 18. A person of ordinary skill in the art would have understood that two layers together act as a mask (*i.e.*, define areas for etching) when etching is performed if each of the two layers has at least some part of its surface exposed to the etchant and thereby defines areas for etching by substantially preventing the etchant from reaching certain areas. That is, even if the top surface of the interlayer material (*i.e.*, the layer underlying the top layer) is not exposed, it still defines an area for etching if its exposed side surface substantially prevents the etchant from reaching and etching certain areas.

64. A person of ordinary skill in the art would have understood that in an etching process, etchant does not flow in a perfectly vertical direction. For example, in an anisotropic process, there is some amount of etchant that flows in a

horizontal direction impacting against sidewalls of a pattern. Thus, a mask's function is not only to define areas for etching by blocking the etchant at the mask's top surface, but also to define areas for etching by blocking the etchant through its side surface. This resistance of the sidewalls to etching becomes important when, *e.g.*, defining high aspect ratio patterns (*e.g.*, as used in the formation of contact holes).

65. One example of an orientation where two layers act as a mask is when edges of the two layers line up—*i.e.*, are "flush"—and an etchant extends down to a layer that underlies the two layers. In such an orientation, an interlayer material (the layer that is underlying the top layer) acts as a mask if at least some part of a side surface of the interlayer is exposed such that it substantially blocks the etchant from reaching certain areas, thereby defining an area for etching. As discussed further above (§VI.A.1), the '696 patent describes several embodiments that use two layers having flush edges as a mask to define areas for patterning lower layers.

66. By blocking the horizontal flow of etchant, sidewalls of a layer (*e.g.*, an overlying layer or intermittent layer) controls the flow of etchant thereby defining areas of an underlying film for patterning. I have provided a figure below to illustrate this. The resulting etch would also be different without the intervening layer (*e.g.*, Layer 2 below)—etching a wider hole than the opening in the first layer (*e.g.*, Layer 1 below).



67. A person of ordinary skill in the art would have understood that Layer 1's bottom portion bordering the hole is part of the mask. There is no meaningful difference between the function of the material bordering the hole at the top of Layer 2 from the material bordering the hole at the very bottom of Layer 1. Layer 1 and Layer 2 act together as a mask as shown above. A person or ordinary skill in the art would have understood that Layer 1 and Layer 2 together act as "a pattern of opaque material used to shield selected areas of a surface (as of a semiconductor) in deposition or etching (as in producing an integrated circuit)." EX3001 (Merriam-Webster Dictionary) 1.

68. I note that a person of ordinary skill would have understood the concept of etch selectivity, where particular materials are more sensitive to (*e.g.*,

more readily etched by) an etchant than other materials. Etch selectivity would cause the etchant to etch those particular materials at a faster rate than the other materials. A material used in semiconductor fabrication generally has at least some etch sensitivity to a conventional etchant, and so at least some amount (even if insignificant or barely noticeable) would be etched by the etchant. But when the material has a very low sensitivity to an etchant, a person of ordinary skill in the art would have understood that the material's exposed surface can substantially block the etchant during etching (*i.e.*, act as a mask).

(b) Multi-Layer Resists are an Example of Using Two Flush Layers as a Mask

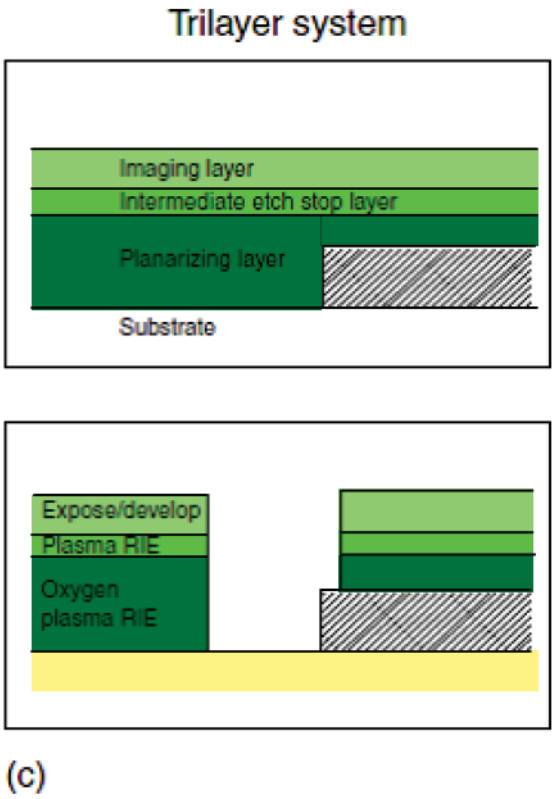
69. Using two flush layers as mask can provide technical benefits. For example, as described in §4.3.1 of the "Handbook of VLSI Microlithography" ("Helbert") (2001), "[m]ulti-layer processing techniques" where layers of radiation sensitive, non-photoresistive organic, and/or inorganic materials are stacked together to server as a "total patterning layer." EX2015 at pp.260-261 ("Multi-layer processing techniques, where layers of radiation sensitive (top), nonphotosensitive organic, and/or inorganic materials sandwiched together to become the total patterning layer…").

(2) Dr. Smith's Assertion that the '696 Patent's Disclosure of Using Two Layers having Flush Edges as a Mask is Inconsistent with the Rest of the '696 Patent Disclosure is Incorrect

70. I understand that Dr. Smith has asserted during his deposition that passages from the '696 patent that describes using two layers that have flush edges (*e.g.*, layers 358 and 355A) as a mask to etch underlying layer 354A are inconsistent with the other embodiments of the '696 patent. EX2010 45:1-47:8. I disagree. As discussed above, the '696 patent discloses three embodiments that expressly use two layers having flush edges as a mask (the modified third embodiment, third embodiment and modified fifth embodiment). Dr. Smith gives no basis to justify simply ignoring these disclosures by labeling them (incorrectly) as inconsistent.

71. Dr. Smith's testimony is also inconsistent with his own publication which describes using multiple layers in a resist (*e.g.*, a multi-layer resist). Dr. Smith is an author and editor of a book chapter entitled "Multilayer Resist Technology." EX2010 49:6-50:9; EX2018 at 657. As Dr. Smith himself confirmed, his book states that a multilayer resist techniques use "physically distinct layers to separate the imaging function from the etch resistance, planarization and reflection suppression function." EX2010 49:6-50:9; EX2018 at 657. An earlier edition of Dr. Smith's book published in 1998 also includes this passage. EX2017 at 592. As illustrated in Fig. 12.3(c), reproduced below from

Smith's book chapter, a multi-layer resist including multiple layers having flush edges (*e.g.*, a planarizing layer, an intermediate etch stop layer, and an imaging layer) is used to define areas for etching a substrate. EX2010 50:10-20, 58:8-59:1; EX2018 at 642-643 ("Three resist layers may be used to allow specific feature shaping…"). This passage is also present in the earlier edition of Dr. Smith's book published in 1998. EX2017 at 574, 592.



EX2017, Fig. 12.3(c) (annotated to show masking layers in green and substrate in yellow)

72. Dr. Smith himself acknowledged that these multiple layers are used to etch a "substrate thin film material…using this process" EX2010 64:5-65:8. Thus,

Petitioner's expert Smith, himself has acknowledged that multiple layers having flush edges (like the multilayer resist in his own text) may be used as a mask.

73. Other references recognize that "multi-layer processing techniques" that collectively form a "total patterning layer" for etching – *i.e.*, for use as a mask – were "common in semiconductor and computer manufacturing R & D labs." *See, e.g.,* EX2015 at p.260 ("Multi-layer processing techniques, where layers of radiation sensitive (top), nonphotosensitive organic, and/or inorganic materials sandwiched together to become the total patterning layer, have become common in semiconductor and computer manufacturing R & D labs."). These same techniques were in use in the field in the late 1990s as well. *E.g.*, EX2017 574, 592.

VII. Grill Is Not Prior Art to the '696 Patent

74. I understand that Petitioner is asserting that Grill (U.S. Patent No. 6,140,226) is prior art to the '696 patent. Pet. at 24-31. I also understand that in order for Grill to serve as prior art to the '696 patent, the priority date of Grill (*e.g.*, earliest filing date to which Grill is entitled) must antedate the priority date of the '696 patent (*e.g.*, earliest filing date to which the '696 patent is entitled). I understand Grill was filed on July 30, 1998, and claims priority to U.S. Provisional Patent No. 60/071,628 ("the '628 application," also "Grill provisional"), filed on January 16, 1998. EX1005 1:6-8. I understand the '696 patent was filed on March 23, 1999, and claims priority to Japanese Patent Application No. 10-079371

("the '371 application"), filed on March 26, 1998. I further understand that in order for a patent reference to be entitled to the filing date of its provisional application, the disclosure of the provisional application must provide written description and enablement support for the claims of the patent reference. *See* §IV.C. I further understand that, similarly, in order for a claim of a patent to be entitled to the filing date of a foreign patent application, the claim of the patent must be supported by the foreign patent application. *See id*.

75. As discussed below, based on my review of Grill and the '628 application, Grill is not entitled to the priority date of the '628 application at least because it does not disclose a step of transferring a pattern into a dielectric layer while concurrently removing a layer or portion of resist, as required by each of Grill's independent claims. Thus, because Grill is not entitled to the priority date of the '628 application, the earliest date to which Grill is entitled to priority is the filing date of Grill, July 30, 1998. Furthermore, as discussed below, based on my review of the '696 patent and the '371 application, claim 13 of '696 patent is entitled to the priority date of the '371 application, March 26, 1998. Because Grill's earliest priority date does not antedate the earliest priority date of claim 13 of the '696 patent, I understand that Grill is not prior art to claim 13 of the '696 patent.

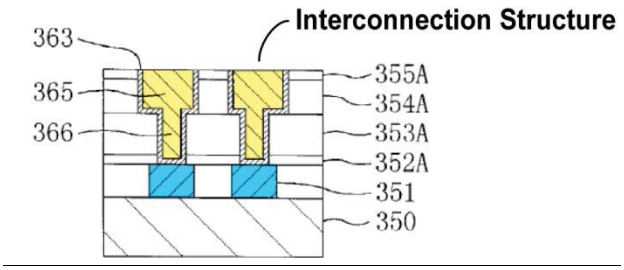
A. Claim 13 of the ’696 Patent is fully supported by the foreign priority document and is entitled to the claimed March 28, 1998 priority date

76. I understand that a claim is entitled to an earlier filing date of a foreign priority document if the foreign priority document enables and provides written description support for the claims, as explained above in § IV.C.

77. I understand that Petitioner and Dr. Smith assert that claim 13 reads onto the fifth and sixth embodiments of the ’696. Pet. at 7; EX1002 at ¶48. However, as discussed below, the ’371 application includes several embodiments, such as the third embodiment and variant of the third embodiment. Claim 13 of the ’696 patent is fully supported by at least the variant of the third embodiment. The ’371 describes the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that applicant had possession of the claimed invention. The ’371 application describes the subject matter claimed in claim 13 and enables one skilled in the art to practice the claimed invention without undue experimentation. I provide a brief summary of the support below.

1. Claim 13 (Preamble) – “A method for forming an interconnection structure, comprising the steps of:”

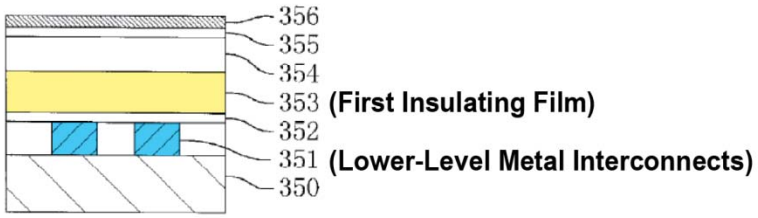
78. The ’371 application discloses a method for “forming an interconnection structure” over first metal wiring 351. *See, e.g.*, EX1014 ¶¶[0089]-[0090], FIG. 17(c).



EX1014, Fig. 17(c) (annotations and coloring added to show wiring structure in yellow, and first metal wiring 351 in blue).

2. Claim 13 (step a) – "forming a first insulating film over lower-level metal interconnects;"

79. The '371 application discloses a step of forming a first insulating film (*e.g.*, first silicon dioxide film 353) over lower-level metal interconnects (*e.g.*, first metal wiring 351). *See, e.g.*, EX1014 ¶[0090], Fig. 15(a).

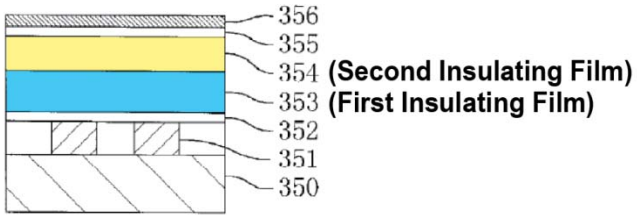


EX1014, Fig. 15(a) (annotations and coloring added to show first insulating film 353 in yellow and lower-level metal interconnects 351 in blue)

3. Claim 13 (step b) – "forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;"

80. The '371 application discloses a step of forming a second insulating film (*e.g.*, organic film 354), having a different composition than that of the first

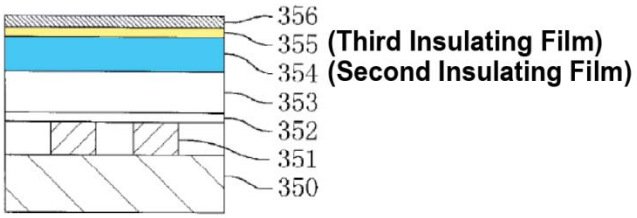
insulating film (*e.g.*, first silicon dioxide film 353), over the first insulating film (*e.g.*, first silicon dioxide film 353). *See, e.g.*, EX1014 ¶[0090], Fig. 15(a). Silicon dioxide film 353 is not an organic film, and thus has a different composition than organic film 354.



EX1014, Fig. 15(a) (annotations and coloring added to show second insulating film 354 in yellow and first insulating film 353 in blue).

4. Claim 13 (step c) – "forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;"

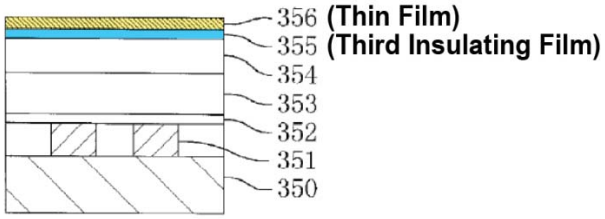
81. The '371 application discloses a step of forming a third insulating film (*e.g.*, a second silicon dioxide film 355), having a different composition than that of the second insulating film (*e.g.*, organic film 354), over the second insulating film (*e.g.*, organic film 354). *See, e.g.*, EX1014 ¶[0090], Fig. 15(a). Second silicon dioxide film 355 is not an organic film, and thus has a different composition than organic film 354.



EX1014, Fig. 15(a) (annotations and coloring added to show third insulating film 355 in yellow and second insulating film 354 in blue).

5. Claim 13 (step d) – "forming a thin film over the third insulating film;"

82. The '371 application discloses a step of forming a thin film (*e.g.*, titanium nitride film 356) over the third insulating film (*e.g.*, a second silicon dioxide film 355). *See, e.g.*, EX1014 ¶[0090], Fig. 15(a).

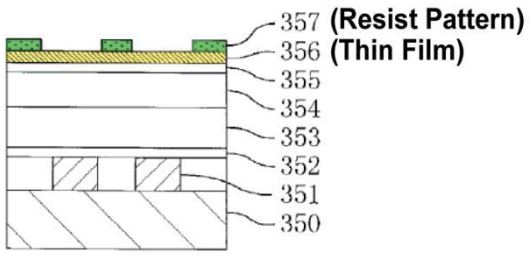


EX1014, Fig. 15(a) (annotations and coloring added to show thin film 356 in yellow and third insulating film 355 in blue).

6. Claim 13 (step e) – "forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;"

83. The '371 application discloses a step of forming a first resist pattern (*e.g.*, first resist pattern 357) having opening for the formation of wiring grooves

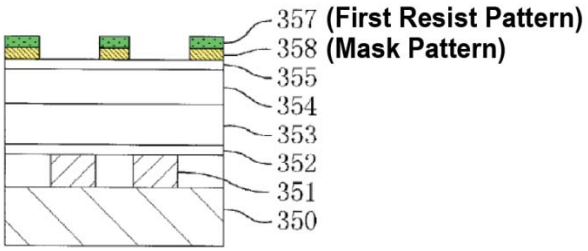
on the thin film (*e.g.*, titanium nitride film 356). *See, e.g.*, EX1014 ¶[0092], Fig. 15(b).



EX1014, Fig. 15(b) (annotations and coloring added to show first resist pattern 357 in green and thin film 356 to be etched in yellow).

7. Claim 13 (step f) – "etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;"

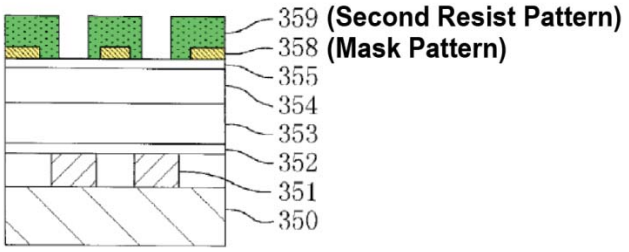
84. The '371 application discloses a step of etching the thin film (*e.g.*, titanium nitride film 356) using the first resist pattern (*e.g.*, first resist pattern 357) as a mask, thereby forming a mask pattern (*e.g.*, mask pattern 358) out of the thin film (*e.g.*, titanium nitride film 356) to have the openings for forming wiring grooves. *See, e.g.*, EX1014 ¶[0092], Fig. 15(c).



EX1014, Fig. 15(c) (annotations and coloring added to show first resist pattern 357 in green and mask pattern 358 in yellow).

8. Claim 13 (step g) – "removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;"

85. I understand that Petitioner asserts that this step is not disclosed in the '371 application's first, second, and fourth embodiments. Pet. at 16-23; EX1002 ¶¶122-127. However, Petitioner never argues this step is missing in the '371 application's third embodiment variant (*See* Pet. at 16-23(raising this issue only in connection with first, second, and fourth embodiments)), and for good reason: the variant of the third embodiment discloses this step. *See, e.g.,* EX1014 ('371 application) ¶[0093]. The '371 application discloses a step of removing the first resist pattern (*e.g.*, first resist pattern 357) and then forming a second resist pattern (*e.g.*, second resist pattern 359) on the third insulating film (*e.g.*, second silicon dioxide film 355) and the mask pattern (*e.g.*, mask pattern 358), the second resist pattern having openings for forming contact holes. *See, e.g.*, EX1014 ¶[0093] ("Subsequently, as shown in Figure 16(a), the first resist pattern 357 is removed and then a second resist pattern 359 having openings for the formation of contact holes is formed on the second silicon dioxide film 355."), Fig. 16(a).



EX1014, Fig. 16(a) (annotations and coloring added to show second resist pattern 359 in green and mask pattern 358 in yellow).

9. Claim 13 (step h) – "dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;"

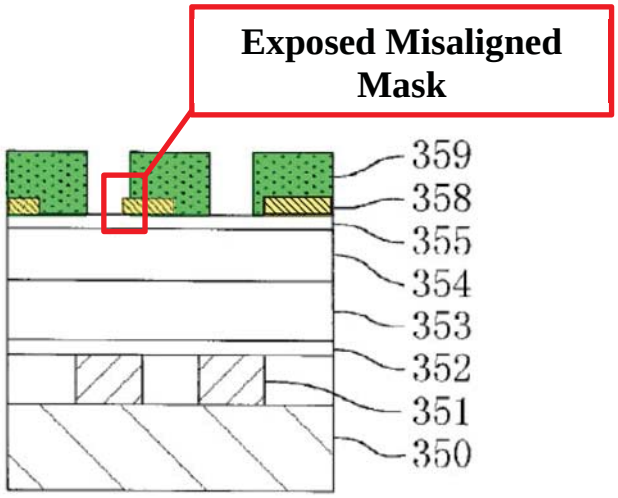
86. I understand that Petitioner asserts that this step is not disclosed by the '371 application. Pet. at 16, 19-21; EX1002 ¶¶122-0124, 128-136. Petitioner and Petitioner's expert Dr. Smith conclude that the variant of the third embodiment does not disclose the mask pattern 358 as a mask. Pet. at 19-21; EX1002 ¶[0133]. I disagree. Petitioner and Petitioner's expert Dr. Smith overlooks support in the passages of the '371 application that discloses a step of dry-etching the third insulating film (*e.g.*, second silicon dioxide film 355) using the second resist pattern (*e.g.*, second resist pattern 359) and the mask pattern (*e.g.*, mask pattern 358) as a mask, thereby patterning the third insulating film (*e.g.*, second silicon dioxide film 355) to have the openings for forming contact holes. *See, e.g.*, EX1014 ¶¶[0093]-[0096], Fig. 16(a)-Fig. 16(c).

87. The ’371 application’s variant of the third embodiment discloses step (h) of claim 13. For example, the ’371 application discloses that the second resist pattern 359 may be misaligned during fabrication. EX1014 ¶[0096]. To address this misalignment, the ’371 application describes etching the underlying mask pattern 358 using the second resist pattern 359 as a mask. *Id.* As a result, edges of the second resist pattern 359 line up and become flush with the edges of the mask pattern 358. Accordingly, when the underlying third insulating film is subsequently patterned, both the second resist pattern and the mask pattern together define areas for the patterning and are both “used . . . as a mask,” as recited in claim 13. Specifically, the ’371 application discloses:

> If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched using the second resist pattern 359 as a mask. ***That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner, the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes.***

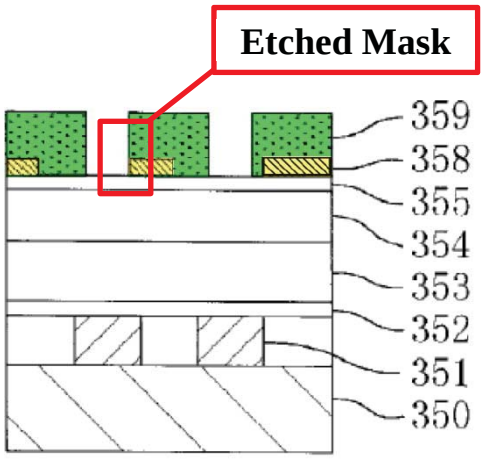
EX1014 ¶[0096] (variant of third embodiment).

88. The series of annotated figures below illustrate this patterning in case of misalignment, according to the disclosure of the '371 application discussed above. The first annotated figure below shows the layers "if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment[.]" EX1014 ¶[0096].



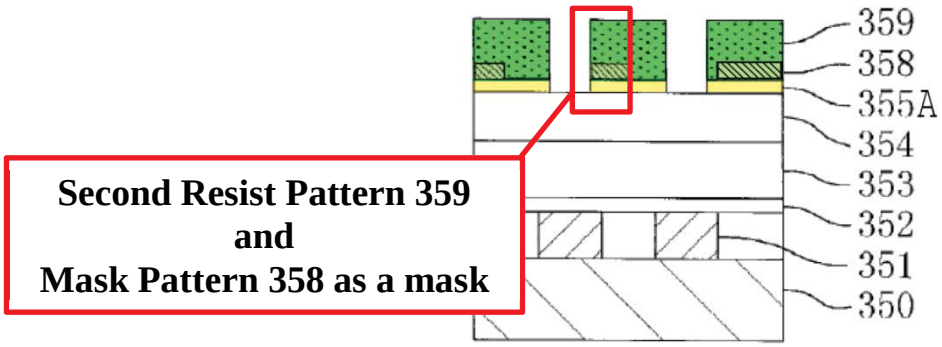
EX1014, Fig. 16(a) (modified according to EX1014 ¶[0096] and coloring added to show second resist pattern 359 in green and exposed portion of misaligned mask pattern 358 in yellow).

89. The second annotated figure below shows the layers after "the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask." EX1014 ¶[0096].



EX1014, Fig. 16(a) (modified according to EX1014 ¶[0096] and coloring added to show second resist pattern 359 in green and etched misaligned mask pattern 358 in yellow).

90. The third annotated figure below shows that, when the underlying third insulating film (355) is thereafter etched, both the second resist pattern (359) ***and*** the mask pattern (358) necessarily define the areas for etching of the third insulating film (355). As such, etching of the "third insulating film [355]" is done "using the second resist pattern [359] and the mask pattern [358] as a mask" as required by step (h) of claim 13. EX1014 ¶[0093].



EX1014, Fig. 16(a) (modified according to EX1014 ¶¶[0093], [0096] and coloring added to show second resist pattern 359 in green, etched misaligned mask pattern 358 in light green, and etched layer 355A in yellow).

91. Additionally, the '371 application provides support for using two layers as a mask in a similar manner as discussed above with reference to Figures 13(b)-13(c) and 16(c)-16(d). *See* §VI.A.1. For example, Figures 13(b) and 13(c) and paragraph [0080] of the '371 application provides similar support as Figures 13(b) and 13(c) and 17:34-40 of the '696 patent. For example, Figures 16(c) and 16(d) and paragraph [0095] of the '371 application provides similar support as Figures 16(c) and 16(d) and 19:50-53 of the '696 patent.

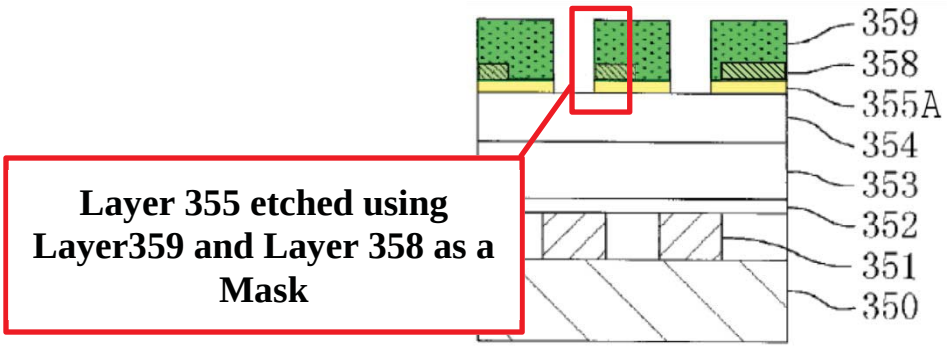
10. Claim 13 (step i) – "dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;"

92. I understand that Petitioner asserts that this step is not disclosed by the '371 application. Pet. at 16, 21-23; EX1002 ¶¶136-139. I disagree. The '371 application's third embodiment variant discloses a step of dry-etching the second insulating film (*e.g.*, organic film 354) using the patterned third insulating film (*e.g.*, patterned second silicon dioxide film 355A) as a mask, thereby patterning the second insulating film to have the openings for forming contact holes. *See, e.g.*, EX1014 ¶[0093], Fig. 16(b).

93. In particular, the '371 application discloses that layers 355 and 354 are "***sequentially***" *etched* using the pattern 359 as a mask. '371 application ¶[0093]. I have created the following annotated figures below, based on Fig. 16(a), when the pattern of 358 is misaligned to the pattern of 359, to illustrate this sequential etching.

94. Thus, at a minimum, a person of ordinary skill in the art would have understood that the following sequence occurs:

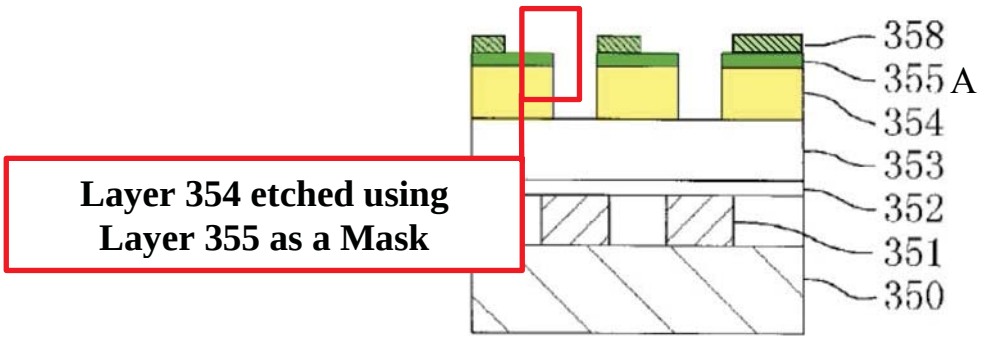
(1) **First**, layer 355 is etched using pattern 359 as a mask. As a result, edges of layer 355 line up and become flush with edges of 359;



EX1014, Fig. 16(a) (modified according to EX1014 ¶¶[0093], [0096] and coloring added to show second resist pattern 359 in green, etched misaligned mask pattern 358 in light green, and etched layer 355A in yellow).

(2) **and then second**, layer 354 is etched "using" at least layer 355 ("the patterned third insulating film") "as a mask" because (1) pattern 359 and layer 355 together define areas for patterning of layer 354 and (2) layer 355

acts as a mask after the removal of layer 359 in the aforementioned sequential etching process. That layer 355 is used as a mask for etching layer 354 is further supported by the '371 application's disclosure that "the second resist pattern 359 is removed during the step of etching the organic film 354." EX1014 ¶[0093] (indicating that layer 355A acts as a mask during the patterning of layer 354 due to the removal of resist 359).

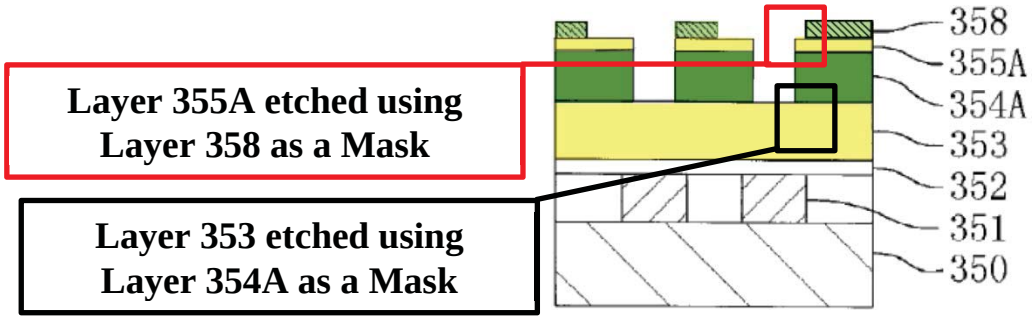


EX1014, Fig. 16(a) (modified according to EX1014 ¶¶[0093], [0096] and coloring added to show etched misaligned mask pattern 358 in green, layer 355A in light green, and etched layer 354 in yellow).

95. Accordingly, the '371 application discloses dry-etching the second insulating film (*e.g.*, 354) using the patterned third insulating film (*e.g.*, 355A) as a mask, as claimed in step 13(i).

11. Claim 13 (step j)– "dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively;"

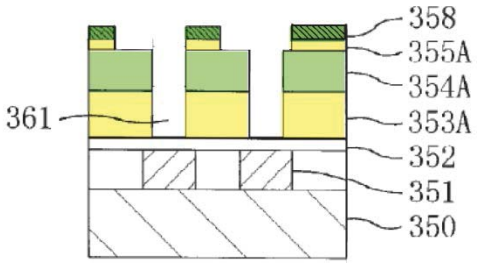
96. The '371 application discloses a step of dry-etching the patterned third insulating film (*e.g.*, patterned second silicon dioxide film 355A) and the first insulating film (*e.g.*, first silicon dioxide film 353) using the mask pattern (*e.g.*, mask pattern 358) and the patterned second insulating film (*e.g.*, patterned organic film 354A) as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film (*e.g.*, patterned first silicon dioxide film 353A), respectively. *See, e.g.*, EX1014 ¶[0094], Fig. 16(c)-Fig. 17(a). [6]



[6] Although the '696 provides exemplary labels for several films (*e.g.*, EX1001 19:4-9) (referring to, *e.g.*, "second insulating film"), a person of ordinary skill in the art would not consider the labels for these films to be definitional or limiting.

EX1014, Fig. 16(b) (modified according to EX1014 ¶¶[0093], [0096] and coloring added to show etched misaligned mask pattern 358 and layer 354A as respective masks in green, and layer 355A and layer 353 to be etched in yellow).

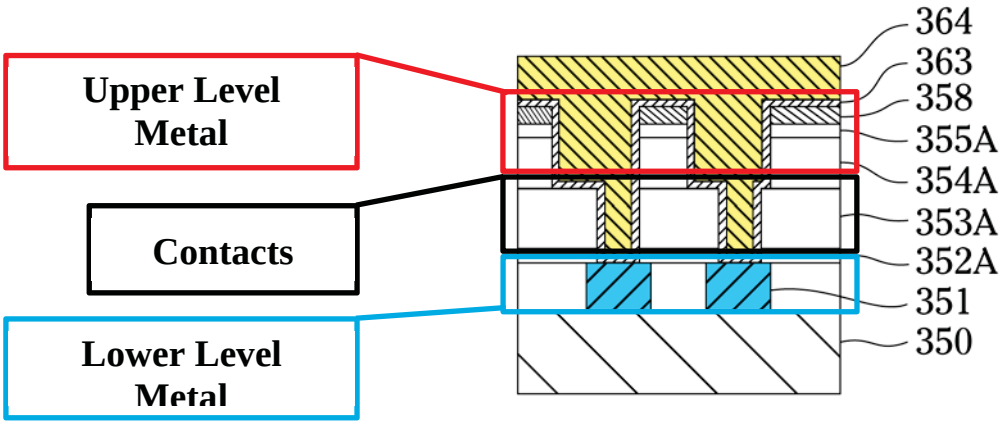
97. After dry-etching the patterned third insulating film (*e.g.,* patterned insulating film 355A) and dry-etching the first insulating film (*e.g.,* insulating film 353), the resulting structure of Fig. 16(c) would appear as:



EX1014, Fig. 16(c) (modified according to EX1014 ¶¶[0093], [0096] and coloring added to show etched misaligned mask pattern 358 and layer 354A as respective masks in green, and etched layer 355A and etched layer 353 in yellow).

12. Claim 13 (step k) – "filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together."

98. The '371 application discloses a step of filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together. *See, e.g.*, EX1014 ¶[0098], Fig. 17(b)-(c).



Modified EX1014, Fig. 17(b), EX1014 (modified according to EX1014 ¶¶[0093], [0096] to show result of process with misaligned mask pattern 358).

99.

100. The modified Fig. 17(b) above illustrates a metal interconnection structure when a wiring groove resist pattern is misaligned from a contact hole resist pattern. As discussed above in reference to (step h), a portion of the misaligned wiring pattern mask may be etched. Although this etching of the wiring pattern mask may result in a slightly wider wire and slightly narrower spacing between wires, it does not ultimately affect the number of wires that are fabricated and therefore does not affect the density or number of wires that can be formed using this process.

101. Accordingly, the ’371 application describes the subject matter claimed in each limitation of claim 13 and enables one skilled in the art to practice the claimed invention without undue experimentation. One reasonably skilled in the art could use the invention from the disclosures in the ’371 coupled with information

known in the art without undue experimentation. Because the '371 application meets the requirements of written description and enablement for each limitation of claim 13, I understand that claim 13 of the '696 patent is entitled to the priority date of '371 application, March 26, 1998.

B. Petitioner has not shown and cannot show that Grill is entitled to the priority date of the Grill Provisional

102. I understand that in order for Grill to claim the benefit of the filing date of its provisional application (the '628 application), Grill's provisional application must provide support for the claims in Grill.

103. Each of Grill's independent claims requires a step of transferring a pattern into a dielectric layer while concurrently removing a layer or portion of resist, illustrated in the table below. EX1005 10:59-65, 12:25-30, 13:54-58, 15:3-7, 16:14-17.

Grill claim	***Limitation***
1	transferring said wiring pattern into said second dielectric layer to form wiring cavities corresponding to said wiring pattern, ***while concurrently removing*** said wiring-patterned layer of resist,
15	transferring said via pattern into said second dielectric layer to form via cavities corresponding to said via pattern, ***while concurrently removing*** said via-patterned layer of resist,
28	transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, ***while concurrently removing*** said via-patterned second layer of resist, and
35	transferring said via pattern in said patterned first hard mask layer into said second dielectric layer ***while concurrently removing*** any residuals of said patterned second layer of resist,
42	transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, ***while concurrently removing*** any residuals of said patterned second layer of resist,

104. For example, claim 28 requires "transferring said via pattern in said patterned first hard mask layer into said second dielectric layer, ***while concurrently removing*** said via-patterned second layer of resist." EX1005 cl.28. Each of Grill's independent claims requires a similar concurrent removal. EX1005 10:58-62,

12:25-30, 13:47-50, 14:62-65, 16:14-18. However, the recited concurrent removal is not supported by Grill's provisional application. Accordingly, each of Grill's independent claims 1, 15, 28, 35 and 42 is both not supported and not enabled by Grill's provisional, the '628 application.

1. Grill includes multiple statements that were added to and not disclosed in Grill's provisional

105. I prepared a comparison of the text of Grill's non-provisional patent to the text of Grill's provisional application. I obtained the text of the description of Grill's non-provisional patent from the USPTO website by searching under Grill's non-provisional patent number U.S. 6,140,226. I obtained the text for Grill's provisional application by conducting an optical character recognition (OCR) process. I then compared the text of the two documents in Microsoft word and corrected for any formatting errors. The final result is attached as EX2011.

106. Based on my comparison of Grill's non-provisional patent text and provisional patent text, I found many statements that were either added to or modified in Grill's non-provisional patent text. *E.g.*, EX1005 2:32-35, 4:5-11, 4:45-47, 4:60-61, 7:25-29, 7:51-55, 7:64-66, 9:39-43, and 9:60-62, as shown in the attached redline comparing the two applications (EX2011).

107. For example, as shown by the comparisons below, a number of statements were added (indicated with bold and underline emphasis) regarding concurrent removal of photoresist layers or residuals of photoresist layers.

Hard mask layer 14 is then patterned with said first pattern by etching through the openings in patterned resist layer 16, as shown in FIG. 1E. Said first pattern is then transferred into the entire thickness of dielectric 12 by an etching process such as reactive ion etching (RIE), as shown in FIG. 1F. **This etching process typically also removes all residuals of patterned resist layer 16**.

Comparing Grill (EX1005) at 4:41-48 and the '628 application (EX1017) at p.13.

The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of FIG. 5F. **Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12**.

Comparing Grill (EX1005) at 7:62-66 and the '628 application (EX1017) at p.15.

Dielectrics 8 and 12 are then etched to transfer the second pattern into the entire thickness of dielectric 12, and the first pattern into the entire thickness of dielectric 8, as shown in FIG. 1I. **This etching process typically also removes all residuals of patterned resist layer 18.**

Comparing Grill (EX1005) at 4:58-60 with the '628 application (EX1017) at p.13.

The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to form the structure of FIG. 7G. **Patterned second resist layer 82 is absent from FIG. 7G because it is typically removed by the etching process used to pattern dielectric 12.** The etching conditions are then changed to removed exposed portions of lower hard mask layer 76 and optional etch stop 10, to form the structure of FIG. 7H.

Comparing Grill (EX1005) at 9:55-65 with the '628 application (EX1017) at p.17.

108. Additionally, several statements were added to the non-provisional that describe wet etching, in addition to ashing for removing photoresist. *Compare* Grill (EX1005) ***e.g.***, 4:37-40, 5:62-67, 6:6-20, 6:49-53 with the '628 application (EX1017) at 13-17.

2. Dr. Smith has failed to show that the '628 provides written description support for the claims of Grill

109. I have been informed that there is a dispute as to whether Dr. Smith's arguments regarding whether Grill is entitled its priority date are admissible in the proceeding. Although I understand that Patent Owner has taken the position that they are not, I provide below my opinion on those arguments by Dr. Smith relating to Grill's priority date. My opinions are not intended as an admission as to whether Dr. Smith's arguments are admissible.

110. The arguments set forth by Petitioner's expert Dr. Smith about Grill's priority date in his declaration fail to show that the '628 provisional provides written description support for any claim of Grill. Pet. at 24-25; EX1002 ¶[0153], App. B. Appendix B of Dr. Smith's declaration (EX1002) purportedly charts the '628 provisional against Grill claim 28, but as explained below, it cannot provide the elements missing in the '628 provisional. *See* EX1002, App. B.

111. As discussed above in §IV.A about relevant legal standards, I have been informed that a prior art reference discloses a feature if it either expressly or inherently discloses that feature. In order for a prior art reference to inherently

disclose a feature, there must be no other possible alternative to the implementation of the feature, in view of the prior art reference's disclosure. However, as discussed below, claim 28's limitations are not "necessarily present" because there exist other possible alternative implementations. *Id*.

112. Dr. Smith has failed to show, under either of these express or inherent standards, that the '628 provisional discloses "transferring the via pattern in the patterned first hard mask layer into the second dielectric layer, *while concurrently removing said via patterned second layer of resist,*" as required by Grill's Claim 28.[7]

[7] As I discussed above in §VII.D, each of Grill's independent claims includes a similar "concurrently removing" limitation. Claims 1, 15, and 28 recite "transferring said [wiring/via] pattern into said second dielectric layer to form [wiring/via] cavities corresponding to said [wiring/via] pattern, *while concurrently removing said* [*wiring/via*]*-patterned layer of resist*"; and claims 35 and 42 recite "transferring said via pattern in said patterned first hard mask layer into said second dielectric layer *while concurrently removing any residuals of said patterned second layer of resist*[.]" EX1005. Thus, the '628 application fails to support any of Grill's claims for the same reasons discussed herein above.

113. The ’628 provisional fails to provide any support for this element of claim 28, which requires concurrently removing a second layer of resist when transferring a via pattern of a first hard mask into the second dielectric layer. The ’628 provisional does not contain any support for concurrently removing ***any*** layer of resist while etching any dielectric layer, let alone concurrently removing the specific resist layer during the patterning of the specific dielectric layer recited in the claim 28.

114. Instead, express statements about the concurrent removal of a photoresist layer or residuals of a photoresist layer were added to the non-provisional application.[8] *See above* at §VII.B. The only support for this element

[8] Further demonstrating that this disclosure was not in the ’628, several similar sentences were added to the non-provisional. *E.g., compare* Grill (EX1005) at 4:41-48 *with* the ’628 application (EX1017) at 13; Grill (EX1005) at 4:44-48, 4:58-60 *with* the ’628 application (EX1017) at 13; Grill (EX1005) at 9:55-65 *with* the ’628 application (EX1017) at 17. *See* §VII.B.1. In addition, Figures 3A-3C shown in Grill’s non-provisional application further show the photoresist pattern 34 being removed ***after*** transferring the wiring pattern into the second dielectric layer 12, ***not concurrently*** with the transfer. *Compare* EX1005 Fig.3A, Fig.3B (showing that the photoresist layer 34 is present ***after*** hard mask layer 14,

of claim 28 contained in Grill was added (as indicated in bold and underlined) in the non-provisional application of Grill:

> The via level pattern is then transferred into dielectric 12 by an etching process such as reactive ion etching, to produce the structure of FIG. 5F. **Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12**.

Compare Grill (EX1005) 7:62-66 *with* the '628 application (EX1017) at 15.

115. Absent any clear disclosure, a person of ordinary skill in the art would have understood that the Grill provisional (the '628 application) does not disclose concurrent removal of photoresist, and indeed fails to provide a disclosure of *any* timing for when the removal of the photoresist happens (*e.g.*, it might occur before or after the transfer of the pattern). Because alternatives exist to the concurrent removal of the photoresist layer or residuals of a photoresist layer, the concurrent removal is not the only way to remove the photoresist layer in Grill. Thus, because it is not the only way to remove the photoresist layer, it is not necessarily present in Grill's provisional, and as such Grill's provisional does not inherently disclose any of these claimed features.

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dielectric 12 and etch stop 10 have been etched), Fig.3C (showing the photoresist layer 34 has been removed).

116. Dr. Smith admits that the bolded and underlined statement above (which describes that the resist layer 62 is removed by the etching process used to pattern dielectric 12) was missing from Grill's provisional and added to Grill's non-provisional application. EX1002 App.B B-9 to B-10. However, Dr. Smith asserts that a person of ordinary skill in the art would already have understood this missing text "to be part of the '628 application's disclosures." EX1002, App.B B-9 to B-10. Dr. Smith is incorrect because he bases his argument on two assumptions that are unsupported by and inconsistent with the actual disclosures of the provisional '628 application and Grill.

(1) **Dr. Smith's reliance on a disclosure relating to etch characteristics in the Background of the '628 application is misplaced**

117. To support his argument that the '628 discloses concurrently removing the second layer of resist when transferring the via pattern of the first hard mask into the second dielectric layer, Dr. Smith relies on a portion of the '628's Background of the Invention section, which states that "difficulties in reworking the second lithography step may occur if the interconnect dielectric and the photoresist stencil used to pattern the hard mask have similar etch characteristics." EX1002, App.B B-9-10. (citing EX1017 11). Based on this disclosure, Dr. Smith concludes a person of ordinary skill in the art "would have

understood that etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have similar etch properties." *Id.*

118. I have been informed that there is a dispute as to whether the reference to layer 58 in Dr. Smith's statement should be revised, as a typographical error, from "concurrently etches ***layer 58***" to "concurrently etches ***layer 62***." attributing the revision to a typographical error. I provide my subsequent analysis on the assumption Dr. Smith's originally-filed Declaration will not be revised. Based on Dr. Smith's originally-filed Declaration, his conclusion that "etching layer 12 under such circumstances concurrently etches layer 58 because the two layers have similar etch properties" is entirely unsupported.

119. Dr. Smith has failed to explain why this portion of the '628 that discusses a *problem in the prior art* criticized by Grill actually applies to the particular embodiment (*e.g.,* "a first preferred embodiment") containing layers 12 and 58 in Grill's asserted invention *responding to these problems* of the prior art. EX1002, App.B B-9-10. He fails to cite any evidence that indicates that "such circumstances"—*i.e.*, the etch properties present in a problematic situation described in the Background section—are present in the particular embodiment and the particular layers disclosed in the '628. Instead, the '628 expressly discloses that the specific layers 12 and 68 that Dr. Smith points to as having "similar etch properties," preferably have ***different*** etch properties: "Hard mask

layers 56 and 58 are preferably formed from different materials which have different etch properties from each other and from the dielectric underlayers 12 and 8." EX1017 15. This contrasts with Dr. Smith's explanation in the same chart that when two layers have different etch properties, one layer is not removed concurrently when etching the other. EX1002, App. B B-7.

120. Additionally, even if Dr. Smith were able to change his testimony, Dr. Smith fails to explain how discussions of "etching" in the Background section can be applied to this embodiment to provide support for this limitation, which requires "removing" an entire layer. More specifically, Grill's claim 28, the subject of Dr. Smith's discussions, uses the terms "etching" and "removing" to describe different acts. *See, e.g.*, EX1005, cl.28 ("selective *etching* of said second hard mask layer with respect to said first hard mask layer"); cl.28 ("concurrently *removing*…layer"). Dr. Smith assumes without providing any support that "etching" is the same as "removing," which is not the understanding of a person of ordinary skill in the art. Even if it could be shown that "etching" equates to partial removal, the claims require "concurrently removing…[the] layer" and not just partial removal.

(2) Dr. Smith's opinion that concurrent etching of the photoresist layer and the dielectric layer is the only possibility is unsupported and contradicted by the '628

121. Dr. Smith additionally opines that a person of ordinary skill in the art would have "further understood that the photoresist layer 62 is not removed prior

to etching [dielectric] layer 12." EX1002, App. B B-10. He then concludes a person of ordinary skill in the art "would have thus understood that the transition between Figures 5E and 5F above is *only possible by concurrently etching* photoresist layer 62 and dielectric layer 12." EX1002, App. B B-10. Dr. Smith's opinion is unsupported by and inconsistent with the disclosures of the '628 application, as understood by a person of ordinary skill in the art.

122. The '628 does not disclose concurrent removal of photoresist, and indeed fails to provide a disclosure of any timing for when the removal of the photoresist happens (*e.g.*, it might occur before or after the transfer of the pattern).

123. Even if it were assumed, as Dr. Smith opines, that a person of ordinary skill in the art would not have removed the photoresist layer prior to etching the dielectric layer, Dr. Smith still fails to explain why the photoresist layer must *necessarily* be removed ***concurrently*** with the etching of the dielectric layer, as opposed to ***after*** the etching of the dielectric layer.

124. Dr. Smith has opined that stripping the photoresist before etching the dielectric would "make it difficult to control the via dimension." EX1002 App. B B-10. However, even if stripping the photoresist before etching dielectric 12 would be undesirable, Dr. Smith's conclusion that the transition between figures 5E and 5F is "*only possible* by concurrently etching photoresist layer 62 and dielectric layer 12" simply does not follow and is unsupported. *Id.* Even if Dr.

Smith were correct in assuming that etching the resist concurrently with the etching of the dielectric makes it *easier* to obtain a certain desirable characteristic, it does not follow that such concurrent etching is the "only possible" way to remove the photoresist.[9] Dr. Smith's attempt to argue inherent disclosure of this limitation clearly fails.

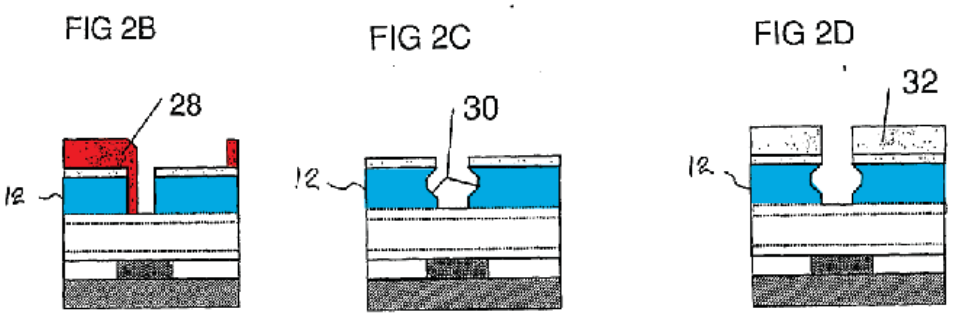
(3) Dr. Smith's opinions are based on problems inapplicable to the independent claims of Grill

125. Dr. Smith's asserts that "the transition between Figs. 5E and 5F is *only possible* by concurrently etching photoresist layer 62 and dielectric layer 12." EX1002 App. B B-10. However, this argument is based on mischaracterizations of the '628's disclosure. To support his opinion, Dr. Smith states that "[a] person of ordinary skill in the art would have further understood that…if the photoresist is stripped with a wet chemical treatment before etching layer 12, the problems

[9] Indeed, passages added to Grill's non-provisional application further confirm that concurrent removal of the photoresist when etching the dielectric layer is ***not*** the only possibility. As discussed above (§VII.B.1), the non-provisional application added the following: "Patterned second resist layer 62 is absent from FIG. 5F because it is ***typically*** removed by the etching process used to pattern dielectric 12." EX1005 7:61-67. Contrary to Dr. Smith's declaration, this added language confirms that concurrent removal is not the *only* possibility.

described with regard to Figures 2C result…. This would damage the exposed interlayer dielectric layer 12 and make it difficult to control the via dimension." *See* EX1002, App.B B-10. However, contrary to Dr. Smith's opinion, the problems described in Figure 2C are not problems for the embodiment associated with Figures 5E and 5F that Dr. Smith relies upon to show support for Grill's claim 28.

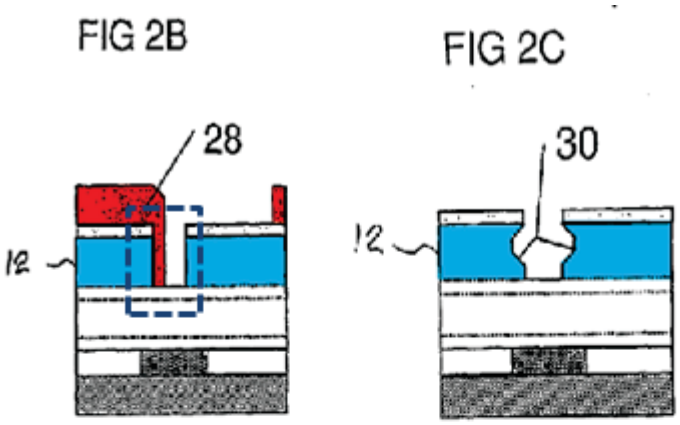
126. Figures 2C-2D address a "problem" where the "[s]idewalls 30 of dielectric 12 are clearly undercut" when "an ashing process [is used] to remove misaligned patterned resist layer 28." *See* EX1017 13, Figs. 2B-2D (disclosing the formation of concave undercuts (*e.g.*, 30) of dielectric layer 12).

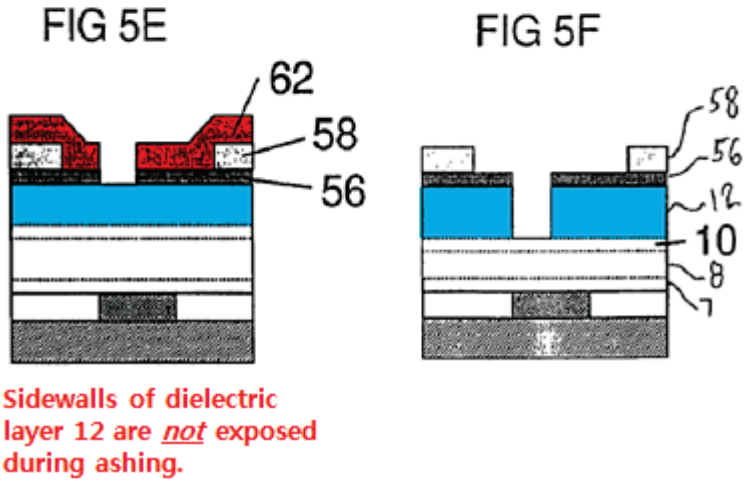


127. For at least three reasons, Dr. Smith's opinion that the "undercut" problem of Figures 2C-2D applies to the process of Figs. 5E-5F is incorrect. *First*, the '628 provisional only discloses removing photoresist by ashing. The disclosure of removing a photoresist by wet chemical treatment was only added later to the specification by Grill's non-provisional application. *Compare* EX1017 *with* EX1005, *e.g.*, 4:37-40, 5:62-67, 6:6-20, 6:49-53. Thus, Dr. Smith's opinion that a

person of ordinary skill in the art would have recognized problems with wet etching based on the '628 is unsupported and unsupportable.

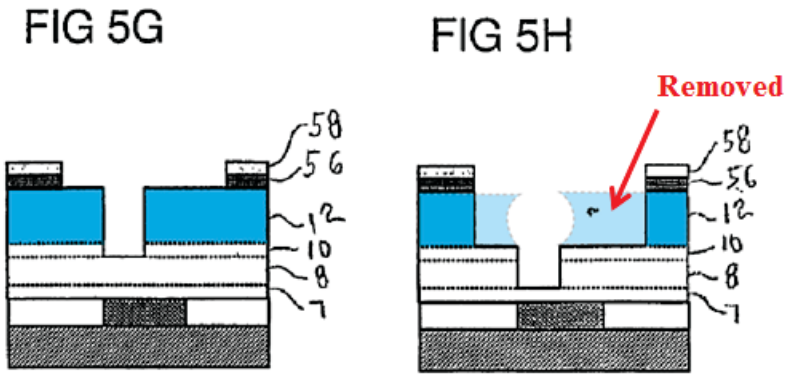
128. *Second*, the "undercut" problem of Figures 2C-2D occurs when the sidewalls are exposed *during ashing*. *See* EX1017 13, Figs.2B-2D. However, Figure 5E clearly shows that no sidewalls have yet been formed. *See* EX1017, Figs.5E-5F (annotated to show that dielectric layer 12 (blue) sidewalls are not exposed until Fig. 5F):





129. Because the sidewalls of dielectric 12 have not yet been formed and thus cannot be exposed to the ashing process, the dielectric 12 would not be subject to the "undercut" problem of Figs. 2C-2D even if the photoresist were removed before etching layer 12 in Fig. 5E.

130. *Third*, the same paragraph relied on by Dr. Smith explicitly teaches that "[undercutting] may not be a problem when the dimensions of said second pattern substantially exceed the dimensions of the first pattern, since the undercut regions would be etched away." EX1017 13. This means that if the dimensions of a second pattern (*e.g.*, a wiring pattern), exceeds the dimensions of the first pattern (*e.g.*, a via pattern), the damaged portions of sidewalls in the smaller pattern would be etched away. This is precisely the circumstance illustrated in Figures 5E-5H. Dr. Smith fails to address that any damage or undercutting to the exposed portion of layer 12 that may result from removing the resist prior to etching (Figs.5E-5F) would not impact layer 12 of the finished structure because any damaged portion of layer 12 would be ultimately removed during the subsequent etch. The embodiment of Figures 5E-5G has an opening in the second hard mask layer 58 with greater dimensions (width) than that of the first hard mask (56). *See* EX1017 Figs.5G-5H (annotated to disclose portion of layer 12 ultimately removed, even assuming undercutting occurred).



131. For the reasons discussed above, Dr. Smith's testimony is unsupported and cannot be credited, as it relies on the problem of Figure 2, which is inapplicable to the process of Figure 5.

132. Accordingly, while the '696 patent is entitled to its claimed foreign priority date, Dr. Smith has failed to show (and cannot show) that Grill is entitled to its provisional date because he has failed to and is unable to show that at least the "concurrently removing" limitation of claim 28 (and all other independent claims) of Grill is supported by the '628 application. As explained above, the subject matter claimed in claim 28 is not described by the '628 provisional application and based on the disclosures in the '628 provisional application, a person or ordinary skill in the art would not reasonably understand that the inventor was in possession of the claimed subject matter. Because the Grill provisional application fails to support the claims of the Grill non-provisional application, including claim 28, Grill is not entitled to its provisional filing date. Because the '696 patent is entitled to its foreign priority date, which predates

Grill's non-provisional filing date, it is my understanding that Grill is not prior art to claim 13 of the '696 patent.

VIII. Overview of Petitioner's Prior Art References

A. Grill

133. U.S. Patent No. 6,140,226 ("Grill"), entitled "Dual Damascene Processing for Semiconductor Chip Interconnects," describes lithographic methods for forming a dual relief pattern in a substrate in order to fabricate multilevel interconnect structures. EX1005 1:10-15. The dual-relief patterns of Grill include a larger wiring pattern and a smaller via pattern that are used to form a dual relief cavity that includes a wiring trench and via hole. EX1005 1:48-49, 7:25-29. As explained above, it is my opinion that Grill is not, in fact, prior art to the '696 patent.

B. Aoyama

134. U.S. Patent No. 6,140,226 ("Aoyama"), entitled "Semiconductor Device Having a Wiring Layer With a Barrier Layer," generally relates to techniques of buried wiring in semiconductors. EX1018 Abstract, 1:6-9. Aoyama describes an example 7 that uses a wider through-hole pattern in combination with an etch stopper layer 45 to control dimensions of its contact holes. EX1018 3:6-38, 6:7-13, 15:48-16:30. Petitioner's expert, Dr. Smith, describes this etch stopper layer 45 as "an etch stopper made of carbon," consistent with Aoyama. *See* EX2010 106:12-20; EX1018 16:3-5. Aoyama's carbon etch stopper layer 45 is

exposed to a photoresist removal process. *See* EX1018 Fig. 18B. As further discussed below, Grill recognizes that such a removal processes is detrimental to organic layers such as Aoyama's carbon etch stop layer (*see*, *e.g.*, EX1005 4:35-40, 5:8-22, 16:3-5, Fig. 2C). This embodiment of Aoyama also uses a photoresist profile that is thicker over a via hole, which Grill warned is detrimental to control of critical dimensions. EX1005 Fig. 2A, 5:28-32.

IX. The Combination of Grill and Aoyama is not obvious

135. I understand that Petitioner proposes to combine Grill's dual-hard masks with Aoyama's wider via pattern. Pet. at 46-49; EX1002 ¶¶162-0163. More specifically, Petitioner proposed to modify Grill's photoresist layer 62 to use Aoyama's wider through-hole pattern. Pet. at 46-49; EX1002 ¶¶162-163. I understand that the Board relied upon arguments by Petitioner and Petitioner's expert Dr. Smith that Grill and Aoyama provide allegedly complementary solutions to address problems of misalignment in a dual damascene process. ID 40. More specifically, the Board relied upon Petitioner's argument that "combining Grill's two hard masks with Aoyama's widened via pattern would not require modification of the Grill process" because "nothing about the width of the via pattern in Aoyama affects the dual-hard mask structure of Grill, and nothing about the dual-hard mask structure of Grill affects the width of the via pattern in Aoyama." *See* ID 40-41 (citing EX1002 ¶[0163], Pet. at 49). I disagree. There are

various reasons why a person of ordinary skill would not have been motivated to combine Grill and Aoyama in the manner proposed by Petitioner and why the person of ordinary skill would not have had a reasonable expectation that the proposed combination would work. And, as further explained below, Petitioner's and Dr. Smith's conclusory assertions that "nothing" from Aoyama "affects" Grill are simply incorrect.

136. When combining references to show the limitations of a claim, I understand that it is improper to use the claims as a roadmap for the combination. Furthermore, I understand that a reference teaches away from a claimed invention if it criticizes, discredits, or discourages investigation of the claimed invention, or if the combination of two references would be inoperable. I also understand that if a proposed modification of a prior art reference changes a principle of operation of the prior art reference the proposed modification might not be obvious. I understand that if a proposed modification of a prior art reference renders the reference inoperable for its intended purpose, then the proposed modification might not be obvious. Additionally, I understand that a combination is not obvious where a person of ordinary skill in the art would not have had a reasonable expectation of success in making and practicing the invention.

137. As explained below, Petitioner's proposed combination appears to rely on the '696 patent as a roadmap. Indeed, a person of ordinary skill in the art

would have understood Grill to teach away from the proposed combination with Aoyama. The modifications of Grill would completely do away with Grill's dual-relief pattern, which is a critical feature of Grill, and thereby eliminates its intended purpose. Petitioner's proposed modification to use a wider via hole pattern, which would expose Grill's upper hard mask layer and lower hard mask layer to an extra etch step, fails to consider problems that would manifest in the form of premature degradation of Grill's upper hard mask that would cause widening of Grill's wire over a via hole—thereby diminishing Grill's control over critical dimensions. Petitioner's proposed modification of Grill to remove layer 7 would result in the creation of an insulating film that would render Grill's final structure inoperable because it would prevent electrical contact between a lower layer and an upper layer. For at least these reasons, a person of ordinary skill in the art would not have found it obvious to modify Grill by Aoyama in the manner proposed by Petitioner.

A. Petitioner's proposed modification of Grill eliminates Grill's use of dual-relief patterns to form dual-relief cavities

138. A person of ordinary skill in the art would have understood that the use of dual-relief patterns to form dual-relief cavities is the expressly stated intended purpose of Grill. As discussed above in §VIII.A, Grill repeatedly emphasizes throughout its specification that its "present invention" is directed to forming a dual relief pattern and using said dual relief pattern to form a dual relief

cavity in a substrate. EX1005 Abstract, 1:12-15, 2:41-50, 7:16-19. Grill uses dual relief patterns to form dual relief cavities in order to control critical dimensions of features such as vias. EX1005 Abstract, 1:12-15, 2:41-50, 5:24-33. Petitioner's expert Dr. Smith has acknowledged in his declaration and confirmed during his deposition that the dimensions of vias "need to be tightly controlled." EX2010 16:16-17:12; EX1002 ¶47; *see also* EX1005 5:24-33, 7:16-29 (discussing "critical dimension" control). Controlling dimensions of vias is essential to increasing density of wires in underlying layers.

139. Grill describes lithographic methods for forming its dual relief pattern in a substrate in order to fabricate multilevel interconnect structures. EX1005 1:10-15. Grill's dual-relief patterns include a larger wiring pattern over a smaller via pattern that are used to form a dual relief cavity that includes a wiring trench and via hole, respectively. EX1005 1:48-49, 7:25-29. Grill only discloses these dual-relief patterns and cavities in the context of a cross-sectional dimension across the width of the wire (*e.g.*, as illustrated below in annotated Figure 5H of Grill). In contrast, Grill does not disclose any cross-section along a length of a wire (*e.g.*, into the page of Figure 5H below).

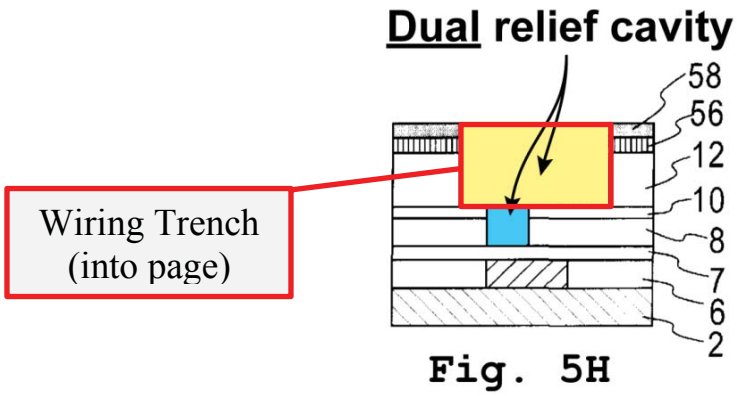


Fig. 5H

140. Petitioner's expert Dr. Smith has admitted that Grill only discloses dual-relief patterns that are in a cross-section direction across a wiring trench, as shown, *e.g.*, in Figure 5H. *See, e.g.,* EX1005 Figs.5F-5H, 7:21-30; EX2010 81:5-18 ("Q. Okay. So can you point me in Grill to where it shows – it shows a three-dimensional view? A. Well…So there is no figure, there's no depiction of that direction…"). Notwithstanding that Grill is devoid of a three-dimensional view, Dr. Smith asserts that such a three-dimensional view "is what's understood in the description." EX2010 81:5-18. I disagree with Dr. Smith. A person of ordinary skill in the art would have understood that Grill's dual-relief cavity is in a direction that is across the width of the wiring trench rather than the length of the wire (*e.g.*, into the page in Fig. 5H). Contrary to Dr. Smith's unfounded argument, Grill's dual-relief patterns are intended to enable precise placement of vias within a wire trench's width—not length. EX1005 2:64-3:1. Grill's dual-hard mask system facilitates rework (*e.g.*, to complete "lithographic misalignment" between via and

wiring patterns) in a cross-sectional direction across the width of a wiring trench—not in a direction along a length of the wiring trench. EX1005 2:64-3:1.

141. Grill is concerned with the sizing of critical dimensions such as wire dimensions and via dimensions. Petitioner's expert Dr. Smith has admitted this as well. EX2010 13:15-14:20 ("A…critical dimension control is the ability to maintain a given…line width or space width to—a specified dimension…"), 18:8-20, 19:14-20:7 ("…it becomes difficult to control the dimension of [Grill's] via…"). Dr. Smith has further confirmed that critical dimension control is important to integration density (*e.g.*, "density of circuit pattern features"). EX2010 13:7-14:3, 14:12-20 ("Without…good control over things like critical dimension…increasing integration density becomes difficult"). Grill further confirms that a wiring dimension and a via dimension are important features in its patterns. EX1005 5:18-22 ("Sidewalls 30 of dielectric 12 are clearly undercut. Such a result may not be a problem when the ***dimensions of said second [wiring level] pattern substantially exceed the dimensions of the first [via level] pattern***, since the undercut regions would be etched anyway.") (emphasis added), 4:34-35, 4:51-52.

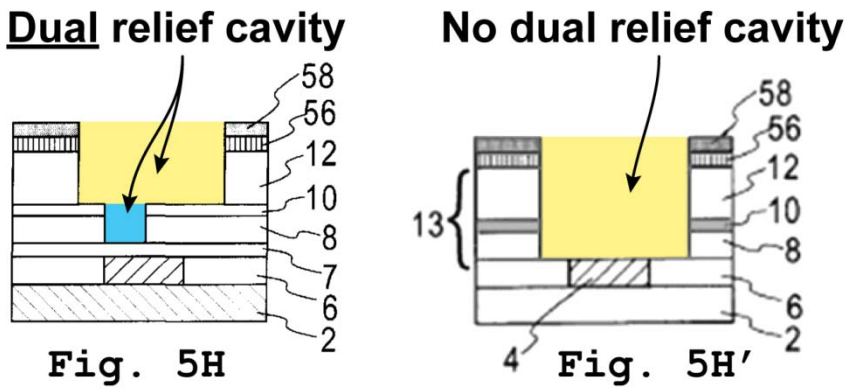
142. A person of ordinary skill in the art would have understood that the critical dimensions in Grill include the width of the wiring trench (*e.g.*, within layer 12 shown above in Figure 5H), and the width of the via (*e.g.*, within layer 8

shown above in Figure 5H), because the width of the wiring trench and the width of the via affect Grill's ability to increase integration density (*e.g.,* "density of circuit patterns"). EX2010 13:7-14:3, 14:12-20. However, a person of ordinary skill in the art would not have understood a length of a wire (*e.g.*, into the page of Figure 5H), would be a critical dimension because the length of the wire does not affect the packing or density of wires. Thus, a person of ordinary skill in the art would have understood Grill's dual-relief pattern and dual-relief cavities in the context of Grill's cross-sections across a wiring trench, that illustrate the critical dimensions of wiring trench width and via width.

143. The dual-relief pattern of Grill enables control of a via pattern dimension independently from an overlying wiring pattern dimension, and thereby facilitates precise placement of a via pattern over an underlying wider wiring pattern. EX1005 5:24-33, 7:16-29. This facilitates repeatable and controllable contact between a via pattern and an underlying wire or via. Grill confirms that in "the general category of dual relief patterns," "all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern." EX1005 7:26-30. The use of a smaller via pattern, combined with Grill's dual-hard mask system, which permits rework of photoresist patterns, facilitates precise placement of the via over an underlying wire. For example, if a via patterned photoresist is misaligned to an underlying metal wire and a wire trench hard mask

pattern, the via patterned photoresist may be removed and re-deposited until the via is positioned on top of the underlying metal wire, and at an appropriate location within the wire trench.

144. The modification of Grill proposed by Petitioner would eliminate the dual-relief patterns and dual-relief cavities of Grill. For example, as confirmed by Petitioner's expert, Figure 5H of Grill, reproduced below, illustrates a dual-relief cavity. EX2010 82:17-20 ("Q…does 5H show a dual relief cavity? A…Well, yes,"). However, Figure 5H', also reproduced below and which illustrates Petitioner's proposed modification of Grill by Aoyama, does not show a dual-relief cavity. This is demonstrated by the absence of a via (*e.g.*, within layer 8) that has a different dimension than a wire (*e.g.*, within layer 12). Petitioner's proposed elimination of Grill's "dual relief pattern" impedes Grill's "critical dimension" control over via dimensions and placement of the via over the underlying metal (*e.g.*, conductive via 4) and frustrates Grill's ability to achieve higher integration density of wire lines. EX1005 Abstract, 1:12-15, 2:41-50, 7:16-29, 5:24-33; EX2010 13:15-14:20, 15:12-16:8, 20:8-20; EX1002 ¶¶47, 158.



145. To the extent that Dr. Smith now attempts to argue (which he did not in his July 11, 2016 declaration) that Grill teaches dual-relief patterns in a direction along a wiring trench (*e.g.*, into the page of Figure 5H), Grill does not disclose any such cross-sectional views in a direction along a length of wiring trench, as Dr. Smith has already admitted. EX2010 80:15-81:15 ("Q. Okay. So can you point me in Grill to where it shows – it shows a three-dimensional view? A. Well…So there is no figure, there's no depiction of that direction…"). Moreover, when Grill contrasts dimensions of a second pattern (*e.g.*, wiring pattern) that "substantially exceed the dimensions of the first pattern [*e.g.*, a via pattern]," it does so in the context of a cross-sectional view across the width of a wire. EX1005 Fig. 2D, 4:34-35, 4:51-52, 5:18-28.

146. Thus, in view of Grill's disclosure of cross-sectional views across a width of a wiring trench, Grill's exclusion of cross-sectional views along a length of a wiring trench, and Grill's discussions of contrasting critical dimensions in the context of a cross-section across a width of a wiring trench, a person of ordinary

skill in the art would have understood and interpreted Grill's dual-relief patterns in the context of a cross-section across the width of a wire, as illustrated in Grill's figures.

147. Thus, because Petitioner's proposed modification to Grill would eliminate Grill's use of dual-relief patterns to form dual-relief cavities (an intended purpose of Grill), Petitioner's proposed modification would render Grill inoperable for its intended purpose. Accordingly, a person of ordinary skill in the art would not have been motivated to modify Grill in the manner proposed by Petitioner. Additionally, a person of ordinary skill in the art would not have had a reasonable expectation that the proposed modification would have worked as intended to yield the claimed invention for the same reasons. Thus, it would not be obvious to a person of ordinary skill in the art to modify Grill in the manner proposed by Petitioner.

B. Petitioner's proposed modifications of Grill would eliminate Grill's control over its wiring dimensions

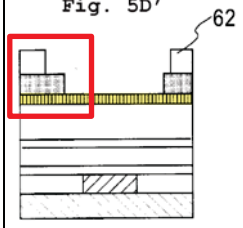
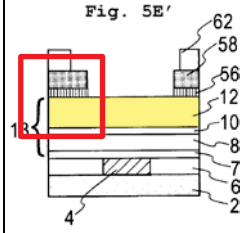
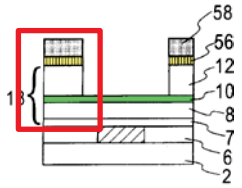
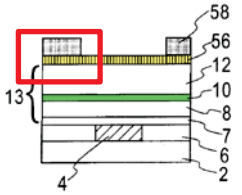
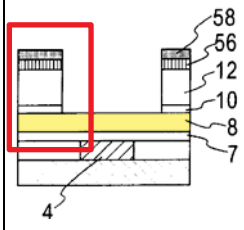
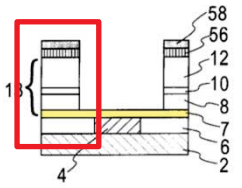
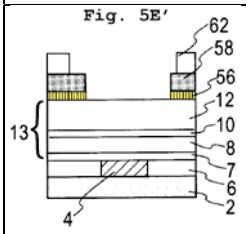
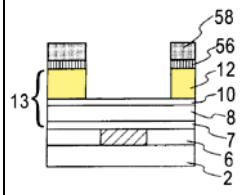
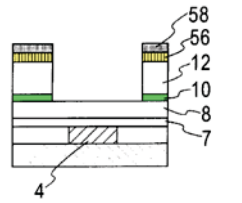
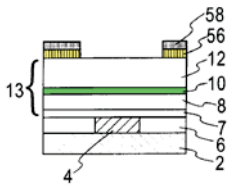
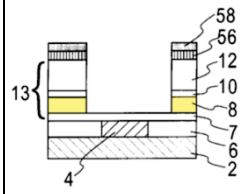
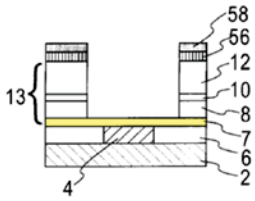
148. A person of ordinary skill in the art would have understood that control over wiring dimensions is part of Grill's principle of operation. As discussed above, Aoyama generally relates to techniques of buried wiring in semiconductors. EX1018 Abstract, 1:6-9. Petitioner relies on Aoyama's example 7 for forming a wider through-hole to modify Grill. Pet. at 49- (citing EX1018 3:6-38, 6:7-14, 15:48-16:30).

149. I understand that at Institution, the Board relied upon testimony of Petitioner's expert, Dr. Smith, that a person of ordinary skill in the art "would have found it obvious that combining Grill's two hard masks with Aoyama's widened via pattern would not require modification of the Grill process." EX1002 ¶0165. Dr. Smith also asserted that "[n]othing about the width of the via pattern in *Aoyama* affects the dual-hard mask structure of *Grill*." *See* Pet. at 49 (citing Dr. Smith's unsupported testimony at EX1002 ¶0165). However, these mischaracterizations by Petitioner and Dr. Smith ignore detrimental effects of Aoyama's wider via hole pattern on Grill's dual-mask system that would undermine Grill's principle of operation of control over critical dimensions of wires, thereby resulting in a wider wiring pattern over a via hole.

150. As confirmed by Petitioner's expert, one of Grill's objectives is the control of critical dimensions. EX2010 13:15-14:20, 18:8-20. These critical dimensions include the dimensions of a wire trench. EX1005 Fig. 2D, 4:34-35, 4:51-52, 5:18-28.

151. As acknowledged by Petitioner, Grill describes using two hard masks to complete lithographic alignment on the hard masks before transferring the pattern into thin films. *See* Pet. at 46; EX1002 ¶[0158]. In Petitioner's proposed modification of Grill, illustrated by Petitioner's Figures 5D'-5G' and 5F''-5G'', and modified figures 5H'-layer, all of which are annotated below, Grill's upper

hard mask 58 must persist through at least five etch steps: (1) etching through layer 56, (2) etching through layer 12, (3) etching through layer 10 and layer 56, (4) etching through layer 8, and (5) etching through layer 7.

Layer 56 etch (EX1005 7:57-61; Pet. 59-61)	**Layer 12 etch (EX1005 7:62-64; Pet. 61-63)**	**Layers 10/56 etch (EX1005 7:67-8:2; Pet. 63-65)**	**Layer 8 etch (EX1005 8:2-5; Pet. 65-67)**	**Layer 7 etch (EX1005 8:5-8)**
Fig. 5D′ 	Fig. 5E′ 	Fig. 5F′  Fig. 5F″ 	Fig. 5G′ 	Fig. 5H′ – layer 
Fig. 5E′ 	Fig. 5F′ 	Fig. 5G′  Fig. 5G″ 	Fig. 5H′ – layer 	Fig. 5H′ – layer 

152. But exposing Grill's upper hard mask 58 to these etch steps prematurely degrades Grill's upper hard mask 58, causing loss of control over the dimension of the wire trench over the via hole.

153. This loss of control over the dimension of the wire trench undermines a principle of operation of Grill's entire process (controlling critical dimension of a wire), and requires redesigning of Grill's system in a manner not contemplated by Petitioner—demonstrating that Petitioner has failed to submit evidence meeting its burden to show by a preponderance of the evidence that a person of ordinary skill in the art would have been motivated to combine the references or had a reasonable expectation of success.

154. Grill uses several hard mask layers including an upper hard mask layer 58 (*e.g.,* composed of silicon oxide), and a lower hard mask layer 56 (*e.g.*, composed of silicon nitride). EX1005 7:35-38. Grill acknowledges that these hard mask layers have different etch rates. EX1005 7:33-35. This is confirmed by references that also describe silicon oxide as etching at a faster rate than silicon nitride—meaning silicon oxide would degrade when both silicon oxide and silicon nitride films are exposed during an etch of silicon nitride. EX2020 at 555-556.

155. Although Grill states that the lower hard mask 56 and upper hard mask layer 58 are preferably formed from "different materials which have different etch properties from each other," a person of ordinary skill in the art would have

understood from Grill's specification and drawings that an etch of lower hard mask 56 would degrade any exposed portions of upper hard mask 58. EX1005 7:33-35. For example, Grill states that lower hard mask 56 may be made of silicon nitride and upper hard mask 58 may be formed from silicon oxide. EX1005 7:34-39.[10] A person of ordinary skill in the art would have understood that silicon oxide etches at a faster rate than silicon nitride when both films are exposed to a silicon nitride etching process. For example, silicon oxide may etch at rate that is at least 2-3 times as fast, and from about 7 to 13 times as fast, depending on the type of silicon oxide film, type of silicon nitride film and etch conditions. EX2020 at 555-556; EX2014 at Fig. 2. Any similar situation wherein the upper hard mask etches more

[10] Grill provides a list of other materials, but does not provide any suggestion on how to use those materials between the lower hard mask 56 and upper hard mask 58, and the Petition and accompanying Smith declaration made no suggestion that other materials should be used. EX1005 7:35-42. Grill also describes using an optional dielectric passivation/adhesion layer 7 and an optional dielectric etch stop layer 10. EX1005 4:1-5. Grill is silent as to the composition of layer 7 and discloses that the optional dielectric etch stop layer 10 may be a silicon containing compound, such as SiO_2, Si_3N_4, SiO_xN_y, SiCOH compounds, silicon-containing DLC (SiDLC). EX1005 4:5-11.

quickly than the lower hard mask during the lower hard mask patterning, results in a substantially similar problem. On the other hand, a lower hard mask that etches faster than the upper hard mask, creates difficulty for control of patterns. That is partly why it is more common to use photoresist on a hard mask.

156. Thus, under Petitioner's proposed modification to use Aoyama's wider through hole pattern 62, the upper hard mask 58 would be exposed to a silicon nitride etch process during etching of lower hard mask 56 in step Fig. 5E'. A person of ordinary skill would recognize that because silicon oxide etches at a faster rate than silicon nitride, such exposure of upper hard mask 58 (*e.g.*, composed of silicon oxide) to a dry etch process of lower hard mask 56 (*e.g.*, composed of silicon nitride), as shown in Petitioner's Figure 5D', would degrade the exposed portions of upper hard mask 58. This is confirmed by Figures 5F and 5G of Grill, which illustrate that when etch conditions are set to remove exposed portions of lower hard mask layer 56 and optional etch stop 10 to form the structure of Fig. 5G, the upper hard mask layer 58, despite having a different etch selectivity from lower hard mask layer 56, is substantially thinned. EX1005 Figs. 5F-5G, 7:64-8:2.[11] Indeed, the degradation of Grill's upper hard mask 58 during

[11] I understand that Petitioner's expert Dr. Smith has opined that the figures of Grill are not to scale. EX2010 at 88:8-12. However, the particular measurements

the etch of lower hard mask 56 is why Grill described protecting upper hard mask 58 with resist layer 62 while etching lower hard mask 56 in Figures 5D and 5E. EX1005 Figs. 5D-5E, 7:51-61.

157. Thus, modifying Grill's second resist layer 62 to use Aoyama's wider via hole pattern in the manner proposed by Petitioner, which exposes Grill's upper hard mask 58, would also degrade the exposed portions of the upper hard mask 58. This degradation is illustrated below, and is contrasted with Petitioner's inaccurate figures.

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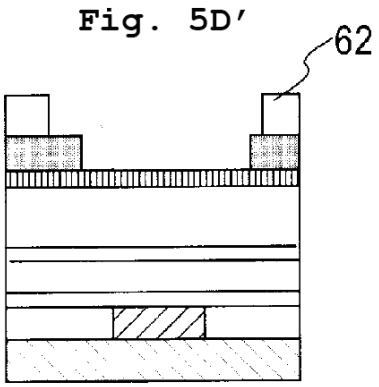
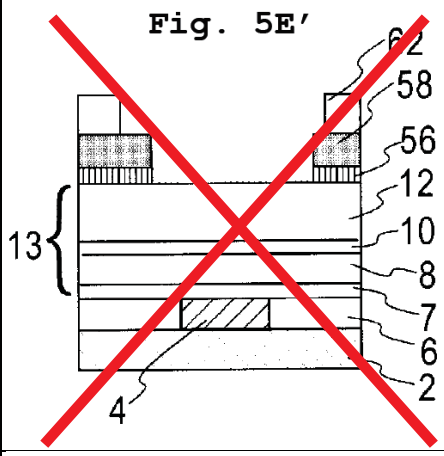
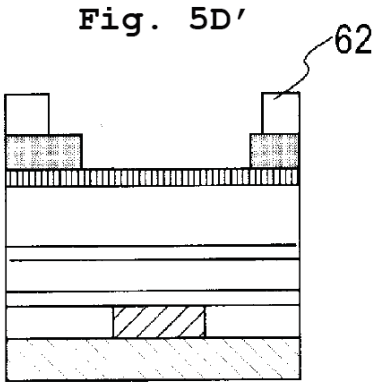
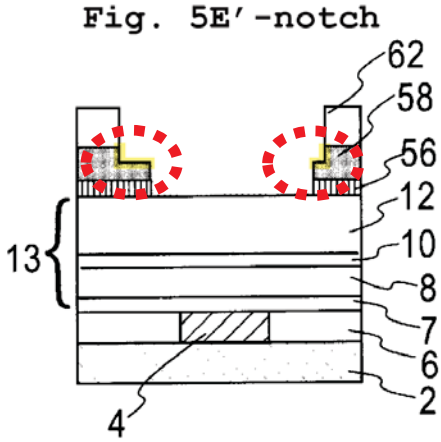
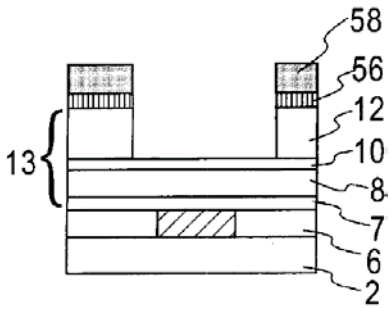
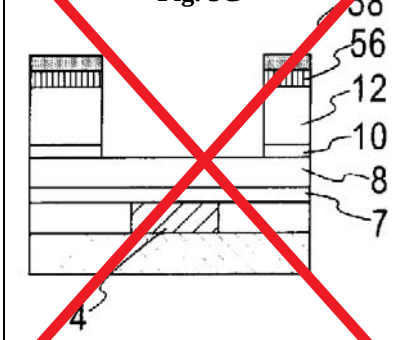
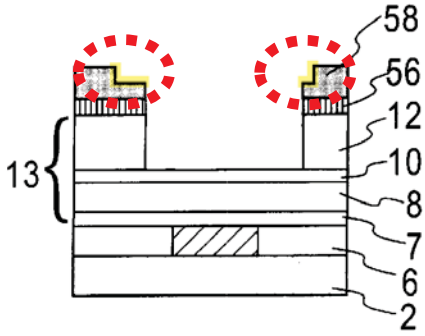
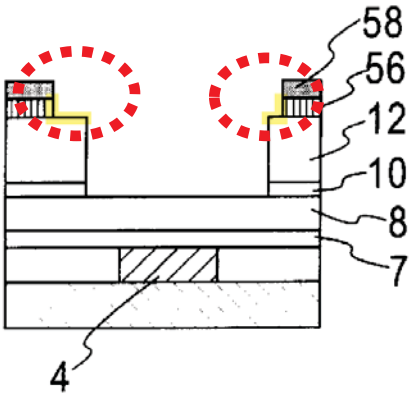
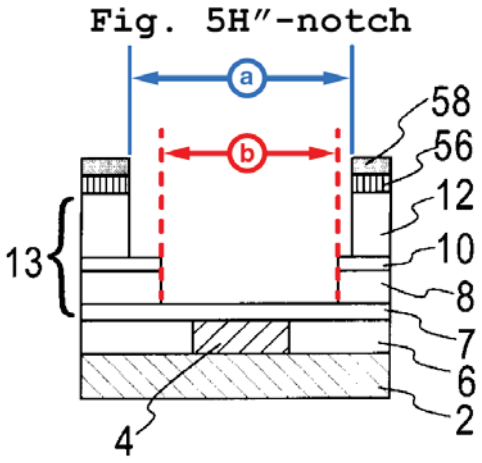
of the Figures of Grill are not the basis for a person of ordinary skill in the art's understanding that Grill's upper hard mask 58 would be prematurely degraded in Petitioner's proposed modification, but instead, Grill's figures (which clearly illustrate the positioning of individual layers) provide confirmation of this understanding.

	Before Etch of layer 56	After Etch of layer 56
Petitioner's Inaccurate Figures		
Damage to Exposed portions of Grill's Hard Mask layer 58		

158. The premature thinning of Grill's upper hard mask 58 in the process of initially etching layer 56 illustrated above in Fig. 5D' and Patent Owner's modified Fig. 5E'-notch would render it inoperable for the subsequent etching of layers 10 and 56 illustrated below in Patent Owner's modified Fig. 5F'-notch and Fig. 5G'-notch. The premature thinning of hard mask 58 would result in the complete etching of lower hard mask 56 during the etching of layer 10. This would leave underlying layer 12 exposed during a subsequent etch of layer 8 as illustrated below in Figure 5'-notch.

	Before Etch of layer 10	After Etch of layer 10
Petitioner's Inaccurate Figures	Fig. 5F′  	Fig. 5G' 
Damage to Exposed portions of Grill's Hard Mask layer 58.	Fig. 5F′-notch  	Fig. 5G′-notch 

159. The result is a width of a wiring groove (annotated as "a" below) that is wider than a designed width (annotated as "b" below) over a via hole, which eliminates Grill's ability to control for wire dimension, which is undesirable as it limits the density of wires that may be formed, and thus thwarts Grill's principle of operation.



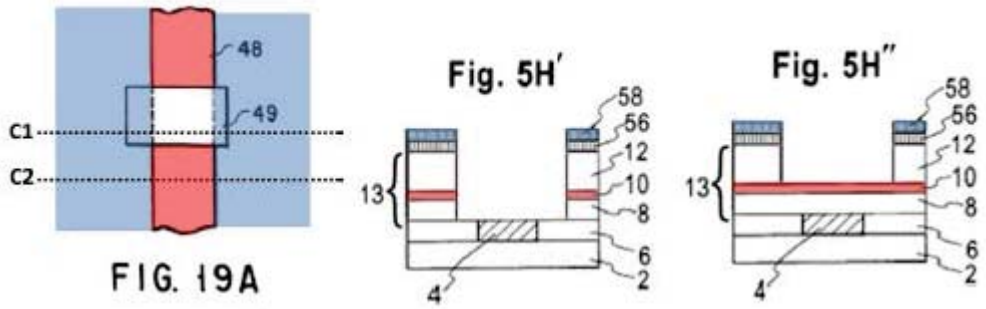
160. I understand that neither Petitioner nor Dr. Smith has argued that (1) a person of ordinary skill in the art would have understood this issue and further considered using a thicker upper hard mask layer 58 to compensate for the premature degradation of upper hard mask layer 58, or that (2) layer 10 is considered optional by Grill and a person of ordinary skill in the art would have considered excluding layer 10. Even if these arguments were allowed to be raised and considered despite not having been asserted in connection with the Petition, each of these arguments would require additional work and create problems that are not contemplated or addressed in the Petition or Dr. Smith's declaration, and thus these arguments could not be used to suggest that Petitioner has met its burden of demonstrating obviousness by a preponderance of the evidence.

161. For example, using a thicker upper hard mask film would introduce additional issues such as thicker resist over etched portions of the upper hard mask, which would require higher dose exposures that Grill disparages as causing loss in

critical dimension control. EX1005 5:28-33. A person of ordinary skill, as well as Dr. Smith, would have understood that widely varied exposure requirements between thicker resists over via holes, and shallower patterns would have created problems for dimensional control. Dr. Smith himself has published a book chapter entitled "Resist Processing" that cautions against the "adverse influence of overexposure" that can result in a "large amount of energy in shadow areas" that would degrade an intended pattern. EX2019 at pp.605-606. This passage is also present in an earlier edition of Dr. Smith's book published in 1998. EX2017 at 537-538. *See also* EX2016 at 229 ("The result of these effects is that the resist can be effectively underexposed where it is thicker and overexposed where it is thinner. This can result in linewidth variations, particularly where the photoresist features cross steps in the underlying structures.").

162. For example, excluding optional dielectric etch stop 10 would require a complete redesign of the process. A person of ordinary skill in the art would have understood that optional dielectric etch stop 10 is necessary in the context of Figures 5A-5F. It provides an endpoint to etching of dielectric 12 to form the wire pattern. Otherwise, without the etch stop there would be no way to definitively determine when to terminate the etching of the wiring groove pattern into dielectric layer 12. Instead, the process would need to guess at when the dielectric trench has been etched to a sufficient depth.

163. Petitioner's own modified Figures 5H' and 5H'', reproduced below, emphasize the important of dielectric etch stop layer 10 in the formation of wiring grooves. Without the dielectric etch stop layer 10, the end point of etching a wiring groove into layer 12, as illustrated in Petitioner's modified figure 5H'', would need to be approximated or guessed without any certainty or uniformity, which a person of ordinary skill would have understood to be unacceptable.



164. The Aoyama embodiment that Petitioner and Dr. Smith rely on includes etch stopper layer 45, which Petitioner and Dr. Smith never addressed in the Petition or accompanying declarations, but which Dr. Smith acknowledged at deposition is "an etch stopper made of carbon" and which is exposed to a photoresist removal process. *See* EX2010 106:12-20; EX1018 16:3-5. Therefore, a person of ordinary skill in the art would not have been motivated to modify Grill to use Aoyama's wider via hole photoresist pattern because doing so would expose upper hard mask to etch processes that would prematurely degrade its thickness resulting in a wider wire pattern over a via hole. This degradation of Grill's upper hard mask 58 eliminates Grill's principle of operation: the ability to control critical

dimensions of its wire width over a contact hole. Thus because Petitioner's proposed modification changes a principle of operation of Grill, a person of ordinary skill would not have been motivated to modify Grill in the manner proposed by Petitioner.

165. Additionally, a person of ordinary skill would not arbitrarily increase the upper hard mask layer thickness because doing so would result in a thicker resist within the upper hard mask cavity which Grill has criticized as being detrimental to control of critical dimensions, as discussed above, due to overexposure of thinner regions. EX2010 106:6-8, 107:11-109:3; EX1005 Fig. 2A, 5:28-32; EX1018 Fig. 18B. Because Grill teaches away from using thicker resists, a person of ordinary skill would not have found it obvious to arbitrarily increase the thickness of the upper hard mask.

166. Moreover, for at least these reasons, a person of ordinary skill in the art would not have had a reasonable expectation that the proposed modification (*e.g.*, using Aoyama's wider contact hole pattern even using a thicker upper hard mask layer), would have worked as intended to yield the claimed invention.

167. Thus, it would not be obvious to a person of ordinary skill in the art to modify Grill in the manner proposed by Petitioner.

C. Grill teaches away from incorporating Aoyama's disclosures

168. As further discussed below, Grill expressly teaches away from using systems that (1) expose underlying organic layers to photoresist stripping processes, and (2) that use photoresist patterns that are "thicker over via areas." EX1005 2:26-32, 5:28-33.

169. Aoyama was filed in October 28, 1994, and describes low dielectric constant materials such as fluorine doped silicon oxide materials. EX1018 5:22-28, 6:27-35. Because Aoyama was directed to fluorine doped oxide materials, Aoyama describes the use of carbon etch stopper layers, which could be removed by oxygen based plasma techniques without damaging underlying fluorinated oxide dielectrics. EX1018 15:60-63.

170. Grill was filed on July 30, 1998, after Aoyama, and is directed to solutions that are entirely different from Aoyama's approach. Grill describes using "carbon-based materials" as low dielectric constant materials. EX1005 4:5-9. Grill also cautions against using oxygen plasma based systems and wet chemical processes to remove photoresist when portions of carbon-based dielectric layers (*e.g.*, layer 8) are exposed. EX1005 2:26-32. Grill expresses concerns (*e.g.*, protecting carbon based layers from oxygen plasma based and wet chemical process based photoresist removal steps).

1. Grill teaches away from incorporating processes that expose carbon based compounds to wet etching or photoresist stripping, and ashing steps

171. I understand that at Institution, the Board relied upon Petitioner's erroneous suggestion that Aoyama addresses the problem of misalignment described in reference to Figures 5A-5D by ***only*** "using a resist pattern having an opening that is wider than the wiring groove." *See* ID at 40; Pet. at 28. Petitioner has improperly ignored that part of Aoyama's misalignment solution is its use of carbon etch stopper film 45.[12]

172. Without the carbon etch stopper film 45, Aoyama would end up with a result that is even worse than the problem it was trying to solve. Instead of a wider wiring groove at the through-hole only during instances of misalignment, Aoyama would always end up with a wider wiring groove at the through-hole, regardless of misalignment. This is illustrated by the annotated figures below,

[12] Aoyama discloses the use of a "second stopper film 45" and refers only to carbon as the material for such a film. EX1018 15:60-63. Petitioner's expert Dr. Smith confirmed at deposition that the stopper film 45 is carbon. 2010 106:12-20 ("it [stopper film 45] is an etch stopper made of carbon that functions as an etch stopper when doing the wiring etch.").

which show a modified version of Aoyama's Figs. 18B-18C without carbon etch stopper film 45.

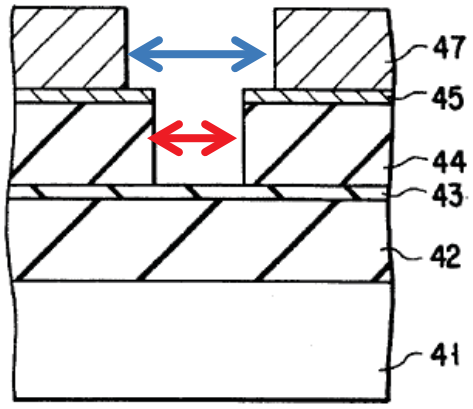


Fig. 18B

Aoyama's Figure 18B

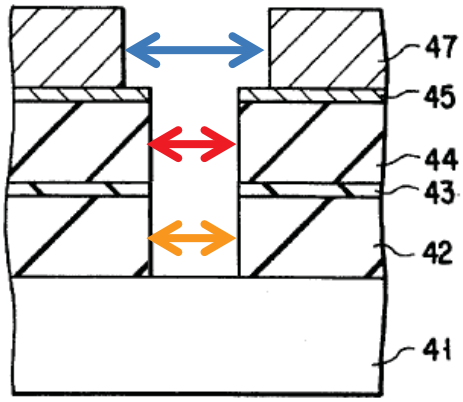


Fig. 18B-etched

Aoyama's Figure 18B result

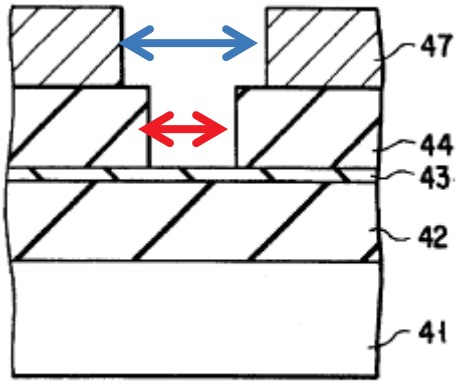


Fig. 18B'

Aoyama's Figure 18B <u>without</u> an etch stopper 45

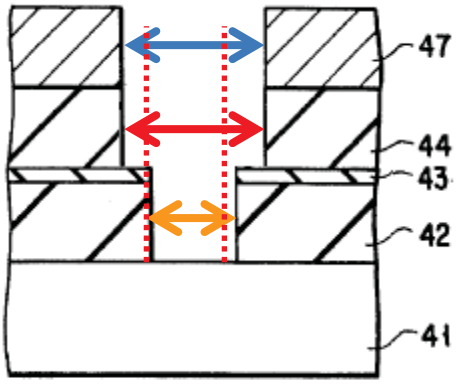


Fig. 18B'-etched

Aoyama's Figure 18B result <u>without</u> etch stopper 45

173. In Aoyama, "the second interlayer insulating film 44 below the stopper film 45 **is not etched by virtue of the second stopper film 45.** Accordingly, as shown in Fig. 19B, a through-hole 50 having the same width as the wiring groove 48 can be formed." EX1018 16:9-16. However, when Aoyama's

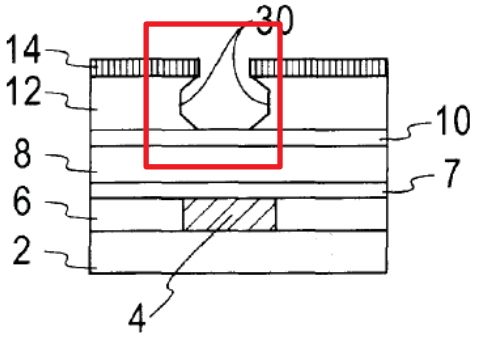
carbon etch stopper film 45 is removed, it no longer protects layer 44 from etching as illustrated above. Without the etch stopper film to protect layer 44, as shown in Fig. 18B', layer 44 would be etched with layer 47's wider pattern, thereby resulting in a wider wiring groove as compared to the use of an etch stopper 45 as shown in Fig. 18B-etched.

174. Thus, Petitioner is incorrect in attributing Aoyama's solution solely to the wider via opening pattern, and thereby has mischaracterized Aoyama and what a person of ordinary skill in the art would have understood and considered when evaluating whether to combine Grill and Aoyama. Instead, a person of ordinary skill in the art would have understood that it would not be possible to modify Grill by combining it with Aoyama's wider via hole pattern (and certainly would not have had a reasonable expectation of success) without also including Aoyama's carbon etch stopper film 45; otherwise a wider wiring pattern over the via hole would result. But a person of ordinary skill in the art, starting from Grill's criticism (discussed below) against exposing carbon based layers to stripping processes, would have recognized that applying Aoyama's wider via hole patterns and carbon etch stopper film 45 to Grill would interfere with Grill's dual-hard mask solution of controlling critical dimensions—rendering Grill unsatisfactory for its intended purpose. To the extent that the carbon etch stopper film 45 is not used by Aoyama, and Aoyama allows the use of ashing with O_2 plasma instead of wet

etching, Grill also teaches against ashing. Grill teaches that ashing damages underlying structures if they are not protected by the hard mask, such as after it is perforated by patterning. (*See* EX1005 4:35-40.) Thus, Grill teaches against an element necessary in the proposed combination.

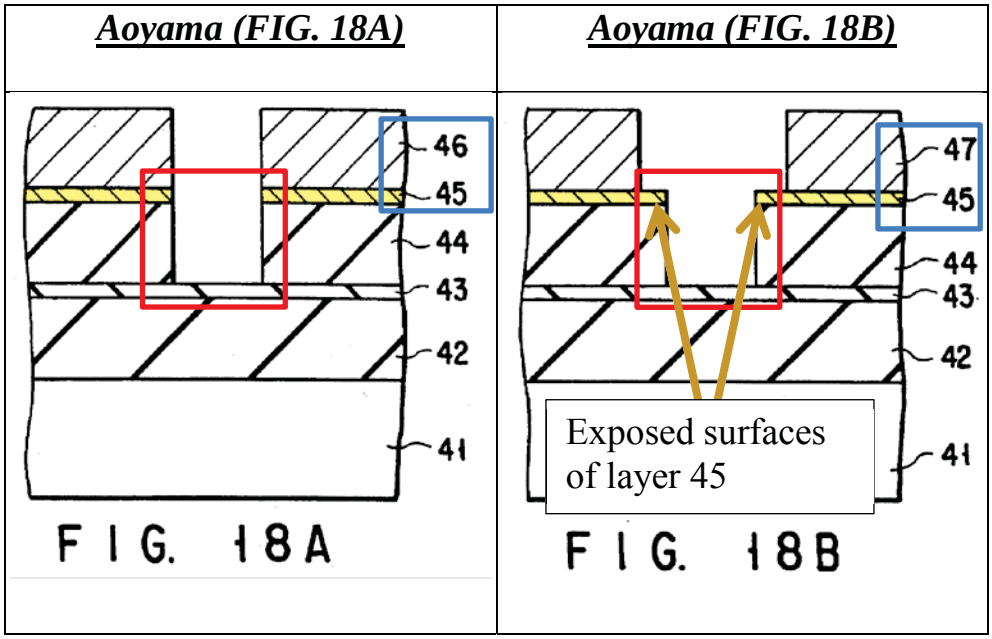
175. Grill expressly identified a known rework problem where carbon-based dielectrics are damaged by exposure to photoresist removal processes such as ashing and wet chemical etching. *See* EX1005 2:26-32, 5:9-28. An example of damage caused to exposed surfaces 30 of the carbon-based dielectric 12 by the photoresist removal process is illustrated in Fig. 2C, reproduced below. *See* EX1005 4:5-8, 14-21, Fig. 2C.

Grill (FIG. 2C)



176. As discussed above, Aoyama's example 7 relied on by Petitioner (Pet. at 34-36, 52-56) shows that using a wider through-hole in resist pattern 47 requires a carbon etch stopper layer 45 to protect insulating layer 44, when etching layers

43 and 42. *See* EX1018 15:60-63, 16:3-14. In Aoyama's example 7, the carbon etch stopper layer 45 is directly in contact with resist pattern 46 as illustrated in Fig. 18A, shown below, and resist pattern 47 as illustrated in Fig. 18B, shown below. *See* EX1018 15:64-16:9.



177. The exposed surfaces of carbon-based layer 45 (annotated above) function as an "etching stopper" and are critical in Aoyama to protect portions of layer 44 that are not covered by resist pattern 47 during a subsequent etch of layers 43 and 42. *Id.* 15:60-63, 16:9-17.

178. But Grill teaches that carbon-based layers should not be used because each photoresist removal step by ashing or wet etching degrades the carbon-based layers. EX1005 5:13-17; EX1018 16:12-14. When combined with Grill, a carbon based layer 45 as required for the teachings in Aoyama would be subjected to at

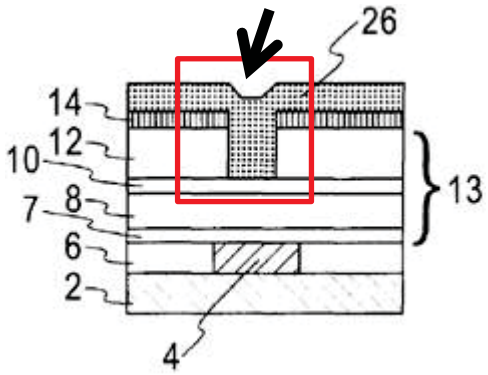
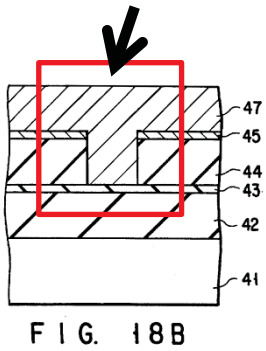
least one photoresist removal step to remove resist pattern 46 and at least one photoresist removal step each time that rework of 47 has to be completed—causing layer 45 to degrade and preventing it from protecting underlying layers (as needed for Aoyama's teachings to be operative).

179. Neither Petitioner nor Dr. Smith have addressed why a person of ordinary skill considering Grill would ignore this problem of Aoyama's process and combine the two references' teachings, nor how a person of ordinay skill in the art could overcome this problem. *See* Pet. at 56. Instead of a complementary solution to a common problem with Grill, as Petitioner argues as the sole rationale for combining them, this wider through hole over and carbon etch stopper aspect of Aoyama is—according to Grill's own teachings—detrimental to Grill's approach. Thus, a person of ordinary skill would not have found it obvious to combine Grill and Aoyama because Grill teaches away from the combination with Aoyama suggested by Petitioner and would not have had a reasonable expectation of success in combining the references as proposed by Petitioner.

2. Grill teaches away from incorporating processes that have a thick resist over via holes

180. Grill expressly criticizes techniques resulting in a resist layer that is thicker over via areas as problematic because such thicker resist requires "higher dose exposures, with consequent loss in CD [critical dimension] control." *See* EX1005 5:29-35. Grill illustrates this problem in Fig. 2A, annotated below. But

tellingly, this problem of thicker resist over via areas identified in Grill, which aggravates misalignment problems by frustrating control of critical dimensions, is actually made worse the teachings of Aoyama that Petitioner proposes to borrow—including in Aoyama's example 7. For example, in a modified Fig. 18B of Aoyama, annotated as Figure 18B-modified below, and as admitted by Dr. Smith (the profile of photoresist layer 47 in Aoyama's Fig. 18B would be "thicker over the…[via] hole," and with "some degree of conformity" (EX2010 108:18-109:2)), the thickness of the deposited resist layer 47, prior to exposure and developing, would be thicker over the intended via than over second insulating film 44.

Grill (FIG. 2A)	***Aoyama (FIG. 18B-modified)***
	 FIG. 18B

181. A person of ordinary skill, as well as Petitioner's expert, Dr. Smith, would have understood that widely varied exposure requirements between thicker resists over via holes, and shallower patterns would have created problems for dimensional control. Consistent with Grill's criticism of thicker resists over via

holes due to issues with exposure, Petitioner's expert Dr. Smith has also published a book chapter entitled "Resist Processing" that cautions against the "adverse influence of overexposure" that can result in a "large amount of energy in shadow areas" that would degrade an intended pattern. EX2019 at 605-606; *see also* EX2017 at 537-538. Thus, even Petitioner's expert Dr. Smith recognizes that having resist patterns that are too thick over via holes can be problematic because they cause thinner resist patterns to be overexposed. Further, this is consistent with Silicon VLSI Technology, by Plummer, Deal and Griffin as discussed above. EX2016 at 229.

182. While Petitioner flatly asserted that Aoyama does not detract from Grill's teachings (*e.g.*, Pet. at 56 ("Nothing about the width of the via pattern in Aoyama affects the dual-hard mask structure of Grill, and nothing about the dual-hard mask structure of Grill affects the width of the via pattern in Aoyama.")), Petitioner never attempted to address this warning in Grill against the very result that Petitioner's proposed borrowing from Aoyama would cause—*i.e.*, underexposure of thicker photo resist patterns over vias or overexposure of thinner portions of resist. This problem raised by Grill (and consistent with Petitioner's expert's own publication) would defeat Grill's approach to misalignment.

183. Thus, because Grill teaches away from aspects of the claimed invention required of Aoyama, a person of ordinary skill in the art would not have

been motivated to combine the references to arrive at the claimed invention, nor would a person of ordinary skill in the art have expected the combination to work as intended. Thus, the person of ordinary skill in the art would not have found it obvious to combine Grill and Aoyama in the manner proposed by Petitioner.

184. For at least the reasons discussed above, in my opinion, a person of ordinary skill in the art would not have found it obvious to combine Grill and Aoyama in the manner proposed by Petitioner and Dr. Smith.

X. Conclusion

185. For the reasons above, my opinion is that Grill in view of Aoyama does not render obvious claims 13 and 15 of the '696 Patent. I reserve the right to supplement this Declaration to address any new claim constructions offered by Petitioner or provided by the Board. I also reserve the right to supplement this Declaration insofar as Dr. Smith or Petitioner are permitted to supplement the record with any additional opinions or arguments.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on this 14th day of April, 2017

Alexander D. Glew

Date: 2017.04.14 18:04:16 -07'00'

Alexander Glew, Ph.D.

At: Mountain View, CA

Attachment A

Curriculum Vitae

Alexander D. Glew, Ph.D., P.E.

Expertise

• **Materials Science Engineering, Thin Films & Equipment, Semiconductor**	• **Mechanical Engineering**
• Semiconductor Equipment and processing: CVD, Etch, RIE, CMP, SOD, EPI, MBE, RTP, and others	• Licensed Professional Engineer (PE) in California, Mechanical Engineering
• Chemical vapor deposition (CVD): plasma, ICP, thermal, MOCVD, LPCVD and others	• CAD, drafting standards, and related.
• Thin film processing for solar, LED, and optics.	• Computation Fluid Dynamics (CFD) Fluid flow, radiation analysis
• Diamond Like Carbon (DLC), Fluorinated amorphous carbon (FLAC)	• Finite Element Analysis (FEA), multi-physics and event simulation
• Dielectric Deposition: Low k dielectric films, SiO2 (glass), fluorinated glass (FSG), BPSG, USG	• Product Design & Testing
• Excimer Laser Sources	• Project management and turnaround
• Laboratory analysis: SEM, TEM, FTIR, SIMS, AES, and others.	• Ultra High Purity Gas and Chemical Delivery Systems
• Materials processing	• Piping, valve, and chemical systems
• Metal deposition and sputtering (PVD)	• Metrology: Flow, pressure, optical properties, thin film properties …
• Plasma and Thermal Processes	• Reverse Engineering
• Thin Film Characterization: stress, strain, thickness, optical and dielectric properties, structure, composition …	• Safety analysis, interlocks, failure mode effects, standards and code analysis.

Curriculum Vitae

Employment History

From:	1997	**Glew Engineering Consulting, Inc.**
To:	Present	Mountain View, California
	Position:	President
		Clients include companies from semiconductor equipment, plasma generation, vacuum systems, fluid delivery systems, flow and pressure component suppliers, laser manufacturers, consumer electronics, industrial electronics, and others. Consulting work includes thin film characterization, process development, project turn-around/rescue, gas flow and vacuum metrology, design of experiments, corrosive gas applications, finite element analysis and related market analysis.
From:	Aug 1987	**Applied Materials, Inc.**
To:	Jan 1997	Santa Clara, California
	Titles	Engineering Manager, Core-Technologist
	Project Mgr. Jan 1996 to Jan 1997	• Sat on corporate engineering/technology (ET) council, one of 15 council members. Responsible for corporate direction in gas delivery technology for all divisions, including CVD, EPI, PVD, RTP, etch, thermal and others. Also, qualified gas and vacuum component selections. Consulted with all divisions on gas and vacuum systems, liquid source delivery systems, components, and supplier selections. • Received patent for improved tungsten (W) CVD deposition. • Successfully proposed and executed a project that SEMATECH S100 funded. The goal was to develop industry methods to determine the effects of trace chemicals on semiconductor processing and equipment reliability. This resulted in two SEMATECH Technology Transfers listed below.
	CVD Supplier Quality Engineering Manager	First, ppb levels of impurities were introduced into both a Tungsten CVD deposition process and an aluminum etching process. The effect on particle generation, deposition rate, uniformity, selectivity and incorporation into the film were examined. This work resulted in a 30% increase in deposition rate. Similarly, ppb-ppm levels of impurities were introduced into HBr gas systems and accelerated lifetime tests were conducted at three sites across the country. Measured by quadrapole mass spectrometry gas composition in situ of Tungsten CVD and Al Etch process.
	Core Technologist	• Responsible for gas, vacuum and chemical components evaluation, testing and supplier quality management. Managed an engineering group that tested and recommended gas, vacuum and chemical components for the CVD division, and developed
	CVD Engineering Manager	

process controls at suppliers. Supervised laboratory and trained individuals to develop specialized testing capabilities to characterize gas delivery and vacuum components. Also supported Etch, PVD and other divisions with common suppliers including vacuum pumps, vacuum transducers, flow controllers, valves and similar.

- Managed group of engineers and support personnel who developed gas panels and liquid source delivery systems for dielectric deposition. Delivered TEOS, TMP, TMB and many other organometallic precursors for SG, BPSG dielectric deposition. Developed organometallic CVD systems extensively.

Systems Engineer

Designed multiple liquid source delivery systems for organometallic chemical precursors, i.e. bubblers, boilers, injectors.

- Managed CVD division design support group: CAD designers, drafters and CAD systems for division. Brought in first 3D CAD systems. Brought in first FEA program.
- Established and managed the customer engineering special group for the CVD division, which engineered all equipment modifications to meet customer specifications. These modifications included changes across the entire system, including process chambers, vacuum systems, gas delivery, power distribution, safety and robotics.
- Worked on the development and release of the landmark product, Precision 5000 CVD, one of which is now in the Smithsonian Institute. This was the first cluster tool for semiconductor manufacturing.
- Developed dielectric layers of silicon dioxide (glass or USG), boron phosphorous silicon glass (BPSG), phosphorous silicon glass (PSG), nitride, oxy-nitride, and others.
- Responsible for flow and vacuum equipment suppliers for company including MFC, valves, mechanical vacuum pumps, cryo-pumps, dry pumps, and others. Supported multiple divisions on these matters.

Doctoral Dissertation:

From: 1996
To: 2002

Stanford University
Stanford, California
Ph.D.
Completed a dissertation in the department of Materials Science & Engineering leading to the Ph.D. degree.
Research includes:

- Plasma Deposition of Diamond-Like Carbon and Fluorinated Amorphous Carbon and the Resultant Properties and Structure

- Characterized stress, strain and hardness of films. Related the stress energy state to the diamond like nature of the thin films.
- Investigation of deposition mechanism fluorinated amorphous carbon (FLAC) and diamond-like carbon (DLC), low k dielectric materials.
- Modeled and conducted experiments on mechanism of ion energy, momentum and flux dependence for FLAC and DLC film synthesis in radio-frequency plasma discharges, including competing mechanisms of sub-plantation, ion-peening, sputtering, and etching.
- Constructed and instrumented a multi-purpose processing chamber for CVD, etch, and sputtering with measurement capability.
- Fabricated MIS capacitors to investigate the dielectric properties of fluorinated amorphous carbon (FLAC). Performed all wafer processing to construct MIS capacitors, including lithography, etch, CVD and PVD.
- Conducted thin film analysis including UV absorption spectroscopy, spectral ellipsometry, multi incident angle ellipsometry, Fourier transform infrared spectroscopy, profilometry, nano-indentation, and gravimetric measurements.
- Modeled dielectric properties and dispersion relationship of fluorinated amorphous carbon (FLAC), and compared spectral ellipsometric measurements to results of electrical CV tests and thickness measurements by profilometry using MIS structures.

Consulting History (Partial)

From To:	2016 Ongoing	VWR Review of new semiconductor technologies for etching and particle reduction in semiconductor processing chambers.
From To:	2016 Ongoing	Confidential Client Reverse engineering of OLED display technology.
From To:	2016-2017	TDA Research Finite element analysis of effluent treatment system for power plant carbon reduction treatments.
From To:	2016 Ongoing	Champion Telecom Engineering support, Finite element analysis, and design of “Cell Towers on Wheels” (COWs). Multiple projects.

From	2016	CarbonTech
To:	Ongoing	Pursue UL listing for thin film carbon heaters. Help productize the technology. Review codes for domestic use.
From	2015	Phiston Engineering
To:	2016	Review ability of equipment to destroy flash memory. Generate report to submit to NSA.
From	2015	United States Air Force
To:	2015	Concluded
	Duties	Advanced semiconductor process equipment engineering for Air Force Laboratory.
From	2013	United States Department of Justice, Antitrust Division
To:	2014	
	Duties	Served as the expert for the DOJ in their investigation of the proposed merger between Applied Materials and Tokyo Electron.
From	2015	VADA
To:	Ongoing	
	Duties	Fluid analysis of venting device.
From	2014	Chemithon
To:	Completed	
	Duties	Finite element analysis (FEA) and computational fluid dynamics (CFD) analysis of thermal and stress analysis of large industrial sized heat exchangers. Redesign to meet structural and performance needs.
From	2013	Barrick Cortes Mines
To:	2013	
	Duties	Analysis of equipment using in mining operations.
From	2013	Life Technologies
To:	2013	
	Duties	Concept design for a portion of a medical device: centrifuge assembly for separation in PCR DNA application.
From	2012	Light failures
To:	2012	
	Duties	Reliability analysis of thermal issues causing light sealing failures for glass metal interface.
From	2012	Legion Industries

To:	2012	
	Duties	Review of electrical surge issues at Google campus.
From	Dec. 2011	CareFusion
To:	2012	
	Duties	Chemical compatibility/reliability analysis of medical device.
From	June 2011	Watlow
To:	2012	
	Duties	Heater and chuck assembly design for use in semiconductor processing.
From	June 2011	Limited Brands
To:	June 2012	
	Duties	Design review of prototype consumer electronics products. Perform engineering analysis of weaknesses and risks in product design.
From	April 2011	EFCI/Environmental Protection Agency
To:		
	Duties	Subject matter expert for green house gas emissions from the electronics industry.
From	June 2011	Intrimed
To:	Current	
	Duties	Consult for Exec. VP on thin film technology in medical devices.
From	April 2010	Zoll Circulation
To:	June 2010	
	Duties	Analysis of electrical contacts in a medical device, cardiac life support pump.
From:	June 2008	Teardown and analysis of IC packaging.
	Sept. 2008	
From	Oct 2008	VModa
To:	Feb 2009	
	Duties	Engineering analysis of headset/earbuds used for iPhone. Performed finite element analysis (FEA) of plug to determine why the plug/cable contacts were breaking. Reviewed designs of a number of competing earbuds, and other musical equipment plugs, and their respective designs for plug reliability improvements.
From	Sep 2008	Malema Sensor
To:	Oct 2008	
	Duties	Safety Analysis of Fluid dispense system for semiconductor equipment.

From To:	Dec 2007 Jan 2008	Damage analysis for insurance valuation.
	Duties	Analysis of damage to equipment from a chemical leak.
From: To:	Apr 2007 Oct 2008	Epicrew
	Duties	Finite element analysis of temperature distribution in process chamber, and leading to safety issues and analysis of emergency conditions in epitaxial equipment. Multi-physics transient radiation, conduction and convection analysis.
From: To:	Apr 2007 Oct 2007	Unicor
	Duties	Analysis by FEA and approval of automotive lifting devices as a licensed mechanical engineer.
From: To:	2007 2008	Altcatel
	Duties:	Consulting on semiconductor foundry processes, low-k spin on dielectrics, that lead to IC failures.
From: To:	2002 Present	Consulting with financial analysts on semiconductor industry through Gerson Lehrman Group.
	Duties:	Provided on the spot analysis of new technologies, companies, and products within the semiconductor and related industry.
From: To:	March 2004 2009	AIU (Now Chartis Insurance.) Hsinchu, Taiwan
	Duties:	Analysis of complete destruction of FAB due to facility design, equipment design, installation, process monitoring and control, etc. International Arbitration.
From: To:	June 2004 Nov 2004	Rosemont Process, Division of Emerson Electric, Inc. Minneapolis, MN.
	Duties:	Market analysis of process monitoring and control needs.
From: To:	Oct 2000 March 2001	Brooks Instrument, Division of Emerson Electric, Inc. Hattfield, PA, and Minneapolis, MN.
	Duties:	Market analysis of semiconductor equipment needs with respect to fluid handling components.
From:	Apr 2000	Lebar, Inc.

To	Oct 2000	Sunnyvale, CA
	Duties:	System design and fluid delivery system design for plasma based photoresist strip (photoresist removal).
From:	Dec 1999	High Speed Industries, Inc.
To	2000	Lake Elsinore, CA
	Duties:	Market analysis of semiconductor equipment needs with respect to fluid handling components.
From:	May 1999	Aeroquip (Division of Eaton Corp.) Ann Arbor, MI
	Duties:	Reviewed new product entry (semiconductor fluid handling) prior to product engineering.
From:	Sep 1999	Steag RTP Systems, Inc.
To:	Nov 1999	San Jose, CA.
	Duties:	Materials evaluation and testing for metallic reduction in thermal SiO_2 films produced by rapid thermal processing (RTP) with steam.
From:	Sep 1998	Cymer, Inc.
To:	Aug 1999	San Diego, CA
	Duties:	Project manager responsible for leading team through concept and feasibility studies for major product enhancement to Excimer laser used in deep ultraviolet lithography.
From:	Jan 1997	Millipore, Inc.
To:	Sep 1998	Rancho Bernardo, CA
	Duties:	• Established a metrology group responsible for vacuum and flow measurements. The metrology is used in the manufacture and service of instruments for semiconductor process equipment. Established statistical process control for production metrology equipment. Established statistical process control on factory floor. • Led development team for new mass flow control device.

Litigation Support Experience (recent)

Client	*Godo IP Bridge*
Case	Godo IP Bridge vs. Broadcom (Ropes and Gray)
Project	Three patents semiconductor processing and devices.
Dates	2015-2016.
Status	Ongoing.

Client	*Ricoh America Corp*
Case	Ricoh America Corp v. Round Rock Research LLC.
Project	Three INTER PARTES REVIEW at the USPTO. Patents semiconductor processing and devices.
Dates	2016.
Status	Declarations in IPR.

Client	*Elm 3DS Innovations*
Case	Elm v. Samsung Electronics, Hynix and Micron C.A. No. 14–cv-01430–LPS-CJB Multiple IPRs
Project	Patent infringement involving thinned and stacked wafers, low stress dielectric materials and other topics of IC memory.
Dates	2014 -

Client	Antitrust Division, US Department of Justice
Case	Proposed merger of Applied Materials and Tokyo Electron
Project	Served as technical expert/industry expert for US DOJ regarding proposed merger of the two largest semiconductor equipment companies.
Dates	2014 -2015

Client	*Semcon* (Russ, August & Kabat)
Case	Semcon v. Micron Inc. CASE NO. 12-532-RGA UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Project	Advanced process control and metrology in semiconductor processing patent case regard CMP.
Dates	2013
Status	Appealed.

Client	*Caterpillar Inc.* (Baker & Hostetler)
Case	Miller UK Limited v. Caterpillar Inc. CASE NO. 10-cv-3770 UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF ILLINOIS EASTERN DIVISION
Project	Trade secret case.
Dates	2013
Status	Completed.

Client	*LAM Research* (Carr & Farrell)
Case	LAM RESEARCH CORPORATION v. XYCARB CERAMICS CASE NO. 3:03-cv-1335 CRB UNITED STATES DISTRICT COURT

	NORTHERN DISTRICT OF CALIFORNIA SAN FRANCISCO DIVISION
Project	Review product for patent infringement.
Dates	2013
Status	Settled

Client	*Amkor* (Schwegman, Lundberg & Woessner, P.A.)
Case	Tessera v. Amkor
Project	Semiconductor manufacturing technology.
Dates	2013 – present
Status	Completed.
Desc.	IPR

Client	*3M* (Fish & Richardson)
Case	TransWeb v. 3M, District Court of NJ, 2:10-cv-04413 (FSH/PS)
Project	Litigation for plasma fluorinated electrets.
Dates	2011-2012
Status	Completed.
Desc.	Patent litigation for plasma fluorination of electrets and filters media, woven polymer fabric forming HEPA filters

Client	*Taiwan Glass* (Allegaert Berger & Vogel LLP)
Case	CVD Equipment v. Taiwan Glass, 10 Civ. 0573 (RH-I) (RLE), Eastern District of NY
Project	Litigation for breach of contract in CVD equipment used in the manufacture of low emissivity window glass and solar glass.
Dates	2010-2012
Status	Expert report, deposed, judgement.
Desc.	Chemical vapor deposition equipment for transparent conducting oxide (TCO) used in solar cells, and low emissivity glass (low E).

Patents

Patent Number	Date Issued	Title
7,118,090	Jan 20, 2007	Control Valves
6,679,476	Jan. 20, 2004	Control Valves
6,204,174	Mar. 20, 2001	Method and Apparatus Rate Deposition of Tungsten.
9,224,626	Dec. 29, 2015	Composite Substrate for Layered Heaters

Curriculum Vitae

Education

2003	Stanford University	Ph.D., Materials Science and Engineering
1995	Stanford University	M.S., Materials Science and Engineering
1987	University of California, Berkeley	M.S., Mechanical Engineering
1985	University of California, Berkeley	B.S., Mechanical Engineering

Publications and Conference Presentations (selected).

A.D. Glew, M.A. Cappelli, "Characterization and dielectric properties of fluorinated amorphous carbon measured by capacitance-voltage versus spectral ellipsometry", *Materials Research Society Symposium Proceedings,* **593***,* Boston, MA, 1999, pp. 341-346.

A.D. Glew, M.A. Cappelli, "In situ plasma analysis, fluorine incorporation, thermostability, stress, and hardness comparison of fluorinated amorphous carbon and hydrogenated amorphous carbon thin films deposited on Si by plasma enhanced chemical vapor deposition", *Material Research Society Symposium Proc*., **565**, San Francisco, CA 1999, pp 285-290.

A.D. Glew, R. Saha, M.A. Cappelli and J.S. Kim, "Ion Energy and Flux Dependence of Diamond Like Carbon Film Synthesis in Radio-Frequency Discharges", *International Conference on Metal Coatings and Thin Films,* Surface and Coatings Technology 114 (1999) 224-229.

A. Glew, R. Saha, M. Cappelli and J. Kim, "Ion Energy and Flux Dependence of Diamond Like Carbon Film Synthesis in Radio-Frequency Discharges", *International Conference on Metal Coatings and Thin Films*, San Diego, CA, April 1998

A. Glew, J, Ammenheuser, M. Crockett, A. Johnson, W. Dax, R. Binder, J. Riddle, "SEMASPEC 97043272A Accelerated Life Tests of Gas System Performance and Reliability," *http://www.sematech.org/public/docubase/abstract/3272atr.htm*.

A. Glew, J. Ammenheuser, J. Riddle, A. Johnson, "SEMASPEC 96083175A-XFR Determining the Effects of Impurities on Semiconductor Thin Film Processing," *http://www.sematech.org/public/docubase/abstract/3175axfr.htm.*

A Glew, "Selecting Gas Purity and Materials of Construction in High Purity Gas Systems," *Semicon West Symposium on Corrosion*, July 1997

Glew, J. Kim, K. Lee, M. Cappelli, "On the Characteristics of Diamond Like Carbon",
A. *International Conference on Metal Coatings and Thin Films*, San Diego, CA, April 1997

A. Glew, D. Porter, "Gas System Reliability Testing in Chlorine", *Semiconductor Fabtech*, May 1996.

Professional Associations

American Society of Mechanical Engineers (ASME)
International Microelectronics and Packaging Society
Materials Research Society (MRS)
IEEE
SEMI

Professional License

Licensed Mechanical Engineer, State of California, M26690

Laboratory analysis

On site: Microscopy, Vis and Near IR spectroscopy, thermal measurements, electrical-mechanical measurements.
Other Laboratory analysis may be provided through supervised third party laboratories: SEM, TEM, ESCA, AES, SIMS, FTIR, AFM ….

Technical Software Packages and Programming Languages (Selected):

Autodesk Simulation Mechanical (Algor™) 2015
Autodesk Simulation CFD (CF Design™) 2015
Autodesk Inventor™, Computer Aided Design 2015
Autodesk AutoCAD™, Computer Aided Design 2015
PTC Creo 3.0
Mathematica™ 10: mathematical analysis
Solidworks 2015

Civic Duties

Vice Commissioner, Design Review Commission, Los Altos, CA

Volunteer and Service Activities

Los Altos Rotary Club
    Veterans Committee and others
California Alumni Association
    Alumni Awards Committee 2015
    Alumni Awards Committee 2014
    Alumni Awards Committee 2013
NorCal Golden Retriever Club

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Fax: 650-292-2210
Email: adglew@glewengineering.com
Web: www.glew.com

Attachment B

Attachment B - List of Materials Considered

Exhibit/Paper	Description
EX1001	U.S. Patent No. 6,197,696 to Aoi et al.
EX1002	Expert Declaration of Dr. Bruce W. Smith, Ph.D.
EX1003	U.S. Patent No. 3,617,824 to Shinoda et al.
EX1004	U.S. Patent No. 3,838,442 to Humphreys.
EX1005	U.S. Patent No. 6,140,226 to Grill et al.
EX1006	U.S. Patent No. 5,635,423 to Huang et al.
EX1007	U.S. Patent No. 5,741,626 to Jain et al.
EX1008	C. Akrout et al., "A 480-MHz Microprocessor in a 0.12μm Leff CMOS Technology with Copper Interconnects," IEEE J. of Solid-State Circuits, Vol. 33, no. 11 (November 1998).
EX1009	J.N. Burghartz et al., "Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates," International Electron Devices Meeting (December 1996).
EX1010	U.S. Patent No. 6,100,184 to Zhao et al.
EX1011	U.S. Patent No. 6,103,616 to Yu et al.
EX1012	File History of U.S. Patent No. 6,197,696 to Aoi et al.
EX1013	Japanese Patent Application No. 10-079371 to Aoi.
EX1014	Certified Translation of Japanese Patent Application No. 10-079371 to Aoi.
EX1015	Japanese Patent Application No. 11-075519 to Aoi.
EX1016	Certified Translation of Japanese Patent Application No. 11-075519 to Aoi.
EX1017	U.S. Provisional Patent Application No. 60/071,628.
EX1018	U.S. Patent No. 5,592,024 to Aoyama et al.
EX2001	N. Sclater & J. Markus, McGraw-Hill Electronics Dictionary (6th ed. 1997) (excerpted)
EX2002	R. F. Graf, Modern Dictionary of Electronics (6th ed. 1984) (excerpted)
EX2003	R. F. Graf, Modern Dictionary of Electronics (7th ed. 1999) (excerpted)
EX2004	S. M. Kaplan, Wiley Electrical and Electronics Engineering Dictionary (2004) (excerpted)
EX2005	October 7, 2016 Preliminary Constructions, *Godo Kaisha IP Bridge 1 v. Broadcom Ltd., et al.*, (E.D. Tex 2:16-CV-134-JRG-RSP)

Exhibit/Paper	Description
EX2006	Declaration of Seung Woo Hur In Support of Patent Owner's Response Under 37 C.F. R. § 42.120
EX2010	Deposition of Bruce Smith in *Taiwan Semiconductor Manufacturing Co., v. Godo Kaisha IP Bridge 1*(P.T.A.B. IPR2016-01376) taken on March 23, 2017
EX2011	Redline Comparing Grill (EX1005) with Grill's Provisional (EX1017) Application
EX2012	Japanese Patent Application 10-079371 to Aoi as Submitted in European Patent Application No. 99 105 946.0 with accompanying translation
EX2013	Declaration of Takeo Ohashi, Ph.D. In Support of Patent Owner's Response Under 37 C.F. R. § 42.120
EX2014	*Influence of reactor wall conditions on etch processes in inductively coupled fluorocarbon plasmas* by M. Schaepkens, et al., J. Vac. Sci. Tech. A 16(4), Jul/Aug 1998
EX2015	*Handbook of VLSI Microlithography, Second Edition, Principles, Technology, and Applications*, edited by John N. Helbert, Noyes Publications, William Andrew Publishing, LLC, 2001 (excerpted)
EX2016	*Silicon VLSI Technology Fundamentals, Practice and Modeling,* by James D. Plummer, et al., Prentice Hall, 2000 (excerpted)
EX2017	*Microlithography: Science and Technology*, by James R. Sheats and Bruce W. Smith, Marcel Dekker, Inc., 1998 (excerpted)
EX2018	*Microlithography: Science and Technology*, 2nd ed., by Kazuaki Suzuki and Bruce W. Smith, CRC Press, 2007 (Chapter 12) (excerpted) (Smith Deposition Exhibit 3)
EX2019	*Microlithography: Science and Technology*, 2nd ed., by Kazuaki Suzuki and Bruce W. Smith, CRC Press, 2007 (Chapter 11) (excerpted) (Smith Deposition Exhibit 9)
EX2020	*Silicon Processing for The VLSI Era Vol. 1 Process Integration* by Stanley Wolf and R.N. Tauber, Lattice Press, 1986 (excerpted)
EX2021	Kenkyusha's New Japanese-English Dictionary, 4th ed., 35th Impression, published by Kenkyusha Ltd., 1997
EX2022	Declaration of Jordan Rossen In Support of Patent Owner's Response Under 37 C.F. R. § 42.120

Exhibit/Paper	Description
EX3001	Mask Definition, Merriam-Webster.com (last accessed Dec. 17,2016) (https://www.merriam-webster.com/dictionary/mask)
EX3002	Claim Construction Memorandum and Order signed by Magistrate Judge Roy S. Payne on Nov. 9, 2016, *Godo Kaisha IP Bridge 1 v. Broadcom Limited et al* (E.D. Tex 2:16-CV-134-JRG-RSP) (Dkt. No. 105)
Paper 2	IPR2016-01376 (Petition)
Paper 6	IPR2016-01376 (Patent Owner Preliminary Response)
Paper 11	IPR2016-01376 (Decision to Institute)