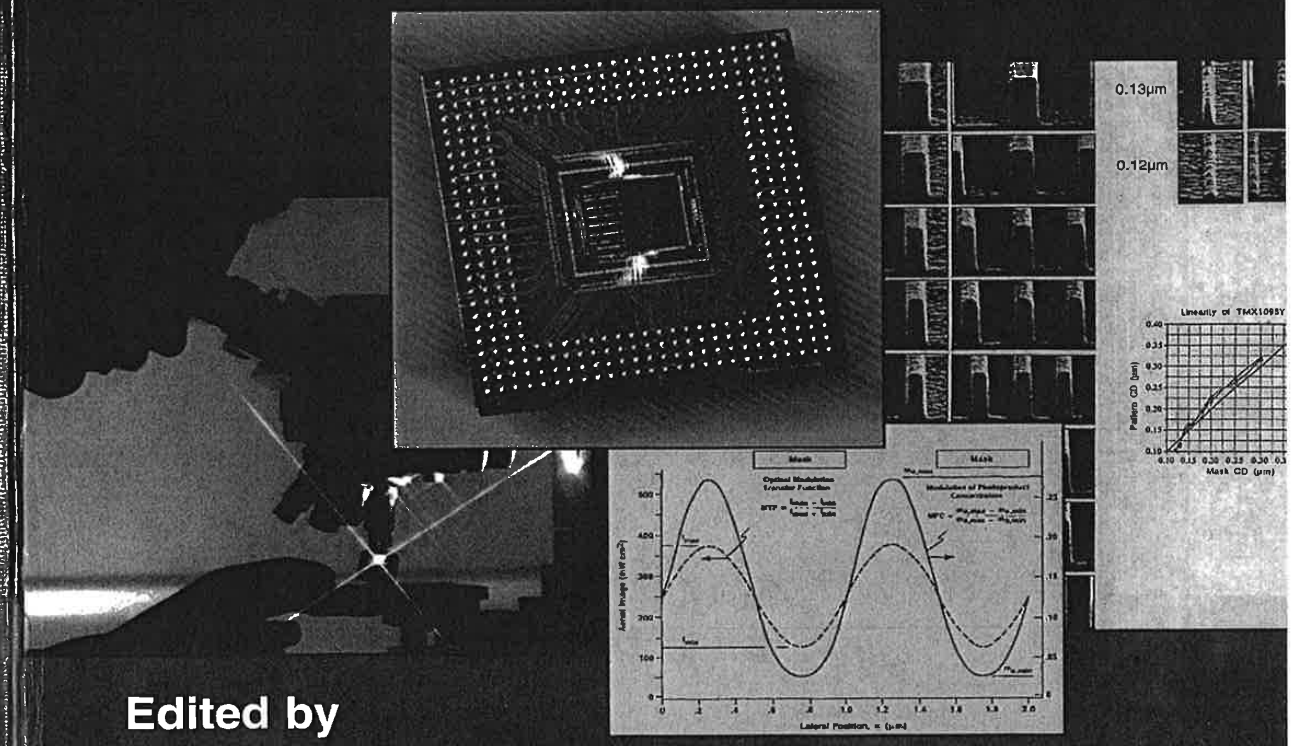
HANDBOOK of VLSI MICROLITHOGRAPHY

Principles, Tools, Technology and Applications • SECOND EDITION



Edited by
John N. Helbert

Gary E. McGuire, Series Editor
Stephen M. Rossnagel, Series Editor
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Helbert

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5.0 APPLICATIONS AND SPECIAL PROCESSES

5.1 Future Device Demands

Integrated circuit lithographic design rules have historically decreased over time, and will continue to do so—at least to the 0.1–0.07 micron level over the next 2–5 years. The driving forces for these increased circuit packing density demands are cost per function decreases, faster switching speeds, and lower chip power consumption. These new design rules will necessitate higher resist and lithographic tool resolution performance. Since the etching technology exists and tool contrast is only improved by the purchase of expensive new equipment, the goal for some process engineers simplifies to one of improving resist process performance. The processes in this section address this issue. Quoting L.F. Thompson of AT&T Bell Labs, "It's all in the processing." Resist processing is really the only variable left to most lithographic engineers with which they can influence device production, because the photolithographic tool aerial image limit is basically fixed by the manufacturer for a given generation of tool.

Conventional single-level positive photoresist technology has recently progressed rapidly, especially in the DUV class, but may be incapable of providing the necessary resist imaging required for the next generation of chips, i.e., less than 0.1 micron CD. Here, resist imaging thickness is the key issue to meet RIE etch masking requirements. Therefore, new resist processing technology (for example, surface imaging, like Desire processing) may be needed. Furthermore, processes which extend the performance levels of existing projection exposure tools or provide depth of focus relief are very attractive due to the increasing cost of new higher performance exposure equipment and the return on net asset demands placed upon chip sales of new devices to pay for these tools.

While a great deal of resist process research has been occurring to extend phototool lifetime, advances in reduction lens design and reflective optical wavelength reductions have also been occurring. As a result, optical lithography continues to relegate direct-write e-beam lithography to a quick turn around Application Specific IC (ASIC) role, and extensive x-ray lithography usage has continued to be delayed for years.

5.2 Introduction to Multilayer Applications

Multilayer processing techniques, where layers of radiation sensitive (top), non-photosensitive organic, and/or inorganic materials sandwiched together to become the total patterning layer, have become common in semiconductor and computer manufacturing R&D labs. (See Fig. 114.)[3] Due to their complexity and problems that have appeared at bilayer interfaces, these techniques have not been widely accepted in high volume production.

Photolithography image edge and dimension quality is limited by two basic effects, bulk and substrate reflectivity.[13][154] The bulk effect arises when lithography patterns are required at two different topographical layer levels of the vertically-fabricated monolithic circuit. Reflectivity effects occur when patterned areas of the circuit have different reflectivity coefficients, as well as topographical levels.

Lithographic exposure tool resolution performance can be influenced by resist processing. Stover et al.[155] have shown K from the resolution equation, $R = K\ wl/2NA$, is directly influenced by multilayer processing: wl is the monochromatic light wavelength and NA is the numerical aperture of the projection optics lens system; K is typically 0.8 in manufacturing with single layer resist processes but can be as low as 0.5 with multilayer processes.[156] Linewidth control is also directly affected by resist processing, and greater resist image critical dimension control can be achieved through multilayer processing[13] combined with anisotropic reactive-ion etching technology.

Lin[157] has done extensive research in bilayer systems, multilayer processes utilizing a UV sensitive material on top with a DUV absorbing or non-absorbing system underneath. This type of multilayer system has seen limited circuit fabrication application, because it is plagued by deleterious interfacial layers formed between layers at coat.[13][158] These problems have been solved by various treatments both before and after image formation, but bilayer technology has taken a backseat primarily to dyed thick single-layer photoresist processes.[159] Some bilayer processes are reported to be free of interfacial mixing problems,[160] and the organic ARC process described is a usable bilayer system.

Trilayer systems[161] utilize an intermediate layer between the photosensitive top layer and the virtually developer-insoluble oxygen RIE patterned bottom layer. It is usually deposited by low temperature (< 250°C) thin film deposition techniques, but can also be applied as a liquid spin-on-glass solution.[162]–[164] The middle layer can also be a spun organic polymer (also water soluble) barrier layer coating for the lithographic trilayer processes, as

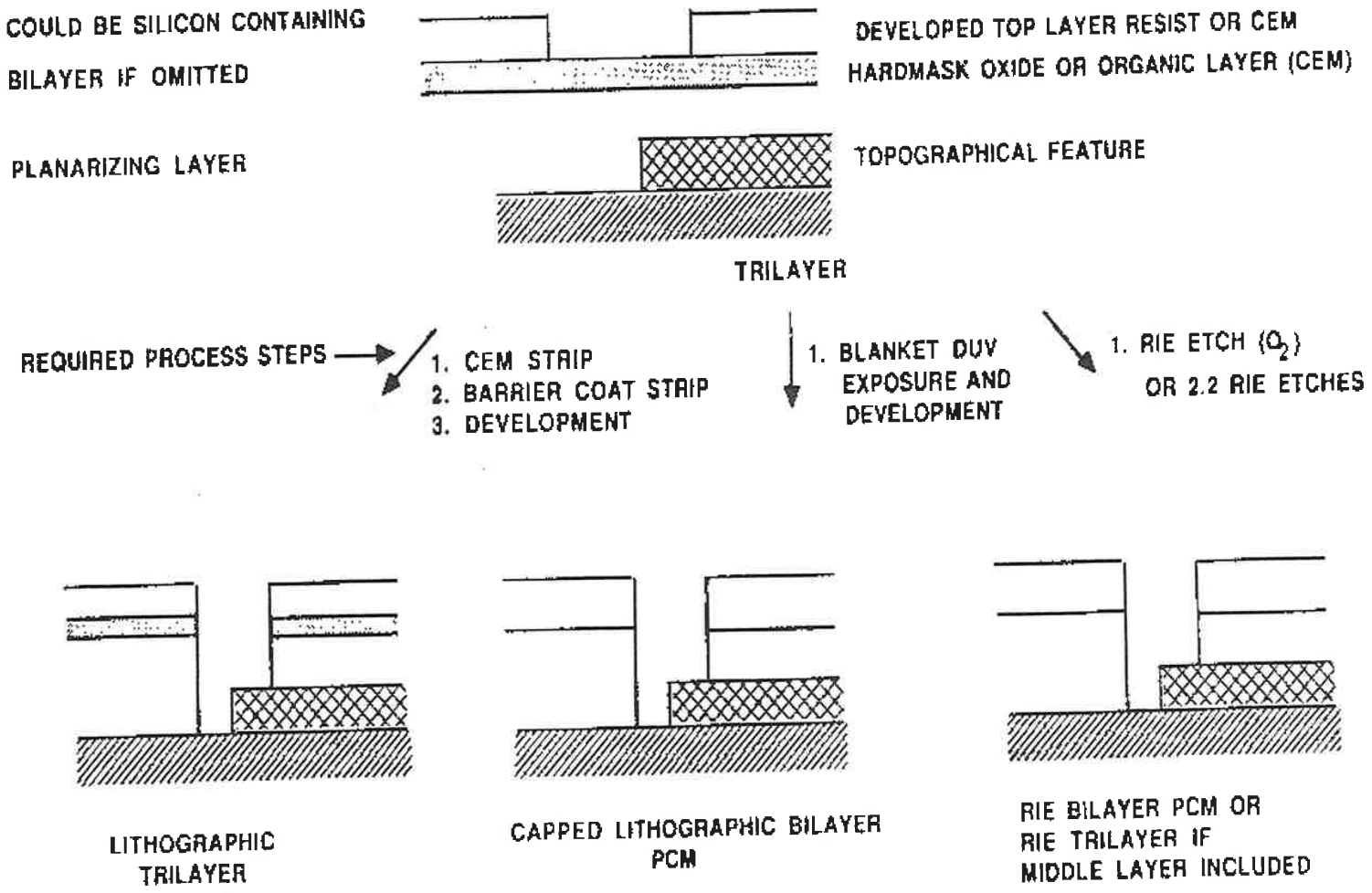


Figure 114. Multilayer resist systems illustrating different multilayer processes and PCM techiques.

opposed to RIE trilayer processes where the middle hard mask material must be RIE etched and cannot be developed by base developers or water. While the former technique is usually void of interfacial mixing layer problems, the latter technique can exhibit this problem intermittently.

All of the multilevel processes described are successful to some degree in relieving resolution and linewidth control limitations of current single-layer optical exposure equipment. Future device fabrication requirements and the application of high numerical aperture exposure equipment, however, will most likely create the need for multilayer processes at one or two critical device levels.

5.3 Introduction to MLM Lithography

The requirements of VLSI/ULSI multilevel metallization (MLM) systems have led to numerous challenges in the photolithographic and etch areas. These challenges arise from two inter-related sources: the continuing trend to smaller geometries and the new materials that must be used to build a successful MLM. Smaller geometries often create a need for new materials, and the ability to process those materials can limit usable geometries. Photolithography and etch technologies with the capability of producing submicron MLM structures are an integral part of the successful fabrication of the high density, high performance, and highly reliable interconnect technologies of the nineties and beyond.

For devices with multilayer metal (MLM) interconnects, these individual layers are insulating dielectrics or metallic interconnect layers. The ability to produce high quality MLM layers depends upon both the lithographic tool imaging capability, quantified by the Modulation Transfer Function (MTF) (see Ch. 5) of the tool optics which in part depends upon the tool objective lens numerical aperture (NA), and the resist process quality or CMTF.[3][165] The electrical yield for MLM device layers depends upon these quantities for device element packing density and the ability of the lithographic tool to align layer to layer; the combination of CD control and alignment control represents the total overlay capability of the system which must be better than that required by the design rules for the circuit.

5.4 Applications

It is well known that lithographic image sizes, better known as critical dimensions or just CDs, and CD variation are governed to first order by the quality of the stepper projection lens (i.e., NA and MTF), the resist contrast

or CMTF, and the degree of the resist process optimization.[3][105][165] As CDs get smaller and the lens and resist parameters approach their practical limits, secondary characteristics such as lens astigmatism and proximity, substrate reflectivity, topographical or bulk effects, and local resist thickness variation begin to be significant and have to be controlled along with the primary effects for successful device fabrication, especially at less than 0.5 μm polysilicon gate, or any other layer for that matter, dimensions for advanced CMOS or BICMOS device fabrication.

Dyed and Thinned Single Layer Resist (SLR) Processes. The two most obvious things to do to improve resist imaging performance on the most difficult substrates (i.e., those requiring greatest resolution and with reflective topography as for device isolation, gate, and MLM metal and via levels), is to reduce the resist thickness and add dyes to it, respectively. Unfortunately, resist thinning is most feasible with multilevel lithography processes,[166] where a thin top resist layer is allowable. Resist thinning in itself accomplishes nothing towards reflective image notching relief, the main observed problem for reflective topographical gate or MLM situations. Furthermore, resist thinning presents a severe problem to step coverage and metal etching because of poor selectivity, and is in fact usually prohibitive. All of these negatives aside, resist thinning has been shown by IBM researchers[167] to improve linewidth control by 15% and focus control by 35%, when and if it is feasible to do it. Therefore, the full advantages of resist thinning may be really only achievable through bi- and trilayer lithographic processes, further reinforcing the restrictive applicability of resist thinning.

The more practical solution to reflective notching problems, those observed on reflective surfaces due to either feature topographical or metal grain boundary relief structures, is provided by resist dyeing. Most device fabrication areas will select this option over multilayer Portable Conformable Mask (PCM)[166] processes due to greater simplicity and lower costs. The resulting dyed and usually thicker (~2 microns) material is still a single level resist process, but without the added complexity of multilayer processes; note also, by going to thicker dyed resists relief from topography induced CD variation, the well-known "bulk effect" is also achieved. Dyeing resists requires a price be paid in lower resist contrast[168] and greater exposure time,[169] but dyeing does provide greater process latitude[97] and reflective notching can be effectively eliminated[76] or at least minimized.

Sandia workers[170] have provided a dyed system for H and G line steppers which has a very small exposure penalty, just 15 mJ/cm^2. Bolson et al.[76] have demonstrated similar results, and an approximately 60% gain in

exposure latitude was achieved or a reduction in k_1 from the Raleigh resolution equation from 1.1 to 0.6 was effectively obtained. On the negative side, adding dye to the resist formulation may lead to a larger standing wave foot,[171] lower depth of focus (Table 5), and reduced imageedge wall angles consistent with the observed bulk contrast reductions reported by Pampalone.[168] Most dramatically, Brown and Arnold[171] have observed a 3-fold increase in CD exposure latitude, a result which explains the wide acceptance of this technique for metal layer lithography by older mature production fab lines, lines where metal CDs are larger and advanced planarization techniques beyond POT processing are not common (see planarization section).

SLR Image Reversal (IREV). Positive photoresist image reversal (i.e., negative toned imagery from a positive toned resist) is a processing technology which addresses the deficiencies of single-layer dyed resists. Moreover, IREV can be accomplished on dyed material to achieve the best of both worlds, namely, relief from topographical or bulk effects and reflective notching minimization. Over the years, many papers have been published on this subject.[172]–[180] The salient contents of those papers will be reviewed and compared. The main focus of this section is on single level thermal induced reversal processes for AZ 5214.

Image reversal is an alternative to conventional positive photoresist technology. Briefly, a single layer of positive photoresist is exposed using a projection aligner, reversed by either doing a post exposure thermal treatment on a hotplate or by adding a base to the resist, flood exposing and developing. The result is a negative toned image with a controllable edge wall angle, something dyed resists with conventional processing cannot deliver. The IREV processes are capable of printing images previously unattainable with the given exposure tool, thus, extending the resolution and focus latitude performance of the alignment tool, and the life of it as a capital asset.

Marriott, Garza, and Spak have written the definitive paper on thermal image reversal.[179] Using both theoretical PROSIM simulation and empirical methods, the AZ 5214 IREV process has been optimized, and good agreement between theoretical images and real images obtained. The process was optimized for photospeed, resolution, focus and CD latitude, and vertical edge wall by adjusting the developer concentration to 0.21 N MF-312 (90 secs), setting the PEB temperature to 110°C, and by using a flood exposure after PEB. This data has been independently verified at Motorola (see Fig. 115). An improvement of 1.25 micron in focus latitude, 150% improvement in CD control and a 8° improvement in image edge wall were also reported.[179] AZ researchers further reported a bulk contrast

performance improvement of roughly 200% for IREV AZ 5214 over that for the positive performance mode. Consistent edge wall imagery improvement can be seen when comparing Figs. 115 and 116, where Fig. 116 portrays images with edge wall angles more typically observed from normal positive tone performance.

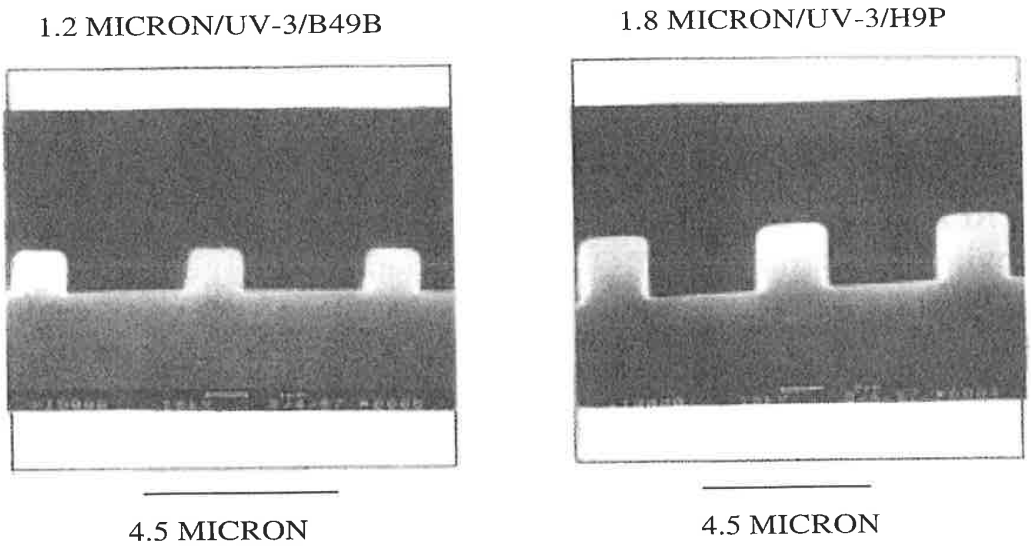


Figure 115. AZ-5214 thermal tone reversal process edge wall profiles illustrating vertical edge walls.

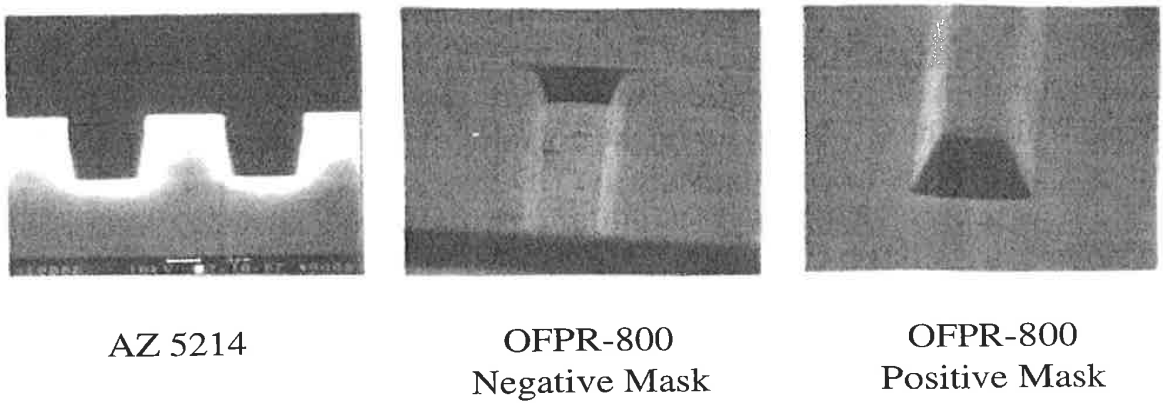


Figure 116. Edge wall profiles for conventionally developed positive photoresist images. Note, the edge walls are poorer than those for both IREV processes.

All in all, it is felt that the image reversal process advantages may overshadow the disadvantages for certain critical device fabrication levels, where standard resist processing technology simply cannot satisfy the future lithographic imaging requirements. Furthermore, work by Gijsen et al. (see Ref. 90 of Ref. 129) has demonstrated image reversal behavior for dyed positive photoresist without degrading edge wall slope advantages, thus providing a process with relief from integrated standing wave and pattern scattering effects in addition to the relief from the bulk effect provided by the undyed reversal process.

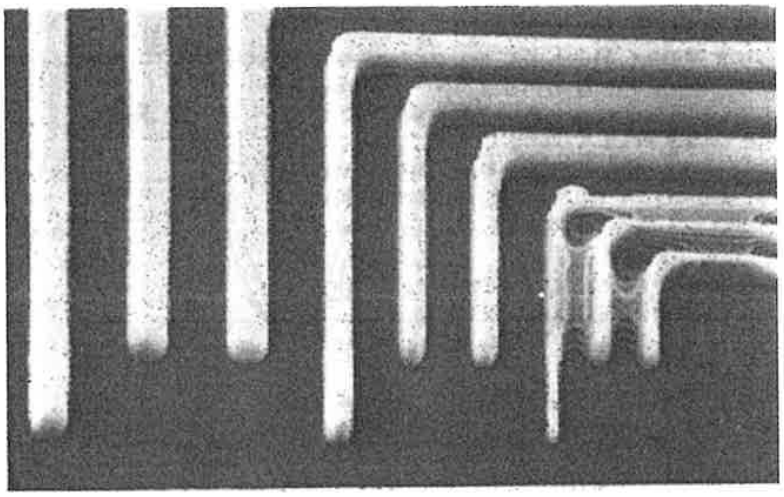
Resist Processes For Reflective and Topographical MOS Gate Situations.[181] In this section, an example, silicided, 0.5 μm polysilicon gate layer is focused upon and all data presented is for that critical device layer. Resist simulations of CDs and substrate reflectivities were obtained employing the version 2.2 PROLITH simulation package.

The problem or dilemma faced early in the 0.5 μm work dealt with polysilicon CDs which were larger in a packed line device configuration than when they were isolated. This was just the opposite to that which was typically observed for metal or for single crystal silicon substrates and even flat polysilicon substrates.[182][183] Furthermore, the results of Ref. 184 have demonstrated that the effect gets larger the smaller the pitch, and those authors actually recommended that this effect be corrected for at design by differential biasing.

On flat surfaces, with all other factors being negligible, the isolated CDs can be anywhere from 0.03–0.06 μm larger than that for the tightly packed features, a bias which is not negligible at 0.5 μm CDs, i.e., it's greater than 10% without any normal processing variation; this bias can actually get as large as 0.08 μm depending upon how large the normal photo/etch bias is. Figure 117 contains PROLITH 2 simulation data consistent with these empirical results, therefore, another mechanism must be controlling the CD behavior on the polysilicon gate device test structures other than the normal iso/dense resist CD bias effect.

PROLITH swing curve simulations, plots of resist CD vs. resist thickness, for silicon and polysilicon substrates were also very similar as found in Fig. 118. But, when swing curves for polysilicon resist images on raised field oxides are compared to those for images on topographically lower active device regions, the curves are shifted along the resist thickness axis for both isolated and dense gate features.[185] This result now provided a mechanism, i.e., the resist thickness differences between field and active regions,[185] to allow for the possibility for the resist polysilicon CD to be

larger or smaller depending on polysilicon underlying structures. Notice, however, that although the data of Ref. 185 shows the effect of swing curve shifting for the first time it still cannot account for the observed gate CDs being larger for packed features, so a closer look is required.



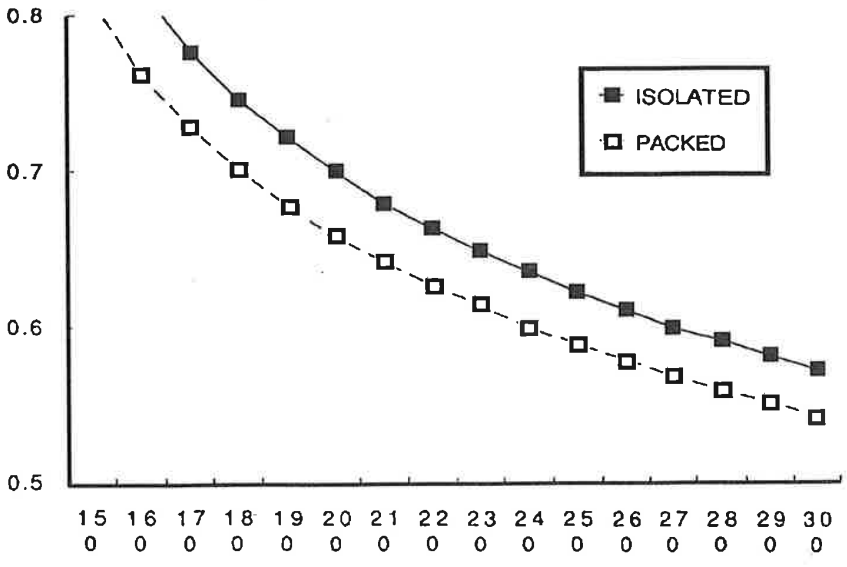


Figure 117. PROLITH generated polysilicon resist CD vs. exposure for isolated and packed lines. The simulations are verified empiracally in the SEM picture on the top.

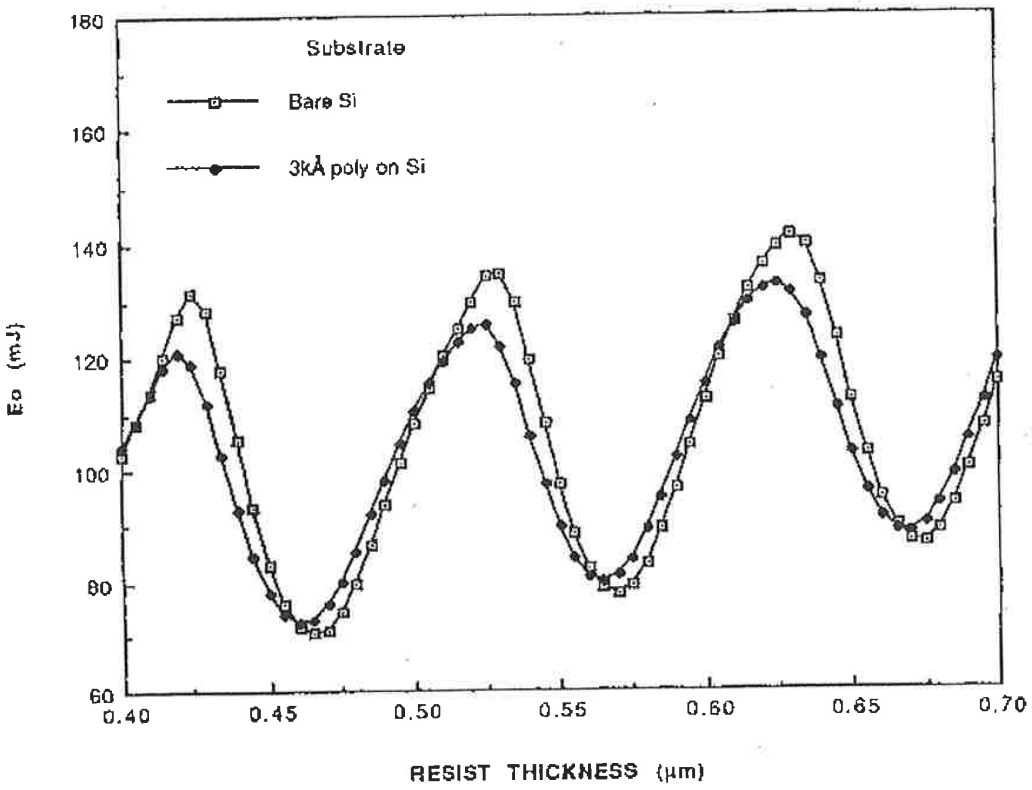
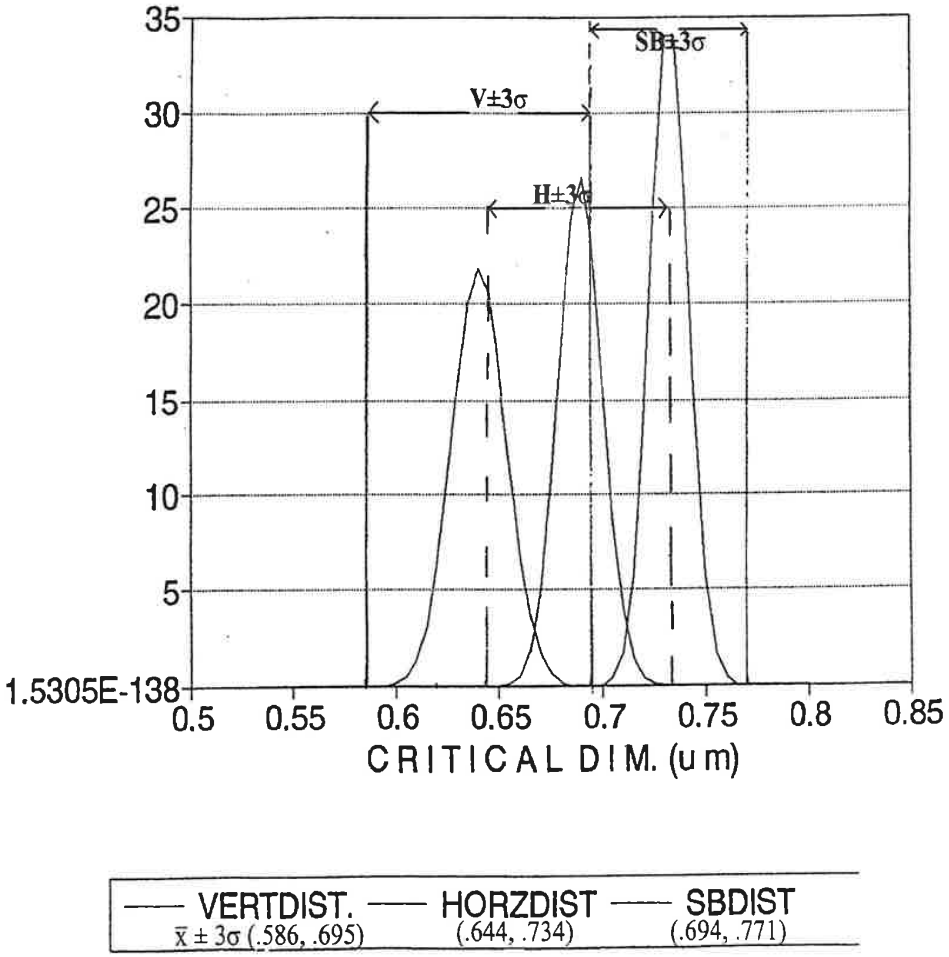


Figure 118. Resist sensitivity vs. resist thickness for gate CDs on polysilicon and silicon wafers. Linewidth vs. thickness would look the same if plotted.

This leads to lens astigmatism. For the Canon 0.52 NA lens employed, the astigmatism was =10 nm, so, this contributor was negligible. This was a valuable piece of information since the packed CDs were oriented 90 degrees off 0 or horizontal to the isolated transistor gates. Figure 119 further illustrates the CD distributions for isolated horizontal gates are also well separated from the vertical isolated gates as well as smaller. As a sanity check, swing curves were generated for silicon and polysilicon test wafers with absolutely no underlying patterns or topography. The polysilicon CDs for these images were as predicted by normal proximity, and reversed in order from those observed for live product wafers (compare the data of Fig. 120 to that of Fig. 118 and 119). So, when the substrate is flat and unpatterned, there are no swing curve phase shifts and the packed gates are smaller than the isolated gates as pure "proximity effect" would dictate.



H_o : Variances equal	F	P
$\sigma_v^2 = \sigma_H^2$	1.98	≈ .10
$\sigma_v^2 = \sigma_{SB}^2$	1.48	≈ .2
$\sigma_H^2 = \sigma_{SB}^2$	1.33	≈ .2

Figure 119. Normal distributions of polysilicon CDs for BIMOS gates showing the effect of gate orientation and gate oxide substrate nature.

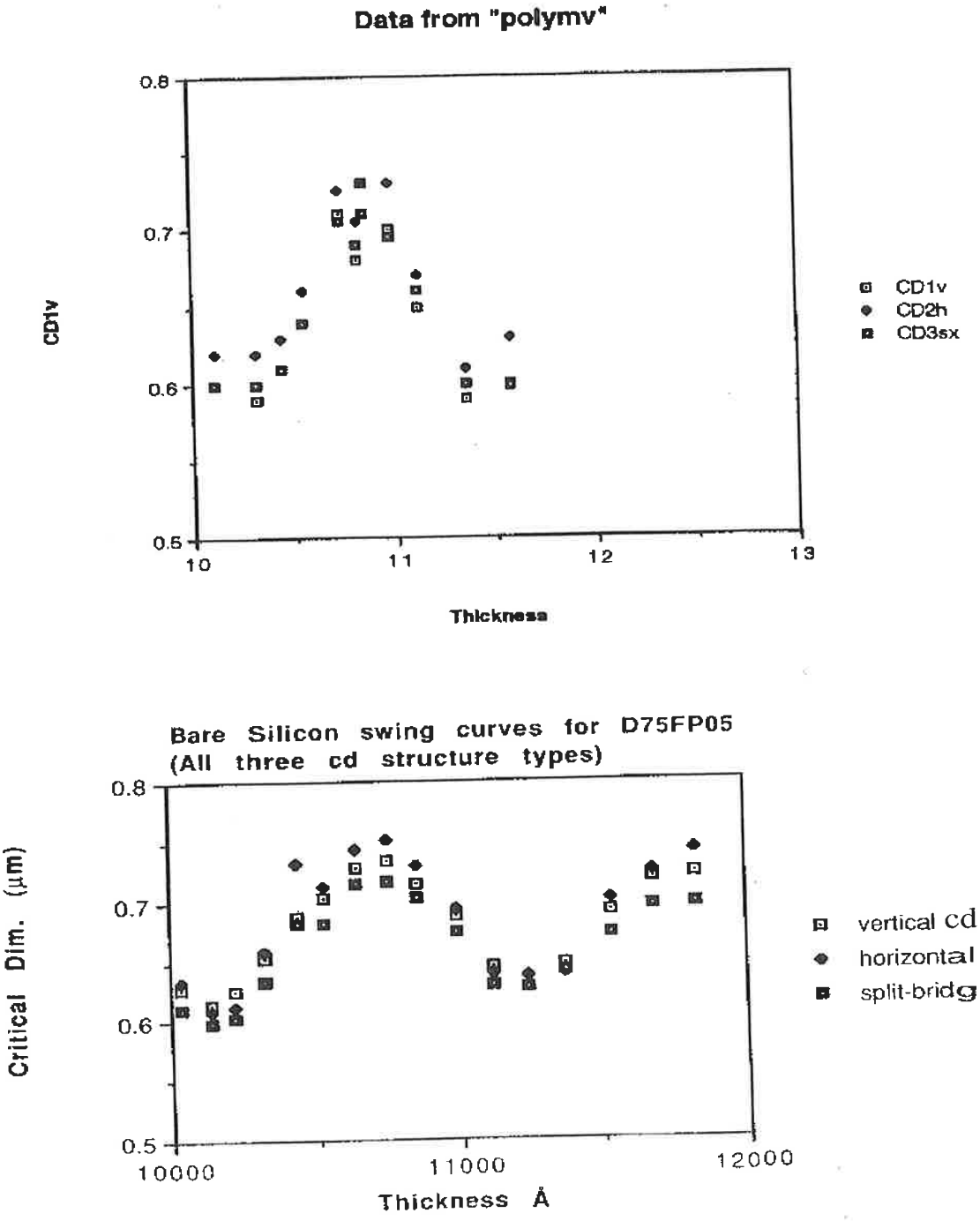


Figure 120. CD vs. thickness of resist for the three gate types on bare silicon wafers with no previous patterns.

How can the data of Fig. 119 be rationalized? The answer lies in the data of Fig. 121. Here, the swing curves have been generated for the three different gates on live BIMOS product wafers as in Fig. 119; notice that the packed gates on field oxide, as for Ref. 185, have a dramatically different swing curve phase than the other curves. At resist thickness of 10,800 Å, the split bridge packed gates are in fact larger than both the horizontal and vertical gates on gate oxide over active area. Hence, a mechanism or a reason for the observed gate CD order results is obtained, which, as for the results of Ref. 185, is attributed to local resist thickness variation in the respective gate areas. Further note, that even though there is little if any lens astigmatism, the horizontal gates are also larger than the vertical gates, again because their swing curves are shifted even though they are at the same topographical level.

The final effect described is reflectivity, R. As for swing curves, polysilicon reflectivity varies sinusoidally with resist thickness due to standing wave interference effects. CD variation with thickness is in phase with R, but CD variation is usually just roughly in phase, or the CD variation on polysilicon is usually a minimum when reflectivity is at a minimum.[186]

In conclusion, the large effects reported here must be canceled out by differential CD biasing at device design CAD or with OPC applied corrections. The proximity induced iso/dense CD effect contribution, which can be completely canceled out or dominated by larger swing curve effects, can be minimized by employing improved resists.

Device Isolation Topography Effect upon Resist Gate CD Control.[187] First generation LDMOS devices, laterally diffused RF devices, are characterized by large gate pattern dimensions (i.e., 1 micron and greater) and mature but topography creating single hipox isolation processing. Figure 122 illustrates the severe topography created by the "bird's beak" of this older device isolation process. This topography creates an unwanted constraint upon the resist coating process, which in turn affects CD control in a negative way, both gate to gate and within gate for the RF device. In fact, the gate dimension across the RF device active area can vary as much as 160 nm as verified by Fig. 123, the "wavy gate effect" first reported in this section. If the resist thickness is measured across the active area, it varies in direct correlation to the CD variation consistent with the well known effect on CDs of varying resist thickness, the resist swing curve effect. This is similar to the effect discussed above for polysilicon gates.

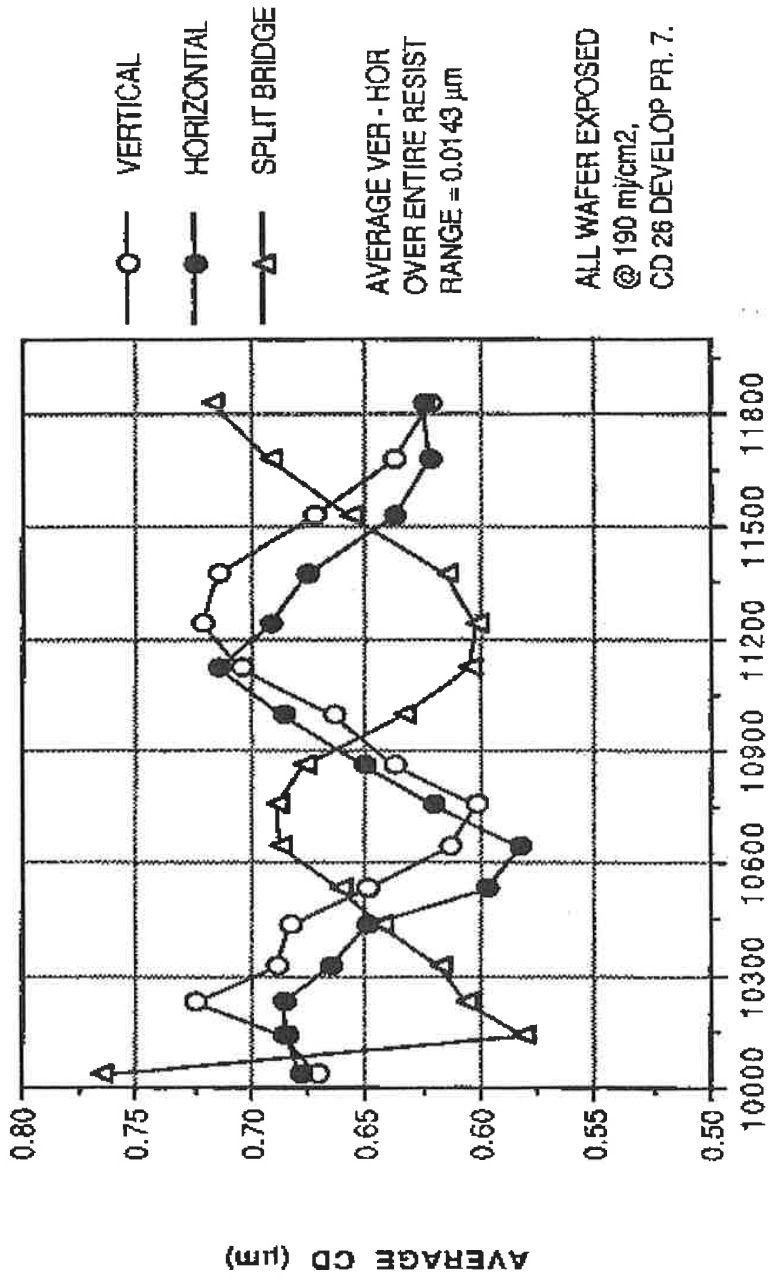


Figure 121. CD vs. resist thickness for actual live BIMOS product illustrating gate type effect upon the individual swing curves.

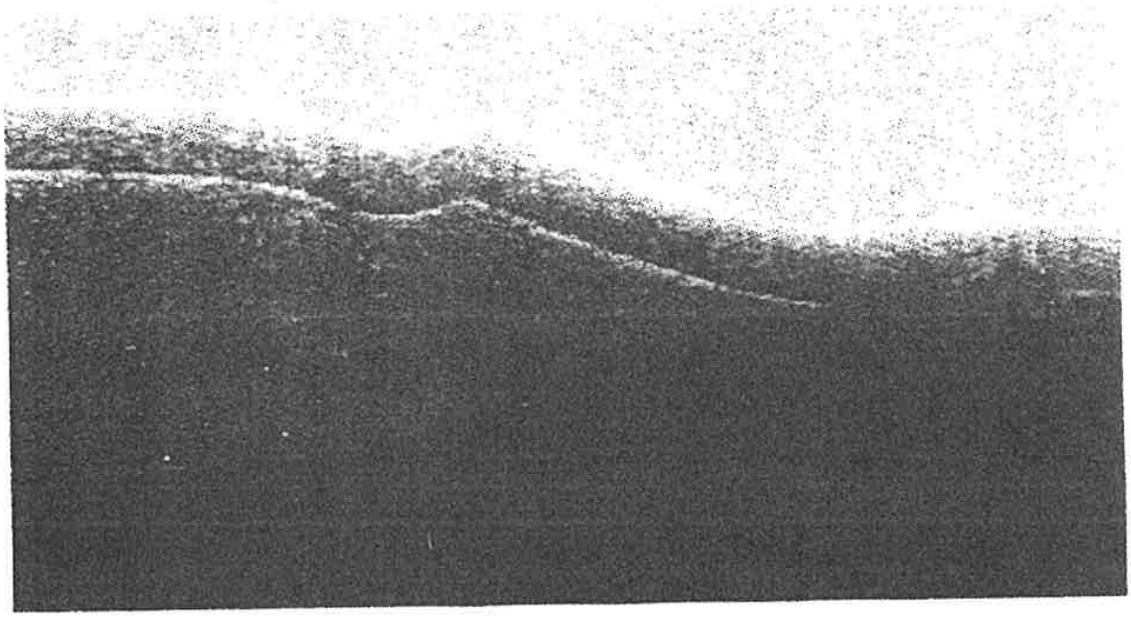


Figure 122. SEM cross section of the "Bird's beak" topography inherent to the single hipox device isolation process.

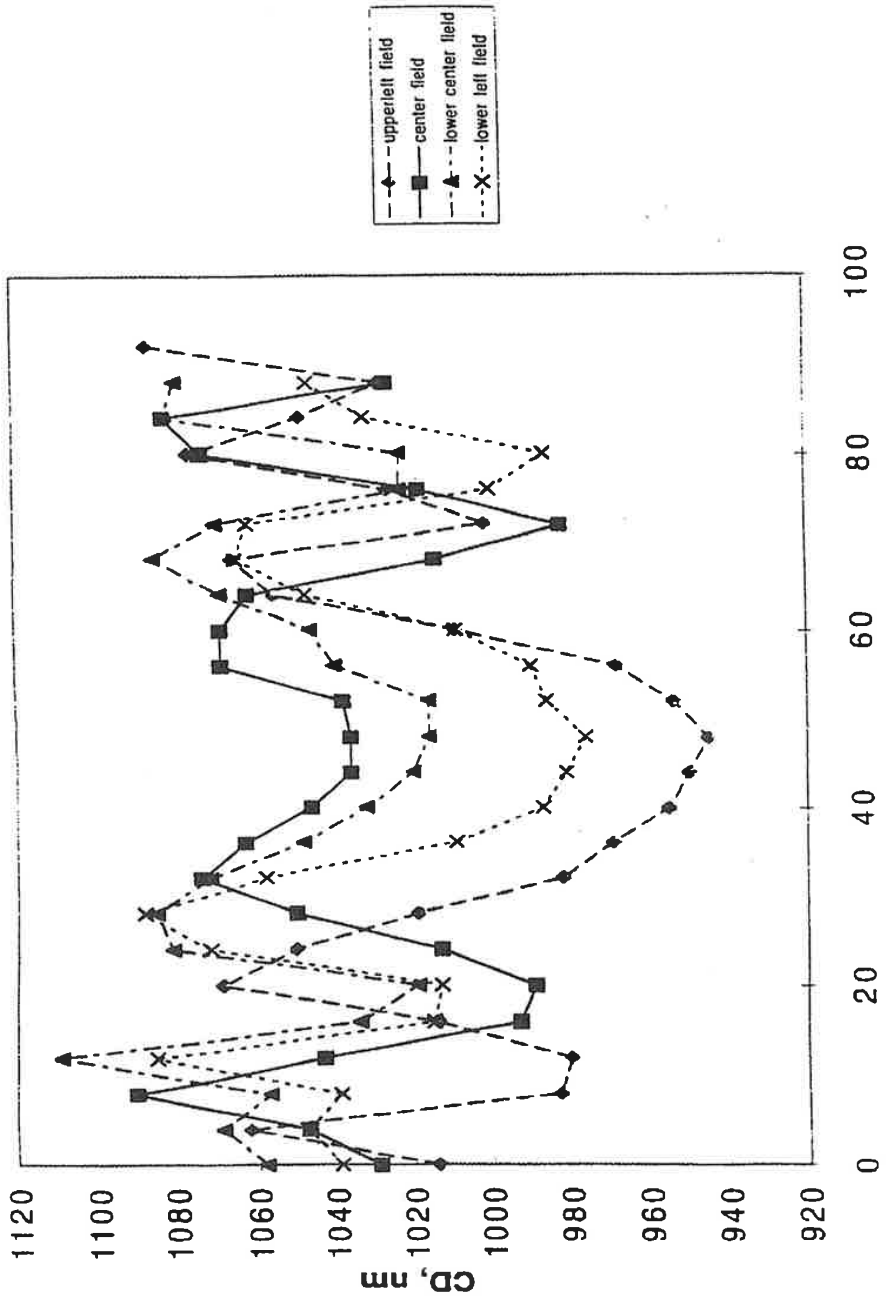


Figure 123. Plot of gate CD vs. position along the gate across the active device area.

Third generation LDMOS devices, however, must have submicron gate dimensions (i.e., < 0.6 microns) and require much less gate image dimensional variation to perform within minimum acceptable device threshold tolerances. The topography minimizing or "bird's beak" reducing effect of the modified double hipox isolation is shown in Fig. 124. There, the first hipox is followed by oxide removal and another hipox to leave the wafer surface much flatter. The effect of this extra device isolation processing is improved wafer flatness as manifested by improved resist uniformity across the active area and the resultant gate CD control. The data of Table 22, clearly demonstrates a factor of four times the improvement due to the less topographical modified double LOCOS isolation process. The gate CD range along the gate for the improved isolation scheme reduces to 22 nm versus the 160 nm observed for the single LOCOS isolation process, and the gate to gate variation is only 39 nm for the new process. These CD improvements are dramatic and more than justify the extra process cycle time incurred.

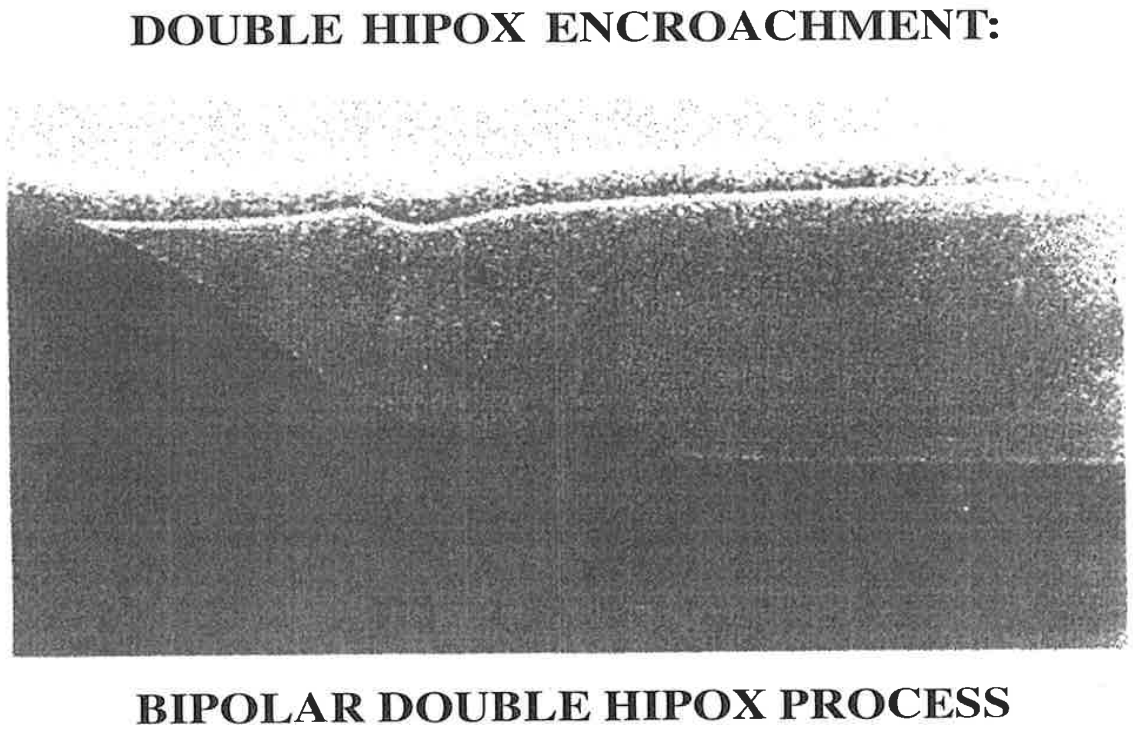


Figure 124. SEM cross section of the reduced topography inherent to the double hipox device isolation process.

Table 22. CD Families of Variation for Both Isolation Processes and The ARC Process With The New Isolation Process[187]

Variance Component Estimates		
Process	Component	Standard Deviation
2-MLOCOS	wafer	3.1×10^{-3} μm
	site [wafer]	6.3×10^{-3} μm
1-LOCOS	wafer	7.67×10^{-3} μm
	site [wafer]	20.8×10^{-3} μm
ARC	wafer	1.01×10^{-3} μm
	site [wafer]	6.55×10^{-3} μm

Notice also that the use of ARC, which usually improves CD control where CDs are varying due to local thickness variation, has little effect upon the multivari CD results as would be predicted. The total CD variation is the same with or without ARC, again as a result of the improved wafer surface flatness created by the modified double LOCOS process.

In conclusion, we have quantitatively compared the effect of resist process and isolation processing upon RFLDMOS gate image CD variation, and found that the modified double hipox isolation process reduces the gate variation by close to a factor of four times. This tighter gate CD variation performance has allowed this device to be manufactured in volume production at high yields and performance levels.

Multilayer Resist Processing—An Optimized Organic ARC Process for I-Line Lithographic Fabrication of 0.5 μm Devices. When dyed resists, which have been widely used to prevent notching reflections in older product line fabs at greater than 1.0 μm metal linewidths, fail to provide the necessary reflective notching relief, multilayer processes may be employed.

Dyed resist useage is limited by reduced contrast, resolution loss due to greater film thicknesses, and poorer general effectivity.[171] An example of the failure of dyed resist processing to prevent metal grain boundary reflective notching is found in Fig. 125; the severe reflective notches are

easily seen along the resist pattern edge. The notching effect caused by the substrate reflectivity of this example can be reduced by employing inorganic or organic antireflective coatings (ARCs) in a bilayer structure, i.e., the ARC layer is below the resist patterning layer on the wafer surface. Bilayer ARCs have been widely used in optical lithography to prevent or minimize problems of linewidth variation caused by substrate topographical reflective notching, i.e., for resist metal line images running over vertically raised steps on the substrate.[171][188]–[194] Antireflective coatings also help reduce standing wave and thin film interference or swing curve effects,[190] a result similar to the effect of increasing the resist B parameter by resist dyeing, and IBM has further shown they can also be top ARC coatings as well.[195]

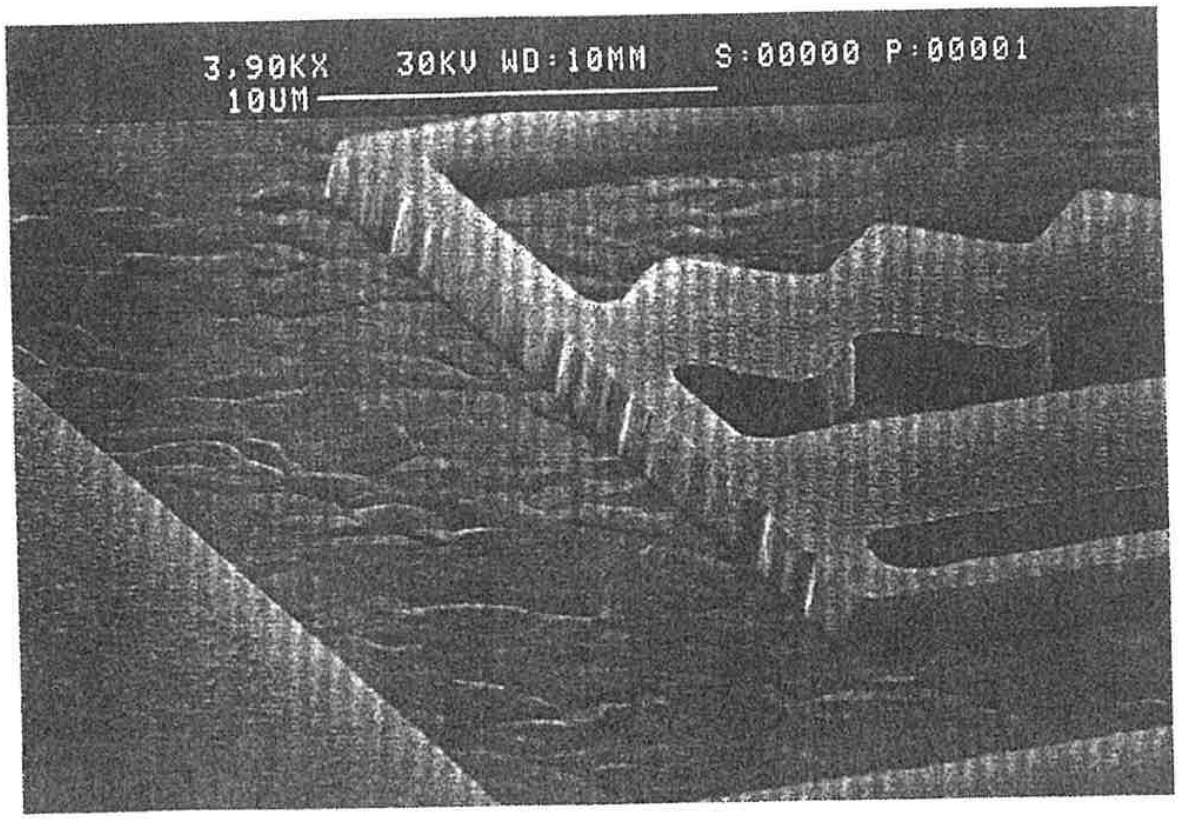


Figure 125. SEM micrograph of notched resist images on large grained aluminum film.

Inorganic layers, sputtered thin films, such as a-Si, V, TiW,[171][188] TaSi and TiN,[189] and TiON,[190] have been tested and employed as ARC layers. Economic factors at larger feature sizes, however, favor the use of organic ARCs based upon equipment costs.[171] The example, and actually an older material, organic ARC referred to primarily in this chapter, is ARC-XLT, manufactured by Brewer Science.[191] Bilayer ARCs from this manufacturer have been, and continue to be, widely used, even in volume MOS production lines. Currently, almost all DUV applications involve either anisotropically dry-developed organic ARCs or inorganic ARCs, such as TiN, Si-rich nitride or an oxy-nitride film. Very few DUV resists are even tested without an appropriate ARC, all being required due to the greater reflectivity of device layers at DUV wavelengths and below.

ARC Processing Example. Organic ARC bake conditions need to be carefully optimized and controlled for aqueous-base developed organic ARCs.[171][192] The bake latitude for the ARC process is found to be extremely critical to the lithographic results.[191][192] This section outlines a strategy for ARC process optimization, which led to improved lithographic results, as verified by metal electrical snake structure probe data. Most significantly, through ARC process optimization, including the develop process, it is found that the ARC application resolution range can be extended to much smaller geometries than the 0.9–1.0 μm limits previously reported;[171][188][191][192] these references attributed that limitation to development undercut of the ARC layer, created by the isotropic nature of it. Furthermore, the greater bake process latitude reported in Ref. 191 has been confirmed.

ARC Process Optimization Strategy. The optimization strategy entails the use of the following two response variables which help by simplifying the type of experiments to be performed: *(a)* ARC thickness remaining after development: Experiments that use this variable as a response are very simple to perform, in that they do not require the use of photoresist or an exposure tool. The rate of ARC development is probably the most important factor in determining lithographic performance for a fixed ARC/photoresist system. This response variable is used to explore and obtain a broad process window, while the final conditions were determined by further experimentation within this window using the response mentioned in *b*, *(b)* Minimum CD remaining without lift off: ARC undercutting has been a limiting factor in determining the upper limit of resolution with regards to lithographic performance. A small circular pillar-like pattern is best for this testing because this structure is very susceptible to undercut lifting. This response variable plays a key role in ARC process optimization.

An example of a pillar functional test working specification for 0.5 μm MLM processing would be 0.6 ±0.1 μm. Furthermore, this simple functional test provides an SPC ARC control test for routine daily qualifications. The following sequence of experiments were all integral parts of the optimization strategy:

i. Identification of bake and develop methods: The following variable combinations will be discussed here:

a. Convection bake/immersion develop

b. Contact bake on a hot plate/single spray puddle develop

ii. Determination of bake uniformity: An acceptable level of ARC thickness uniformity following bake has to be achieved and verified by ellipsometry.

iii. Screening design experiment to determine significant variables: This experiment was a 2^{7-4} fractional factorial[99] using ARC thickness after development as a response. Wafers were coated with ARC only. Resist softbake /PEB were taken into account in the process simulation. The development time used was 5–10% of the actual develop time for resist coated wafers. Variables used in this design were:

a. Dehydration bake

b. Delay between ARC coat/dehydration bake

c. Delay between convection bake/ARC coat

d. Bake temperature

e. Delay between resist coat/ARC bake

f. Resist softbake

g. Post exposure bake

These variables may vary depending on the type of bake used. Variables such as proximity bake, wafer gap from hot plate may be included as desired.

iv. Determination of development rate of ARC in developer: ARC thickness remaining after develop was determined for a series of development times. From the screening experiment, bake temperature and time were determined to be the only significant variables. Hence, a two factor

Central Composite Inscribed (CCI) design was[100] run using these two factors and ARC thickness, post develop, as the response variable. This experiment led to an empirical result with a broad enough process window for further experimentation to take place. The final ARC thickness at the end of the photoresist/ARC develop process has to be zero. However, the ARC thickness should not approach zero early on in the develop process because this will lead to severe undercutting, hence, the reason for process optimization.

v. Minimum feature size remaining without lift off on metal wafers: The two factor Central Composite Inscribed design above was run using a range of ARC bake temperatures and times. Minimum CD without pattern liftoff was determined. Wafers were checked for possible ARC scumming. ARC bake conditions were selected for lowest possible CD remaining without the presence of ARC scum, which occurs readily at high bake temperatures (greater than 180°C) due to excessive ARC curing.

vi. Process verification using SEM cross-section/electrical probe: An electrical probe structure in the form of a standard snake pattern was used to verify process conditions. CDs may also be determined electrically using linewidth split cross bridge structures. Cross sections using the SEM reveal final ARC/resist profiles. SEM measurement waveforms may also be used to qualitatively determine profiles for the presence of an ARC foot.

Optimized Process Comparisons. Results of the screening design experiment for convection bake/immersion develop suggested that the only significant variables were bake temperature and bake time from RS1 empirical modeling.

Plots of ARC thickness remaining were obtained for different temperature/time combinations using a 2-factor CCI experiment. The statistical analysis confirmed bake temperature, bake time squared, and the product of bake temperature and bake time to be significant factors for this response.

A follow up 2-factor factorial experiment was conducted using these conditions and using metal snake probe yield as a response. Neither

temperature nor time was determined to be statistically significant for probe yield, however, the product of temperature and time was still significant.

The optimum process conditions were determined to be 163°C bake for 41 minutes This is a 1.3 μm line, 0.7 μm space pattern, and ARC undercutting is clearly visible as reported in Refs. 171, 188, 191, and 192. Table 23 clearly illustrates improvement in CD control with the optimized ARC process compared to the unoptimized process. The ARC process optimized for immersion develop can also be used successfully in conjunction with track development. However, the presence of an ARC foot can be a problem if the same bake conditions are used. The foot problems are most likely related to problems with convection baking which include *(i)* temperature variation in the oven as a function of position, *(ii)* heat loss upon opening of oven, and *(iii)* operator errors leading to overbake. The presence of the ARC foot combined with the problems mentioned above made it necessary to switch to track baking of the ARC, which provides better temperature and time control, and it increases wafer process throughput. Plus, wafer track processing is more manufacturable.

Table 23. Mean CD and Total CD Variation for Resist Processes With and Without ARC

Process	Mean CD μm	CDVariation 3-sigma
SPR 500/unoptimized ARC	1.10	0.35
SPR 500/optimized ARC	1.04	0.09
SPR 500 (dyed)/optimized ARC	1.08	0.13
SPR 500/no ARC	severe notching	>0.4
SPR 500 (dyed)/no ARC	notching	>0.4

By employing optimized wafer track, contact baking and development, 0.6 line/space patterns have been successfully achieved as verified by actual etched metal probe results and the SEM cross section of Fig. 125. Metal lines from the process ranged between 0.5 and 0.6 μm due to process bias, but these

features were far below the limits established by previous studies.[171][188][191][192] Furthermore, the footed features which plagued the convection baking process have been eliminated. Metal snake yields using a 1.0 line/space pattern were determined to be 94.8%. Also, 90% snake yields using a 1.3 μm line/0.7 μm space were obtained.

In conclusion, the process optimization of an organic ARC has been accomplished and submicron feature capability demonstrated, as verified by electrical probe and SEM methods (see Fig. 126). The resulting optimized ARC example process is currently being employed to manufacture advanced BiCMOS and CMOS devices with submicron features. Note, that the same optimization methodology can be applied to any lithographic process such as the photoresist process, and this is usually done by the resist manufacturer to define a recommended baseline process prior to customer receipt.

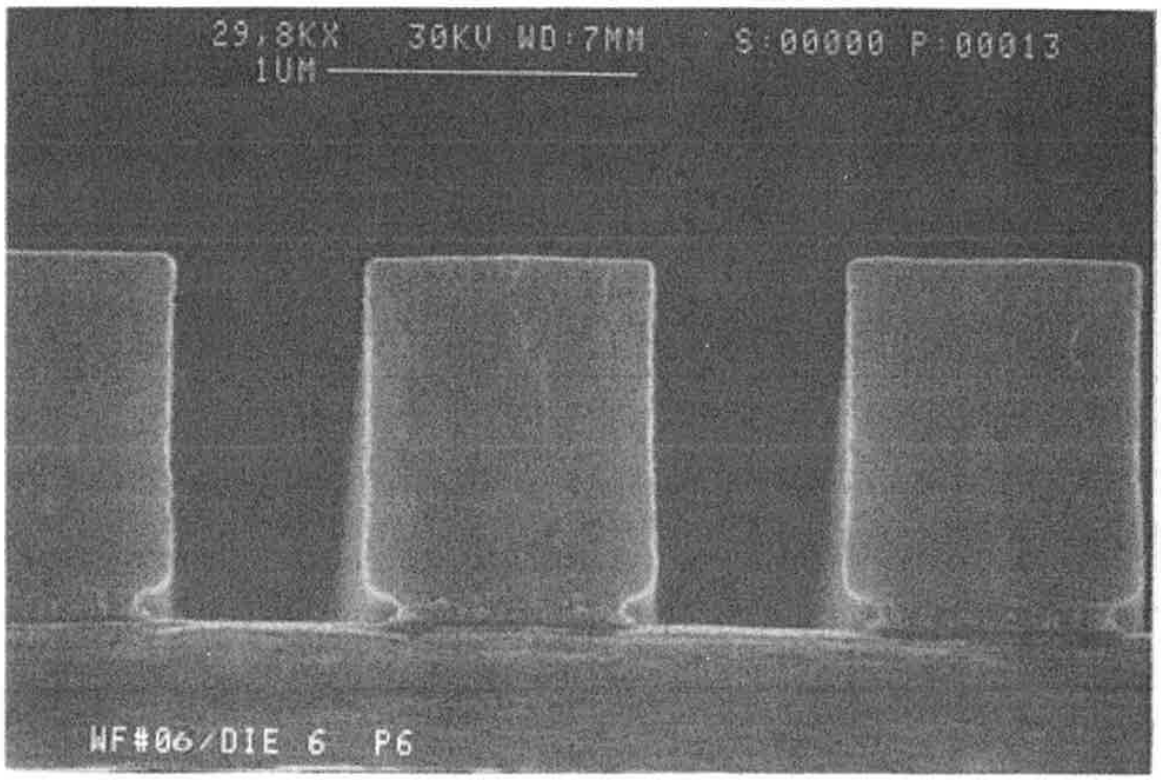


Figure 126. SEM cross section micrograph of immersion developed resist/ARC process on AlCu at 0.6 micron space resolution.

Resist Image ARC CD Control Advances—Inorganic ARC Design.[196] In photolithography, substrate and photoresist reflectivity variations introduce linewidth variations within-wafer or more importantly within the field. As feature sizes shrink below 0.35 μm, this variation goes beyond acceptable CD tolerances. To have an advanced CMOS process in manufacturing today, technology to dampen these reflections is necessary—"Without it, i-line gate lithography below 0.4 μm is not possible," said Dr. John Sturtevant, senior process engineer at Motorola (Austin, Texas).[196]

Work has continued in the area of i-line ARC bilayer processing from the work discussed earlier. A minor controversy developed as to whether organic (dry-developed) or inorganic ARC systems were best. Since both types of systems have been used in volume production, the decision boils down to what performance level is required and the COO. In the rest of this section, we will highlight the literature and present data for both systems with applications at the MOS gate level in mind. Remember that CD control at this level can determine logic or DRAM device performance and can translate to device manufacturing profitability as well (see Ch. 1).

As gate dimensions shrink from 0.5 to 0.1 micron, CD variation within the print field can be as large as 0.1 micron, or between 20–56% of the nominal CD. The reason CD control was observed for the ARC data presented in secs. 5.3.3 and 5.3.4 is because substrate reflectivity was controlled to ~10%, and for those somewhat larger CDs, adequate CD control was obtained. In Figs. 127 and 128, later swing curve suppression data for JSR 061 resist on silicon gate, or with the Si-rich nitride (SiRN) inorganic ARC, and the later generation, Brewer Science organic ARC XHRi are shown. If gate CDs had been plotted, they would have changed proportionately to that as for the E_0 variation shown. Note that varying degrees of suppression are obtained depending upon the ARC system employed (see Fig. 129 for percent suppression vs. ARC type).

Will Conley has outlined the important issues governing CD control at 0.25 micron CD and below.[198] Suppression of the swing in gate CD must be attained by controlling the gate surface reflectively to less than 0.5%; swing curve control to less than 1% must be achieved; greater conformality and less planarization from the ARC coating is desirable, which favors inorganic systems; better optical performance or operation at higher k_1 values is required, which again favors inorganic systems, and is desirable; and, enhanced defectivity and process integration compatibility must be maintained, which again favors the employment of inorganic ARCs. If one looks at the predominance of inorganic ARC device applications at 248 nm DUV, this may be the indicator signaling the application trend break to be occurring in favor of the inorganic ARC systems.

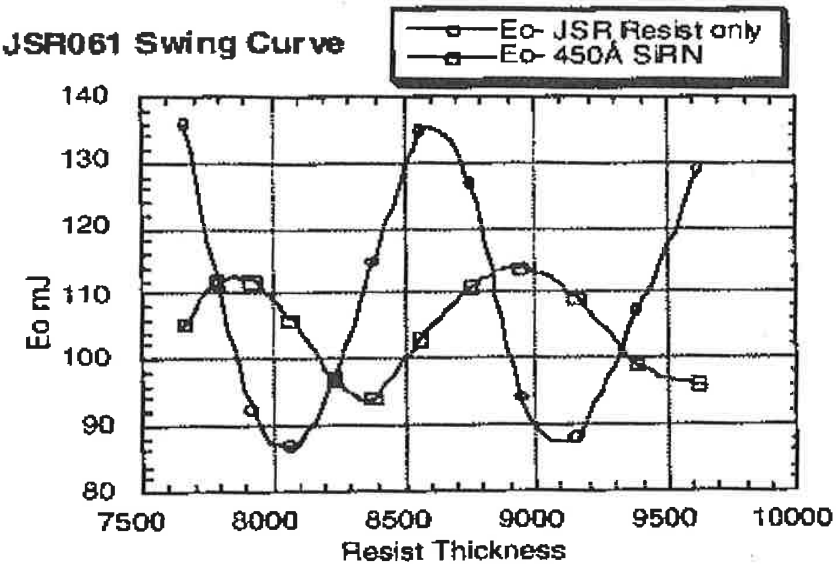


Figure 127. JSR 061 swing curve showing the suppression created by an Si-rich nitride ARC vs. no ARC. *(Data courtesy of Mike Brown of Motorola CS-2.)*

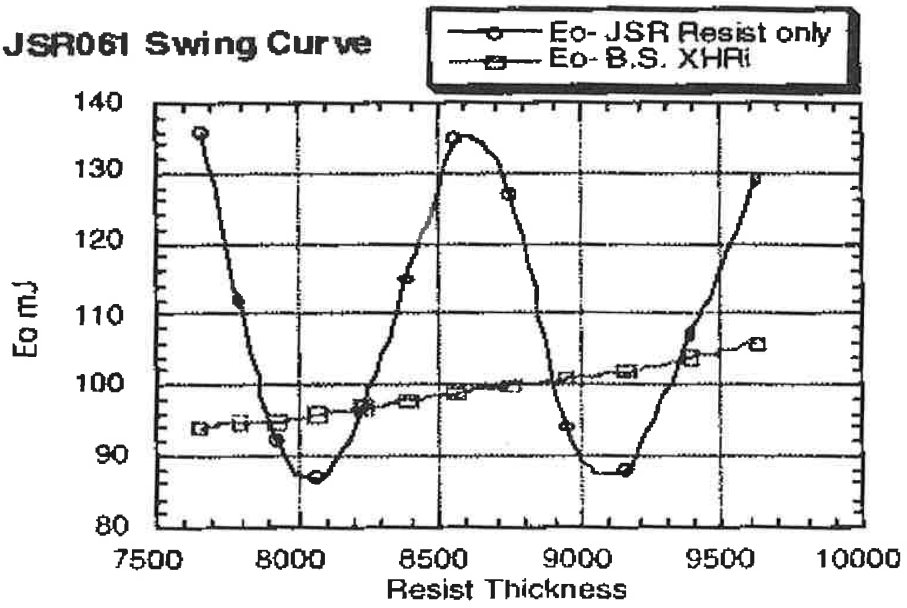


Figure 128. JSR 061 swing curve showing the suppression created by an organic ARC XHRi vs. no ARC. *(Data courtesy of Mike Brown of Motorola CS-2.)*

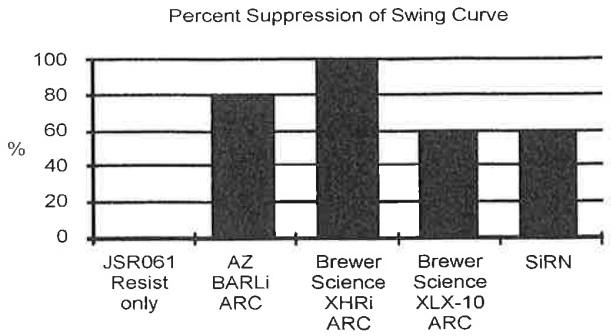
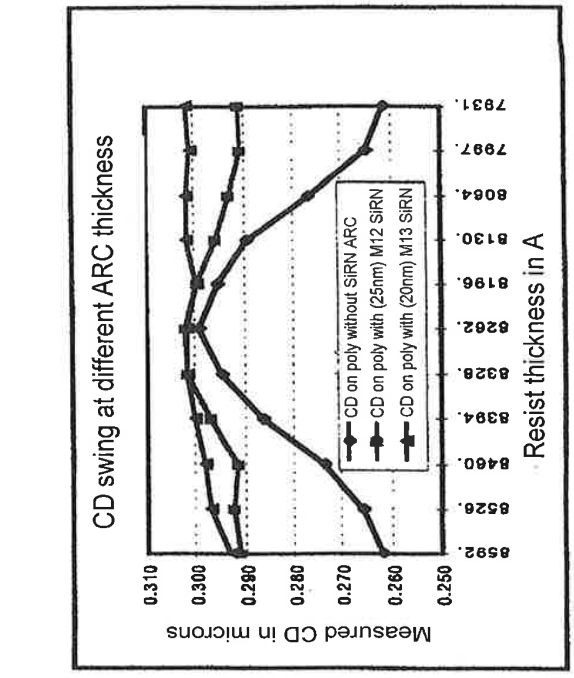


Figure 129. Swing curve suppression vs. ARC type. Notice also: all of the ARCs are effective at suppressing CD variation with the worst system providing 60% improvement.

Graca et al. have characterized the use of SiRN as an i-line and DUV ARC.[198] Although organic top anti-reflection coating (TARCs) have shown promise in reducing linewidth swings arising from thin film interference effects, they do not effectively eliminate the serious problem of localized exposures arising from reflective substrate topology; i.e., reflective notching. For this reason most efforts focus upon BARCs. Organic bottom antireflection coatings (BARCs) have been widely used to minimize these background reflections, and although effective, they have proven difficult to integrate and maintain low cost of ownership early on. More recently, however, novel, plasma-deposited, inorganic BARCs have been proposed for 365 nm and 248 nm lithography that appear to offer good control of critical gate patterning, easy integration, and cost effectiveness.

To understand the initial effectiveness of the deposited SiRN BARC, the simulation tool Prolith 2, a commercially available software, can be used to investigate the substrate reflectivity at various ARC film thickness. The simulation data shows 25 nm thick SiRN BARC works best for DUV reflectivity suppression, and 35 nm thick SiRN ARC is optimum or works best for i-line (see Fig. 130).[199] With the ARC thickness around 27 nms, less than 2% substrate reflectivity for 248 nm DUV should be obtained and less than 5% substrate reflectivity at i-line. The i-line characterization shows the E_o swing has been reduced from 24 mj to 10 mj, without an increase in E_o by using the SiRN ARC. The DUV data, at 248 nm, clearly indicates that a reduction of the CD swing from 40 nm to about 10 nm is achieved for a resist thickness change over a full swing cycle, by applying the SiRN ARC. Based on the measured optical properties of the SiRN ARC and the Prolith simulation results, the 25 nm ARC film is found to be optimal for DUV processing and it also provides a significant reduction of the substrate reflectivity for i-line process as well.[199]

Summary:					
	Thickness (+/- 3s) in nms	n @ 250 nm	K @ 250nm	n @365nm	K @365nm
Lot T27090	26.2 (+/-2.1)	2.3214	0.67126	2.4468	0.27719
Lot T27091	27.1 (+/-2.5)	2.3547	0.71477	2.5402	0.3338



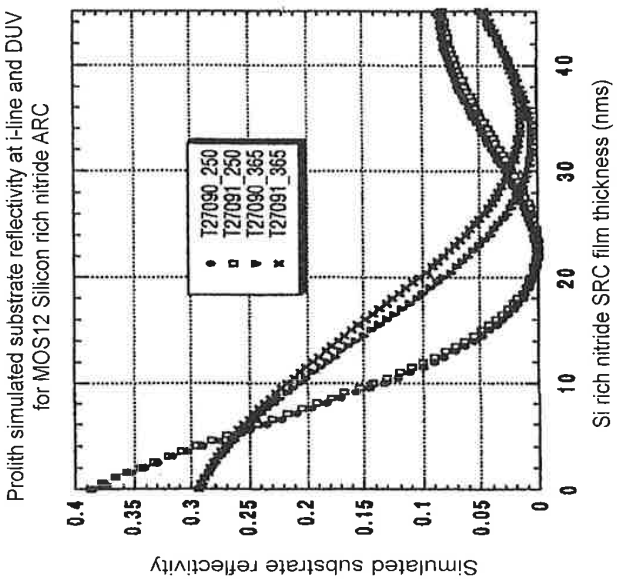


Figure 130. Gate polysilicon Prolith reflectivity simulations for Si-rich nitride (*left*) and CD swing data (*right*) for the respective ARC layers.

The optical film properties for both silicon-rich plasma enhanced nitride (PEN) and silicon-rich silicon oxynitride (SiON) ARCs have been established at advanced fabs for use as potential inorganic ARCs.[200] Additionally, the plasma ARC films render to the top resist process increased depth of focus and better resolution. With the installation of the Motorola APRDL 8" AMAT 5200 Centura™ system having the resistively heated DxZ™ chamber, development of the plasma ARC layers was further expanded beyond the Si-rich PEN system to include Si-rich silicon oxynitride. The primary advantage of inorganic BARCs is "pure optical performance," says Sturtevant of Motorola: "It's possible to tune these inorganic type films precisely to the optical properties needed."[197]

The key is a high k value approaching 1 which provides a greater tuning latitude. The k value, one of three parameters which determine substrate reflectivity, indicates optical density or film absorption.[201] The following parameters can be tuned by adjusting deposition temperature and pressure:

i. Real refractive index (n)

ii. Imaginary refractive index (k)

iii. Film thickness (t)

Inorganic AR coatings also provide the ability to conformally deposit from plasma over topography. This has meant better performance—performance which outweighs inconvenience, longer processing time and higher expense, according to Sturtevant. For DUV, Si_xN_y, and silicon oxynitrides have been used, and for i-line, TiN. In the 1997 timeframe, there were indications that inorganic BARC processing could easily be incorporated into the process flow, and this has proven to be the case. The further consideration is to fine-tune these optical films with a continuously changing refractive index from bottom to top of the AR coating layers to build a gradient effect. If n and k of ARC layers are perfectly matched to the adjacent layers, technically, there will be no reflections. The two interfaces at the substrate and at the photoresist, however, are typically very different in their refractive indices, and this is what gives rise to the large reflectivity. By placing a layer, in between that is well matched on the bottom to the substrate and on the top to the resist, may be very effective at reducing reflections, according to Sturtevant.

For manufacturing, inorganic coating technology is confronted with several issues. First, the parameters must be carefully controlled. Thickness and optical properties require tight control to minimize variations across the wafer and between wafer. Second, inorganic layers have chemistries similar to the underlying layer which can make removal difficult. However, some

companies are adapting ways to leave the layers in place and thus avoid removal. And third, in terms of capital, this process is more expensive. Although in-house equipment is typically used, to put it in-line means added cost and footprint to increase capacity. Dedicated production tools for inorganic plasma deposition are becoming available, such as Applied Materials' silane-based dielectric CVD. By eliminating ammonia from the plasma, this system can be used to deposit AR film which is compatible with DUV chemically assisted resists as well as with i-line.

Defectivity with organic BARC coatings is a process problem. Interfacial defects appear as small bubbles between the bottom organic AR coat and photoresist layers due to the surface tension mismatch. One way to eliminate them is by adjusting the photoresist or AR coating process. For BARCs, when the layer is spun on and the photoresist is then applied with a dynamic dispense at a minimum of 2500 rpm, the bubbles are thrown off. Interfacial defects have also been addressed chemically. By implementing chemistry to achieve better matching for the AR layer surface energy and photoresist, the need for special resist processes has essentially been eliminated in new BARC products.

The TFI effect may be reduced with a flatter wafer surface. Several processing techniques, such as chemical mechanical planarization (CMP), shallow trench isolation and dual damascene, are gaining interest as lithography tools as device features shrink below 0.35 μm. Some researchers have obtained reasonable process control and tight CD distributions in the face of small geometries and wafer topography—the only alternative to AR coatings is the elimination of topography, according to Johnson.

While ARCs have been used to enhance IC lithography for years, the CD budget allowed in advanced sub-0.35-μm lithography is placing more demands on them.[202] Design specifications of next-generation devices will require ARCs to *(a)* suppress greater than 99% of substrate-reflected light, *(b)* meet stringent photoresist and device contamination requirements, and *(c)* operate at extended ultraviolet wavelengths. Many of these requirements are not met by the conventional ARCs in production today.

During photolithography, light from the stepper is passed through a mask and the pattern is transferred to the wafer coated with photoresist. However, when the underlying film is highly reflective, as in metal and polysilicon layers, light reflections can destroy the pattern resolution by three mechanisms: *(a)* off-normal incident light can be reflected back through the resist that is intended to be masked; *(b)* incident light can be reflected off device features and expose "notches" in the resist; and *(c)* thin-film interference effects can lead

to linewidth variations when resist thickness changes are caused by wafer topology or non-flatness.

CVD-deposited dielectric ARCs work by phase-shift cancellation of specific wavelengths. This requires the simultaneous specification of three optical parameters: refractive index n, extinction coefficient k, and thickness d. Proper choice of these three parameters ensures that the transmitted wave that passes through the ARC film will, on reflection from the substrate, be equal in amplitude and opposite in phase to the wave reflected from the resist-ARC interface. In practice, phase cancellation requires very tight control of process parameters such that, for example, the thickness of the ARC is maintained to within 15Å. Conversely, CVD-deposited dielectric ARCs are thin (200–300 Å), conformal to device features, and usually very selective during the ARC etch, so that CD control is easily maintained during pattern transfer.

Typical simulation input variables include stepper parameters, mask pattern details, resist and developer types, and pre-and post exposure bake conditions. Of these parameters, only the wavelength, substrate film stack, and resist index of refraction are critical to the design of the dielectric ARC. These parameters will determine the substrate reflectivity, which can be minimized by adjusting the dielectric ARC optical constants n, k, and d. In the straightforward case of aluminum, neither the underlying film structures nor the aluminum film thickness plays a critical role, because the extinction coefficient of aluminum is high enough ($k = 2.35$–2.94 at 248 nm) so that any DUV will attenuate rapidly. The accurate predictions of resist profiles and CD control, however, require attention to all the input parameters. Second order effects, such as the angular distribution of substrate illumination, have not been considered in optimization of the ARC properties.

MLM Resist Issues. Total device layer to layer overlay is a complex situation, but to first order requires that the reticles stack well, the stepper alignment be good (i.e., three to four times smaller than the CD), and that the CDs for both layers are within specification. Even though the latter terms are usually the smallest terms, they can be large for poor processes and lead to poor circuit yield. Typically, CD control is specified at ±10% of the design rule or better. As of 1992, this requirement translates to approximately ±0.1 μm, 3-sigma, CD control for critical layers. In the late 90s, this budget has reduced by more than three times and some would argue that the 10% CD budget number is now more like ±8%.

MLM Metrology Calibration. (Also see Ch. 4.) To prevent resist image shorting of high density interconnects due to photolithographic bridging, the photolithographic metrology must have the ability to measure 10% of the

nominal CD and/or the nominal alignment tolerance ideally. The task then is to establish this type of gauge capability for both the CD and alignment measurement tools used to monitor MLM fabrication verification data. For example, the SPC capability of an Hitachi 7000 to measure 0.5 μm features in resist is between 20–30 nm, and the IVS ACV4 capability is between 20 and 33 nm, depending upon the MLM layer being measured. Clearly, these capabilities are larger than the 10% ideal target, but these numbers are probably adequate until newer metrology equipment can be developed or measurement methods or algorithms improved. Notice that at larger design rules, i.e., 0.8 μm CD/0.25 μm alignment, these capabilities are very adequate. At smaller features approaching 0.1 μm, SEM gauge capabilities must be of the order of a few nanometers, and modern SEMs do achieve these levels.

CDs are calibrated either electrically (see Fig. 131) or by SEM cross sections (i.e., the CD at the image base is referenced). The offset in Fig. 131, the difference between the electrical CD data and the Hitachi SEM data, is the sum of the RIE etch bias and the Hitachi bias. For metal layers, split cross bridge electrical structures are routinely used to calibrate either ADI or ACI CDs since they are absolute measurements. For via type structures, via resistance measurement for long via chains may be employed for calibration or electrical test structures recently developed by Lin can be employed.[203] More typically at via, SEM cross section calibrations are done. Here, metrology SEM measurements are typically compared to analytical SEM cross section measurements at 100,000X for the same features. Of course, the pitch for these patterns is well known to facilitate the calibration. Example MLM SEM cross sections for via and metal resist CDs are found in Figs. 132 and 133.

For alignment, electrical structures are also prevalent like those employed by Prometrix commercial electrical measurement systems, but these systems are hardly ever used on actual circuit reticles due to space issues, or if they are included, they are only found in PC cells. More typically, IVS or KLA optical alignment systems are employed to check alignment of product wafers during fabrication and those tools are SPC controlled vs. secondary standard wafers in a continuous mode as for all the other lithographic tools discussed previously.

Substrate Reflectivity Issues. Variations in wafer substrate film stacks can have a significant effect upon the resist critical dimension (CD) and exposure level for layers patterned to fabricate advanced four level metal BiCMOS MLM devices. In the fabrication of these VLSI devices, patterning is frequently performed on film stacks of varying thickness and optical properties.

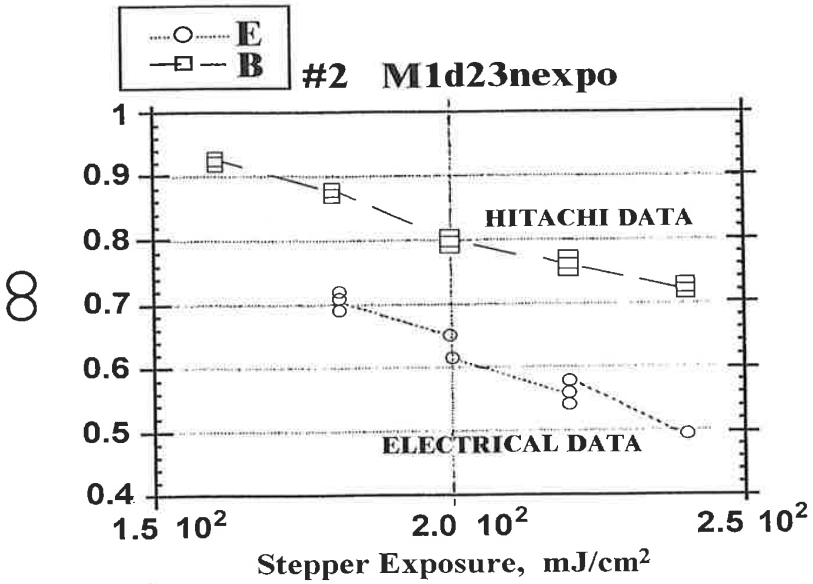


Figure 131. CD vs. stepper exposure for 0.6 micron metal 1 patterns illustrating CD calibration and the difference between SEM data and electrical probe data.

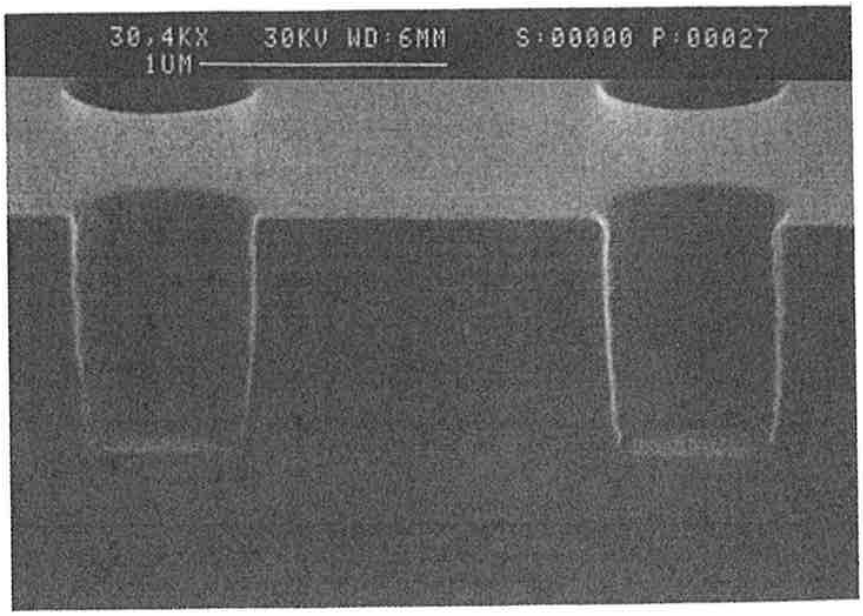


Figure 132. SEM cross section for a 0.6 micron via printed with a Canon 2000i1 stepper.

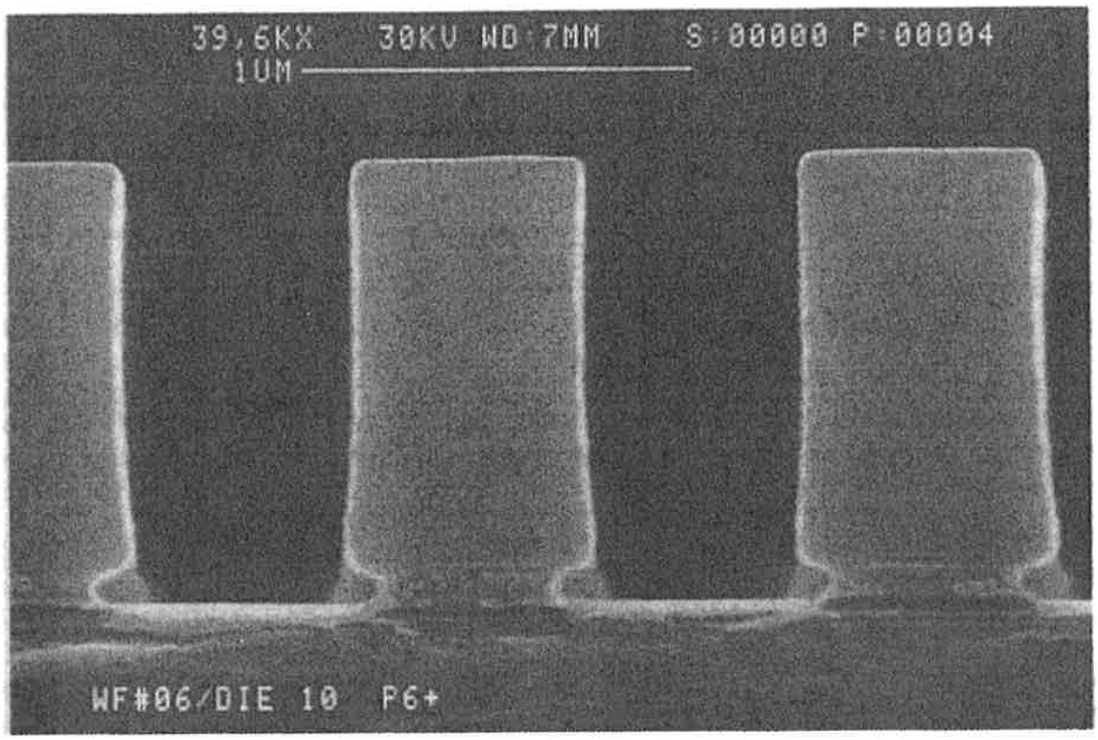


Figure 133. SEM cross section for a 0.6 micron metal 1 line on AlCu at 1.2 micron pitch printed with a Canon 2000i1 stepper.

PROLITH 2[204] can and has been used to simulate lithography behavior on actual device film stacks, and the results compare favorably to data collected from actual MLM product wafers. These simulations can be used to accurately predict the exposure changes needed to compensate for changes in film thickness and film stack upon CD. In most cases studied, less than 3% deviation between the experimental and simulated results is observed. Thin film reflectivity is also observed to have a strong influence on CD variation. The significant improvements in CD variation have been generally correlated with reductions and/or optimizations in substrate reflectivity. Electrical probe CD data for backend metal layers has also been evaluated for thin film notching behavior, and the CD variation is minimized by applying the results from PROLITH reflectivity analysis.

The constructive and destructive interference of light reflected from each film stack layer gives rise to reflectivity minima and maxima which can have an adverse effect on CD control.[205] Front-end and back-end CDs, printed under fixed processing conditions, can vary up from ±5–25% or a

large part of the usual CD variation budget due to film thickness and reflective notching effects. On metal layers, grain boundaries cause large local reflectivity variations which can cause notching (see Fig. 125).[159]

Brunner[206] has developed a simple analytical expression, based upon the Fabry-Perot Etalon optical model for thin film interference, which accurately predicts the effect of thin film interference upon CD behavior. This expression can be used to account for reflectivity effects upon resist CDs, and examples of reflectivity interference related peak to peak amplitude minimization for both resist top surface and substrate antireflective coatings have been demonstrated.[206] Furthermore, detailed example results for the latter case are provided here.

In this section, PROLITH 2 was used to simulate reflectivity and CD behavior on actual device film stacks and the results compared to data collected from product wafers. Results are described from a study of thin film lithographic effects in the fabrication of advanced BiCMOS devices employing Shipley System 9 (900 series resist in tables) or SPR 500, or JSR 500 high performance, resists. The TiW inorganic ARC films were sputter deposited and MRC films.

Results for Metal and Via MLM Layers. The film stack shown in Fig. 134 is representative of the layers encountered in BiCMOS and Bipolar devices at metal and via photo steps. The only difference between metal and via layers is the oxide thickness, 1.5 kÅ versus 7.5 kÅ. In this case, the aluminum-copper (AlCu) is sufficiently thick to behave as bulk Al which is opaque to the exposing wavelength. Hence, any layer lying beneath the Al layer can be ignored for the purposes of the reflectivity calculation. The PROLITH 2 simulations in Fig. 135 show how the substrate reflectivity varies with TiW thickness in the absence of an oxide overlayer; in Fig. 136 similar data for TiN deposited from a Varian metal system are also shown (Note: both metal cap systems are efficient at suppressing Al reflectivity taken as ~100% for the figure). It can be seen that TiW behaves as an inorganic antireflection coating, and can reduce the reflectivity (at 365 nm) of the underlying AlCu from 65% to less than 30%.

When an oxide and resist layer are present, the reflectivity behaves as shown in Fig. 137. Interference effects are responsible for the modulation in reflectivity with oxide and TiW layer thicknesses. At a fixed TiW thickness, variations in the oxide thickness can cause a 13% change in R (Note: The reflectivity changes from min. to max. when the oxide thickness changes by 1.25 kÅ). It is also easily noticed from Fig. 137 that ARC is a much more efficient reflectivity suppresser that TiW (i.e., see triangle data at bottom). The simulations in Fig. 137 (right hand photo) show that over

this reflectivity range a ±0.05 μm change in CD can occur. When the ARC is included, this CD change becomes more tolerable at ±0.03 μm and the impact of the interference effects are effectively minimized.

The theoretical reflectivity curve in Fig. 138 shows that ARC-XLT can reduce the AlCu reflectivity to below 10%. When used in conjunction with TiW, the overall reflectivity and modulation is reduced significantly as shown in the right hand curve in Fig. 137. Figure 139 shows there is good agreement between theoretical and experimental results.

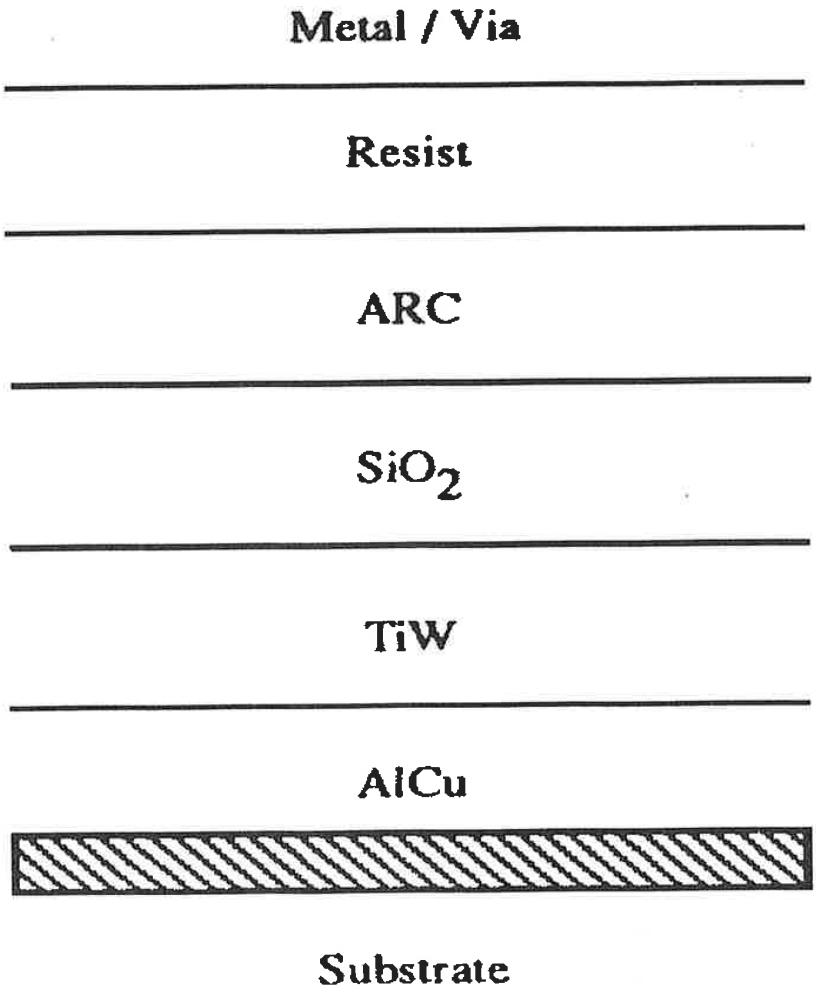


Figure 134. Film stack of BICMOS and Bipolar devices at metal and via photo steps.

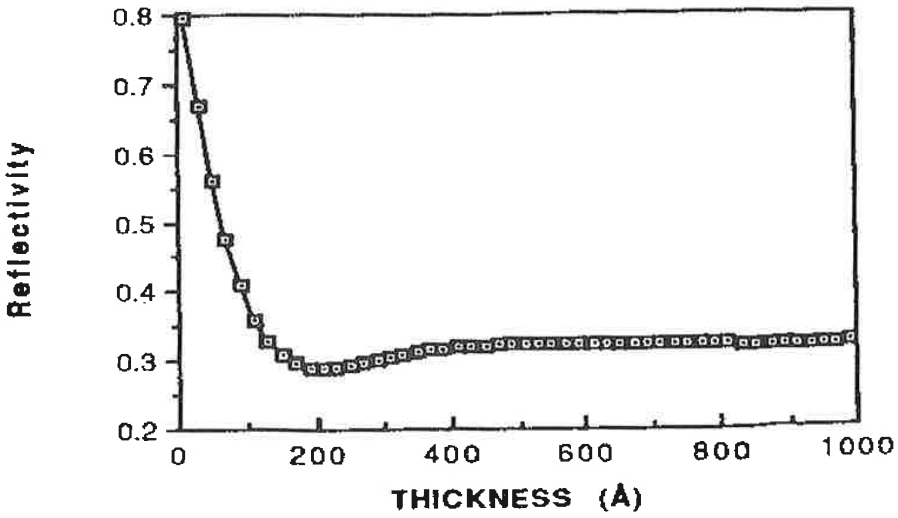


Figure 135. Dependence of reflectivity on TiW thickness. Substrate is 6.5 kÅ AlCu on silicon.

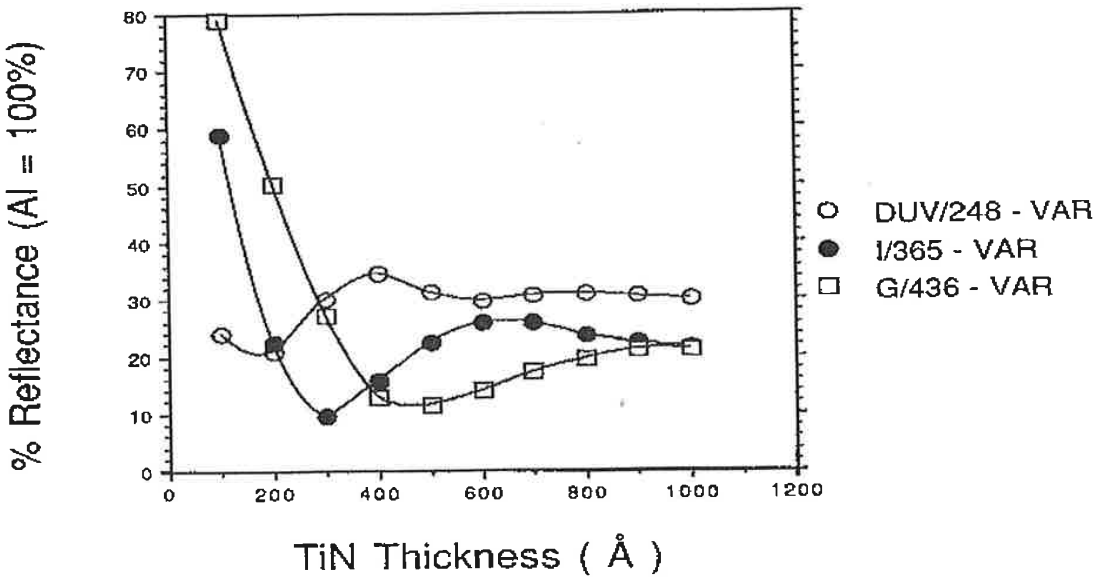


Figure 136. Dependence of reflectivity on TiN thickness.

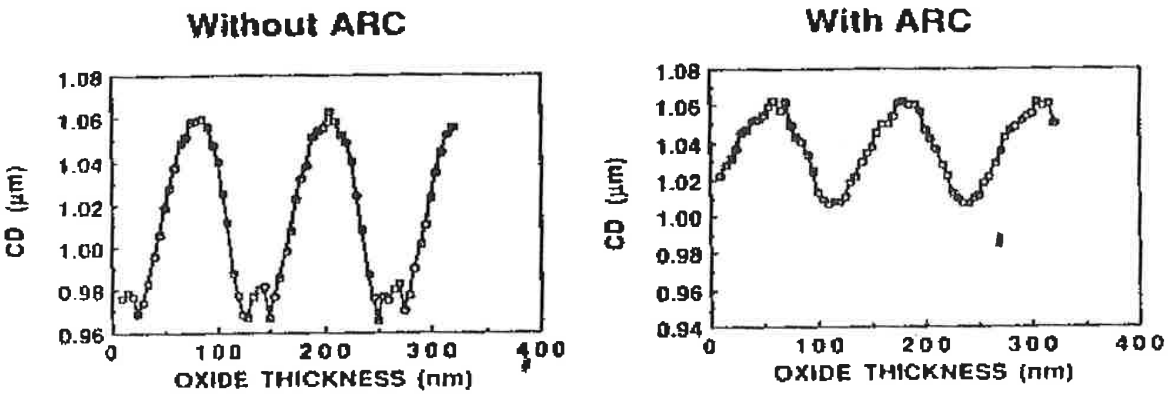


Figure 137. Effect of oxide thickness on CD variation film stack is resist/oxide/TiW/6.5 Å AlCu.

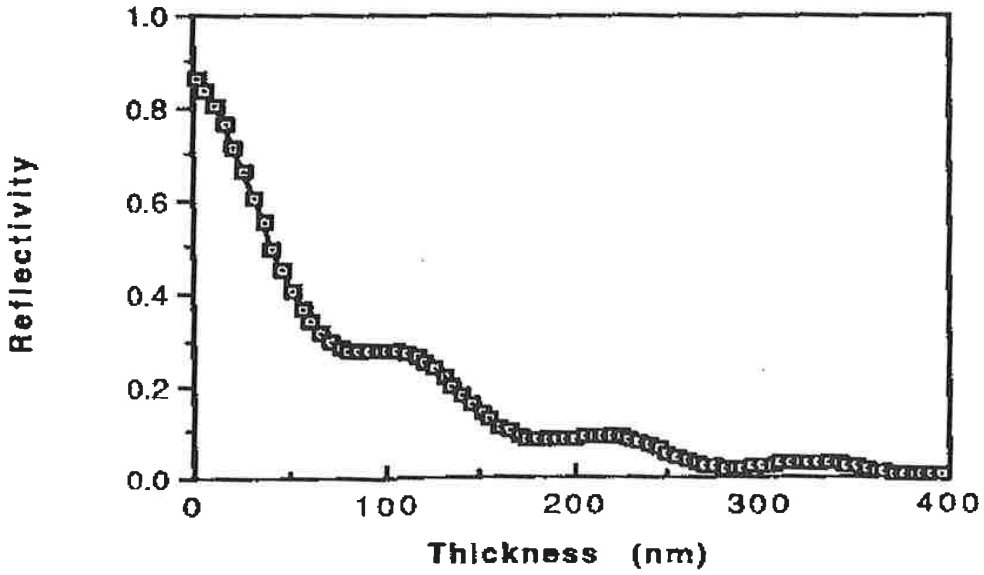


Figure 138. Dependence of reflectivity on ARC-XLT thickness. Substrate is 6.5 kÅ AlCu on silicon.

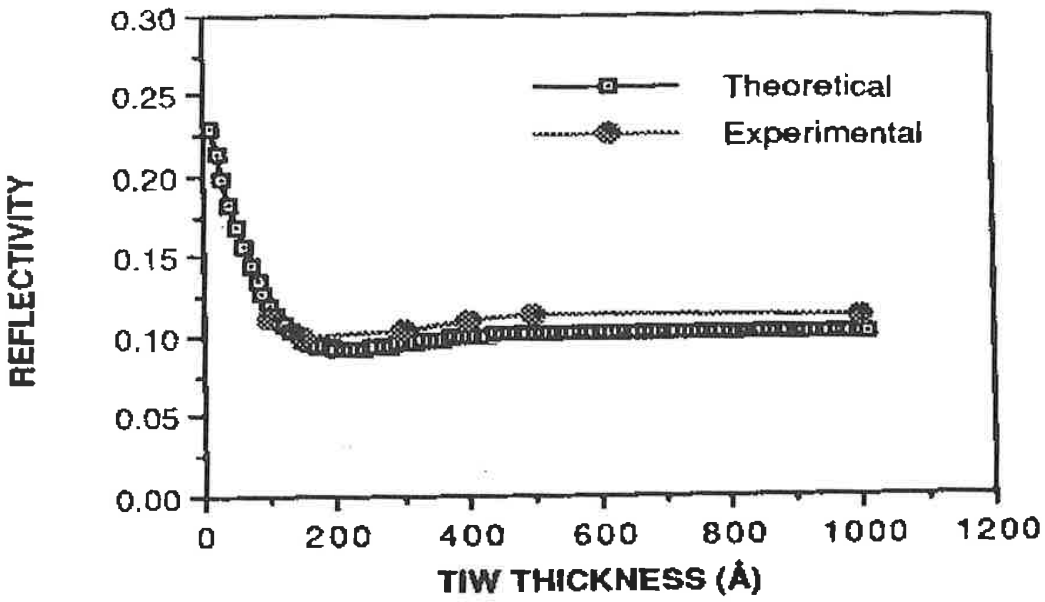


Figure 139. Comparison of experimental vs. theoretical reflectivity; film stack is resist/ARC/oxide/TiW/AlCu.

The data shown in Table 24 demonstrates the effect of reflectivity on via CD control. In via patterning experiments, vias printed with only resist exhibited high CD variation (~0.25 μm, 3-σ) due to substrate reflectivity and reflective notching. Actually, larger CD variation (greater than 0.30 μm) has been observed on live product depending upon the lot. In an extensive multivari experiment with notching and non-notching lots, almost the entire via CD variation was attributed to the presence of grain boundaries in the underlying metal. The use of a higher performance Shipley dyed resist (510L) did not improve the CD variation. When an optimized ARC was used in conjunction with the resist, CD variation dropped by 35% for the Shipley 915 dyed resist process and notching was minimized. By using 510L which is a higher contrast dyed resist, 0.11 μm, 3-σ, variation was obtained. The significant improvement in CD variation observed with ARC and 510L/ARC has been correlated with the reduction and optimization of substrate reflectivity.

Table 24. Mean CD and Total CD Variation for Via MLM Patterning

Resist Systems	CD Mean	Std. Dev. (3-σ)
915(no ARC)*	1.09 μm	0.24 μm**
510L(no ARC)***	0.97	0.26
915/ARC	0.94	0.15
510L/ARC	0.93	0.11

* Shipley dyed resist for I-line.

** Significant amount of notching appears without ARC. Values can be as high as 0.30 μm.

*** Shipley positive resist generation after 900 series. L means dyed material.

The results of linewidth experiments on metal substrates are show in Table 25. Wafers patterned only with 915 resist showed waviness and notching which contributed to poor linewidth control (0.22 μm, 3-σ). Similar to the via results described above, the addition of ARC reduced CD variation by 40% and minimized the effect of notching. Our CD control target of ±0.1 μm was exceeded using 511 + ARC.

Table 25. Mean CD and Total CD Variation for Metal 1 MLM Patterning

Resist Systems	CD Mean	Std. Dev. (3-σ)
915(no ARC)*	1.31 μm	0.22 μm
915/ARC	1.33	0.12
511/ARC**	1.28	0.09

* Shipley dyed resist for I-line.

** Shipley undyed positive resist generation after 900 series.

Thin film reflectivity has been demonstrated to be a major issue in MLM lithography and has been shown to have a strong influence on device CDs, level exposures, and CD variation. 0.09 and 0.11 μm, 3 σ, CD control can be achieved on difficult metal and via layers, respectively. The significant improvement, i.e., reduction in CD variation, has been correlated with a reduction and optimization of substrate reflectivity, consistent with the work of Brunner.[206] In patterning the highly reflective layers encountered in BiCMOS backends, the use of a high contrast resist in conjunction with ARC-XLT can significantly improve CD variation by reducing the effect of substrate reflectivity. This bilayer process effectively suppresses the effects of reflective notching and interference swing contributions to CD variation below that allowed by device design CD tolerance levels. An undyed resist/ARC process is currently employed in patterning metal layers where ±0.10 μm or better CD control is required for device yield.

Process Biasing. Metal features are usually biased larger than their design to allow for size erosion during fairly harsh etch processes (see Sec. 5). Older resists used to fabricate mature devices require at least +0.2 μm bias (i.e., here, total bias for both image sides is used) be added to achieve the required resist image CD before etch processing. For some very old processes, biases as large as 0.5 μm have even been employed, but these were for fairly isotropic etch processes and much lower contrast resists.

Today's resist processes are higher contrast materials and photo biases are now zero or near zero, i.e., the chromium image from the reticle is printed divided by the reduction ratio of the tool. Metal etch biases may still be ~0.1 μm, but they too are being reduced through improved processing and by implementing next-generation single wafer etchers (for example, Applied Materials 5000 etchers). Via images were typically biased to be undersized so that greater CD control could be achieved through greater exposures. Recently, however, processes have been improved so substantially that truly zero bias processes are now achievable for both photo and etch biasing. Typical biases for older via/contact processes were of the order -0.2 to -0.3 μm, but it is fairly apparent that for next-generation dense circuits near-zero photo and etch biases are required.

DOF Budget and Focus Offsets. To successfully print MLM features, the wafer field must stay within a certain focus range or patterns may be missing in parts of the die or print field. The resist image DOF as shown in Figs. 140 and 141 must be wider than the DOF budget determined by summing wafer, lens, and reticle/pellicle budget contributions.[207] Table 26 contains an example budget for a 0.5 μm metal 2 or via 1 processes. Since the DOF window data

of Fig. 140 is greater than this budget, the metal 1 patterns should print across the field with fidelity with an estimated 0.7 μm surplus tolerance. Note, that the budget may be somewhat smaller or better for via layers because they are all printed to a single metal plane determined by the metal thickness and they are small square images that do not extend over great lengths as metal line interconnects do. The metal 3 budget may be slightly worse because two layers of planarization errors must be budgeted for instead of just the one contributor encountered at metal 2. Similarly, there may be a frontend topographical contributions that deminish the budget at metal 1, but overall the budget estimates should all be less than the resist process DOF. This has been verified on MLM wafer line monitors, i.e., greater than 95% metal snake yields have been routinely achieved with the example DOF budget estimates.

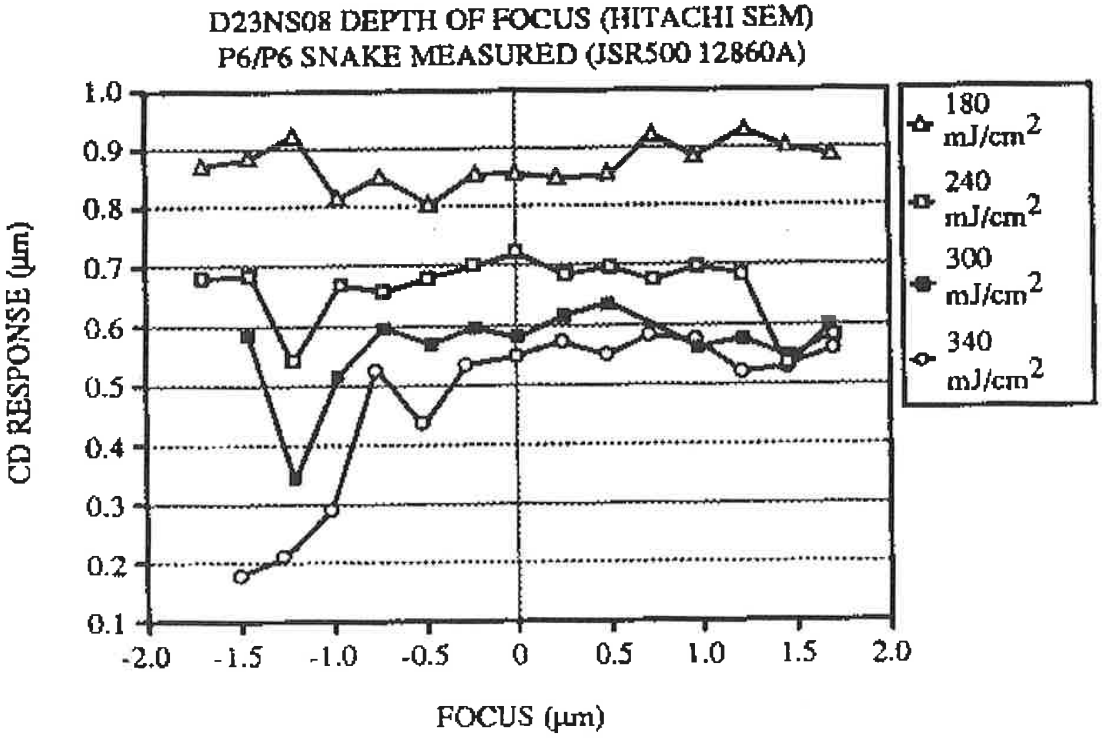


Figure 140. Metal 1 CD vs. defocus for the JSR 500/ARC process.

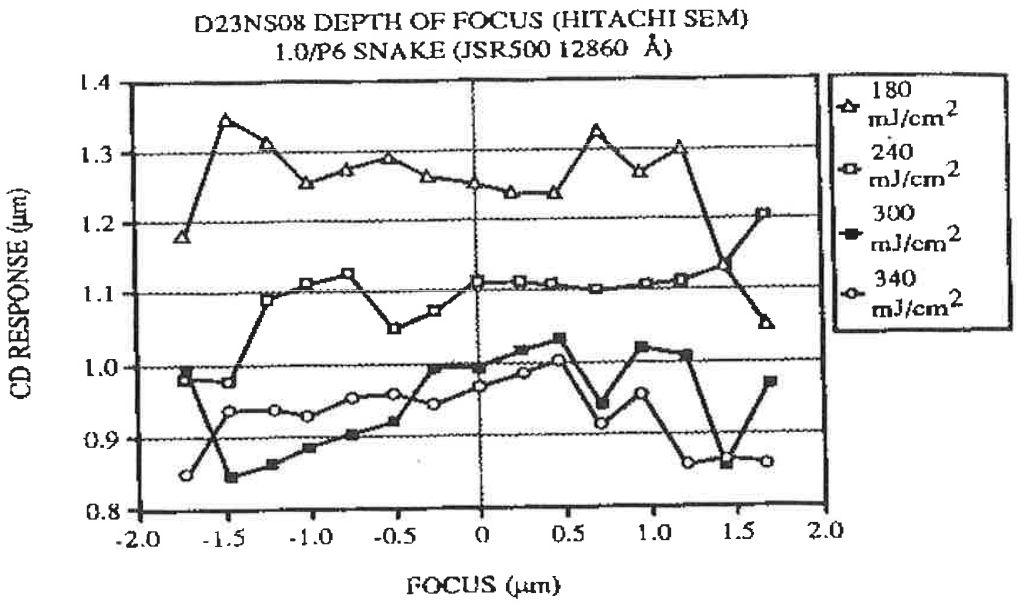


Figure 141. Metal 1 CD vs. defocus or the JSR 500/ARC process with -0.6 micron focus offset.

Table 26. DOF Budget for 5X Canon 2000i with N-layer Planarization at Metal 2 or Via 1

Contributor	3-sigma Contribution
Lens Field Curvature	0.4 µm
Focus Repeatability	0.1
Field Leveling Repeatability	0.15
Reticle Flatness, etc.	0.1[a]
Wafer LTIR	0.5
Residual Planarity topography[b]	0.3[c]
Total DOF =	1.55 µm[d]

[a] B. J. Lin, Ref 62.

[b] Doubles at Metal 3.

[c] Contribution may be closer to 0.1 µm since the vias all land on metal of the same thickness.

[d] At M1 approx. the same DOF, but at M3 the DOF is ≈ 1.8 µm

Figures 140 and 141 are referenced to demonstrate another principle governing MLM requirements, that is, focus offsets may and usually are required. They are required primarily because the effective thickness of the resist must be corrected for the refractive index of the resist (~1.5); as a result, negative offsets for most layers range from -0.3 μm to -0.6 μm. The offset centers the defocus CD data at machine zero so that wafer flatness or other errors, which can be as large as 0.5 μm and as great as several microns at edge die of severely distorted wafers, do not create a yo-yo effect where the wafer CDs move up and down the steeply varying CD vs. defocus curve on the negative side of defocus. From Fig. 140, it is apparent that without an defocus offset, probably half of the optical fields will be precariously near the CD cliff edge (left hand side of Fig. 141) with little process tolerance or margin available.

MLM Planarization Processes. The DOF budgets for many new devices are very tight, especially those at DUV R&D facilities where the DOF of the resist/tools are currently ~1 μm TIR. Additionally, wafer flatness on an exposure field basis, termed local total indicated range (LTIR), can be much greater than the 0.5 μm usually budgeted for wafer flatness and can have values as high as several microns. Without planarizing steps between metal layers to achieve some degree of global planarization, the topography alone can be as great as 2–3 μms. Obviously, employing advanced four or five level MLM processing dictates some sort of planarization processing from first level ILD to fourth or fifth level metal or the stepper images needed to be printed at third via or third metal will probably be out of focus and not print with fidelity.

The three processes in current development[208] are Chemical Mechanical Polishing (CMP), and two different 2-layer etchback techniques, I-layer or negative blocked 2-layer[208][209] and N-layer, termed positive resist 2-layer blocked.[210][211] The last technique will be discussed here because it is probably the most mature process from a defectivity point of view and experience with it is extensive.[210] The first two processes provide better global planarity, but require equipment development and negative resist development, respectively. IBM researchers have also reported using both N-layer and CMP together to achieve excellent global and local layer planarization.[212]

Two-Layer Photo Planarization Process. The conventional POT process,[210] i.e., where the dielectric layer is planarized by the application of one sacrificial layer followed by an etchback of that layer, is always considered first as a leading candidate for the planarization of any device MLM backend due to its simplicity. However, it is hampered by the fact that conventional, commercially available organic materials and spin-on glasses

can only planarize underlying features up to a finite distance from the edge of the feature, and neither group of materials is capable of more than step rounding or smoothing in reality. This distance is approximately 10–20 μm, and is known as the planarization length. Thus, for large, greater than 20 μm isolated features separated by more than 20 μm such as bonding pads, etc., the degree of planarization achieved with conventional materials spun to workable thicknesses (less than≈2 μm) decreases dramatically, to the point where there will be vast numbers of features on typical circuitry left completely unplanarized. For these types of structures, the only thing gained using conventional POT processing is simple rounding of the edges, which does improve things by helping maintain metal line continuity over steps and by eliminating shorting bars or picket fences during metal etch at those locations.

The Two Layer Photo (TLP) process has been described in the literature[213]–[215] as a means, through the use of an extra masking step per ILD layer, to overcome the shortcomings of conventional POT and provide nearly perfect dielectric planarization independent of underlying topology. Figure 142 *a-f* describes the method. After the given metal layer is etched, the initial TEOS layer is deposited. In the standard POT process, the sacrificial organic would be spun on at this point, giving a large variation in the vertical altitude of the organic surface due to the dependence of the planarizing ability of the coated layer on the dimensions of the underlying topography.[216][217] This problem becomes more severe as feature sizes continue to shrink. With the TLP process, the problem of global planarization is lessened substantially by the use of the additional masking step. A photoresist layer is spun onto the structure (Fig. 142*b*), and is patterned with a mask that is roughly an inverse image of the underlying metal pattern (Fig. 142*c*). This leaves resist in the field areas between the metal lines, effectively plugging these areas and planarizing the structure. In order to achieve planarity, the thickness of this resist layer (known as an "N-layer") must be equal to that of the step height, which is the sum of the metal thickness and the degree of overetch into the underlying glass layer during the metal etch step.

The N-layer is not an exact reverse image of the underlying metal because of several reasons. First, the TEOS deposited onto the sides of the etched metal steps effectively widens the features by an amount equal to 60% of the deposited glass thickness, independent of feature size. Second, there is a limit to how small the N-layer "plugs" can be made. Since patterning resist layers planarize small gaps fairly well without TLP and adhesion and overcoat compatibility concerns exist for small N-layer images, n-layer plugs are usually larger than the lower limit of 1–2.0 μm. Finally, alignment tolerance comes into play. This tolerance is aligner

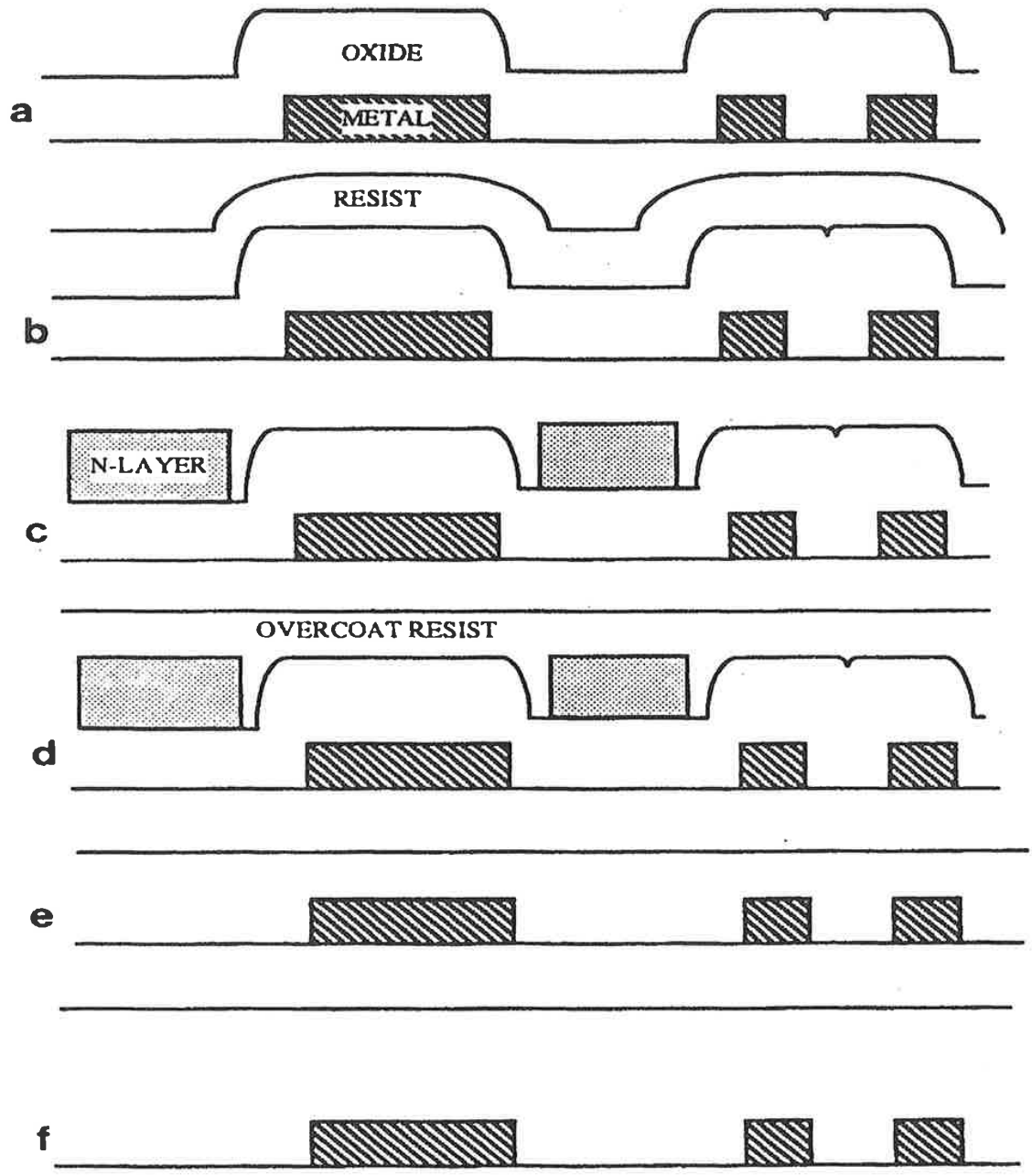


Figure 142. (*a*) Structure after metal etch and initial TEOS deposition. (*b*) After N-layer resist spin. (*c*) After N-layer patterning. (*d*) After overcoat and resist spin. (*e*) After etchback planarization. (*f*) After TEOS redeposition.

specific, but is typically set to be ≤ 0.25 μm, meaning that there is a nominal 0.25 μm or smaller gap between the edge of the glass and the edge of the N-layer plug. This is necessary because if the tolerance is made too tight, normal misalignments could result in full-thickness N-layer structures ending up on top of features, to the detriment of surface planarity. Thus, areas on the circuit with gaps between glass sidewalls smaller than $1 + (0.25 \times 2) = 1.5$ μm will not get plugged. For any thickness (ILD_t) used for the initial TEOS deposition for first ILD, the areas with a gap between neighboring metal features of size N_{min} of less than

Eq. (7) $$\text{Max unplugged dim.} = N_{min} + 2 \times (ILD_t \times \text{sidewall coverage})$$

will not be plugged. For future generations of back end product, the adhesion and alignment tolerances will be tightened, resulting in a larger percentage of the circuit getting N-layer plugs and n-layer plugs as small as 0.5 μm may be easily obtained.

After the N-layer feature has been patterned, the wafers are coated with another organic layer which is similar to the sacrificial organic used in the POT process. A typical thickness of this organic layer is about 8500 Åfor all three ILD's, but thinner layers of the order of 0.3 μm are more attractive for etchback time reduction reasons and films this thin are still capable of the misalignment gap filling required. A thinner resist overcoat is attractive out of concern for the overall nonuniformity of the glass thickness after etchback planarization. The thicker the resist/TEOS stack, the larger the magnitude of thickness variation after the etch, assuming the percent nonuniformity remains constant as a function of stack thickness. Its only purpose is to fill in the gaps that the N-layer has not plugged due to the photolithographic alignment considerations (Fig. 142*d*). The overcoat layer does not have to be photo sensitive and should not be for cost reduction reasons.

Great care must be taken in the treatment of the wafers after completion of the N-layer patterning before the overcoat layer is spun. The N-layer resist must be either baked to high temperatures[209] or deep UV cured to prevent dissolution of the bottom N-layer resist images. If this N-layer image insolubility process does not occur, planarization of the surface will not occur due to dissolution of that layer at the overcoat step. Deep UV curing has been reported[214] to be a necessary component of the TLP process, and is used extensively. A high temperature bake will accomplish the same purpose, but temperatures high enough to prevent image dissolution (greater than 160°C) will also cause greater shrinkage of the N-layer resist to leave larger gaps. Because this shrinkage occurs to the same degree

in all directions, a gap of several microns can open up between the edge of the N-layer plug and the edge of the glass. For this reason lower temperature baking followed by a deep UV cure is the recommended process. Others have used a layer of sputtered quartz to separate the two resist layers, but the deep UV cure is a simpler technique, without the added deposition and has been demonstrated to work well.[210]

The example n-layer process depicted is the result of three basic experiments. First, the temperature where n-layer image shrinkage was zero or as small as possible to prevent pattern pull away and film stress needed to be determined. Next, the early literature was unclear as to whether DUV curing, high temperature curing, or both were necessary or what order was essential for n-layer double coating. By doing the experiments of Figs. 143 and 144, it was determined that DUV was required and that it should occur after baking. Furthermore, baking before DUV is necessary to prevent "eyelash" defects from forming around the n-layer image edges as shown in the Fig. 145. "Eyelash" images will transfer to the underlying TEOS layer during etchback and there is a considerable amount of deleterious topography associated with them, so they must be avoided. Any photoresist can be used for the n-layer process; in fact, at least four different resists have been successfully tested. Images for all of these resists are rendered insoluble to the planarization overcoat before etchback by the 120°C baking followed by the several hundred mJ/cm^2 DUV cure/exposure.

Early on, there was concern about the limitation of the N-layer resist's ability to fill the narrowest crevice left in the glass after initial TEOS deposition. This problem never materialized, however, and the resist overcoat easily fills gaps of approximately 1500 Å without leaving voids. Any gaps that the resist does not fill should be plugged by the TEOS redeposition. After the overcoat layer is spun on, it is also important not to overbake the wafers, as excessive temperatures cause layer "bubbling," which causes a phenomenon to occur near the boundary between N-layer plugs and glass edges reminiscent of localized resist reticulation. This problem becomes more severe as the metal thickness increases, which can cause local N-layer build up. The cause of this problem is believed to be due to excessive volatile product build up in the film that cannot escape quick enough as for thinner film regions. This is a common DUV curing problem as resist thicknesses are increased.

The resist/TEOS sandwich is next etched back to within some targeted distance above the top of the metal using a chemistry that etches resist and TEOS at roughly the same rate (Fig. 142*e*), and then another TEOS deposition brings the final ILD thickness up to the specified target (Fig. 142*f*).

A great deal of discussion has transpired regarding the need for the complex processing associated with the TLP N-layer technique. Until other techniques such as CMP are established in volume production as cost effective, (note: in the 1990s this occurred) TLP process will be employed extensively, at least in R&D fabs doing advanced MLM processing.

N LEVEL FACTORIAL ANALYSIS

	NO DUV		DUV	
	120°C	160°C	120°C	160°C
5214	NO PATTERNS 15500	SOME PATTERNS 28600	PATTERNS 27600	PATTERNS 28000
910	NO PATTERNS 12900	SOME PATTERNS 15100	PATTERNS 26200	PATTERNS 25700

ONLY SIGNIFICANT VARIABLE IS RESIST

Figure 143. N-layer 3-factor factorial analysis results to determine the minimum full thickness process required to prevent N-layer dissolution at the overcoat planarization process.

FACTORIAL ANALYSIS

N LEVEL TREATMENT

OVERCOAT BAKE TEMP	DUV FIRST		DUV LAST	
	120°C	140°C	120°C	140°C
120°C	E, E	R, R		
140°C	R, R	R, R	E, E	

E = EYELASHES
R = RETICULATION
(ALSO HAVE EYELASHES)

Figure 144. 3-factor factorial results of the experiment designed to determine the processing conditions that prevent the "eyelash" problem. Note: no eyelash cells to the right.

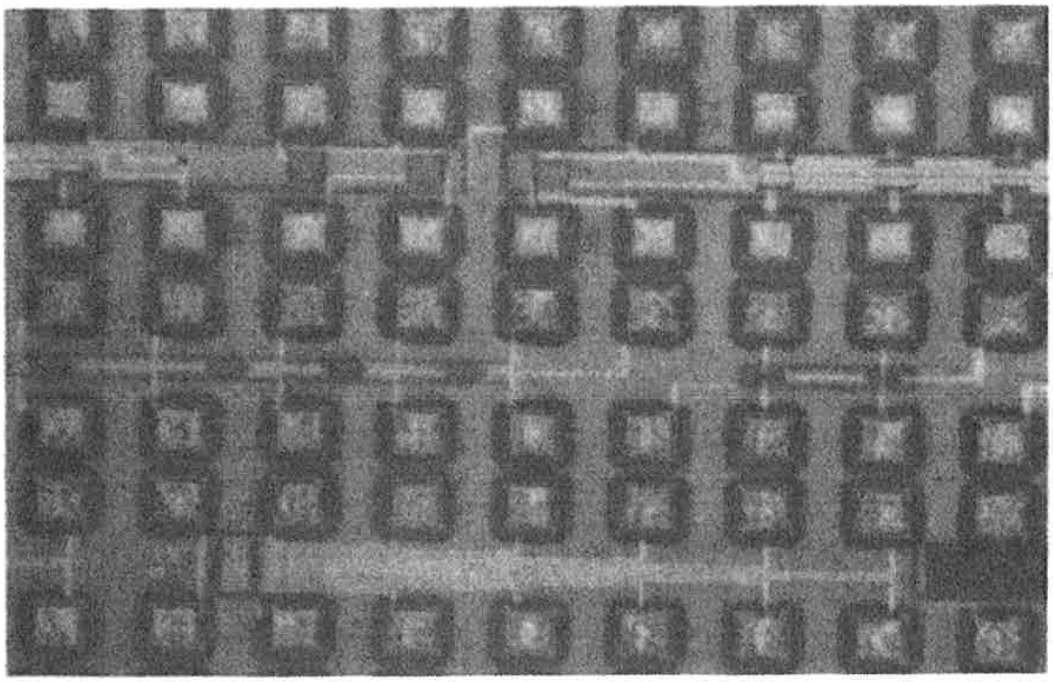


Figure 145. Optical micrograph illustrating the "eyelash" problem of improperly processed N-layer images around MLM bonding pads.

Alternate Processes to TLP Etchback. There has also been an ongoing effort to investigate the claims of several photoresist vendors of the perfection of materials giving far better planarization lengths than today's resists. At this writing, impressive degrees of planarization (in excess of 80%) have been achieved with some of these materials such as Futterex PC2-1500.[208] Problems remain with purity and stability, however. It is hoped that use of these materials in the simpler POT-like process will be a viable alternative to N-layer processing in the near future.

Of course, this type of single layer process would require an organic material capable of planarizing substantially large pads, 100 microns square and isolated. A careful survey of the literature turned up several ideas, some involving multiple layers and various processing sequences. These were all tested, the results of which are found in Table 27. The results of the table clearly indicate a lack of planarization for large feature geometries and a large discrepancy between the degree of planarization between center and edge of the test wafers. Even though this center to edge phenomena is not well understood, the results are also not acceptable, because the maximum planarization value observed was only 27%.

Table 27. Planarization Measurements for Literature Systems Before 1988

Organic Systems	Planarization* at Wafer Center, %	Planarization* at Wafer Edge, %
SINGLE LAYER SYSTEMS		
OCG WX-214(Special Spin)**	1.8	24.2
OCG WX-214(Std. spin)	~0	18.5
Polystyrene	0	8.5
TLS(Polysiloxane)	3.1	23.6
FUTTEREX (early version)	~0	19.1
BILAYER SYSTEMS		
OCG WX-214/OFPR-800***	~0	25.4
OCG WX-214/OFPR-800	~0	21.7
Polystyrene/OFPR-800(180 C)	~0	26.8
OFPR-800/Polyvinyl alcohol	~0	26.8
OFPR-800/Polyacrylic acid	1.5	19.3

* Calculated from P=100X (Pad Step Ht.- Meas. Step Ht. at Coat)/Pad Step Ht.

** Special spin has a very short spin of a few seconds and the wafer drys with the chuck stationary not spinning as for Std. WX-214 is a standard photoresist.

*** Dynachem standard photoresist.

Stillwagen[217][219] was also aware of these limitations, and was able to formulate a series of polymeric compounds which were capable of planarization due to highly viscous flow and long spin times. Unfortunately, these compounds are not practical for use to the electronics industry, but they did demonstrate satisfactory planarization could be achieved and provide an existence proof of that. Since that work, several polymer systems have been developed by OCG and Futterex, which are capable of thermal flow after coating followed by thermally induced crosslinking reactions to harden them. This creates planarity over 1 micron topography of up to 70–90%

for Hunt and Futterex test materials, respectively. The later data occurred for 200°C cures, and should be adequate for initial POT process experiments without N-layer lithographic steps. Even though these advances are impressive, it appears that CMP research has won out over the long term and these POT like processes have faded away.

Via Layer Processing. Via layer images of an MLM process are square small contact geometries and allow the layers of metal to be connected at specific sites. So, for every layer of metal there is a via level which follows it, including even the last layer of metal which must be contacted through passivation dielectric in order to place the chip into a package. The via imagesare printed usually on a TEOS oxide or any type of insulating dielectric layer, then transferred into the dielectric to the lower metal surface using RIE as in Sec. 3.

Via Layer CD Control. The issues for via CD control are very similar to those for metal layers, i.e., reflectivity, focus, and exposure. As for metal layers, image focus can be very important. In Figs. 146 and 147, the importance of putting in a focus offset to center the CD vs. the range of defocus data is demonstrated. Without an offset, the process is performed precipitously close to the right hand data of Fig. 146 which is going out of CD control quickly at less than 1 μm of positive defocus (see 370 and 420 mJ/cm^2 data). The CD spec is 0.5 ±0.1 μm and notice there is an interaction of exposure and defocus at large minus and positive defocus values. By working at the machine defocus of zero from Fig. 146, if any thing happens across the wafer or the print field, the data will go out of specification quickly. In comparison the data of Fig. 147 is better centered at zero machine focus after putting in the -0.7 μm offset and now any changes that occur up to ±1.4 μm in local field planarity will have only a minimal effect on the via CD. Notice, that this empirically determined offset value is very close to the theoretical value you would calculate to compensate DOF for resist thickness,[207] the resist thickness 1.28 kÅ divided by the refractive index of 1.6 or -0.8 μm. The data of both figures also allows the etch bias of this example process to be estimated to be about +0.05 μm, i.e., the via gets a little larger after etch by using the fixed 420 mJ/cm^2 data from both plots. As via CDs decrease with time, processes with no photo or etch bias will be required.

Via CD variation can also be affected by metal reflectivity in the same way metal CDs are affected, because they too are printed to the same type of metal grainy surface (see ARC section). If reflective notching is a problem at the preceding metal layer, it most likely will also be a problem at the via layer as well since the metal has not changed. In fact, studies on 1 μm vias cut to

metal requiring ARC demonstrated greater CD control when the ARC was also used at the via layer. The asymmetric notched via images with no ARC are found in Fig. 148 with the heavily notched via CD line aids, also printed with the via. After employing ARC at via, the reflective notch induced CD variability is reduced from between 27–37%, from separate studies.

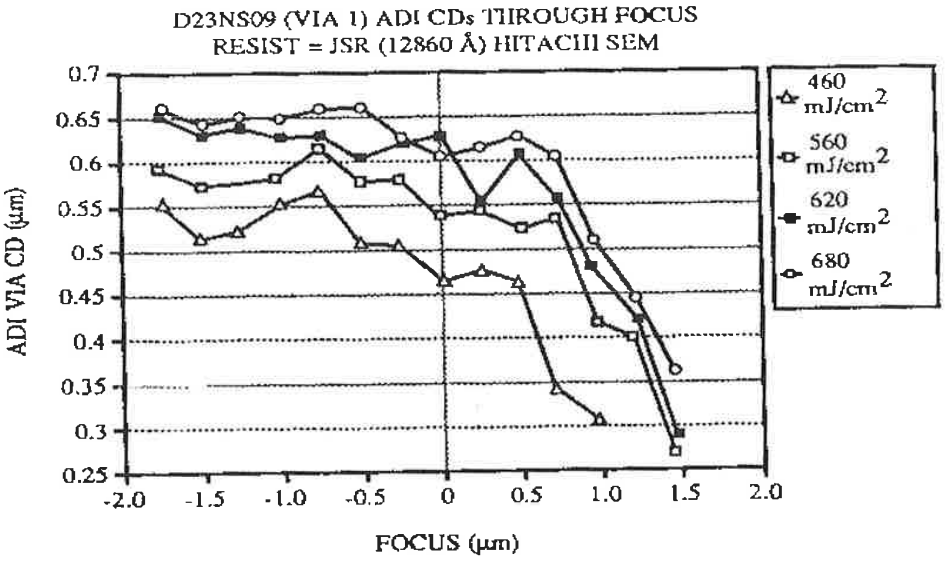


Figure 146. Via 1 CD vs. defocus for the JSR 500 process.

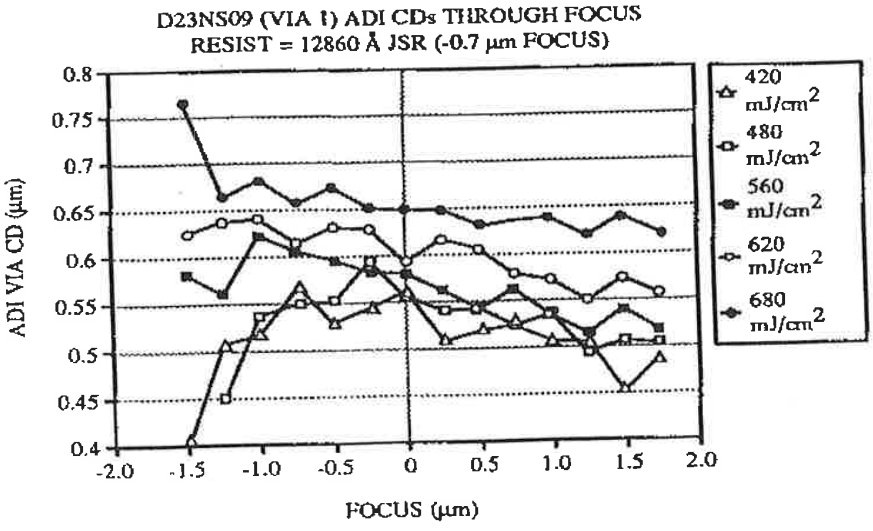


Figure 147. Via 1 CD vs. defocus for the JSR 500 process with -0.7 micron focus offset.

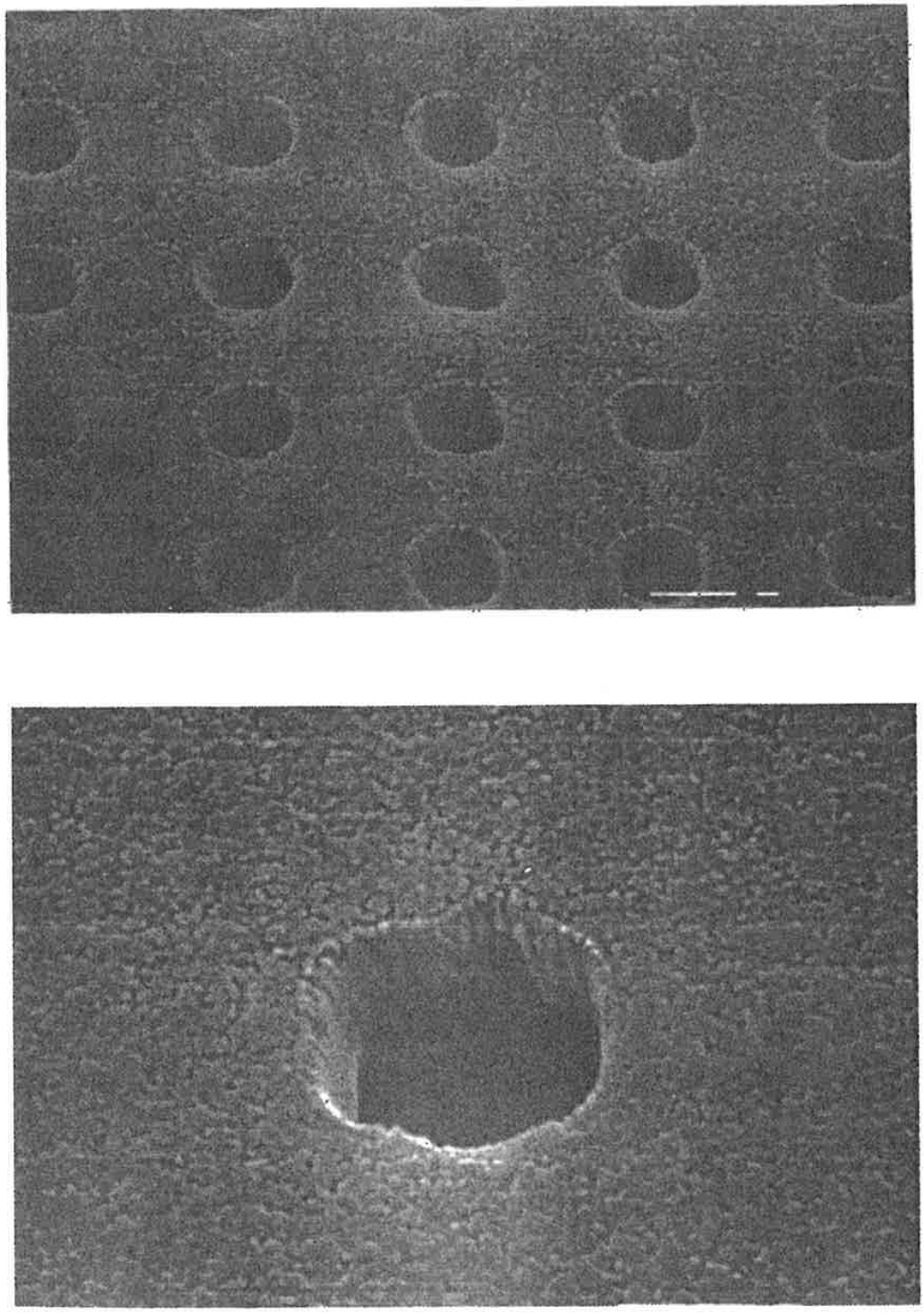


Figure 148. SEM micrographs of notched vias illustrating asymmetry vias that occurs without an ARC undercoating.

For smaller vias at 0.5 μm, CD variability can be as large as 0.13 μm (all families of variation for ten lots of real wafer data, 5 wafers/lot, 5 sites/wafer, 3-sigma), without ARC with the largest family of variation being wafer via site to site variation. This is really not too surprising because reflective notching does vary via to via as is seen in Fig. 148. By employing an ARC at via, that variation can be reduced to within the ±0.1 μm specification level. Vias printed with only resist exhibited "reflective notching dominated" CD 3-sigma variation of 0.10 μm greater, or double the specification, than that observed where an optimized ARC process was employed under the resist to minimize substrate reflectivity.

5.5 Summary and Future Predictions

The MLM photo processes of this section were basically for 0.8–0.7 Bipolar and 0.5 μm BiCMOS design rule technologies. With further design rule shrinkage to 0.35 μm and below, zero bias processes will be required. For example, the authors of Ref. 220 demonstrated 0.25 μm capability with an i-line stepper with oblique illumination combined with attenuated phase shift reticles, which is one of the easier phase shift techniques to employ. Of course, advances in phase shift technology processing and inspection must also occur before these technology goals can be achieved. Advances in DUV tool technology and phase-shift reticle technology are also pushing the frontiers of lithography and may eventually achieve 0.10 μm production lithography by the year 2000.

5.6 Future Processes

With the advent of the extension of optical lithography to shorter wavelengths and higher numerical apertures to resolution values approaching 0.1 micron and smaller, the future processing needs will surely be in the surface sensitive processing area, termed Desire processes.[221]–[223] This processing has considerable potential, because it would allow for relief of e-beam proximity effects and photolithographic bulk and focus tolerance effects.

The Desire-type processing allows thick SLR systems to be employed effectively as bilayers for RIE selectivity and bulk effect relief, and with no inter-layer mixing problems. Desire processing is accomplished by post HMDS treatment of the exposed photoresist to yield an in-situ silylated bilayer, and renders the system as a RIE bilayer system as opposed to the more typical lithographic bilayer systems. The system requires oxygen RIE development of the final image. It allows simplified processing over that

for conventional bilayer processes in that (1) the second resist spin and other top layer processing, (2) the top layer development, (3) the DUV flood exposure of the bottom layer, and (4) a subsequent separate development are eliminated and replaced by a high pressure HMDS treatment and RIE development. Obviously, Desire processes have an even greater advantage when DUV or EUV lithography are involved where thinner resists are involved and resist exposure penetration is limited.

Desire processing, like the other special processes of this section, possesses higher process contrast.[222][223] This is achieved because the process images only the thin top part at the top of the thick resist layer. Furthermore, all feature sizes can be written at nearly the same exposure level, and dye can be incorporated to provide reflective notching effect relief. The process is not without problems, however, as swelling effects have been observed and reported as early as 1988.

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